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ColdADC_P2: A 16-Channel Cryogenic ADC ASIC for the Deep Underground Neutrino Experiment

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***Abstract*— The second and final version of ColdADC, called ColdADC_P2, is presented. ColdADC_P2 is a 16-channel, 12-bit, 2 MS/s digitizer application-specific integrated circuit (ASIC) intended for use inside the DUNE Far Detector. ColdADC_P2 contains two 16 MS/s pipelined analog-to-digital converters (ADCs) that each digitizes the output of eight sample-and-hold amplifiers (SHAs). Because the application requires immersion in liquid argon (LAr), ColdADC_P2 was developed using specialized design techniques for long-term reliability in cryogenic environments and a customized cryogenic standard cell library. ColdADC_P2, with a die area of approximately 52.4 mm^2 and fabricated in 65-nm CMOS technology, achieves 130-μV rms noise performance and 11.8-bit effective-number-of-bits (ENOB) at a temperature of 77 K, with channel-to-channel crosstalk of <0.06% while dissipating 338 mW (21 mW per channel). Residual nonlinearity that is consistent with dielectric absorption in the capacitors internal to the ADC is corrected using a lookup table.**

***Index Terms*— Analog-to-digital conversion, cryogenic electronics, deep underground neutrino experiment (DUNE).**

I. Introduction

THE deep underground neutrino experiment (DUNE) is an international experiment for neutrino and proton decay studies [1]. DUNE consists of two large-scale neutrino detectors: The Near Detector at Fermilab and the Far Detector in South Dakota. The Far Detector will consist of four liquid argon (LAr) time projection chambers (TPCs), each with a volume containing approximately 17 kTon LAr total mass. ColdADC_P2 is designed to work together with two other application-specific integrated circuits (ASICs): a preamplifier (LArASIC) [2] and a digital data aggregator (COLDATA) [3]. Approximately 40 000 ColdADC_P2 ASICs will be used in the Far Detector complex and will spend the duration of the experiment immersed in LAr [4].

II. ColdADC_P2

ColdADC_P2 is a 16-channel, 12-bit, 2 MS/s digitizer. The first prototype of the ASIC, called ColdADC_P1 [5], was fully evaluated and successfully operated in a LAr time projection chamber (LArTPC). ColdADC_P2 was redesigned to correct several design errors, to improve performance, and to add a number of new features. To meet physics requirements, the primary goal of ColdADC_P2 is to achieve noise performance well below that of the preceding preamplifier ASIC, so the overall noise of the signal path is limited by the front-end preamplifier ASIC. Secondary requirements include good linearity and low crosstalk. Power dissipation is not a key concern, as long as it remains within the available cooling power of the detector cryostat. In fact, power dissipation was traded off in several areas to achieve lower noise or higher reliability. To facilitate prototype evaluation and testing, ColdADC_P2 was designed to be fully functional across a wide temperature range. It is intended to meet key requirements both at room temperature (290 K) and the target temperature (88 K).

A block diagram of ColdADC_P2 is shown in Fig. 1. The overall design was highly conservative to increase the chance of first-time functional success. The 16 analog inputs are organized in two banks of eight multiplexed sample-and-hold amplifiers (SHAs) each. The output of each SHA bank is then digitized by a self-calibrated 12-bit, 16 MS/s pipelined analog-to-digital converter (ADC). The ADC output is then formatted and serialized for transmission to COLDATA. All bias currents and reference voltages are generated using on-chip circuits.

The individual SHAs are implemented using switched-capacitor design techniques and have the ability to accept

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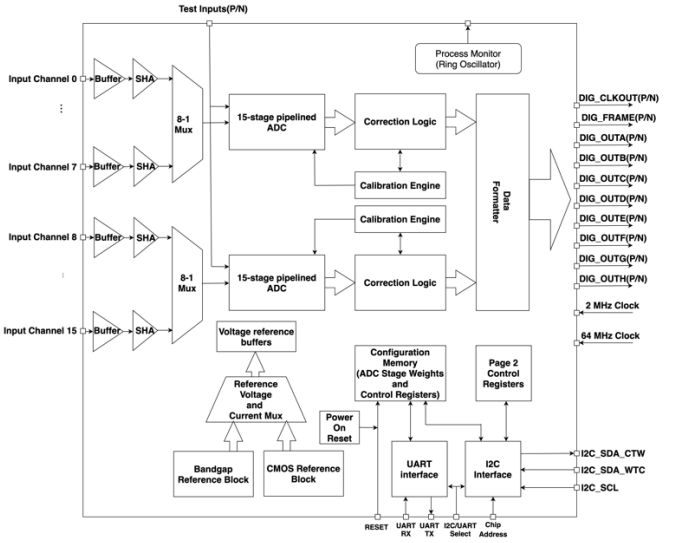

Fig. 1. Block diagram of ColdADC_P2.

either single-ended or differential inputs. The pipelined ADC in ColdADC_P2 uses a conservative design with digital self-calibration as discussed below. ColdADC_P2 outputs 16-bit words that are intended for truncation to 12 or 14 bits off-chip. Using ADC code lengths larger than 12 bits increases the resolution (and reduces quantization noise) but does not improve the linearity. The individual stages of the Pipelined ADC are scaled in area and bias current to minimize power dissipation.

To maximize the signal-to-noise ratio, thick-oxide devices were used to implement the analog circuits of ColdADC_P2. The use of thick-oxide devices allowed an internal differential voltage swing of 3 V which reduced noise for a given power dissipation relative to using thin-oxide devices with a reduced power supply voltage.

To mitigate design risk, a large amount of redundancy was included in ColdADC_P2. For example, two selectable voltage references, a bandgap reference and a reference based on the threshold of a CMOS transistor, are used to generate internal bias current and voltages. ColdADC_P2 can be configured using either of two slow control interfaces, one based on I2C and one based on a simple UART.

ColdADC_P2 is intended for operation without replacement for 30 years or more at cryogenic temperatures [1]. At cryogenic temperatures, the mobility of charge carriers is increased with respect to room temperature and a greater fraction of charge carriers can acquire enough kinetic energy to ionize silicon atoms. This “hot carrier effect” can limit circuit lifetime [6]. Therefore, good long-term reliability under temperature stress is critical to the success of ColdADC_P2. The DUNE Collaboration undertook extensive empirical studies of cold-temperature reliability of devices implemented in 65-nm CMOS technology [7]. These studies resulted in a set of design guidelines that were followed in the design of ColdADC_P2 to ensure long-term reliability. The key guidelines were to use a reduced power supply (10% below nominal) and to use transistor channel lengths at least 50% larger than the process minimum. In addition, a custom digital standard cell library was developed that embodies these design guidelines [3]. Custom cryogenic simulation models based on measured test structures were also used to ensure that the analog circuits in ColdADC_P2 were appropriately simulated [7].

As well as improved performance, ColdADC_P2 also introduced several new features, such as a power-on-reset capability to simplify operation, a ring-oscillator-based process monitor, and digital overflow and underflow protection.

III. ADC Calibration

After an extensive design study, the Pipelined ADC architecture was selected for ColdADC_P1 and ColdADC_P2 as it embodies a good balance between the requirements of noise, speed, linearity, and chance of first-time success. The ADC comprises 15 physical stages, and each stage has two decision levels (this is known as the 1.5 bit/stage architecture). The 1.5 bit/stage Pipelined ADC architecture is highly tolerant of comparator offset and the accuracy of the overall ADC is almost entirely dependent on the gain accuracy of the constituent stages [8]. When high-gain op-amps are used, the gain accuracy is primarily determined by capacitor matching. The linearity goal for ColdADC_P2 of less than one least-significant bit (LSB) at a 12-bit level is beyond the native capacitor matching capabilities of the CMOS process used for ColdADC_P2. While design approaches exist to allow pipelined ADCs to have linearity beyond the limits set by raw matching (e.g. the use of multi-bit front-end stages), these approaches lead to other compromises. In addition, there were not enough statistics available to determine whether the capacitor matching performance changed at low temperature. Therefore, the ADC in ColdADC_P2 employs a simple self-calibration that corrects for gain errors between stages. The calibration is entirely done internal to the chip and only requires the user to set a configuration bit to start the calibration process. While calibrating, the ADC ignores any analog input (it can still accept configuration commands). The calibration takes approximately 250 ms.

Each of the 15 ADC stages in ColdADC_P2 is implemented with a sample and hold, a three-level Flash sub-ADC, a three-level digital-to-analog converter (DAC), and a subtractor. The sample-and-hold, DAC, and subtractor circuits are combined into a multiplying DAC, or MDAC [8]. The MDAC for the calibrated stages of ColdADC_P2 is shown in Fig. 2. In this circuit, which uses a flip-around structure (capacitor C_F is used as both a sampling capacitor and feedback capacitor), either an input signal (the output of the previous stage) or a stage decision level (which is used as a calibration signal) can be sampled. The accuracy requirements of the calibration signal are relaxed because of the redundancy provided by the Flash ADC [9]. The uncalibrated stages share the same structure as the MDAC for the calibrated stages but omit the capability to sample the sub-ADC thresholds. The common-mode output voltage is stabilized using a switched-capacitor common-mode feedback circuit [10].

The calibration algorithm used in ColdADC_P2 indirectly measures the gain of the seven first stages in the ADC [11]. For each stage, it uses the remaining stages to measure the

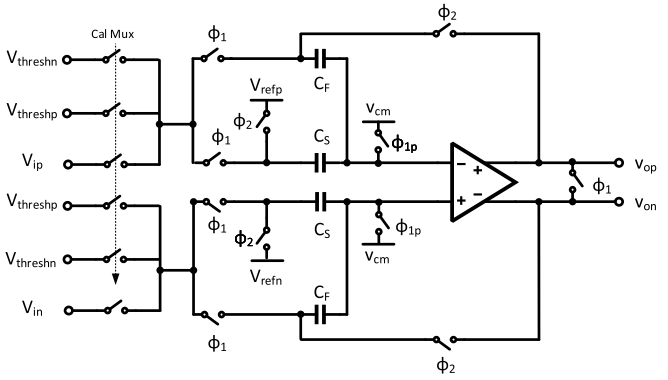

Fig. 2. ADC MDAC. Either the output of the previous stage or one of the sub-ADC decision levels can be used as the input. The calibration of the stages works by digitizing the decision levels as a test signal to estimate the stage gains.

jumps in that stage by setting the analog input to each decision level and forcing both decisions. This can be used to estimate the stage gains (one gain estimate is associated with the upper decision level and the other gain estimate is associated with the lower decision level). The algorithm then moves to the preceding stage and the process repeats. To ensure enough resolution in the measurement of the seventh most-significant stage (the first stage calibrated) the ADC comprises 15 physical stages (rather than the 11 nominally required to implement a 12-bit ADC). Because the MDACs that implement the least-significant stages are scaled in area and bias current, the additional stages required to improve the resolution of the calibration data dissipate little power and consume little area compared to the most-significant ADC stages.

The calibration algorithm provides a linear gain estimate, but is not able to correct for stage gain nonlinearity caused by low open-loop gain in the MDAC [12]. Therefore, the operational transconductance amplifiers (OTAs) used in the MDACs employ folded-cascode topologies with gain boosting to ensure high open-loop gain over the operating range of the amplifier [13].

One consequence of the calibration technique used here is the possibility of digital overflow (or underflow). Because the true gain of each stage may be more or less than two, it is possible that the final ADC output estimate is greater than the final resolution. In this case, the digital output will overflow when the analog input is near full scale, causing a gross error. What should be a large digital output (for instance) will appear as a small digital output (and vice versa). To deal with this issue, earlier implementations of this general calibration approach designed the stages for a nominal gain significantly less than two, and made sure the gain was reduced from two by more than the expected worst case error due to mismatch. While this was successful in eliminating overflow, it has the downside that by lowering the interstage gain, it increases the effective noise of downstream stages when referred to the ADC input. Because minimizing noise was the key requirement in this design, a digital overflow detector was included in ColdADC_P2 that monitors the ADC output codes and detects overflow. In case of overflow or underflow the monitor pins the output at the appropriate value.

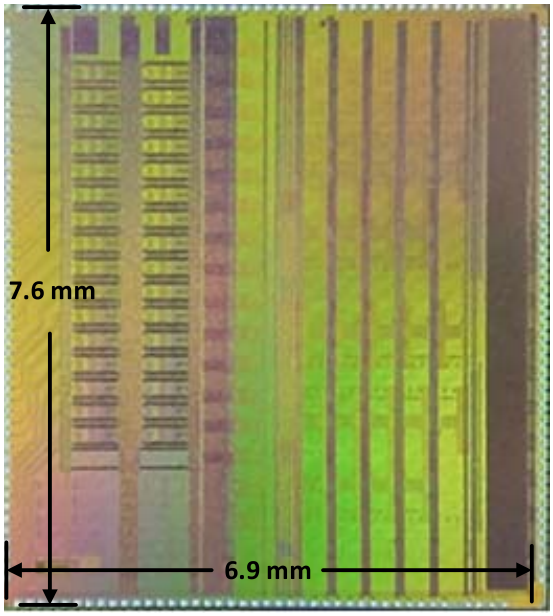

Fig. 3. ColdADC_P2 die photograph. The physical dimensions of the ColdADC_P2 die are approximately 6.9 mm by 7.6 mm. ColdADC_P2 is implemented in 65-nm CMOS technology.

IV. Prototype

ColdADC was implemented using 65-nm mixed-signal CMOS technology and fabricated at a commercial foundry. A die photograph of the 16-channel prototype is shown in Fig. 3.

To minimize coupling between digital and analog circuitry, most of the ColdADC_P2 sub-circuits are laid out in deep n-wells. There are four isolated power domains, as shown in Table I. All of the analog circuitry is powered by VDDA2P5 and resides in a single large deep n-well, with the local substrate connected to VSSA2P5. The digital circuitry that directly controls analog functional blocks is powered by VDDD2P5. It also resides in a single deep n-well, with its local substrate connected to VSSD2P5. Most of the rest of the digital circuitry (configuration registers, calibration and correction logic, clock generation, and the like) is powered by VDDD1P2. The digital core resides in its own deep n-well, with the local substrate connected to VSSD1P2. The LVDS drivers and CMOS drivers and receivers are powered by VDDIO and reside in separate deep n-wells, with each local substrate connected to VSSDIO. The pads, ESD protection diodes, and voltage clamps are not placed in deep n-wells. The protection diodes and voltage clamps are powered by VDDIO.

ColdADC_P2 is highly tunable under digital control. This is important because it allows the performance of the chip to be optimized at different temperatures and allows the chip to be tolerant of inaccuracies in simulation modeling. As the temperature decreases, the magnitude of the threshold voltage of the CMOS devices changes by approximately -1 mV/°C [14]. Therefore, the threshold will shift by about 200 mV from room temperature to LAr temperature. To optimize the performance across temperatures most of the key bias currents and voltages can be adjusted under digital control using on-chip DACs.

TABLE I
COLDADC_P2 POWER DOMAINS

Power Domain Name	Description	Value
VDDA2P5	Analog Power	2.25 V
VDDD2P5	ADC Digital Power (Logic & Switches)	2.25 V
VDDD1P2	Digital Logic Power	1.1 V
VDDIO	ESD Ring / CMOS I/O Power	2.25 V

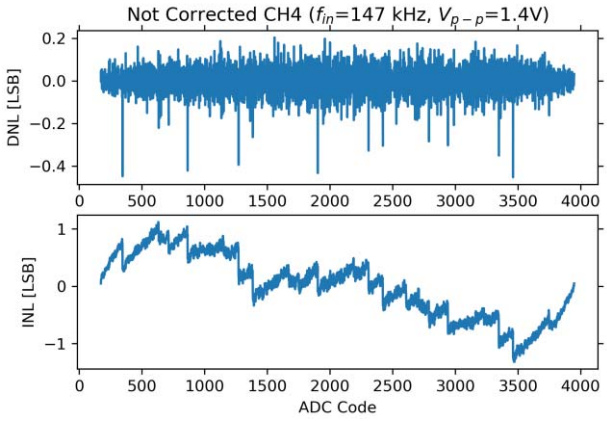

Fig. 4. Typical static nonlinearity of a ColdADC_P2 channel at 77 K (after calibration but without offline correction). The INL shows a marked polynomial shape that suggests it could be corrected with a cubic (or another odd-order polynomial).

V. DIELECTRIC ABSORPTION

The static linearity was measured both using slow ramps and sinusoids with identical results. We did not observe any missing codes after executing the on-chip self-calibration.

While the differential linearity (DNL) achieved by ColdADC_P2 was within expectations, the integral nonlinearity (INL) was larger in magnitude than expected and presented a characteristic shape that suggested a systematic cause. The measured raw DNL and INL of a typical channel after ADC self-calibration is shown in Fig. 4 (additional performance measurements are shown in Section VI). In each of these static linearity measurements, approximately 20 million samples of a single channel were captured and analyzed (other channels were biased at nominal dc levels).

The structure of the linearity shown in Fig. 4 could, in principle, be due to various sources. We conducted a number of experiments to narrow down the root cause. Increasing the bias currents in the ADC stages did not reduce the nonlinearity, ruling out an MDAC settling problem. We also observed that the linearity could be markedly improved by slowing down the ADC clock rate [15]. This eliminated capacitor nonlinearity as the explanation for the observed behavior. We also eliminated reference voltage transients as an explanation by adjusting the bias currents of the on-chip reference buffers. Decreasing the settling time of the buffers did not affect the observed linearity. Based on the elimination of these and other explanations, we believe the nonlinearity shown in Fig. 4 is consistent with the presence of dielectric absorption in the capacitors themselves [16].

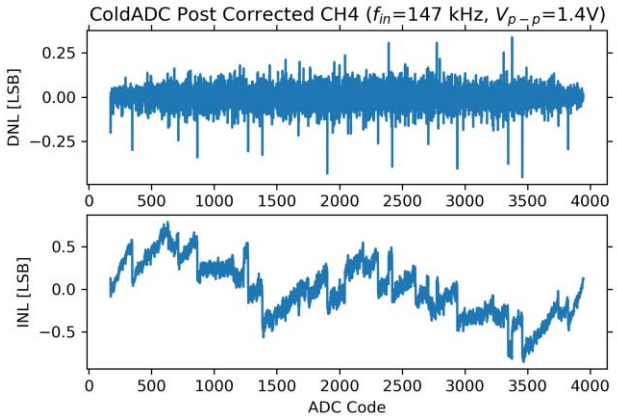

Fig. 5. Post-corrected static nonlinearity of a separate measurement (on a different day) of the same ColdADC_P2 channel from Fig. 4 at 77 K. The INL is improved here by the use of a third-order polynomial fit to the INL shown in Fig. 4.

The capacitors used within the switched-capacitor amplifiers internal to the ADC in ColdADC_P2 are implemented using metal–insulator–metal (MIM) structures. To increase capacitor density (and subsequently reduce die area) MIM capacitors are typically implemented using a high-k dielectric. A known characteristic of capacitors implemented using high-k dielectrics is the presence of dielectric absorption. Dielectric absorption is a phenomenon by which charged capacitors only partially discharge after being charged for a long time. In modern integrated MIM capacitors, this is typically a minor effect but can be observed at the 12-bit level [17].

Dielectric absorption is also called dielectric relaxation and capacitor soakage in the literature [18]. It is caused by the presence of multiple time constants in the discharge process of the capacitor and is related to surface states in the insulator [19]. Therefore, MIM capacitors with very thin dielectrics and that have a high surface-area-to-volume ratio can exhibit significant dielectric absorption [16].

Because dielectric absorption is a fundamental and repeatable characteristic of the capacitors used in ColdADC_P2, it is possible to correct it using a polynomial correction. The technique is to fit a polynomial to the INL shape and then generate a lookup table to cancel the INL and linearize the ADC output codes. We studied various polynomials and observed that while increasing the order of the fitting polynomial did improve performance, the improvement beyond the fitting of a cubic polynomial was minimal. The correction data are then used in a pre-computed lookup table.

The result of fitting a third-order polynomial to the INL of the ADC is depicted in Fig. 5 and using the data in a lookup table to correct new data taken by the same ADC channel on a different day (and after multiple temperature cycles) is shown in Fig. 5.

The structure in the linearity that is attributed to dielectric absorption is remarkably stable. We have found that the linearity correction is stable for at least several months (the time limit to nonlinearity stability is unknown, but in practice, the transfer function will be measured *in situ* from time to time). We have also found that the majority of the nonlinearity is consistent across chips. In other words, we have found that

the correction polynomial calculated for one channel in a given chip can be used to correct the linearity for the corresponding channel in a different chip. We also found that a correction polynomial calculated for data captured at 77 K can be used to correct data at 290 K (and vice versa). Although the efficacy of the correction is reduced in both cases, a large portion of the nonlinearity is still corrected. This is strong evidence that the nonlinearity is systematic and while it does not prove that the observed structure in the ADC linearity is due to dielectric absorption in the capacitors it is consistent with the theory.

Assuming dielectric absorption is the cause of the observed structure in the ADC linearity, a significant re-design of the ADC in ColdADC_P2 would be required to remove the effects of dielectric absorption from the ADC transfer function. One possible mitigation would be to implement a nonlinear ADC calibration algorithm, which would greatly increase complexity. Another option would be to move from the dense MIM capacitor currently used in the ADC to either a less-dense MIM capacitor available in the process (that has a lower surface-area-to-volume ratio) or to a metal–oxide–metal (MOM) capacitor that does not suffer from dielectric absorption. As either choice would significantly alter the capacitor area and routing requirements of the ADC, the layout would need to be designed again.

VI. Measured Results

ColdADC_P2 was fully functional at both room temperature (290 K) and 77 K and various measurements including noise, static and dynamic linearity, and crosstalk were made. While the target temperature is LAr boiling temperature (88 K), performance of ColdADC_P2 was evaluated at 77 K because of the convenience of using liquid nitrogen (LN_2) for cooling. The cold measurements were made at Lawrence Berkeley National Laboratory (LBNL), Fermilab National Accelerator Laboratory (FNAL), and Brookhaven National Laboratory (BNL). The tests at LBNL and BNL were made using a custom temperature-controlled cold box called the cold test system (CTS), developed at Michigan State University [20]. One important feature of the CTS is that it allows the device-under-test to be immersed in cryogen while the rest of the test board is at room temperature, simplifying testing. To ensure a smooth temperature transition and to keep the electronics free from condensation, heater strips are included on the test board. A photograph of the CTS and the overall cryogenic test setup at LBNL are shown in Fig. 6.

A photograph of the custom test solution developed at LBNL for use with the CTS is shown in Fig. 7. The motherboard is half-submerged in LN_2 within the CTS. The ColdADC_P2 is mounted on a daughtercard that is plugged into the submerged part of the motherboard. Heater strips included on the motherboard keep condensation away from the room temperature electronics on the top of the board. Single or differential signals can be plugged into connectors on the warm side of the board, limiting the number of cables required in the cold section. A CAPTAN + FPGA mezzanine board [21] allows high throughput data acquisition and connection to a computer through an Ethernet interface.

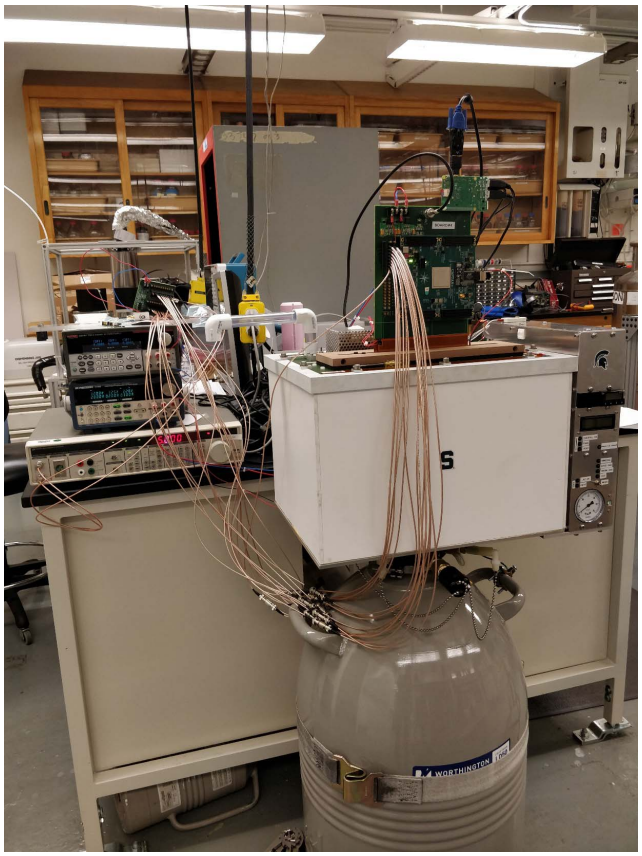

Fig. 6. ColdADC_P2 test setup at Lawrence Berkeley National Laboratory. The CTS is sitting on top of an LN_2 dewar. Half of the ColdADC_P2 test system is immersed in LN_2 while the other half is at room temperature (and visible in the photograph). Test equipment for measuring ADC performance is stacked to the left of the CTS.

A commercial Raspberry Pi board is used to control the system and ColdADC_P2 through a slow control interface.

The key performance requirement of ColdADC_P2 is noise. An idle channel test [22] was used to measure the noise of ColdADC_P2 and the results are shown in Fig. 8. In an idle channel test, the input of the channel is left floating or set to a dc level, and then the resulting ADC codes are collected. The variance of the ADC output codes is then interpreted as random noise. We performed the test both with the ColdADC_P2 input disconnected or connected to a filtered dc voltage with the same measured results.

By observing output codes generated by very slow input ramps, we confirmed that ColdADC_P2 does not exhibit any particularly noisy codes. The noise performance of the ADC was largely consistent across its input range.

A breakdown of the noise of ColdADC_P2 from the various contributors is shown in Fig. 9. The noise is dominated by the kT/C noise associated with the capacitors in the SHA and the first few stages of the ADC. The internal ADC references and reference buffers together add about 15% of the total noise.

An output spectrum from ColdADC_P2 at 77 K calculated using a fast Fourier transform is shown in Fig. 10. In this measurement, 14-bit ADC data were used (i.e., the ADC output codes were not truncated to 12 bits) and a single channel was converted with the other channels left disconnected. The measured low-frequency signal-to-noise plus distortion

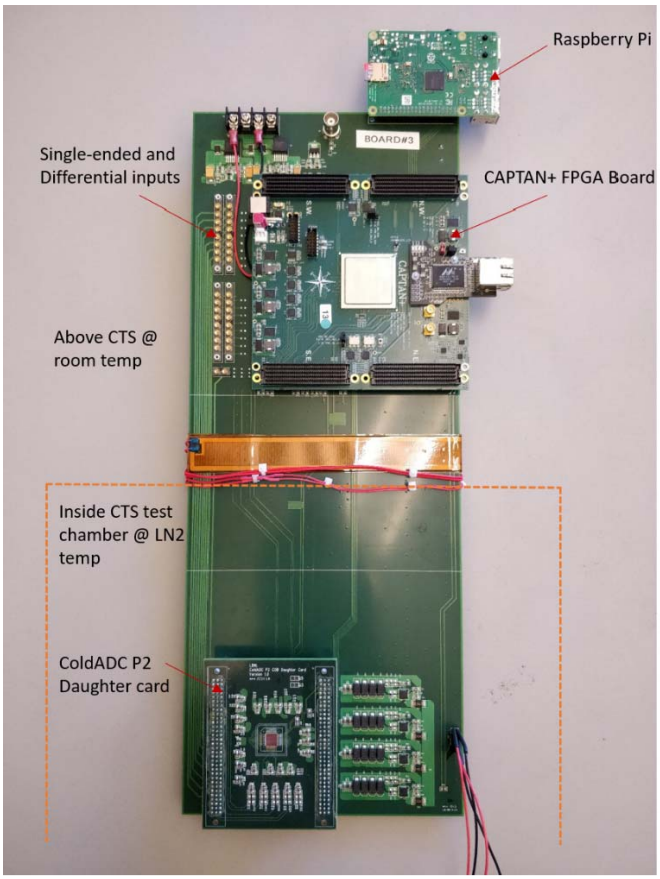

Fig. 7. Custom four-board cryogenic test solution developed at LBNL. The section in the dotted lines is immersed in LN_2 and the section outside the dotted lines is kept at room temperature.

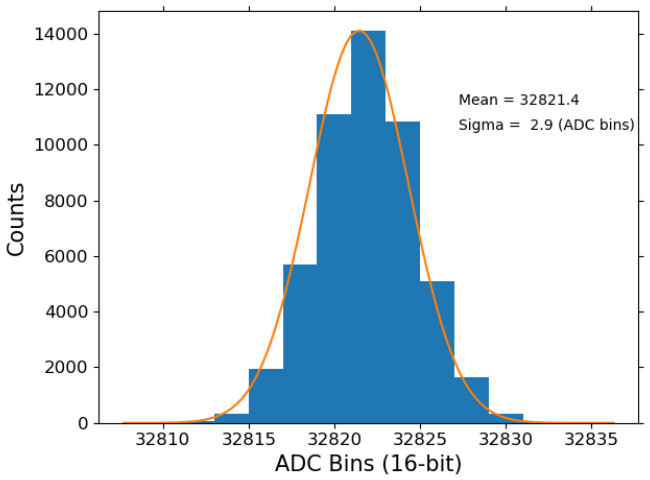

Fig. 8. Measured ColdADC_P2 noise performance with differential input for a typical channel at 77 K. The noise was measured here using the raw 16-bit outputs of the ADC to provide maximum resolution. The average measured noise is approximately 130 μV rms and varies less than 4% across channels.

ratio (SNDR) from this test is approximately 72.9 dB, giving an effective-number-of-bits (ENOB) metric of 11.8 bits. The low-frequency spurious-free dynamic range is about 82.1 dB. Truncating the data to 12 bits has the effect of increasing the quantization noise. In cases where the SNDR is limited by

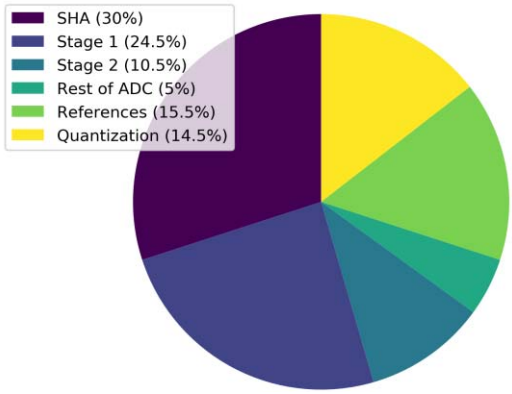

Fig. 9. ColdADC_P2 noise contributors at 77 K.

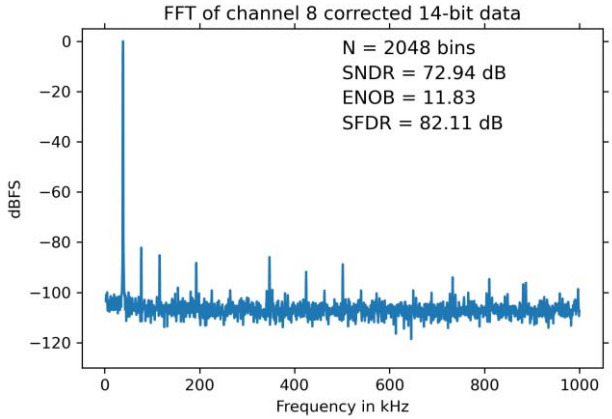

Fig. 10. Frequency spectrum of ADC output codes at 77 K after linearity correction. The input frequency is approximately 38.6 kHz.

nonlinearity, truncating has minimal effect. In cases where the ENOB is noise limited, truncating had more effect. In our measurements in situations where the ENOB was noise limited, we observed a reduction in ENOB of approximately 0.5 bit when we truncated 14-bit data to 12 bits.

The measured dynamic performance of ColdADC_P2 as a function of input frequency is shown in Fig. 11. The LArASIC preamplifier chip that will precede ColdADC_P2 has a -3 dB bandwidth of approximately 410 kHz (when the shortest shaping time of 0.5 μs is selected) [2], so ColdADC_P2 needs good dynamic performance up to about that frequency. The SNDR falls as a function of input frequency faster when the analog supply VDDA is set to its nominal value of 2.25 V compared to when it is increased to 2.5 V. This suggests that the biasing of the MDAC is not optimal at 2.25 V. Nevertheless, ColdADC_P2 exceeds its linearity requirements across the required input frequency range.

We compared the measured internal ColdADC_P2 calibration coefficients across temperature and found that the difference between warm and cold calibration coefficients for the same ColdADC prototype was approximately 0.2% for the most significant stage. The difference between warm coefficients for two different prototype ColdADC_P2 devices was about 0.3%. While we have low statistics, initial measurements suggest that the capacitor matching is not strongly affected by temperature, and the change in observed calibration

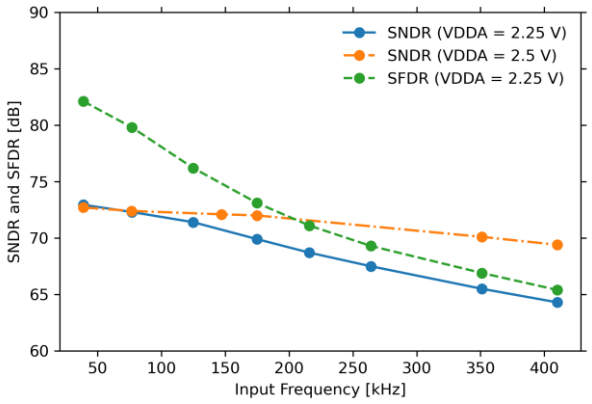

Fig. 11. Measured dynamic performance of ColdADC_P2 as function of input frequency at 77 K.

TABLE II
COLDADC_P2 POWER DISSIPATION AT 77 K

Power Domain Name	Description	Power Dissipation [mW]
VDDA2P5	Analog Power	286.0
VDDD2P5	ADC Digital Power (Logic + Switches)	11.9
VDDD1P2	Digital Logic Power	1.3
VDDIO	ESD Ring / LVDS / CMOS I/O Power	32.6
Total		331.8
Per channel		20.7

coefficients as the temperature is reduced is due to the expected increased open-loop op-amp gain at cold temperature.

An important requirement of ColdADC_P2 is low crosstalk. In ColdADC_P1, low-temperature crosstalk up to 0.5% was observed for adjacent channels. It was determined during the evaluation of ColdADC_P1 that the crosstalk was primarily caused by a bandwidth limitation in the analog multiplexer that is part of the SHA array (the circuit that allows eight analog channels to share a single ADC). This bandwidth limitation allowed kickback from the switched-capacitor sampling circuits to affect the next sample, leading to a memory effect. The multiplexer was redesigned to settle faster and the channels were re-routed in the layout with special care taken to avoid long parallel traces. The result of these efforts was a reduction in low-temperature crosstalk in ColdADC_P2 by almost an order of magnitude compared to ColdADC_P1. The channel-to-channel crosstalk measured in ColdADC_P2 for differential data at 77 K is shown in Fig. 12. The peak crosstalk was reduced from 0.5% in ColdADC_P1 to 0.06% in ColdADC_P2. The peak crosstalk was between the current channel and the next channel in the multiplexing cycle. The other channels exhibit much less crosstalk. This indicates the crosstalk performance is still limited by the bandwidth of the multiplexer. We also observed little effect from saturating a channel. The target crosstalk performance for ColdADC_P2 is <0.1% because below that level crosstalk does not need to be considered in the data analysis for the intended application in the DUNE experiment.

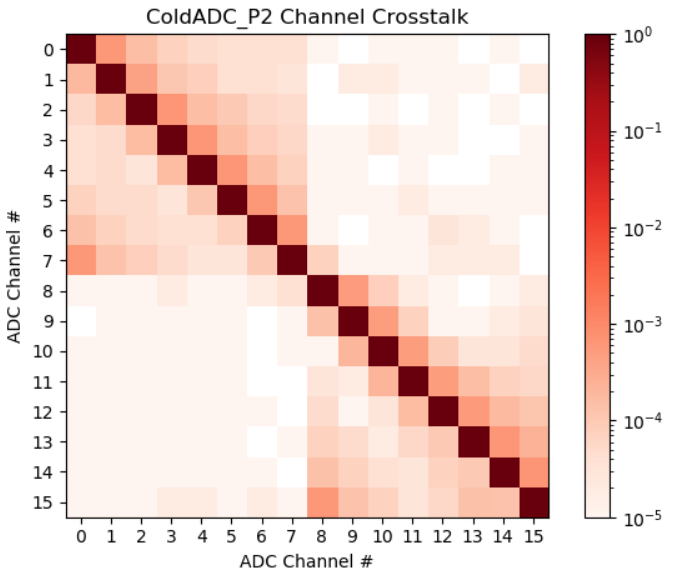

Fig. 12. Differential channel-to-channel crosstalk in ColdADC_P2 at 77 K.

TABLE III
MEASURED RESULTS

	290 K	77 K	Units
CMOS Technology	65	65	nm
Number of Channels	16	16	
Channel Sampling Rate	2	2	MS/s
ADC Resolution	12 or 14	12 or 14	bits
Full-Scale Range	3.0	3.0	V-ppdiff
Noise (input referred)	207	130	µV-rms
DNL (after dielectric absorption correction)	-0.3 / 0.4	-0.4 / 0.3	LSB (12-bit)
INL (after dielectric absorption correction)	-0.8 / 0.7	-0.7 / 0.6	LSB (12-bit)
Channel-to-Channel Crosstalk	0.35	< 0.06	%
SNDR	70.5	72.9	dB
SFDR	82.6	82.1	dB
ENOB	11.4	11.8	bits
Power Dissipation	371	332	mW
Die Area	52.4	52.4	mm^2

ColdADC_P2 dissipates approximately 332 mW (or 20.7 mW per channel) in a typical configuration (differential input mode) at 77 K. The key contributors to power dissipation at 77 K are shown in Table II. The majority of the power dissipation is in the VDDA2P5 domain that powers the thick-oxide analog circuits. The key driver for power dissipation in ColdADC_P2 is the need for large capacitors in the ADC stages and SHAs in order to lower the kT/C noise [23]. The power in ColdADC_P2 was reduced by over 20% compared to the power dissipation in ColdADC_P1. This was primarily achieved by design improvements that allow the analog circuits in ColdADC_P2 to be operated at a lower VDDA2P5 and VDDD2P5 than was possible in ColdADC_P1.

The performance of ColdADC_P2 is quite consistent across channels with measured noise variation of less than 4% across channels. The peak static linearity is uniform to within about 15% and the ENOB varies by approximately 0.5 bits.

The measured performance of the ColdADC_P2 prototype at room temperature (290 K) and a temperature of 77 K is summarized in Table III. For the 290 K measurements, the analog supply was set at 2.5 V, while for the 77 K measurements the analog supply was set at 2.25 V (its nominal voltage for reliability purposes). The increased power dissipation measured for operation at 290 K is due primarily to the higher nominal supply voltages.

VII. Conclusion

ColdADC_P2 meets or exceeds all requirements for the digitizer ASIC for the DUNE Far Detector. The ASIC has successfully demonstrated low-noise, high-linearity digitization at both room and cryogenic temperatures and has significantly reduced crosstalk compared to the previous version. Like ColdADC_P1, ColdADC_P2 was implemented using a conservative design style and published design guidelines for highly reliable long-term operation at cryogenic temperatures.

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