UNIVERSITY OF CALIFORNIA,
IRVINE

Low-Power Integrated Circuits For Biomedical Applications

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Electrical Engineering

by

Alireza Karimi Bidhendi

Dissertation Committee:
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2019

DEDICATION

To my parents whom their encouragement, moral support and unconditional love gave me strength to be the best of myself.

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ABSTRACT OF THE DISSERTATION

Low-Power Integrated Circuits For Biomedical Applications

By

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Doctor of Philosophy in Electrical Engineering

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Professor Payam Heydari, Chair

With thousands new cases of spinal cord injury reported everyday, many people suffer from paralysis and loss of sensation in both legs. Beside the healthcare costs, such a state severely deteriorates the patients' quality of life and may even lead to additional medical conditions. Therefore, there is a growing need for cyber-physical systems to restore the walking ability through bypassing the damaged spinal cord. This goal can be achieved by monitoring and processing patient's brain signals to enable brain-directed control of prosthetic legs. Among several existing methods to record brain signals, electrocorticography (ECoG) has gained popularity due to being robust to motion artifacts, having high spatial resolution and signal to noise ratio, being moderately invasive and the possibility of chronic implantation of recording grids with no or minor scar tissue formation. The latest property is of particular importance for the whole system to be a viable fully implantable solution. Furthermore, the implanted system has to operate independently with no or minimal need of external hardware (e.g. a bulky personal computer) to be individually and socially accepted.

To implement a fully implantable system, low-power and miniaturized electronics are needed to reduced heat generation, increase battery life-time and be minimally intrusive. These requirements indicate that many of the system's components should be custom-designed to integrated as much functionality as possible in a given real estate. This thesis presents

silicon tested prototypes of several building blocks for the envisioned system, namely, ultra low-power brain signal acquisition front-ends, a low-power and inductorless MedRadio transceiver, and a fast start-up crystal oscillator. Brain signal acquisition front-ends provide low noise amplification of weak ECoG biosignals. MedRadio transceiver enables communication between the implant and end effectors or base station (e.g. prosthetic legs or desktop computer). Crystal oscillator generates the reference signal for other system's components such as analog to digital converter. Novel techniques to improve important performance parameters (power consumption, low noise operation and interference resilience) have been introduced. Electrical, *in-vitro* and *in-vivo* experimental measurements have verified the functionality and performance of each design.

Chapter 1

Introduction

Brain-Computer Interface (BCI) systems have emerged as a multidisciplinary field with vast potentials and applications. BCI systems enable communication between brain and external devices, mainly computers to analyze and process the received time series data for multiple purposes including control of a prosthetic limb [1]. Among these applications, restoring the gait functions in patients suffering from spinal cord injury (SCI) has gained attention recently. This is due to the fact that there is no biological treatments available and the independence, quality of life and financial conditions of those affected are severely degraded due to SCI.

Despite the advances in BCI algorithms and signal processing, implementation of a miniature, portable, aesthetically acceptable system with long battery life remains a challenge. Recent works have proposed implementations using off-the-shelf components to evaluate the feasibility and operation of such systems [2–4]. However, any proposed solution to be clinically viable and widely accepted by the public need to have several important features: It has to be miniature in size, portable, low-power (to elongate battery life time and has low heat generation) and very high degree of accuracy to minimize safety risks.

Integrated circuits revolutionized the electronics and communication precisely because of their miniature scale that has made signal processing and significant computation power possible for consumer usage. This miniaturization also made circuits operate at increasingly higher speeds [8–10], enabling development of complex transceiver architectures [11–21] and wireless networks [5–7].

This work presents design, implementation and experimental results of three building blocks of the BCI system in complementary metal-oxide-semiconductor (CMOS) processes. Each design encompasses novel techniques to reduce power consumption, improve speed and data throughput, and provide low-noise operation. The summary of this thesis is as follows:

In the first chapter, two brain signal acquisition (BSA) front-ends incorporating two CMOS ultra-low power low noise amplifier arrays and serializers operating in MOSFET weak inversion region are presented [22]. To boost the amplifier's gain for a given current budget, cross-coupled-pair active load topology is used in the first stages of these two amplifiers. These two BSA front-ends are fabricated in 130 nm and 180 nm CMOS processes, occupying 5.45 mm^2 and 0.352 mm^2 of die areas, respectively (excluding pad rings). The CMOS 130 nm amplifier array is comprised of 64 elements, where each amplifier element consumes 0.216 μW from 0.4 V supply, has input-referred noise voltage (IRNoise) of 2.19 μV_{RMS} corresponding to a power efficiency factor (PEF) of 11.7 and occupies 0.044 mm^2 of die area. The CMOS 180 nm amplifier array employs 4 elements, where each element consumes 0.69 μW from 0.6 V supply with IRNoise of 2.3 μV_{RMS} (corresponding to a PEF of 31.3) and 0.051 mm^2 of die area. Non-invasive electroencephalographic (EEG) and invasive electrocorticographic (ECoG) signals were recorded real-time directly on able-bodied human subjects, showing feasibility of using these analog front-ends for future fully implantable brain signal acquisition and brain computer interface systems.

A MedRadio 413–419 MHz inductorless transceiver (TRX) for an implantable brain-machine interface (BMI) in a 180 nm CMOS process is discussed in the second chapter [23]. Occu-

pying 5.29 mm^2 of die area (including pad ring), this on-off-keying (OOK) TRX employs a non-coherent direct-detection receiver (RX), which exhibits a measured in-band noise figure (NF) of 4.9 dB and S_{11} of –13.5 dB. An event-driven supply modulation (EDSM) technique is introduced to dramatically lower the RX power consumption. Incorporating an adaptive feedback loop, this RX consumes 42/92 μW power from 1.8 V supply at 1/10 kbps data-rates, achieving –79/–74 dBm sensitivities for 0.1% bit-error-rate (BER). The TX employs a current-starved ring oscillator with an automatic frequency calibration loop, covering 9% supply-voltage variation and 15–78°C temperature range which guarantees operation within the emission mask. The direct-modulation TX achieves 14% efficiency for a random OOK data sequence at –4 dBm output power. Wireless testing over a 350 cm distance accounting for bio-signal data transfer, multi-user coexistence, and *in-vitro* phantom measurement results are demonstrated.

The last chapter presents a theoretical study and design of two techniques used to reduce start-up time (T_S) and energy (E_S) of Pierce crystal oscillator (XO) [24]. An analytical study of precise injection on a crystal resonator is introduced, and based on this study, a relaxation oscillator with a dithered frequency is designed. Next, a study of negative resistance of XO's active circuitry and a method to boost its value beyond the limit set by crystal static capacitor are presented. A gyrator-C active inductor with high linearity is developed to accelerate the start-up process by boosting the negative resistance. A prototype integrating these techniques is fabricated in a 180 nm CMOS process, and shows a significant improvement compared to prior art. Specifically, T_S and E_S are reduced by 102.7× and 2.9×, compared to the XO start-up with no assisting circuitry, to 18 μs and 114.5 nJ for a 48 MHz XO across -40–90°C temperature range. The measured steady-state power and phase noise of the XO are 180 μW and -135 dBc/Hz at 1 kHz offset frequency.

Chapter 2

Ultra Low-Power Brain Signal Acquisition Front-Ends

2.1 Introduction

It is estimated that every year there are ∼500,000 new cases of spinal cord injury (SCI) worldwide [25]. This condition substantially decreases independence and quality of life of those affected, and the resulting disability and comorbidities pose a significant economic burden on the individual as well as on society. Since there are no satisfactory means to restore motor function after SCI, novel approaches to address this problem are needed. Bypassing the damaged spinal cord by means of a brain-computer interface (BCI), which enables direct brain control of prostheses, constitutes one such approach. Non-invasive electroencephalogram (EEG)-based BCIs have the capacity to restore basic ambulation after SCI [26], [27], although their applicability is limited by the low information content (i.e., limited bandwidth and low spatial resolution) of EEG signals. Invasive BCIs, on the other hand, have enabled control of multi-degree-of-freedom robotic prostheses [28]. However, they utilize bulky and

power-hungry general-purpose recording hardware, and rely on skull-protruding electronic components. Furthermore, these systems typically employ intracortically implanted micro-electrode arrays, which can trigger foreign body responses such as inflammation and scarring, ultimately leading to failure of the system within months to few years [29]. These factors represent a serious obstacle to a widespread adoption of invasive BCI technology.

These problems may be addressed by developing a fully implantable BCI system that uses highly stable electrocorticogram (ECoG) signals [30]. Such a BCI system is envisioned to consist of ECoG electrodes, amplifiers, a processor, and a wireless module to control and communicate with output devices (e.g., prostheses), all implemented in a miniaturized form factor and operating in a low-power regime in order to facilitate permanent implantation. Since ECoG electrodes are placed above the arachnoid layer without breaching the neuronal tissue, ECoG signals have long-term stability [30, 31], while providing the spatiotemporal resolution necessary for high-performance BCI applications [32], [33]. In particular, studies have shown that the ECoG high-γ frequency band (70–120 Hz) exhibits spatially localized amplitude modulation that is correlated with individual's physical movements [34], and this feature has been used to decode arm [35] and finger movements [36]. Chronic *in vivo* recording of ECoG signals has been used for neurological treatment. The Medtronic Activa PC+S system [37, 38], was used in patients having Parkinson disease with ECoG electrode strips implanted over the motor cortex and depth electrodes in the subthalamic nucleus [39]. Chronic recordings from these areas were used to study the association between gamma band oscillations and dyskinesia. The Activa PC+S system was also used for recording signals from ECoG electrode strips over the motor cortex of a patient with amyotrophic lateral sclerosis (ALS) to facilitate BCI-control of a virtual keyboard [40]. Finally, as shown in prior art, a fully implantable system eliminates the need for bulky skull-protruding components, often employed in the state-of-the-art invasive BCIs, as well as bulky recording hardware and external computers.

There has been extensive research on low-power amplifier and amplifier array designs for neural signal sensing applications, which vary substantially in frequency and dynamic range. For example, in [41], the authors present a folded-cascode operational transconductance amplifier (OTA) using current-splitting and current-scaling techniques with a cascaded 6th-order band-pass filter for detecting epileptic fast ripples between 250 and 500 Hz. The stack of 4 transistors and large degeneration resistors in this design increase the required supply voltage to accommodate sufficient output voltage headroom. In [42], a closed-loop neural recording amplifier has been developed that utilizes a T-network in its feedback path in order to achieve high input impedance and common-mode rejection ratio (CMRR) within a small chip area. The authors argued that the T-network in the feedback path is useful when the routing area overhead, crosstalk and input-referred noise (IRNoise) do not dominate the performance [42].

Most of the previously developed neural sensing amplifiers focus on EEG or single-unit recordings. Consequently, their designs are not optimal for use in other recording modalities, such as ECoG. Moreover, a few studies that exist with analog front-end (AFE) designs for ECoG recording lack *in vivo* experimental validation in humans. For example, [43] presents a 32-channel integrated circuit (IC) for ECoG recording, followed by *in vivo* measurements in a rat. The power consumption of this system is too high, making it unsuitable for human ECoG signal acquisition, especially in a fully implantable form. In [44], an ECoG/EEG IC has been introduced which records signals in 4 different sub-bands as opposed to simultaneously capturing the complete ECoG spectrum. This IC has been validated by comparing the measurements of a pre-recorded human ECoG signal with those generated by a model of the signal acquisition chain. This approach, however, does not accurately capture the IC's interface with the body (e.g. 60 Hz noise), which may significantly affect the performance. When tested in an awake monkey, the signals simultaneously measured by this IC and those acquired using a commercial system showed only modest correlations in α (8–12 Hz) and high-γ (70–120 Hz) bands. This can be explained by the dominating effects of flicker and

thermal noise at these frequencies. On the other hand, the signals in the β (13–35 Hz) and low-γ (35–70 Hz) bands were only qualitatively compared with no correlation coefficients reported. Recent work [45] reports on an AFE consuming 1.08 μW of power per channel, which is achieved by narrowing the AFE bandwidth and filtering out the noise. A potential problem with this approach may lie in the high sensitivity of the designed G_mC filters to process variation. The proposed AFE has been tested in its ability to reproduce pre-recorded ECoG data and acquire ECoG signals *in vivo* from an anesthetized monkey. However, human testing and direct comparison of recorded signals to those acquired with a commercial-grade system have not been performed. Finally, the work in [46] presents a 64-channel wireless micro ECoG recording system with the front-end achieving a power-efficiency factor (PEF) that is 3× smaller than the state-of-the-art. *In vivo* measurements from an anesthetized rodent show the power increase with respect to the pre-sedation state in δ (1–4 Hz) and θ (4–7 Hz) bands, but very little change in BCI-relevant frequency bands. *Furthermore, none of the above systems were tested in a hospital environment, which is typically characterized by extremely hostile ambient noise and interference conditions.* In summary, while the development of these architectures has been inspired by human BCI applications, their *in vivo* testing in humans and comparison to conventionally acquired ECoG signals are conspicuously missing.

This paper presents the design, experimental validation, and comparative study of two CMOS ultra-low power (ULP) amplifier array and serialization circuitries that constitute core building blocks of two brain signal acquisition (BSA) front-ends. These BSA front-ends can act as the basis for a future, fully implantable ECoG-based BCI system (Fig. 2.1(a)). The AFE IC will be housed within an enclosure, called the skull unit, to be surgically implanted into the skull [47]. Other building blocks required to develop a complete ECoG-based BCI, e.g., transceiver, power management unit and digital signal processor are intended to be placed in another unit away from the patient's brain. This approach imposes less health hazards for the patient as well as more practical system specifications for a portable, user-

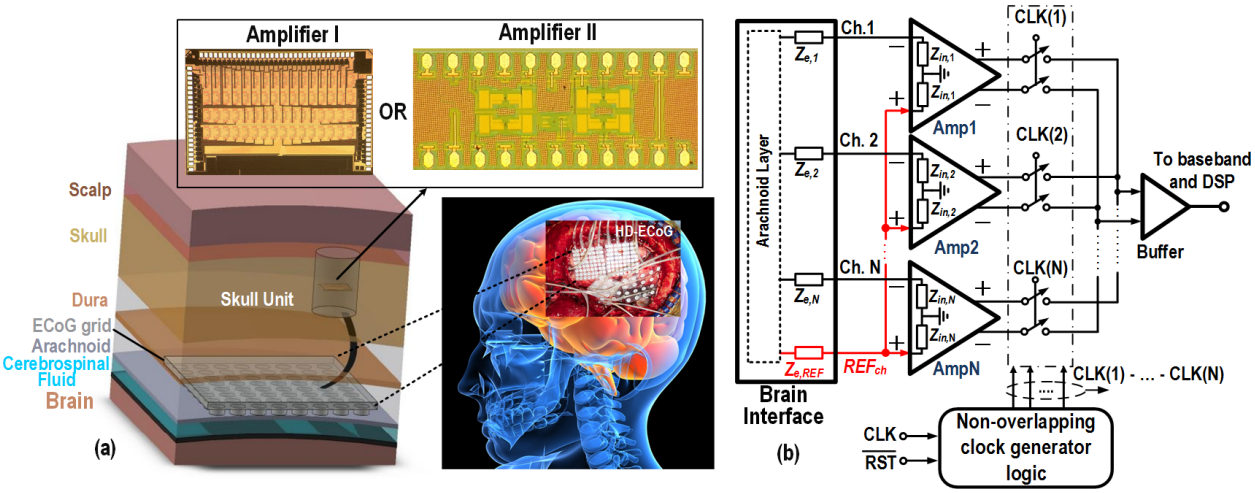


Figure 2.1: Proposed AFE: (a) A cross-sectional view of the envisioned fully implantable BSA circuit, enclosed within a skull unit module. The BSA circuit is connected to a subdurally implanted high-density (HD)-ECoG electrode grid that senses brain signals. (b) Block diagram of the structure showing the brain interface electrodes with their corresponding impedances and BSA comprised of an array of fully differential amplifiers, serializer and buffer.

friendly solution. All circuits in this work are designed to operate in the weak inversion (WI) region to maximize power efficiency and minimize heat dissipation, while maintaining high gain and low noise operation. *In vivo* human measurements and objective validation against a commercial bioamplifier are done in (1) a human subject using non-invasive EEG cap, and (2) a human subject with subdurally implanted high-density ECoG grid.

The paper is organized as follows. Section 2.2 presents the proposed AFE for recording ECoG signals and identifies the criteria and required specifications of the building blocks for designing the system. Sections 2.3 and 2.4 discuss the design and implementation of the two BSA front-ends, BSA I and BSA II, respectively. Section 3.6 illustrates the electrical and neural measurement results of both front-ends. Finally, Section 3.7 presents concluding remarks and potential extensions of this work.

2.2 Proposed System Architecture

Responsible for sensing and amplification of microvolt-level brain signals, the amplifier array IC is a critical building block of a BSA front-end. To be employed as a fully implantable device, the signal acquisition front-end should be small in size and consume micro-watt level of power. The system-level diagram of the proposed AFE is shown in Fig. 2.1(b) [48]. The AFE IC includes fully differential amplifiers, a serializer, and an output buffer all biased in the WI region. The outputs of the array are multiplexed in time to better facilitate input-output cable management by reducing the number of wires. The non-overlapping clock generator within the serializer generates N-phase clock signals, each with $1/N$ duty cycle. Non-overlapping clock signals ensure that only one amplifier is connected to the output buffer at a time during the channel switchover. This work presents two ULP BSA front-ends, BSA I and BSA II. BSA I provides symmetrical and complementary signal amplification paths to achieve energy-efficient low noise signal conditioning. BSA II is designed to achieve a high CMRR (i.e., better than 70 dB), thereby reducing the detrimental effect of power-line 60 Hz interference on the recorded signal.

Minimizing both noise and power dissipation imposes stringent design trade-off in an AFE for an implantable system, mandating meticulous considerations at every level of the design process. For example, at the device level, this notion implies that transistors should be designed to operate in a region which yields minimum power consumption for a given IRNoise imposed by minimum detectable ECoG signal power.

It is well-known that the MOS transistors in the WI region achieve maximum g_m/I_{DS}-ratio, resulting in the highest power efficiency at the cost of lower operation maximum bandwidth [49], [50]. Fig. 2.2 demonstrates g_m/I_{DS} and $log_{10}(I_{DS})$ variations with respect to V_{GS} for the two technologies given the same transistor sizes and bias conditions. Referring to Fig. 2.2(a), a higher subthreshold leakage current and a higher slope are observed in the

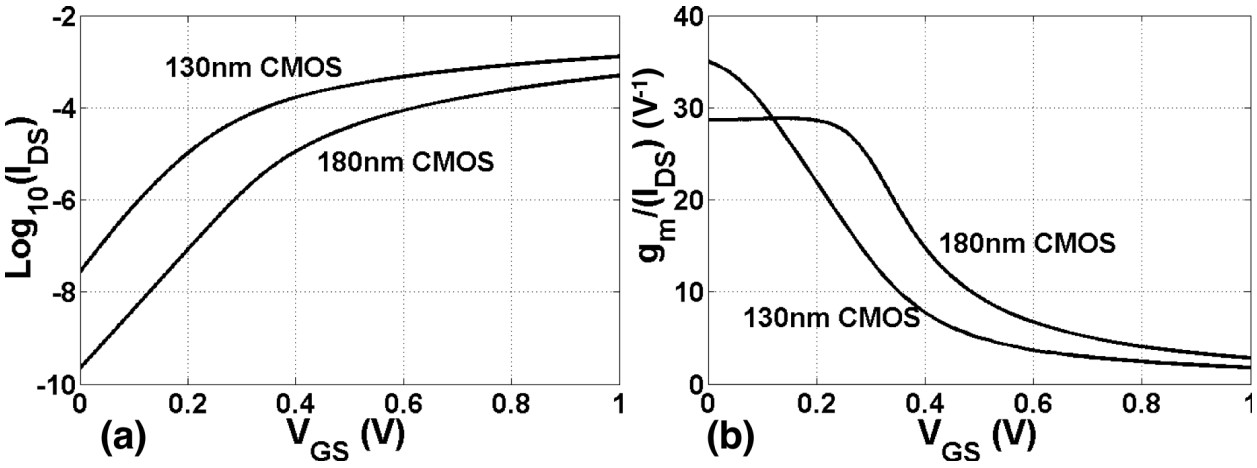


Figure 2.2: (a) Drain-source current (I_{DS}) vs. gate-source voltage (V_{GS}) for the two technologies. (b) g_m/I_{DS} vs. V_{GS} for the two technologies. W/L = 20μm/2μm with 10 fingers, V_{DS} = 1V for both transistors and body temperature of 37 is considered for simulation.

weak-inversion region for the 130nm process compared to the 180nm process. A higher slope corresponds to a larger g_m for the same bias current. This feature translates to a better power efficiency (Fig. 2.2(b)) and noise performance for transistors designed in this specific 130nm process. It is noteworthy that the g_m/I_{DS}-plot for the 130 nm CMOS process does not show the expected flat region in the deep subthreshold region. This is because BSIM4 device model was adopted for this process by the foundry. On the other hand, the 180 nm process employed PSP device model, which can predict the device behavior in deep subthreshold region more accurately.

ECoG signals typically have an amplitude of around 50–100 μV [51], with β and high-γ bands typically providing the most informative features for BCI applications [34]. The IRNoise of the AFE should be kept lower than the noise floor of the ECoG electrodes. Our recorded measurements using a commercial BCI signal acquisition equipment showed that the RMS noise floor, integrated over a frequency range of 8–200 Hz, is typically less than 10 μV_{RMS}, which is in compliance with the data reported in literature, e.g. [52]. Low noise operation is of particular interest for high-γ band, because the ECoG signal power becomes weaker with frequency [53].

The CMRR and power-supply rejection ratios (PSRR) should be large to attenuate the effect of environmental noise sources (e.g., 60 Hz power-line noise). Assuming an IRNoise level of $2\mu V_{RMS}$ in the presence of common-mode interference with 10 mV_{RMS}, a nominal 34 dB attenuation (i.e., 74 dB CMRR) is needed so that the output noise and interference voltage magnitudes are equal. In addition, the amplifier should show a high input impedance to lower the effect of common-mode interference. This attribute is especially important for multi-channel recordings since the impedance mismatch between electrodes ($Z_{e,1}$, ..., $Z_{e,N}$) as well as the mismatch between the impedance seen from the common reference input (parallel combination of $Z_{in,1}, ..., Z_{in,N}$ in Fig. 2.1) and $Z_{in,k}$ ($1 \leq k \leq N$) reduces the overall CMRR. Subdural electrodes' impedance have been reported (as well as measured) to be about 1 kΩ [30], thus the input impedance at the frequency of interest should be $\gg$ 1 MΩ [54]. Moreover, large DC offset associated with neural recording electrodes should be eliminated so as to minimize distortion or avoid saturation of the amplifier. Furthermore, electrical shielding and DC isolation are needed between the IC and implanted electrodes. Finally, the crosstalk in a multi-channel system should be mitigated to avoid contamination of the overall information recorded from different channels.

2.3 BSA I: An Array of 64 Amplifier I Circuits and A Serializer

BSA I incorporates 64 units of Amplifier I and a serializer, as shown in Fig. 2.1(b). Fig. 2.3 shows the general block diagram of the OTA used in the Amplifier I, composed of complementary NMOS-PMOS input stage. Intuitively, the signal is amplified by the transconductance gain of the input transistor pairs and subsequently applied to the current gain stage in each of the top and bottom branches ($A_{I,N}$ and $A_{I,P}$). Upon flowing through the load impedance Z_L, the summing current will generate the output voltage. Fig. 2.4(a) shows the top-level

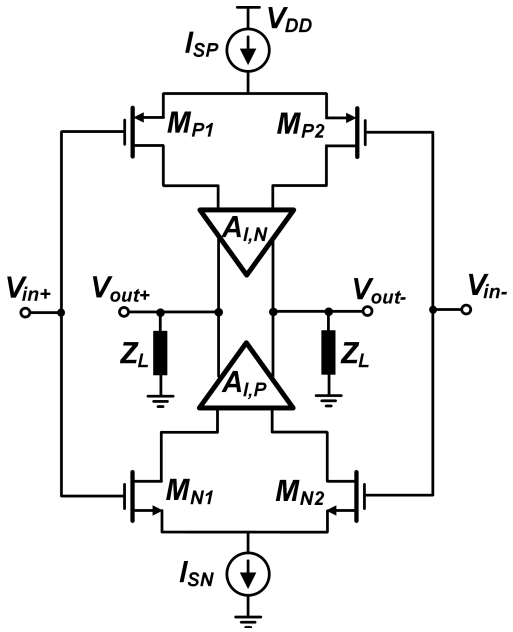


Figure 2.3: Complementary input structure of the OTA used in Amplifier I

topology of Amplifier I employing an OTA with an RC feedback network. The AC-coupled input provides DC rejection between the recording electrodes and the OTA input, thus providing a layer of electrical safety and isolation between the patient's brain and the amplifier. Fig. 2.4(b) depicts the transistor-level schematic of the OTA utilized in Amplifier I, including common-mode feedback (CMFB) circuitry (in gray) [47]. The OTA device sizes and aspect-ratios together with operating points of the individual devices are presented in Table 2.1. NMOS and PMOS transistors' body connections are tied to the ground and supply rails, respectively. The minimum headroom for a single transistor biased in the WI region is $\sim 4U_T$ (where $U_T \approx 26$ mV at room temperature) [55]. As a result, the OTA is biased at 0.4 V supply to mitigate large process variations resulting from WI operation, while achieving low power and low noise. The first stage employs a complementary NMOS-PMOS differential configuration with a complementary active load comprising parallel combination of diode-connected transistors and a cross-coupled pair [47, 56]. Cross-coupled pair and diode-connected transistors are identically sized as shown in Table 2.1, thereby having the same transconductance. The effective output resistance of the input stage is thus increased from

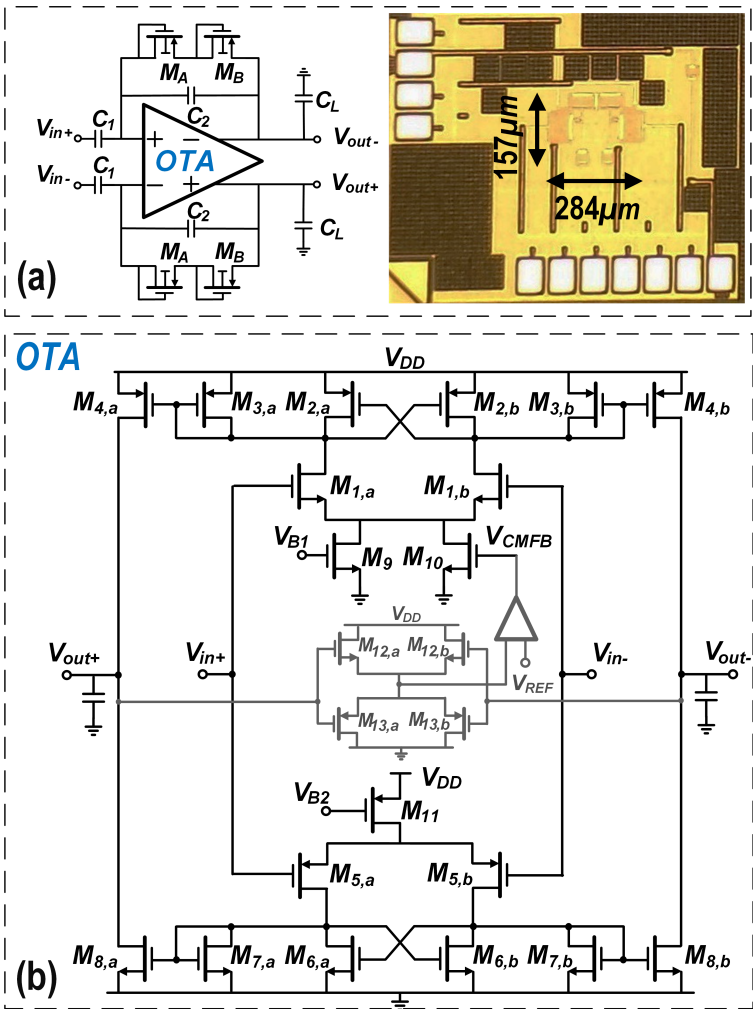


Figure 2.4: (a) Amplifier I comprising a closed-loop amplifier with capacitive feedback and its die microphotograph, and (b) the schematic of the complementary NMOS-PMOS OTA [47]

$\frac{r_{o3}}{1+g_{m3}r_{o3}}||r_{o1}$ (in the absence of cross-coupled pair load) to $r_{o1}||r_{o2}||r_{o3}$, where r_{o1}, r_{o2} and r_{o3} are the drain resistance of M_1, M_2 and M_3, respectively. The active-load devices are sized in a way that no instability or latch-up happens due to the process variation. The size of output transistors M_4 and M_8 are chosen to exhibit large drain resistance and low current consumption at the output stage.

The capacitance ratio C_1/C_2 ($C_1 = 20$ pF and $C_2 = 200$ fF) defines the closed-loop gain with high accuracy so long as the open-loop gain is sufficiently high. High output impedance of the OTA imposes a high impedance load for the feedback and next stage circuits. Pseudo-

resistors realized by transistors M_A and M_B (as in [57]) provide large equivalent resistance R of few GΩ, self-bias the input stage of the OTA without consuming any additional power for closing the loop, and set the lower 3-dB cutoff frequency ($f_L = (2\pi RC_2)^{-1}$). Compared to pseudo-resistor used in [58], this implementation provides a wider linear range of operation. Assuming all transistors are identically matched (to simplify the analysis), the IRNoise power spectral density (PSD) of the open-loop OTA ($\overline{V_{in,OTA}^2}$) is calculated to be:

$$\overline{V_{in,OTA}^2(f)} = \frac{4kT\gamma}{g_{m1}}\Big(1+\frac{2g_{m2}}{g_{m1}}\Big) + \frac{K_{p,1/f}}{C_{ox}(WL)_1}\frac{1}{f}\Big[1+2\frac{K_{n,1/f}}{K_{p,1/f}}\frac{(WL)_1}{(WL)_2}\big(\frac{g_{m2}}{g_{m1}}\big)^2\Big] \tag{2.1}$$

where k is the Boltzmann constant, γ, $K_{p,1/f}$ and $K_{n,1/f}$ are technology-dependent parameters, f is frequency, C_{ox} is the gate oxide capacitor, and T is the temperature. γ, the excess thermal noise factor, is slightly lower in the WI region than in the strong inversion (SI) [49]. Note that the complementary structure used in this OTA doubles the overall G_m. Flicker noise and mismatch effects are slightly attenuated by large input transistors and symmetrical circuit layout. In addition, dynamic compensation techniques such as chopper stabilization and autozeroing are commonly used to reduce the effect of amplifier offset and flicker noise [59–63]. However, these techniques require switches with low on-resistance to accommodate highly linear operation for autozeroing techniques and low residual input-referred offset voltage for chopping techniques. Thus, a high-swing on-chip clock needs to be generated at the

Table 2.1: Amplifier I device sizes and operating points

Devices	W/L (μm/μm)	I_D (nA)	g_m/I_D (V^{-1})
M_{1a}-M_{1b}	53.5/1.35	130	34
M_{2a}-M_{2b}	50/10	65	25
M_{3a}-M_{3b}	50/10	65	25
M_{4a}-M_{4b}	3.7/32	1.5	25
M_{5a}-M_{5b}	140/1.2	138	29
M_{6a}-M_{6b}	15/30	69	28
M_{7a}-M_{7b}	15/30	69	28
M_{8a}-M_{8b}	0.4/40	1.5	26
M_9	80/0.36	89	34
M_{10}	80/0.36	170	35
M_{11}	120/0.13	277	25

expense of high power consumption. Therefore, we have not used these compensation techniques in the current design. The IRNoise of Amplifier I in Fig. 2.4(a), $\overline{V_{in,tot}^2}$, is calculated to be:

$$\overline{V_{in,tot}^2(f)} = \big(4kTR + \overline{V_{in,OTA}^2(f)}\big)\big(\frac{f_L}{G_c f}\big)^2 + \overline{V_{in,OTA}^2(f)}\big(\frac{C_1 + C_2 + C_{in}}{C_1}\big)^2 \qquad (2.2)$$

where G_c is the midband closed-loop gain defined by C_1/C_2 and C_{in} is the equivalent input capacitance seen from the input of the OTA.

Sizing of the input transistors is critical due to existing trade-off between $\overline{V_{in,OTA}^2}$ and $\overline{V_{in,tot}^2}$. More precisely, large input transistors with low flicker noise will reduce $\overline{V_{in,OTA}^2}$. On the other hand, a larger device size leads to larger input capacitance, C_{in}, which adversely affects the system sensitivity. Another point to consider is that C_{in} shunts the gate of the input transistor to ground, causing a capacitive voltage division between C_1, C_2 and C_{in}. This, in turn, lowers the differential loop-gain, thereby preventing the closed-loop gain to be accurately defined. Moreover, as f_L decreases, the thermal noise contribution of the pseudo-resistors to $\overline{V_{in,tot}^2}$ is reduced, while the flicker noise contribution of the OTA to $\overline{V_{in,tot}^2}$ is increased.

The serializer in Fig. 2.1(b) is clocked at 64 kHz and is composed of a custom-designed 6-bit synchronous binary counter, a 6-to-64 decoder and 2×64 complementary pass-gate switches for selecting the amplifier channels. A reset signal puts the circuit in an initial state (channel 64) and the clock signal selects the channels sequentially [47].

Section 3.6 presents the measurement results of the BSA I, which was fabricated in a 130nm CMOS process [47].

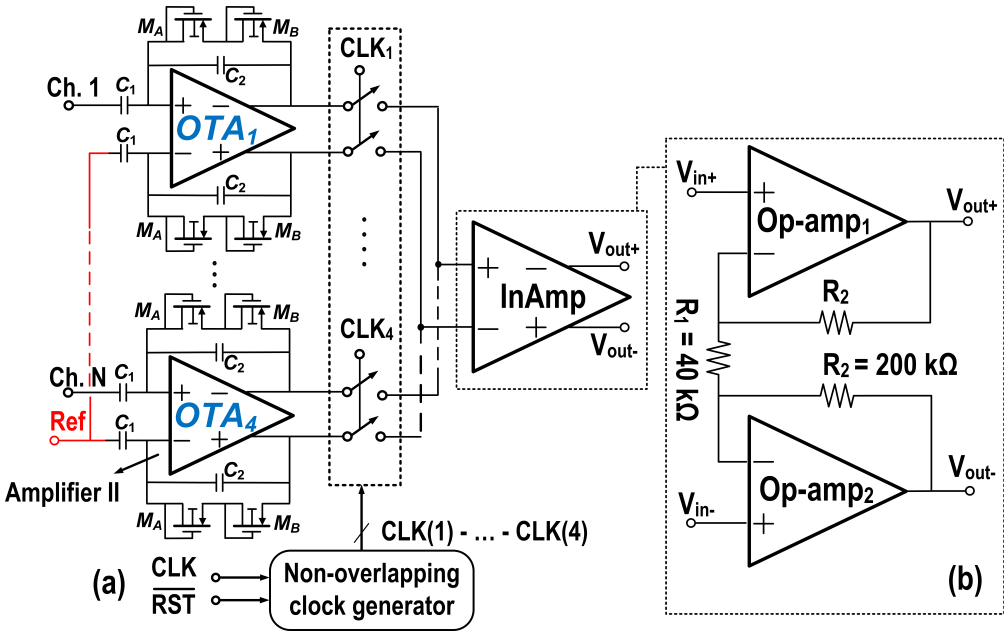


Figure 2.5: BSA II: (a) overall topology, including 4 Amplifier II circuits and one InAmp (b) InAmp implementation

2.4 BSA II: An Array of 4 Amplifier II Circuits, A Serializer, and an Instrumentation Amplifier

The existence of two signal paths in Amplifier I leads to a degradation in CMRR (≈60 dB). To further elaborate, suppose that the only existing mismatch is the one between each of the input pairs in Fig. 2.3 (i.e., Δg_{m_N} and Δg_{m_P}). This mismatch directly contributes to the common-mode to differential-mode gain for Amplifier I, which is derived as follows:

$$A_{cm-dm} \approx \frac{\Delta g_{m_N} \times A_{I_P} Z_{out}}{(g_{m_{N1}} + g_{m_{N2}}) Z_{S_N}} + \frac{\Delta g_{m_P} \times A_{I_N} Z_{out}}{(g_{m_{P1}} + g_{m_{P2}}) Z_{S_P}} \tag{2.3}$$

where Z_{out}, Z_{S_N} and Z_{S_P} are output impedances of Amplifier I, I_{S_N} and I_{S_P}, respectively. It is inferred from (2.3) that the CMRR of Amplifier I can statistically be degraded by a factor of 2 compared to an amplifier with a single path from the input to the output. A high CMRR is important in brain signal amplifiers due to the presence of a strong 60 Hz power-line noise in the amplification band. If not eliminated, major degradation in the output signal-to-noise

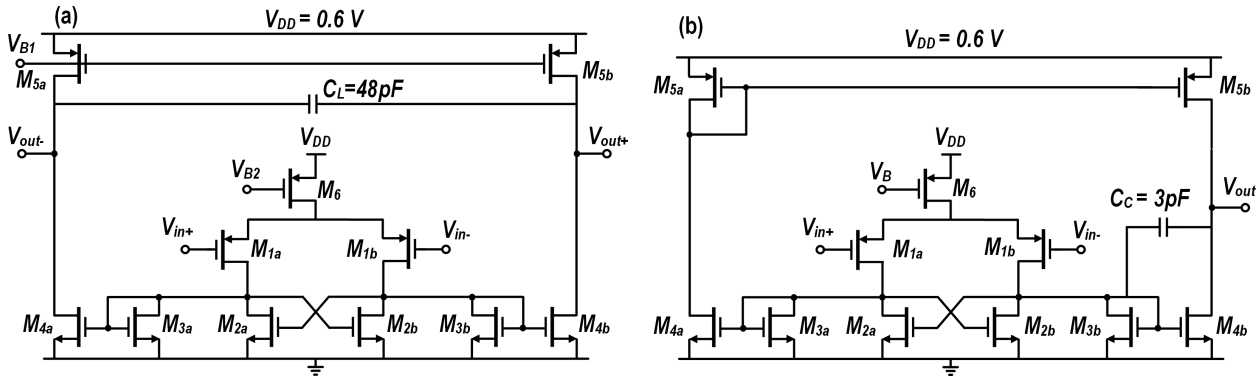


Figure 2.6: (a) OTA schematic used in Amplifier II (b) Op-amp schematic used in InAmp

ratio (SNR) will be seen. To further improve this feature, Fig. 2.5 introduces the block diagram of BSA II, which is composed of an array of 4 Amplifier II circuits, a serializer, and an instrumentation amplifier (InAmp). Similar to Amplifier I, Amplifier II is realized as a fully differential RC feedback circuit incorporating 200 fF feedback and 18 pF input AC-coupled capacitors. Matching accuracy of the feedback capacitor limits the achievable CMRR. For instance, it is readily shown that for closed-loop gain of 100 and 10% mismatch of the feedback capacitor, CMRR is lower than 60 dB. The open-loop OTA within Amplifier II employs PMOS input differential-pair with NMOS cross-coupled active loads, as shown in Fig. 2.6(a). Having one signal path from the input to the output relaxes the mismatch considerations present in complementary signal paths used in the first design.

The IRNoise of the open-loop OTA is calculated to be:

$$\overline{V_{in,OTA}^2(f)} = \frac{8kT\gamma}{g_{m1}}\Big(1+\frac{2g_{m2}}{g_{m1}}\Big) + \frac{2K_{p,1/f}}{C_{ox}(WL)_1}\frac{1}{f}\Big[1+2\frac{K_{n,1/f}}{K_{p,1/f}}\frac{(WL)_1}{(WL)_2}\big(\frac{g_{m2}}{g_{m1}}\big)^2\Big] \tag{2.4}$$

Assuming a single-pole frequency response, it is readily proven that the noise efficiency factor (NEF [64]) reaches a lower-limit of $2\sqrt{n\gamma}$ (where n denotes the subthreshold slope factor [55]) for both OTAs used in Amplifiers I and II if no dynamic compensation techniques are employed. The use of the same closed-loop architecture as in Amplifier I indicates that the IRNoise of Amplifier II is also expressed by (2.2).

The InAmp, after the serializer, provides further amplification and buffering to the output. It is commonly known that isolated resistive feedback circuitry (R_1 and R_2) provides flexibility in the design of an InAmp and its constituent open-loop op-amps with no concern of loading on preceding circuits [65]. In addition, any variation in R_1 is widely known to only contribute to the differential gain variation and will not increase common-mode to differential-mode gain (A_{cm-dm}) [66], [67]. Therefore, the CMRR is not degraded. As for the contribution of the mismatch between the R_2 resistors ($R_{2\Delta}$=R_2+ΔR) on CMRR, the InAmp's A_{cm-dm} induced by this mismatch is derived first:

$$A_{cm-dm} = \frac{E_{CM} - 1}{1 + \frac{R_{2\Delta}}{R_1 A_{dm2}} - \frac{R_{2\Delta}}{A_{dm1} R_1} E_{CM} + \frac{1}{A_{dm2}}} \tag{2.5}$$

where:

$$E_{CM} = \frac{1 + \frac{1}{A_{dm2}}\left(1 + \frac{R_2 + R_{2\Delta}}{R_1}\right)}{1 + \frac{1}{A_{dm1}}\left(1 + \frac{R_2 + R_{2\Delta}}{R_1}\right)} \tag{2.6}$$

In deriving Eq. (2.5), the open-loop gains of the op-amps, A_{dm1} and A_{dm2}, are assumed to be finite, while each op-amp exhibits negligible differential to common-mode gain. The common-mode gain A_{cm} of the InAmp is almost unity. If followed by a high-CMRR amplification stage, the contribution of A_{cm} on CMRR will be negligible. On the other hand, to reduce the impact of A_{cm-dm} on CMRR, the op-amps need to exhibit large open-loop gain. Large open-loop gain significantly reduces the contribution of R_2 mismatch on the CMRR. Ideally, if the op-amps are perfectly matched ($A_{dm1} = A_{dm2}$), A_{cm-dm} would become zero regardless of ΔR value.

Amplifier II and the InAmp are DC-coupled, eliminating the need for large coupling capacitors. Considering a 39-dB gain for the OTA, the expected differential input amplitude of the InAmp is less than 9 mV, which falls within the input common-mode range of InAmp (0 to $V_{DD} - 2V_{DS,sat}$ where $V_{DS,sat}$ is the drain-source saturation voltage).

Figs. 2.6(a) and (b) show the transistor-level schematics of the OTA used in Amplifier II

and the op-amp used in InAmp, respectively. Both amplifiers use similar topology while the devices are sized according to the performance specs needed from each circuit, namely, low noise and high transconductance for the OTA (high driving power and high voltage gain for the op-amp). Tables 2.2 and 2.3 show device sizes and operating points for the OTA and the op-amp, respectively. All transistors are biased in WI to maximize power efficiency. To achieve a maximum ECoG bandwidth of 200 Hz in the OTA and avoid out-of-band noise accumulation, a large 48 pF capacitor C_L is placed differentially at the output. The input transistors operate in deep WI to maximize their g_m/I_D-ratio so as to reduce the IRNoise contributions of active-load devices (M_{2a} – M_{2b} and M_{3a} – M_{3b}). PMOS transistors are used in the input differential pair to have a lower flicker noise. Furthermore, the use of a PMOS input pair for the op-amp makes common-mode levels of the OTA output and the op-amp input compatible, thereby making it possible to DC-couple the two. DC-coupling eliminates the need for large decoupling capacitors as well as biasing circuitry of the op-amp inputs. The OTA bandwidth and stability are determined by its output stage where the dominant pole is located. On the other hand, the op-amp's dominant pole is located at its first stage's output node, as its output stage should provide high current drive capability. The op-amp is thus Miller-compensated and its bandwidth is chosen to be $\approx$ 800 Hz in order to accommodate 4 recording channels.

Fig. 2.7 shows the proposed CMFB circuit to set the output common-mode voltage of the OTA. The drain currents of transistors M_{4a} and M_{4b} are steered to ground or to transistor M_6 depending on common-mode level of V_{in}. M_{3a} and M_{3b} mirror M_6, sinking current from

Table 2.2: Amplifier II device sizes and operating points

Devices	W/L (μm/μm)	I_D (nA)	g_m/I_D (V^{-1})
M_{1a}-M_{1b}	152/0.18	510	27
M_{2a}-M_{2b}	12.8/20	255	20.7
M_{3a}-M_{3b}	12.8/20	255	20.7
M_{4a}-M_{4b}	0.8/25	27	16.6
M_{5a}-M_{5b}	16/12	67	22.9
M_6	192/1	1020	27

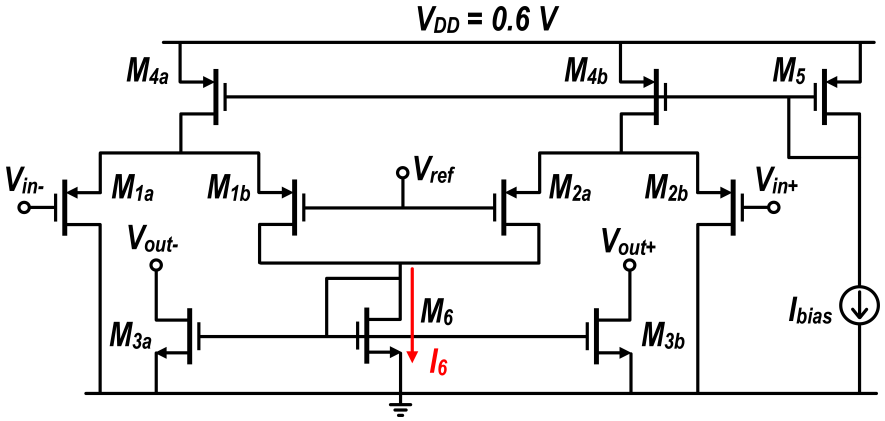


Figure 2.7: CMFB circuit used in Amplifier II

the OTA's output stage, thereby adjusting the OTA common-mode level. Note that the input and the output of the CMFB are physically connected together. The CMFB output currents are expressed as:

$$I_{3a} = I_{3b} = \frac{W_3}{W_6} \times g_{m1,2} \times \left(\frac{V_{in+} + V_{in-}}{2} - V_{ref}\right) \tag{2.7}$$

where $g_{m1,2}$ denotes the transconductance of $M_{1a} - M_{1b}$ and $M_{2a} - M_{2b}$, W_3 is channel width of $M_{3a} - M_{3b}$, and W_6 is M_6 width. Input transistors ($M_{1a} - M_{1b}$ and $M_{2a} - M_{2b}$) should remain in saturation region for proper operation of the CMFB. Having few millivolts swing at the OTA's output ensures that no transistor leaves saturation. Transistors M_{3a} and M_{3b} are designed to have long channel length, with negligible loading effect on the OTA. Their parasitic capacitances are absorbed in the OTA's load capacitor. The simulation of the CMFB shows a current consumption of 24 nA and a common-mode phase margin of at least 35°.

Table 2.3: Op-amp device sizes and operating points

Devices	W/L (μm/μm)	I_D (nA)	g_m/I_D (V^{-1})
M_{1a}-M_{1b}	100/0.18	80	29
M_{2a}-M_{2b}	1/5	40	21
M_{3a}-M_{3b}	1/5	40	21
M_{4a}-M_{4b}	8/5	320	21
M_{5a}-M_{5b}	32/4	320	21
M_6	200/1	160	28

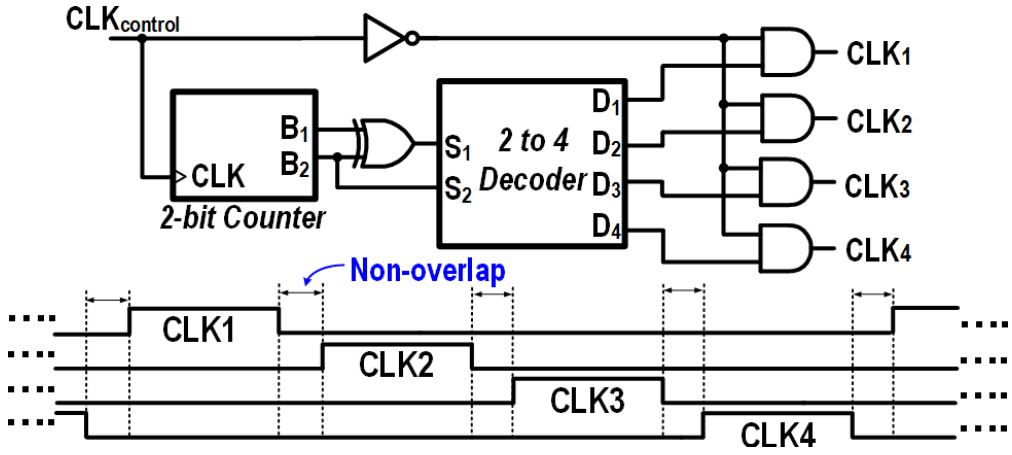


Figure 2.8: Non-overlapping clock signals applied to serializer switches

The circuitry for the serializer logic used in BSA II is presented in Fig. 2.8. This logic contrives i) non-overlapping clock signals for time-multiplexing, and ii) a gray-coding scheme for a 2-bit binary counter to eliminate race conditions. The serializer clock signal's duty-cycle produces temporal spacing between clocks applied to the serializer switches (Fig. 2.8). A Gray-code converter is used to convert binary code to Gray code such that the counter exhibits no race condition, which could otherwise result in sparks in the 2-to-4 decoder in Fig. 2.8. A T-network switch is used for channel selection in this serializer to provide large input-output isolation and minimize the effects of charge-injection and clock-feedthrough.

2.5 Measurements

The functionality of BSAs I and II was verified by electrical and *in vivo* measurements. The EEG test verified the functionality of Amplifiers I and II to detect weak signals in the presence of environmental noise. BSA II was further tested in a hospital environment on a patient who underwent ECoG grid implantation over the motor cortex area. It was experimentally shown that BSA II was capable of recording signals with high output SNR and comparable performance with respect to a commercial EEG acquisition unit, while consuming orders of magnitude less power.

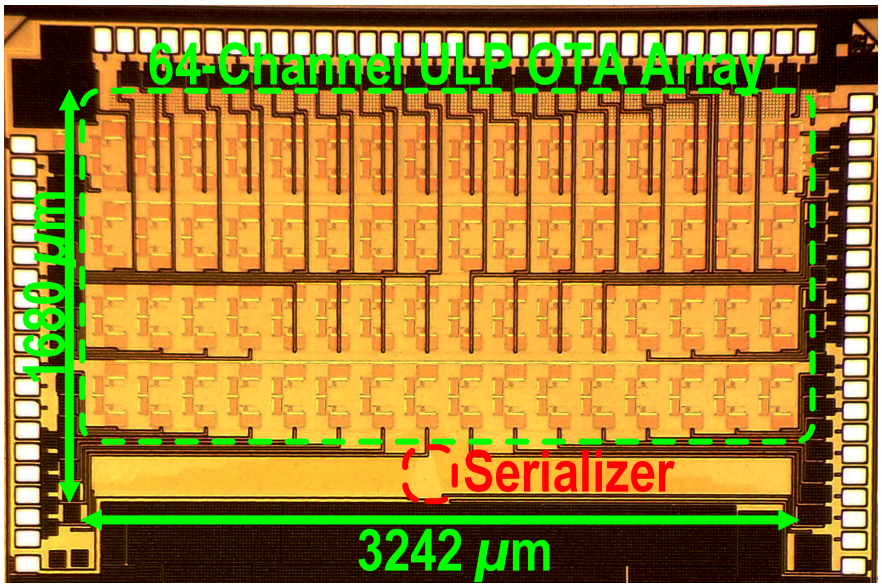


Figure 2.9: Die microphotograph of BSA I with 64-channel amplifier array and serializer [47]

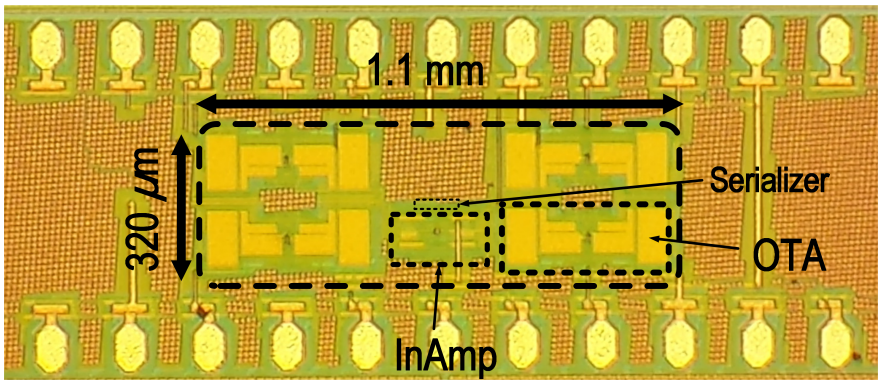


Figure 2.10: Die microphotograph of the BSA II with 4-channel amplifier array and serializer

2.5.1 Electrical Measurements

Amplifiers I and II were fabricated in 130nm and 180nm CMOS processes, occupying 0.044 mm^2 / 0.052 mm^2 die areas, and consuming 0.216 μW / 0.69 μW from 0.4 V / 0.6 V externally provided supply voltages, respectively. Figs. 2.9 and 2.10 show die microphotographs of BSA I and BSA II front-end circuits. The first chip (BSA I) occupies 5.45 mm^2, and the second chip (BSA II) occupies 0.352 mm^2 (excluding pad rings). The pad ring incorporates a 2 kV HBM ESD protection circuitry with negligible leakage current. BSA I prototype uses an off-chip buffer to drive commercial signal acquisition unit (MP150 with 12-bit ADC, Biopac

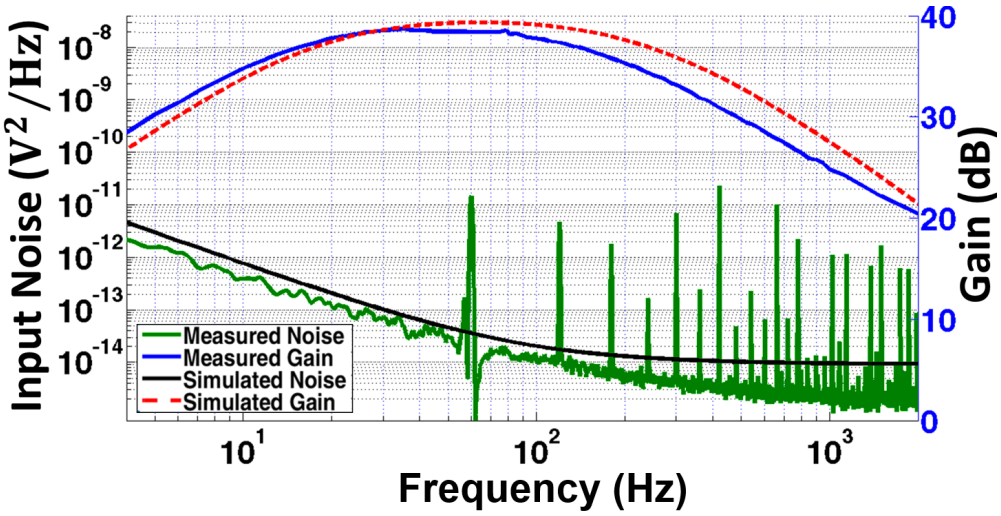


Figure 2.11: Measured and simulated Amplifier I gain and noise responses. Note that the sharp peaks were due to 60 Hz harmonics on the unshielded cables [47].

Systems Inc., Goleta, CA) [47]. The overall amplification gain for the two AFEs have been measured using Agilent 33250A waveform generator and SMA attenuators, each providing 39 / 58 dB voltage gain and IRNoise of ∼2.19 / 2.3 μV_{RMS} across 12–190 Hz / 2–175 Hz of operation bandwidth, respectively (Fig. 2.11 and 2.12). Without explicit calibration scheme, the lower-cutoff frequency is not well controlled across process corners. In this work, this frequency was chosen to be smaller than the 8-Hz corner frequency of α-band with negligible effect on noise performance. Simulations show that this lower-cutoff frequency varies from 2 to 10 Hz across process corners. The 60 Hz interference and its harmonics were removed from the noise plot and calculations in Fig. 2.12. Linearity and noise measurements were done using Agilent E4448a spectrum analyzer. A low noise off-the-shelf instrumentation amplifier (AD620) was used to boost the noise level and drive the spectrum analyzer. The calculated dynamic range of the Amplifier I at 37 Hz for ∼1% Total Harmonic Distortion (THD) was 58 dB. The Amplifier II harmonics for 0.2 mV input voltage at 47 Hz (which is 2 times higher than the expected neural signal amplitude) was lower than the measured noise floor, indicating linear operation. For 150 mV_{pp} signal at 60 Hz, Amplifier I / II exhibits a CMRR greater than 60 dB / 74 dB and a PSRR greater than 58 dB / 70 dB, respectively. Table 2.4 provides the performance summary of the designed amplifiers and comparison with

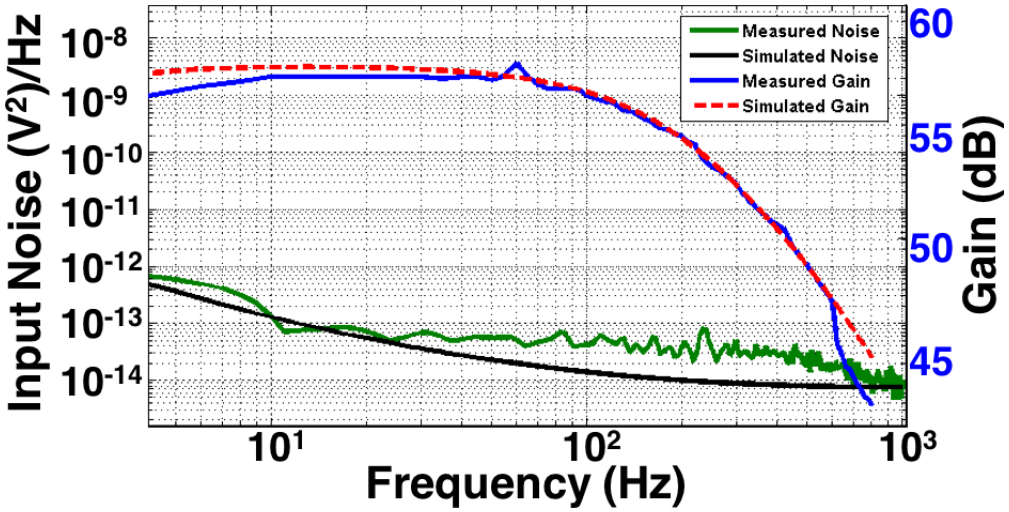


Figure 2.12: Measured and simulated gain and noise responses for a single channel of BSA II

prior art from academia and industry.

2.5.2 Human Neurological Measurements

This study was approved by the Institutional Review Boards of the University of California, Irvine and the Rancho Los Amigos National Rehabilitation Center, and is considered non-significant risk. Three human subjects provided informed consent to participate. The chip was powered by a current-limited (2 mA) supply source. The hospital instruments were disconnected to avoid creation of any unwanted electrical loop. The AC-coupled connection between the electrodes and the amplifiers provides DC isolation.

EEG

For two healthy subjects (male, 26 and 27 years old), the impedances of electrodes AFz, Cz, Pz, and Oz in the 10/10 EEG system [68] were reduced to < 3 kΩ using conductive gel. Measurements were performed on one of the subjects using Amplifier I, as follows. EEG from Cz, Pz, and Oz (all referenced to AFz) was recorded at 2353.2 Hz per channel using

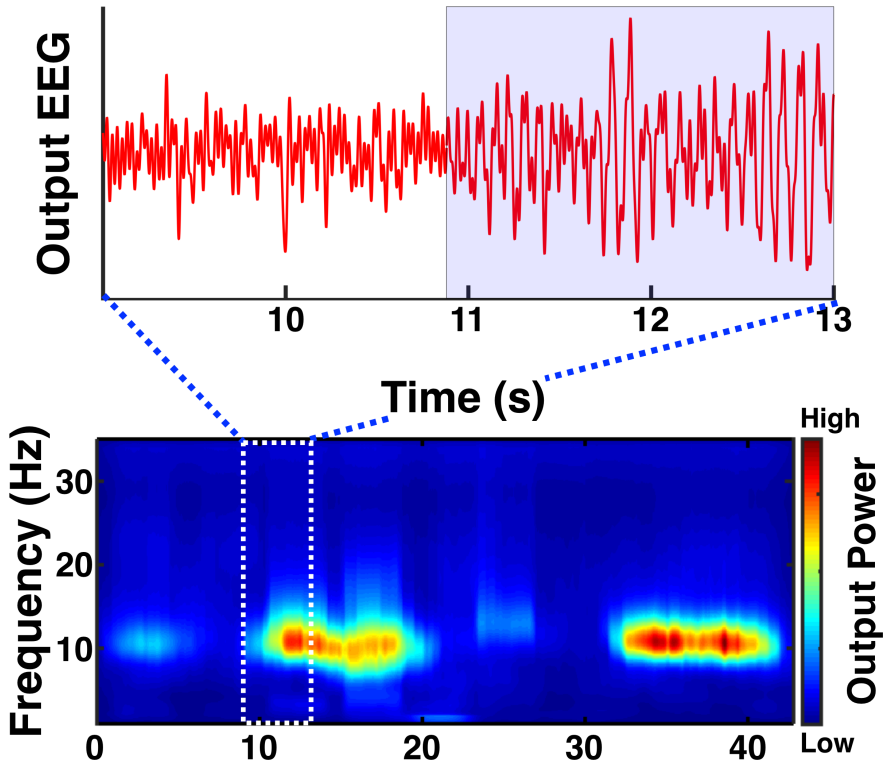


Figure 2.13: Amplifier I EEG time series (top) and spectrogram (bottom) from channel Oz with 10 dB increase in the posterior dominant alpha rhythm (8–12 Hz) amplitude when the subject closed his eyes (arrow). The subject closed his eyes at 10 and 32 s and opened again at 20 and 42 s [47].

a data acquisition system (Biopac MP150). This sampling rate corresponds to a sampling period of ∼100 μs per channel. The subject was provided verbal cues to alternate between eye opening/closing every 10 s. As a representative example, Fig. 2.13 shows prominent changes (∼10 dB) in the power of the occipital posterior dominant α rhythm at channel Oz in both the time series and the time-frequency spectrogram during this task. This is consistent with classic neurophysiological findings [69].

Measurements were performed on the second subject using Amplifier II, as follows. EEG from channel Oz (referenced to AFz) was split to Amplifier II as well as to a commercial bioamplifier (Biopac EEG100C) and sampled at 50 kHz. The output from both systems was downsampled to 2 kHz and filtered into the 8–35 Hz frequencies in software (see Fig. 2.14). The two signals exhibited a Pearson correlation coefficient of 0.89, and their envelope powers

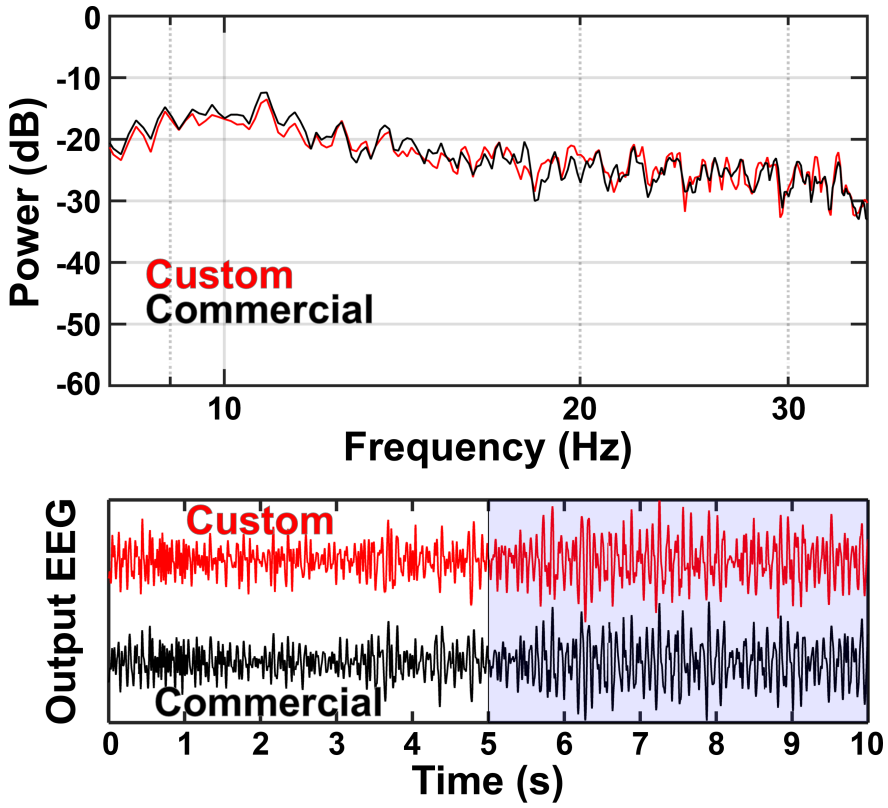


Figure 2.14: Top: PSD of the BSA II (red) and commercial (black) bioamplifier from 30 s of EEG data. Bottom: EEG α/β-band (8–35 Hz) time-series data from channel Oz (referenced to AFz) using the BSA II (red) and commercial (black) bioamplifiers. The subject was instructed to alternate between eyes-open (white background) and eyes-closed (blue background).

exhibited a correlation of 0.93. In addition, we recorded multiplexed EEG from electrodes AFz, Cz, Pz, and Oz (all referenced to AFz) using Amplifier II and the results after demultiplexing in software are shown in Fig. 2.15. As physiologically expected, electrodes Oz and Pz exhibit larger amplitudes of the occipital posterior dominant α rhythm during the eyes-closed state.

ECoG

One subject (43-year-old male) undergoing ECoG implantation for epilepsy surgery evaluation participated in the study. This subject had an 8×8 grid (Ad-Tech, Racine, WI) of

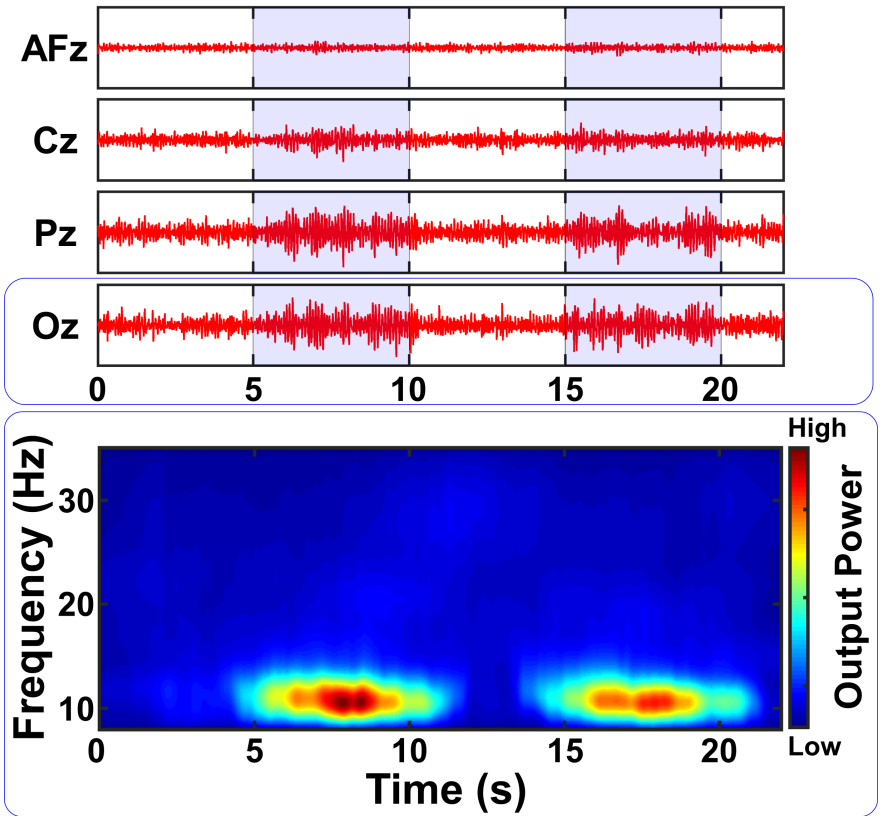


Figure 2.15: BSA II EEG α/β-band (8–35 Hz) time-series data (top) and spectrogram (bottom) from channel AFz, Cz, Pz, and Oz (all referenced to AFz) as the subject was instructed to alternate between eyes-open (white background) and eyes-closed (blue background). The channel-multiplexed data from the custom designed IC were demultiplexed in software.

2 mm-diameter electrodes (4-mm center-center spacing) implanted over the primary motor cortex. Fig. 2.16 shows the locations of the implanted electrodes (derived by co-registering a CT scan and MRI of the head, as in [70]). The subject completed his epilepsy monitoring procedure and was awaiting ECoG grid removal the next day. Hence, the hospital EEG system was disconnected at the time of measurement. ECoG signals were simultaneously routed to Amplifier II and a commercial EEG100C bioamplifier using unshielded cables, as shown in Fig. 2.17. Negligible loading effect and source impedance mismatch from EEG100C (2 MΩ input impedance) on Amplifier II is expected due to a relatively small electrodes' impedance (<1 kΩ). ECoG electrodes' impedance is reported to be stable over time [30], eliminating the need for constant monitoring of its value. The output from both amplifiers was recorded at 25 kHz by the MP150 system for 30 s. Note that the subject was asleep during this time

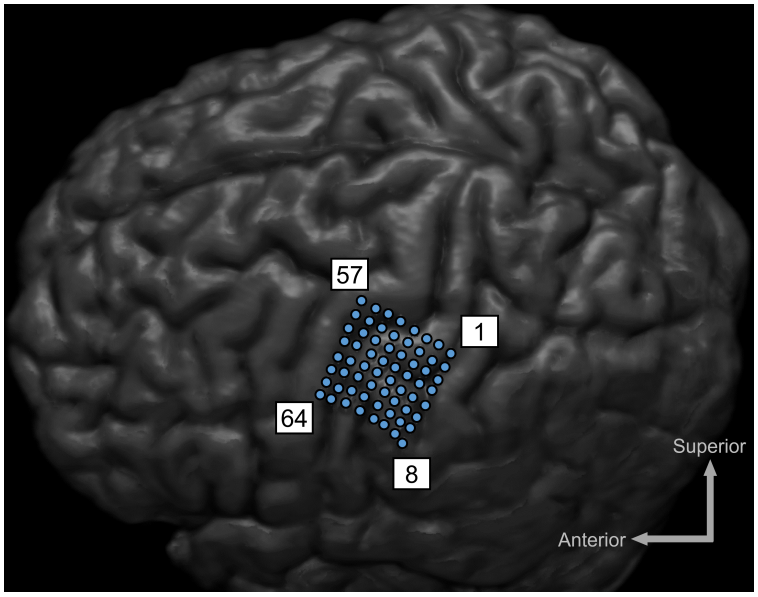


Figure 2.16: MRI of the patient with implanted ECoG grid over the left motor cortex. Electrodes 28 and 24 were used as the reference and ground, respectively.

and did not participate in any associated behavioral task for further verification of the amplifier array. The resulting signals were then downsampled to 2 kHz in software for further processing. The correlation coefficient between the signals from BSA II and the EEG100C was 0.99 from 8–35 Hz (covering the α and β bands), 0.94 from 35–70 Hz (low-γ band), and 0.72 from 70–120 Hz (high-γ band). Moreover, the correlation between each system's envelope power in α/β, low-γ, and high-γ bands was 0.99, 0.99, and 0.89, respectively. This slight decrement in the high-γ band correlation between the bioamplifiers is expected since the signal power decreases with frequency and approaches the Amplifier II's noise floor. A software notch filter was applied on the signal from 57 to 63 Hz before calculating the correlations. A representative PSD of the recorded signals across the α, β and γ bands (8–120 Hz) and 10-s output time-series of BSA II and its commercial counterpart are shown in Fig. 2.18, demonstrating qualitative similarities between the two. The peaks at 60 Hz for custom and commercial PSDs are caused by limited CMRR of the signal chain as well as the coupled power line interference to the unshielded interface between the analog output and the external ADC.

Table 2.4: Comparison and performance summary of AFEs

	JSSC 2011 [41]	JETCAS 2011 [43]	TBCAS 2014 [71]	JSSC 2015 [46]	TBCAS 2016 [45]	RHD2000 Intan [72]	Amp. I [47]	Amp. II [22]
Power (μW)†	2.44	56	23-46	1.4	1.08	7.4[9]	0.216	0.69
Supply (V)	2.8	3.3	+/- 0.6	0.5	1	3.3	0.4	0.6
Gain (dB)	39.4	60	Variable	30	40	45.7	39	39[1]
BW (Hz)	0.4–1.3k	300	1–15k	1–500	0.5–150	0.02–1k[10]	12–190	2–175
Noise (μV)[7]	3.07	0.5	13[2]	1.23	N/A[3]	2.4	2.19	2.3
NEF	3.09	4.4	7	3.7	4.52[5]	4.37[9]	4.65	7.22
PEF	26.7[6]	64[6]	58.5[6]	6.9	20.43[5]	63[9]	11.7	31.3
PSRR (dB)	> 80	69	39–93	67	68	75	58	70
CMRR (dB)	> 66	51	51–97	88	82	82	60	74
Area (mm^2)	0.13	86[8]	12.19[8]	0.025	0.085	N/A	0.044	0.052
% THD at mV$_{pp}$	1% (10)	1% (2.6)	1% (4.5)[4]	0.4% (1)	1% (4)	0.8% (10)	1% (5)	<1% (0.2)
Technology	0.6 μm	0.35 μm	0.13 μm	65 nm	65 nm	N/A	0.13 μm	0.18 μm

†Power dissipation includes only the front-end amplifier unless otherwise stated. [1]58 dB for the whole AFE. [2]7.3 μV_{RMS} for 300–15 kHz. 13 for 1–300 Hz μV_{RMS} [3]112 nV/$\sqrt{Hz}$ at 150 Hz. [4]Including ADC. [5]Reported for a defined single frequency. Actual value is higher. [6]Value calculated from reported results. [7]Integrated over the bandwidth. [8] Total chip area. [9] Estimated over 1 kHz bandwidth. [10] Bandwidth tunable from 0.02–20 kHz

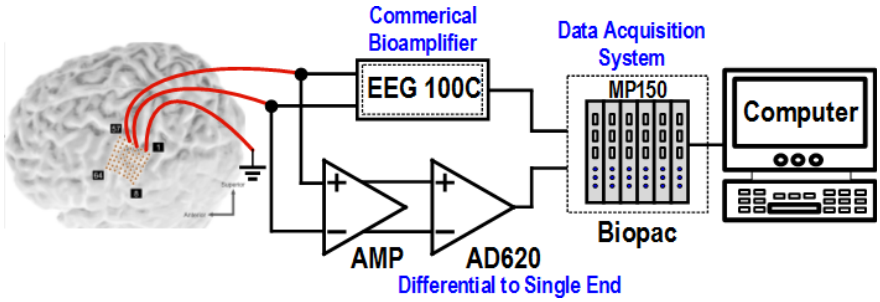


Figure 2.17: *In vivo* ECoG measurement setup.

2.6 Conclusion and Future Work

Two brain signal acquisition front-ends designed in the WI region were presented. Fabricated in 130nm and 180nm CMOS processes, each amplifier within the arrays consumes 0.216 / 0.69 μW, respectively (not including buffer and InAmp). Measured IRNoise across the bandwidth was 2.19 / 2.3 μV_{RMS} corresponding to NEF of 4.65 / 7.22 and PEF of 11.7 / 31.3[73]. Objective comparison of human *in vivo* EEG and ECoG measurements acquired by our custom IC and a commercial bioamplifier demonstrated that our BSAs were able to record these neural signals reliably. This suggests that the circuit architecture presented in this work can serve as the basis for a highly miniaturized and ultra-low power brain signal acquisition unit for a future fully implantable BCI system. Future work will focus on further reducing the susceptibility of the front-end to environmental noise, e.g., including an on-chip analog-to-digital converter, and incorporating the capability of large interference rejection at low supply voltages in the presence of a sensory feedback stimulation circuitry.

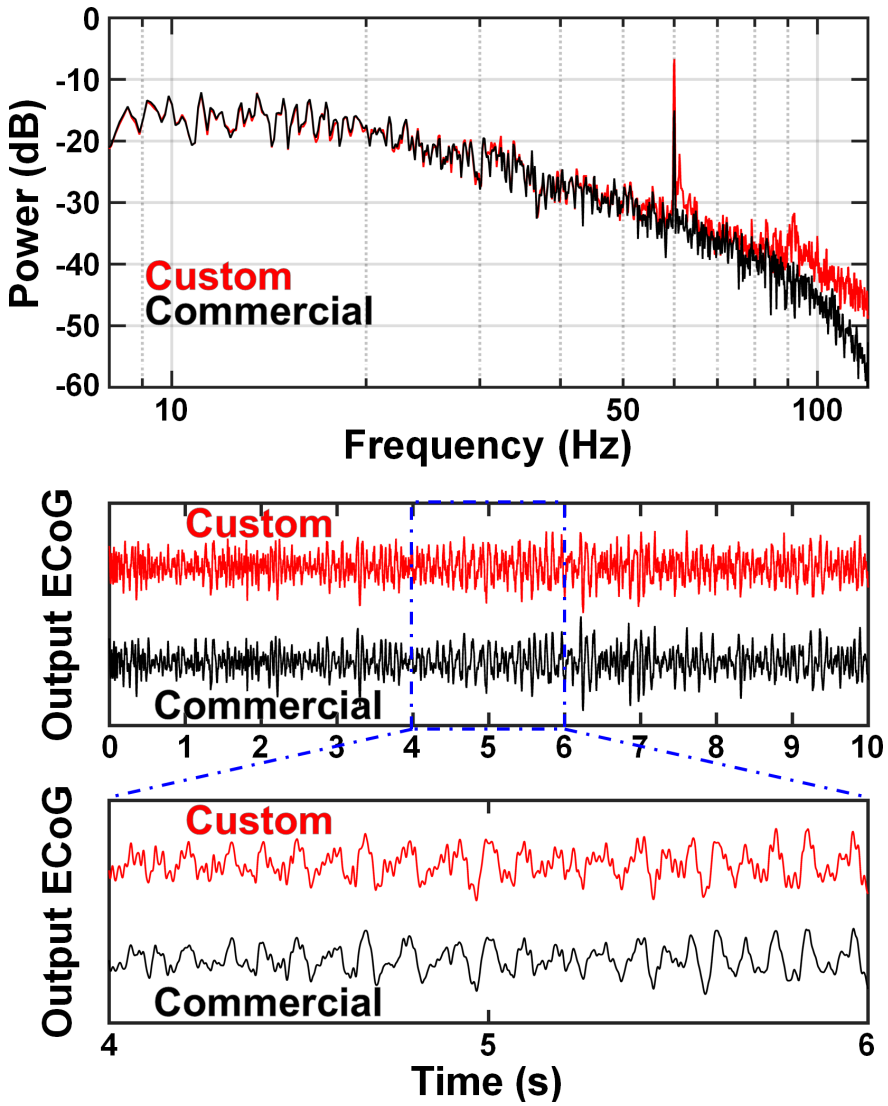


Figure 2.18: Top: PSD of the BSA II (red) and commercial (black) bioamplifier from 30 s of ECoG data. Middle: Filtered (8–120 Hz) time-series data from the implanted ECoG grid with the BSa II (red) and commercial (black) bioamplifier. Bottom: Zoomed-in view of the recorded ECoG.

Chapter 3

A CMOS MedRadio Transceiver with Supply-Modulated Power Saving Technique for an Implantable Brain-Machine Interface System

3.1 Introduction

Implantable medical devices, such as deep brain stimulators [74] or responsive neurostimulators [75], are routinely used for the treatment of neurological conditions. As technology advances, these systems are also becoming more sophisticated, and this trend will continue in the future. In addition, current brain implants will likely be re-purposed or redesigned in the future to address unmet clinical needs [76]. To fulfill their role, these future implantable systems will need to be endowed with additional features and functions. One such novel clinical application is the restoration of motor function after stroke or spinal cord injury

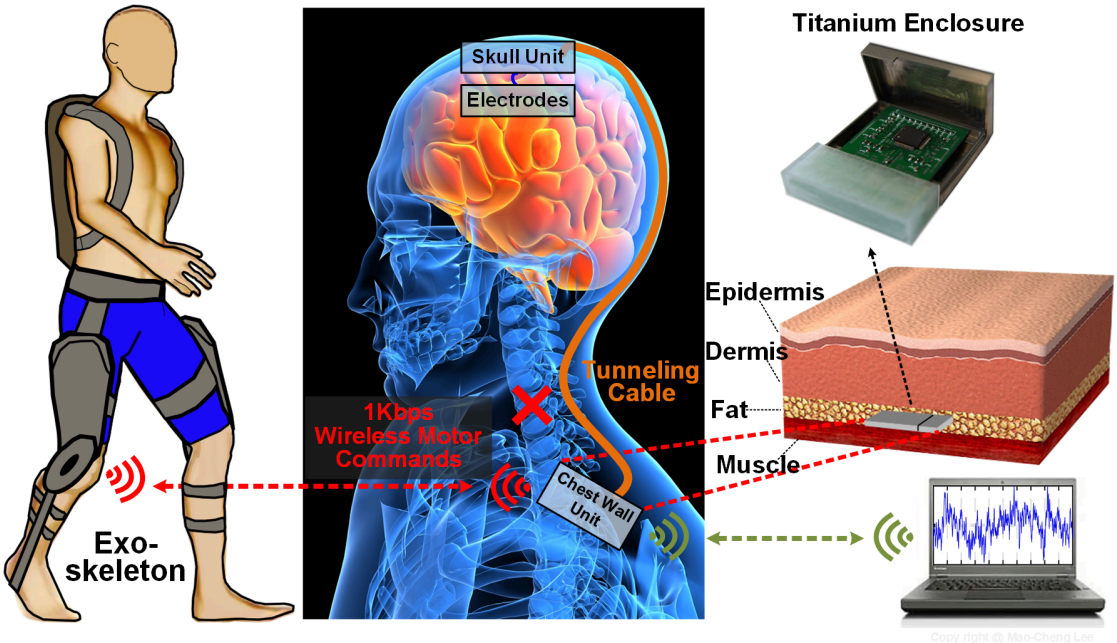


Figure 3.1: Proposed fully-implantable BMI system for restoration of walking, with a signal acquisition front-end (skull unit) and signal processing and wireless communication modules (chest wall unit). This system bypasses the injured spinal cord and enables direct brain control of an exoskeleton.

(SCI) using brain-machine interfaces (BMIs). Generally, BMIs record, process, and decode cortical signals in real time, and use this information to control external devices [77]. This enables those with paralysis to operate prostheses [78] or muscle stimulators [79] directly from the brain while bypassing the neurological injury. Current state-of-the-art invasive BMIs are mostly used in a laboratory setting, and their clinical adoption will critically depend on the ability to make them fully implantable. Despite encouraging results [80], these systems rely on external electronics and skull-protruding components, which makes them impractical, less safe, and generally unsuitable for everyday at-home use. These obstacles can be circumvented by designing a fully implantable BMI with internal electronics and no skull-protruding components.

Fig. 3.1 shows an example of a hypothetical implantable BMI system for restoration of walking in individuals with SCI. This system comprises a skull unit for brain signal sensing and a chest-wall unit (CWU) for signal processing. μV-level brain signals sensed by the

skull unit are routed out of the head by a subcutaneous tunneling cable (similar to modern deep-brain stimulators [81]), and delivered to the CWU. The CWU processes brain signals to detect walking intentions and converts them into 1–10 kbps wireless commands for external prostheses, such as robotic exoskeletons or functional electrical stimulators. A major design challenge for this system is then to perform signal processing and wireless data transmission tasks, while meeting the size, power, and magnetic resonance imaging (MRI) compatibility constraints necessary for safe human implantation. This includes trading off the power consumption of the DSP and TRX modules.

For example, wireless communication between the implantable devices and external computers is typically a power-hungry process. Therefore, minimizing the power consumption of the wireless TRX would enable allocation of a higher fraction of the overall power budget to the brain signal processing units within the CWU. Based on our preliminary estimate, the proposed CWU should consume less than 50 mW for which DSP, data converter and other modules account for 80-90% of total budget and with the remainder allocated to the TRX block. Additionally, limited enclosure area requires small form factor for all wireless unit's constituent components including the antenna. Also, to meet the most stringent field conditions (i.e. static magnetic field stength, specific absorption rate, etc.) due to interactions with magnetic field of MRI system, the proposed CWU in Fig. 3.1 relies on an inductorless TRX with no off-chip component except an antenna. Commercially available MRI-conditional devices use customized structures to enclose antenna to further reduce magnetic interaction and hence satisfy the MRI requirements for implantable systems (e.g., Medtronic W1DR01/W1SR01 [82]).

Multiple telemetry methods – such as near-field magnetic coupling, conduction through the body, and short-range RF communication – exist that establish the link between the implanted device and external units or actuators. Human body communication (HBC defined in IEEE 802.15.6 standard) uses human body as a channel, and has emerged as a promising

method for low power and relatively high data rate (>1 Mb/s), while being free from shadowing effect. However, challenges such as interference, difficulty in estimating the channel, impedance variation of skin-electrode interface, and mutipath problem have to be addressed for this method to become widespread [83, 84]. IEEE 802.15.4 bluetooth low energy (BLE), and IEEE 802.15.6 narrowband (NB) and ultra wideband (UWB) PHYs standards have been developed for short-range radios and cover low-power applications (e.g., wireless personal area network and wireless body area network). These standards employ duty cycling for power saving and interference mitigation. While low-power, the radios based on these standards still do not satisfy the severe power budget, heat dissipation, low emission power, and small area constraints required for an implantable BMI system such as the one in Fig. 3.1. A near-field radio for syringe-implanted sensor nodes was presented in [85] which implemented a communication protocol that eliminated the need for symbol boundary synchronization in the sensor RX. The asymmetric nature of the architecture shifts the performance burden (i.e., high sensitivity RX and high power TX) toward the base station [85]. The N-path uncertain-IF and dual-IF architectures proposed in [86, 87] conduct high-Q selectivity frequency translation without the power-hungry phase-locked loop (PLL). A TX-referenced RX published in [88] improves the interference robustness, and breaks the tradeoff between power, sensitivity, and linearity. A two-tone TRX using a simple envelope-detection RX and a direct-modulation TX was presented in [89].

MedRadio band (401–406 MHz) was dedicated by the Federal Communications Commission for implantable and wearable devices, which has been expanded recently by allocating four 6-MHz bands at 413–419 MHz, 426–432 MHz, 438–444 MHz and 451–457 MHz. Recently published MedRadio TRXs in [90–93] employed a bulky on- or off-chip inductor for impedance matching and/or performance improvement. Expanding on our prior work [94], this paper presents analysis and design of a CMOS low-power inductorless OOK TRX for the MedRadio 413–419 MHz band intended for transferring the BMI control commands and monitoring bio-signals wirelessly. A novel event-driven supply modulation (EDSM) tech-

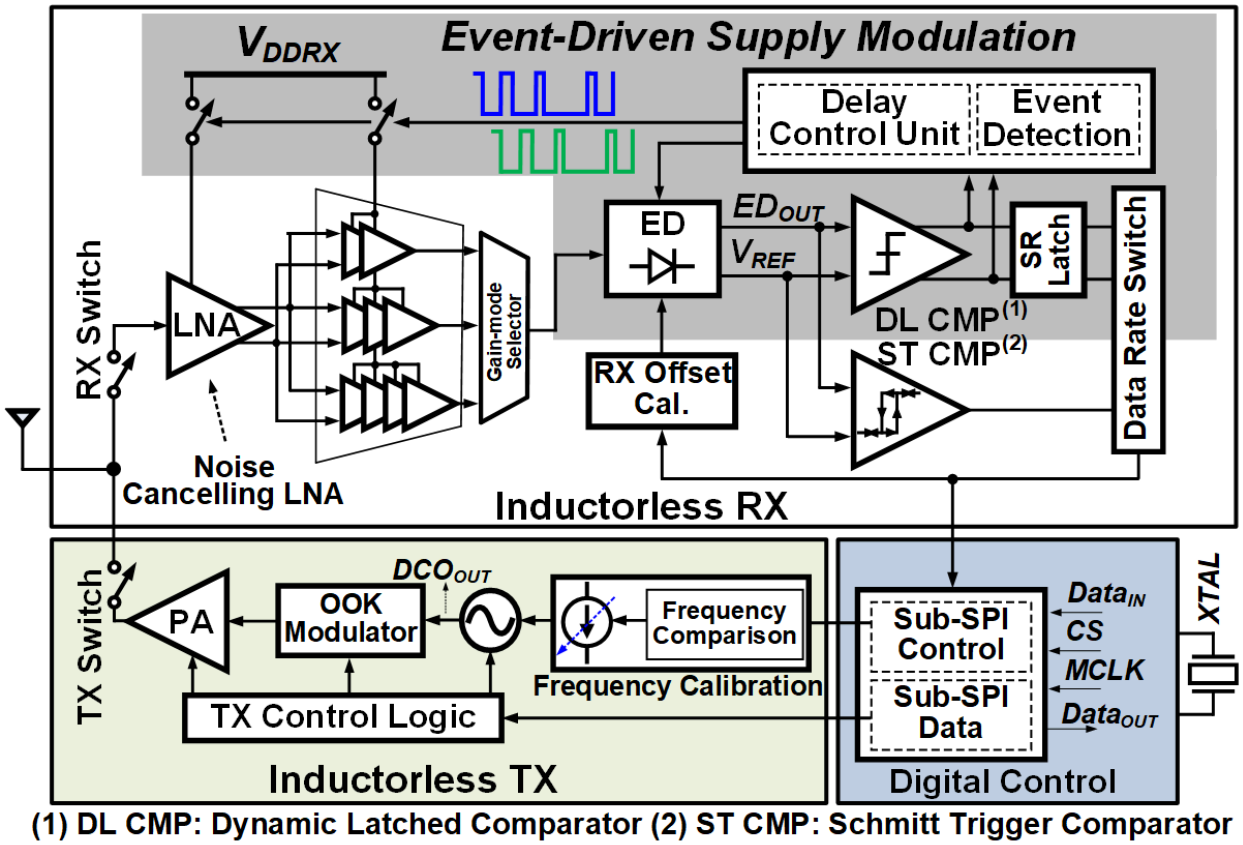


Figure 3.2: The architecture of the proposed low-power OOK TRX

nique on the RX side (see Sections 3.3 and 3.4) and a fast start-up power-cycling capability on the TX side (see Section 3.5) are utilized.

3.2 TRX Architecture

Fig. 3.2 demonstrates the proposed MedRadio TRX comprising a supply-modulated non-coherent direct-detection RX and a direct-modulation OOK TX. On the RX side, the incoming signal is strobed by a periodically-activated noise canceling low-noise amplifier (LNA) above the Nyquist rate of the baseband (BB) signal representing the BMI control commands. The BB signal is then recovered after passing through an envelope detector (ED) and a dynamic latched comparator, as a decision circuitry. A feedback control circuit turns off the RX

amplifiers as soon as the current bit is resolved, effectively duty-cycling the RX. As will be illustrated in Section 3.3, this approach will minimize the average power consumption with minor degradation ($\sim$ 5dB per 1 decade increase in data rate) in RX sensitivity. On the TX side, the BB data modulates the free-running digitally controlled oscillator (DCO) incorporating a fast frequency calibration loop, which allows the entire TX to be power-cycled. The OOK modulated signal is amplified by a self-biased, inverter-based power amplifier (PA), and is subsequently delivered to an off-chip antenna (for testing purpose only).

3.3 Asynchronous Event-Driven Supply Modulation

A conventional direct-detection RX continuously senses, amplifies, and detects the envelope (or power) of the received signal [95, 96]. Following the envelope detection, the clocked comparator generates the BB data. However, the power-hungry blocks, namely, LNA and gain stages – operating at high current levels for noise and power matching purposes – are always activated during the entire detection/comparison phase irrespective of BB signal activities. A number of duty-cycling-based power reduction techniques have been presented [97, 98] to periodically switch off power-hungry blocks with an enable signal. The average power consumption of the duty-cycled RX is approximated as:

$$P_{avg} = P_T \times \left(\frac{2T_{on}}{T_b}\right) \times OSR + P_{bias} \tag{3.1}$$

where P_T is the total power consumption of the RX core without duty-cycling technique, T_{on} represents the RX on time, T_b denotes the bit period, and OSR is the oversampling ratio. P_{bias} is power consumption of the bias generation circuit. Clearly, the duty-cycling technique leads to significant amount of power saving if $T_{on} \ll T_b$. However, the supply switching in prior work is done at a fixed pulse-width $T_{on,fix}$ (indicated in Fig. 3.3(a)) which must account for worst case conditions, i.e., lowest LNA gain, largest comparator metastability time-

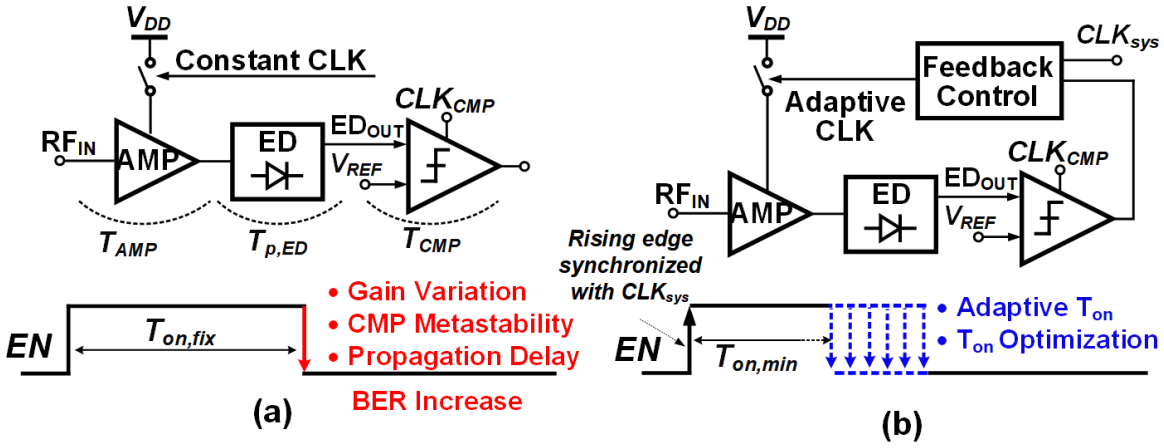


Figure 3.3: (a) Envelope detector based receiver with a fixed pulse-width. (b) The proposed EDSM receiver with adaptive feedback control loop.

constant, and signal propagation delay uncertainty across process, voltage, and temperature (PVT) variation. As a result, the amount of power saving is severely limited by this non-optimal $T_{on,fix}$.

To overcome the power-saving limitation due to $T_{on,fix}$ and further reduce T_{on}, we first study the parameters affecting it. T_{on} is approximately lower-bounded by: $T_{on} \geq T_{on,min} (= T_{AMP} + T_{p,ED} + T_{CMP})$. T_{AMP} denotes the time taken for the duty-cycled amplifier to reach its stable dc-bias point at the rising edge of the EN signal shown in Fig. 3.3(b). $T_{p,ED}$ is the input-output propagation delay of the ED. T_{CMP} represents the time taken by the comparator to make a decision. For the dynamic comparator adopted in this design (see Fig. 3.5(a)), T_{CMP} is readily derived to be:

$$T_{CMP} \cong \frac{2|V_{THP}|C_L}{I_{SS,1}} - \frac{C_L}{G_m} \ln(\Delta V_{IN}) \tag{3.2}$$

where V_{THP} indicates the PMOS threshold voltage, $I_{SS,1}$ is the tail current, M_1. C_L is the load capacitor seen at the output of the comparator. G_m represents the equivalent large-signal transconductance of each cross-coupled CMOS inverter (M_4-M_8 and M_5-M_9) realizing regenerative load of the comparator. ΔV_{IN} is the comparator's input amplitude and T_f is

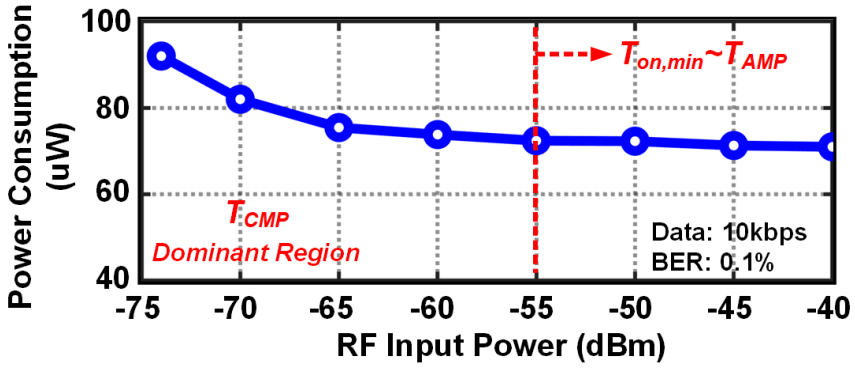


Figure 3.4: Simulated RX power consumption vs. the input power.

a fixed time which is determined by the bias current, the load capacitor, and input device parameters. T_{CMP} is signal dependent, whereas T_{AMP} and $T_{p,ED}$ are both functions of PVT and may vary from chip to chip. Fig. 3.4 displays the simulated RX power consumption vs. the RF input power. From Fig. 3.4, T_{CMP} will become a major contributor to the power-saving feature as the input power decreases below a certain level (e.g., -55 dBm). Besides, T_{AMP} can constitute an increasingly larger portion of T_{on}, eventually limiting the functionality of the EDSM-based RX to data rates below 0.5 Mbps. In this case, techniques such as bias pre-charge should be used in the amplifiers to minimize T_{AMP} and $T_{p,ED}$.

The functional block diagram of the EDSM-based RX is depicted in Fig. 3.3(b) where an adaptive feedback control loop (details in Section 3.4) is employed to guarantee duty-cycling at $T_{on} = T_{on,min}$. Similar to the conventional architecture, upon envelope-detection and the BB data recovery, the feedback control unit will capture the comparison result and generates the control pulses to turn off the power-hungry blocks, thereby lowering the average power consumption. Unlike the duty-cycled RX architectures with constant on time (Fig. 3.3(a)), the EDSM technique generates control pulses whose pulse-widths vary with $ED_{out} - V_{ref}$ at the comparator inputs. More precisely, the falling edge of these pulses are automatically adjusted depending on the RF signal power, the amplifier gain, and the envelope detection responsivity across PVT variation as soon as the comparator decision has been

made (Fig. 3.3(b)). In summary, this technique optimizes the turn-off edge of EN signal to minimize T_{on}, thereby achieving the lowest power consumption.

3.4 Receiver Implementation

The EDSM RX architecture is shown in Fig. 3.5(a). An event detection circuitry and a delay control unit generate and adjust variable duty-cycle power-switching pulses $SM_{\phi 1}$ for amplifiers and settling-time accelerating pulses $SM_{\phi 2}$ for the ED. The system clock (CLK_{SYS}) is provided by an external source (a crystal oscillator (XTAL) in this design). The external source will be provided by a micro-controller, once this TRX is integrated with the CWU. Running at Nyquist rate of the BB signal, CLK_{SYS} periodically turns on the LNA to strobe the received signal. A delayed version of CLK_{SYS}, CLK_{CMP}, triggers the clocked comparator and marks an "event," T_{CMP} seconds after its positive edge (*cf.* Fig. 3.5(b)). During the event interval, the outputs are captured in an SR latch and are also fed to the event detection circuitry. Enabled by CLK_{SYS}, the event detection circuit generates the falling edges of $SM_{\phi 1}$ once it senses an event, and subsequently turns off the power-hungry LNA and amplifiers until the next strobing edge (set by the positive edge of CLK_{SYS}). While the linearity requirement of a direct-detection OOK RX is relaxed, its noise performance deserves attention. The noise analysis of a direct detection RX is more involved as the inherent nonlinearity of the ED causes whole host of issues, such as the noise self-mixing phenomenon. Although the commonly used noise-equivalent power (NEP) provides a more accurate evaluation of an ED's noise performance especially at high frequencies, relating it to the overall NF of the RX is not straightforward. We thus utilize the conversion gain (See Section 3.4.2) to characterize noise and signal frequency-translations in an ED. The RF noise at the ED input will be translated to low frequency at the output through its conversion gain. On the other hand, the low frequency noise within the ED bandwidth is

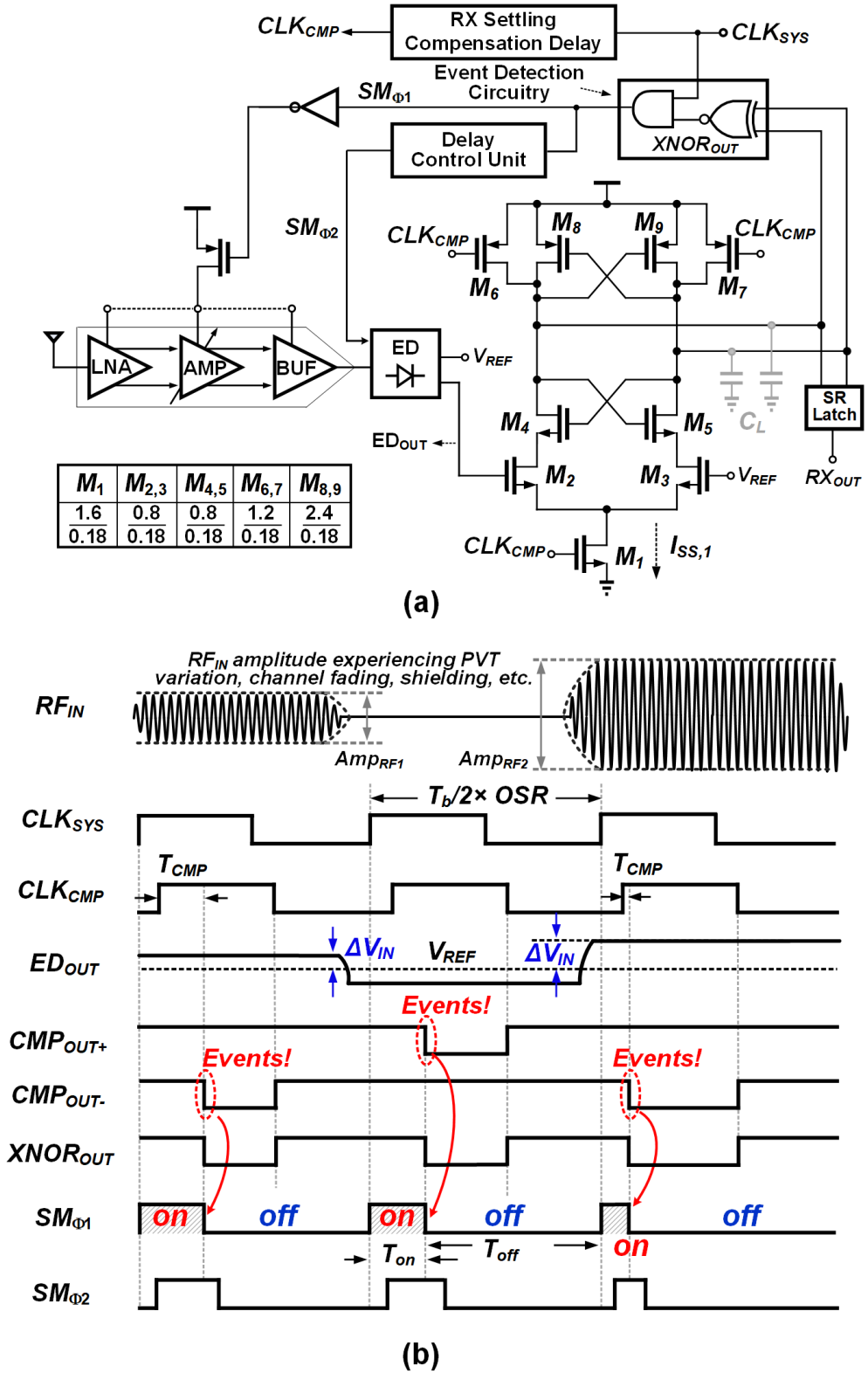
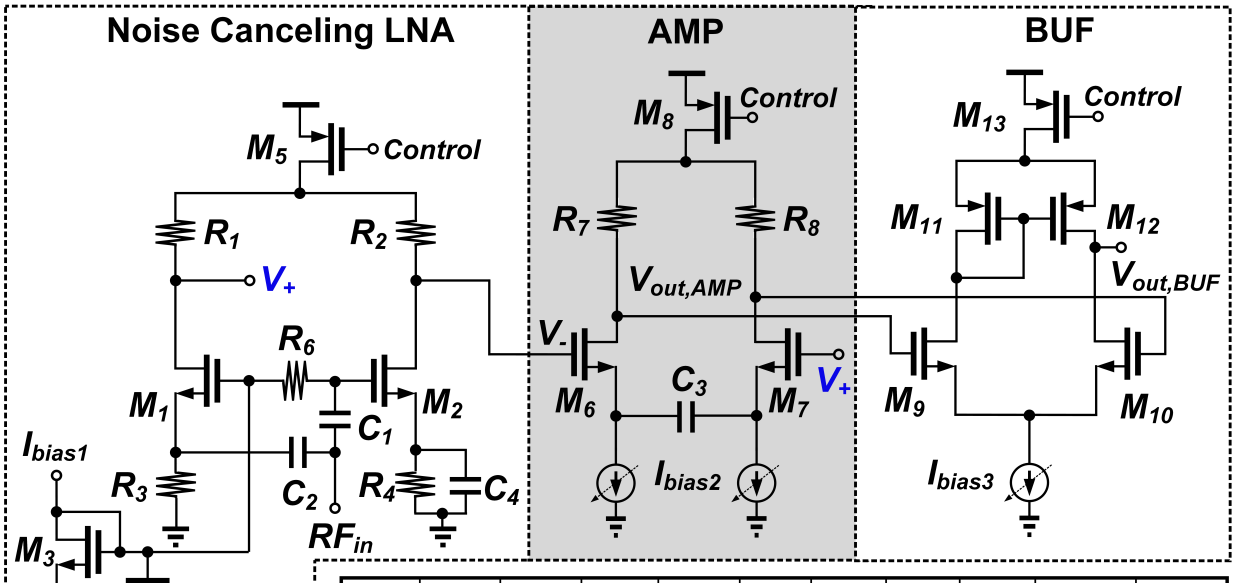


Figure 3.5: (a) Event-Driven supply modulated RX schematic. (b) The timing diagram of EDSM RX.



M_1	M_2	M_3	M_4	M_5	R_1	R_2	R_3	R_4	R_5	R_6
160/0.18	320/0.18	0.5/0.18	300/10	100/0.18	560Ω	280Ω	400Ω	200Ω	11.2kΩ	100kΩ

All the transistors ratio are W/L

I_{bias1}	I_{bias2}	$C_{1,2}$	C_3	C_4	$M_{6,7}$	M_8	$R_{7,8}$	I_{bias3}	$M_{9,10}$	$M_{11,12}$	M_{13}
4uA	420uA	44pF	2.5pF	100pF	24/0.18	60/0.18	1500Ω	390uA	4/0.18	10/0.18	100/0.18

Figure 3.6: The schematic of noise canceling low-noise amplifier, capacitively-degenerated cascaded gain stage unit and differential to single-ended buffer.

amplified by a large and linear DC gain. The RX chain's NF is derived as follows:

$$NF_{RX} = NF_{amp} + \frac{\overline{V_{n,ED}^2} + \overline{V_{n,LF}^2} A_{ED,DC}^2}{4kTR_s A_V^2 A_{ED}^2} \tag{3.3}$$

$\overline{V_{n,LF}^2}$ and $\overline{V_{n,ED}^2}$ are the low-frequency noise power at the ED input and the noise contribution of the ED, respectively. NF_{amp} is the NF of amplification chain, A_V is the voltage gain of the entire amplification chain, $A_{ED,DC} = V_{o,DC}/V_{in,DC}$ and $A_{ED} = V_{o,DC}/V_{in,RF}$ are the DC and conversion gains of the ED, respectively.

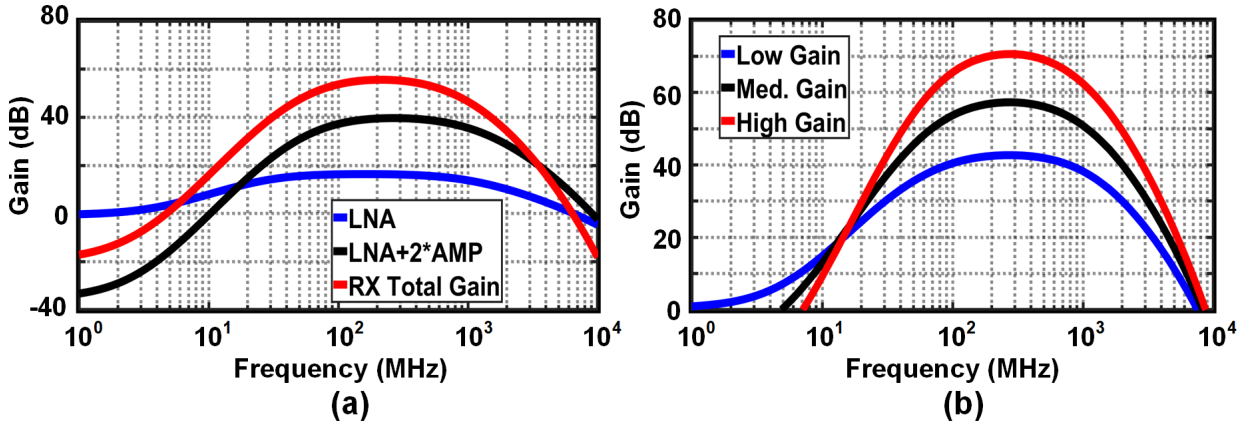


Figure 3.7: (a) The simulated gain of each stage in the receiver chain. (b) The simulated gain curves of receiver in different gain-modes.

3.4.1 Noise Canceling LNA and Gain Stages

Fig. 3.5 shows the overall RX front-end consisting of a noise-canceling LNA, cascaded gain stage unit(s), differential to single-ended buffers and a gain-mode selector. To cover an adequate TX-RX link range, three distinct parallel paths accommodating low, medium, and high gain-modes are considered in this design. The use of three gain paths instead of VGA allows for noise and power optimization of devices in each path distinctly, resulting in better power efficiency [99]. The gain mode can be selected through a digital automatic gain control in the back-end processor (an off-chip microcontroller). Fig. 3.6 shows the LNA schematic, which is based on [100]. The common-gate stage M_1 provides a resistive 50-Ω matching to the antenna impedance (R_s). Furthermore, the common-gate and common-source branches have been biased to have identical output common-mode operation. The noise contribution of M_1 is nullified if $g_{m1}R_1 = g_{m2}R_2$. This LNA's NF is readily derived to be:

$$NF_{LNA} = 1 + \frac{R_s}{R_3} + \gamma\frac{R_2}{R_1} + \frac{R_s}{R_1} + \frac{R_sR_2}{R_1^2} \tag{3.4}$$

where γ is the MOS thermal noise coefficient. The LNA is followed by a capacitively-degenerated differential amplifier and a differential to single-ended buffer. The simulated gain plots of the RX front-end, the LNA, and the amplification stage for the medium-gain

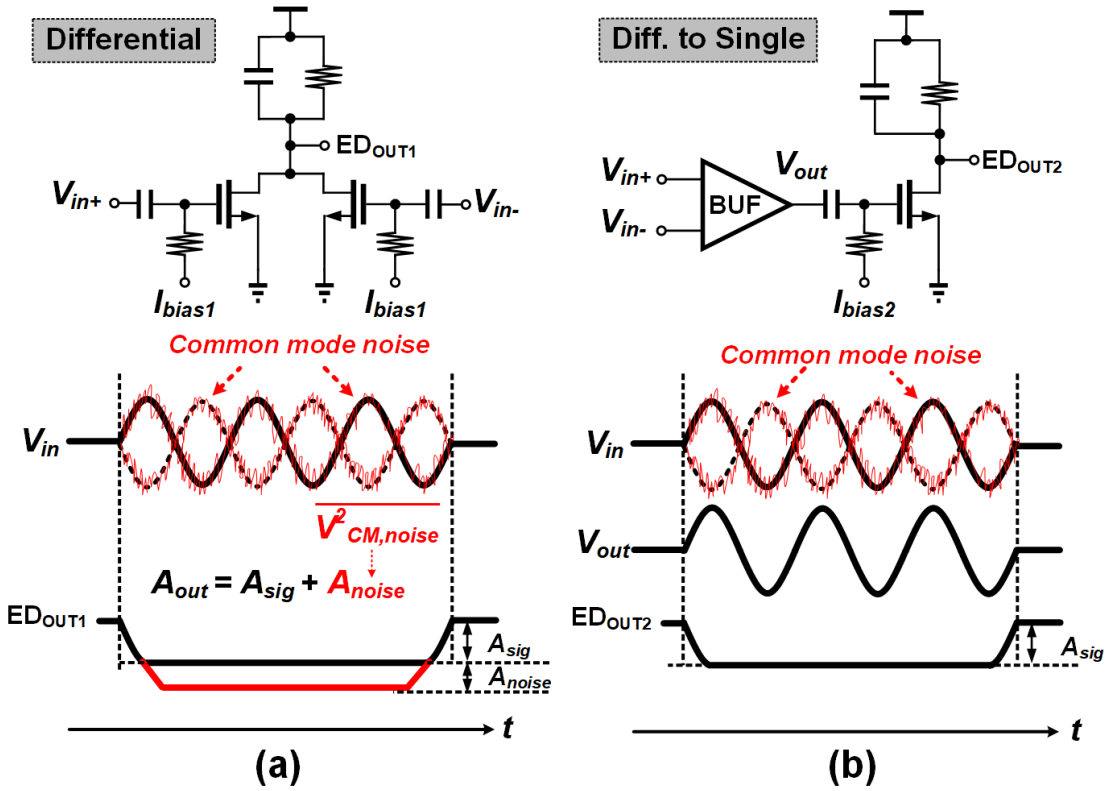
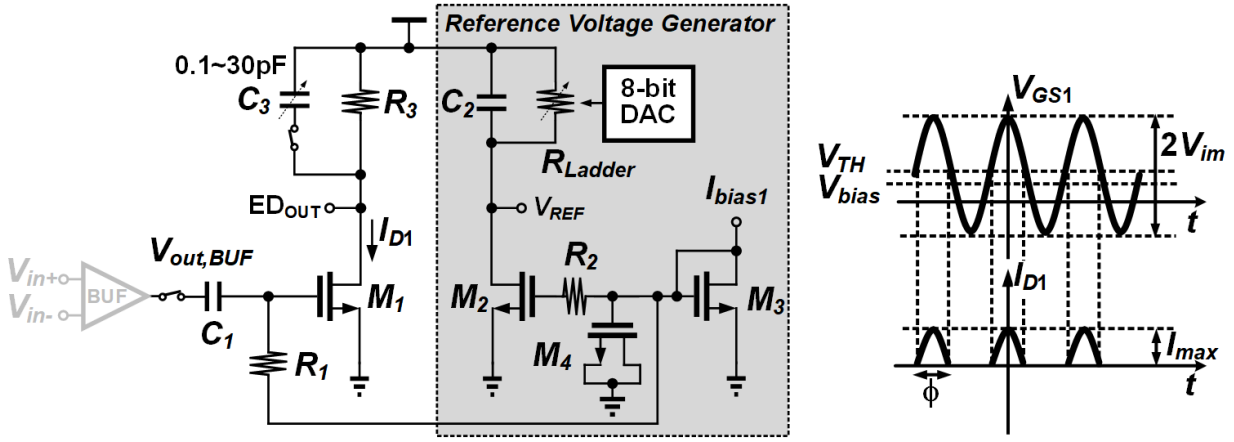


Figure 3.8: The output voltage level with input signal with common-mode noise in (a) active differential architecture. (b) differential-to-single first approach.

mode are shown in Fig. 3.7(a). Fig. 3.7(b) depicts the simulated gain plot of the RX front-end under different gain-modes. The RX provides 30 dB (from 40–70 dB) gain adjustment range at 416 MHz.

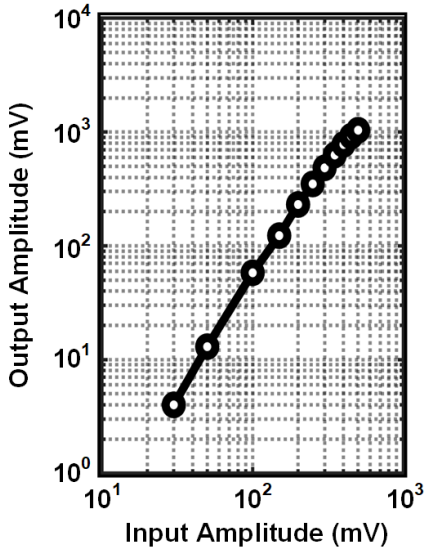
3.4.2 Envelope Detector and Offset Calibration

The active differential-input envelope (power) detectors (e.g., [101][102]) achieve high responsivity at the expense of common-mode noise accumulation. Fig. 3.8(a) shows an active differential-input push-push ED. The ED output is the sum of average signal and noise powers (V_{in}^2 and $\overline{V_{CM,noise}^2}$), inducing an unwanted rms voltage drop, A_{noise}, to the output. Fig. 3.8(b) shows a common-source-based single-ended ED. This detector is preceded by the last-stage differential to single-ended buffer in Fig. 3.6, which mitigates the common-mode noise accumulation. Fig. 3.9(a) shows the schematic of the ED used in this design. Assuming

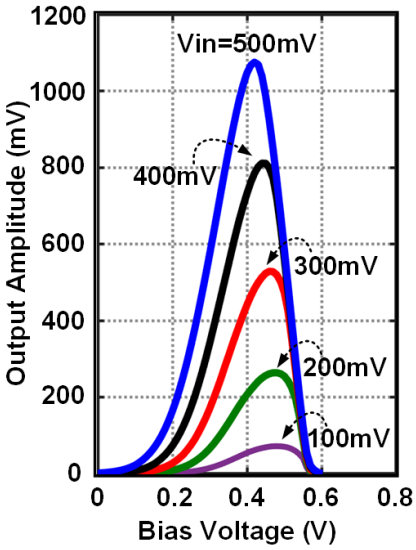


I_{bias1}	$M_{1,2}$	M_3	M_4	$R_{1,2}$	R_3	C_1	C_2
2.5uA	2/0.18	2/0.18	300/10	100kΩ	100kΩ	0.55pF	26pF

(a)



(b)



(c)

Figure 3.9: (a) Schematic of the proposed envelope detector. (b) simulated envelope detector output amplitude with different input amplitude. (c) simulated output DC voltage vs. input bias voltage.

the long-channel MOS model and filtering of fundamental and high-order harmonics of the input, the output voltage of this ED is expressed as:

$$V_{o,DC} = ED_{OUT} - V_{REF} = \frac{1}{4}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 R_3 V_{im}^2 \tag{3.5}$$

where V_{im} denotes the RF input amplitude. At MedRadio frequencies, the power gain is abundant, and thus the RF blocks are directly cascaded with no inter-stage matching network. This implies that the ED's conversion gain, A_{ED}, provides more insight about the ED performance rather than its responsivity R $(= V_{o,DC}/P_{in,RF})$.

$$A_{ED} = \frac{1}{4} g_{m1} R_3 \frac{V_{im}}{V_{OD}} = \frac{1}{4} A_{ED,DC} \frac{V_{im}}{V_{OD}} \tag{3.6}$$

where V_{OD} and g_{m1} are the overdrive voltage and transconductance of transistor M_1 in the circuit of Fig. 3.9(a). The simulated output vs. input amplitude of this detector is shown in Fig. 3.9(b), which follows the anticipated square-law transfer characteristic.

Fig. 3.9(a) shows the ED's input voltage and drain current (approximated by periodic rectified cosine function) waveforms. Maximizing the second harmonic current will maximize the conversion gain. Using the analytical study in [103], the second harmonic current in terms of the peak drain current I_{max} and conduction angle $\phi\big(= 2\cos^{-1}(\frac{V_{TH}-V_{bias}}{V_{im}})\big)$ is obtained:

$$I_2 = I_{max} \frac{2\sin^3\frac{\phi}{2}}{3\pi(1-\cos\frac{\phi}{2})} \tag{3.7}$$

I_2 is maximized for $\phi = \pi$, resulting in $V_{bias,opt} = V_{TH}$. This means that the ED should operate as a deep class-AB stage to maximize conversion gain, and thus relax the sensitivity constraints of the following comparator. Fig. 3.9(b) presents the simulated envelope detector output amplitude with different input amplitude. Fig. 3.9(c) shows the simulated output DC voltage vs. input bias voltage of the ED for five different values of the input amplitude.

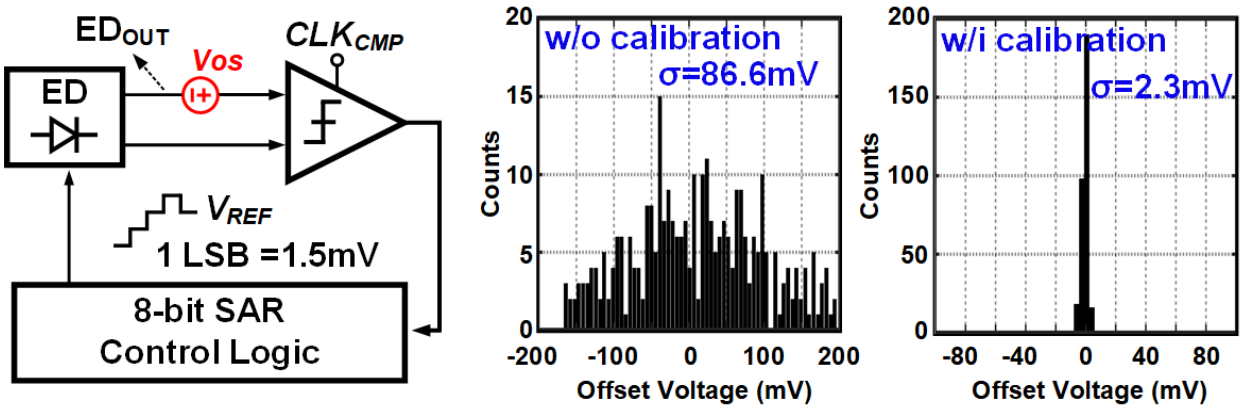


Figure 3.10: Offset calibration system and Monte-Carlo simulation results.

As shown in Fig. 3.9(c), biasing transistor M_1 around its threshold voltage (≈0.45 V) will maximize the conversion gain.

The ouput thermal noise of the ED is derived as follow:

$$\overline{V_{n,ED}^2} = 4kTR_3(1 + \gamma g_{m1} R_3) \tag{3.8}$$

As mentioned before, the undesired low-frequency noise in the passband of the ED is amplified by $A_{ED,DC}$. It is worth noting that the single-ended structure in Fig. 3.9(a) is sensitive to the offset of the following comparator. To overcome this problem, an 8-bit offset-calibration circuit incorporating a successive approximation register (SAR) feedback loop is utilized (see Fig. 3.10). Based on the comparator output logic level, the SAR control logic determines the output of the 8-bit DAC to compensate for the input-referred offset of the dynamic comparator, capturing up to ±190 mV input-referred comparator offset within 0.3 ms. Fig. 3.10 compares the statistical input-referred offset voltages of the comparator with and without this calibration scheme using Monte-Carlo simulation. From the Monte-Carlo simulation with 300 different samples, the result shows a 38-fold improvement (i.e., σ is reduced from 86.6 mV to 2.3 mV).

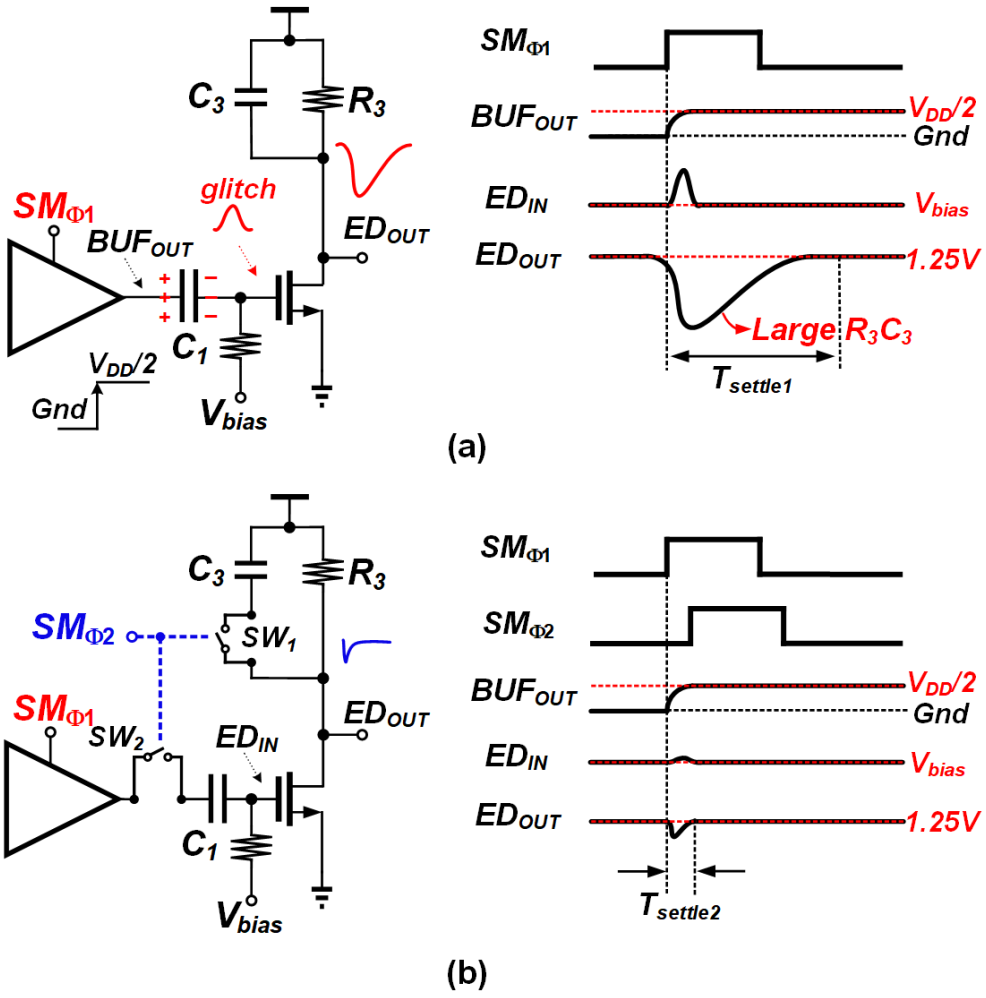


Figure 3.11: The settling time of (a) conventional envelope detector. (b) the proposed envelope detector with acceleration switch.

3.4.3 Settling-Time Acceleration Switch

The amount of power saving in this RX is directly dependent on its ability to function properly within extremely short T_{on}'s. However, since the EDSM scheme turns amplifier stages on and off in every clock cycle, the voltage level at the output of the ED slews up too slowly to reach its default value, causing the comparison error at the comparator. Depicted in Fig. 3.11(a), the charging of the decoupling capacitor C_1 during the off-to-on dc-bias transition at the output of the buffer would induce a glitch at the gate of M_1, causing a large transient voltage drop at the output. Fig. 3.11(b) shows the ED incorporating two settling-time acceleration switches SW_1 and SW_2 to shorten the settling-time. To hold the

charge across C_1 constant, the delay control unit applies a delayed version of $SM_{\phi 1}$ to SW_1 and SW_2. This avoids the voltage change at the gate/drain of M_1 during the control-signal transition and thus considerably reduces the ED settling time.

3.5 Transmitter Implementation

3.5.1 Direct-Modulation Transmitter

The MedRadio band at 413–419 MHz relaxes carrier frequency stability requirement, particularly for constant-amplitude modulation schemes. Shown in Fig. 3.12(a), the proposed TX chain is comprised of a free-running DCO with automatic frequency calibration (AFC), OOK-modulating T-switch, and power-configurable inverter-based driver and PA circuits. Fast startup time of the DCO allows for the whole TX to be power-cycled which not only saves power, but also avoids unnecessary power emission when transmitting 0s. The entire PA circuit following the DCO consists of a self-biased inverter followed by a tapered chain of 8-parallel inverter-based drivers and the PA, all biased at half-V_{DD}. The TX output power can be configured from -4 to 4.5 dBm using 8-bit driver and PA switches. Fig. 3.12(b) shows the measured TX power spectrum in the continuous-wave (CW) operation. With the design parameter values listed in Fig. 3.12(a), the T/R switch shows –1.2 dB insertion loss at –4 dBm output power.

3.5.2 Current Starved Ring Oscillator with AFC Loop

To achieve low power operation, a 5-stage current starved ring oscillator with digital AFC [104] is designed (Fig. 3.12(c)). The oscillation frequency, f_{osc}, is controlled by 5-bit coarse- and 5-bit fine-tuned current mirrors from SPI and the AFC loop, respectively, to com-

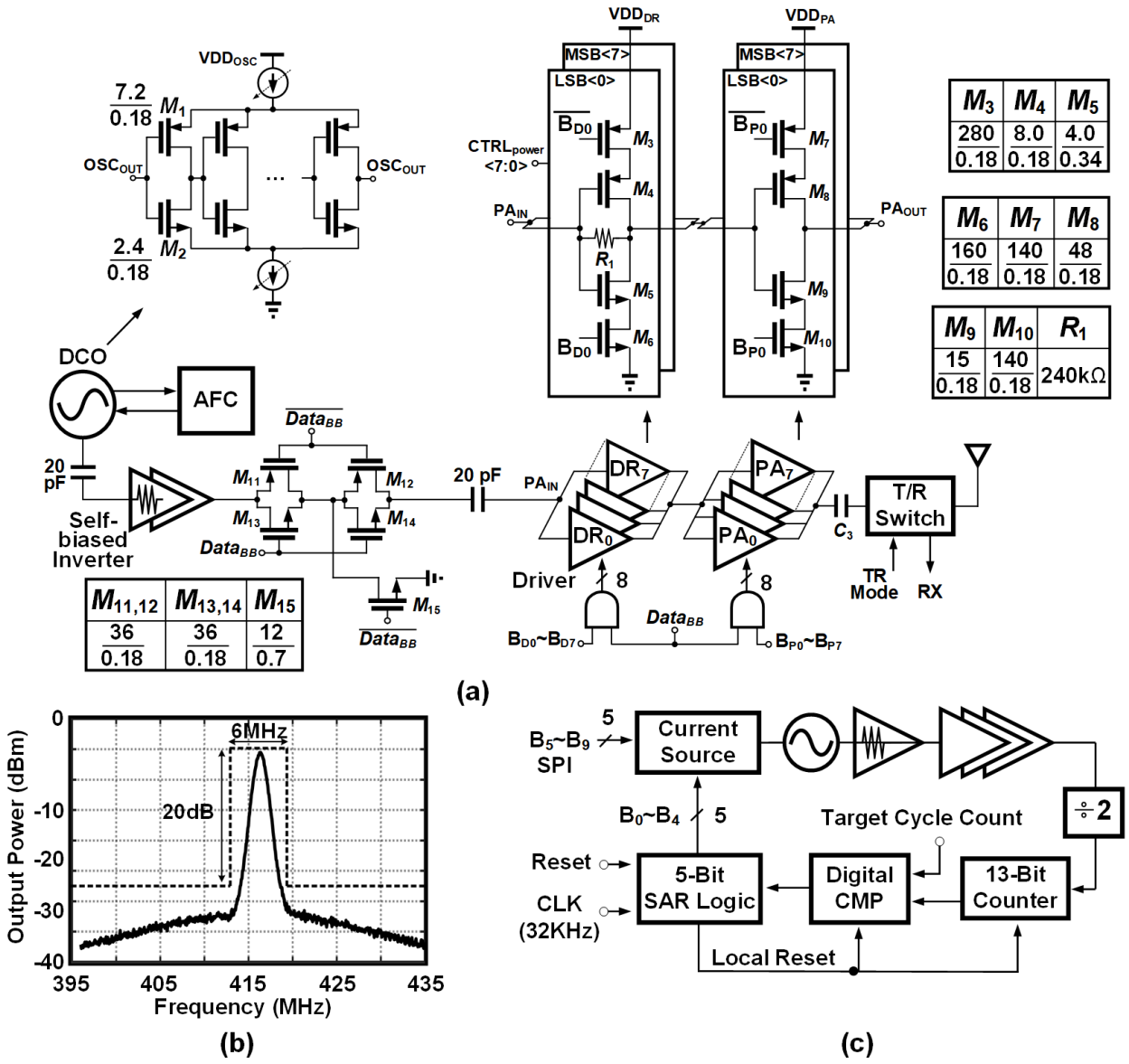


Figure 3.12: (a) The schematic of proposed direct-modulation transmitter. (b) Measured TX output power spectrum. (c) AFC block diagram.

pensate for PVT variations. Within AFC block, the 13-bit counter computes the binary representation of divide-by-two oscillation frequency by counting its cycles over the 32.768 kHz reference clock period from a Pierce crystal oscillator (shared by the RX). The result is compared with the target cycle count N_{CYC}, where $N_{CYC} = f_{osc}/(2f_{XTAL})$, and fed to a SAR logic to adjust the oscillator current. The tuning range is $\Delta f = 2^B LSB$, where LSB is the fine tuning resolution (2.5 MHz in this work) and B is the number of control bits in SAR algorithm (5 in this work). The calibration algorithm allocates one clock period for cycle counting, one for comparison, and one for internal reset. Therefore, the total calibration time T_{cal} is derived as: $T_{cal} = 3 \times B/f_{XTAL}$. For our application, this AFC-backed DCO was implemented to achieve fine-tuning across 80 MHz frequency range within an estimated 0.47 ms calibration time. It is possible to further extend the frequency operation range by increasing the total number of control bits in the calibration system at the expense of a longer calibration time, a larger area and additional power consumption.

3.6 Experimental Results

Designed and fabricated in a 180 nm CMOS technology, this TRX occupies 2.35 × 2.25 mm^2 of die area including pads (Fig. 3.13). The functionality of the TRX was verified by both electrical and *in-vitro* phantom measurements. The system-level measurement include wireless testing for TX-RX distances varying from 25–350 cm as well as wireless transferring of pre-recorded bio-signals. Additionally, coexistence testing in a multi-user environment was conducted.

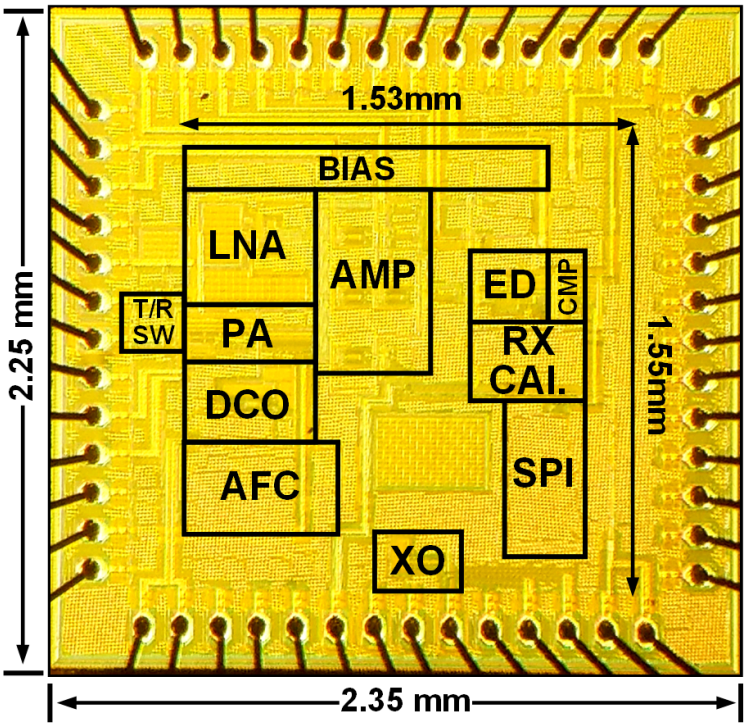


Figure 3.13: Chip micrograph with main circuit blocks labeled.

3.6.1 Receiver Electrical Measurements

Fig. 3.14(a) presents the measured BER at 1- and 10-kbps data-rates using PN15 data sequence at 1.5-V supply voltage. The BER stays below 0.1% for the input power larger than –79 and –74 dBm at 1- and 10-kbps data-rates in the high-gain mode, respectively. Link-budget calculation reveals that to maintain the wireless operation at BER's below 0.1% over short distances down to 25 cm, the RX should tolerate a maximum input power larger than –28.8 dBm. Fig. 3.14(b) shows measured transfer characteristic and BER vs. input power under the RX's low-gain mode. The measured P_{1dB} is –28.5 dBm. Moreover, BER stays below 0.1% for input powers from –62 to –25 dBm, resulting in an overall dynamic range from –79 to –25 dBm across all gain modes. Fig. 3.14(c) shows both simulated and measured NF and S_{11} vs. frequency. The EDSM RX achieves –13.5 dB S_{11} and 4.9 dB NF at 416 MHz, respectively, without any on/off chip inductor.

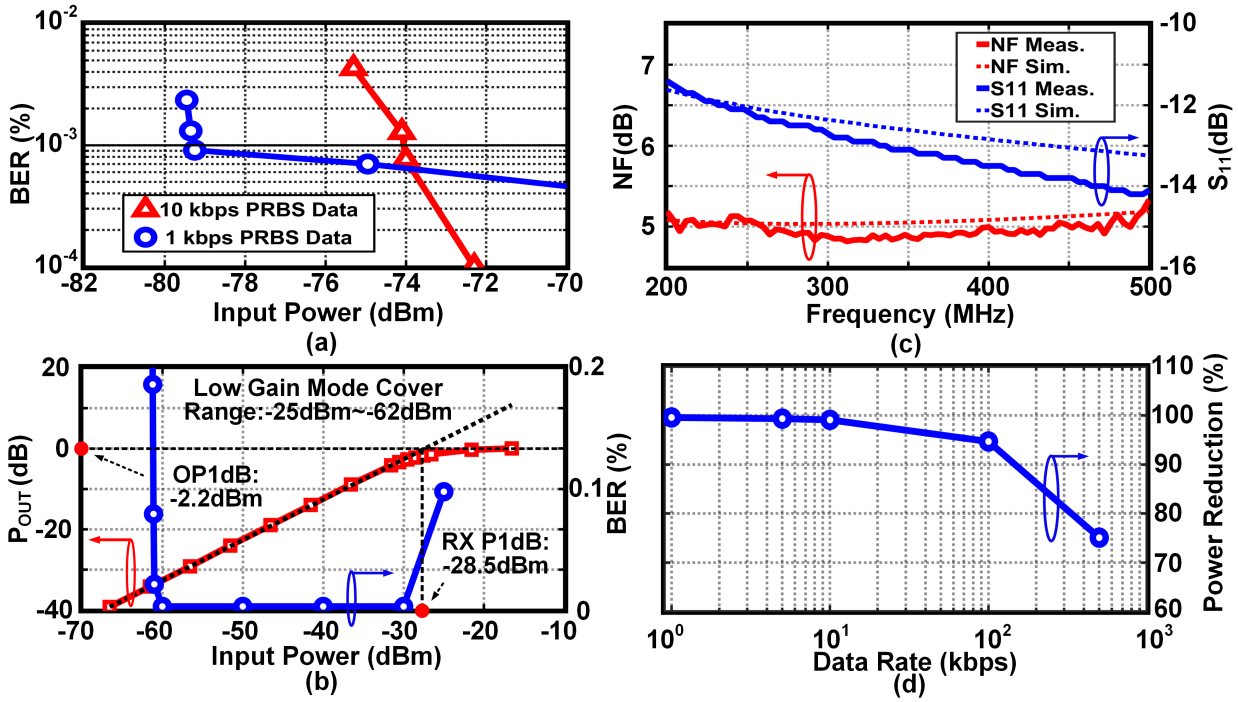


Figure 3.14: RX electrical measurement results: (a) Measured BER with different data-rate. (b) Linearity and BER measurement in low-gain mode. (c) Measured S11 and NF. (d) Input data rate vs. power saving percentage.

Table 3.1 shows the measured power consumption of each RX block before and after applying EDSM technique. The EDSM technique is capable of reducing the RX power by 99.6% to 42 μW at 1 kbps and by 99.1% to 92 μW at 10 kbps. Fig. 3.14(d) demonstrates the power-reduction percentage as a function of the data rate, showing above 90% power reduction at data rates below 100 kbps.

Table 3.1: Measured Transceiver Power Consumption Breakdown

Block	Before EDSM	After EDSM
LNA	5.8 mW	17.3 μW
AMPs	3.8 mW	9.2 μW
BUF+ED	0.6 mW	9.8 μW
CMP	4.2 μW	4.2 μW
Total	10.2 mW	42 μW

Block	OOK Mode
PA	1.69 mW
Driver	0.7 mW
VCO	0.42 mW

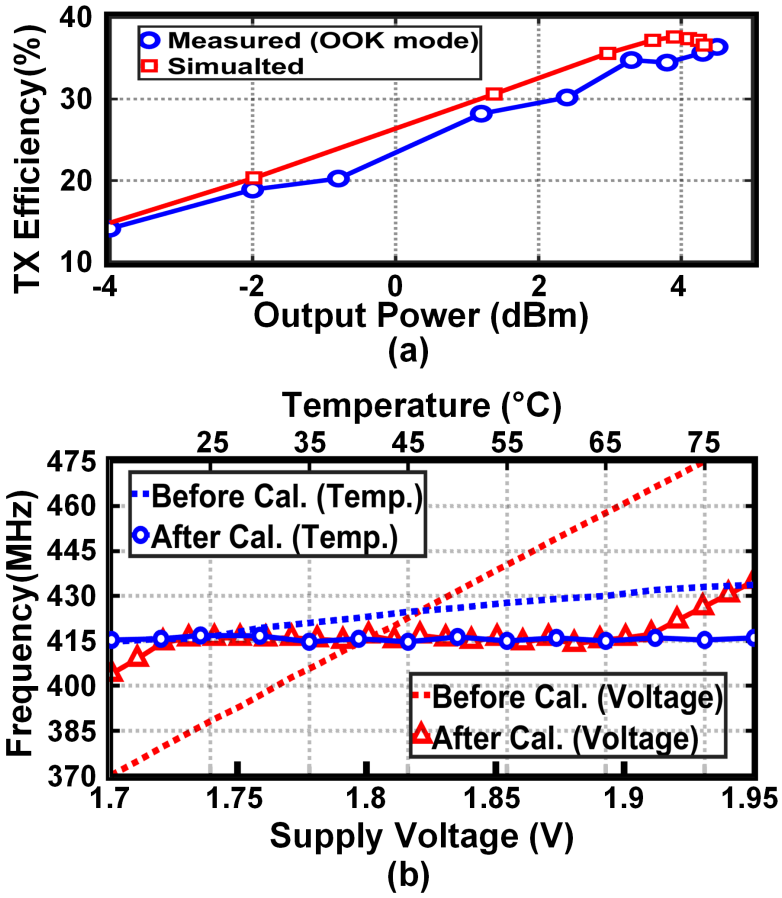


Figure 3.15: (a) TX efficiency vs. output power. (b) Frequency variation before and after using AFC.

3.6.2 Transmitter Electrical Measurements

Fig. 3.15(a) shows both measured and simulated overall TX efficiency vs. output power for OOK modulated signal. The TX output power varies from –4 to 4.5 dBm with efficiency varying from 14% to 36%. In the CW mode, the efficiency varies from 7% to 18%, since for half the time the data is 0 and the TX is powered off. TX power breadkdown in the OOK transmission mode is shown in Table 3.1. The AFC periodically monitors the TX carrier frequency. The frequency-drift tolerance is significantly improved from 19% down to 0.24% across 1.73–1.9 V supply interval and from 4.6% down to 0.3% across 15–78°C temperature range (*cf.* Fig. 3.15(b)).

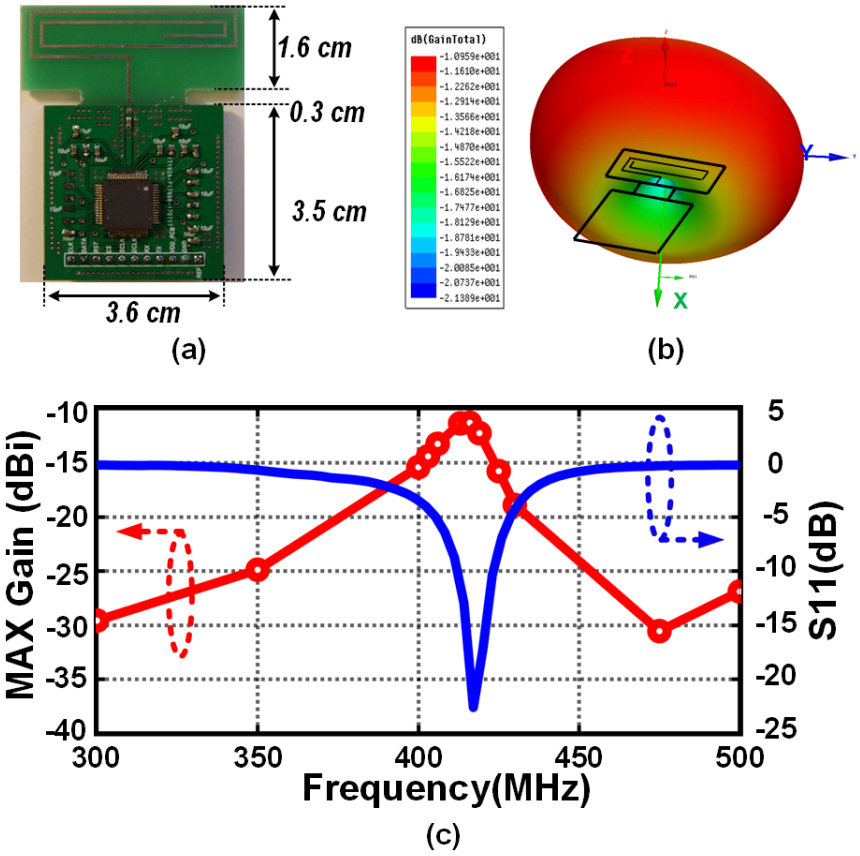


Figure 3.16: (a) PCB including an on-board loop-antenna and TQFP packaged IC. (b) Simulated antenna radiation pattern. (c) Measured antenna gain and S_{11} vs. frequency.

3.6.3 Wireless Connection Measurement Setup and Results

To test wireless connectivity, a 416-MHz PCB loop-antenna was designed and fabricated (Fig. 3.16(a)). Figs. 3.16(b)-(c) demonstrate the simulated radiation pattern at 416 MHz and the measured antenna gain and S_{11} vs. frequency, respectively. As is clear from Fig. 3.16(c), RF band selectivity is partially provided by the antenna. With an emission power of –16 dBm from TX, an antenna gain of –12 dBi, and considering a 35-dB path loss across a 3 m distance at 416 MHz, the RX sensitivity is smaller than –63 dBm. Fig. 3.17(a) shows the wireless testing setup. With TX-RX distances of 25–350 cm and for 1–10 kbps data rates, the measured BER always remains <0.1% (Fig. 3.17(b)). The other wireless testing of the TRX is established by transferring pre-recorded electrocorticogram (ECoG) and electromyogram

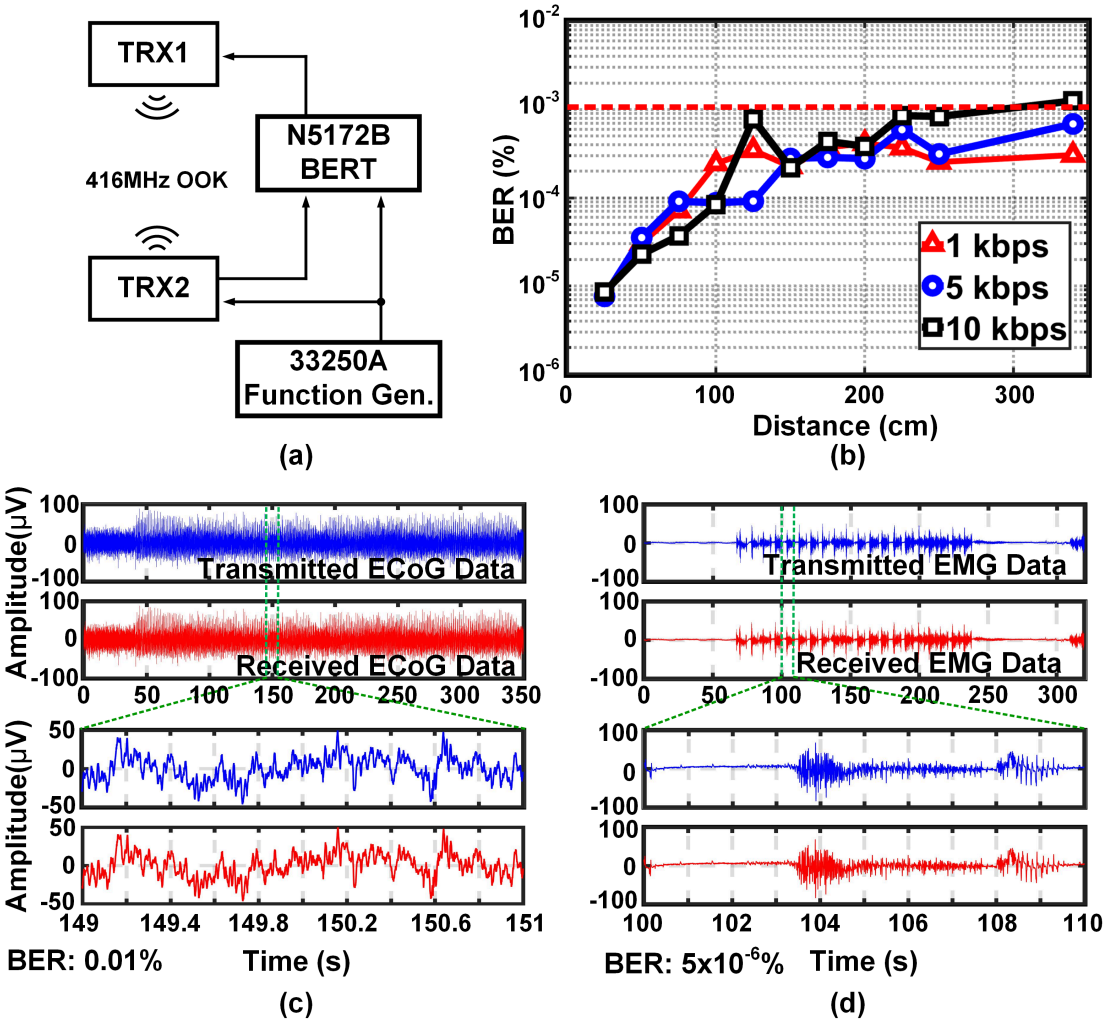


Figure 3.17: (a) The setup for wireless connection measurement. (b) The measured BER with different TX-to-RX distance. The transmitted and received (c) ECoG signal. (d) EMG signal.

(EMG) signals at 1-m distance. The transmitted and received time-domain plots of ECoG and EMG signals with BER below 0.01% and 5×10^{-6}% are shown in Figs. 3.17(c) and (d), respectively.

3.6.4 Multi-User Coexistence and Interference Testing

It is commonly known that the path loss and wireless signal energy absorption of the human tissue increase with frequency. For example, the human tissue (composed of 2-cm skin and

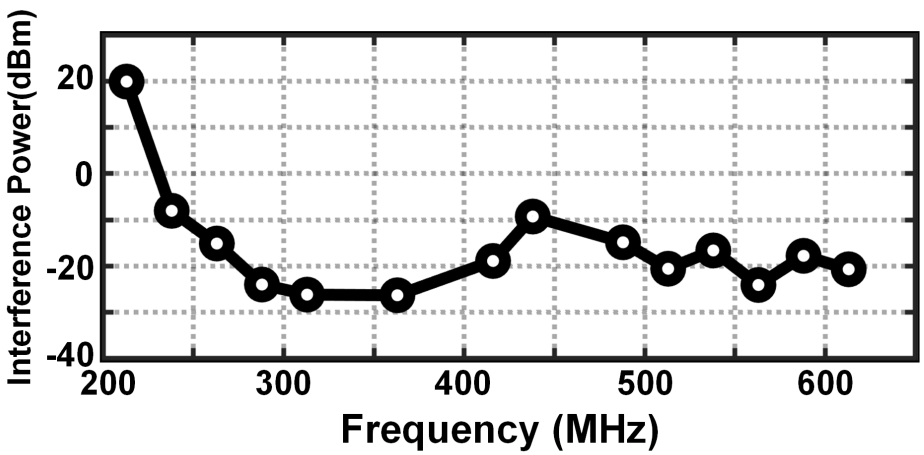


Figure 3.18: The measured interference power causing BER higher than 0.1%

fat) causes ∼63 dB attenuation for 2.4-GHz frequency band of standards such as WBAN, bluetooth and IEEE802.11b/g [105]. In addition, accounting for 26 dB free-space path loss over 20-cm distance and less than –30 dB antenna gain, the received signal falls below RX sensitivity. Another major issue that BMI systems encounter is the interference between multiple MedRadio-band users operating in the vicinity of one another. Fig. 3.18 presents the measured interference power over a wide frequency range that causes a BER higher than 0.1%. Compared to other architectures with high-Q internal/external passive components, this inductorless design exhibits a lower interference tolerance. To address this issue, we notice that MedRadio has limited the transmission time of TXs to 0.1% during a specific period. This notion was utilized to implement a listen-before-talk (LBT) protocol with the TRX operating in the burst-mode data transfer (*cf.* Fig. 3.19(a)). This protocol advances through 10 time-slots in search of an available slot in the presence of an interferer, TRX3, for exclusive pairing of TRX1 and TRX2. A typical coexistence scenario is demonstrated in Fig. 3.19(b), where the TRX3-TRX2 distance is shorter than the TRX1-TRX2 distance by 0.5 m. This protocol improves BER from 4.53% (continuous mode) down to 0.03% (LBT). Although not implemented here, a frequency-domain LBT protocol can also be adopted as envisioned in the MedRadio standard. This is possible due to wideband operation and large tuning range of this TRX. For the BMI application targeted in this design, wireless

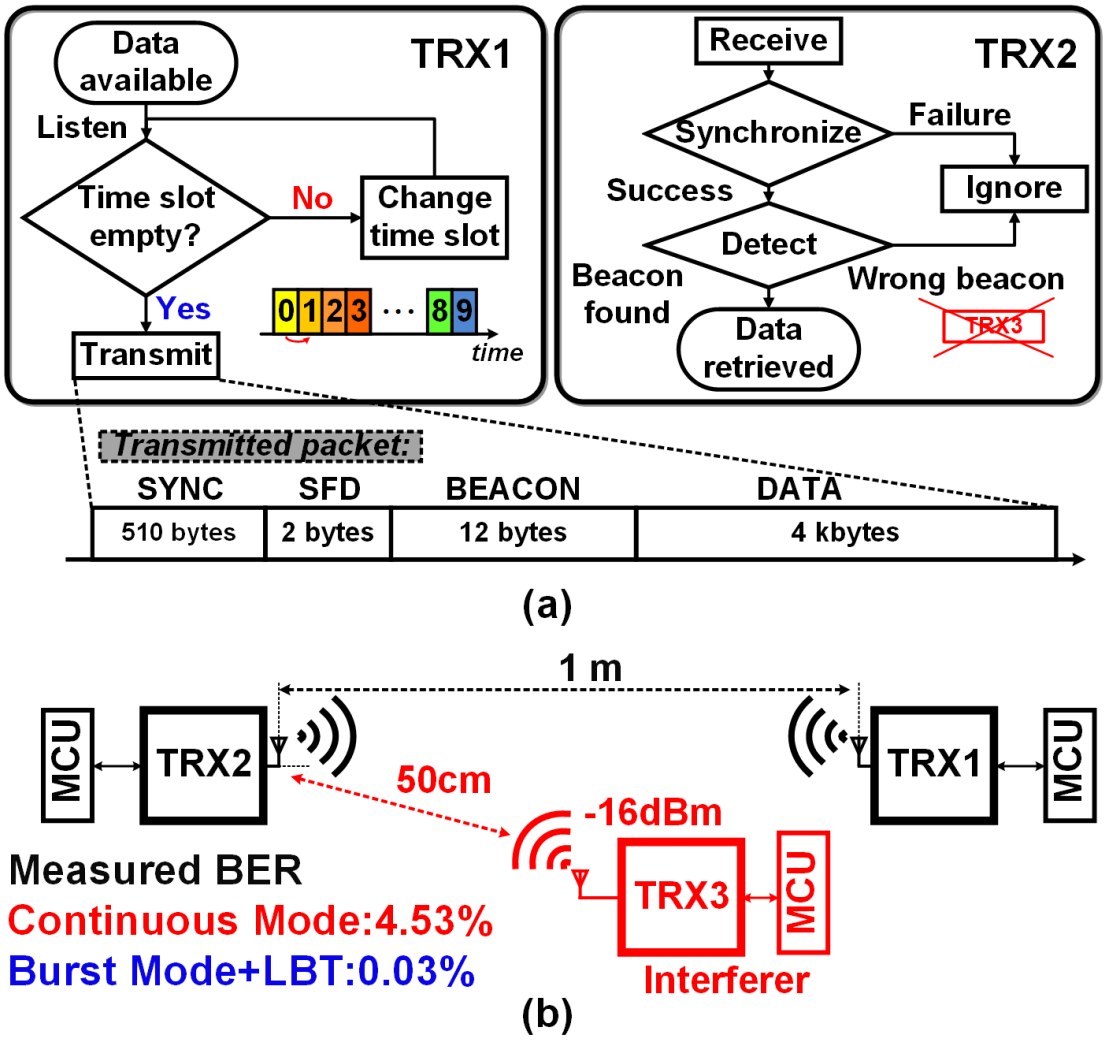


Figure 3.19: (a) The flowchart of listen-before-talk protocol adopted in this work and (b) coexistence test setup.

communication is primarily intended for transferring a limited number of commands, thus the BER degradation due to the interferers can be further reduced in the backend processor by introducing redundancy in the command data package.

3.6.5 *in-vitro* Phantom Measurements

Figs. 3.20(a) and (b) present the *in-vitro* wireless connection setup and cross-section of the phantom material, respectively. The dimensions of titanium enclosure and plastic cap

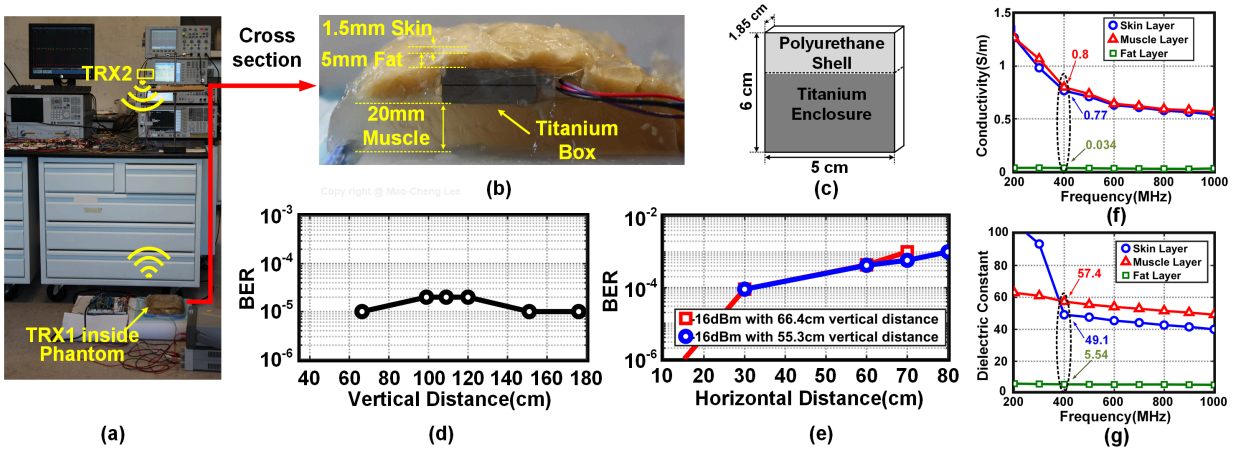


Figure 3.20: (a) *in-vitro* phantom measurement setup. (b) The cross-section of the phantom material. (c) The dimension of titanium box and plastic cap. (d) The measured BER results with different vertical distance. (e) The measured BER results with different horizontal distance. (f) Phantom layers conductivity vs. frequency. (g) Phantom layers dielectric constant vs. frequency.

is shown in Fig. 3.20(c). A phantom composed of 3 layers, emulating the conductivity, permittivity and thickness of the human skin, fat, and muscle in chest area [106, 107] is used to emulate the signal attenuation through human tissue. The measured conductivity of skin, fat and muscle layers are 0.77, 0.034, 0.8 S/m, respectively. The measured permittivity of each corresponding layer is 49.1, 5.54 and 57.4, as indicated in Figs. 3.20(f) and (g). Wireless connectivity was evaluated by positioning TX and RX at various horizontal and vertical distances. The BER remains <0.1% for a maximum vertical distance of 1.8 m. Similarly, the BER remains <0.1% for a maximum horizontal distance of 0.8 m while the position of TRX2 is fixed (as shown in Fig. 3.20(d) and (e)).

Table 3.2 and Table 3.3 compare the performance of the proposed TRX with prior art. The non-coherent EDSM RX achieves –79/–74 dBm sensitivity and dissipates 42/92 μW at 1/10 kbps, respectively. The TX reaches 14% global efficiency at -4 dBm output power with 9.5 dB tuning range.

Table 3.2: Receiver Performance Comparison

Reference	ISSCC 2011 [108]	JSSC 2012 [89]	ISSCC 2014 [90]	TMTT 2014 [91]	TCAS-I 2016 [92]	JSSC 2016 [86]	JSSC 2016 [88]	JSSC 2019 [23]
Process (nm)	130	90	40	180	180	65	65	180
Carrier Freq. (MHz)	403	915	402∼405 / 420∼450	403/433	402∼405	2400	915	413∼419
Supply Voltage (V)	1	1	1	1.2	0.45	0.5	1	1.5
Architecture	Low-IF	2-Tones	Zero-IF	Direct Conv.	Low-IF	Dual-IF	TX-referenced	EDSM
Modulation	FSK	OOK	GMSK/DBPSK	ASK	OOK/FSK	OOK	BPSK	OOK
Inductor Type	Off-Chip	On-Chip	Off-Chip	Off-Chip	On-Chip	Off-Chip	Off-Chip	None
Data Rate (kbps)	200	10	11.7/562/4500	10	50/120	10	10	1/10
Sensitivity (dBm)	–70/–90	–56/–83	–112/–93/–83	–72/–73	–55/–53.5	–97	–76	–79/–74
Power μW	44/120	63[a]/120[a]	2190	2190	352	99	135	42/92

[a]Excluding FPGA and IF clock generation.

Table 3.3: Transmitter Performance Comparison

Reference	ISSCC 2014 [90]	TMTT 2014 [91]	JSSC 2009 [93]	This Work
Process (nm)	40	180	180	180
Carrier Freq. (MHz)	402∼405 420∼450	403	403	413∼419
Supply (V)	1	1.2	1.8	1.8
Architecture	Polar/Direct Mod.	Direct Mod.	Direct Mod.	Direct Mod.
Modulation	GMSK / DBPSK	OOK / OQPSK	FSK	OOK
Inductor Type	Off-Chip	Off-Chip	On-Chip	None
Output Power (dBm)	–10/–17	–20.9/–17	–20∼0	–4∼4.5
Data Rate (kbps)	11/4500	100/1000	50	1/10
Efficiency	NA	NA	33%[a] @-5 dBm	14%(OOK) 7%(CW)
Power (mW)	2.27/2.28	3.32	4.9	2.8[b] 5.6[c]

[a]PA only. [b]With -4 dBm output power in OOK mode. [c]With -4 dBm output power in CW mode.

3.7 Conclusion

A low-power MedRadio OOK TRX in 180 nm CMOS was presented. An event-driven supply modulation (EDSM) technique was introduced to dramatically lower the RX power consumption. Analysis has been done to qualitatively explain the EDSM operation, and to evaluate the noise of the RX and ED properties on the overall performance. A power-cycled TX including a free running oscillator with AFC is demonstrated. The wireless data transfer, interference, multi-user coexistence testing and *in-vitro* phantom measurements also revealed that the TRX can serve as a basis of highly integrated and robust wireless chip, providing a solution for low-power TRX design for an implantable BMI systems.

Chapter 4

A Fast Start-up Crystal Oscillator Using Precise Dithered Injection and Active Inductance

4.1 Introduction

The advent of emerging fields such as body area networks for health care applications and massive wireless sensing for Internet of Things demands ultra-low power electronics to enhance the battery life-time. A common method of reducing the power consumption, increasing the battery life-time, thus eventually enabling battery-less systems is to power cycle the whole system and operate in an intermittent fashion [109],[110],[111]. The wireless sensor nodes primarily constitute a transceiver for communication, an analog-to-digital converter for data conversion and a back-end processing block, all required to be low power. Reference frequency synthesis, digital clock timebase and the carrier frequency generations in these blocks are often realized using a crystal oscillator (XO) [112]. An XO commonly employs

Pierce structure, shown in Fig. 4.1(a), due to its many advantages such as low power consumption, low component count, ease of design, and low phase noise. The start-up time T_S of an XO (few milliseconds for a MHz crystal) constitutes a bottleneck in effectiveness and performance of power cycling schemes, either limiting the system latency or raising the stand-by power.

One approach to reduce stand-by power consumption overhead is to minimize the XO's power dissipation. In [113], a stacked amplifier was used as the XO's active network to increase the inverter's effective transconductance for a given bias current, thus lowering the power dissipation to 19 μW. [114] implemented automatic self power gating (ASPG) and multistage inverter for negative resistance (MINR) to intermittently power-off and reduce the short circuit current in the oscillator's inverter, thus lowering the power to as low as 9.2 μW. A more efficient way, which further decreases the sleep-mode power of the system, is to duty-cycle the XO and allow it to be active only when needed. This approach, however, would need a mechanism to quickly start and stabilize the XO before the rest of the system is awakened. Therefore, techniques to reduce T_S with minimal energy overhead is of great interest.

A commonly used approach to lower T_S is shown in Fig. 4.1(b), which aims at increasing the active circuitry's negative resistance, R_N, by modifying the inverting amplifier's g_m or the capacitors C_1 and C_2. [115] describes a method in which a minimum load capacitor C_L (defined as $C_L = C_0 + C_1C_2/(C_1 + C_2)$) is applied to the oscillator during start-up and once a stable oscillation is detected, a second capacitor bank is switched in to adjust the frequency and reach the desired steady-state. [116] and [117] implemented a similar concept to reduce T_S as well as startup energy E_S by 13.3× and 6.9×, respectively, without the need to use a start-up sequence. However, this approach causes the oscillation frequency to be pulled away from the target, which results in an increase in T_S, defined as the time taken for XO to settle within a specified frequency error (e.g., ±20 ppm in [116]). [118] presents two techniques to

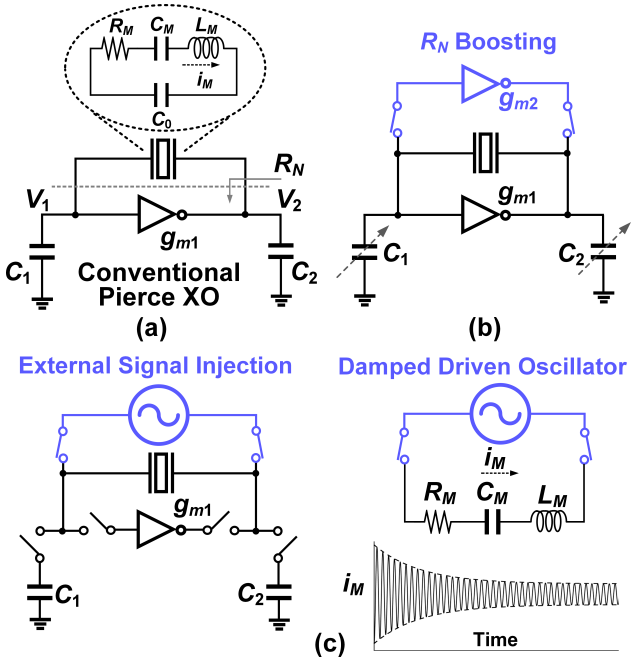


Figure 4.1: (a) Pierce XO (b) boosting negative resistance by modifying capacitors and amplifier's gain (c) kick starting the oscillator using an external periodic source and oscillation amplitude behavior under injection.

reduce T_S, namely, decreasing C_1/C_2 and increasing the current of the inverting amplifier during start-up. Another approach pursued by [119]-[120] is to increase C_L to enhance maximum achievable R_N. To be effective, this approach should be accompanied by increasing the amplifier's gain concurrently, which, in turn, increases E_S. If being implemented as a high-gain multi-stage circuit [114, 119, 121], the inverting amplifier can introduce a significant phase shift which varies over process, voltage and temperature (PVT). This phase shift may pull the XO frequency to even below the crystal's series resonance frequency ω_S so as to make the overall phase shift around the loop 360°, compromising the XO frequency stability and accuracy. Furthermore, under this condition, the crystal no longer behaves inductively and is forced to oscillate below the frequency it is calibrated for. Due to this problem [121] proposed to use two different amplifiers, one for start-up and another for steady-state operation.

Among several existing techniques, external signal injection is widely used to minimize T_S. For this technique to be effective though, the injected signal frequency should be close to

the XO resonance frequency (e.g., within ±0.25%). Several implementations of this method have been proposed, each with various degrees of success. [122] proposes a calibration system where proper frequency setting for a tunable oscillator is determined to help quickly start the XO by precise signal injection. A similar method was presented in [123], where a ring oscillator with a calibration circuitry injects a precise signal to reduce T_S of a 32 MHz Pierce XO to 50 μs. [124] introduced a dithering technique to compensate for the frequency variations over process and temperature, and reduced T_S of a 24 MHz XO to 64 μs. For a PVT-robust injection, [125] proposed a chirp injection (CI) mechanism to sweep the injection frequency around the crystal's resonance frequency. Another CI technique was proposed in [121] to reduce the area occupied by the chirp signal generator. To improve the signal injection accuracy, [126] proposed a 3-step initialization sequence. In the first step, a coarsely tuned (±0.5% frequency accuracy) ring oscillator increases the XO amplitude to 0.2 V. In the second step, a phase-locked loop (PLL) aligns the ring oscillator frequency to within 20 ppm of the XO resonance frequency, and finally, applies the injection again in the last step. T_S is reduced to 19 μs, a 31.5× improvement compared to normal start-up condition. In order to continuously drive the crystal with an external oscillator, [127] proposed synchronized signal injection technique. Since there is frequency offset between the injection signal and crystal resonance, the phase difference between the two accumulates over time, which results in the injection signal counteracting the crystal resonance. The underlying idea in [127] is to realign the phase of the injection signal and the crystal resonance periodically to avoid this phase accumulation. For a 0.75 V steady-state differential amplitude (0.37 V single ended), T_S = 23 μs and E_S = 20.2 nJ. A precisely-timed injection method was presented in [128] and analysis was provided to determine the optimum duration of injection. It also implemented a voltage regulation loop to limit the oscillation amplitude to ≈ 0.2 V (at the cost of higher phase noise) and achieved a T_S of 2 μs. Such small amplitude can easily be built-up through a signal injection over a short time. Furthermore, the regulation loop itself assists the oscillation by providing a larger bias current during the start-up transient and a

smaller one in the steady-state.

4.2 Background and the proposed ideas

It is well known that the envelope of the XO motional current i_M is a direct indication of the oscillation behavior. In this work, a rigorous study of signal injection for XO T_S reduction is presented and the conditions leading to an optimal start-up behavior are derived. It will be proven that precise injection with exactly the same frequency as the crystal's series resonance frequency provides the fastest oscillation start-up. It will also be shown that in reality, due to non-zero injection frequency inaccuracy, this mechanism alone cannot energize the crystal to skip the regenerative process interval. Therefore, another mechanism is needed to minimize this interval and thus lower T_S close to its theoretical lower limit.

In this paper, two techniques are proposed to realize this thought process. Fig. 4.2(a) illustrates the schematic of proposed ideas, namely a relaxation oscillator (RXO) as an injection signal source and an active inductor (AI). The initialization start-up sequence and a symbolic behavior of oscillation amplitude growth is shown in Fig. 4.2(b). In the first phase, ϕ_1, of the start-up sequence, RXO rapidly increases the oscillation amplitude, equivalent to an increase of the start-up initial condition for the XO. In the second phase ϕ_2, RXO is detached while the AI, C_1, C_2 and an additional amplifier are switched in. In the steady-state, only C_1 and C_2 will remain connected to sustain the oscillation.

To be able to achieve a significant reduction in T_S and E_S, a deep understanding into fundamentals of crystal and XO operation is necessary.

The rest of this paper is organized as follows: Section 4.3 presents transient analysis in the presence of a periodic injection signal and studies parameters affecting T_S. It also covers the design and implementation of the RXO. Section 4.4 illustrates the AI method to boost

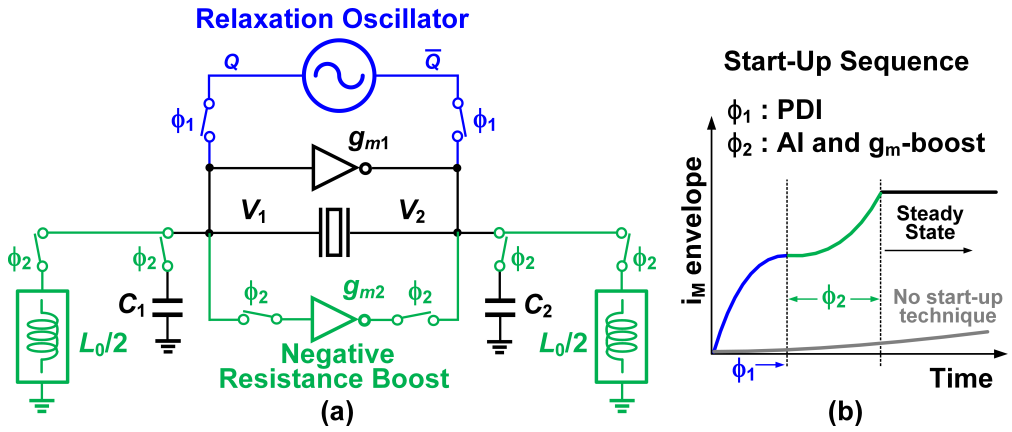


Figure 4.2: (a) Proposed implementation of the fast starting XO (b) oscillation amplitude growth with the start-up aids and without them.

R_N, and elaborates on the design trade-offs and considerations for a robust operation of the AI leading to improvement of the XO start-up time. Section 4.5 discusses measurements of the fabricated XO and its start-up assisting circuitry, and finally, Section 4.6 concludes the paper.

4.3 Precise Dithered Signal Injection

Consider Fig. 4.1(c), demonstrating an external signal injection mechanism for a Pierce XO and i_M behavior under injection. A differential periodic square signal is generated by an external oscillator (e.g., a ring or an RC oscillator), and then is buffered and applied to the crystal. Since a crystal resonator exhibits ultra-high quality factor ($\sim 10^6$) and very narrow bandwidth, it heavily attenuates any applied signal with frequencies not matching its resonance frequency. Thus, only the fundamental component is considered in the Fourier series expansion of the applied signal, while any phase noise around this tone is omitted. We assume zero initial conditions for crystal and only analyze the forced response to a periodic square signal applied at time $t = 0$. This is a valid assumption since, in practice, the initial condition is determined by the oscillator thermal noise. Non-zero initial conditions just

complicate the analysis without adding much circuit insights.

4.3.1 Problem Statement: Damped Driven Oscillator

The characteristic differential equation for a crystal resonator excited by a periodic voltage source (i.e., damped driven oscillator), shown in Fig. 4.1(c), for $t \geq 0$ is:

$$v(t) = \frac{4V_{DD}}{\pi} sin(\omega_{inj} t) = L_M \frac{di_M}{dt} + R_M i_M + \frac{1}{C_M} \int_0^t i_M d\tau \tag{4.1}$$

where ω_{inj} is the injection frequency. L_M, R_M, and C_M are motional inductor, resistor and capacitor of the crystal, respectively. With zero initial conditions, taking the derivative of (4.1) results in:

$$\frac{4V_{DD}\omega_{inj}}{\pi L_M} cos(\omega_{inj} t) = \frac{d^2 i_M}{dt^2} + 2\alpha \frac{di_M}{dt} + \omega_S^2 i_M \tag{4.2}$$

where $\alpha = R_M/2L_M$ and $\omega_S = 1/\sqrt{L_M C_M}$. Taking the Laplace transform and then using its convolution property, i_M is derived as:

$$i_M(t) = \frac{4V_{DD}\omega_{inj}}{\pi L_M \omega_d} \int_0^t e^{-\alpha(t-x)} sin(\omega_d (t-x)) cos(\omega_{inj} x) dx \tag{4.3}$$

where $\omega_d = \sqrt{\omega_S^2 - \alpha^2}$ is the damped natural frequency. Note that for crystal resonators, $\alpha \ll \omega_S$, hence, $\omega_d \simeq \omega_S$. Using trigonometric identities, the integration in (4.3) is expanded, i.e.,

$$\begin{aligned} i_M(t) = {} & \frac{2V_{DD}\omega_{inj}}{\pi L_M \omega_d} e^{-\alpha t} sin(\omega_d t) \times \Big[\int_0^t e^{\alpha x} cos((\omega_d - \omega_{inj})x) dx - \int_0^t e^{\alpha x} cos((\omega_d + \omega_{inj})x) dx \Big] \\ & - \frac{2V_{DD}\omega_{inj}}{\pi L_M \omega_d} e^{-\alpha t} cos(\omega_d t) \times \Big[\int_0^t e^{\alpha x} sin((\omega_d - \omega_{inj})x) dx - \int_0^t e^{\alpha x} sin((\omega_d + \omega_{inj})x) dx \Big] \end{aligned} \tag{4.4}$$

The integrals in (4.4) with sum frequency components, $\omega_d + \omega_{inj}$, are contributing negligibly to $i_M(t)$ and are thus ignored. If evaluated for an ideal case of $\omega_d = \omega_{inj}$ for which the crystal amplitude undergoes its fastest growth, (4.5) is readily derived:

$$i_M(t) \simeq i_{M,env}(t) sin(\omega_d t) \tag{4.5}$$

where $i_{M,env}(t)$ denotes the envelope of $i_M(t)$ and is calculated to be:

$$i_{M,env}(t) = \frac{2V_{DD}}{\pi L_M \alpha}\big(1 - e^{-\alpha t}\big) = \frac{4V_{DD}}{\pi R_M}\big(1 - e^{-\alpha t}\big) \tag{4.6}$$

T_S is defined as the time when $i_{M,env}(t) = 0.9|I_{M,SS}|$, where $I_{M,SS}$ is the steady-state magnitude of i_M. It has been shown that at this time instance, the oscillation frequency has also settled within the required accuracy for most communication standards [125**?**]. The minimum achievable start-up time, $T_{S,min}$, in the XO is thus obtained from (4.6), and is equal to

$$T_{S,min} = \frac{2L_M}{R_M} \ln(1 - \frac{\pi R_M}{4V_{DD}} \times 0.9|I_{M,SS}|)^{-1} \tag{4.7}$$

It is instructive to acquire a quantitative insight into $T_{S,min}$ using (4.7) for the widely used Pierce XO. As demonstrated in [129], in steady-state:

$$|I_{M,SS}| \simeq 0.5\Big(1 + \frac{C_0}{C_S}\Big)\omega_{osc} C_1 |V_1| \tag{4.8}$$

where $\omega_{osc} = \omega_S(1 + C_M/2C_L)$ is the oscillation frequency, V_1 denotes the input voltage of the inverting amplifier, and C_S is the series combination of C_1 and C_2 in Fig. 4.1(a). For a sample 48 MHz crystal with parameters: $C_M = 4$ fF, $L_M = 2.749$ mH, $R_M = 15\ \Omega$, $C_L = 8$ pF, $C_0 = 2$ pF and $|V_1| = V_{DD}$, $T_{S,min}$ is calculated to be 11.9 μs.

Now, assuming an injection frequency inaccuracy of $\Delta\omega = \omega_d - \omega_{inj}$, $i_M(t)$ becomes:

$$\begin{aligned} i_M(t) = \frac{2V_{DD}\omega_{inj}}{\pi L_M \omega_d(\alpha^2+\Delta\omega^2)} sin(\omega_d t) \times \Big[\alpha cos(\Delta\omega t) + \Delta\omega sin(\Delta\omega t) - \alpha e^{-\alpha t}\Big] - \\ \frac{2V_{DD}\omega_{inj}}{\pi L_M \omega_d(\alpha^2+\Delta\omega^2)} cos(\omega_d t) \times \Big[\alpha sin(\Delta\omega t) - \Delta\omega cos(\Delta\omega t) + \Delta\omega e^{-\alpha t}\Big] \end{aligned} \tag{4.9}$$

In practice, even for an integrated oscillator carefully designed to produce a precise injection frequency, it is still difficult for ω_{inj} to be within $\pm 0.1\%$ of ω_d across PVT variations (e.g. for typical crystals operating in the MHz range, $\alpha \sim$ 1–10 kHz while $\Delta\omega \sim$ 0.1–1 Mrad/s); hence, $\alpha \ll \Delta\omega$. Therefore, The expression in (4.9) is reduced to:

$$i_M(t) \simeq \frac{2V_{DD}}{\pi L_M \Delta\omega}\big(1 - \frac{\Delta\omega}{\omega_d}\big) \times \Big[sin(\omega_d t)sin(\Delta\omega t) + cos(\omega_d t)\big(cos(\Delta\omega t) - e^{-\alpha t}\big)\Big] \tag{4.10}$$

4.3.2 Analysis of the Motional Current's Envelope

To calculate the envelope of $i_M(t)$ in (4.10), Hilbert transform is invoked. For an arbitrary waveform $v(t)$ a complex signal $z(t) = v(t) + j\hat{v}(t)$ is defined, where

$$\hat{v}(t) \equiv H\big[v(t)\big] = v(t) * \frac{1}{t} = \frac{1}{\pi}\int_{-\infty}^{\infty} \frac{v(\lambda)}{t-\lambda} d\lambda \tag{4.11}$$

is the Hilbert transform of $v(t)$. It is proved that the magnitude of $z(t)$ is the envelope of $v(t)$, i.e., $v_{env}(t) = |z(t)| = \sqrt{v^2(t) + \hat{v}^2(t)}$. For clarity, (4.10) is rewritten as:

$$i_M(t) = K\Big[x(t)cos(\omega_d t) + y(t)sin(\omega_d t)\Big] \tag{4.12}$$

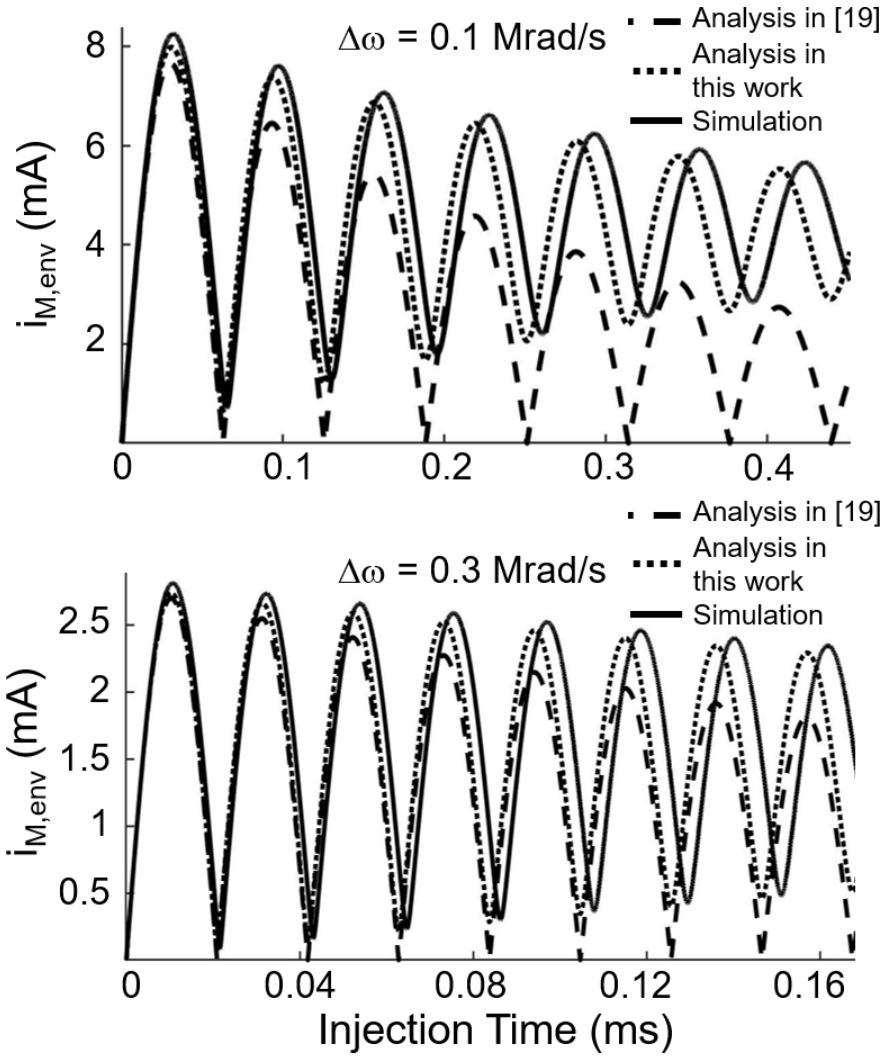


Figure 4.3: Envelope of the i_M for $\Delta\omega = 0.1$ and 0.3 Mrad/s.

where

$$K = \frac{2V_{DD}}{\pi L_M \Delta\omega}\left(1 - \frac{\Delta\omega}{\omega_d}\right)$$
$$x(t) = cos(\Delta\omega t) - e^{-\alpha t}, y(t) = sin(\Delta\omega t) \tag{4.13}$$

$\hat{i}_M(t)$ is derived as:

$$\hat{i}_M(t) = K\Big[x(t)sin(\omega_d t) - y(t)cos(\omega_d t)\Big] \tag{4.14}$$

The envelope of $i_M(t)$ is thus readily calculated from (4.12) and (4.14):

$$i_{M,env}(t) = K\sqrt{x^2(t) + y^2(t)} = \frac{2V_{DD}}{\pi L_M \Delta\omega}\left(1 - \frac{\Delta\omega}{\omega_d}\right)\sqrt{1 + e^{-2\alpha t} - 2cos(\Delta\omega t)e^{-\alpha t}} \tag{4.15}$$

A consequence of the condition $\alpha \ll \Delta\omega$ is that it is unlikely the injection oscillator alone can build up the oscillation amplitude of the Pierce XO all the way to its steady-state, unless the steady-state amplitude is made small (e.g., $<0.2V_{DD}$, as was done in [128, 130]). Therefore, $i_{M,env}(t)$ after injection is smaller than $I_{M,SS}$ and other techniques need to complement the signal injection, as was carried out by [125] and [121]. Following the excitation period, the crystal is detached from the external source and connected to the inverting amplifier.

Fig. 4.3 compares the time-domain variation of $i_{M,env}(t)$ obtained from both simulation and calculation (i.e., Eq. (4.15)) of crystal resonator under injection for two values of $\Delta\omega = 0.1, 0.3$ Mrad/s, validating the proposed analysis. For comparison, the $i_{M,env}(t)$ variation with injection time obtained from analysis in [128] (for the same circuit conditions and the same crystal model) is overlayed on the same figure. [128] approximates the frequency response of crystal with an impulse function, only a valid approximation for small T_{inj}. On the contrary, the proposed dynamic analysis of the crystals motional current is based on the characteristic differential equation of the crystal with no assumption about its frequency- and/or time-domain responses.

For T_S to get sufficiently close to $T_{S,min}$, the injection should cease when $i_{M,env}(t)$ in Eq. (4.15) is at its maximum (*cf.* Fig. 4.3). This optimum injection time, T_{OPT}, is calculated to be $T_{OPT} \simeq \pi/\Delta\omega$. Moreover, the maximum of $i_{M,env}(t)$ is:

$$i_{M,env}(t)_{max} \simeq \frac{4V_{DD}}{\pi L_M \Delta\omega}\big(1 - \frac{\Delta\omega}{\omega_d}\big) \tag{4.16}$$

It is inferred that for crystals with high Q-factors or injection sources with poor frequency accuracy, $i_{M,env}(t)$ assumes smaller values for $t \leq T_{OPT}$, an intuitively expected result.

In the case that injection oscillator's frequency is close to ω_d, it can be readily proved that so long as $\Delta\omega<(4C_M/\pi C_L)\omega_{osc}$, the injection mechanism alone is capable of bringing the oscillation amplitude to its steady-state.

4.3.3 Sensitivity to Timing and Injection Frequency Inaccuracies

It was shown in the previous sub-section that injection should be stopped once $i_{M,env}$ reaches its peak value to minimize T_S. Two phenomena affect T_S, namely, inaccurate injection frequency ($\Delta\omega$) and time (T_{inj}). Recall that $i_{M,env}(t)$ exhibits a damped sinusoidal characteristic, as shown in Fig. 4.3. Thus, at the time when $i_{M,env}(t)$ is at maximum, its time-derivative is at minimum, which in turn lowers the impact of injection duration inaccuracy on T_S. This is in contrast with the injection approach in [128], where the injection is stopped before the envelope reaches its maximum. In case the oscillation amplitude has not reached its steady-state at the end of injection period, it will grow exponentially by the amplifier:

$$i_M(t) = i_{M,env}(T_{inj})e^{(t-T_{inj})/\tau}u(t-T_{inj}), \tau = \frac{-2L_M}{R_M + R_N} \tag{4.17}$$

where $u(t)$ is the unit step function. To derive a closed-form expression for T_S, we assume the amplifier remains linear and retains a constant R_N as the amplitude grows. Combining (4.8) and (4.17) yields

$$T_A = \tau \ln \frac{0.9(C_S + C_0)\omega_{osc}V_{DD}}{i_{M,env}(T_{inj})}, T_S = T_{inj} + T_A \tag{4.18}$$

where T_A is the time taken for the amplitude to grow toward its steady-state after injection. Combining (4.16) and (4.18), the effect of $\Delta\omega$ on T_S is calculated:

$$T_S \simeq \frac{\pi}{|\Delta\omega|} + \tau \ln \left[0.7L_M(C_S + C_0)\omega_{osc}|\Delta\omega|\right] \tag{4.19}$$

Fig. 4.4 demonstrates the sensitivity of T_S to $\Delta\omega$ for the sample 48-MHz quartz crystal, based on quantitative evaluation of (4.16) and (4.19). Evaluating the effect of each term of (4.19) on T_S, if $\Delta\omega$ or crystal's Q-factor are small, the first term will be dominant. On the other hand, as the oscillation amplitude becomes large, the active circuitry becomes

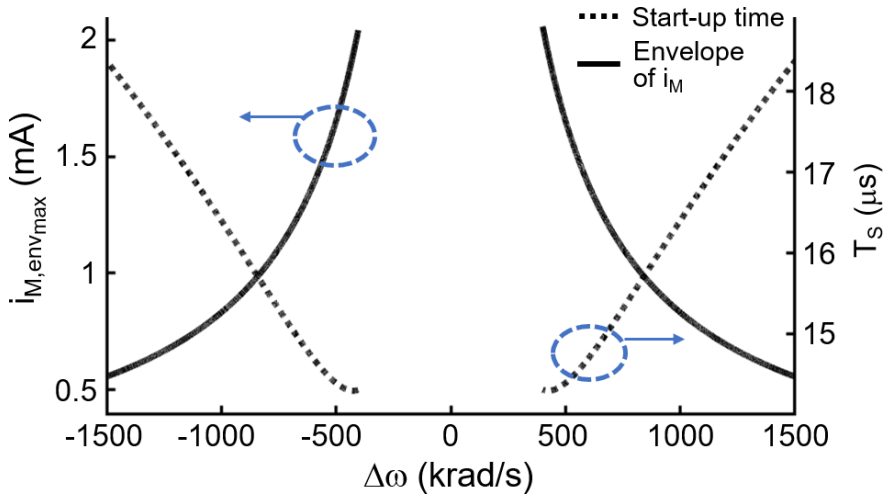


Figure 4.4: Effect of injection frequency inaccuracy on maximum value of $i_{M,env}$ and overall T_S, given injection stops at $t = T_{OPT}$ and $R_N = 50R_M$.

nonlinear. Therefore, τ starts to get larger and the second term in (4.19) may dominate T_S. Similarly, larger Q-factors also increase the contribution of the second term on T_S. To reduce the effect of $\Delta\omega$ on T_S, one can lower τ to reduce T_S and its sensitivity to inaccurate frequency errors. To evaluate the sensitivity of T_S to injection duration errors, the injection oscillator is assumed to be sufficiently precise such that $\Delta\omega$ falls within $\pm 0.15\%$ of ω_d. The frequency of this oscillator is measured and, if required, calibrated before applying to the XO. Based on (4.15) and (4.18), Fig. 4.5 illustrates the variation of T_S with $\Delta\omega$ for four distinct injection times. For injection frequency errors less than 600 krad/s, T_S varies from 14.4- to 20.4-μs as T_{inj} increases from 5- to 8-μs. In practice, the phase-noise-induced frequency skirts around ω_{inj} pump larger energy within the crystal bandwidth compared to an ideal single-tone injection. As will be illustrated in Section 4.3.5, this can be achieved through dithering, and therefore, resulting in lower T_S variation. Moreover, as will be seen in Section 4.4, this sensitivity is further reduced by introducing an AI to the circuit to significantly lower τ.

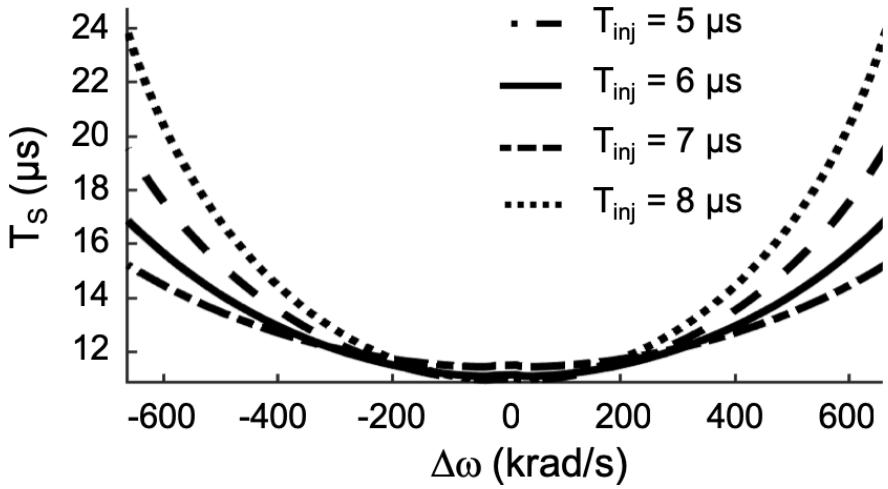


Figure 4.5: Effect of injection timing inaccuracy on overall T_S for the sample crystal parameters. R_N is assumed to be $50R_M$.

4.3.4 Interpretation of the Analysis

From the equations above, a number of observations are made:

- $i_{M,env}(t)_{max}$ can reach twice the final value under continuous injection (steady-state value).
- A smaller $\Delta\omega$ results in larger $i_{M,env}(t)_{max}$, T_{OPT}, and $i_{M,env}(t)$ during the start-up interval $0 < t < T_{OPT}$.
- To the first order, T_{OPT} is only a function of injection signal accuracy and not the crystal properties. In actual implementations, $\Delta\omega$ is larger for crystals with higher operating frequencies. This is because it becomes increasingly more difficult to guarantee the accuracy of an integrated oscillator as frequency rises.
- It can also be shown that smaller $\Delta\omega$ leads to larger local minimums for $i_{M,env}(t)$, an effect not predicted in [128] (see Fig. 4.3).

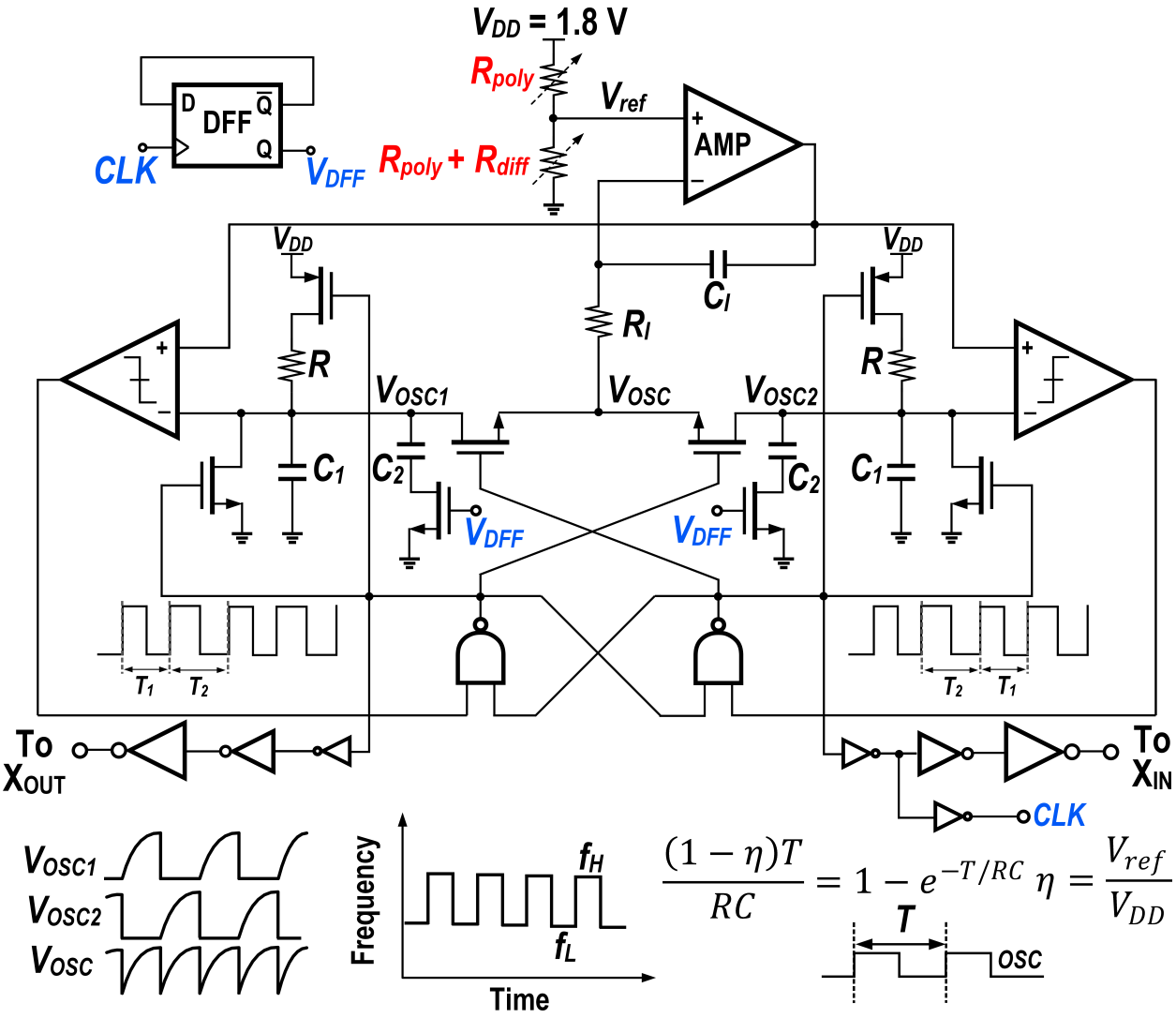


Figure 4.6: RXO circuit implementation.

4.3.5 Relaxation Oscillator Implementation

Among various candidates to create injection signal, ring oscillators have been used extensively, providing features such as fast turn-on time, small area and power dissipation at the cost of large PVT susceptibility and low frequency precision. Alternatively, this work employs an RXO, which provides a more precise injection, as its frequency depends on an easily tunable *RC* time constant instead of transistor parameters. A modified version of the architecture in [131] is implemented at 48 MHz while maintaining the performance across PVT (Fig. 4.6). To account for the crystals ultra-high Q, the RXO frequency ω_{inj} is modulated

by toggling its capacitance C_2 between 400 fF and 415 fF through an internal feedback, as depicted in Fig. 4.6. Thus, ω_{inj} alters by ±0.25%, slightly spreading the injection signal power spectrum over a wider frequency range and raising the phase noise. This ensures that the RXO contains enough energy across the crystal bandwidth to limit T_S variation over temperature, resulting in a robust start-up behavior. As opposed to [124] where a relatively inaccurate ring oscillator was used, higher frequency accuracy of RXO allows for a lower dithering range of ±0.25%. To reduce RXO frequency variation due to PVT, reference voltage V_{ref} is generated by a resistive voltage division ratio. Series poly and diffusion resistors with complementary temperature coefficients are employed to generate V_{ref}, thereby compensating for the RXO frequency variation due to temperature across process corners [131]. These resistors employ 5 bits of coarse and 4 bits of fine tuning, which translates to 40 kHz of frequency resolution and tuning range from 27 to 84 MHz. Due to several percentage-point variations of on-chip resistors and capacitors, a simulation-assisted initial calibration is inevitable for any signal injection technique including the proposed precise dithered injection (except for the chirp signal injection where the frequency is swept across a wide range). Measurement of this RXO shows frequency variation within ±0.15% over -40–90°C, significantly better than temperature-compensated ring oscillators. Simulations show ±0.2% frequency variation across temperature at different process corners. Furthermore, Monte Carlo simulations of both process and mismatch variations show a sigma of 100 kHz (0.21%) in the nominal corner. The RXO and buffer dissipate 3.6 mW from a 1.8 V supply, a significantly larger value compared to [131] because of higher operation frequency and more stringent specification on its frequency stability which requires smaller comparators' delays. The power would be significantly lower on an advanced technology node or for smaller target frequency.

4.4 Active Inductor

4.4.1 Effects of C_0 on XO Start-up

The presence of the static capacitance C_0 in the crystal greatly influences the XO behavior (*cf.* Fig. 4.1(a)). Besides limiting the pull-ability of XO, it lowers the active circuitry's negative resistance according to [129]:

$$R_N = \frac{-4g_m C_S^2}{(g_m C_0)^2 + 16\omega^2 C_S^2 C_L^2} \tag{4.20}$$

Furthermore, it limits the maximum negative resistance, $R_{N,max}$, and sets an optimum value of amplifier's g_m beyond which R_N will start to decrease (Fig. 4.7).

$$R_{N,max} = \frac{1}{2\omega C_0(1 + C_0/C_S)}, g_{m,opt} = 4C_S\omega\big(1 + C_S/C_0\big) \tag{4.21}$$

Additionally, C_0 poses a limit on how much C_L can be lowered to achieve larger R_N [116], [**?**]. To address the limitation imposed by C_0, [121] proposed a dual-mode g_m scheme, employing one amplifier for start-up (A_{XO-3}) and another one for steady-state (A_{XO-1}) operation. A_{XO-3} is designed to show an inductive reactance X around the XO nominal

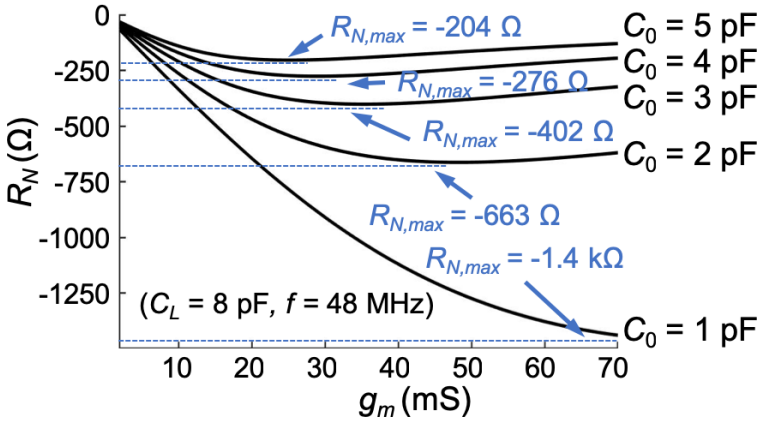


Figure 4.7: Negative resistance and its maximum vs. amplifier transconductance gain for various C_0 values.

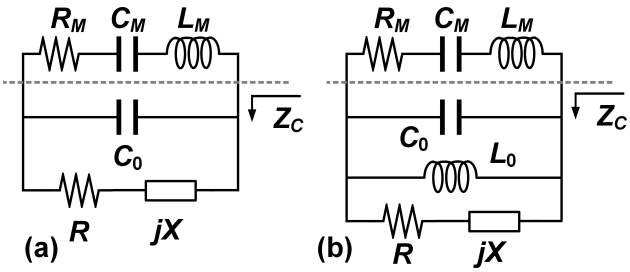


Figure 4.8: One-port linear model of the XOs in (a) [121] and (b) this work.

operation frequency to counteract C_0. Starting with Fig. 4.8(a) which shows a linear model of the XO, the impedance Z_C seen from the motional branch is derived as:

$$Z_C = \frac{R + j\big(X(1 - C_0X\omega) - R^2C_0\omega\big)}{(1 - C_0X\omega)^2 + (RC_0\omega)^2} \tag{4.22}$$

In a conventional design, $X = -1/C_S\omega$ and crystal's motional branch is loaded with $C_S + C_0$. On the other hand, maximizing the real-part of Z_C for the circuit model in Fig. 4.8(a) leads to $X = 1/C_0\omega$, while its imaginary part becomes $-1/C_0\omega$. Therefore, during start-up, when A_{XO-3} is enabled to boost the negative resistance, crystal's motional branch is effectively loaded with an equivalent capacitor of C_0 and ω_{osc} will shift toward ω_p. This frequency drift along with the nonlinearity effects of A_{XO-3} which was pointed out in [121] increase both amplitude and frequency settling times.

4.4.2 Proposed R_N Boosting Method

Fig. 4.8(b) illustrates a simplified linear model for the approach presented in this work. An inductor is explicitly placed in parallel with crystal to maximize the real-part of Z_C for the circuit model in Fig. 4.8(b). Crystal's motional branch is now loaded with

$$Z_C = \frac{Z_{amp}L_0s}{L_0s + Z_{amp}(1 + L_0C_0s^2)}, Z_{amp} = R + jX, \tag{4.23}$$

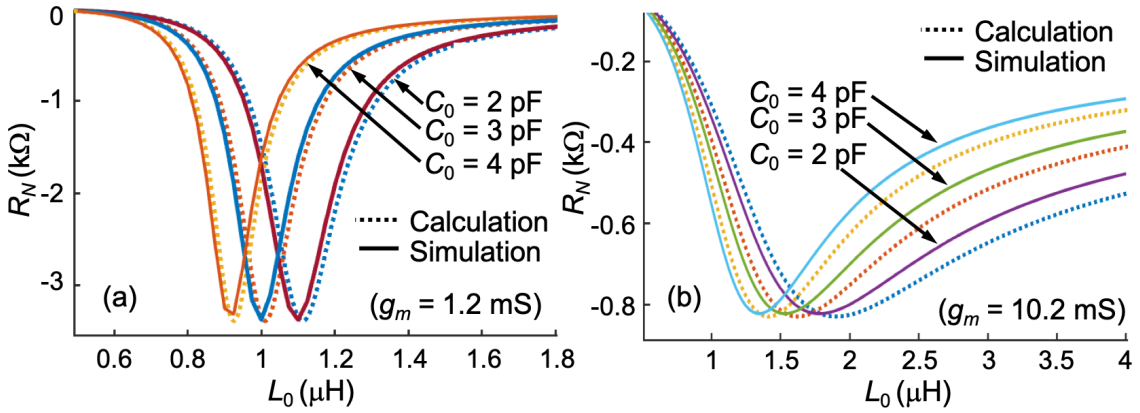


Figure 4.9: R_N at 48 MHz after addition of L_0 for amplifier's transconductance gain of (a) 1.2 mS and (b) 10.2 mS.

with real and imaginary parts expressed as:

$$Re\{Z_C\} = \frac{RL_0^2\omega^2}{R^2(1-L_0C_0\omega^2)^2 + \big(L_0\omega + X(1-L_0C_0\omega^2)\big)^2} \tag{4.24}$$

$$Im\{Z_C\} = \frac{R^2L_0\omega(1-L_0C_0\omega^2) + XL_0\omega\big(L_0\omega + X(1-L_0C_0\omega^2)\big)}{R^2(1-L_0C_0\omega^2)^2 + \big(L_0\omega + X(1-L_0C_0\omega^2)\big)^2} \tag{4.25}$$

L_0 boosts the real part of Z_C, and in contrast to [121], this can be accomplished without imposing any constraints on C_S value or amplifier's characteristic. More precisely, L_0 reduces the effective static capacitance, $C_{0,eff} = C_0[(\omega_0/\omega)^2 - 1]$ (where $\omega_0 = 1/\sqrt{L_0C_0}$), thereby increasing $R_{N,max}$. One may choose to leverage this property to decrease C_S so as to achieve larger R_N. Figs. 4.9(a)-(b) demonstrate both simulated and calculated R_N variation with respect to L_0 under three values of C_0 (i.e., 2-, 3-, 4-pF) and for two g_m values (i.e., 1.2- and 10.2-mS) at 48 MHz, where L_0 is assumed to be an ideal inductor. As shown in the plots, the maximum achievable R_N is larger for an amplifier with a lower g_m. It is also observed that this larger R_N value requires more precise and linear L_0 over PVT variations, which is challenging to realize in practice. Therefore, to reduce the R_N sensitivity to L_0 variation, g_m should be increased (Fig. 4.9(b)).

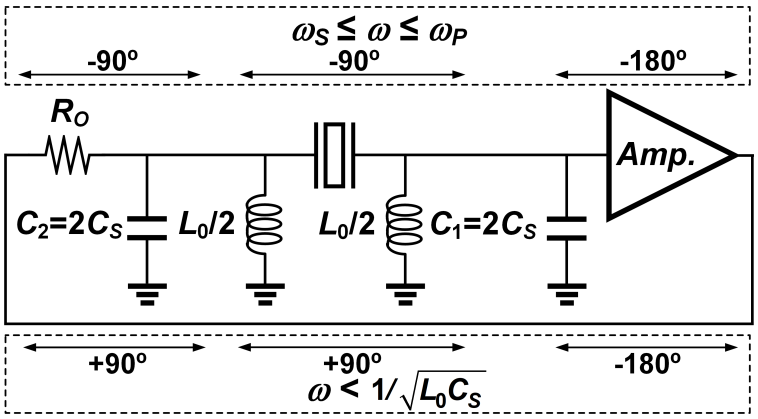


Figure 4.10: Simplified phase shift around the loop of Pierce XO at different frequency ranges.

4.4.3 Design Considerations for Active Inductor Implementation

The addition of L_0 creates the possibility of an unwanted oscillation caused by the resonance through L_0, crystal and the amplifier. A qualitative view is displayed in Fig. 4.10. The AI is decomposed in two equal parts placed on crystal's input and output nodes. For the oscillation to take place, the phase shift across the loop should be $n\times360°$ where n is an integer number. Neglecting the AI first, one can identify a 180° phase lag from the amplifier, a phase lag of about 90° from $R_O - C_2$ and another 90° phase lag from the crystal$-C_1$ at $\omega_{osc} = \omega_S$, where R_O is the amplifier output resistance. On the other hand, in the presence of AIs, the resulting passive network and the crystal form a dual resonance network with two oscillation modes. Besides the oscillation mode at $\omega_{osc} = \omega_S$, the second oscillation mode is created by the 90° phase leads associated with R_O–L_0 and crystal$-L_0$, and a 180° phase lag from the amplifier. With sufficient gain, the loop may in fact oscillate at this parasitic mode. One solution to suppress this mode is to decrease AI's Q-factor; an easily achievable task as the AI's Q-factor is inherently lower than that of monolithic or off-chip components. For better illustration, Fig. 4.11 shows the open-loop (from amplifier's output to its input) gain and phase-shift simulation of the dual-resonance network for two Q-factors.

The AI's Q-factor cannot be arbitrarily low, because it will increase the XO resistive loss. As

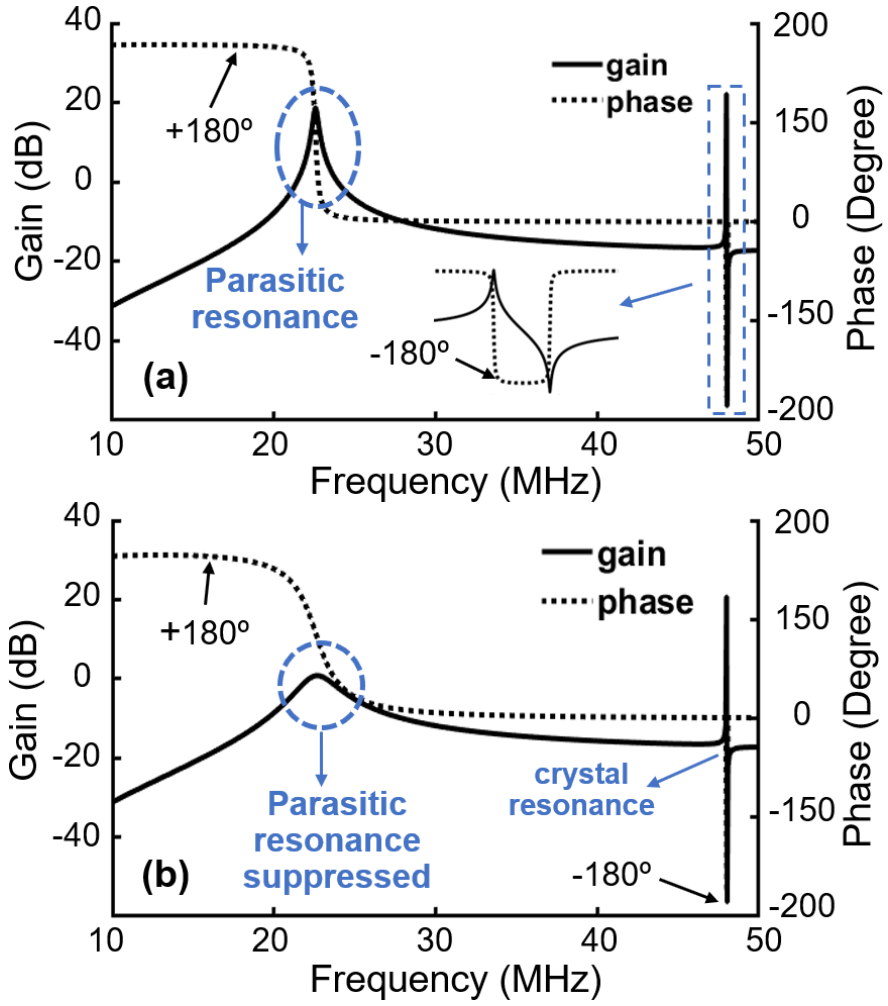


Figure 4.11: (a) Tank frequency response after inclusion of L_0 with a quality factor of (a) 83 and (b) 11.

a secondary measure to ensure the XO oscillation in its desired mode without compromising on the AI's Q-factor, the injection mechanism raises the XO initial condition around ω_S to a value substantially larger than the one provided by thermal noise to the unwanted mode. Once the desired operation takes over, the unwanted mode is automatically eliminated. Another issue is the possibility of operation at one of the crystal's overtones. To prevent this problem, notice that for the feedback to remain positive and oscillation to take place, the reactances at the crystal's input and output in Fig. 4.10 should be of the same sign (e.g., both negative) at the oscillation frequency of interest. Thus, placing half of L_0 on both sides of the XO guarantees this condition to satisfy at the fundamental frequency.

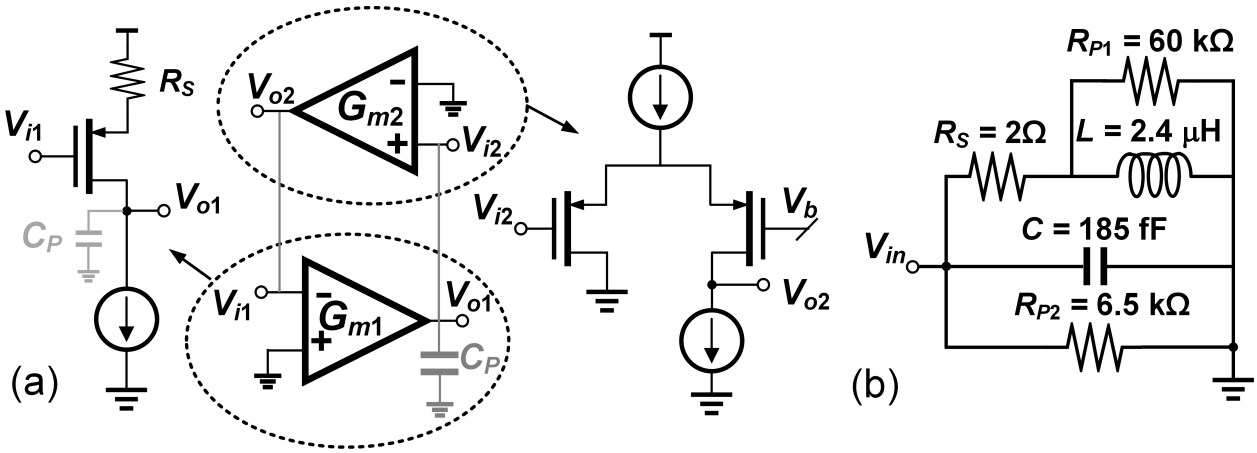


Figure 4.12: AI implementation concept: (a) constructing positive and negative transconductances (b) approximate model of the actual design.

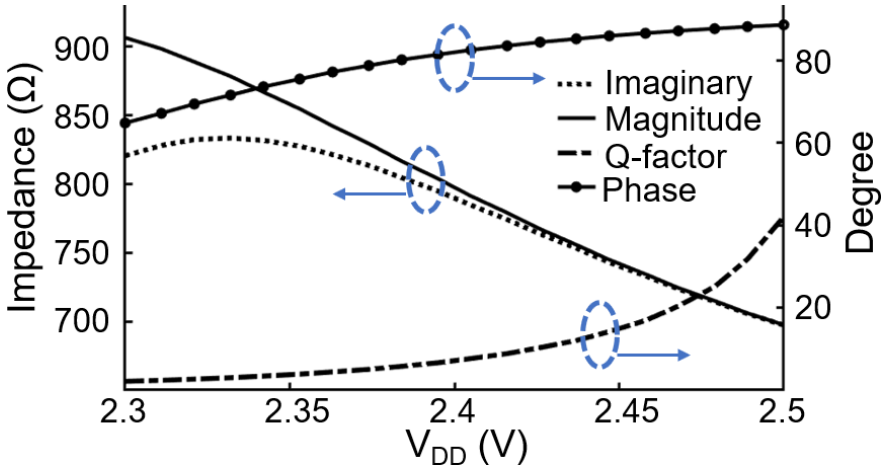


Figure 4.13: AI input impedance characteristics at 48 MHz across supply.

Finally, when it comes to the XO circuit design, comprehensive transient and spectral simulations have been performed to account for all the nonidealities (e.g., amplifier gain and bandwidth, nonlinearity and frequency response of AI).

4.4.4 Circuit Implementation

Fig. 4.12(a) shows the building blocks of the gyrator-C AI. The negative transconductance is a degenerated common-source stage and the positive one is a source-coupled structure. These blocks provide large input and output impedances, thereby increasing the Q-factor of

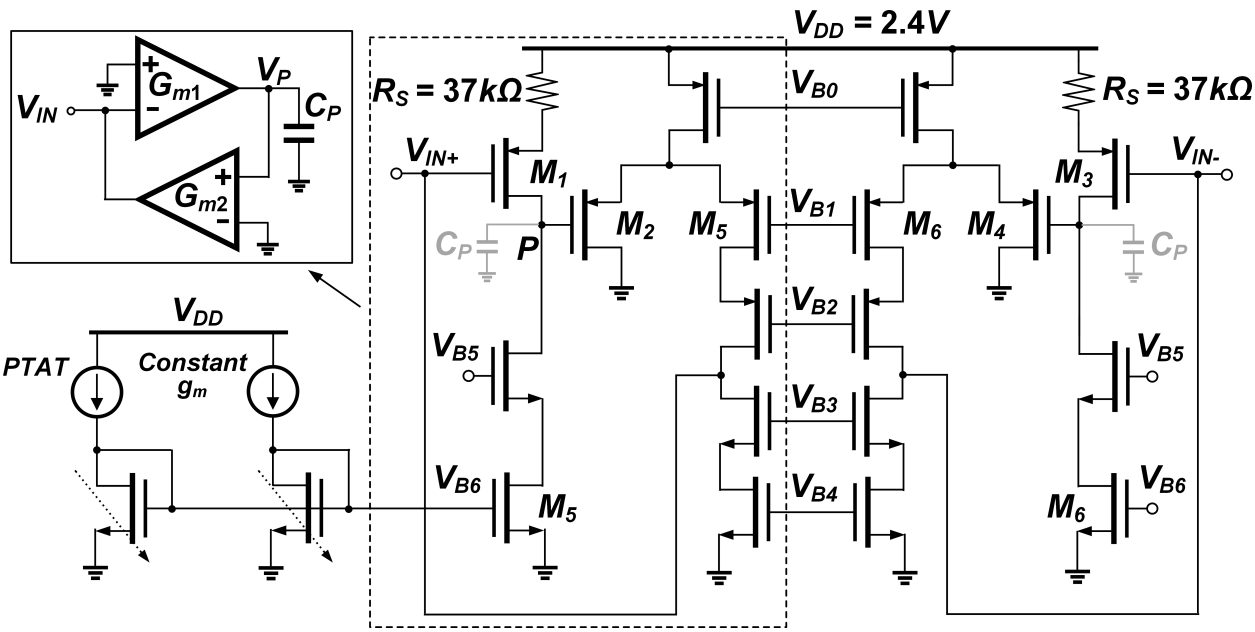


Figure 4.14: AI circuit schematic.

the AI. Source degeneration reduces the dependency of G_{m1} on the input level, reduces the voltage gain at the output (to keep the transistors in saturation), and improves linearity as well as sensitivity to supply variation. Fig. 4.13 shows the input impedance of AI at 48 MHz and corresponding Q-factor variations vs. V_{DD}. The reactance varies by ±9% from 2.3–2.5 V, roughly translating to the same variation in the effective inductance. Reduced G_{m1} has to be compensated for by increasing G_{m2}, which leads to higher power consumption (bias current of 1.5 mA for G_{m2} cell). Cascode current sources are used for biasing to increase Q-factor of the structure. PMOS transistors are used to provide higher input voltage range, since AI and XO are DC-coupled. Shown in Fig. 4.14, the AI schematic is comprised of two single-ended structures operating at 2.4-V supply to accommodate stacked transistors and maintain constant transconductance values (and effective inductance) over a large signal swing. A combination of PTAT and constant-g_m current sources with 1.5 μA and 1 μA tuning resolutions, respectively, are used to bias M_1 with a nominal bias current of 14 μA, tune the effective inductance value, and reduce its variation across PVT. The AI operates over a wide frequency range (i.e., up to its self-resonance frequency), virtually accommodating all MHz crystals. The AI is notorious for being noisy and thus is usually used in applications

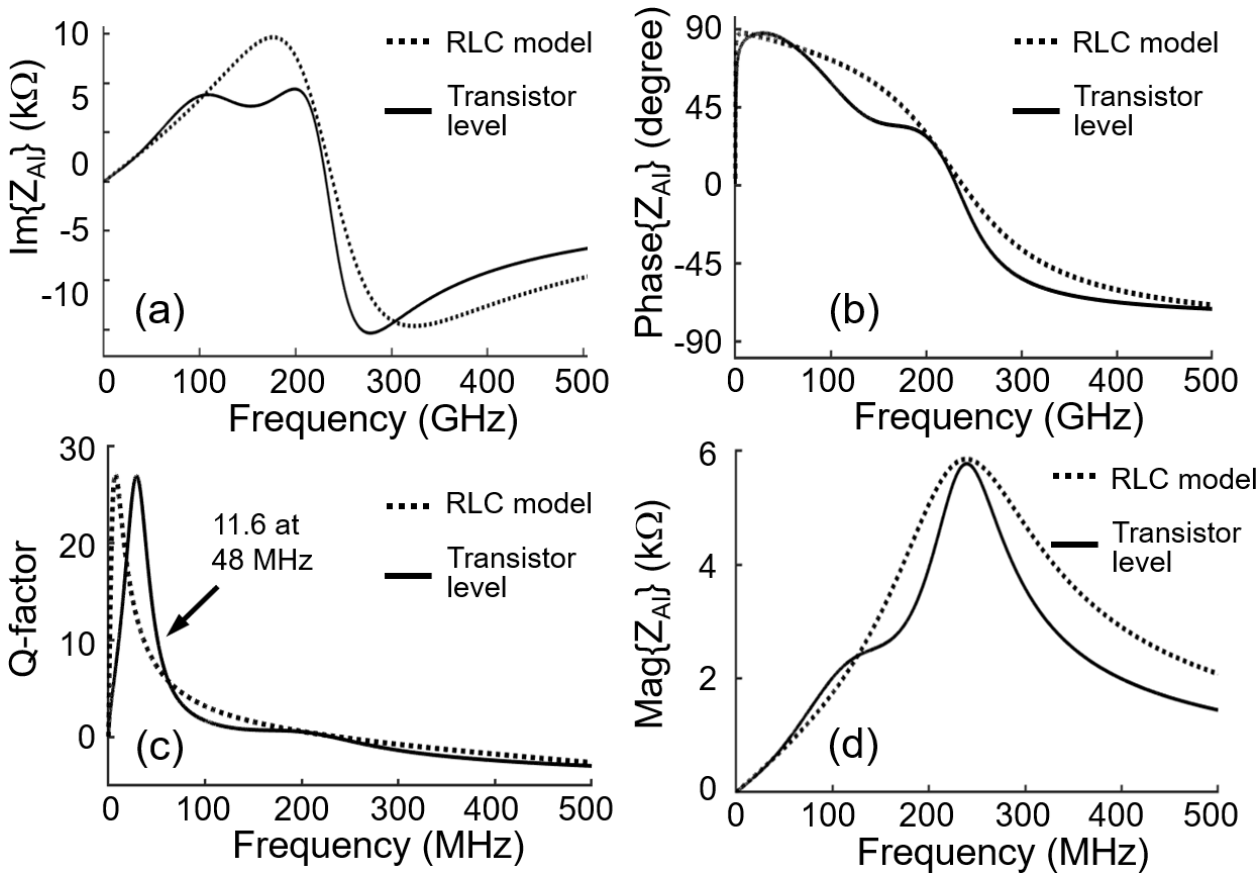


Figure 4.15: AI reactance vs. frequency and its equivalent circuit model.

with relaxed noise requirements. Nonetheless, for the intended purpose of the XO start-up improvement in this work, the AI's noise indeed helps in reducing T_S.

Fig. 4.12(b) shows the synthesized equivalent RLC model for the proposed AI. The equivalent RLC components are readily derived by equating the input impedances of this model and the AI circuit in Fig. 4.14, i.e.,

$$\begin{aligned} L \simeq \frac{C_P}{G_{m1}G_{m2}}, R_{P2} = R_{o2}, R_S = \frac{1}{G_{m1}G_{m2}R_{o1}}, C = C_{in} \\ R_{P1} = \frac{R_{o1}}{1+g_{m1}R_S}, G_{m1} = \frac{g_{m1}}{1+g_{m1}R_S}, G_{m2} = \frac{g_{m2}}{2} \end{aligned} \tag{4.26}$$

where C_P (R_{o1}) and C_{in} (R_{o2}) are capacitances (resistances) at the drain and gate of M_1, respectively. Fig. 4.15 shows and compares the frequency response and Q-factor of the AI and its RLC model. The AI has multiple poles which causes the two responses to deviate

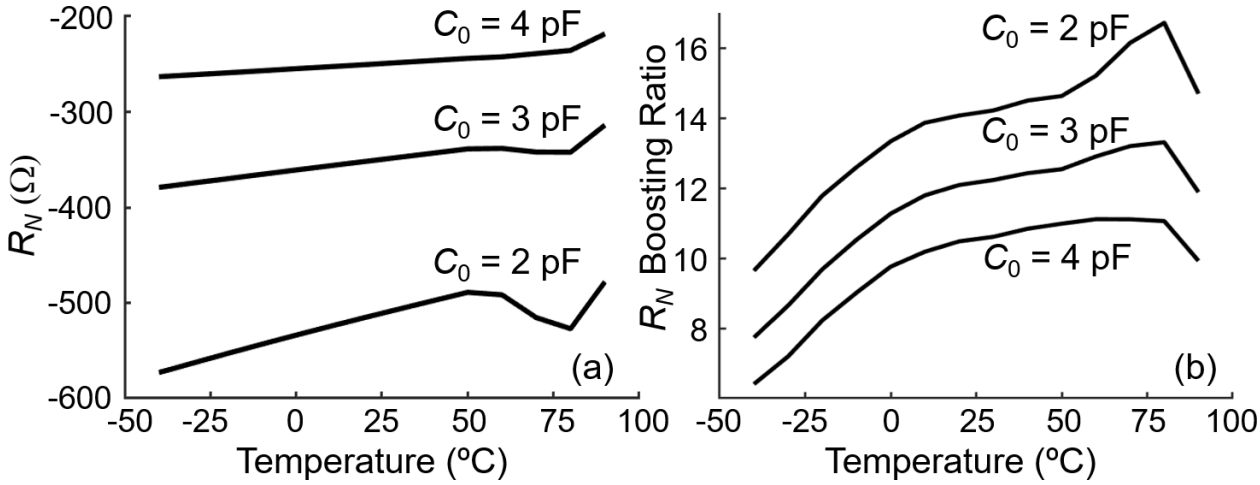


Figure 4.16: Simulated temperature variations of (a) R_N after addition of the AI and (b) R_N boosting ratio

at high frequencies. However, the model is sufficiently accurate up to ∼0.1 GHz. Fig. 4.16 illustrates the simulation results for the negative resistance and its associated boosting ratio across temperature after the addition of the AI. The R_N values in Fig. 4.16 are estimated from the rate of oscillation amplitude growth in large signal transient simulations. These values are smaller in magnitude than the ones predicted in Fig. 4.9 because of the AI nonlinearity, namely, variation of G_{m1} and G_{m2} with signal swing. For a given C_0, the AI maintains a relatively constant R_N (<±9% worst-case variation for C_0 = 2 pF) across -40-90°C temperature range, which thus keeps the T_S variations small.

To lower T_S for crystals with large C_0 values, the duration of the second phase ϕ_2 of the start-up sequence in Fig. 4.2 should increase. According to simulations of motional current amplitude in the nominal process corner and at room temperature, T_S increases from 17 μs to 22 μs for C_0 varying from 1- to 6-pF (for the same unloaded crystal Q-factor). The optimal value of ϕ_2 can be found using two methods: (1) measuring crystal's R_M and C_0 and using simulations to find the optimum duration, or (2) using an oscillation amplitude detection circuitry to disable ϕ_2 when near-steady-state amplitude is reached. Signal injection duration ϕ_1 is independent from C_0 since T_{OPT} only depends on $\Delta\omega$.

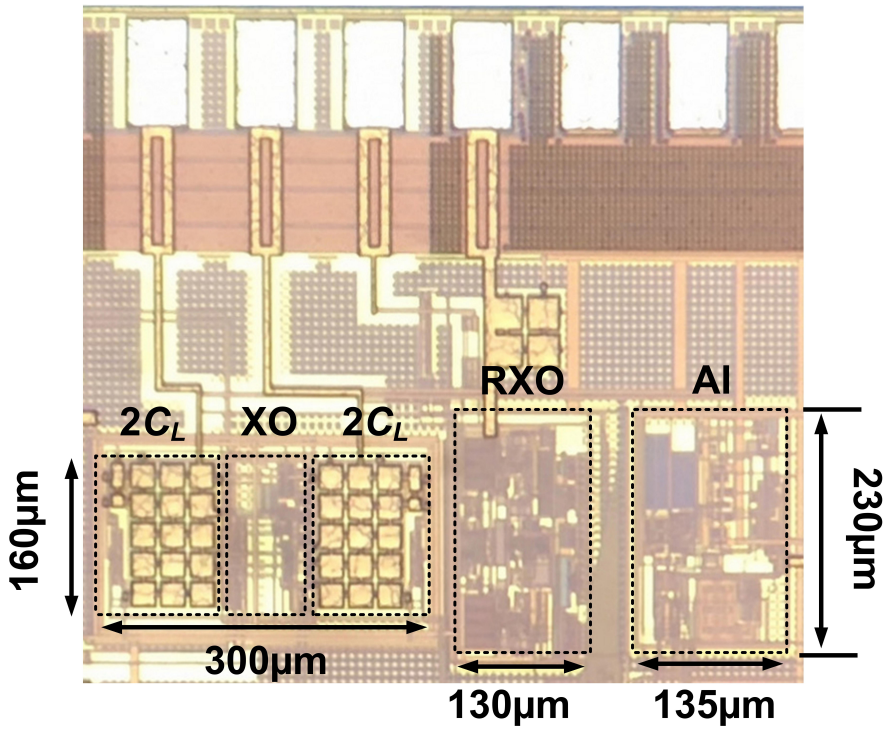


Figure 4.17: Die micrograph of the prototype.

4.5 Measurement Results

Fig. 4.17 shows the die micrograph of the chip fabricated in a 180 nm CMOS process. Occupying an active area of 0.108 mm^2, this chip integrated on-chip capacitors including a capacitor bank to create the equivalent 8-pF C_L. It was wirebonded into a QFN package and mounted on an FR-4 PCB. Operating at 48 MHz, the oscillator employs a surface-

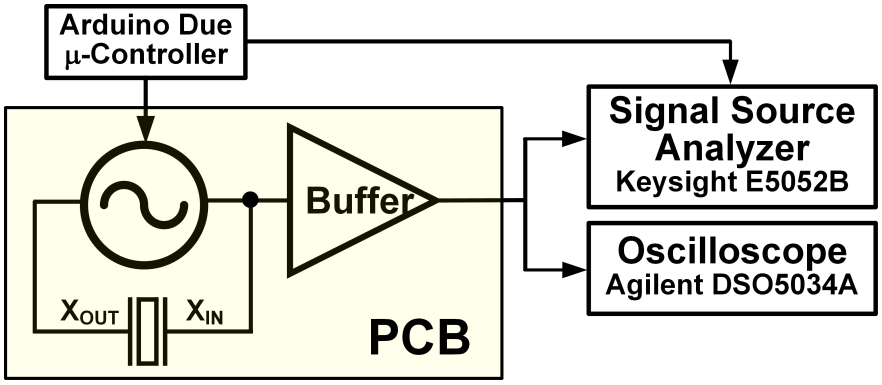


Figure 4.18: Measurement setup.

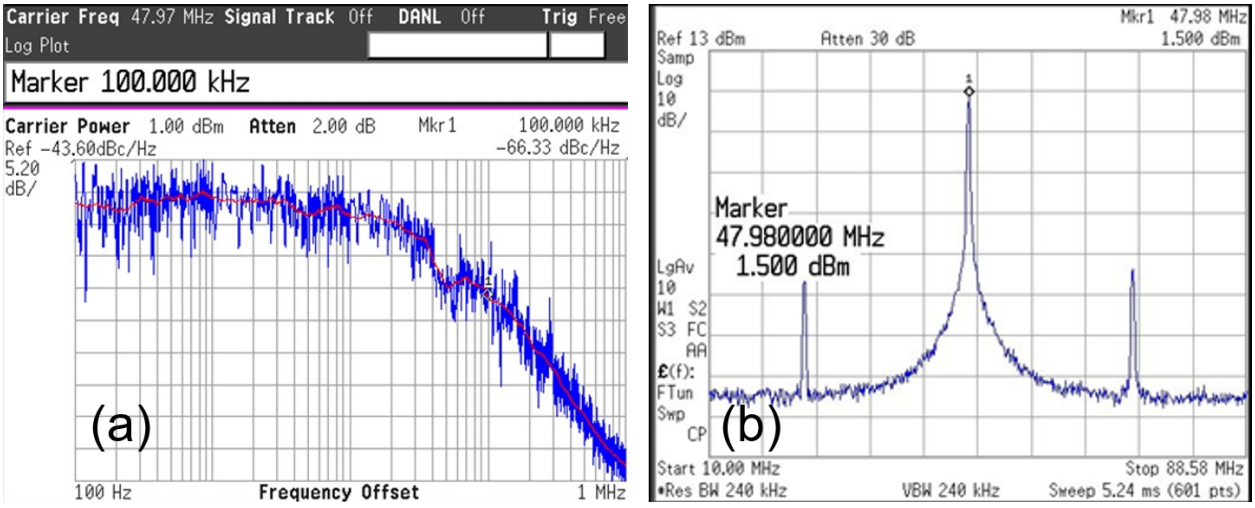


Figure 4.19: (a) Measured RXO phase noise and (b) power spectral density.

mount crystal with a 3.2×2.5 mm^2 package size, and dissipates 180 μW from 1-V supply (generated through a low dropout regulator) at steady-state. The supply of 1 V was chosen for ease of comparison with prior work. The steady-state power is mainly determined by the supply voltage, operation frequency, C_L, oscillation amplitude and crystal properties. It can be minimized through circuit techniques such as stacked-amplifier architecture in [113]; however, this was not the focus of this work.

Measurement setup is depicted in Fig. 4.18. An off-chip buffer was used to monitor signal on X_{IN} and a micro-controller generates the start-up sequence. The RXO phase noise and power spectral density are shown in Fig. 4.19. The RXO phase noise was purposely increased to -66 dBc/Hz at 100 kHz offset through dithering. The two spurs in the RXO's power spectrum are due to the fact that the RXO output is sum of two half-wave rectified signals. The measured RXO frequency settles within 0.8 μs, as shown Fig. 4.20, which is dominated by the RXOs integrator pole $R_I C_I$ in Fig. 4.6. Although this start-up time is larger than that of a ring oscillator, it is still negligible compared to the XO's T_S. Therefore, the accurate and stable frequency provided by the RXO justifies its usage. Fig. 4.21 shows the measured voltage at X_{IN}, demonstrating the oscillation start-up behavior using the AI only. The XO supply is increased to 1.5 V with a steady-state oscillation voltage of 0.95 V and $T_S = 3.96$

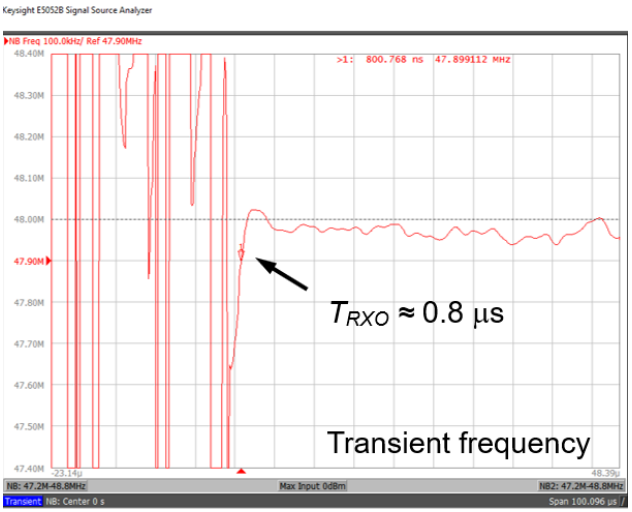


Figure 4.20: RXO start-up time.

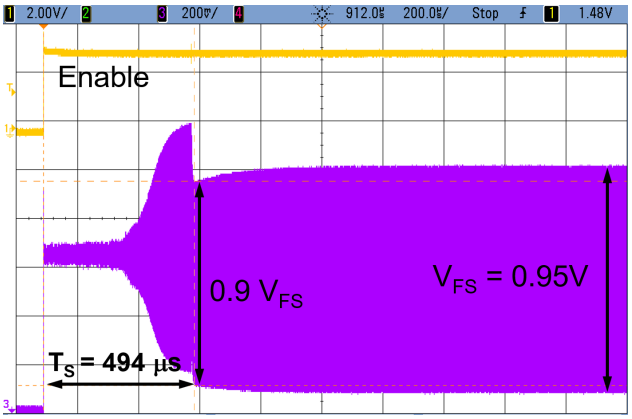


Figure 4.21: T_S improvement using AI only for a large steady-state oscillation amplitude of 0.95 V.

ms without the AI. Even at this large voltage swing, the AI is able to reduce T_S to 0.494 ms, an 8× improvement ratio. Figs. 4.22(a)-(f) show the strobed voltage X_{IN} to evaluate T_S and E_S using different techniques. Absent of any start-up assistant technique, T_S and E_S of the XO was measured to be 1.85 ms and 333 nJ, respectively. The RXO frequency was calibrated using the trimming poly and diffusion resistors (*cf.* Fig. 4.6) and the injection time is fixed at 7 μs. Using the precise and dithered injection (PDI) technique, T_S and E_S were improved by 11.1× and 6.2× to 166 μs and 54 nJ. Enabling the PDI and the AI without increasing the amplifier's g_m (i.e., using the same g_m as in the steady-state), T_S was reduced to 38 μs, inferring ≈5× boosting of R_N. Applying PDI and rising the amplifier's

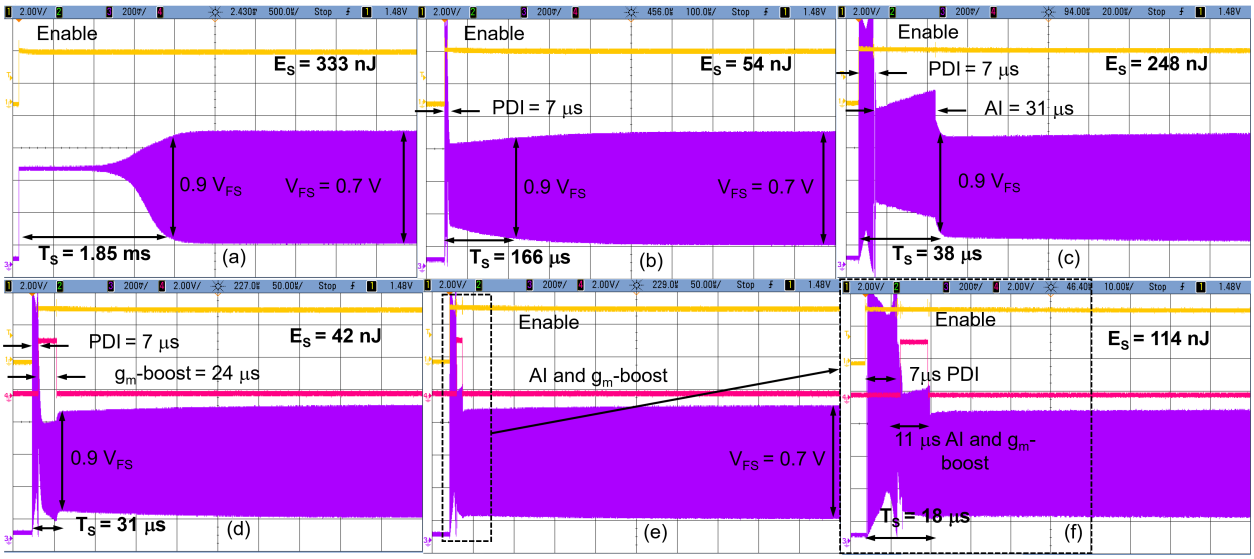


Figure 4.22: Start-up behavior of XO with (a) no kick-start technique, (b) PDI only, (c) PDI and AI techniques (d) PDI and g_m-boost, (e,f) all techniques combined.

g_m (g_m-boost) by switching in g_{m2} (*cf.* Fig. 4.2(a)), T_S was reduced to 31 μs with a slight decrease in E_S compared to using PDI only. Combining all techniques, T_S and E_S were further reduced by 102.7× to 18 μs and 2.9× to 114.5 nJ, respectively, compared to the case where no techniques were utilized. The start-up time has been significantly improved compared with prior work that boost negative resistance (e.g., [116] and [121]), albeit with higher E_S. In systems where latency is of concern or power dissipation during their active period is large, minimizing start-up time is considered to be the main objective function. The increased E_S is due to high power consumption associated with the AI and g_m-boosting techniques. Measured power consumption (estimated E_S) for AI, RXO (including buffers) and amplifiers g_{m1} and g_{m2} (Fig. 4.2(a)) are 7.2 mW (79 nJ), 3.6 mW (27 nJ), and 0.5 mW (8 nJ). According to transient simulations of the XO start-up behavior, hypothetically if AI is removed and the R_N-boost amplifier g_{m2} is scaled in size and power by an additional factor of 12 and 3, $T_S \simeq 22$ μs and $E_S \simeq 124$ nJ. The measured T_S varies by 2% for a 25% variation in the injection time and by ±12% over -40–90°C temperature range. Transient frequency of XO during start-up settles within ±20 ppm of its steady-state in <18 μs, as depicted in Fig. 4.23. Fig. 4.24 shows the measured phase noise profile of the XO, where

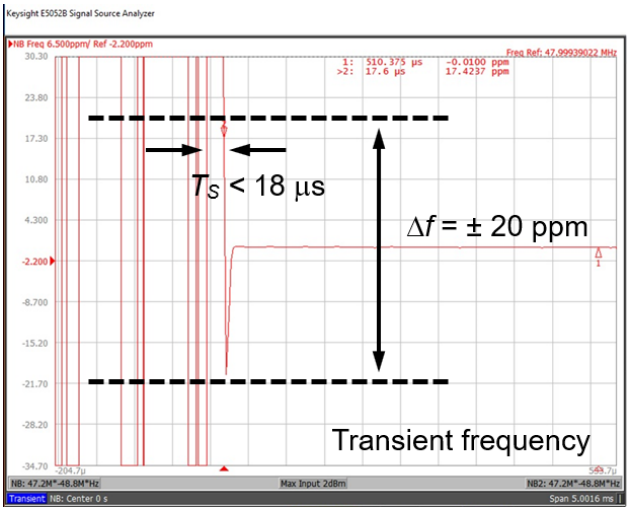


Figure 4.23: Settling of XO oscillation frequency.

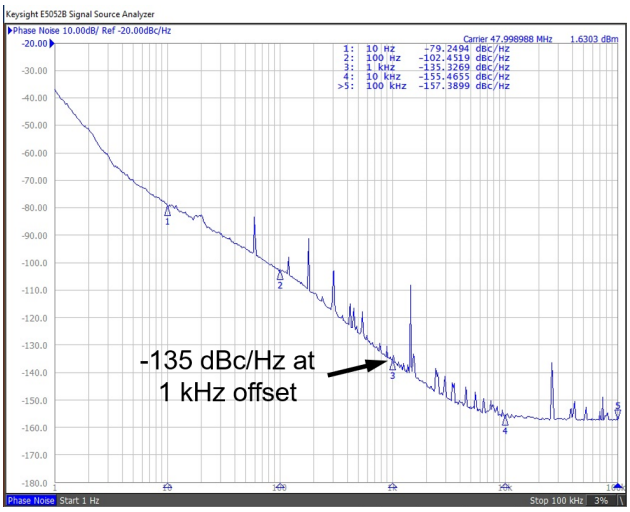


Figure 4.24: Measured phase noise.

a –135 dB/Hz phase noise at 1 kHz offset is reported. Spurious tones seen on the profile are due to weak supply bypass capacitors on board. Table 4.1 summarizes performance of the XO using the proposed techniques in comparison with prior work. To better assess the effectiveness of various start-up techniques, both C_L and the steady-state amplitude which is proportional to square root of crystal energy should be taken into consideration (see Eq. 4.8) and are thus included in Table 4.1. This work achieves the largest T_S improvement ratio to date, while maintaining an E_S improvement ratio comparable with prior art.

Table 4.1: Measurement summary and Comparison with prior art

	[125]	[124]	[116]	[121]	[128]	[126]	[127]	[24]
CMOS process (nm)	180	65	90	65	65	65	55	180
Core area (mm^2)	0.12	0.08	0.072	0.023	0.09	0.069	0.049	0.108
Supply (V)	1.5	1.68	1	0.35	1	1	1.2	1
Frequency (MHz)	39.25	24	24	24	50	54	32	48
Load capacitor C_L (pF)	6	6	10	6	9	6	6	8
Steady-state amplitude (V)	1.5	N/A	N/A	0.3	0.2[2]	0.7	0.37	0.7
Phase noise (dBc/Hz) at 1 kHz	-147	N/A	N/A	-134	N/A	-139.5	N/A	-135
Steady-state power (μW)[1]	181	393	95	31.8	195	198	190	180
Start-up time T_S (μs)	158	64	200	400	2.2[2]	19	23	18
T_S improvement ratio	13.3×	6.7×	13.3×	3.3×	N/A	31.5×	17.4×	102.7×
Start-up energy E_S (nJ)	349	N/A	36	14.2	13.3[2]	34.9	20.2	114.5
E_S improvement ratio	1.1×	N/A	6.9×	2.8×	N/A	N/A	N/A	2.9×
ΔT_S over Temp. (%)	7	±35	27.5	7.5	7	±1.25	±10	±12
Temp. range (°C)	-30 to 125	-40 to 90	-40 to 90	-40 to 90	-40 to 90	-40 to 85	-40 to 140	-40 to 90
Start-up technique	Chirp injection g_m boost	Dithered injection	Dynamic load, g_m boost	3-stage g_m, Chirp injection	Precisely-timed injection	2-step injection	Synchronized signal injection	PDI, AI

ECS-33B SMD crystal is used.

[1]Heavily depends on frequency, supply, C_L, crystal properties and steady-state amplitude.

[2]Steady-state amplitude is limited to ∼0.2V by a regulation loop, requiring only an external injection for a very short time.

4.6 Conclusion

This paper presented a study and design of two techniques used to reduce start-up time (T_S) and energy (E_S) of Pierce crystal oscillator (XO). An analytical study of the external signal injection was presented and an RXO was proposed as an alternative external injection source to minimize T_S. An overview of limitation imposed by crystal's static capacitor on XO start-up time was presented and an active inductor was designed to mitigate its effects. Simulation and measurement results of a prototype in 180 nm CMOS process verified the efficacy of the proposed techniques. A significant increase in T_S improvement ratio was achieved across a wide temperature range.

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