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ABSTRACT

The requirements for multiple-coincidence counting systems with 10^{-8} - to 10^{-9}-sec time resolution can be met economically with presently available high-frequency transistors. The design of solid-state coincidence circuits, amplitude discriminators, and decade scalers is considered and their operation discussed. Several systems have been designed utilizing up to 180 channels from scintillation detectors.

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INTRODUCTION

Solid-state circuit components have properties that are ideal for nuclear counting applications. Among these are low impedance, low operating potentials, and small size. The resolution time, temperature dependence, or cost have often limited the usefulness of these devices in nanosecond (nsec) counting applications however. It was not until quite recently that transistors with gain-per-rise-time factors greater than 0.2 per nsec were available at a cost that economically justified widespread use in counting applications. (The gain/rise-time factor is related to the gain-bandwidth product as follows: Gain/rise-time = gain-bandwidth/0.35).

The counting groups at the Lawrence Radiation Laboratory in Berkeley a year and a half ago began the development of components for general-purpose scintillation-counter coincidence systems.

We began with the design criterion that a solid-state counting system should have a resolution time at least comparable to its existing electron tube counterpart. It was felt that the increase in reliability and the savings in space and power dissipation would more than offset the additional cost of semiconductor components. A basic coincidence system would consist of a multichannel coincidence-anticoincidence unit with sufficient signal power to drive an amplitude discriminator. The discriminator in turn would operate a scaling unit with a choice of several scale factors from 10 to 10^4. The output of the scaler would be stored in a mechanical register. System input signals would still be derived directly from the anode or last dynode of multiplier phototubes. Also because of the greater sensitivities of transistors, it was expected that one could operate solid-state coincidence circuits with an order-of-magnitude less gain in the phototube. Some cost savings should be realized in this way. The desired time resolution was still of the order of 1 nsec, and the maximum continuous counting rate, 10^7 pulses per second.

Design has centered around several MADT (micro-alloy diffused base) and Mesa germanium transistors. In the interests of fast switching, saturation operation has been avoided by limiting base drive to the transistors.

To date a coincidence unit, a pulse-amplitude discriminator, and decade scaling units have been developed and are in use. Work is still under way on scaler of 10^{-8} sec resolution, pulse amplifiers, and gate generators. At the same time a number of special-purpose multichannel coincidence systems have been developed; these also employ transistors as active elements almost exclusively.

Coincidence Circuit

Widespread use has been made at our Laboratory of the nanosecond-resolution coincidence circuit originally developed by Wenzel.[1]

Our unit capable of three-channel coincidence with one-channel anti-coincidence is an adaptation of this circuit; solid-state components are employed throughout. The block diagram is shown in Fig. 1 and the schematic circuit diagram in Fig. 2. Negative input signals, fed directly from multiplier phototubes, are inverted[2] to positive pulses and fed to common-emitter amplitude limiters (Q-1, Q-2, and Q-3). Monitor jacks allow the input signals to be observed on an oscilloscope or fed to additional circuits. When not used in this fashion, the jacks should be terminated in the characteristic impedance of the input system.

Both type 2N501 and type 2N1143 transistors have been employed as amplitude limiters. The 2N1143 gave approximately 25% improvement in collector-rise-time response to a step-function input. A standing collector current of about 15 ma is cut off with input signals over 0.25 volt. The limiter stage presents an input impedance of 125 ohms with less than a 5% voltage reflection coefficient for signals of 4 nsec rise time. This relation holds for input amplitudes up to 5 volts. Thus good limiting action and impedance matching are obtained over a 20-to-1 signal ratio. The coincidence circuit is a Rossi circuit using Qutronics Q6-100 gold-bonded diodes (CR7, CR8, and CR9). Other diodes have lower forward impedances and others faster recovery times; these units appear to provide the best compromise between forward dynamic impedance and reverse recovery time. Shorted clipping lines in each coincidence channel provide signals of uniform duration to the diode coincidence circuit. Clipping lines are provided with connectors on each end. Bias current is fed through the clipping line to each diode of the coincidence circuit. To turn a channel off, the diode is reverse biased, and the collector potential of the limiter is removed.

One channel of anticoincidence is provided; an emitter follower (Q-4) is cut off in the presence of an anticoincidence signal. This renders a diode (CR-6) conducting and prevents a signal from appearing at the output.

Many circuits were explored to determine the best method of discrimination. A reverse-biased diode followed by an emitter-follower stage gave the best coincidence ratio[3] (doubles-to-singles ratio) of 50/1. However, the output signal amplitude was only about 70 mv. The best compromise to get sufficient output was simply a reverse-biased emitter-follower stage (Q-5). On coincidence the base signal over comes the reverse emitter bias. An examination of Fig. 3a and b indicates a coincidence ratio of about 20/1. The output level with 4-nsec slipping lines was 0.2 volt. By sacrificing coincidence ratio, it is possible to increase this value--e. g., going to 4/1 gives about 0.4 v.

The definition of coincidence time for a coincidence circuit of this type expresses a convenient measure of the time resolution of the unit itself without requiring an analysis of an entire coincidence system. The coincidence time[3] of this circuit was measured by feeding a 0.25-volt 200-nsec-wide signal to each input. The length of the clipping lines was then shortened until the output amplitude dropped to 50% of the output level for long clipping lines.

The double transit time of the clipping lines for this condition varied between 3.3 and 4.3 nsec in different units. Figure 4a shows a plot of this relation. Then, with 4-nsec-long clipping lines, one input signal was delayed until the output amplitude dropped an additional 50%. This delay time is defined as the coincidence time; it varied between chassis from 2.7 to 4.1 nsec for a threefold coincidence. Figure 4b illustrates the delay characteristic of one unit which had a coincidence time of 3.4 nsec.

The 2N1143 transistor amplitude limiters are not quite as fast as electron tube limiters (e. g., E180F), but because of the time spread in present photomultipliers, it is possible with careful adjustment to obtain very nearly the same over-all time resolution (i. e., a drop in counting rate of a factor of 100 for a delay of 1 nsec) with the transistor unit.

A test was made to determine the resolution time of the unit operating in a twofold coincidence system. Two 6810A multiplier phototubes were illuminated by a pulsed mercury light source[4] with a light level of 1850 photons impinging on each photocathode. The pulse repetition frequency was 60 pps. Phototube signals were fed directly to the coincidence circuit. The output signal was amplified by a Hewlett-Packard 460A distributed amplifier followed by a 460B amplifier. This signal was amplitude-discriminated and the resultant output counted in a scaler. Figure 5 portrays a typical time resolution curve of one unit.

Two coincidence circuits are constructed on a standard 5-1/4-in. relay rack panel with a common Zener diode-regulated power supply.

Pulse Amplitude Discriminator

Circuits providing amplitude discrimination with respect to an adjustable threshold level fulfill a number of needs in nuclear counting applications. An important use is to provide more precise amplitude discrimination in a coincidence system thus improving the time resolution without severely sacrificing counting rate.

Our design specifications called for a discriminator with an input threshold adjustable over a range from a few tenths of a volt to a few volts, acceptance of an input signal of less than 10-nsec duration, an output signal suitable for driving our existing tube or transistor scalers, a maximum continuous counting rate of 10^7 pps, and a variation in threshold level with temperature of the order of 1 mv/°C. The threshold also should not drift more than 1 mv/day at constant temperature.

A number of circuits were explored; the resulting one is shown in block diagram in Fig. 6 and the schematic circuit diagram in Fig. 7. When dealing with pulses in the nanosecond region, it is imperative that the input circuit present a constant load impedance over the expected input amplitude of the unit. A common-base stage (Q-1) provides a better match than the common-emitter configuration.

Sensing of a threshold could be accomplished by either turning on or turning off bias current in a semiconductor junction. Leakage currents and signal feed through would be a problem if the diode were cut off in the quiescent condition, so the normally conducting condition was employed instead.

A monostable multivibrator was selected as the pulse-forming circuit. Two type 2N1143 transistors (Q6-Q7) in a emitter-coupled timing circuit were used. Transistor Q6 is normally conducting. The pulse rise time is 10 nsec and the amplitude 6v. An input signal of 0.5 v was required to effectively trigger the multivibrator. Since the desired minimum input threshold signal was 0.1 v, a two-stage common-emitter amplifier (Q4-Q5) was interposed between the threshold diode (CR-1) and the multivibrator.

To achieve a low-output impedance for these pulse widths, the circuit employed was a solid-state counterpart of the familiar White cathode follower. The output impedance is about 60 ohms. Figures 8a and 8b show a 4-v output signal operating into a 125-ohm load at 10^6 and 10^7 pps respectively. The signal has a 12-nsec rise time and a 40-nsec pulse width at half amplitude.

Fast counting circuits can be made to operate stably from 25° to 55°C ambient temperature. By balancing base-to-emitter voltage drops it was possible to reduce the threshold drift with temperature to 1.2 mv/°C when the unit was operated with a 15-volt Zener diode regulated supply. By employing three 5-v Zener diodes with lower coefficients for change of voltage with temperature, it was possible to reduce the threshold coefficient to 0.2 mv/°C.

The final range of adjustment of input threshold signals was from 0.1 to 2.1 volts. Figure 9 indicates the excess signal required for pulses shorter than 50 nsec. It is noted that a 5-nsec pulse requires only an additional 100 mv over the maximum threshold sensitivity of 100 mv for long pulses. At the minimum sensitivity level an additional 450 mv is required for 5-nsec-wide pulses. These tests were performed with a mercury relay pulser operating at 60 pps. Since the incoming pulse length is usually determined by clipping-line techniques, this variation in sensitivity with pulse width is not a serious deficiency.

It is important that a discriminator threshold also remain constant over a wide range of counting rates. Figure 10 shows the variation in pulse amplitude required to trigger the discriminator at various pulse repetition rates when the threshold was adjusted to minimum sensitivity. The input requirements varied only 25 mv between 10^6 and 10^7 pps. A 10-Mc pulser developed in this laboratory[5] was employed in this measurement.

Figure 11 illustrates the variation in delay time of the output signal as a function of the signal amplitude. The threshold in this case was adjusted to 0.1 v. This test was made with a mercury switch pulser generating a 120-nsec-wide pulse.

Decade Scaler

Adequate scaling means is of paramount importance in nuclear experiments. Our requirements called for a flexible arrangement of decade scalers allowing scale factors between 10 and 10^4 with the overflow accumulated in a mechanical register. It was also required that the units be capable of electronic gating, remote readout, and remote as well as ganged reset.

The arrangement finally adopted allows a selection of printed-circuit modules. These plug into a frame which also houses the power supply as shown in Fig. 12. So far a 5-Mc scaler, a 1-Mc scaler,and a 1-Mc scaler-register unit have been produced and are in laboratory operation. One frame can be arranged to provide any combination of scale factors available from four decade units. In each combination a mechanical register is associated with that decade counting the most significant figure. The block diagram of the basic scaler-register unit is shown in Fig. 13. The table shows some of the operating specifications for the 1-Mc and the 5-Mc units. The maximum pulse width listed as 1 μsec is significant only in that pulses of 30 v amplitude and wider than 1 μsec cannot be gated off by the input gate circuit. Greater amplitudes or wider pulses can be counted if the gating feature is not necessary. The schematic circuit diagram for the 5-Mc counter is shown in Fig. 14. A continuous counting rate of 10^6 pps was achieved by using type 2N247 transistors in the flip-flop circuits. When these were replaced with type GT 643 transistors, whose maximum factor of gain per rise time is 57/μsec, and the coupling-time constants adjusted appropriately, the counting rate increased to 5×10^6 pps.

The gate circuit allows one to reduce accidental counts by scaling only during a specified period. We use a Rossi gate comprised of diodes 1, 2, and 13.

The four binary counter stages are Eccles-Jordan flip-flops (Q 1-2, 3-4, 5-6, 7-8) with diode steering gates. The transistors are kept out of the saturation region by maintaining suitable small base drive currents.

The scale-of-sixteen counter is modified to decade operation by two feedback loops. On the fourth pulse the second flip-flop is reset by a delayed pulse from flip-flop 3; On the sixth pulse the third flip-flop is reset by a delayed signal from flip-flop 4.

Visual readout is achieved by means of a meter which reads the sum of four currents, one from each flip-flop. The meter deflection is proportional to the residual count in the decade.

An emitter-follower output stage (Q-9) supplies a positive pulse to trigger subsequent units. For modules which include a mechanical register, transistor Q-9 also triggers the register blocking oscillator.

A mechanical register has been modified by adding an additional winding with 10% of the turns of the original "count" winding. These two windings together with a 2N102 power transistor form a blocking oscillator which actuates the register. The maximum continuous counting rate of a Sodeco type TCeF4 Frz register with a 24-v coil modified in this manner is 15 pps. Some difficulty was experienced in turning off transistors with high common-emitter current gains (β); consequently we rejected transistors with current gains greater than 120. It has been found that scaler units perform satisfactorily up to ambient temperatures of 65°C.

Special-Purpose Counting Equipment

The aim of the counting groups is to enable the experimenter with multichannel scintillation counter systems to process the experimental data electronically and present them in a form suitable for input to a computer. One system developed in this direction at the Laboratory employs 180 channels of scintillation-counter information. Signals from 84 type-7046 multiplier phototubes are each fed to two solid-state coincidence circuits. The remaining 12 channels are used for timing information. The presence of a coincidence in any channel during a nuclear event is registered in a coincident-current core-storage matrix. The 1800-core storage allows as many as 10 nuclear events to be recorded during one accelerated beam burst from the Bevatron. The core store is read out during the 5-sec interval between acceleration cycles and recorded on punched paper type. A later conversion to magnetic tape allows immediate analysis in a computer. A paper describing this system is in preparation.

Acknowledgments

We would like to express out appreciation to Prof. Donald O. Pederson for his many helpful discussions and to Dr. Yahia A. El Hakim for making the evaluation tests of the coincidence circuit.

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1. William A. Wenzel, Millimicrosecond Coincidence Circuit for High-Speed Counting, Lawrence Radiation Laboratory Report UCRL-8000, Oct. 1957 (unpublished).

2. C. Norman Winningstad, Nanosecond Pulse Transformers, IRE Trans on Nuclear Sci. NS-6, No. 11, 26-31 (March 1959).

3. Definitions used here are those described in the UCRL Counting Handbook, UCRL-3307 (Rev.)., Section CC-5.

4. Kerns, Kirsten, and Cox, A Generator of Fast-Rising Light Pulses for Phototube Testing, Rev. Sci. Intr. 30, 31-36 (1959).

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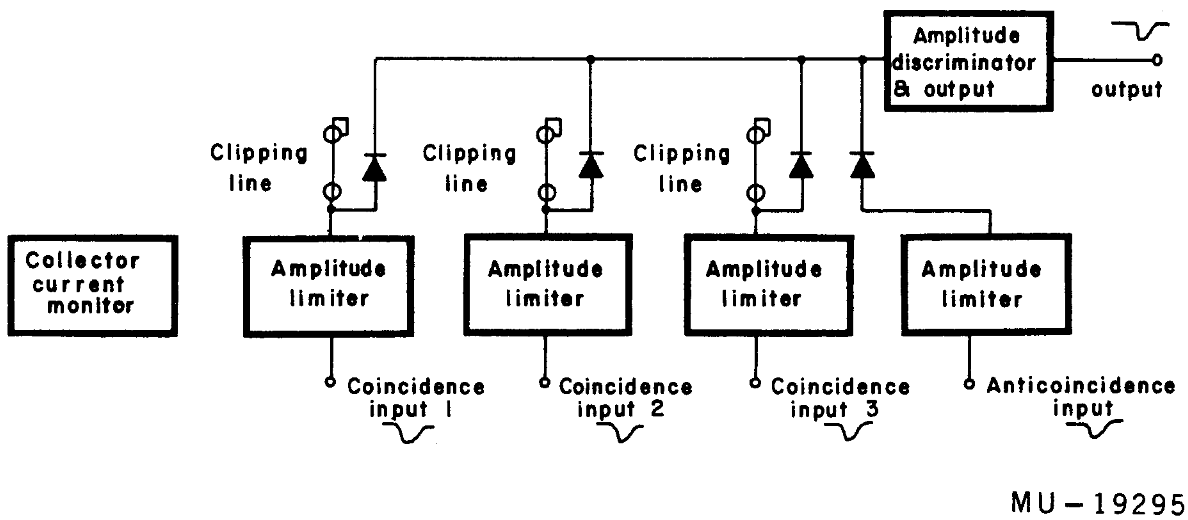

Fig. 1. Coincidence circuit.
Specifications: input siganl, -0.25 to -5v; output signal, -0.3v; maximum repetition frequency, 10^7 pps.

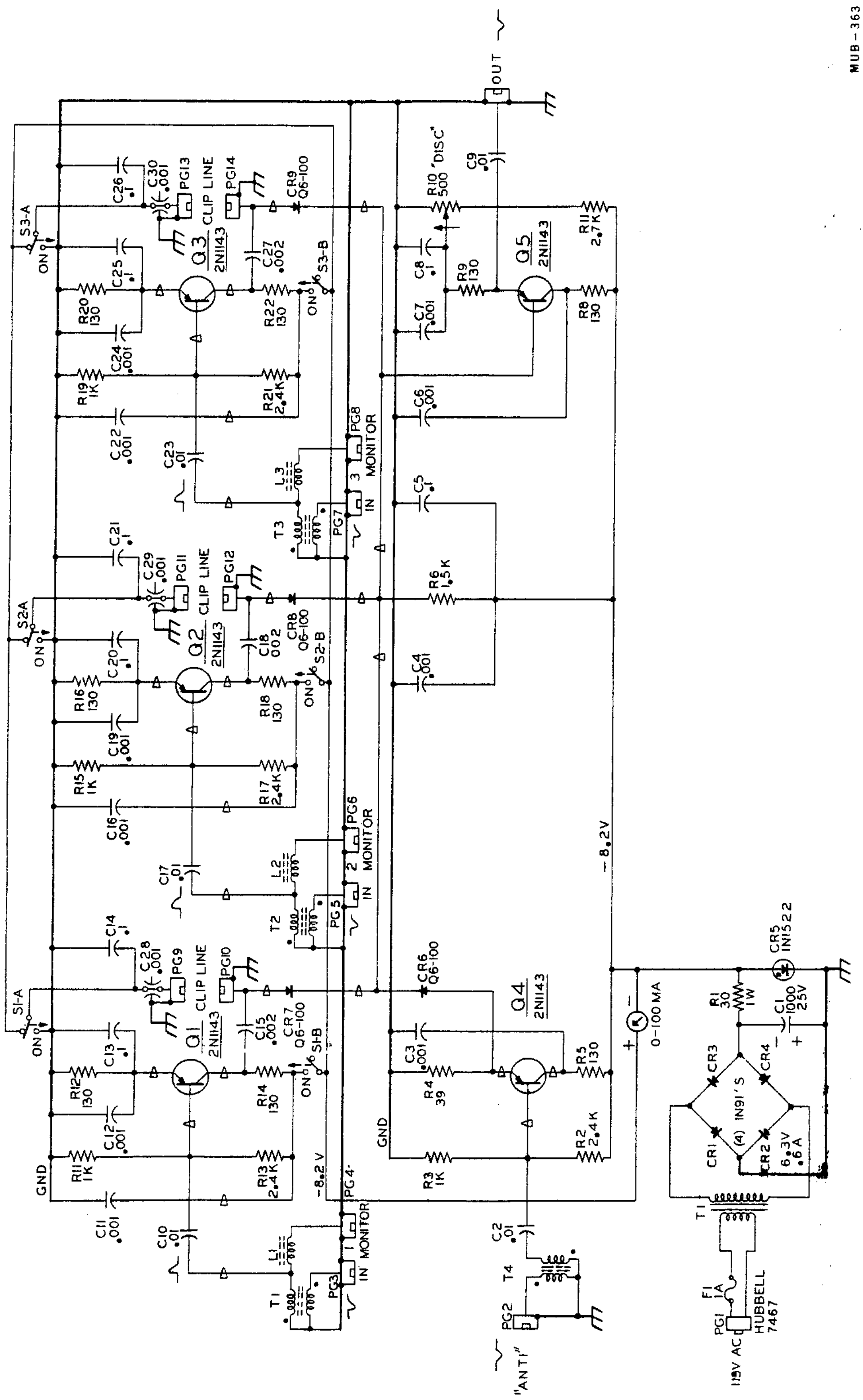

Fig. 2. Three-channel coincidence and anticoincidence transistor unit.

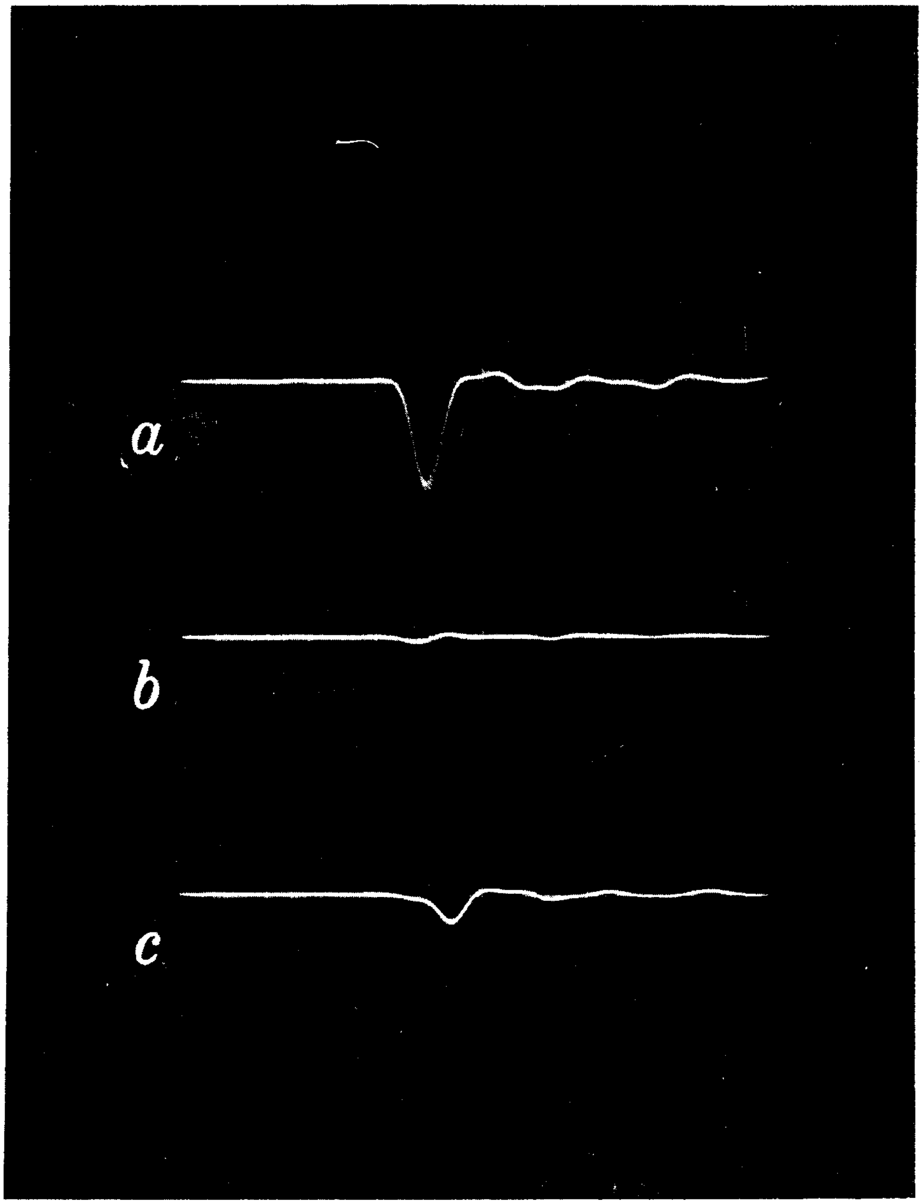

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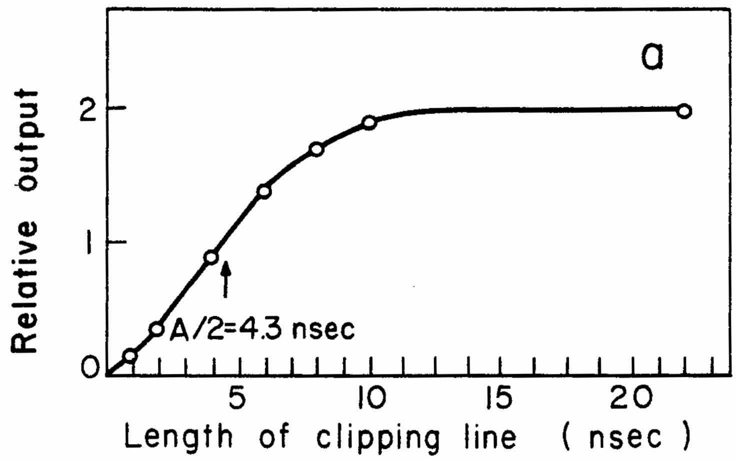
Fig. 3. Coincidence circuit: output signals for (a) twofold coincidence, (b) one input signal, (c) delay of 5 nsec in one channel.

Horizontal sweep, 10 nsec/cm; vertical, 0.1 v/cm; input pulse, 10 nsec; clipping line, 4 nsec; repetition frequency, 10^5 pps.



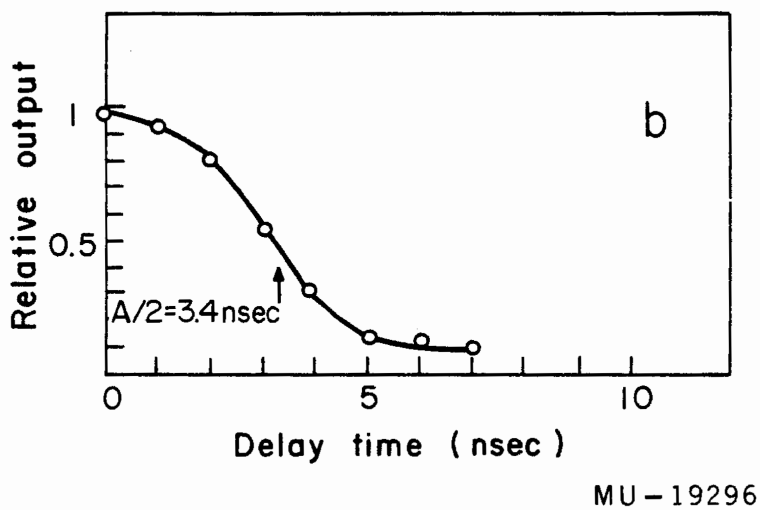


Fig. 4. Coincidence circuit: determination of coincidence time. Output amplitude as function of (a) clipping time: E_{in} = 0.25v at 200 nsec, threefold coincidence; (b) delay time; E_{in} = 0.25v at 200 nsec, clipping line = 4 nsec, threefold coincidence.

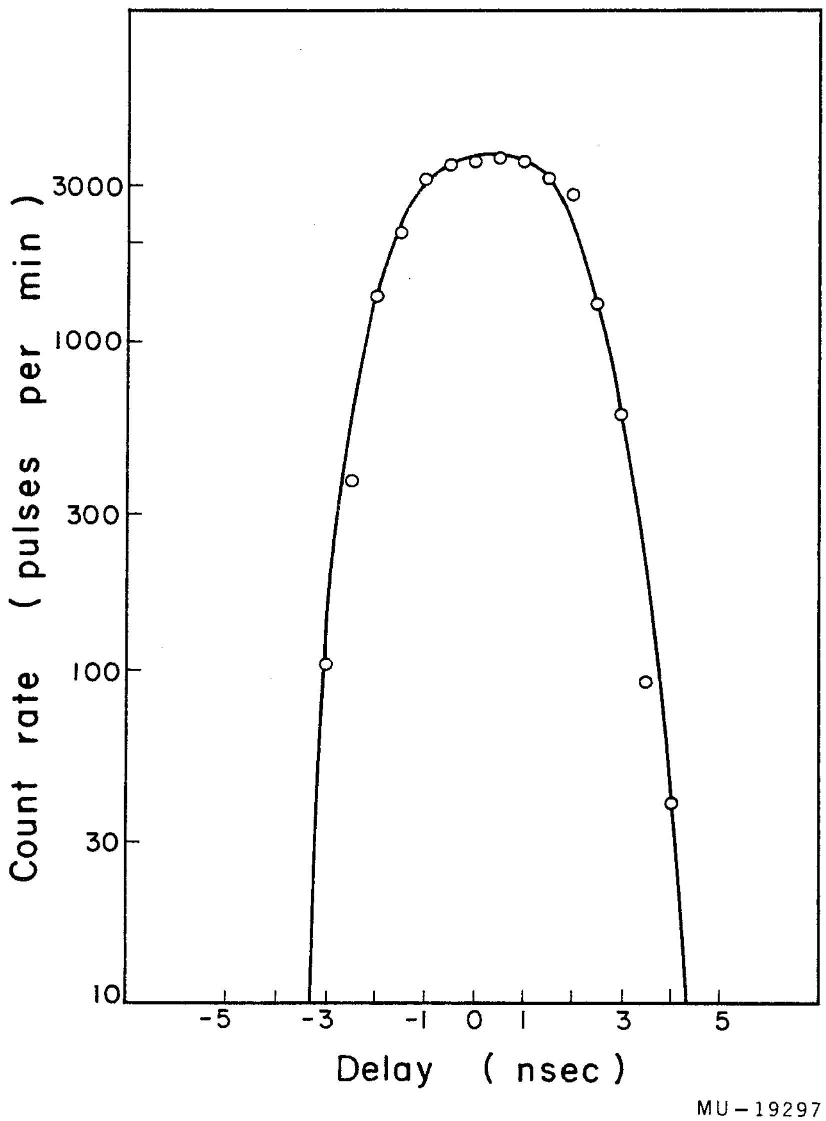


Fig. 5. Resolution time of coincidence circuit.
Pulsed mercury light source; light level, 1850 photons at photocathodes of two 6810A photomultipliers; coincidence circuit followed by a HP-460A and a 460 amplifier, pulse discriminator, and 1-Mc scaler.

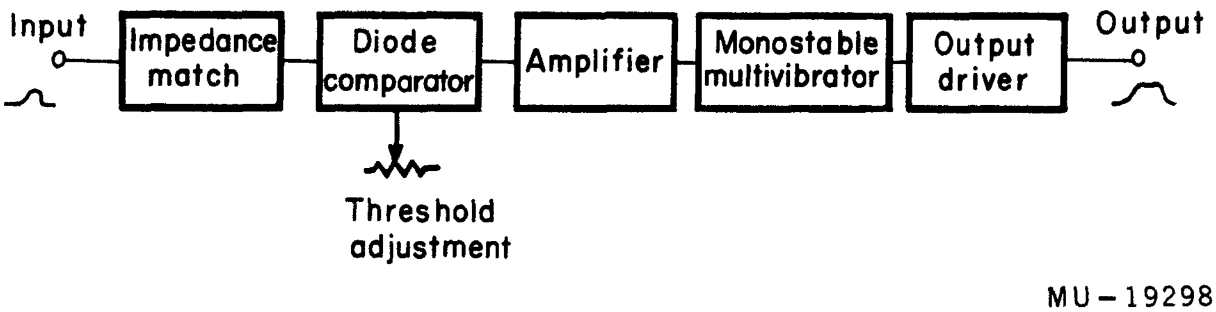


Fig. 6. Pulse-amplitude discriminator.
Specifications: input threshold, +0.1 to +2.1 v; maximum repetition frequency, 10^7 pps; temperature coefficient of threshold, 1.2 mv/°C; output signal, +4 v at 40 nsec wide into 125-ohm load.

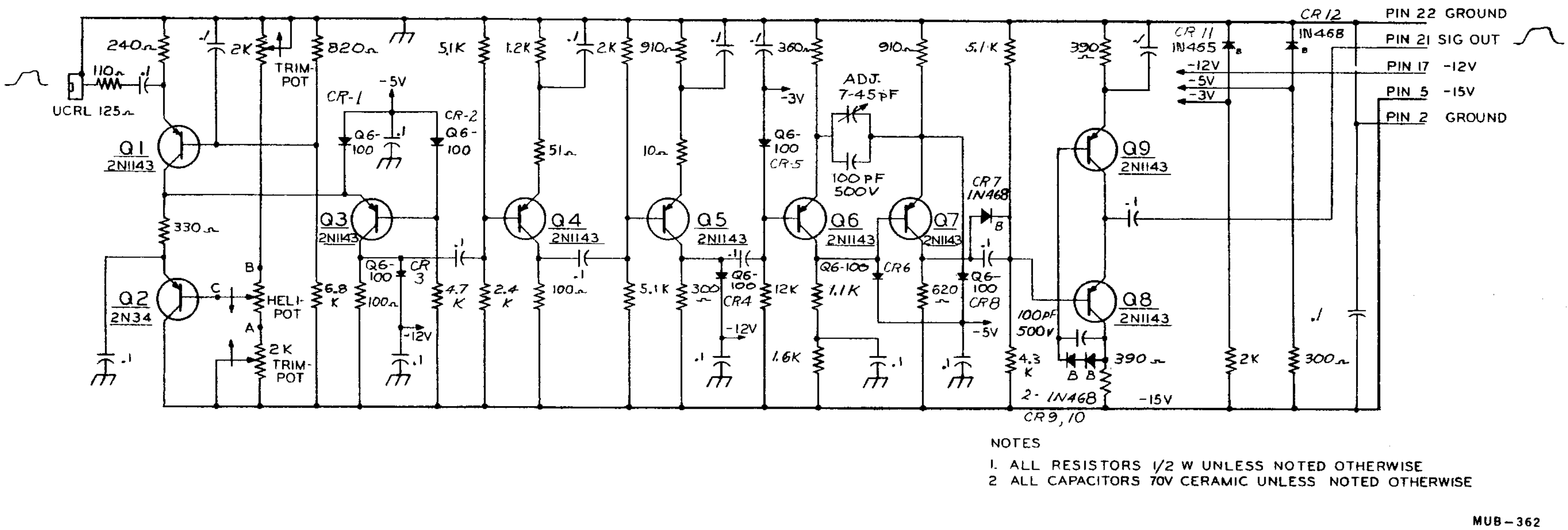


Fig. 7. Pulse-amplitude discriminator: schematic circuit diagram.

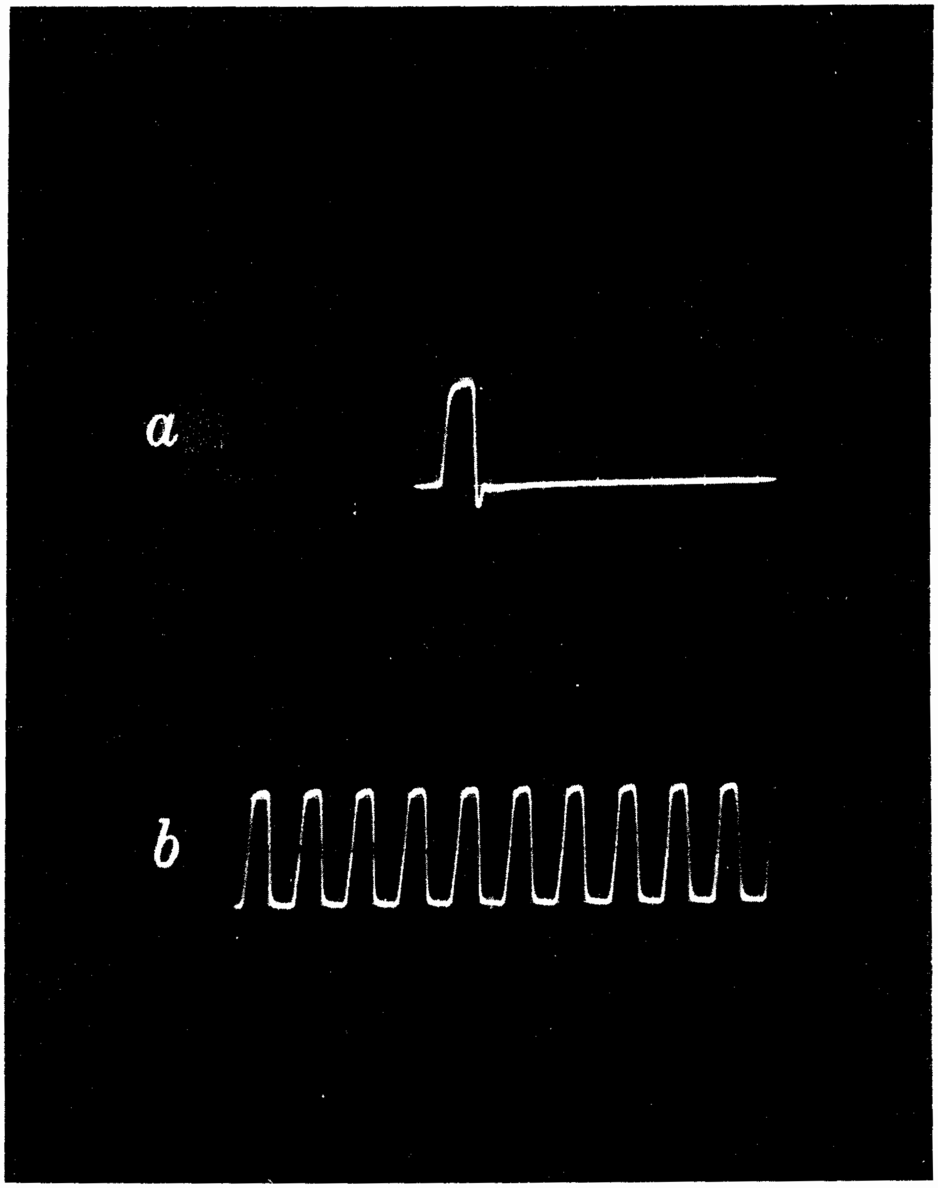


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Fig. 8. Pulse-amplitude discriminator output signals (a) at 10^6 pps repetition frequency, (b) at 10^7 pps. Horizontal sweep, 100 nsec/cm; vertical, 2 v/cm.

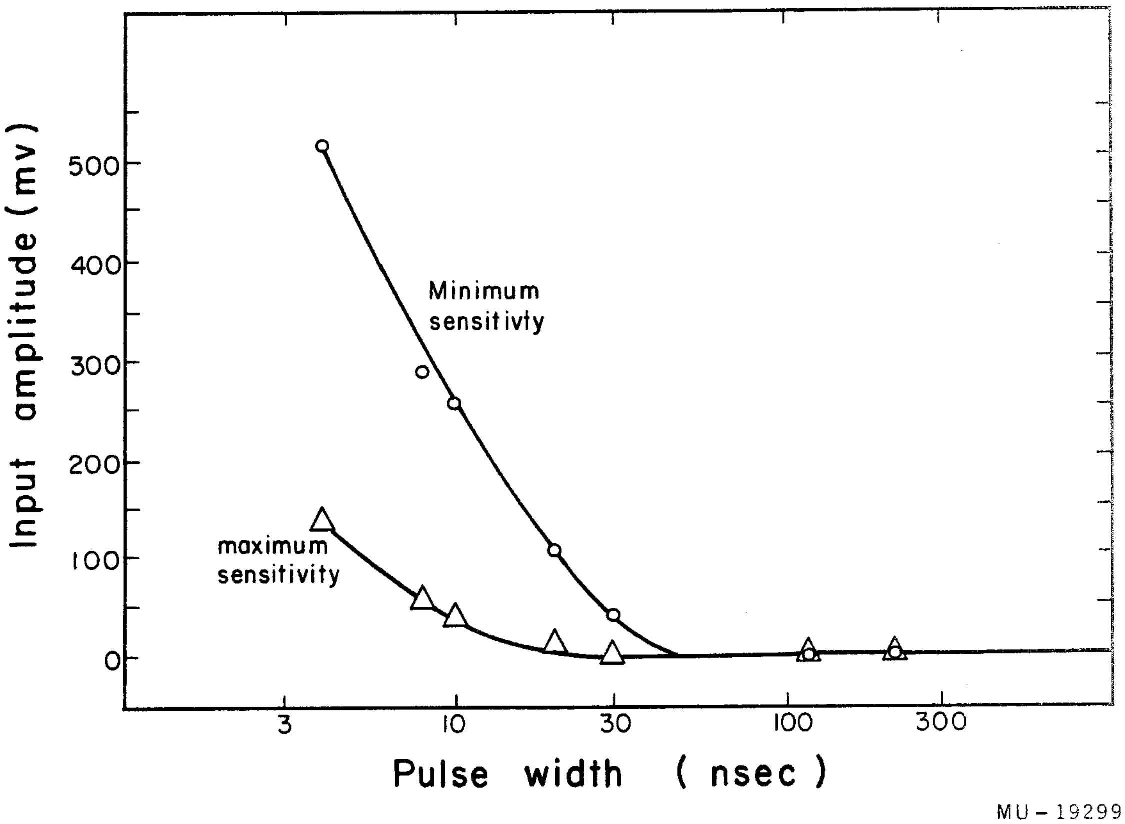

Fig. 9. Pulse-amplitude discriminator: excess input signal required for short pulse lenths at maximum and minimum threshold sensitivity settings. Repetition rate 60 pps.

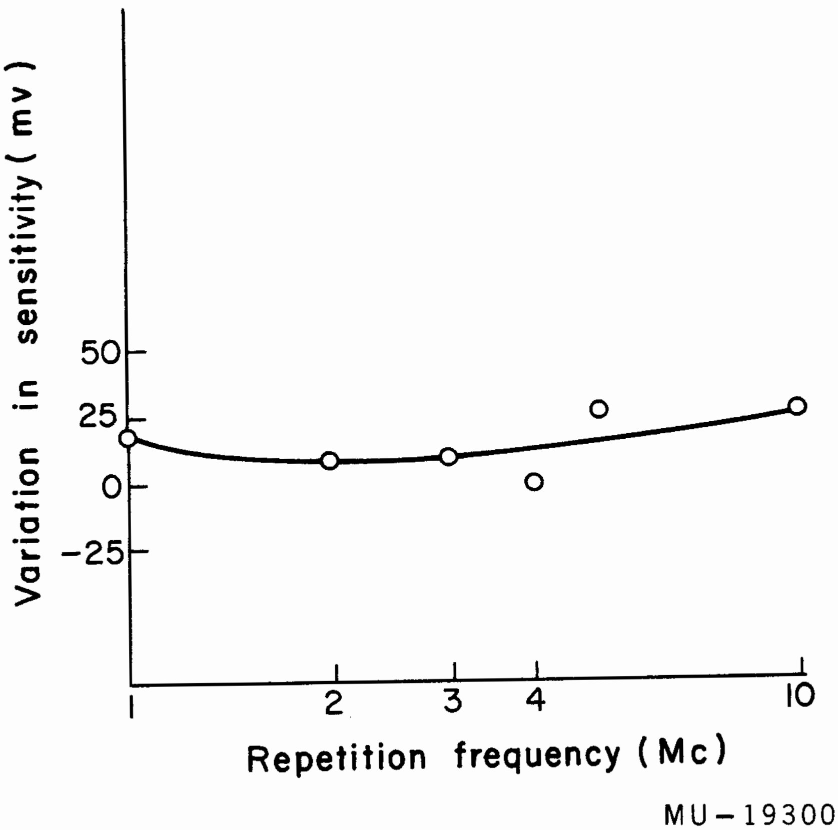

Fig. 10. Pulse-amplitude discriminator: input sensitivity at maximum threshold setting as a function of frequency. E_{in} = 2.3v; pulse width = nsec.

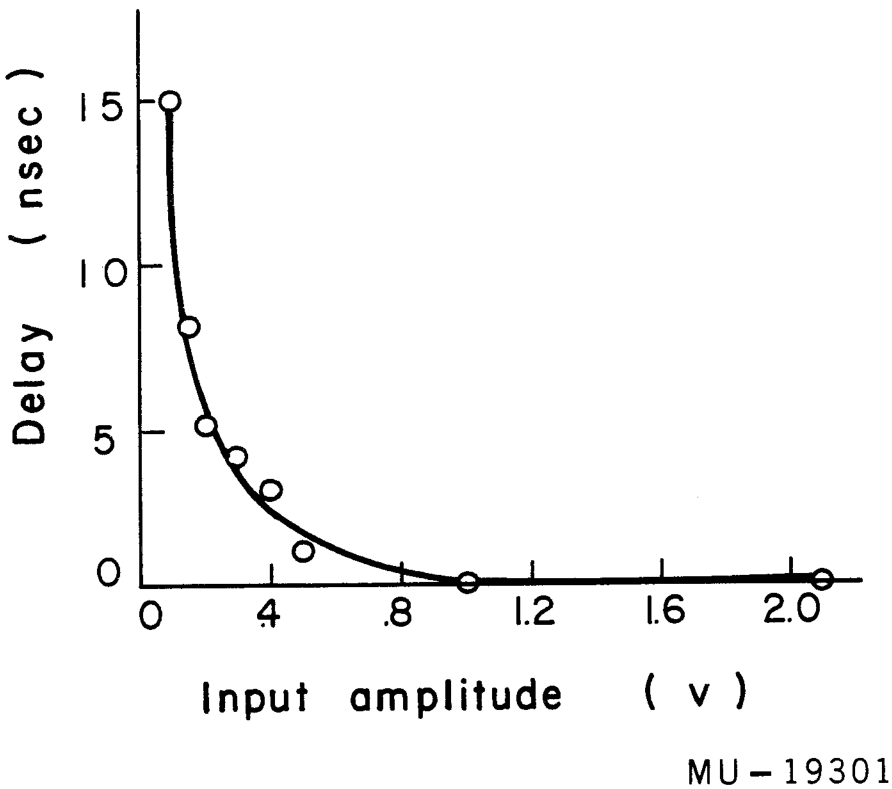

Fig. 11. Pulse-amplitude discriminator: relative delay of output signal as a function of input amplitude. E_{thresh} = 0.1 v; pulse width = 120 nsec.

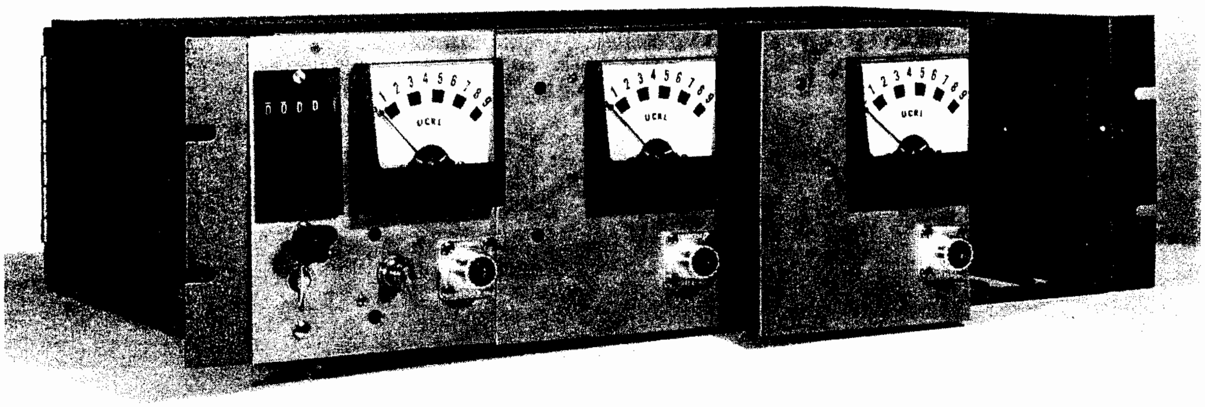

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Fig. 12. Plug-in-module decade scaler (front view).

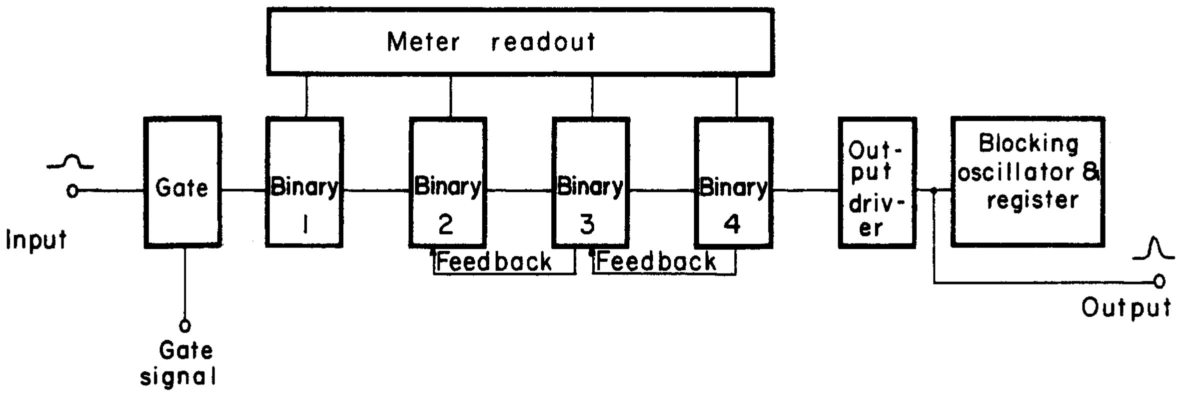

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Fig. 13. Decade scaler.

Specification:	5-Mc unit	1-Mc unit
Minimum resolution time (sec)	0.2	1.0
Minimum input amplitude (v)	+4	+4
Minimum pulse width (sec)	20	100
Maximum pulse width (sec)	1	1
Input impedance (ohms)	400	400

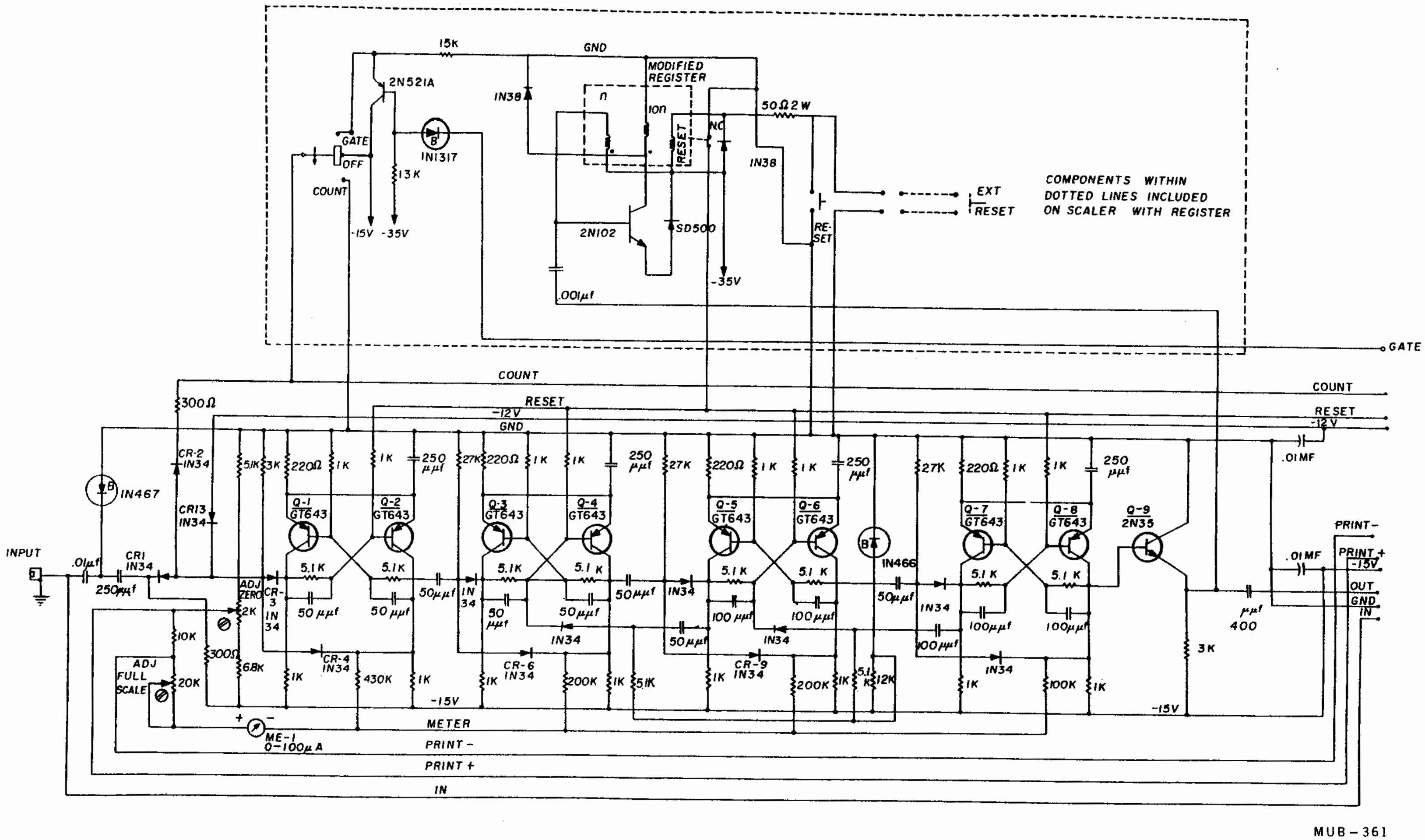

Fig. 14. 5-Mc decade scaler: schematic circuit diagram.