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End-to-end Power Optimization of Circuits for Analog Coherent Optical Links

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by

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Para mi papá.

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Abstract

End-to-end Power Optimization of Circuits for Analog Coherent Optical Links

by

Hector Andrade

Data centers today account for about 2.5 % of the total electricity usage in the United States. The portion of that power that is consumed by the internal network is increasing dramatically, as server-to-server traffic grows over 23 % every year. As a result, there is great demand for scalable power-efficient intra data center (IDC) optical communication links. IDC links today are based on intensity-modulation direct-detection modulation formats (IMDD). Thus far, the scaling of IMDD links has been achieved by increasing the number of signal amplitude levels, by moving to higher baud rates, and by adding multiple wavelengths or fibers. However, each of these scaling paths is severely constrained. Whereas IMDD systems only utilize the intensity of signal, coherent detection (CD) also leverages the two polarizations and two quadratures of the fiber optic channel, and thus is more scalable. CD also improves sensitivity by up to 20 dB by mixing the received signal with a strong local oscillator. CD has been employed in long-haul links for many years, yet these systems rely on power-hungry high-speed analog-to-digital converters (ADC) and digital signal processing (DSP) and thus may be unsuitable for IDC links. A compelling alternative to DSP-based CD is analog coherent detection (ACD), in which polarization demultiplexing, carrier recovery, and phase demodulation are performed using analog circuits.

This work focuses on the co-design of analog circuits and opto-electric devices that enable low-power ACD-based IDC links. First, a discussion of a proposed next-generation ACD IDC link architecture is outlined as motivation for the low-power circuit designs.

Three monolithic 50 Gb/s opto-electric receiver topologies in SiGe BiCMOS technology are analyzed and compared. Then, a 100 Gb/s QPSK hybrid receiver in 45 nm CMOS is described. The co-design of a driver 56 Gb/s and traveling-wave Mach-Zehnder modulator (TW-MZM) is also presented. Finally, the thesis describes a TW-MZM equalization technique based on a tunable termination mismatch.

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Chapter 1

Introduction

The past decades have seen an enormous increase in the number of Internet users, which is expected to reach 5.3 billion, or two thirds of the world's population, in 2023 [1]. Data centers have been crucial in enabling the explosive growth of the Internet and have become a key component of the world's infrastructure. In the United States, data centers currently consume 73 TWh of power per year. This accounts for 2.5% of total electricity usage and historically has doubled about every 8 years [2]. The portion of data center power that is consumed by the internal network is increasing dramatically, as server-to-server traffic grows over 23% every year [3].

Fig. 1.1 shows the US Department of Energy's Advanced Research Projects Agency – Energy (ARPA-E) data center power consumption forecast. The red curve denotes current power trends, accounting for improvements in computing efficiency due to Moore's Law, as the internal network data center power becomes more significant and electrical I/O power scales with data rates. The green curve depicts how the power consumption trend can be suppressed while meeting internet traffic demands by enabling optical I/O and optical switching. The latter has the potential to transform entire data center networks, leading to drastic improvements in power efficiency. However, to enable optical

switching it is necessary to have sufficient unallocated link budget to accommodate the added losses in the fiber channel. This is not feasible in the intra-data center (IDC) links that are deployed today, which already operate with a very restricted loss budget. As IDC link data rates continue to increase, the unallocated link budgets are not expected to grow. IDC links today are based on intensity-modulation direct-detection (IMDD) modulation formats. Scaling IMDD-based links to meet the future demands is already proving to be difficult. Instead, we propose a paradigm shift towards links based on analog-coherent detection, which can scale to higher data rates while potentially enabling optical switching by increasing the unallocated budget [4].

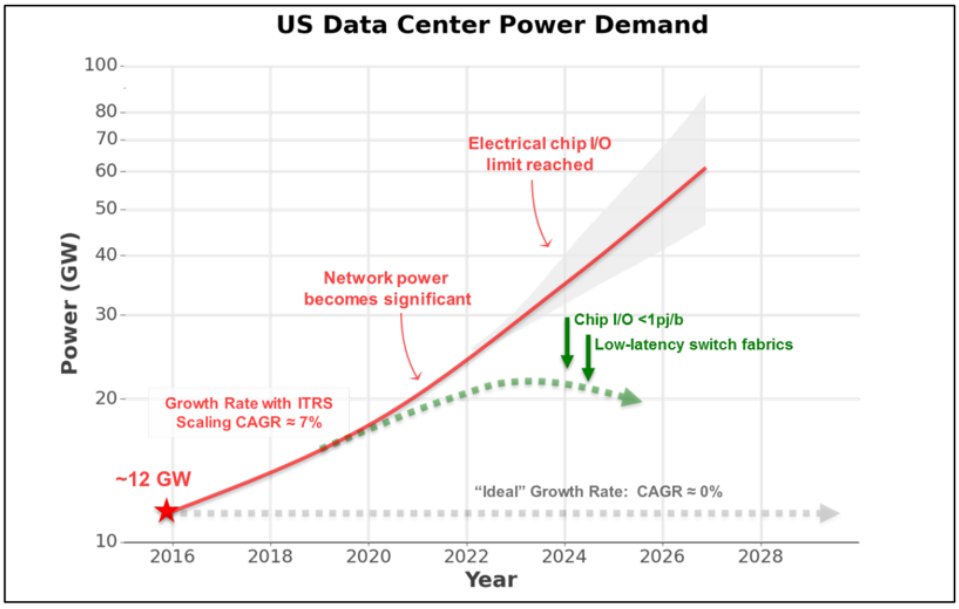

Figure 1.1: Aggregated power consumption of US datacenters as a function of time.

1.1 Intra-data Center Link Scaling Challenges

IDC links today are based on IMDD formats. Thus far, the scaling of IMDD links has been achieved by increasing the number of signal amplitude levels, by moving to higher

baud rates, and by adding multiple wavelengths or fibers [5]. However, each of these scaling paths is severely constrained. IMDD IDC links operate with a tight loss budget. Therefore, the sensitivity penalty that results from increasing the number of signal amplitude levels places a bound on scaling to higher order IMDD formats. Progressing to higher baud rates has become increasingly challenging as increases in data rates outpace the bandwidth improvements of electronic and photonic devices available in commercial semiconductor processes. It is prohibitively expensive to increment the number of fibers per link, since that requires continous recabling of the data center. Chromatic dispersion sets a limit on the optical transmission bandwidth. As a result, increasing the number of multiplexed wavelengths reduces the spacing between channels. This imposes stricter limits on the wavelength stability of the lasers, which are uncooled due to power density constraints. Whereas IMDD systems only utilize one of the intensity of signal, coherent detection (CD) also leverages the two polarizations and two quadratures of the fiber optic channel, and thus is more scalable. CD also improves sensitivity by up to 20 dB by mixing the received signal with a strong local oscillator, which can directly increase the unallocated link budget. CD has been employed in long-haul links for many years, yet these systems rely on power-hungry high-speed analog-to-digital converters (ADC) and digital signal processing (DSP) and thus may be unsuitable for IDC links. A compelling alternative to DSP-based CD is analog coherent detection (ACD), in which polarization demultiplexing, carrier recovery, and phase demodulation are performed using analog circuits. Power-efficient ACD links can scale to meet future generation data center demands while also enabling optical switching by increasing the unallocated link budget.

1.2 Optical Switching in Future Data Centers

Fig. 1.2 shows a simplified version of a conventional three-level data center fat-tree

topology network [6]. At the bottom of the hierarchy there are servers mounted on vertical racks, which are interconnected using top-of-rack (ToR) switches. The ToR switches are

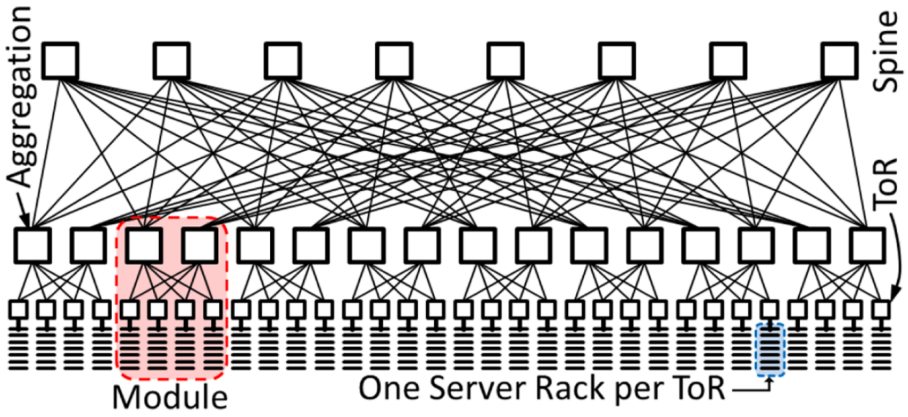

Figure 1.2: Conventional, three-level, folded-Clos (fat-tree) data center utilizing large spine and aggregation switches of the same size and smaller ToR switches [6].

interconnected via aggregate switches, and the aggregate switches are then connected using spine switches at the top of the network hierarchy. In modern data centers, optical IMDD links are used to connect ToR, aggregate, and spine switches. The electro-optical (EO) and opto-electric (OE) conversion required for each optical link requires significant amounts of power. Optical switching can eliminate the need for power-hungry EO-OE conversion at every node, and can have profound implications for the data center as a whole by enabling flatter, more power efficient networks. Fig. 1.3 depicts a novel data center network that employs optical routing in order to reduce the electrical switching levels from three to two [6]. In this design, arrayed waveguide grating routers (AWGRs) are inserted between the two electronic switching levels, resulting in a 50% reduction in the total number of required transceivers compared to a modern conventional data center network. In order to accommodate the optical AWGRs losses, it is necessary to increase the link loss budget. Following the analysis approach described in [7], Fig. 1.4 shows the achievable link budgets offered by candidate link architectures assuming the same laser powers, MZM modulators, and target BER of 10^{-5}. Our proposed ACD QPSK

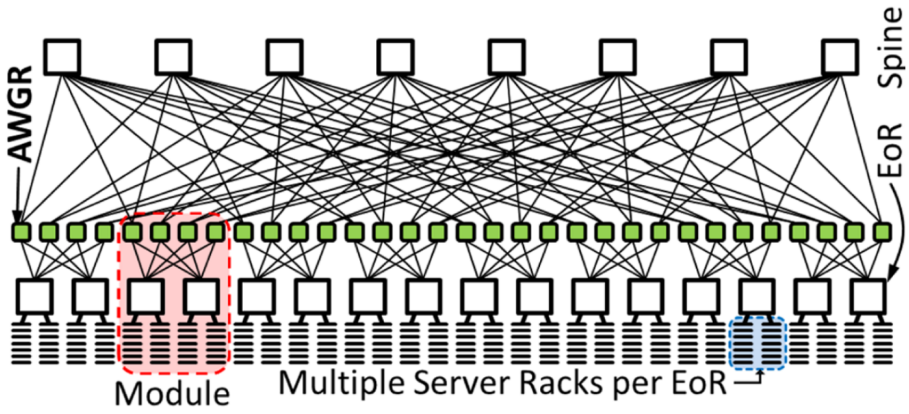

Figure 1.3: Novel data center architecture utilizing two levels of large (spine and EoR) electronic switches of the same size, interconnected with WDM fibers, with an added layer of AWGRs (small, shaded boxes) [6].

implementation can enable optical routing by supporting link budgets of 13 dB with a wall-plug power efficiency of 5 pJ/bit [4].

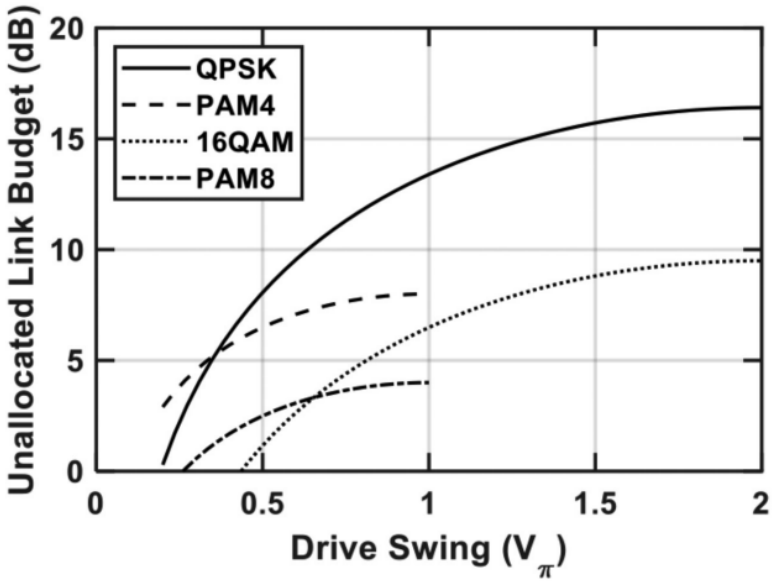

Figure 1.4: Comparison of unallocated link margin in coherent and IMDD links, assuming MZM drive, and a target BER of 10^{-5}. The QPSK curve assumes analog coherent link performance as described in [4].

1.3 Analog Coherent Link Implementation

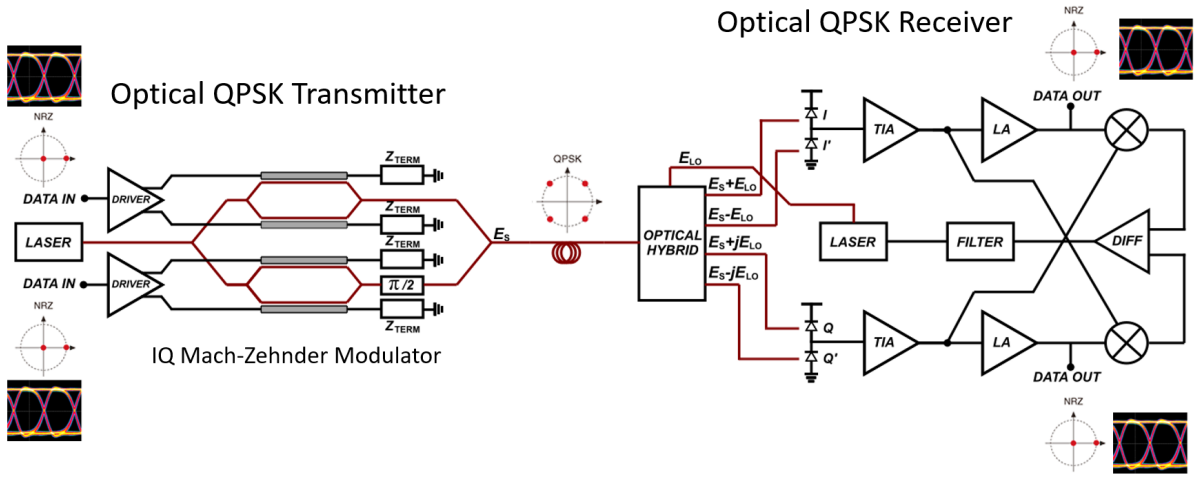

Figure 1.5: Proposed implementation of an analog coherent QPSK optical link.

Our proposed link implementation, as described in [4], is an O-band analog coherent wavelength-multiplexed 200 Gb/s/λ DP-QPSK link with an OPLL-based receiver. The transmitter consists of a IQ modulator for each polarization, each of which contains two nested traveling wave Mach-Zehnder modulators (TW-MZMs) that are out of phase by $\pi/2$. The TW-MZMs are null-biased to produce a phase inversion at each bit transition. Each wavelength utilizes a separate O-band laser. The nested TW-MZMs are each modulated using differential limited drivers, each of which produces a 56 Gb/s on-off keying (OOK) signal. A polarization splitter rotator (PSR) at the output of one of the two QPSK modulators rotates the TE component to TM to generate the DP-QPSK signal, which propagates across up to 2 km of single-mode fiber. The link has an unallocated budget of 13 dB. The signal is then coupled to a QPSK receiver that employs a Costas Loop for carrier recovery and phase demodulation [8]. Costas-loop based optical phase-locked loops (OPLL) have been previously demonstrated at up to 40 Gb/s [9]. At the receiver, a polarization controller recovers the original transmitted state of polarization. Then a PSR is used to rotate the TM component to TE so it can propagate along the

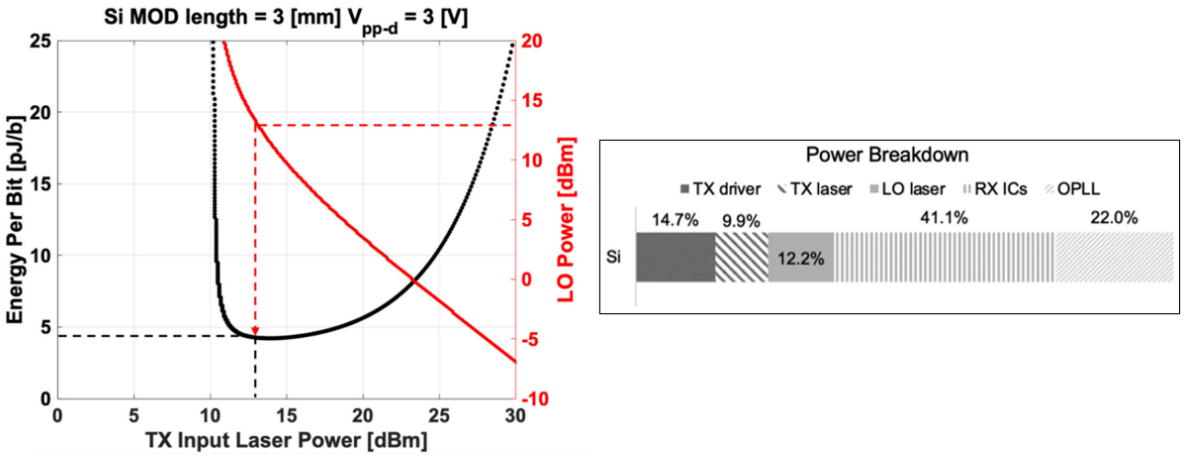

Figure 1.6: Calculated link power efficiency in pJ/bit vs transmitter input laser power for the link implementation described in [4]. The power breakdown corresponds to the optimum power efficiency point. The transmitter and receiver circuits account for about 80 % of the total power.

waveguides on the receiver. Each QPSK signal is then routed to an optical 90-degree hybrid. The other input of the hybrid is a local oscillator tunable laser. The hybrid generates the four signals corresponding to the desired vectorial additions of the two input optical fields, which are routed to two pairs of photodiodes (PD), one for the in-phase (I) channel and the other for the quadrature channel (Q). Balanced or differential PDs convert the I and Q optical signals into photocurrent. The PDs are connected to TIAs, which convert the photocurrent into a voltage signal. Limiting amplifiers are then used to amplify and limit the signal. A phase-frequency detector (PFD) is implemented by mixing the I and Q channels and subtracting the output signal via a differential to single-ended amplifier. At the output of the amplifier is the PFD error signal, which in the phase-locked state is proportional to the phase error between the local oscillator and the carrier of the received signal. The PFD output signal is then filtered by a loop filter, which typically is a proportional-integral (PI) controller. The loop filter output is connected to a phase section of the local oscillator laser, which functions as a current-controlled oscillator. This closes the phase-locked loop. The proposed implementation

for one of the multiplexed wavelengths for each of the two polarizations is shown in Fig. 1.5.

It has been calculated [4] that the transmitter and receiver electronics consume the majority of the total link power. Fig. 1.6 contains a plot of the calculated link power efficiency in pJ/bit as a function of the transmitter input laser power for a specified bit-error rate of 1^{-5}. The power breakdown, which corresponds to the optimum power efficiency point, indicates that the circuits account for about 80% of the total power.

1.4 Overview

In our proposed ACD link implementation, the majority of the power is consumed by the transmitter and receiver circuits. This work focuses on the co-design of analog circuits and opto-electric devices that enable low-power ACD-based IDC links.

In chapter 2, three monolithic 50 Gb/s opto-electric receiver topologies in SiGe BiCMOS technology are analyzed and compared. Then, chapter 3 describes a 100 Gb/s QPSK hybrid receiver in 45 nm CMOS. Chapter 4 presents the co-design of a TW-MZM 56 Gb/s driver implemented in 130 nm SiGe BiCMOS. Finally, in chapter 5, a TW-MZM equalization technique based on a tunable termination mismatch fabricated in a monolithic 90 nm silicon photonics process is demonstrated.

Chapter 2

Transimpedance Amplifiers in Monolithic Electronic/Photonic 250 nm SiGe BiCMOS

2.1 Introduction

The optical interconnect industry is in the process of moving towards 400G Ethernet with current standards supporting 4 streaming channels at 53.125 GBd PAM-4 [10, 11]. However, PAM-4 adds linearity requirements on the TIA circuitry relative to NRZ signaling and has reduced sensitivity resulting in limited link power margin. For low-power applications, such as analog (DSP-free) optical coherent links that employ DP-QPSK modulation [5], there is demand for high sensitivity TIAs that operate above 50 Gb/s. Fig. 2.1 shows the TIA within an analog optical QPSK receiver. The increasing bandwidth (BW) and sensitivity requirements set stringent design tolerances on the receiver packaging parasitics that result from hybrid optoelectronic integration. Monolithic optoelectronic (O/E) integration drastically reduces parasitics since wirebonds and

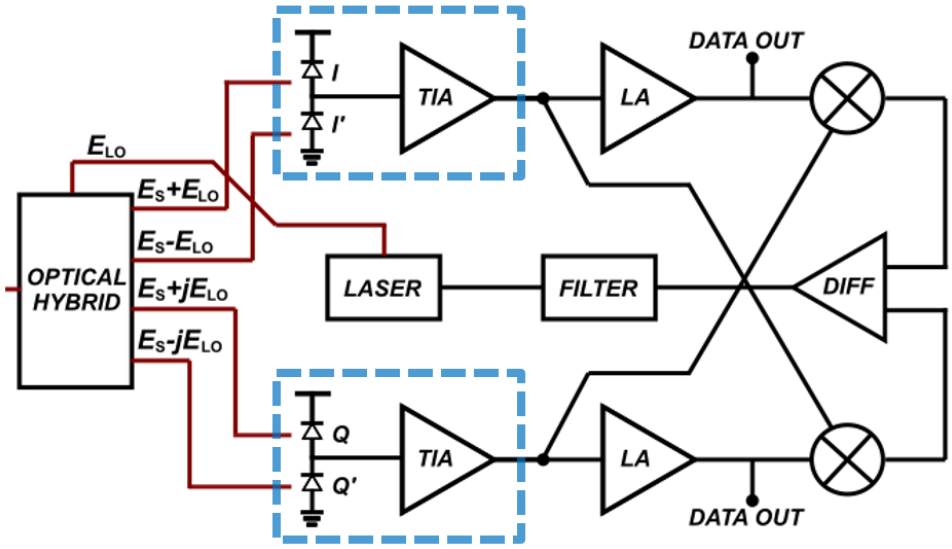

Figure 2.1: TIA within an analog optical coherent QPSK receiver.

bond pads are replaced with back-end-of-line interconnects [12]. The reduction in the wiring capacitance improves the achievable transimpedance for a given transistor performance. Prior high-rate monolithically integrated TIAs have been demonstrated based on SiGe processes. In [13], 25 Gb/s transmission was achieved at a power efficiency of 1.5 pJ/bit, and a 90 Gb/s AC-coupled receiver was shown in [14]. The Cherry-Hooper with emitter-follower (CHEF) topology, which we employ in our receivers, has been previously utilized in an receiver operating at over 50 Gb/s [15]. In this chapter we report three monolithically-integrated optical receiver designs that achieve up to 40 Gb/s at BER = 10^{-12} without transmitter equalization and 50 Gb/s at BER = 10^{-10} with transmitter equalization at a power efficiency as low as 1.1 pJ/bit. In Section 2.2, the advantage of monolithic integration is examined in the context of the transimpedance limit. A comparison of the balanced differential, unbalanced differential, and AC-coupled TIA topologies is presented in Section 2.3. Section 2.4 details the core TIA circuit design and comparison of noise performance in each of the three designs. The experimental results are discussed in Section 2.5 and the chapter is concluded in section 2.6.

2.2 Monolithic Integration and Transimpedance Limit

The transimpedance is given by:

$$R_T = \frac{A}{A+1} R_f \approx R_f \tag{2.1}$$

where A is the open-loop gain of the amplifier. The approximate expression is valid when $A >> 1$. The transimpedance limit describes the maximum transimpedance, R_T, that a TIA can attain for a given BW and device technology as characterized by the unity current gain transition frequency f_T [16, 17].

$$R_{T,max} \approx \frac{f_T}{2\pi C_{in} f_{3dB}^2} \tag{2.2}$$

where f_{3dB} is the desired 3-dB BW, and C_{in} is the total input capacitance. This expression is obtained by relating the BW to the open-loop gain by the approximation $A \approx f_T/f_{3dB}$ and assuming the photodiode (PD) series resistance is small. Given constraints on the acceptable BW and device technology, the input capacitance of the TIA directly impacts how much transimpedance is achieved with a single gain stage. When transimpedance is limited to lower values, more gain stages are required at the expense of power consumption and noise.

A hybrid approach to integration incorporates bond pads to connect a PD chip to the TIA (Fig. 2.2 (a)). Ignoring series inductance, e.g. wirebonds, for illustration purposes, $C_{in} = C_j + 2C_{pad} + C_{amp}$, where C_j is the PD junction capacitance, C_{pad} is the bond pad capacitance, and C_{amp} is the capacitance due to the amplifier. In a monolithic receiver (Fig. 2.2 (b)), the bond pads are eliminated and $C_{in} = C_j + C_{amp}$. Additionally, ESD protection devices are not required in the monolithic approach, which results in a further reduction of C_{in}. The reduced C_{in} of the monolithic approach should improve the R_T.

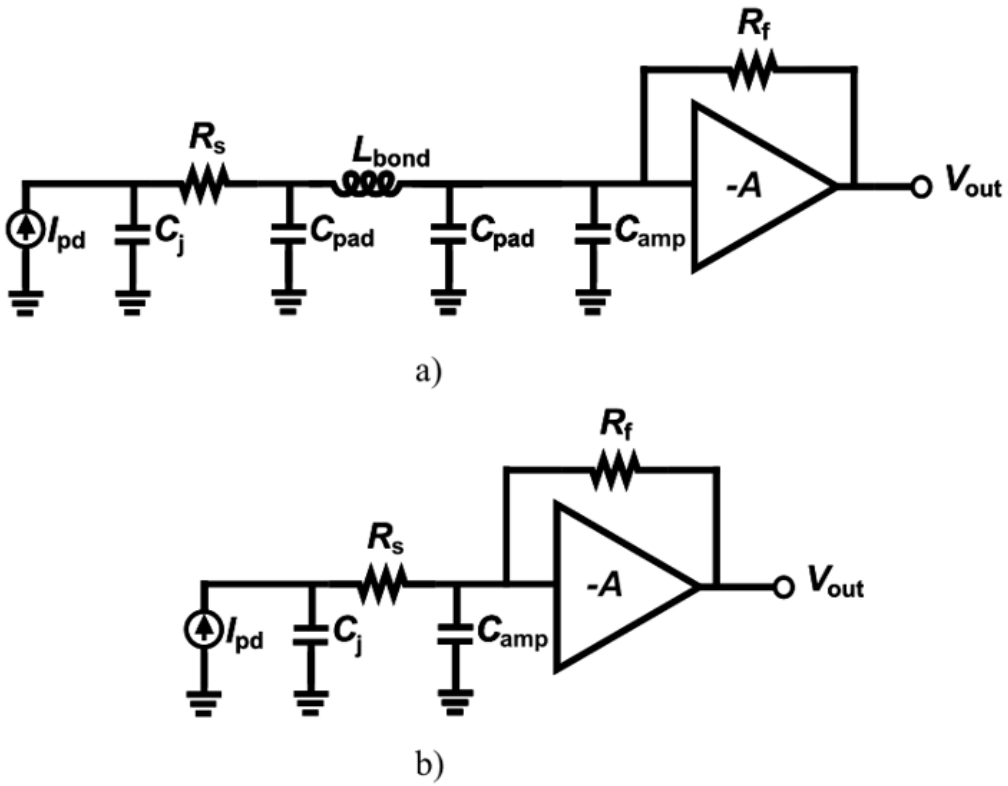

Figure 2.2: Shunt-feedback TIA with PD model a) with packaging parasitics (hybrid integration) and b) without packaging parasitics (monolithic integration).

To understand the trade-off in transimpedance limit from monolithic integration of the PD, Fig. 2.3 shows the transimpedance limit for various data rates with C_j = 10 fF, C_{amp} = 10 fF, and f_T = 190 GHz as a function of the bond pad capacitance. The 3-dB BW is assumed to be 2/3 of the bitrate. The resistance, which is plotted in dBΩ, is given by $R(dB\Omega) = 20log_{10}(R)$. The bond pad capacitance scales with 4.5 pF/mm^2 to account for variation in the bond pad area. The dotted vertical lines indicate common dimensions of square bond pads. The detrimental effect of the bond pad capacitance is significant even for small bond pads.

In the case of the monolithic receiver at 50 Gb/s, an R_f of 62.5 dBΩ can be achieved, while in a hybrid receiver it drops below 57 dBΩ for 50 µm x 50 µm bond pads. A bond pad of these dimensions can be difficult to bond reliably and 75 µm x 75 µm bond pads

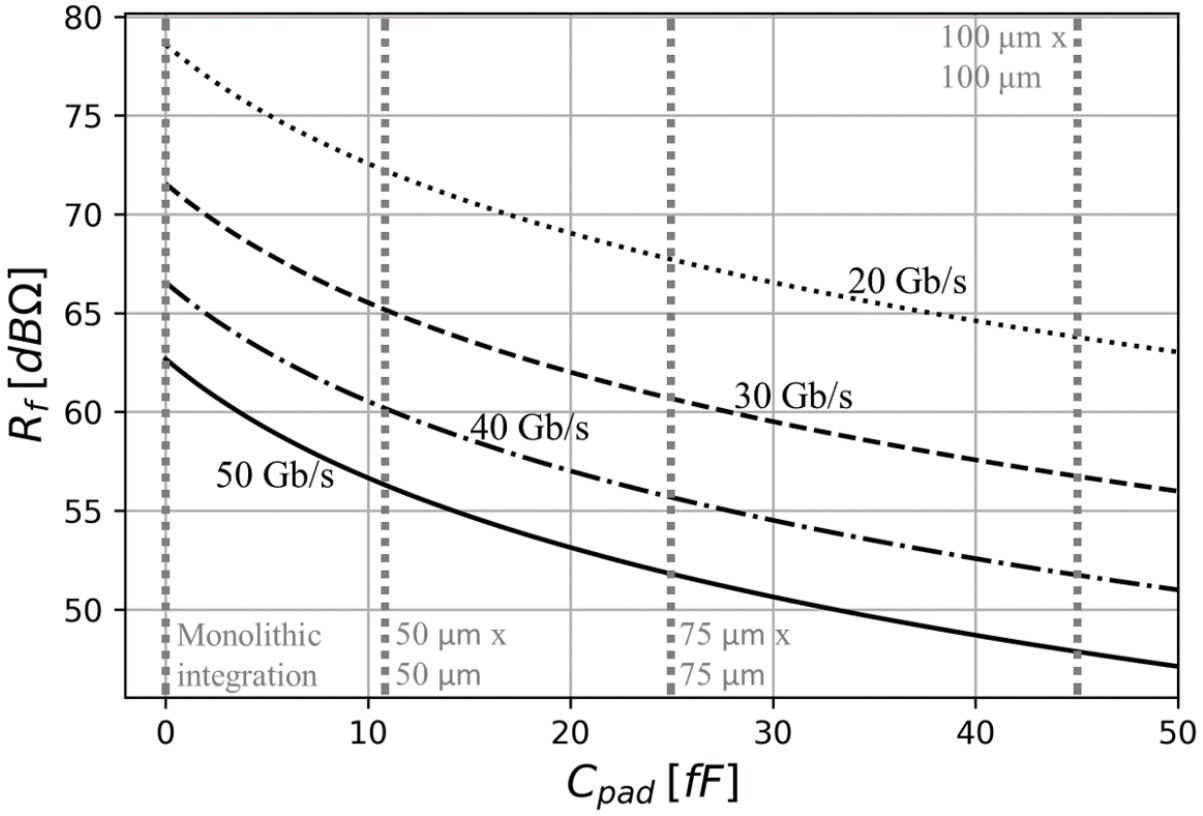

Figure 2.3: Transimpedance limit versus bond pad capacitance at various data rates. The dotted vertical lines indicate the dimensions of a square bond pad.

or greater may be required for volume manufacturing. This would result in a R_T of 52 dBΩ, which constitutes a reduction of over 70 % as compared to monolithic. It can be observed that this reduction in percentage is equal for all data rates.

The derivation of the transimpedance limit does not account for the bandwidth extension that is possible with a series inductance between the PD and TIA. Hybrid integration can introduce a bond wire (L_{bond}) to provide this bandwidth extension [18] with respect to the known bond pad and photodiode capacitance. However, the required inductance for bandwidth extension at 50 Gb/s for bond pads below 40 fF is greater than 1 nH. For monolithic integration the 3 nH of inductance is required, which is likely too large to be feasibly implemented as an on-chip inductor.

2.3 TIA Topology Comparison

While the transimpedance limit indicates the trade-off between a transistor and photodetector, it does not lend to conclusions regarding the sensitivity, overload current, or voltage offset metrics relevant in modern optical communications. Two sources contribute to DC voltage offset at the output of a differential TIA. The first is the input DC current difference between the two differential inputs and is inherent to connections to single-ended photodiodes. A clear example is the unbalanced differential TIA, in which the photodiode is connected to only one of the two TIA inputs, and thus has an unbalanced input DC current. We will refer to the elimination of its resulting offset as DC level restoration (DCLR). The second source is the random, built-in voltage offset that is caused by process variations during semiconductor fabrication and is present in all TIA variants. Its elimination is referred to as DC offset compensation (DCOC). Both DCLR and DCOC may be implemented with automatic control loops [19]. Here, we analyze three common TIA topologies that utilize differential amplifiers to gain insight into their design trade-offs. The three variants are shown in Fig. 2.4 consisting of balanced, unbalanced, and AC-coupled architectures.

In the balanced variant (2.4 (a)), matched PDs are connected to each of the differential inputs. This architecture is commonly used with a single PD where the other input is connected to an on-chip capacitor designed to match the PD capacitance. However, an advantage of monolithic technologies is that it is convenient to utilize an actual dark PD, which improves matching. This topology is employed in applications such as coherent systems where only balanced detection is possible after 90-degree hybrids. In IMDD systems one PD receives the signal while the other PD is left dark. This variant requires DCLR to cancel the effect of the DC current imbalance in addition to DCOC. Both can be achieved by inputting a DC optical signal to the otherwise dark photodiode. One

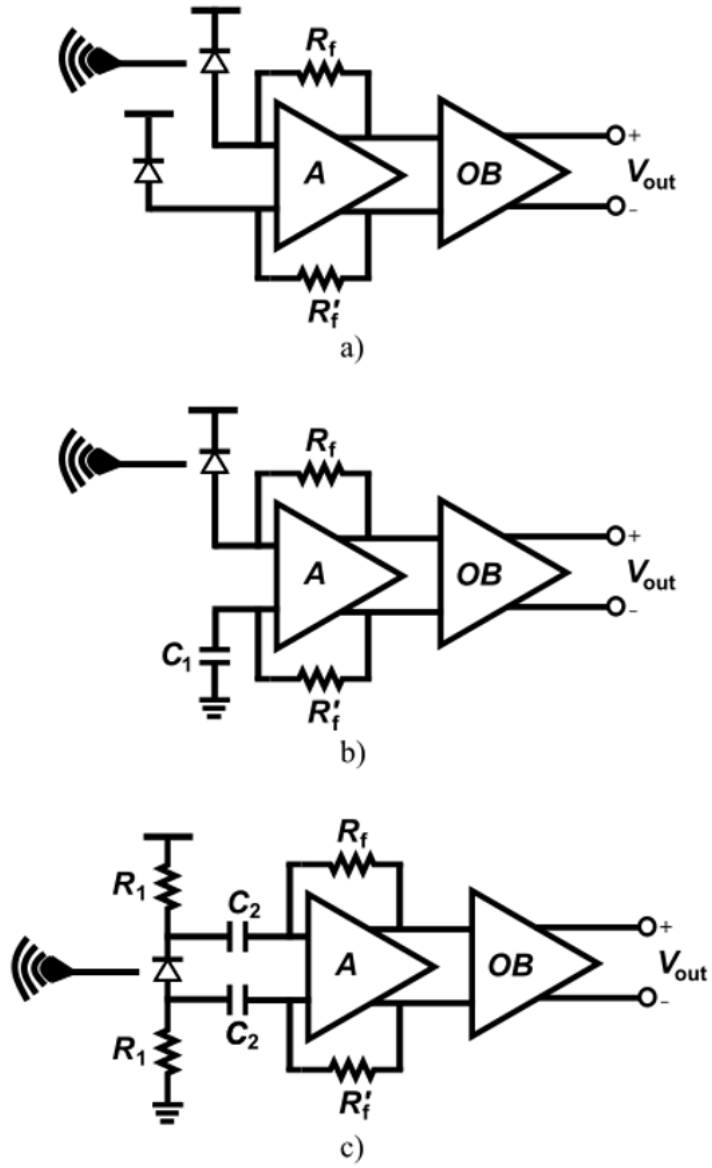

Figure 2.4: Block-level schematic of the a) balanced, b) unbalanced, and c) AC-coupled differential TIA variants.

advantage of this topology is that any power supply or substrate noise will couple equally to both inputs and is expected to be rejected as a common-mode signal [19].

In the unbalanced, or pseudodifferential, variant (2.4 (b)), the dark PD is replaced with capacitor C_1, which in our implementation is a 1.2 nF off-chip capacitor that provides an AC ground at the input. This eliminates the noise contribution of $R_f^{'}$ down to the

cutoff frequency determined by C_1 and the input resistance R_{in}, which is given by $R_{in} \approx R_f/A$ for $A >> 1$. However, the input impedances are no longer balanced, and thus immunity to noise from the power supply and the substrate is poor. Additionally, the input capacitor must be large at the expense of silicon die area or off-chip assembly. An external current source can be connected to the capacitor input, since both DCOC and DCLR are required.

In the AC-coupled variant (2.4 (c)), each PD terminal is connected to one of the R_1 resistors (2 kΩ) and capacitors C_2. In our implementation these capacitors are realized as 4 pF on-chip metal-insulator-metal (MIM) capacitors. R_1 and C_2 set the low-frequency cutoff frequency of the receiver. DCOC is required but DCLR is not, because there is no DC current at any of the TIA inputs.

Both unbalanced and AC-coupled variants can be employed in IMDD systems such as VCSEL-based optical interconnects [20].

The midband gain of each TIA variant is investigated with the small-signal model transfer functions assuming an emitter-coupled differential pair amplifier. The schematics, assuming a large r_π, are shown in Fig. 2.5. Since the purpose of the model is to obtain the midband gain, the large capacitor of the unbalanced variant is assumed to be grounded and the junction capacitance of the dark PD of the balanced variant is considered to be an open circuit. The R_1 of the AC-coupled variant produces a low-pass response with C_j and thus must be small enough to not limit the overall receiver BW. However, it must be large enough that the R_1, R_{in} current division does not significantly reduce the midband gain. The transimpedance gain of the balanced receiver is

$$R_{T,BAL} = \frac{V_{o1}}{i_{PD}} = \frac{R_C(2 + g_m(R_C - R_f))}{2 + 2g_m R_C} \approx -\frac{R_f}{2} \tag{2.3}$$

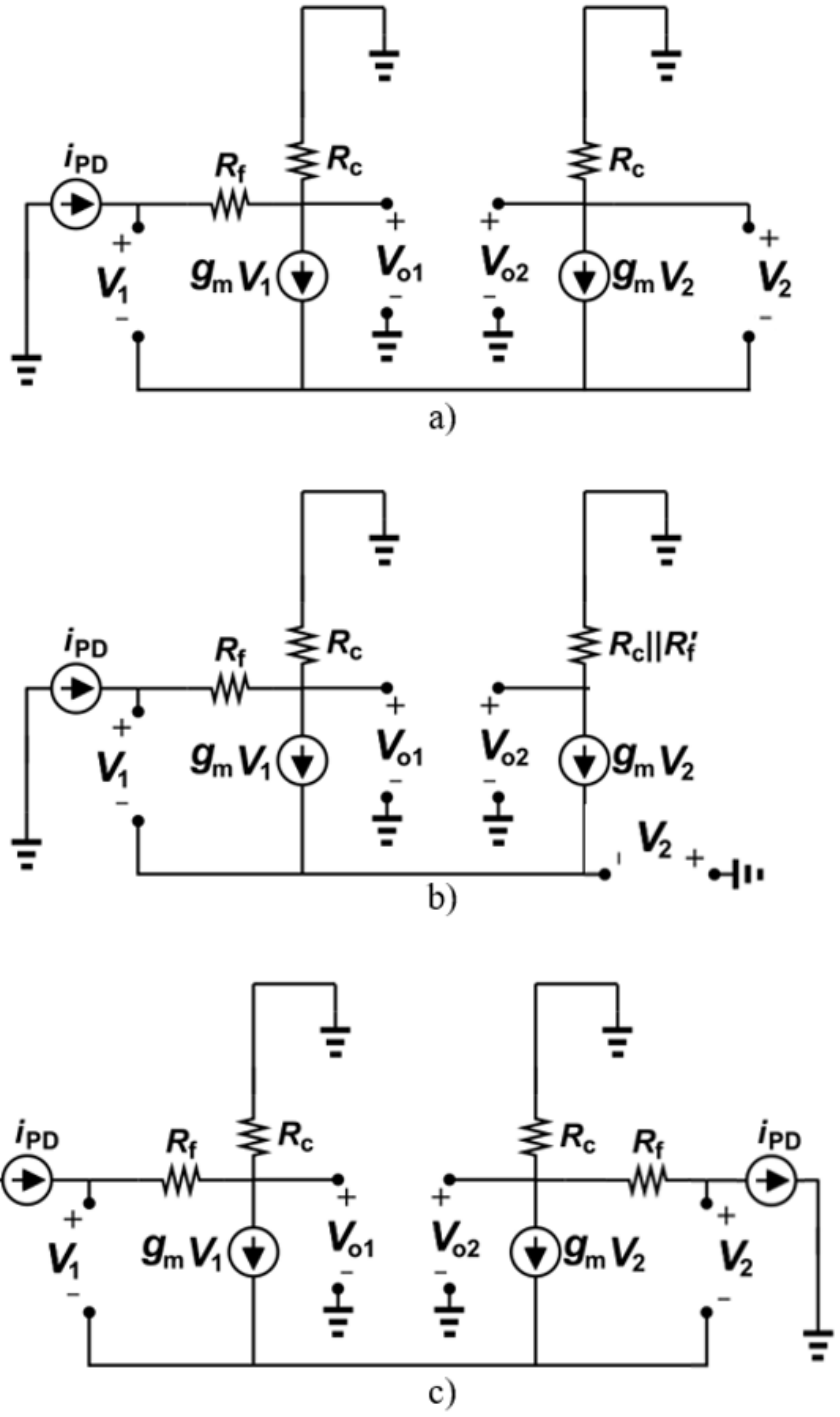

Figure 2.5: Small signal model assuming $r_\pi >> 1$ of the a) balanced, b) unbalanced, and c) AC-coupled variants.

for the unbalanced receiver it is

$$R_{T,UNBAL} = \frac{V_{o1}}{i_{PD}} = \frac{R_C(2 - g_m R_f)}{2 + g_m R_C} \approx -R_f \tag{2.4}$$

and for the AC-coupled receiver it is

$$R_{T,AC} = \frac{V_{o1}}{i_{PD}} = \frac{R_C(1 - g_m R_f)}{1 + g_m R_C} \approx -R_f \tag{2.5}$$

The approximate expressions are valid when $g_m R_C >> 1$ and $R_f >> R_C$, which is conventionally true. For TIAs that utilize high amplifier gain, the transimpedance of the unbalanced configuration is expected to be close to twice that of the balanced one. Likewise, the transimpedance of the AC-coupled variant is also approximately twice as large since both PD terminals are connected to the TIA. This doubles the input differential current.

We will inspect the details of these implementations and the noise characteristics of the different circuits in the following section.

2.4 TIA Circuit Design

All three TIA variants were realized with the same core circuit and were nominally biased at the same DC operating points shown in Fig. 2.6. It consists of a shunt-feedback TIA and a 50 Ω differential output buffer. The voltage amplifier has a Cherry- Hooper with emitter-follower (CHEF) feedback topology and emitter follower buffers at the output. The design of the CHEF amplifier utilizes feedback between cascaded common-emitter amplifiers to extend the bandwidth provided that the inverse transconductance of the second stage is much smaller than the value of the feedback resistance between the stages. Emitter-followers are added to drive the load capacitance. The resistor values of

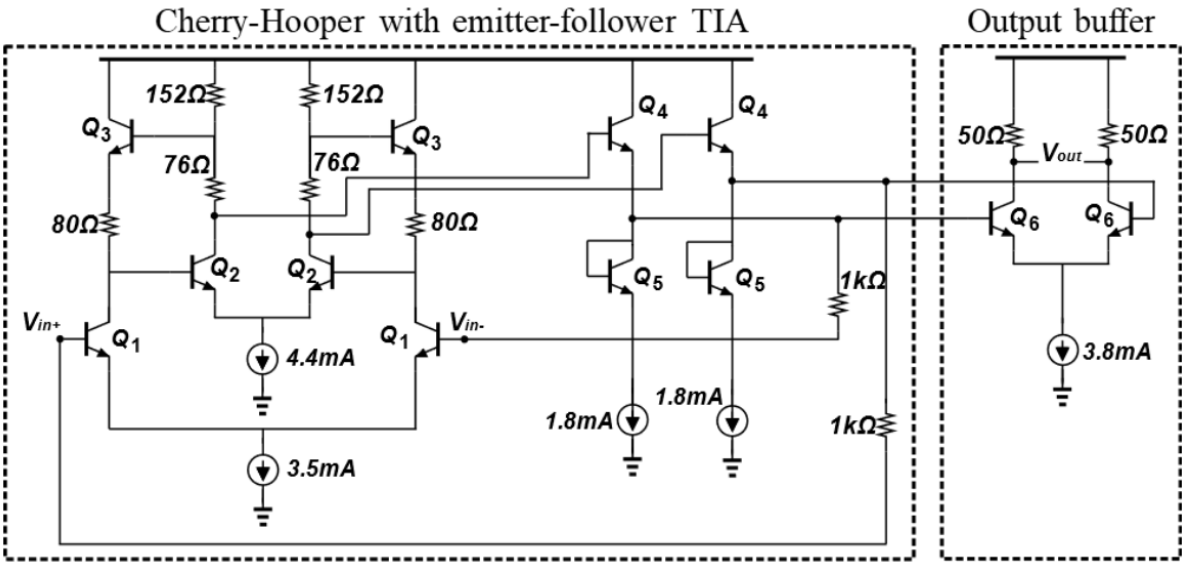

Figure 2.6: Receiver core schematic, common to all three variants.

R_f (1k Ω), R_1 (152 Ω), R_2 (76 Ω), and R_3 (80 Ω) are chosen to produce a Bessel response where the group-delay is maximally flat [21].

A Ge PD is incorporated into the SiGe process and has a reported bandwidth of 70 GHz, a responsivity at 1550 nm of 0.9 A/W, series resistance of 35 Ω, and junction capacitance of 10 fF [22]. Therefore, we anticipate that the circuit response is the limiting factor for the overall 3-dB bandwidth.

2.4.1 Frequency response

Fig. 2.7 plots the single-ended small-signal transimpedance gain of the three receiver variants including output inductance (150 pH) and capacitance (40 fF) that result from packaging parasitics and an RC PD model to verify the midband transimpedance gain prediction. This simulation does not account for post-layout parasitics. While there is a difference of approximately 5 dB between the balanced and unbalanced variants, the -3 dB electrical bandwidths are similar (40.3 GHz, 37.6 GHz, and 38.6 GHz for

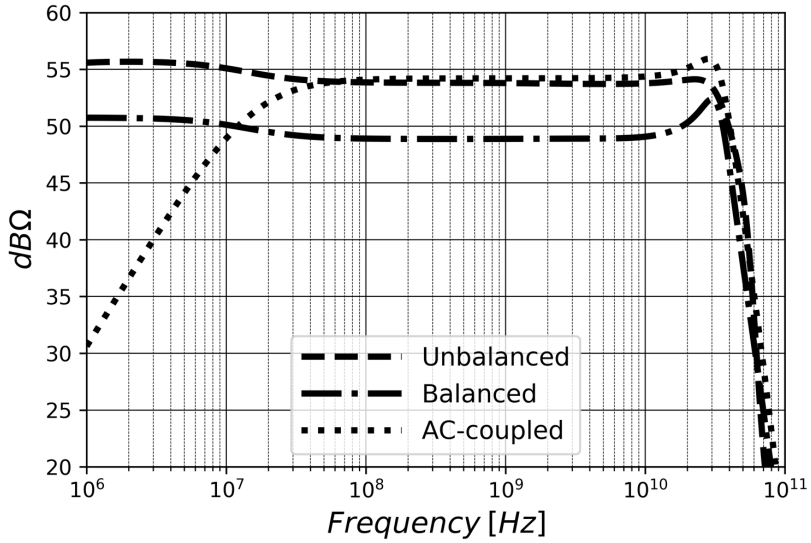

Figure 2.7: Simulated transimpedance gain of the three receiver variants. Output wirebond inductances (L = 150 pH) and bond pad capacitances (C = 40 fF) are considered.

the balanced, unbalanced, and AC-coupled variants, respectively). The midband gain difference is approximately equal to what was predicted in section 2.3. The DC-cutoff of the AC-coupled receiver is 20 MHz, which is viable for use in 8b10b encoded links but is not suitable for 64b/66b encoding. The DC-cutoff frequency is limited by chip area and MIM parasitics. And for large capacitors, self-resonance of the DC-blocking MIM capacitors should also be considered.

2.4.2 Group-Delay Variation

The CHEF amplifier was designed for a flat GDV. However, the addition of the PD and the packaging parasitics, as well as the resistors and capacitors specific to each topology, resulted in an increased GDV. The GDV above 1 GHz, shown in Fig. 2.8, is 6 ps in the unbalanced variant, 12 ps in the AC-coupled variant, and nearly 18 ps (0.9 UI at 50 Gb/s) in the balanced variant. Fig. 2.9 shows the GDV and frequency response of the CHEF TIA assuming an ideal PD with $C_j = 0$. The transimpedance has 5 dB of

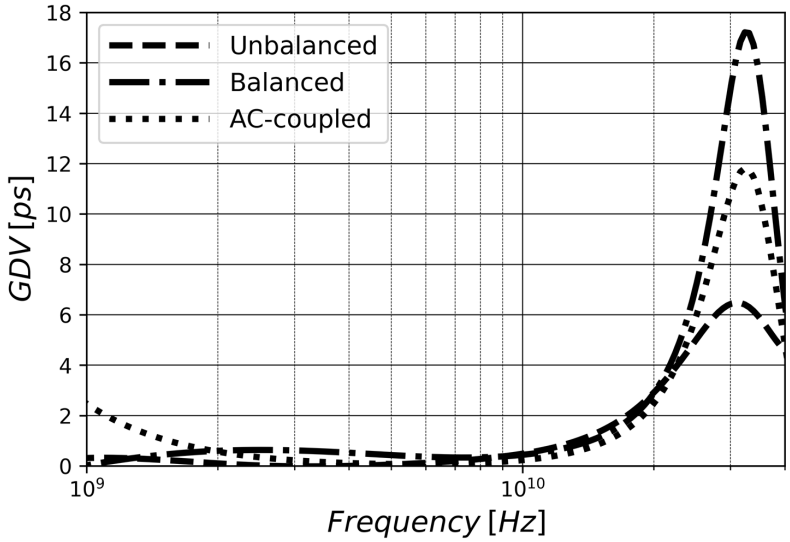

Figure 2.8: Simulated GDV above 1 GHz of the three TIA variants.

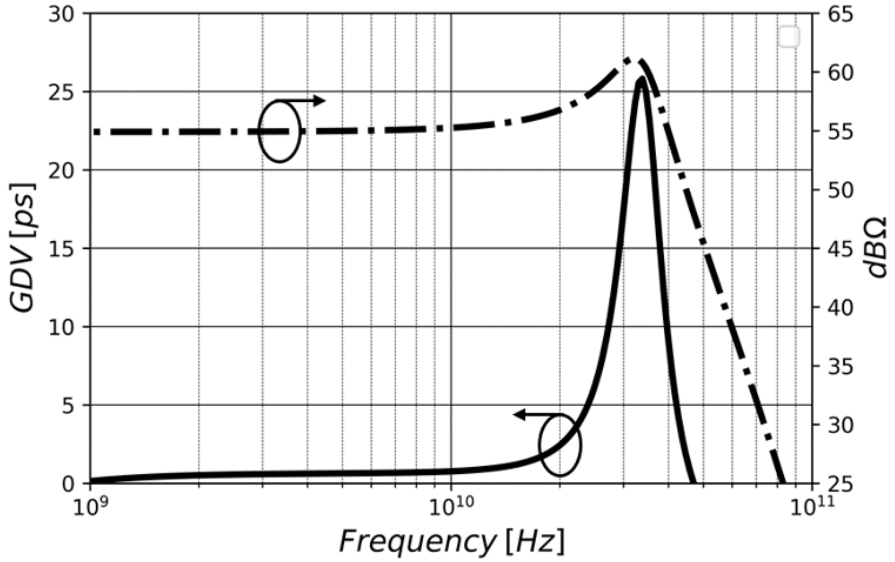

Figure 2.9: CHEF TIA simulated GDV and transimpedance above 1 GHz with an ideal PD ($C_j = 0$).

peaking, which introduces a GDV of over 25 ps. The PD C_j and the other capacitances introduced in the receiver variants serve to dampen the response and decrease the GDV. Fig. 2.10 shows the normalized frequency response of the three front-end topologies when the CHEF TIA is replaced by an ideal resistor R_{in}. The BWs are 80, 85, and 130 GHz for

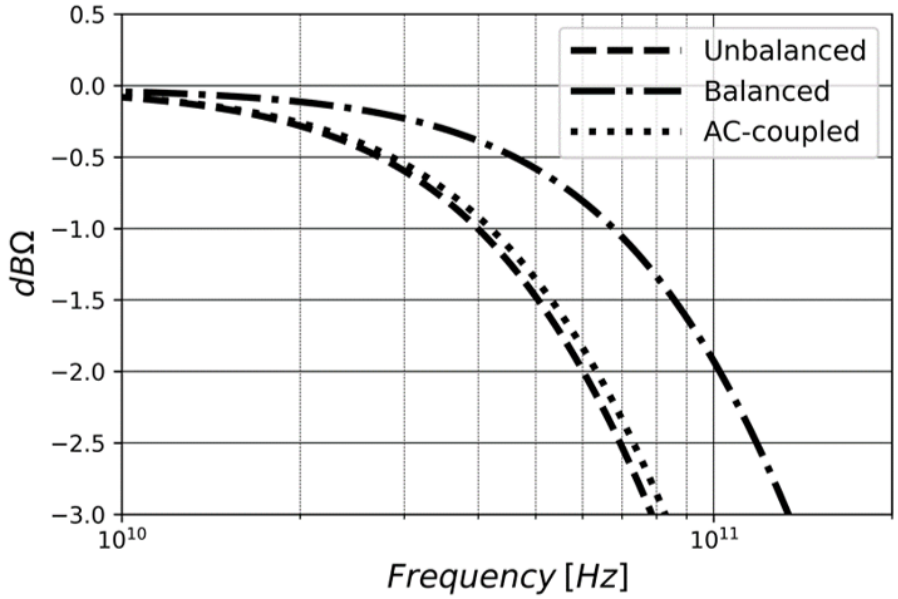

Figure 2.10: Simulated normalized frequency response of the three front-end topologies when the CHEF TIA is replaced by an ideal resistor R_{in}, which is given by $R_{in} \approx R_f/A$.

the unbalanced, AC-coupled, and balanced receivers, respectively. The balanced receiver, which has the highest BW, also has the highest GDV. The unbalanced receiver, with the lowest BW, dampens the TIA response the most, and has the lowest GDV.

2.4.3 Sensitivity

The input-referred current noise and output voltage noise spectral densities are plotted in Fig. 2.11. The input current noise is generally assumed to be approximated by a white noise component and a f^2 region.

$$\frac{I_{n,ckt}^2}{\Delta f} = \alpha_0 + \alpha_2 f^2 \tag{2.6}$$

where α_0 and α_2 are the white noise and violet noise parameters. The white noise parameter is typically due to the TIA feedback resistor thermal noise and the base shot

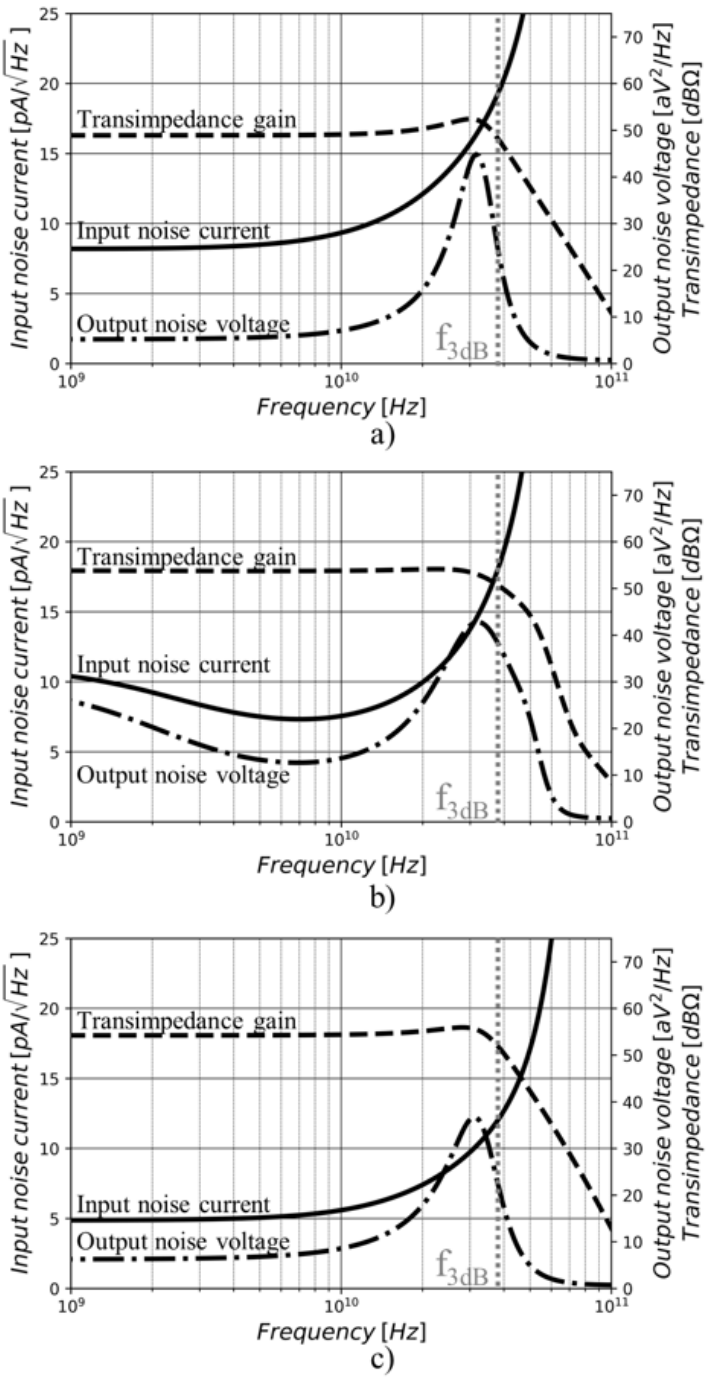

Figure 2.11: a) Balanced, b) unbalanced, and c) AC-coupled receivers simulated input-referred noise current spectral density, output noise voltage spectral density, and transimpedance.

noise contribution at the input. The violet noise contribution is related to the input device collector shot noise and the base resistance thermal noise. Both have a white spectrum and are transformed into f^2 components as they are referred back to the input and are roughly proportional to C_j^2 [19]. The DC input-referred noise level is lowest for the AC-coupled TIA and is larger for the balanced and unbalanced TIAs. The input referred noise current density in all three cases generally follows the white and violet noise power spectrum.

At low frequency, the dominant noise contributor of the unbalanced TIA is the emitter degeneration resistance of the biasing current mirror. However, it is a negligible fraction of the total integrated output noise voltage. At high frequency, the input noise current spectral density exhibits a f^2 dependence. In all variants the shape of the output voltage noise spectral densities suggests that the f^2 terms dominate the output rms noise, since most of the area under the curve is found after the f^2 terms have begun to dominate. The main noise contributor in all variants is the collector shot noise, which scales with f^2. The second most-significant contribution in both the balanced and unbalanced receivers is the R_f thermal white noise. In the AC-coupled receiver, the NPN base resistance is the secondary contributor because its input referred current noise is proportional to C_j^2, the value of which is effectively doubled with respect to ground when both PD terminals are connected to the differential inputs. Due to the asymmetry of the unbalanced TIA, the contribution of the collector shot noise on the PD-connected terminal is about twice as large as that of the other NPN, and the $R_f^{'}$ contribution is eliminated. The input-referred peak-to-peak current sensitivities (i_{sens}) for $BER = 10^{-12}$ are listed in Table 2.1. In the remainder of this chapter, i_{sens} will only refer to sensitivities for $BER = 10^{-12}$.

2.4.4 Noise Transfer Functions

The input-referred current sensitivities do not consider the impact of the noise from the power supplies, which can be significant in practical environments with limited capacitive decoupling. Fig. 2.12 shows the transfer functions of the noise from the PD supply and the CHEF TIA voltage supply of the three receiver variants. The PD supply noise transfer functions show that the balanced variant noise gain is over 20 dB lower than the AC-coupled receiver below 40 GHz, and below 60 GHz with respect to the unbalanced variant. This is because the PD supply noise couples to only one of the TIA inputs in both the unbalanced and AC-coupled variants, while it couples to both inputs in the balanced variant and is cancelled out due to common-mode rejection. The CHEF TIA supply noise gain transfer functions of the AC-coupled and balanced variants are nearly identical, and over 10 dB lower than the unbalanced variant for frequencies below 40 GHz. Given that the off-chip capacitor connected to one of the TIA inputs unbalances the differential amplifier of the unbalanced variant, noise from the supply rails are present at the outputs.

The simulated impact of the PD and TIA supply noises on the input-referred sensitivity is investigated by varying their spectral densities while assuming they are white. The supply noise is then integrated and added to the previously calculated circuit noise. It is assumed that they are uncorrelated. The resulting input-referred sensitivity currents and optical modulation amplitudes (OMA) in µW are shown in Fig. 2.13. For PD noise power spectral densities (PSD) below 3 x 10^{-14} V^2/Hz the AC-coupled variant is the most sensitive and for higher PSD, the balanced variant is more sensitive. It can be observed that the unbalanced variant is never more sensitive than the AC-coupled since their slopes are equal once the PD supply noise dominates. Similarly, for TIA supply PSD below 3 x 10^{-15} V^2/Hz the AC-coupled receiver is the most sensitive, and at higher

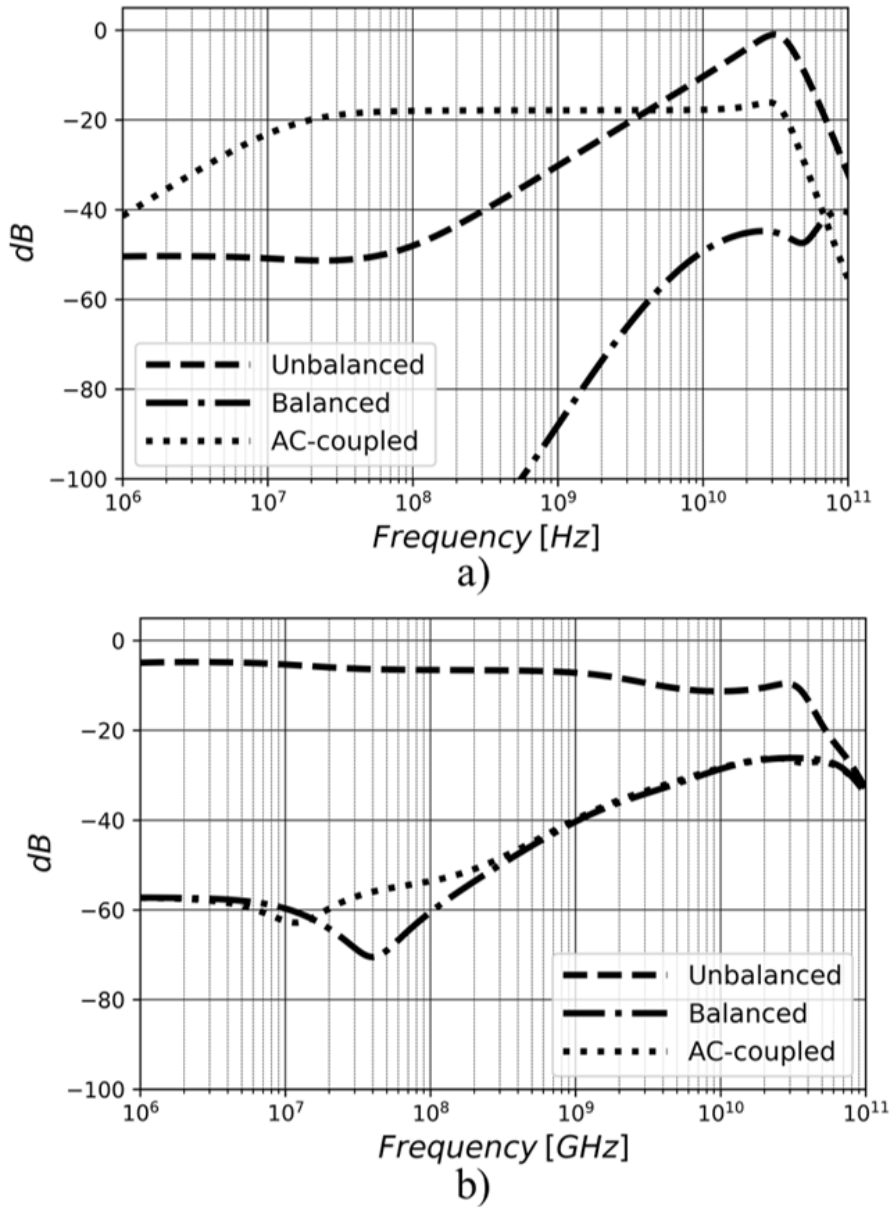

Figure 2.12: Simulated noise transfer functions for the three receiver variants of the a) PD voltage supply and b) the CHEF TIA voltage supply.

densities the balanced variant performs the best. As expected from the noise transfer functions, as TIA supply noise increases, the unbalanced and AC-coupled tend to have an equal input-referred sensitivity.

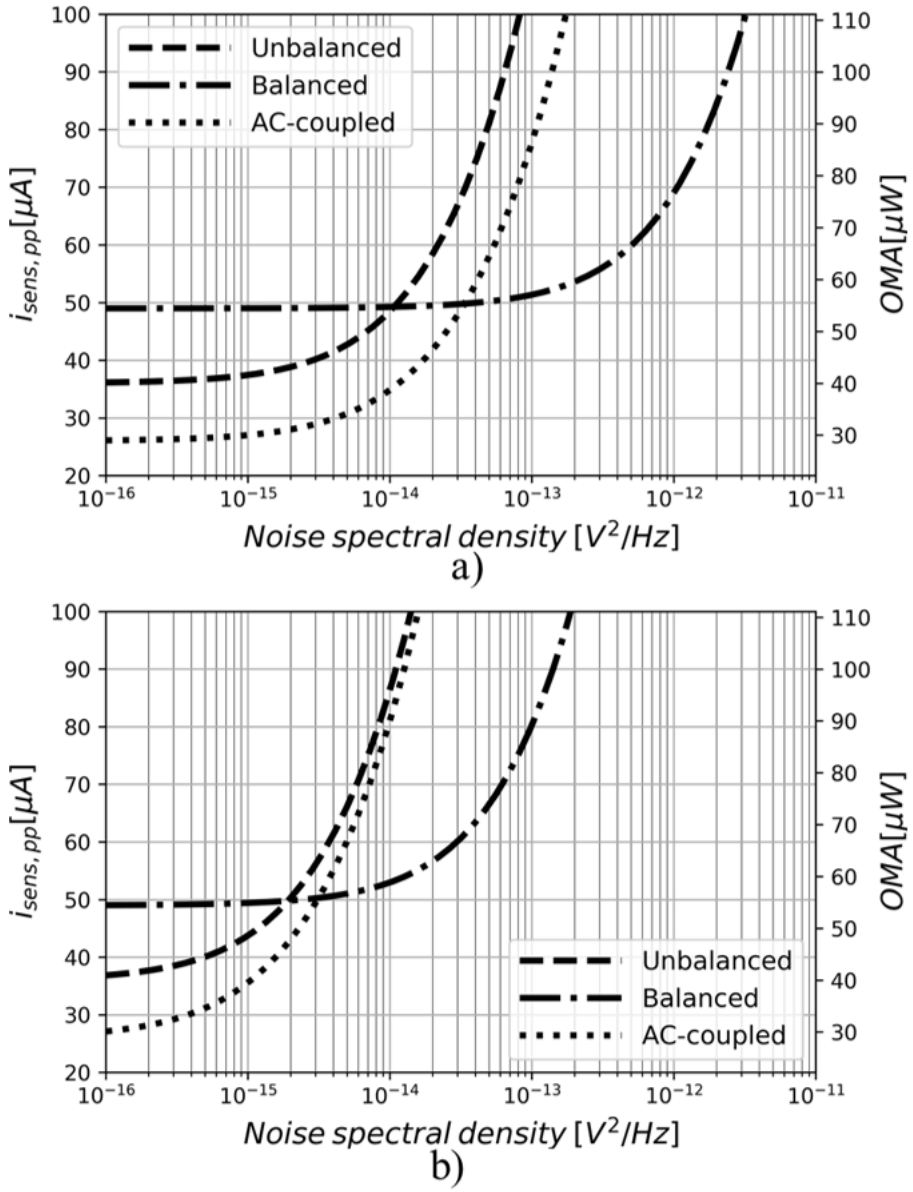

Figure 2.13: Simulated input-referred sensitivity and OMA vs a) PD supply and b) TIA VCC supply noise spectral densities, assuming both have white noise spectrums.

2.4.5 Eye-diagram Simulations

Simulated eye diagrams for an input current of 100 μA_{pp} are plotted in Fig. 2.14. In all transient simulations, including sections 2.4.6 and 2.4.7, the output DC voltage is eliminated. The greater GDV of the balanced and AC-coupled receivers translates to

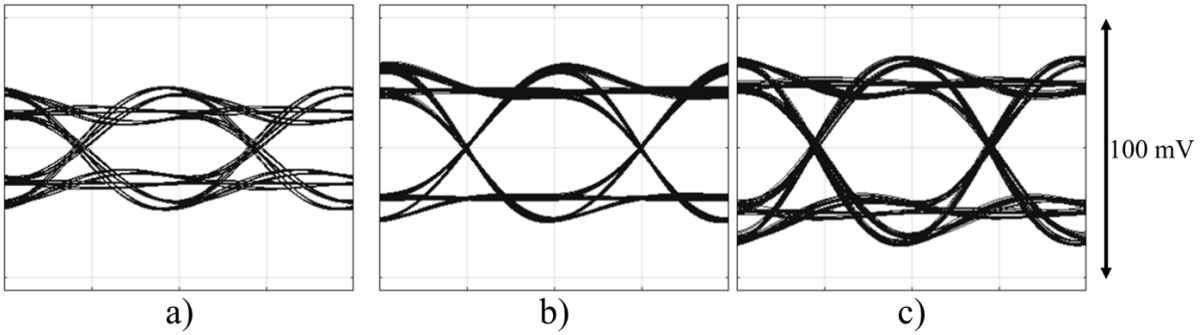

Figure 2.14: a) Balanced, b) unbalanced, and c) AC-coupled receiver 50 Gb/s simulated eye-diagrams with PD current of 100 μA_{pp} at infinite extinction ratio (ER).

jitter in the time domain. The unbalanced receiver, which has the lowest GDV, shows very sharp crossings. Given that the signal is not limited at that current input swing, the midband R_T difference among the variants results in varying eye amplitudes.

2.4.6 Dynamic Range

Transient simulations were done at various average input signal power levels in order to qualitatively compare the dynamic range of the three receiver variants. In general, nonlinear distortion does not limit the BER as a function of signal power because at high enough input power the TIA output becomes limited and thereby compressed. Instead, the increase in nonlinearities that result in a larger GDV are what increase the BER due to increased jitter in the crossings. Fig. 2.15 shows the simulated eye-diagrams for each variant at -6, -3 and 0 dBm of OMA and infinite ER. While the eye distortion is noticeable in all variants, the increase in jitter is more significant in the unbalanced and AC-coupled variants as the signal power increases.

2.4.7 DC Phocurrent Overload

The ER of the received signal can vary, e.g. the signal is emphasized at high-frequencies, and the average signal power for a given OMA is usually increased. There-

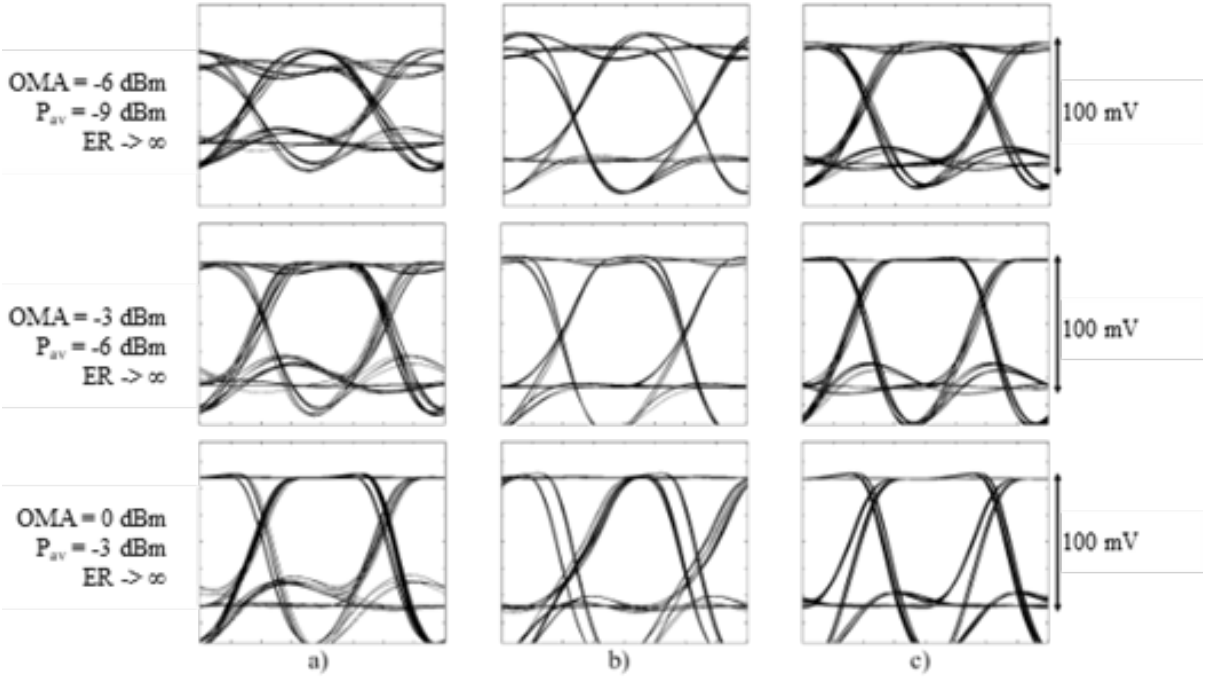

Figure 2.15: a) Balanced, b) unbalanced, and c) AC-coupled receiver 50 Gb/s simulated eye-diagrams at various input signal power levels with infinite ER.

fore, another important design characteristic is the capacity for the receiver to handle large DC currents even when these are differentially balanced. This is also important in coherent receivers, where the optical signal is mixed with a local oscillator (LO) to increase the signal power. As the LO power increases relative to that of the optical signal, the DC photocurrent for a given current swing also rises [23]. Fig. 2.16 contains output eye-diagrams for the three receivers at varying ERs at a fixed OMA of -6 dBm. This corresponds to 227 μA_{pp}. The first and second rows correspond to infinite ER, and ER = 3, respectively. In all the receiver variants, there is no notable difference between the two DC operating points. However, as the ER is reduced to 1.36, which is represented on the third row, the balanced variant shows a significant increase in jitter. An ER of 1.36 is chosen since it results from a LO and signal power ratio of 16 dB, which is feasible in a coherent receiver. The balanced variant shows a slight increase in ISI (intersymbol interference) in comparison with the eye at ER = 3. The AC-coupled variant performance

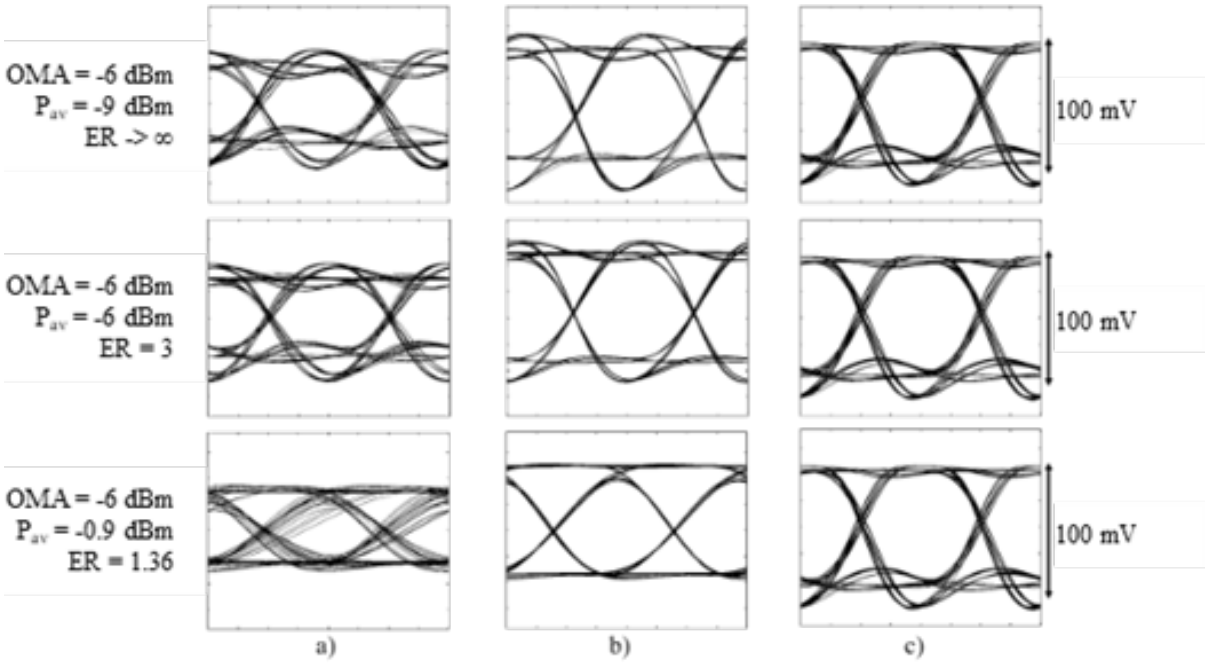

Figure 2.16: a) Balanced, b) unbalanced, and c) AC-coupled receiver 50 Gb/s simulated eye-diagrams at a fixed OMA and various ERs.

remains unchanged, because no DC current passes into the input of the TIA. However, this simulation uses a small-signal PD model, and thus does not capture the increased drop across the R_1 resistors due to DC photocurrent. This reduces the PD reverse bias voltage and may decrease the BW of the PD.

Table 2.1 contains a summary of the performance characteristics discussed in section 2.4.

2.5 PAM4 Simulations

While NRZ links typically employ limiting TIAs, PAM4 signaling requires the TIA operation to be linear. The optical receivers described in this work do not have limiting amplifiers and are expected to have a sufficiently large linear range for PAM4 operation. The total harmonic distortion (THD) of the three variants is shown in Fig. 2.17. The

	Balanced Differential	Unbalanced Differential	AC-coupled
Midband transimpedance (R_T) [dBΩ]	48.9	53.9	54.1
3dB BW [GHz]	40.3	37.6	38.6
DC cutoff [MHz]	0	0	20
GDV [ps][a]	17	6	12
BER = 10^{-12} Sensitivity (i_{sens})[μApp] / OMA [dBm][b]	49 / -12.7	36 / -14	26 / -15.4
Input-referred current noise density [pA/Hz$^{1/2}$]	17.5	11.6	9.6
Output DC voltage offset elimination	Requires DCLR and DCOC	Requires DCLR and DCOC	Only requires DCOC
Power (P_{DC}) [mW]	53.8	53.8	53.8
Power efficiency at 50 Gb/s [pJ/bit]	1.08	1.08	1.08

[a]The GDV is evaluated from 1 GHz to the 3dB BW
[b]The photodiode responsivity is 0.9 A/W and infinite ER

Table 2.1: Receiver Variants Performance Comparison

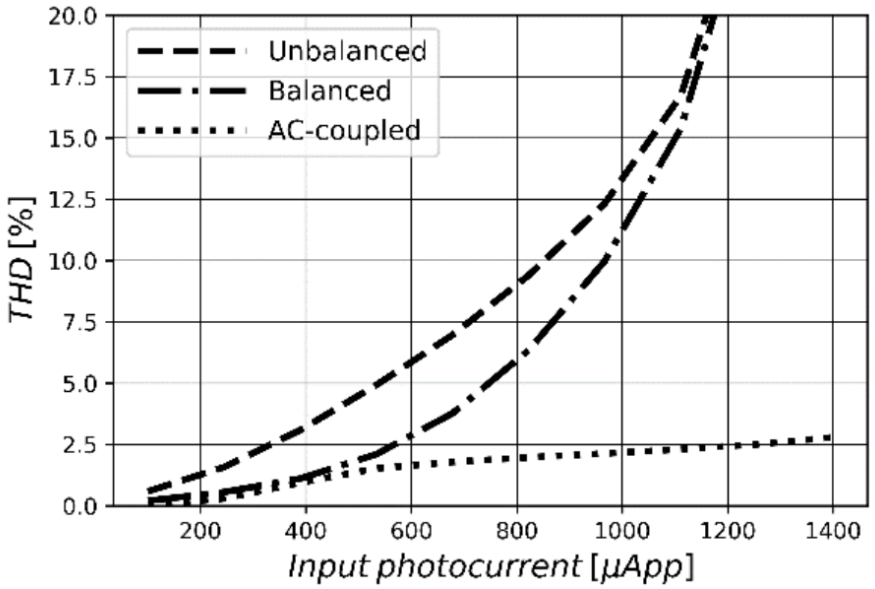

Figure 2.17: THD as a function of input photocurrent swing for the three receiver variants.

input power was swept by varying the peak-to-peak amplitude of a 1 GHz sinusoidal input. The balanced receiver THD is about half that of the unbalanced receiver's up to 800 μA_{pp}, and they converge above 1.1 mA_{pp}. The AC-coupled receiver performs significantly better with a THD below 3% up to 1.4 mA_{pp}. This is due to a reduction of the second-order harmonic by approximately 24 dB with respect to the unbalanced receiver.

Fig. 2.18 shows the TIA output PAM4 eye diagrams at 25 Gbaud (50 Gb/s) for the three receiver variants. The decrease in symbol rate from 50 Gbaud OOK to 25 Gbaud

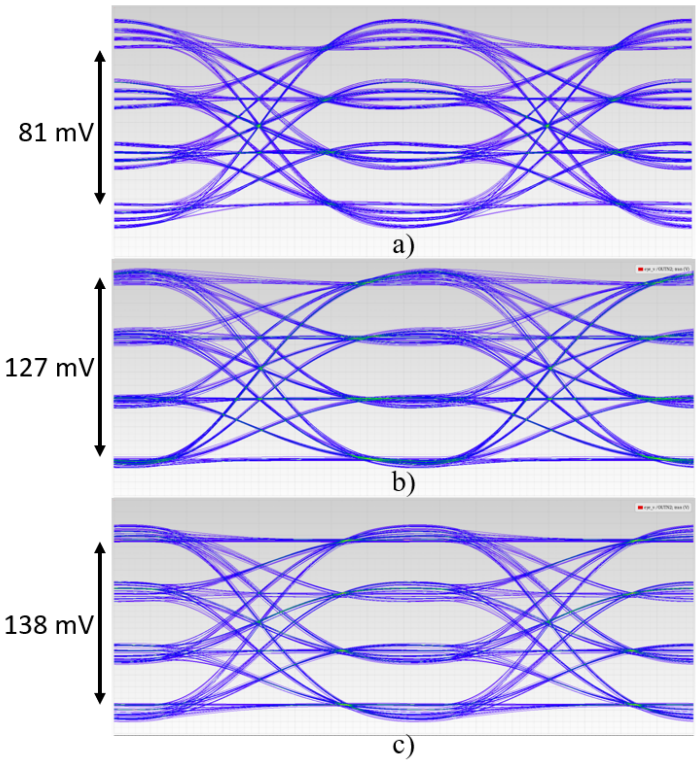

Figure 2.18: Simulated 25 Gbaud PAM4 eye diagrams for the a) balanced, b) unbalanced, and c) AC-coupled receiver variants for a TIA input current of 150 µApp. This current swing is above the BER = 10-12 sensitivity of all the variants.

PAM4 results in a lower TIA target BW to approximately 20 GHz. To decrease the transimpedance BW, the TIA supply and biases are lowered with respect to those shown

in Fig. 2.6 from 3.6 V to 3 V, and 11.5 mA to 4.6 mA, respectively. The output buffer bias current is increased to 8.4 mA in order to increase the output voltage swing. These bias conditions result in an improved power efficiency of 0.73 pJ/bit for all three variants. The sensitivity is also improved by the BW reduction. The simulated sensitivity currents for BER = 10^{-12} are 48 μA_{pp}, 57 μA_{pp}, and 83 μA_{pp} for the balanced, unbalanced, and AC-coupled variants, respectively.

2.6 Experimental Results

2.6.1 Optical Receiver Assembly

The receivers were implemented on the IHP SG25H4_EPIC process that combines BiCMOS with silicon photonic devices. The total chip dimensions, limited by the bond pad frame, are less than 1 mm x 1 mm, and the bondpad pitch is 150 µm. The PD and active electronics occupy 130 µm x 120 µm. The AC-coupled receiver variant is shown in Fig. 2.19. The ICs of the other two variants have the same padframe. Each receiver was wire-bonded to custom-built PCBs, as shown in Fig. 2.20. Mini SMP connectors rated for up to 65 GHz were used for the TIA outputs and broadband 1.2 nF capacitors were added to each DC power supply. Additionally, on chip bypassing capacitors provide PD supply low-pass filtering above 240 MHz in the balanced and unbalanced receivers.

2.6.2 Bias conditions

All the variants were designed for the same 3.6V VCC supply and the bias currents detailed in Fig. 2.6. However, it is predicted that the deviation of the Cherry-Hooper resistances due to variations in the fabrication process resulted in a change in the optimal VCC voltage and current of the unbalanced variant's CHEF TIA to 4 V and 10.3

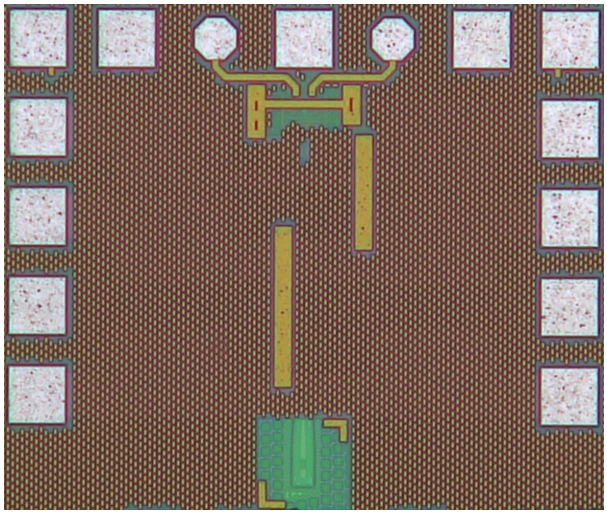

Figure 2.19: Photograph of the AC-coupled variant. The IC area is less than 1 x 1 mm and is bondpad-limited. The bondpad pitch is 150 µm. The PD and active electronics occupy 130 µm x 120 µm. The two octagonal pads are the RF outputs. The balanced and unbalanced variants have the same IC padframe.

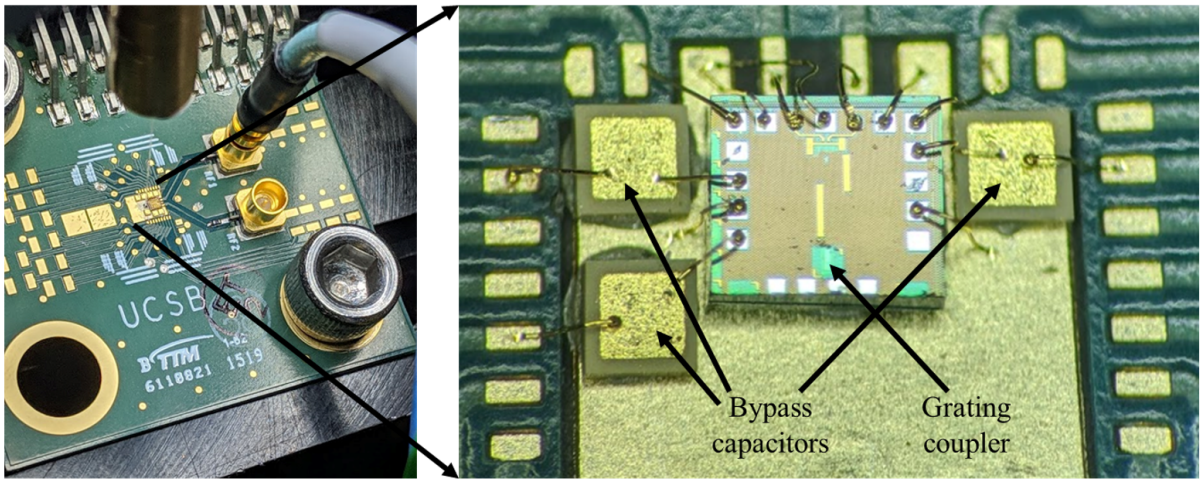

Figure 2.20: Optical receiver assembly. The optical fiber probe and RF connectors are shown on the left-hand picture. On the right, the wire bonded assembly is shown. Each of the three receiver variants was assembled as shown.

mA. Similarly, since the bias currents are set by current mirrors that are sensitive to resistor variations, the output buffer bias currents varied from 3.6 to 5 mA, which lead to variations among the output voltage swings. In the balanced and unbalanced variants, the bias across the PD was 4V. In the AC-coupled variant the bias across the two R_1

resistors and the PD was 5.3 V. This corresponds to 4 V across the photodiode for a photocurrent of 325 µA, due to the drop across the R1 resistors. The photodiode biases were determined by increasing the voltage until there was no noticeable improvement in sensitivity. In the balanced and unbalanced variants DCLR was implemented off-chip by measuring the PD current and sourcing an equal current to the other differential input.

2.6.3 Measurements

Fig. 2.21 shows setup for eye-diagram and BER measurements. The optical NRZ sig-

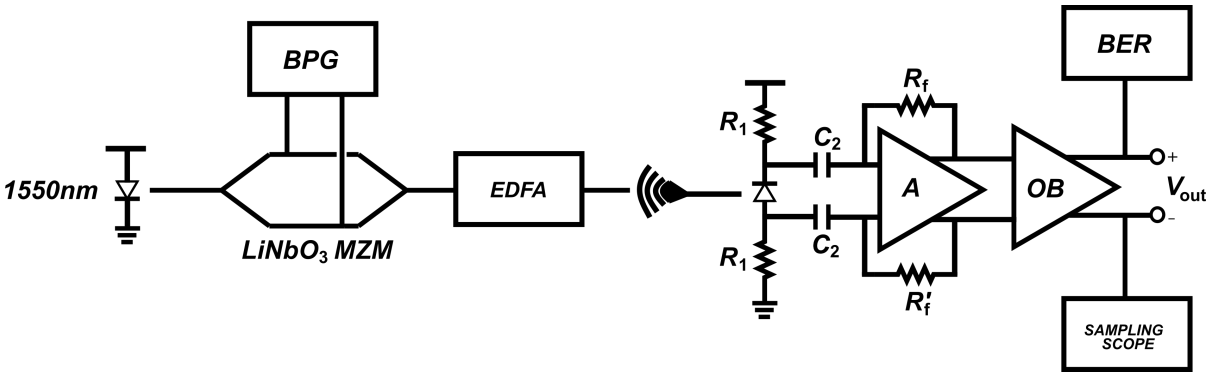

Figure 2.21: BER vs power measurement setup for the AC-coupled variant. The setup is the same for the other two variants.

nal is generated by modulating a 1550 nm laser with a $LiNbO_3$ Mach-Zehnder modulator (MZM).

The signal is then amplified and coupled to the DUT and the differential outputs of the TIA are connected to the bit error-rate tester (BER) and a sampling oscilloscope. The bit pattern generator (BPG) contains multiple independent channels with adjustable skew and amplitude, each of which has non-inverted and inverted outputs. The MZM has two differential high-frequency inputs. This allows for two methods of driving it. In the first (without equalization), the MZM inputs are connected to the non-inverted and inverted outputs of a single BPG channel. In the second (with equalization), the MZM

inputs are connected to the non-inverted outputs of two separate BPG channels with different amplitudes and a time skew between them to produce a feed forward equalizer (FFE), as described in [24].

A script was developed to measure BER as a function of OMA which runs two attenuation sweeps for each bitrate. The first sweep is used to find the optimal bit sampling point, and the second to find the BER at varying OMAs at that fixed sampling point. Each BER value was evaluated until at least 5 errors were found or the time corresponding to 5 errors at BER = 10^{-12} passed. In the balanced and unbalanced variants, the photocurrent is measured at each attenuation point and an equal current is fed into the other TIA input to emulate DCLR control loops. A PRBS31 run length was used in the balanced and unbalanced receivers, and for the AC-coupled variant, due to the 20 MHz DC-cutoff, the run length was reduced to PRBS7. For measurements without TX equalization, the MZM was biased at quadrature and the BPG signal amplitude was adjusted to obtain a V_π peak-to-peak swing. The data for all three receivers is shown in Fig. 2.22. The ER was measured to be 40, and therefore $OMA \approx P_{av} + 3dB$. The measured OMA values for BER = 10^{-12} are -9 dBm, -8 dBm, and -9 dBm, and hence the i_{sens} are 114 μA_{pp}, 143 μA_{pp}, 114 μA_{pp}, for the balanced, unbalanced and AC-coupled variants, respectively. By referring to Fig. 2.13 and the simulated i_{sens} values in Table 2.1, we deduce that the VPD and VCC supply noise contribute significantly to the input-referred sensitivity in all three cases. The balanced receiver's measured sensitivity is 3.7 dB higher than the simulated one. This difference is 6 dB and 6.4 dB for the unbalanced and AC-coupled receivers, which is consistent with the fact that the balanced variant is the most tolerant to supply noise. At 40 Gb/s only the balanced variant achieves BER < 10^{-12}, since the other two variants saturate at -2 dBm of OMA. The overload simulations shown in section 2.4 show that the balanced variant has a slightly better performance at 0 dBm. This may explain its higher dynamic range.

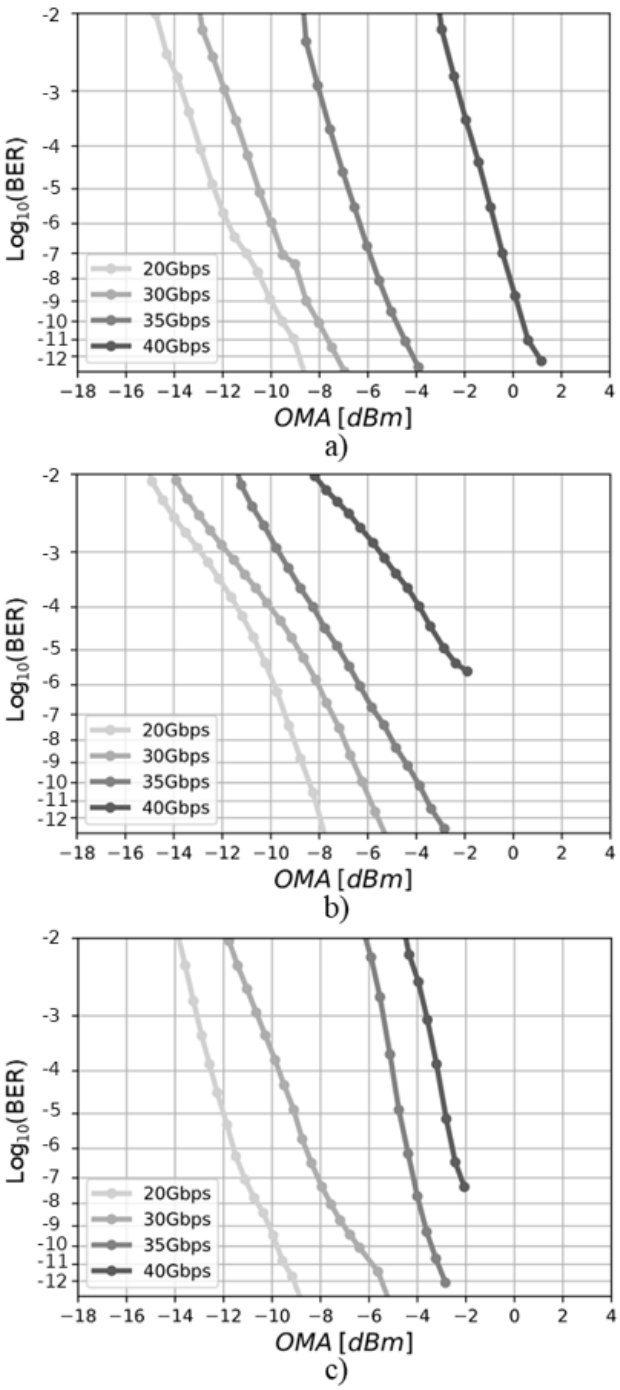

Figure 2.22: BER vs Pav for at various data rates without TX pre-emphasis for the a) balanced, b) unbalanced, and c) AC-coupled receiver variants.

For the BER vs P_{av} measurements with TX equalization, the MZM bias was set to quadrature, one input (main) amplitude was maintained as in the no TX equalization

configuration, and the amplitude and skew of the other input signal (tap) was adjusted to optimize the BER vs P_{av} performance. The optimal tap amplitude was found to be half of the main amplitude. This resulted in $ER \approx 3$, and so $OMA \approx P_{av}$. The optimal skew was found to be 0.5 UI. The same test script was used to obtain the data, which is presented in Fig. 2.23. At 20 Gb/s the BER response is approximately the same as without TX equalization because the power penalty due to ISI is expected to be low. The 30 Gb/s BER curve overlaps with the 20 Gb/s curve. This indicates that the total receiver BW is enhanced and that a minimum ISI sensitivity penalty is achieved. At 35 Gb/s the BER curves shift between 3 and 5 dB towards lower OMAs is observed. The increased BW now makes it possible to measure the BER at 45 and 50 Gb/s. The balanced and unbalanced receivers saturate at lower OMAs in comparison with the unequalized measurements. This agrees with section 2.4.7, where it was shown that these variants are less tolerant to high DC currents. This is because with TX equalization the received Pav for a given OMA is 3 dB higher than without equalization. A BER below 10^{-10} at 50 Gb/s was achieved for the AC-coupled variant.

Transmitter (TX) eye-diagrams are shown in Fig. 2.24. At 50 Gb/s without equalization, it can be observed that there is no eye closure at the TX output as the optical link is not limited by the MZM BW, and instead by the packaged optical receiver BW. The TIA output eye-diagrams are taken at a signal power between -5 and -3 dBm and graphed in Fig. 2.25. At 40 Gb/s without TX equalization, the unbalanced and AC-coupled eye-diagrams appear overloaded due to high current swing. At 50 Gb/s without equalization, the balanced variant performs the best while all variants have severe eye closure. At the same data rate with equalization, the eyes are similar as expected from the BER as a function of P_{av}. However, as the signal power is increased, the balanced and unbalanced receivers deteriorate before the AC-coupled variant, which can be attributed to a better tolerance to a high DC photocurrent.

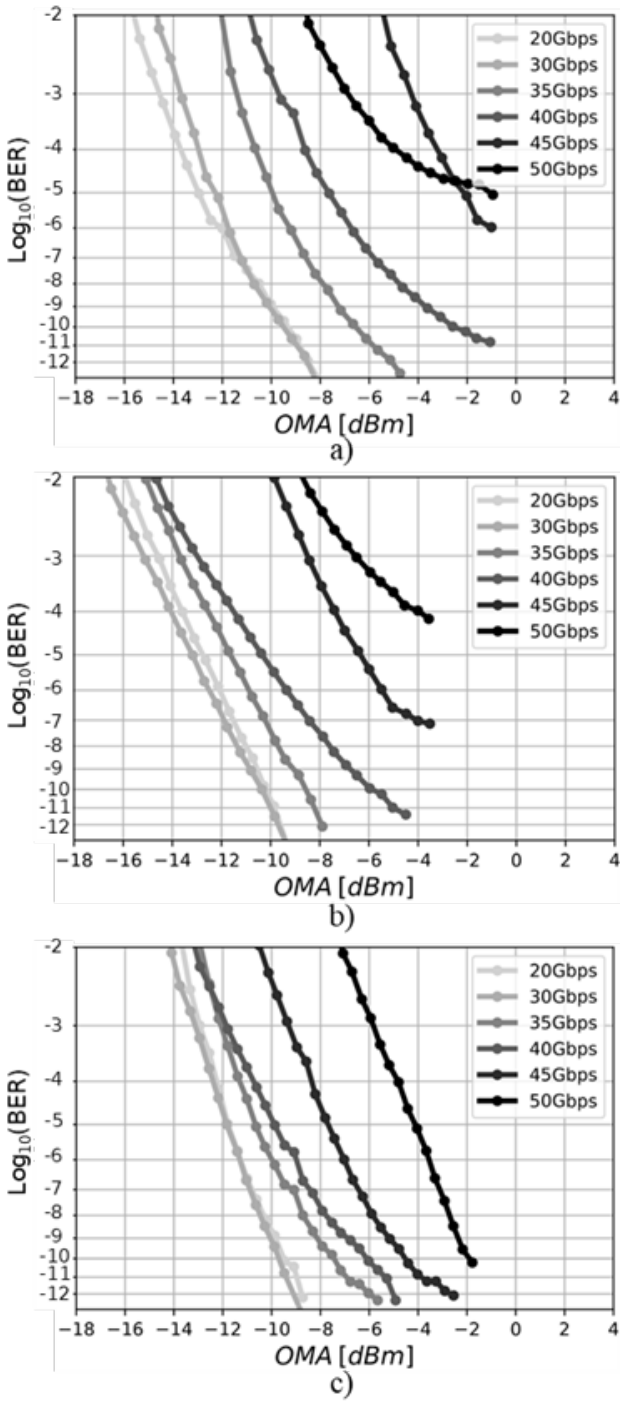

Figure 2.23: BER vs Pav for at various data rates with TX pre-emphasis for the a) balanced, b) unbalanced, and c) AC-coupled receiver variants.

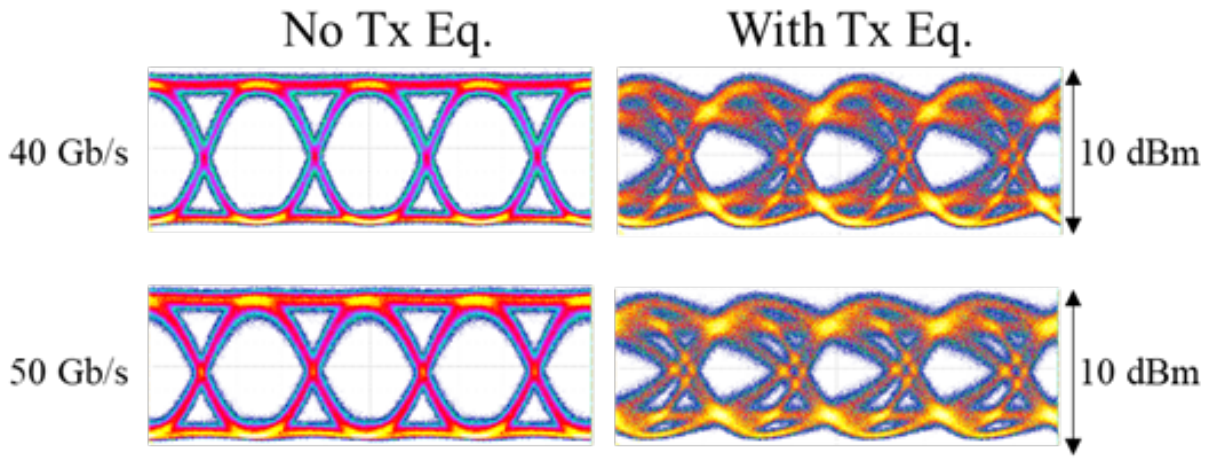

Figure 2.24: Measured TX eye-diagrams taken at the output of the MZM using an optical module on the sampling oscilloscope.

The receivers nominally consume 54 mW of power, which corresponds to 1.08 pJ/bit at 50 Gb/s. Simulations show that this figure would increase for a higher required output voltage swing, e.g. to 1.62 pJ/bit for a single-ended output of 150 mV_{pp}, since the output stage would require 3 V and a tail current of 6 mA. A comparison of the three receiver variants described in this chapter with state-of-the-art optical receivers is shown in Table 2.2.

2.7 Conclusion

A comparison of the three most common optical receiver topologies employing differential TIAs was presented. This analysis considered the tradeoffs in midband RT, BW, GDV, sensitivity, tolerance to supply noise, dynamic range, DC current overload, and output DC voltage cancellation.

Also, the case for the monolithic integration of optical receivers was made by showing the improvement of the transimpedance limit due to the elimination of packaging parasitics. The three receiver variants, which were implemented monolithically in the

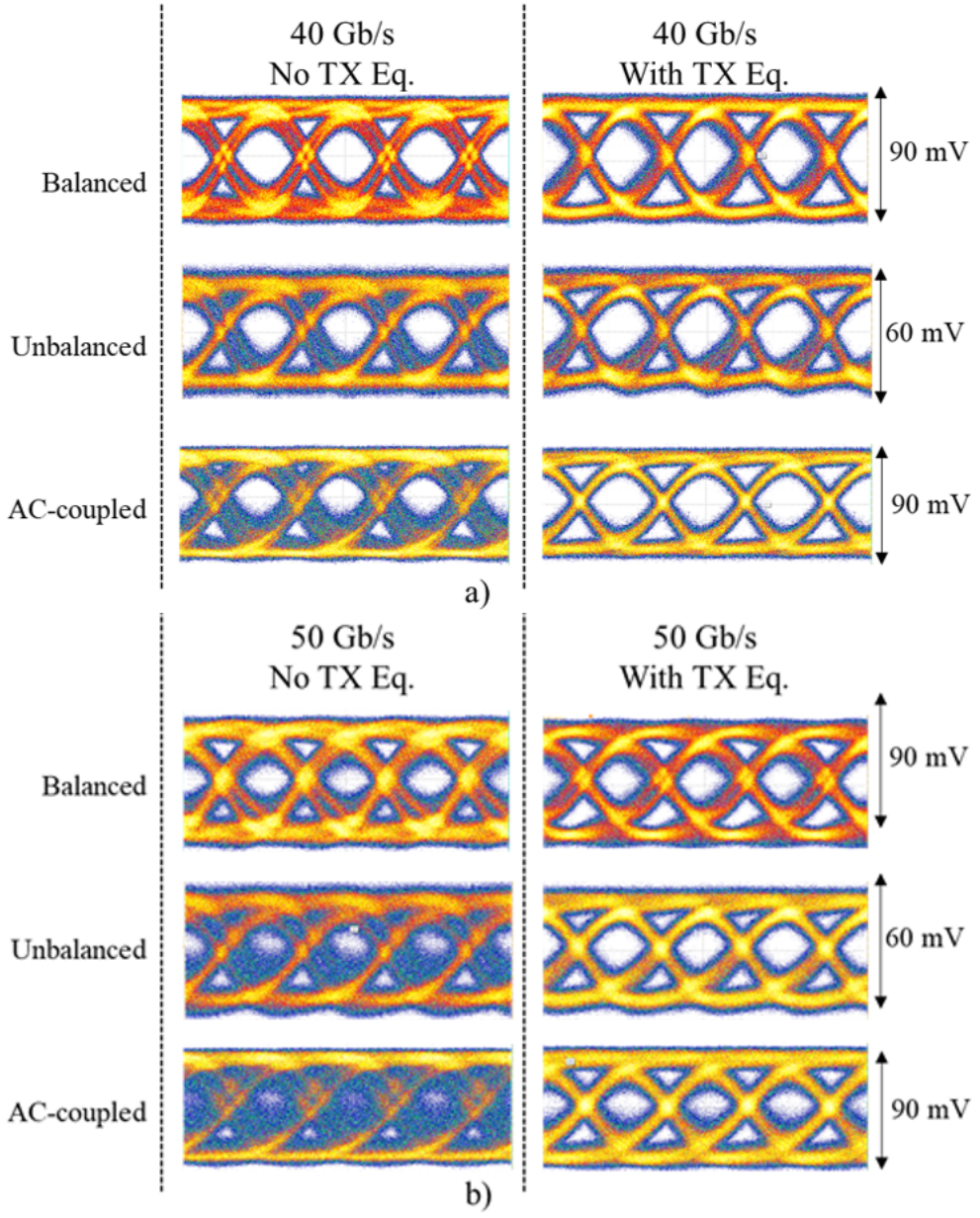

Figure 2.25: Measured TIA output eye-diagrams at a) 40 Gb/s and b) 50 Gb/s taken between -5 and -3 dBm of average signal power.

SG25H4_EPIC IHP BiCMOS process, were packaged and measured. BER vs P_{av} measurement data was presented, and eye-diagrams were shown.

In summary, the optimal receiver architecture depends on design priorities and the application setting. In our three variants the PD BW is much higher than the required

BW for the target data rate of 50 Gb/s, so the choice of architecture does not determine the total receiver BW. However, the midband transimpedance does depend heavily on the type of frontend. The unbalanced and AC-coupled variants have roughly twice the R_T as the balanced receiver. This can save power by reducing the amount of limiting amplifier stages required to obtain a specified output voltage swing. The input-referred sensitivity also varies significantly among the different variants. In low-noise environments the AC-coupled variant is more sensitive. However, in an environment where the PD and TIA supplies are noisy the balanced receiver is a better choice. The combined power penalties from ISI and a high input-referred sensitivity may lead to large OMA and DC photocurrents. Therefore, under conditions where the BW requirements are very stringent and/or the environment noise dominates, the dynamic range and DC power handling of the receiver is critical. The balanced receiver performs best at high OMAs, as evinced by the no TX eq. BER measurements. The BER measurements with TX eq. showed that the AC-coupled receiver is superior at high DC photocurrents, which may eliminate the need for DC current sink control. An additional benefit of the AC-coupled variant that results in reduced circuit complexity is that DCLR control is not required, which can save power. The main disadvantage of the AC-coupled variant is the DC-cutoff, which limits the maximum run-length it can tolerate.

Reference	**Technology**	**Integration Level**	**OE BW (GHz)**	**Data Rate (Gbaud)**	**R_T (dBΩ)**	**PD Resp. (A/W)**	**IRNC (μA_{rms})**	**IRNCD ($pA/\sqrt{Hz}$)**	**P_{DC} (mW)**	**Energy efficiency (pJ/bit)**
This work[a]	**250nm SiGe BiCMOS**	**Monolithic**	**37.6**	**50**	**53.9**	**0.9**	**3.5**	**17.5**	**54**	**1.08**
This work[b]	**250nm SiGe BiCMOS**	**Monolithic**	**37.6**	**50**	**53.9**	**0.9**	**2.57**	**11.6**	**54**	**1.08**
This work[c]	**250nm SiGe BiCMOS**	**Monolithic**	**38.6**	**50**	**54.1**	**0.9**	**1.86**	**9.6**	**54**	**1.08**
[25]	250nm SiGe BiCMOS	Monolithic	34	56	66	0.7	2.08	11.3	205	3.66
[26]	250nm SiGe BiCMOS	Monolithic	31	40	65	0.8	5	28.1	275	6.88
[27]	55nm SiGe BiCMOS	Hybrid	N/A	56	72.5	0.8	2.2	N/A	170	3.04
[28]	130nm SiGe BiCMOS	Hybrid	28	40	80	0.75	N/A	14	77	1.93
[29]	130nm SiGe BiCMOS	Hybrid	27	34	73	N/A	N/A	20	313	2.30
[30]	130nm SiGe BiCMOS	Hybrid	26	32	74	N/A	N/A	12.2	218	4.36
[31]	40nm CMOS	Hybrid	N/A	28	68	N/A	2.56	N/A	120	2.14
[32]	28nm CMOS	Hybrid	N/A	53	74	0.55	N/A	N/A	34.6	0.65
[33]	40nm CMOS	Hybrid	N/A	25	96	N/A	2.41	N/A	254	10.16
[34]	14nm Fin-FET	Hybrid	N/A	32	76.9	0.52	0.83	N/A	45	1.4

Table 2.2: Performance Comparison with State-of-the-Art Optical Receivers

[a]Balanced variant. [b]Unbalanced variant. [c]AC-coupled variant. The noise current values corresponding to this work are from simulations.

Chapter 3

50 GBaud QPSK 0.98 pJ/bit Receiver in 45 nm CMOS and 90 nm Silicon Photonics

3.1 Introduction

There is currently an increasing demand for scalable power-efficient intra-datacenter links. O-band coherent detection has important benefits for use in <2 km optical interconnects. Coherent detection results in higher link margin than the IMDD schemes in use today. This increase in link margin allows for more power efficient network architectures, such as those that utilize optical switching[35]. A key advantage of O-band is that the chromatic dispersion minimum of commercial single-mode fiber is located near 1310 nm, which relaxes DSP requirements.

The energy efficiency of coherent links to be used within the data center will depend heavily on the receiver electronics. Recently, a 56 GBaud monolithic O-band SiGe BiCMOS receiver with a power consumption of 485 mW has been reported[36]. Other

relevant work includes a 34 GBaud DP-QPSK receiver consisting of a SiGe BiCMOS EIC and a SiP PIC with a power consumption of 313 mW per channel[29]. It has been estimated that the front-end transimpedance amplifier (TIA) and limiting amplifiers (LA) implemented in a SiGe BiCMOS, with an assumed combined power consumption of 410 mW, account for >40% of the total power in analog coherent intra-datacenter links that employ silicon photonics. This figure increases to >50% when indium-phosphide optics are utilized[4]. CMOS-based receiver electronics consume significantly less power than those implemented in SiGe BiCMOS, and thus can be a suitable alternative. The recent release of the GlobalFoundries (GF) 45CLO fabrication process demonstrates an industry trend towards monolithic integration of silicon photonics devices with CMOS transistors targeting low-cost, mass-production, and high performance optical transceivers[37], for which low-power receiver topologies will be required.

In this chapter, we first present a single-polarization O-band QPSK receiver consisting of an electronic integrated circuit (EIC) fabricated in the GF 45RFSOI 45 nm CMOS process and a photonic integrated circuit (PIC) fabricated in the GF 9WG process. Experimental results demonstrate the operation of the receiver at up to 50 GBaud. We then describe the phase-frequency detector (PFD) and loop-filter OpAmp to be used in a QPSK Costas Loop analog optical coherent receiver.

3.2 Coherent Receiver Data Path

3.2.1 Receiver Design

Fig. 3.1 shows a block diagram of the data path of an optical QPSK Costas loop receiver designed for analog coherent intra-datacenter links[35]. The focus of this section, denoted by the dashed area, is the design and characterization of the electronics in the

QPSK data signal path and their integration with the PIC.

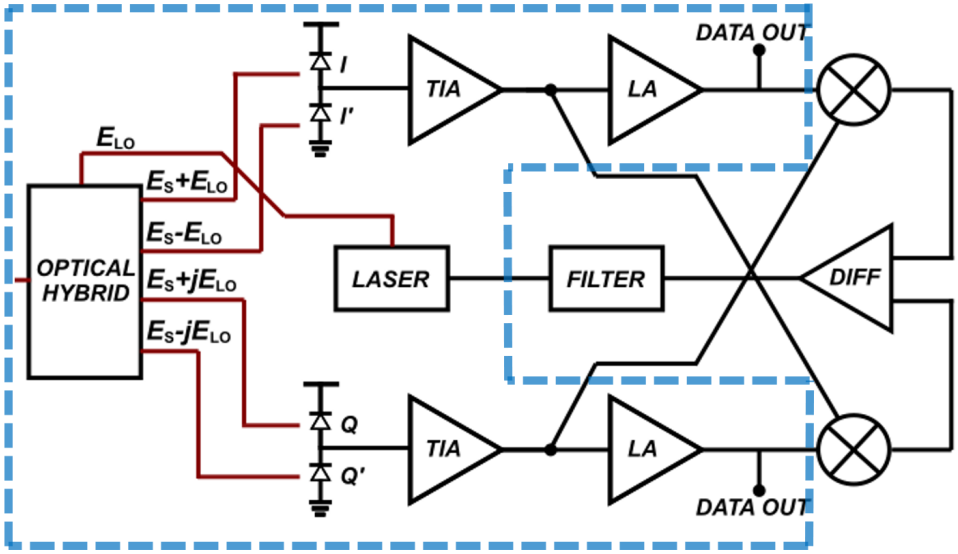

Figure 3.1: Optical QPSK Costas-loop OPLL. The dashed area denotes the work presented in section 3.2.

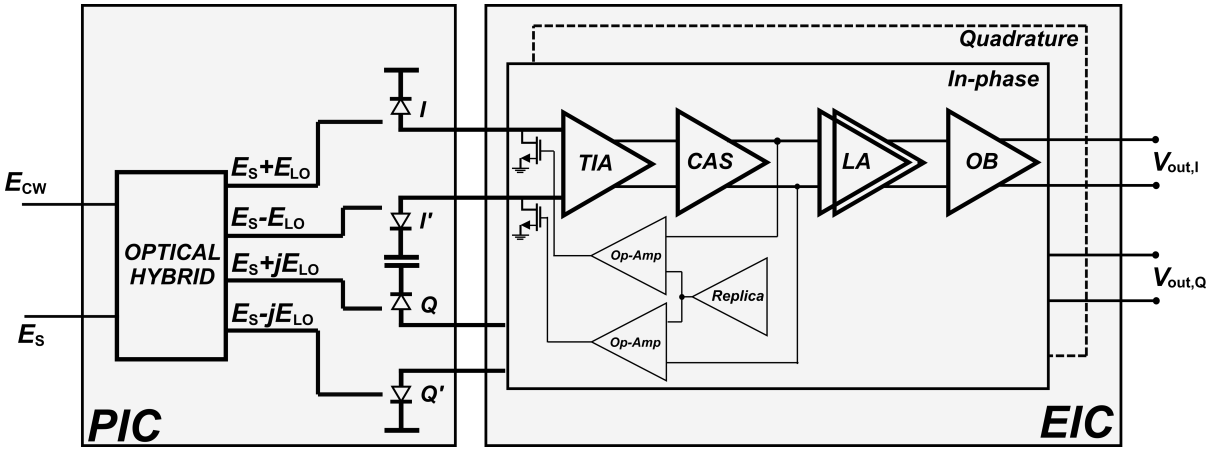

Figure 3.2: Optical receiver block diagram. The PIC consists of an optical hybrid and 4 photodiodes. The photodiode anodes are connected via wirebonds to the TIA inputs of the EIC.

A block diagram of the PIC and the EIC is shown in Fig. 3.2. The optical hybrid receives a CW laser signal (E_{LO}) and a QPSK modulated signal (E_S) and generates the four signals corresponding to the desired vectorial additions of the two input optical fields, which are routed to two pairs of photodiodes (PD), one for the in-phase (I) channel and

the other for the quadrature channel (Q). The electronics consist of a TIA, a cascode amplifier (CAS), a cascade of LAs, and an output buffer (OB). A slow loop based on a replica TIA and Op-Amps is used for DC-offset compensation (DCOC) and to sink any excess DC photocurrent.

Fig. 3.3 shows the schematic of the receiver TIA and cascode amplifiers. Connected to each PD there is an inverter shunt-feedback TIA. The inverter topology combines both NMOS and PMOS transconductances, resulting in high gain at low power consumption[38, 39] and the pseudodifferential configuration saves power by minimizing the voltage headroom. At the TIA output, a cascode amplifier is used to raise the common-mode voltage to the required value for the subsequent source-coupled limiting amplifiers.

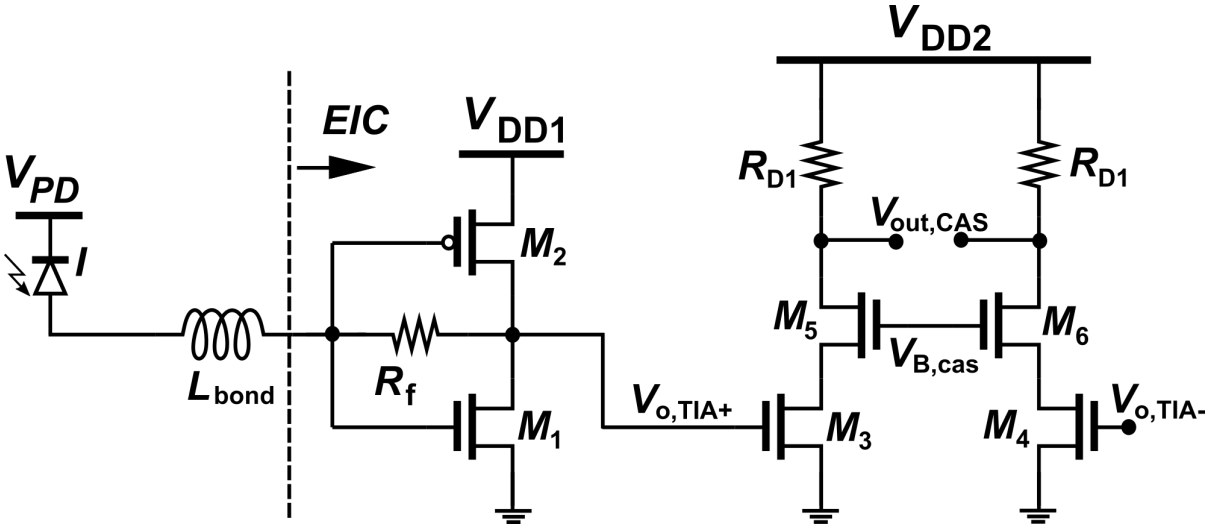

Figure 3.3: Schematic of the receiver TIA and cascode amplifiers.

Source-coupled amplifiers were utilized for the LA and OB stages to provide common-mode rejection. The LA chain consists of six cascaded amplifiers of increasing transistor widths to minimize the loading between stages. The schematic of the LA and OB stages, depicted in Fig. 3.4, shows only one of the LA stages. R_S and varactor C_S provide tunable equalization. The 50 Ω OB has shunt inductive peaking to compensate for the

output channel loss.

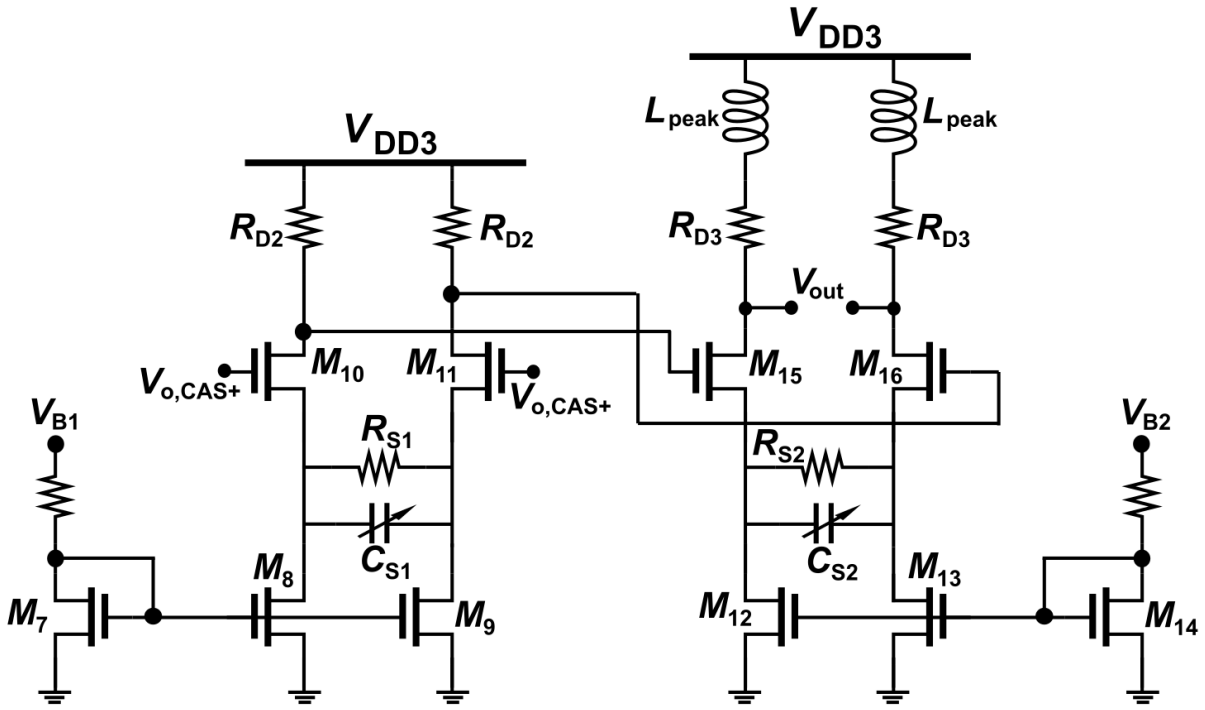

Figure 3.4: Schematic of the source-coupled limiting amplifiers and output buffer.

The simulated post-layout 3 dB BW assuming a 40 GHz PD BW, and including wirebonds and bondpad capacitances, is 23 GHz. The simulated midband transimpedance is 55 dBΩ.

3.2.2 Experimental results

The measured power consumption of the EIC including the OB is 98 mW, or 0.98 pJ/bit for 50 GBaud QPSK transmission. If the OB is omitted, in case a 50 Ω output is not required, the power is reduced to 77 mW, or 0.77 pJ/bit. The measured output noise of the EIC is 3 mV rms, the midband transimpedance is 477 Ω, and the calculated input-referred noise is 6.3 μA rms. The EIC was initially measured electrically by driving it with a bit-pattern generator (BPG) at a voltage swing equivalent to 136 μApp. The

resulting eye diagrams with a voltage swing of 65 mVpp at 40 Gbps and 50 Gbps are shown in Fig. 3.5.

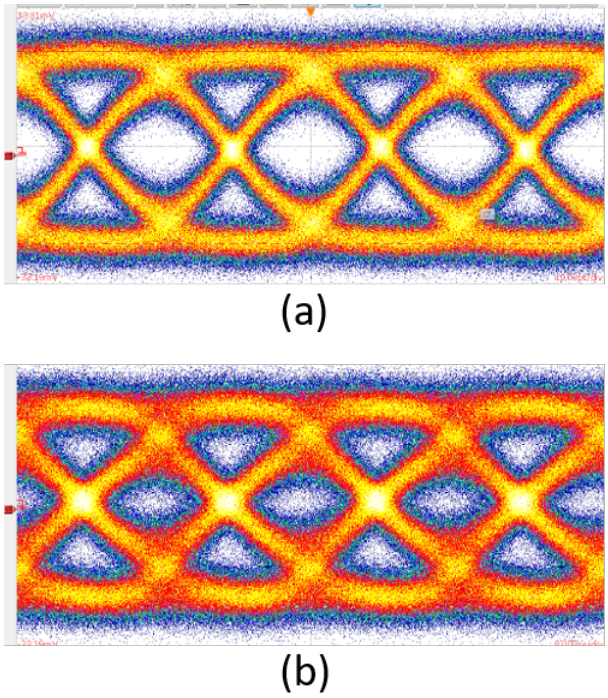

Figure 3.5: Electrical single-ended eye-diagrams at (a) 40 Gbps and (b) 50 Gbps with an input voltage swing equivalent to 136 μApp. The output voltage swing is 65 mVpp.

A photograph of the receiver IC is shown in Fig. 3.6. The EIC dimensions are 1.88 mm x 1.28 mm. Fig. 3.7 shows the receiver assembly on a PCB. and the PIC dimensions are 6 mm x 1.1 mm. The PIC-to-EIC and EIC-to-PCB wirebonds are approximately 200 μm and 750 μm, respectively. Off-chip 1.2 nF bypassing capacitors were added to the PD and EIC supplies. Mini SMP RF connectors are used to measure the two differential data outputs.

Fig. 3.8 shows the self-homodyne test setup used. An EXFO T100S-HP-O external cavity laser (ECL) set to 1310 nm and 13 dBm of power is connected to a 3 dB coupler. One coupler output is connected to an iXblue MXIQER-LN-30 IQ-MZM. Two channels of an SHF 12104A BPG are amplified and used to drive the IQ-MZM to generate the QPSK

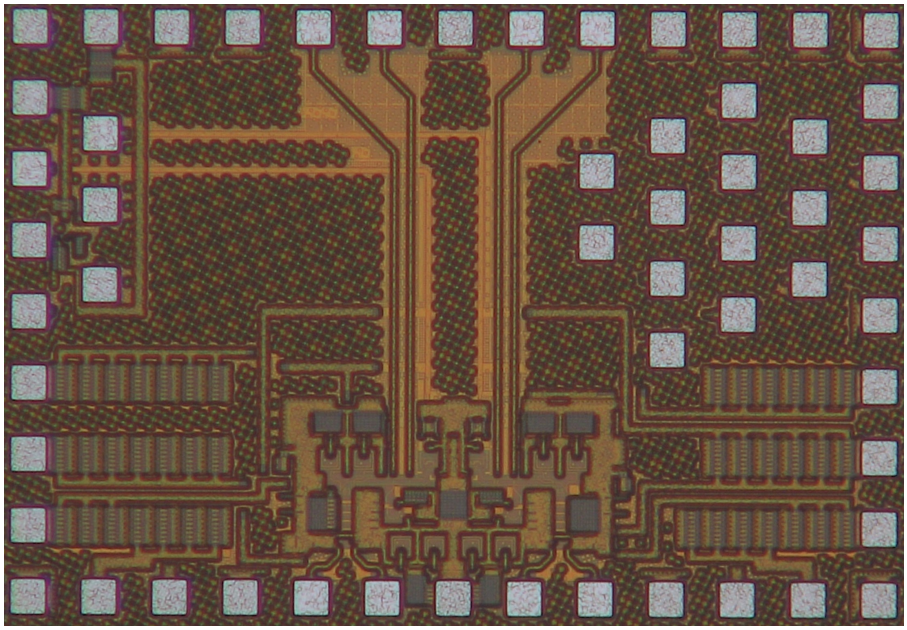

Figure 3.6: Photograph of the coherent receiver IC, implemented in the GlobalFoundries 45RFSOI 45 nm CMOS process. The dimensions are 1.88 m x 1.28 mm. The bondpad pitch is 150 μm.

signal, which is then amplified using a praseodymium-doped fiber amplifier (PDFA) and edge-coupled to the PIC. The other output of the 3 dB coupler is amplified using a semiconductor optical amplifier (SOA) and then connected to an attenuator, the output of which is edge-coupled to the PIC. The EIC outputs are connected to a Keysight real-time oscilloscope (RTO) and the samples are compared to the PRBS sequence for error counting. The specified BW of the IQ-MZM is 25 GHz. To compensate for the IQ-MZM response, feed-forward equalization (FFE) was constructed using two outputs of the BPG with a coaxial power combiner.

The PD responsivity is assumed to be 1 A/W. The data was taken at equal E_{CW} and E_S powers to minimize the DC current and thus minimize the shot noise for a given PD current swing. This way the receiver is characterized in terms of the circuit input-referred noise sensitivity and the intersymbol interference (ISI) power penalty. The measurements are expressed in terms of OMA received at each PD. All constellations consist of at least

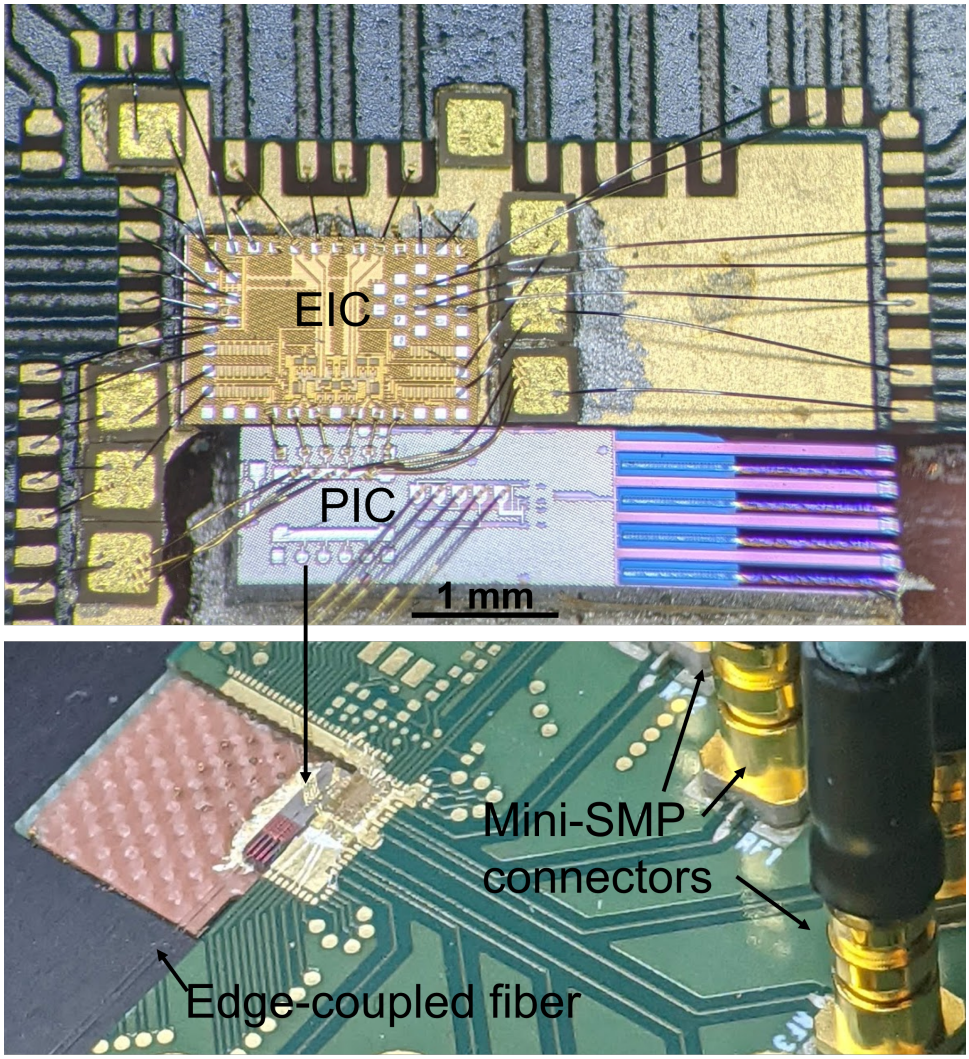

Figure 3.7: Opto-electric receiver assembly on a PCB. The PIC-to-EIC and EIC–to-PCB wirebonds are approximately 200 μm and 750 μm, respectively. Off-chip 1.2 nF bypassing capacitors were added to the PD and EIC supplies. Mini SMP RF connectors are used to measure the two differential data outputs.

2^{18} points and were generated using PRBS15. Measured constellations at 40 GBaud with OMA of -7.6 dBm and 50 GBaud with OMA of -5.5 dBm are shown in Fig. 3.9 a) and b), respectively. At 40 GBaud the FFE tap/main ratio was set to 0.5 and at 50 GBaud the ratio was set to 0.65. At 40 GBaud the BER is 1.2 x 10^{-5} and at 50 GBaud the BER is 9.7 x 10^{-4}, which is below the hard-decision forward error-correction (HD-FEC) limit of 3.8 x 10^{-3}.

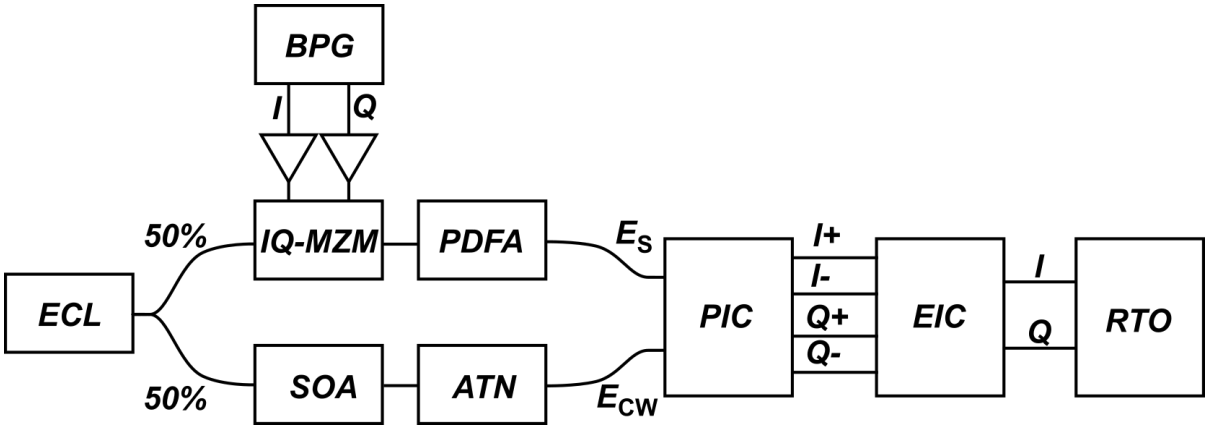

Figure 3.8: QPSK self-homodyne measurement test setup. Polarization controllers and length-matching fiber are omitted from the schematic.

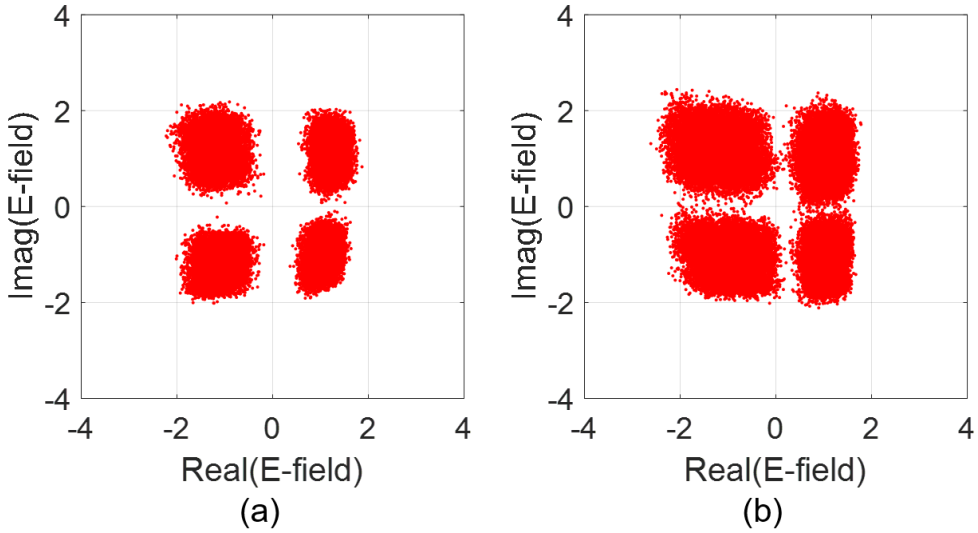

Figure 3.9: Measured QPSK constellations at (a) 40 GBaud and (b) 50 GBaud, both with FFE applied to the IQ-MZI. The measured voltage swings are 60 mVpp and 80 mVpp for 40 GBaud and 50 GBaud,respectively.

The measured BER for various data rates, with and without transmitter FFE, is plotted versus OMA in Fig. 3.10. At 50 GBaud with FFE, the BER is below the HD-FEC limit for an OMA of -8.4 dBm. At 40 GBaud without FFE the required OMA for the same limit is is -8.7 dBm. A 2nd optoelectric assembly of the EIC was built using a Rockley SiPh receiver PIC. The assembly of the optoelectric receiver is shown in Fig. 3.11. The measured constellations and BER vs received signal power is shown in Fig.

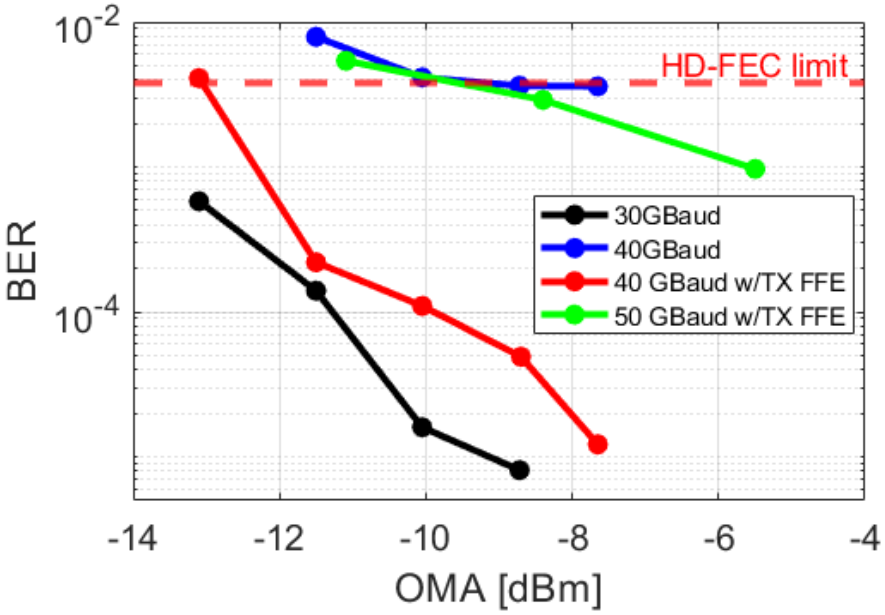

Figure 3.10: BER vs. OMA received at each PD

3.12. FFE was enabled for all of the Rockley receiver measurements.

Table 3.1 shows a comparison with state-of-the-art O-band coherent receivers implemented using silicon photonics. At 0.98 pJ/bit, our receiver design achieves record energy efficiency.

Reference	**Technology**	**Integration Level**	**Data Rate (Gbaud)**	**Mod. format**	**R_T (dBΩ)**	**IRNC (μA_{rms})**	**P_{DC} (mW)**	**Energy efficiency (pJ/bit)**
This work	**45nm CMOS / 90nm SiPh**	**Hybrid**	**50**	**QPSK**	**53.6**	**6.3**	**98**	**0.98**
[36]	250nm SiGe BiCMOS	Monolithic	56	QPSK	74	2.22	485	4.33
[40]	130nm SiGe BiCMOS / 90nm SiPh	Hybrid	40	QPSK	67.2	7	534	6.68

Table 3.1: Performance Comparison with State-of-the-Art Optical Receivers

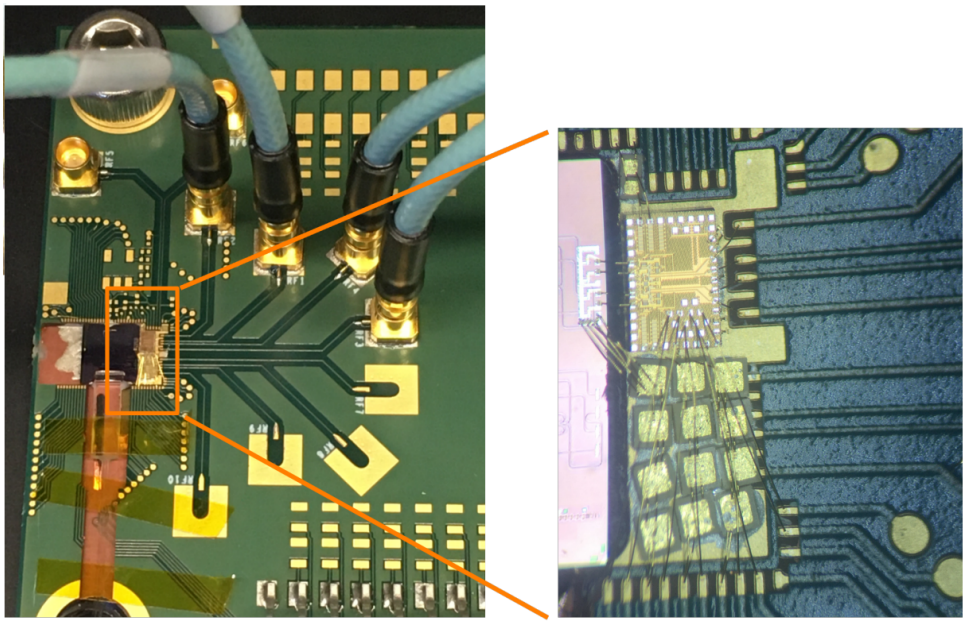

Figure 3.11: PCB Assembly of EIC and Rockley SiPh PIC.

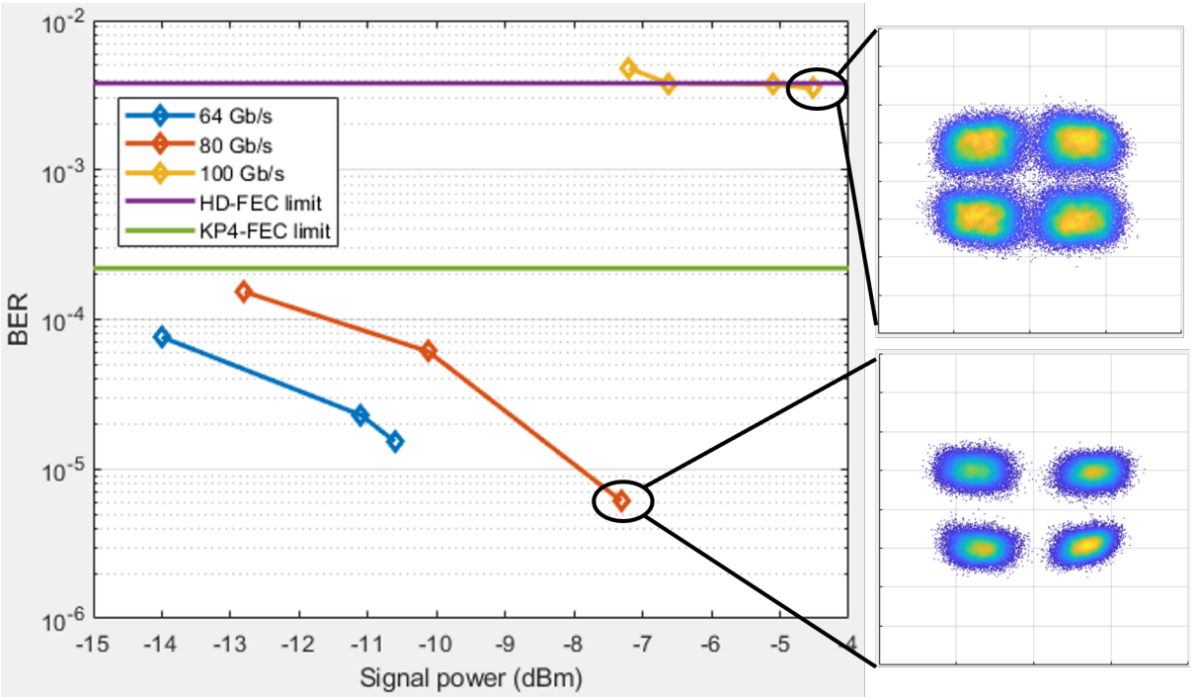

Figure 3.12: Sensitivity Curves and Constellation of the optoelectric receiver with the Rockley SiPh PIC.

3.3 Costas Loop Phase-Frequency Detector and Loop Filter

3.3.1 Phase-Frequency Detector

The Costas Loop is an extension of the phase-locked loop. It is used to simultaneously for carrier phase recovery and phase demodulation. A key component of the Costas Loop is the phase-frequency detector (PFD). The PFD produces an error signal that, in the small-signal regime, is proportional to the phase error between the local oscillator and the carrier of the received data signal. Fig. 3.13 shows the PFD block within a QPSK Costas Loop optical receiver. The PFD is composed of two voltage mixers and a differential to

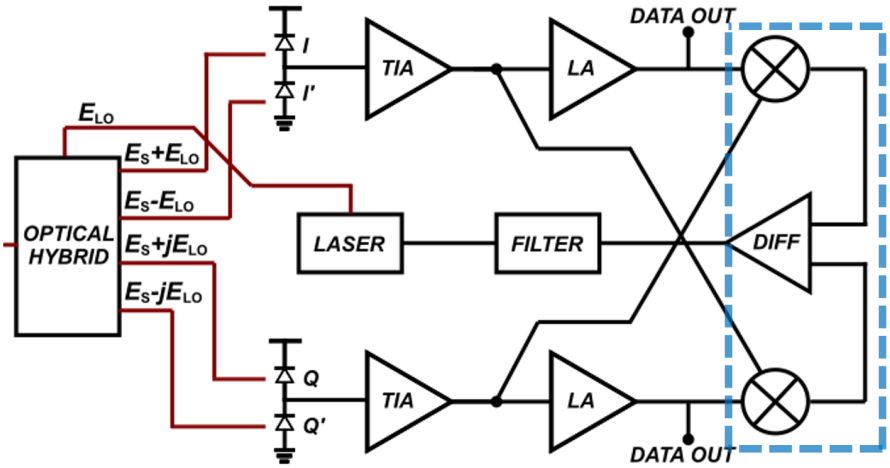

Figure 3.13: PFD block within a QPSK Costas Loop Optical receiver. The PFD is composed of two voltage mixers and a differential to single-ended amplifier.

single-ended amplifier, as shown in Fig. 3.14. The simulated 3-dB BW of the PFD obtained with a step response is 232 MHz and the gain is 76 mV/rad. The PFD is tested by inputting an electrical signal that emulates the PD response to a frequency error between the local oscillator laser and the transmitter laser, without any data modulation. A Keysight arbitrary waveform generator (AWG) was used to generate the quadrature

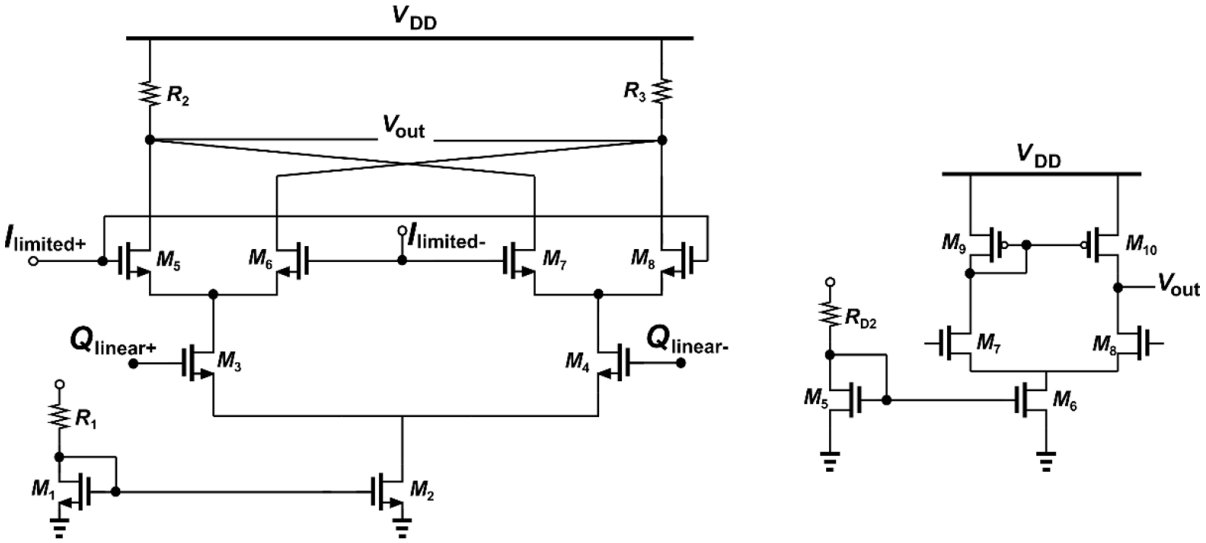

Figure 3.14: Schematic of the Gilbert Cell mixer and differential to single-ended amplifiers. These blocks make up the PFD that is utlized in the QPSK Costas Loop.

beat tone at the TIA input. Fig. 3.15 shows the measured time-domain waveforms. The I and Q dataOut waveforms are the amplified beat tones measured at the output of

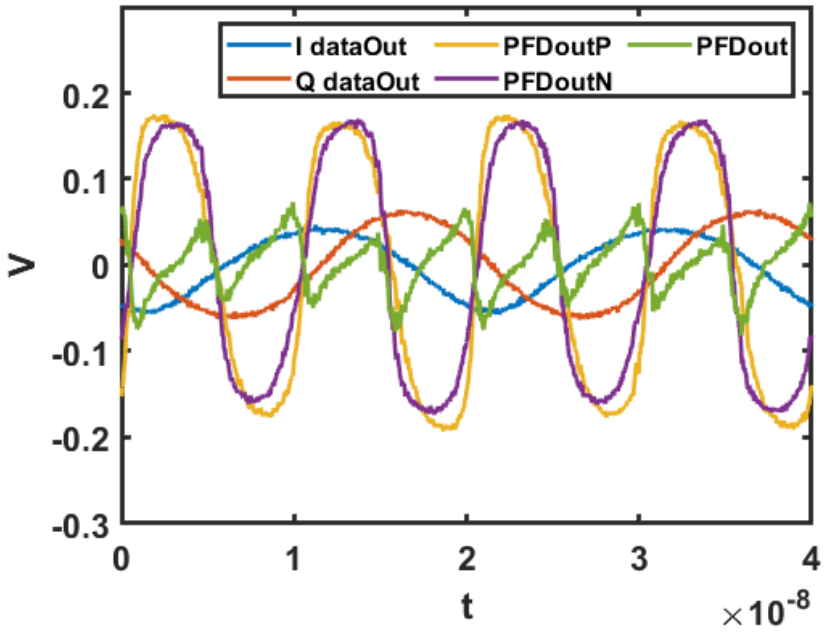

Figure 3.15: Transient measurement of the PFD response to a 50 MHz beat tone. The beat tone is emulated by inputting a sinusoidal waveform at each TIA input. The two input stimuli are in quadrature.

the receiver output buffer. The PFDoutP and PFDoutN waveforms corresponds to the measured single-ended waveforms at the PFD output, and PFDout is the subtraction of the two PFDoutP and PFDoutN. PFDout is a sawtooth with 4 times the frequency of the beat tone [41].

3.3.2 Loop Filter OpAmp

In the QPSK Costas Loop the PFD output signal is filtered before being fed back to the local oscillator laser to keep it locked to the carrier of the received signal (Fig. 3.16). The loop filter is typically a proportional-integral controller, with tunable proportional

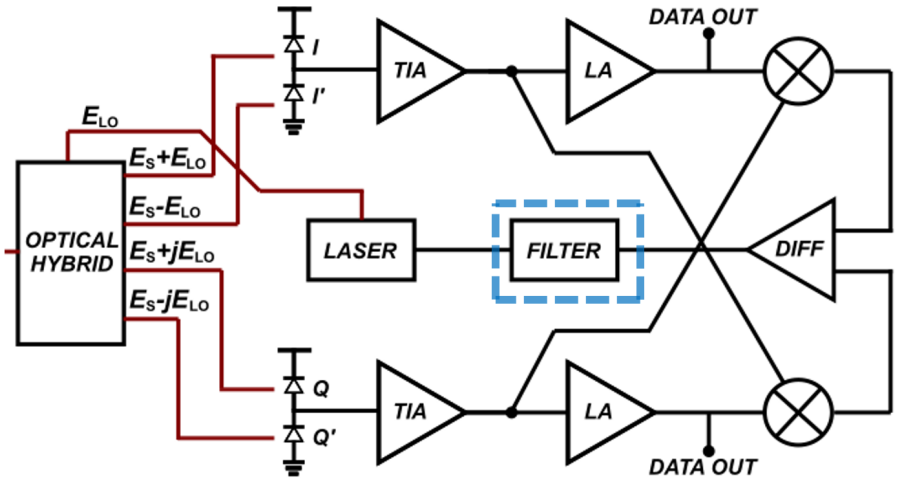

Figure 3.16: Loop filter within a QPSK Costas Loop Optical receiver. The loop filter is a PI controller composed of an OpAmp and resistors and capacitors that define the proportional and integral gain coefficients.

and integral gain coefficients. The loop filter is implemented with an OpAmp, resistors and capacitors, as shown in Fig. 3.17. The two time constants are $\tau_1 = R_1C$ and $\tau_2 = R_2C$. The transfer function of the loop filter assuming an ideal OpAmp is:

$$F(s) = -\frac{s\tau_2 + 1}{s\tau_1} = -(\frac{\tau_2}{\tau_1} + \frac{1}{s\tau_1}) \tag{3.1}$$

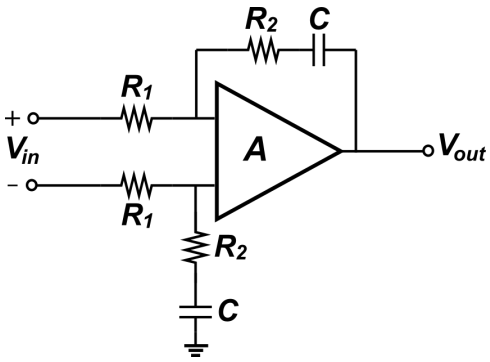

Figure 3.17: Proportional-integral controller implemented with an OpAmp.

The proportional gain coefficient is given by $K_p = \tau_2/\tau_1$ and the integral gain coefficent is given by $K_i = 1/\tau_1$. In our loop filter implementation, a two-stage on-chip OpAmp is used to minimize the delay between the PFD output and OpAmp input. The schematic is shown in Fig. 3.18. The post-layout open-loop frequency response of the OpAmp is

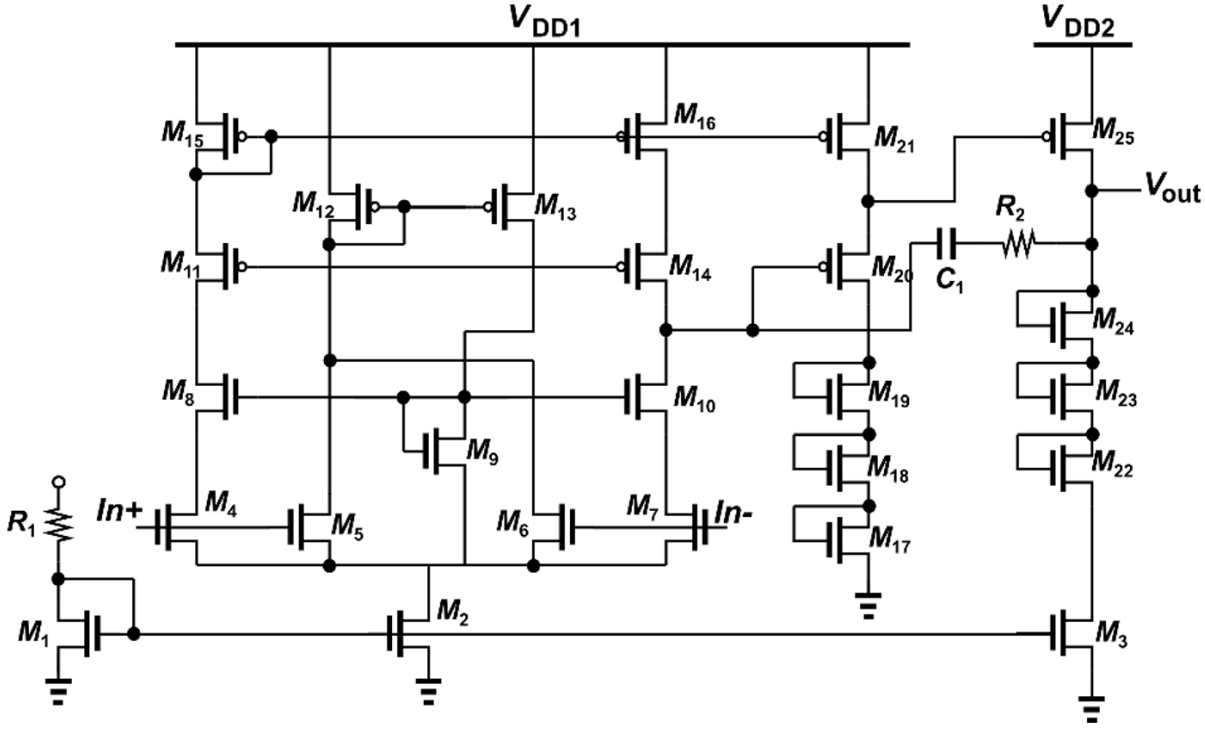

Figure 3.18: Schematic of the two-stage OpAmp.

plotted in Fig. 3.19. The midband gain is 65 dB and the 3-dB BW is 200 MHz. The

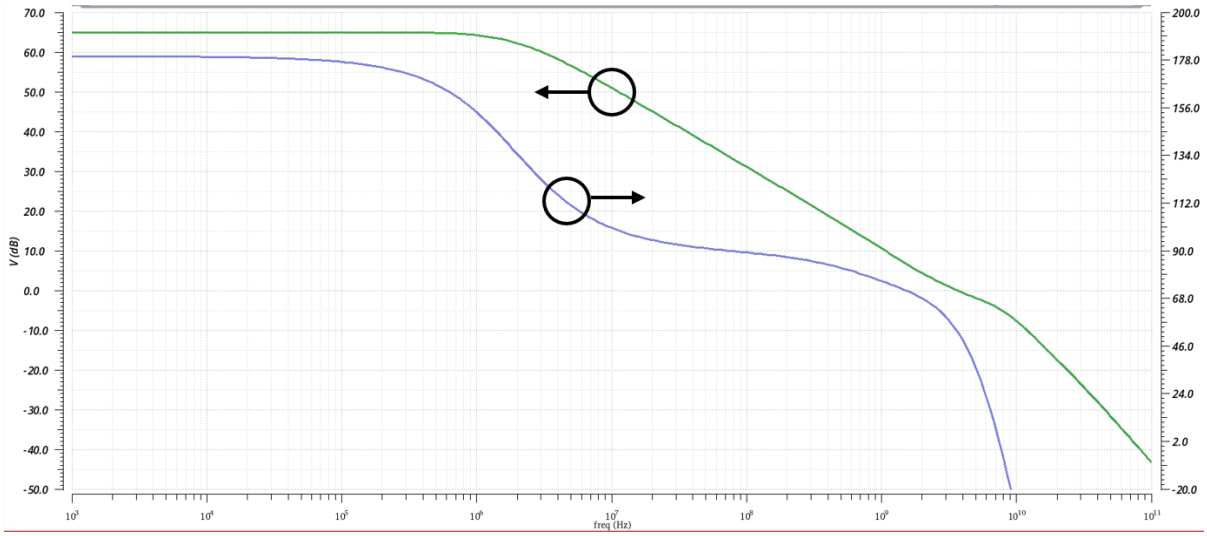

Figure 3.19: Simulated post-layout OpAmp open-loop frequency response.

OpAmp has a unity-gain BW of 3.5 GHz, a 49 degree phase margin and 5 dB of gain margin. Initial time-domain open-loop measurements were performed on the on-chip OpAmp (Fig. 3.20).

3.3.3 QPSK Costas Loop Open-Loop Response

The open-loop response of the QPSK Costas Loop is calculated by cascading the PFD, loop-filter, and the local oscillator laser phase section. The PFD transfer function has one pole at 232 MHz and 76 mV/rad of gain. The simulated OpAmp midband gain and unity-gain BW are both large enough for it to be approximated as ideal. There is a transconductance stage at the output of the OpAmp, consisting of an NFET with a g_m of 6.2 mA/V. The transconductance stage is connected to the local oscillator phase section, which is modelled as a current-controlled oscillator with a τ of 1.6 ns and gain of 2 GHz/mA. An integrator (1/s) is then added to convert from frequency to phase. The total loop delay, which accounts for delay on the EIC, PCB and waveguides on the receiver PIC, is lumped into a single loop delay of 183 ps. The QPSK Costas Loop transfer function

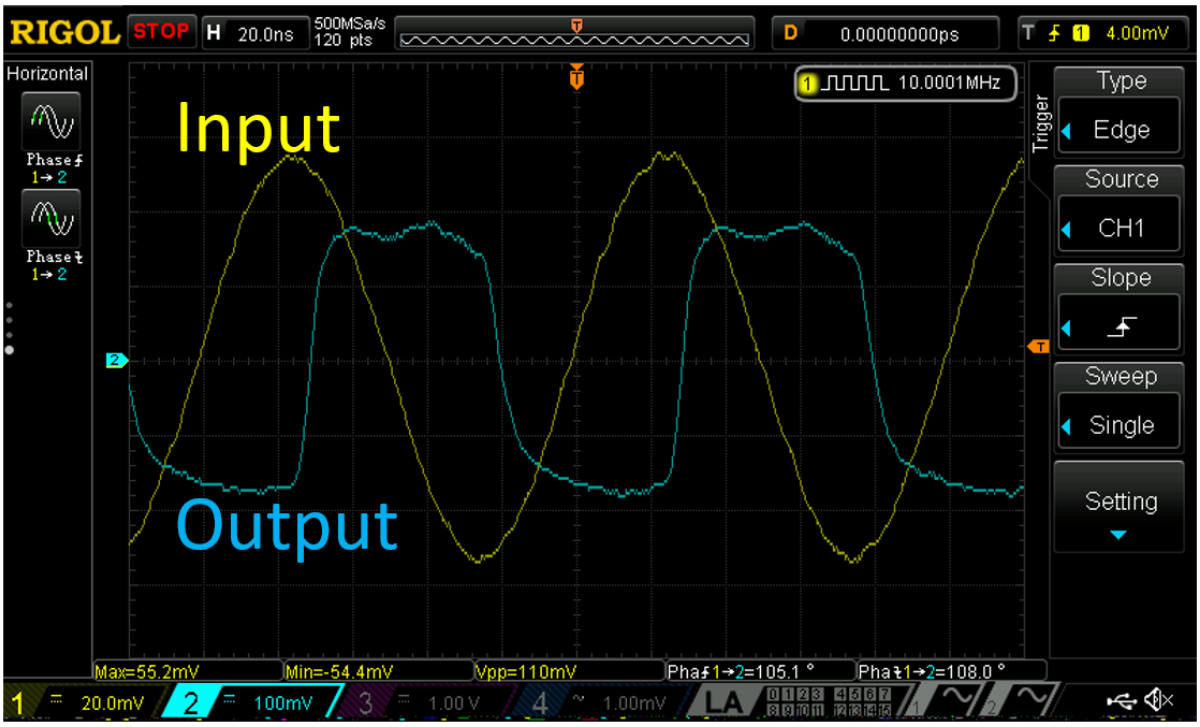

Figure 3.20: Simulated post-layout OpAmp open-loop frequency response.

block diagram is shown in Fig. 3.21. The post-layout open-loop response, simulated with a beat tone amplitude of 200 μA_{pp}, is shown in Fig. 3.22. The QPSK Costas Loop has a unity-gain BW of 108 MHz, a phase margin of 15°, and a gain margin of 43 dB.

3.4 Conclusions

In this work, we presented a 0.98 pJ/bit single-polarization O-band QPSK receiver fabricated in 45 nm CMOS and a 90 nm SiP process. The operation of the receiver was demonstrated at up to 50 GBaud below the HD-FEC BER limit. The EIC was assembled with two different SiPh PICs, and 100 Gb/s BER was achieved in both. With these results, we believe that the PIC and the electronics can be utilized within a carrier recovery system such as QPSK costas loop to enable low power intra-datacenter optical links. The QPSK Costas Loop PFD and loop filter OpAmp were also described and

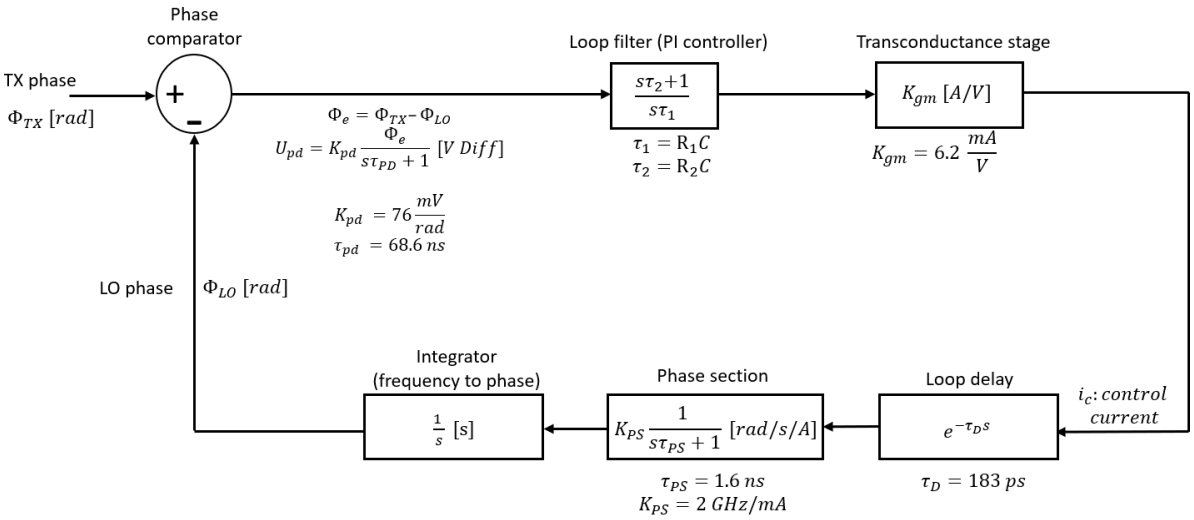

Figure 3.21: QPSK Costas Loop transfer function block diagram.

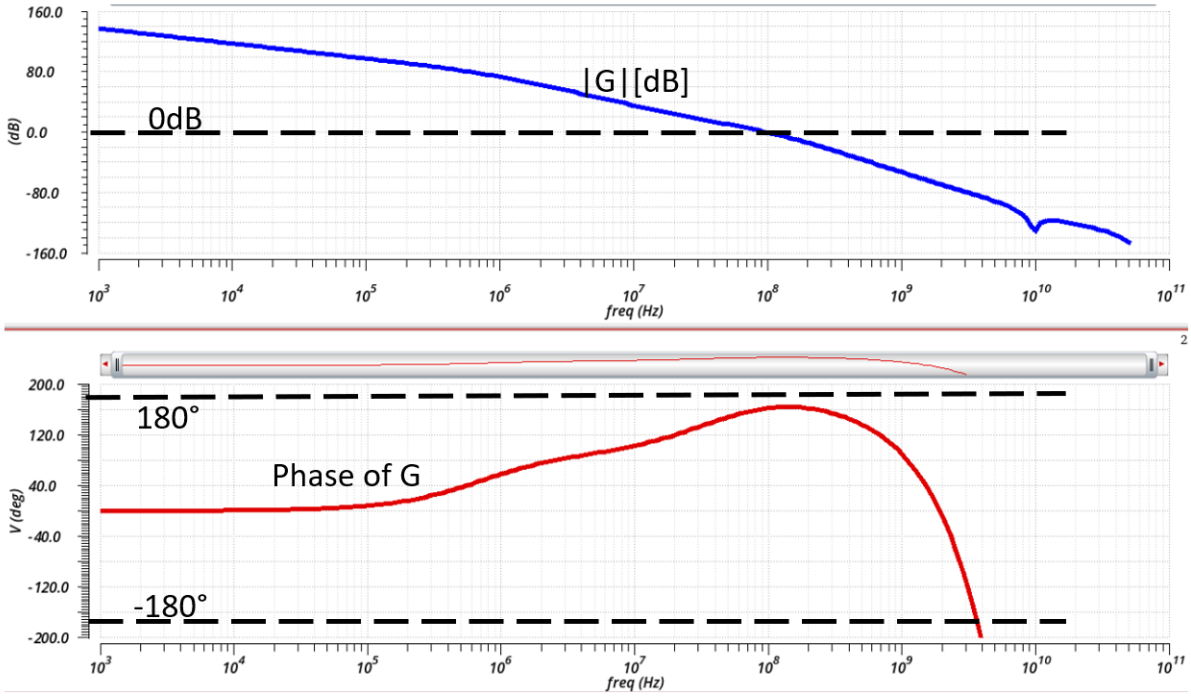

Figure 3.22: QPSK Costas Loop post-layout simulated open-loop frequency response.

initial time-domain measurements were presented. Post-layout open-loop simulations of the QPSK Costas Loop were also described, which indicate that stable 100 MHz response can be achieved.

Chapter 4

An 8.2-pJ/bit, 56 Gb/s Traveling-wave Modulator Driver with Large Reverse Terminations

4.1 Introduction

While optical transmitters (TX) based on narrow-band ring-resonator modulators have been demonstrated [42], these are highly sensitive to process and temperature variations [43] compared to MZM devices, which are broadband and thus area widely used in commercial settings. TXs based on segmented MZMs (SEG-MZM) have also been reported [44] to lower insertion loss compared to unamplified TW-MZMs. However, when SEG-MZMs are implemented using hybrid integration, the packaging complexity increases significantly. While monolithic integration reduces the packaging complexity of TXs based on SEG-MZMs, the power dissipation of TW-MZMs can be significantly lower while still achieving the required optical output power by utilizing semiconductor optical amplifiers (SOA) [45].

The challenges of scaling intra-datacenter intensity-modulation direct detection (IMDD) links beyond 100 Gb/s have driven an increased interest in analog coherent detection (ACD) [4]. Dual polarization quadrature phase shift keying (DP-QPSK) has been proposed as a modulation format for ACD. One key advantage of DP-QPSK is that highly linear electronics are not required, which results in significant power savings. Silicon Photonics (SiPh) TW-MZMs are expected to enable low energy-per-bit (EPB) operation in DP-QPSK links while minimizing fabrication costs [4].

The design presented here drives a SiPh TW-MZM to generate one of four DP-QPSK channels. Shown in Fig. 4.1 are the drivers within one of the polarizations of a DP-QPSK transmitter. A cascode topology is employed to obtain 17.7 dB of differential gain, a 3dB BW of 47 GHz accounting for packaging parasitics, and 4.4 V_{ppd} swing in a 50 Ω environment, with a power consumption of 460 mW, equivalent to 8.2 pJ/bit at 56 Gb/s.

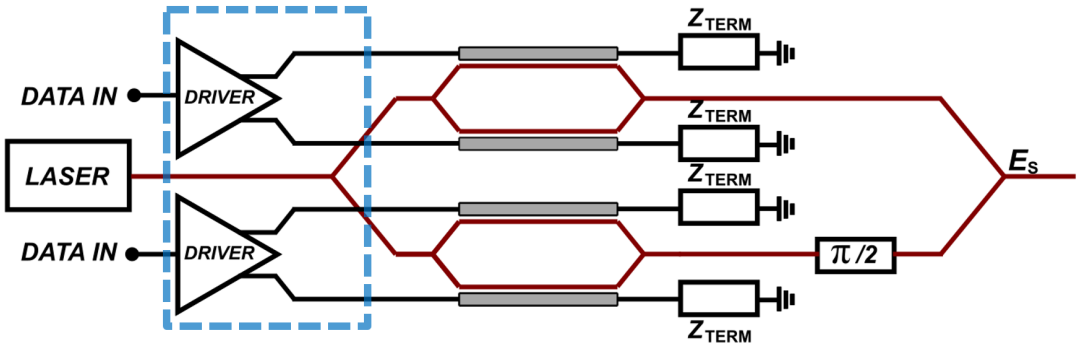

Figure 4.1: Driver variants for biasing the TW-MZM at a) 4 V and b) 1 V reverse bias. The middle ground electrode is omitted for simplicity.

4.2 Circuit Topology and Driver-Modulator Co-design

4.2.1 MZM Biasing Variants

SiPh TW-MZMs are based on PN junction phase shifters that exploit the plasma dispersion effect, in which the carrier concentration, which depends on the electric field, changes the refractive index. The phase efficiency, the waveguide optical loss, and the PN junction capacitance all depend on the PN junction bias voltage. While the capacitance and optical loss decrease with higher reverse bias, the phase efficiency also typically decreases [46]. Because of this tradeoff it is beneficial to evaluate different TW-MZM bias voltages. Fig. 4.2 depicts two TX configurations for which driver variants were fabricated. In the configuration shown in Fig. 4.2 a) the TW-MZM ground electrodes are connected

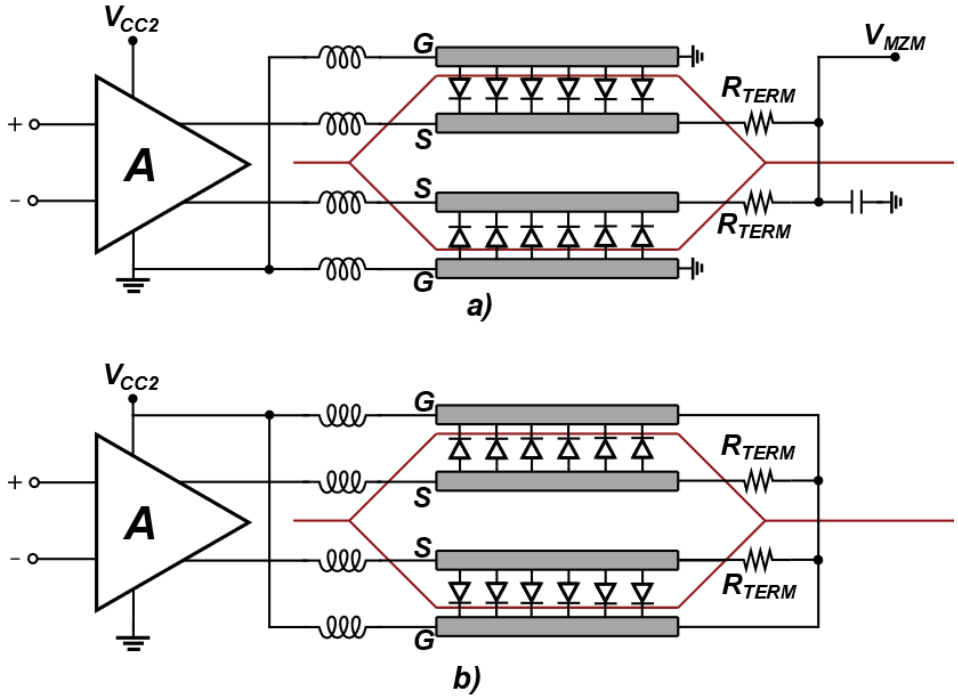

Figure 4.2: Driver variants for biasing the TW-MZM at a) 4 V and b) 1 V reverse bias. The middle ground electrode is omitted for simplicity.

to the driver ground node and the PN junction has a reverse bias of approximately 4 V.

In the other configuration (Fig. 4.2 b)), the TW-MZM ground electrodes are connected to the voltage supply of the driver output stage and has a PN junction reverse bias of approximately 1 V. Both configurations enable even-mode termination, which extends down to DC in the 1 V configuration and has a low-frequency cutoff determined by on-chip and off-chip bypassing capacitors in the 4 V configuration.

4.2.2 Circuit Topology

The circuit schematic is shown in Fig. 4.3. The driver consists of input 50 Ω-matching

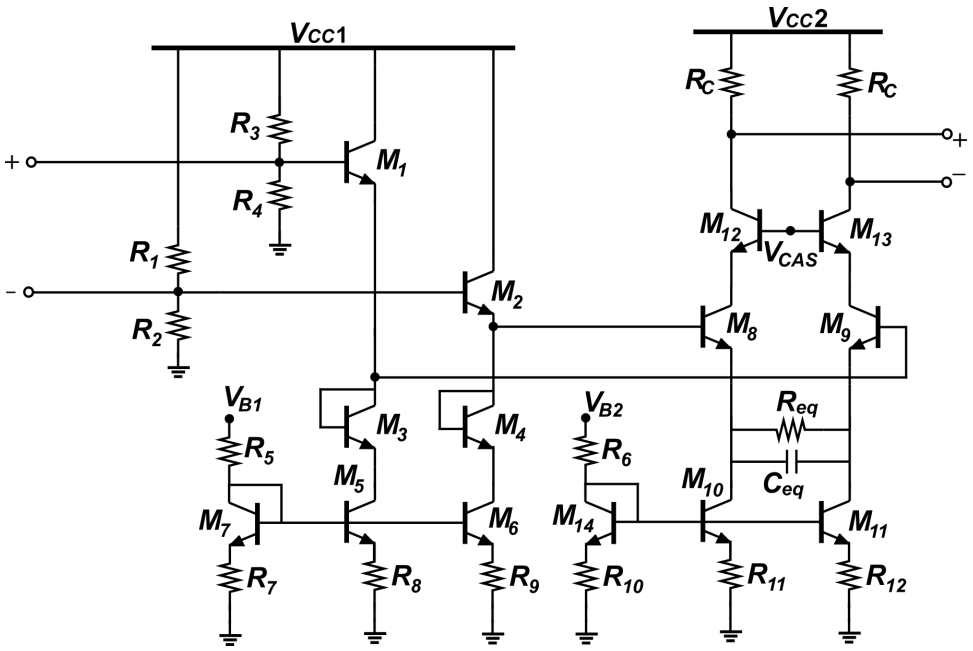

Figure 4.3: Cascode TW-MZM driver circuit schematic.

emitter-followers and a cascode stage with supplies of 3 V and 5.8 V, respectively. The device lengths are 10 µm for M_1-M_6, 30 µm for M_8-M_{11}, 18 µm for M_{12} and M_{13}, and 2 µm for the current mirror devices M_7 and M_{14}. Emitter degeneration resistors R_7 – R_{12} are added to improve current matching and output resistance. The load resistors (R_C) are 130 Ω. The cascode stage allows for BW extension by reducing the miller capacitance while

also increasing the output voltage swing. Continuous-time linear equalization (CTLE) is implemented with R_{eq} (3 Ω) and C_{eq} (820 fF), which introduces a zero to add peaking at the expense of DC gain. The supplies are 3 V and 5.8 V for VCC_1 and VCC_2, respectively, and the output DC voltage is 5V. The output stage has a total current of 65 mA and is designed to produce 3 V_{pp} of differential swing to a DC-coupled 30 Ω TW-MZM, as shown in Fig. 4.2. 30 Ω was chosen because it is a typical single-ended Z_0 (60 Ω differential) for SiPh TW-MZMs [46]. The simulated post-layout differential gain and group delay frequency response at the TW-MZM input are shown in Fig. 4.4. The assumed bond pad capacitances are 15 fF and 25 fF for the driver and TW-MZM,

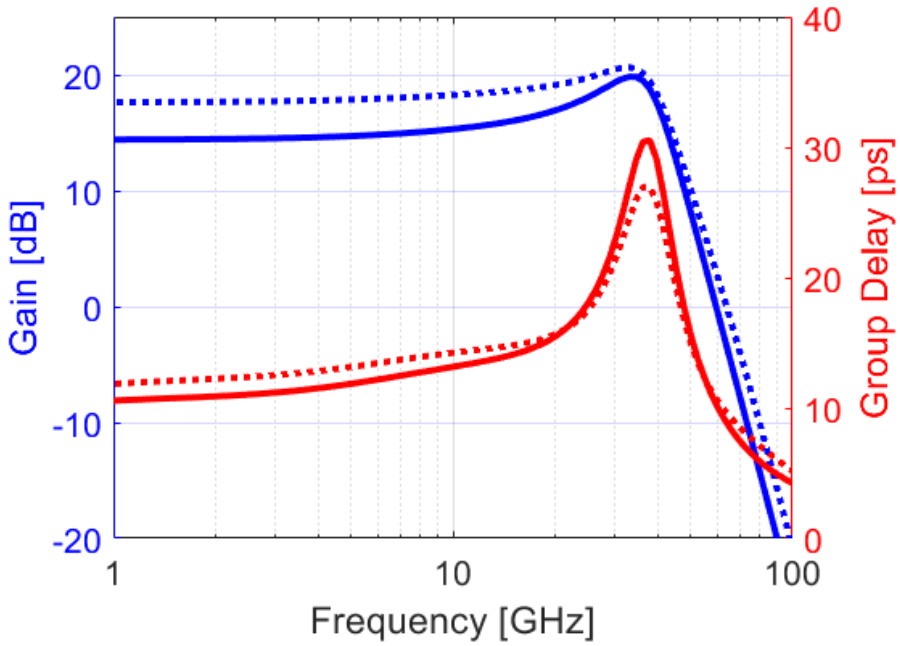

Figure 4.4: Simulated post-layout differential gain and group delay versus frequency for TW-MZM input impedances of 50 Ω and 30 Ω, accounting for packaging wirebond and bond pad parasitics.

respectively. The simulated wirebond inductance between the PCB and EIC ($L_{bond,in}$) is 200 pH and between the EIC and PIC ($L_{bond,out}$) it is 150 pH. When loaded with 50 Ω, the driver has a differential midband gain of 17.7 dB and 3 dB of peaking. When the

load is 30 Ω, the gain is reduced to 14.5 dB and the peaking increases to 5.4 dB, which also results in a larger group delay variation (GDV) by 3 ps when calculated up to 35 GHz.

4.2.3 Packaging Considerations

Simulations indicate that the packaging of the driver and TW-MZM is critical to achieve the target bit rate. Difference in die thicknesses of EICs and PICs, as well as the lateral separation between EICs and PICs on the PCB, can result in excessive inductance values for $L_{bond,in}$ and $L_{bond,out}$t when utilizing wirebond connections. The simulated TX electro-optic (EO) BW and GDV, versus $L_{bond,in}$ and $L_{bond,out}$, are shown in Fig. 4.5 a) and b), respectively. The EO BW of the standalone TW-MZM is assumed to be 25 GHz, which was simulated as a high impedance first-order low-pass filter (LPF). The simulated TW-MZM input impedance (Z_{in}) is 30 Ω. The GDV was calculated up to 35 GHz, which is 62.5% of 56 Gb/s, and is a typical target BW at the transimpedance amplifier (TIA) output for the optimum compromise between inter-symbol interference (ISI) and noise power penalties. The blue contour curves denote typical targets for the TX EO BW of 40 GHz and GDV of 4 ps in Fig. 4.5 a) and b), respectively. It can be observed that the GDV specification imposes a stricter constraint on the input and output wirebond inductances.

4.2.4 Quasi Open-Collector Driver

A common approach to high-swing MZM driver design is to utilize an open-collector (OC) output stage [47] [48]. An advantage of OC is that power consumption is minimized for a given voltage swing. However, one drawback of OC drivers is that back-propagating waves are entirely reflected at the driver output, which produces ISI. Back-propagating

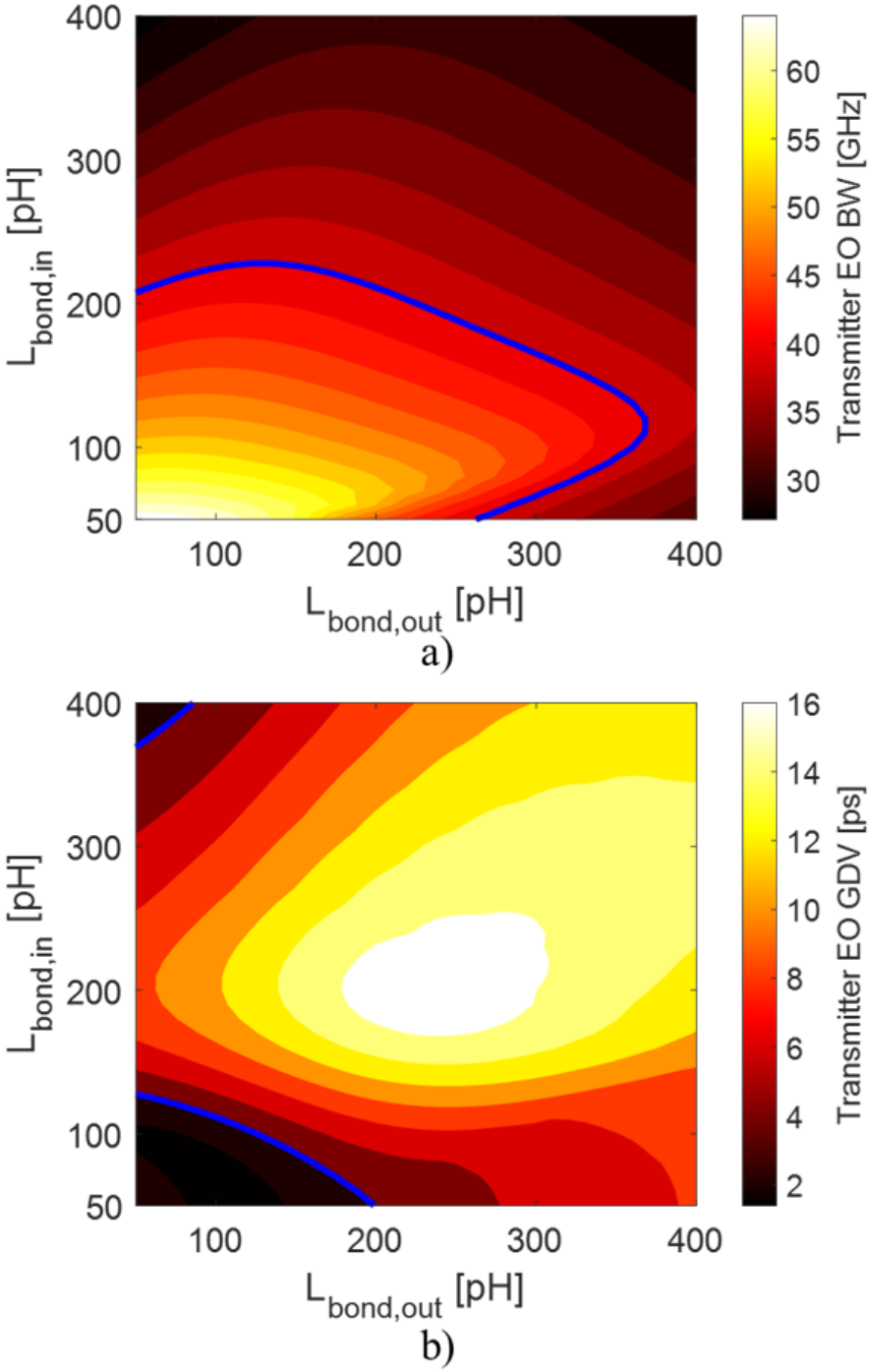

Figure 4.5: Simulated transmitter a) electro-optic (EO) BW and b) GDV, versus input and output wirebond inductances. TW-MZM Zin = 30 Ω. The blue contour curves denote the design targets of 40 GHz in a) and 4 ps in b).

waves are produced at the impedance mismatch along the transmission line and if the MZM termination (R_{term}) is not matched to the transmission line. The latter case can be more significant, since R_{term} can be purposefully mismatched to produce an equalizing effect on the EO response. For this reason, a quasi open-collector design was implemented with 130 Ω driver load resistors. This reduces the reflection coefficient by 38% while increasing the power consumption of the output stage by less than 20%, and the total driver power by less than 15%. Moreover, decreased reflections minimize the need

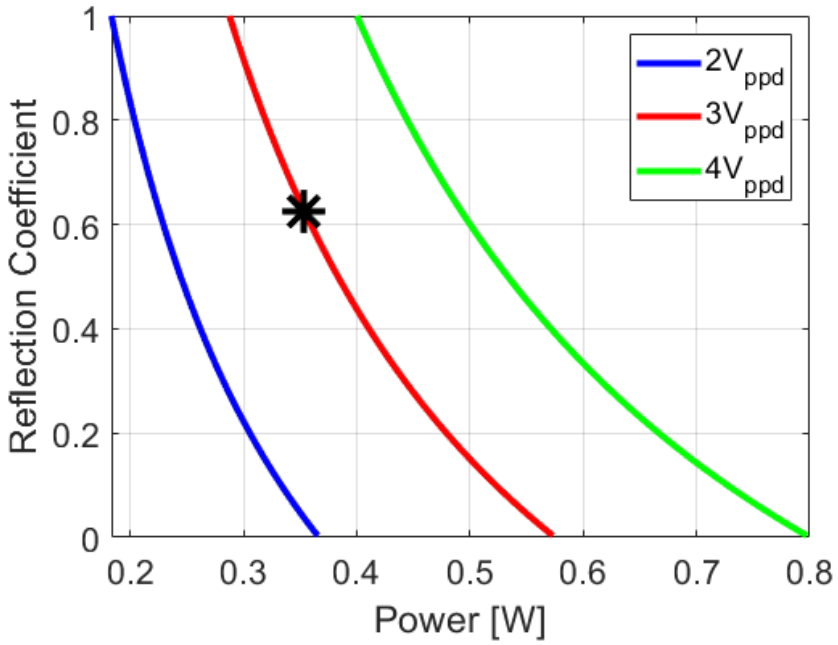

Figure 4.6: Relationship between the reverse termination Γ, output stage collector resistance, and the output stage power for various differential voltage swings.

for DSP, which can significantly reduce the optical link power. Fig. 4.6 depicts the calculated reflection coefficient (Γ) versus the output stage power consumption for various differential voltage swings (V_{sd}), assuming $R_{term} \approx Z_0$. The power was calculated for the configuration shown in Fig. 4.2 b), assuming a 5 V driver output common-mode voltage (V_{cm}) and a TW-MZM Z_0 of 30 Ω. At higher voltage swings, it becomes more power-demanding to reduce Γ. The asterisk denotes our driver design. The power consumption

of the output stage is calculated as:

$$P = \frac{V_{sd}(4V_{cm} + V_{sd})}{8(R_C||R_{term})} \tag{4.1}$$

4.2.5 Measurement Results

The driver was fabricated in the GlobalFoundries 8XP 130 nm SiGe BiCMOS process. The die area is 1.23 mm x 0.73 mm for a two-channel driver. The ICs of the two driver variants, as described in Fig. 4.2 are shown in Fig. 4.7. Fig. 4.8 shows a photograph of the wirebonded EIC assembly on a PCB. The die thickness is 250 µm and the estimated length of the RF wirebonds is 320 µm. Off-chip 1.2 nF bypassing capacitors were added to VCC_1 and VCC_2. Mini SMP RF connectors are utilized at the driver inputs and outputs. Bias-tees were used to AC-couple the 50 Ω Tektronix sampling oscilloscope (SO) and to source current to emulate a DC-coupled TW-MZM, as shown in Fig. 4.9. The signal was attenuated by 10 dB to operate within the SO limits. A SHF 12104a

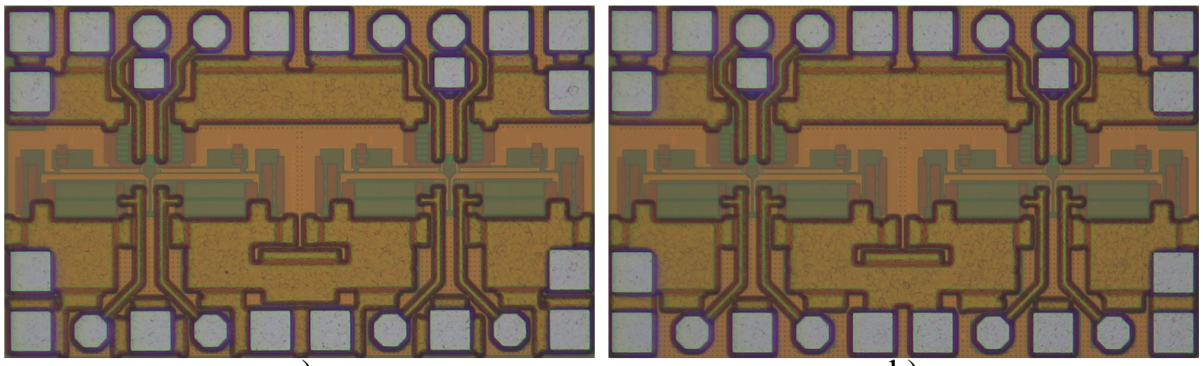

Figure 4.7: Photograph of the driver ICs. The configurations correspond to those shown in 4.2.

bit-pattern generator (BPG) was used to generate the PRBS31 signal with a single-ended amplitude of 400 mV_{pp}. Fig. 4.10 contains the measured eye-diagrams at several data rates. BER Bathtub curves, taken with a SHF 11104A bit error tester (BERT), for 30,

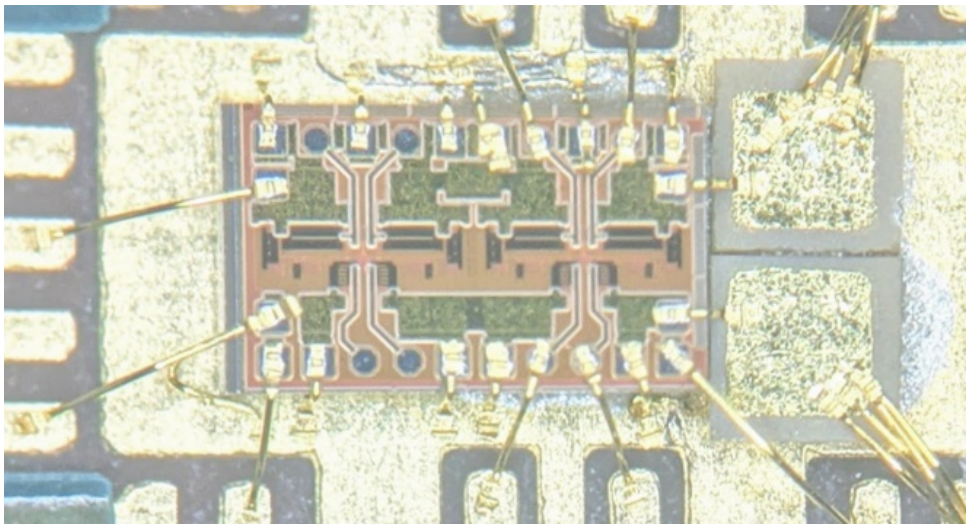

Figure 4.8: Driver assembly on a PCB. The IC corresponds to the configuration a), as shown in Fig. 4.2. The die thickness is 250 µm and the estimated length of the RF wirebonds is 320 µm. Off-chip 1.2 nF bypassing capacitors were added to VCC_1 and VCC_2. Mini SMP RF connectors are utilized at the driver inputs and outputs.

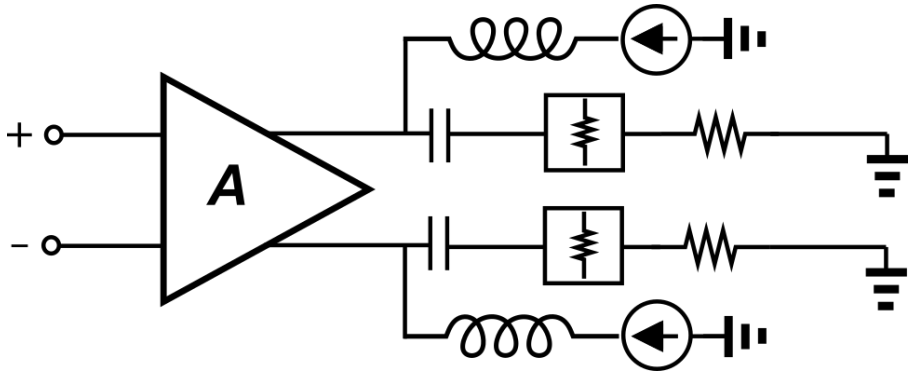

Figure 4.9: Electrical testing schematic. Bias-tees were used to AC-couple the 50 Ω SO and to source current to emulate a DC-coupled TW-MZM. The signal was attenuated by 10 dB to operate within the SO limits.

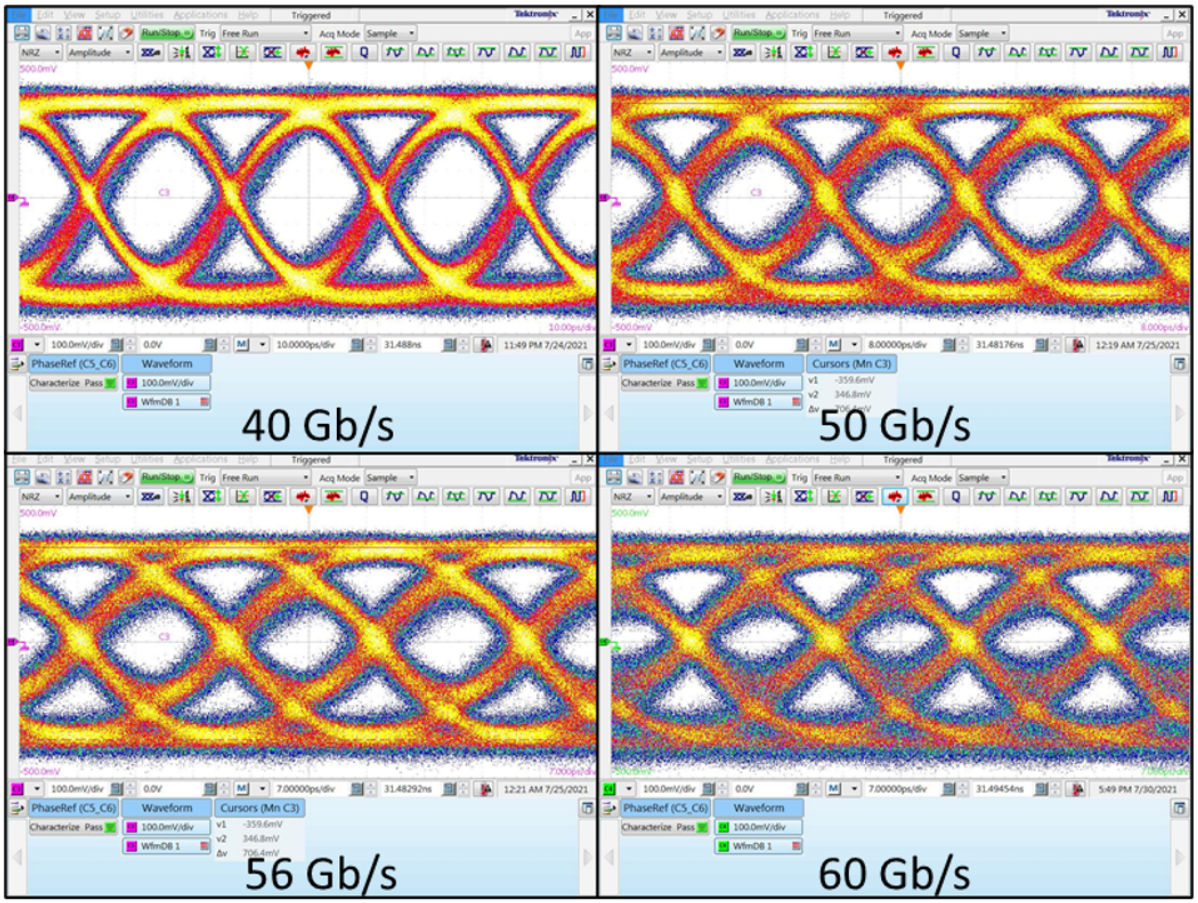

Figure 4.10: Single-ended PRBS31 eye-diagrams at various data rates. The voltage swing is 710 mV after 10 dB of attenuation.

40, and 50 Gb/s are shown in Fig. 4.11. At least ten errors were counted for all the BER measurements above 10^{-12}. For the error-free measurements, at least 3 x 10^{12} bits were transmitted, resulting in a specified BER of 10^{-12} with a confidence level of 95%. Table

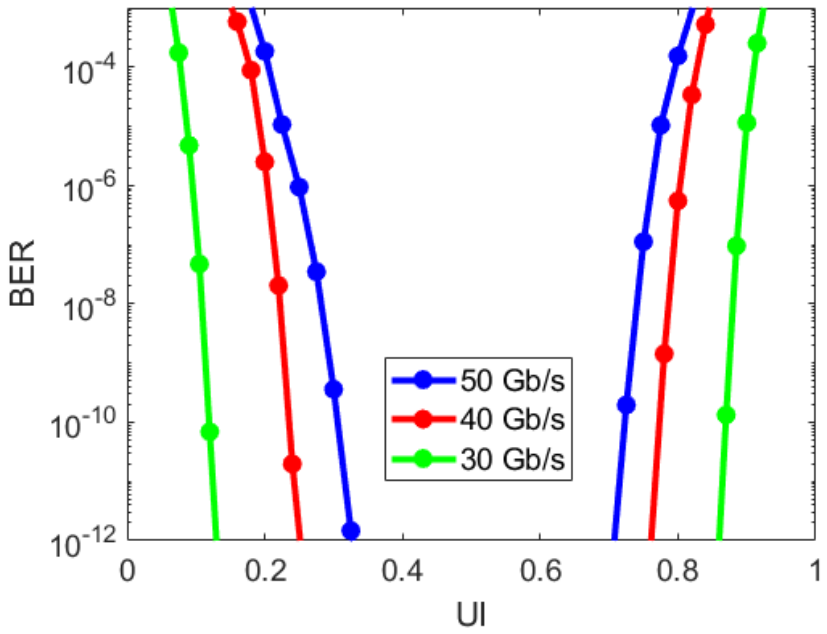

Figure 4.11: Bathtub curves for 30, 40, and 50 Gb/s.

4.1 contains a summary of state-of-the-art TW-MZM drivers. The reflection coefficient for a 30 Ω load is included, as this is a typical value for a SiPh TW-MZM. The modulation factor (FM) is calculated for a typical 3 mm SiPh TW-MZM with a $V_\pi L$ of 19 V*mm [4]. The F_M indicates the modulation factor for a null-biased MZM. For a differential voltage swing of $2V_\pi$, F_M=1 and there is no modulation loss, as shown in Fig. 4.12[4]. If the voltage swing is decreased to V_π, F_M=0.5. A figure-of-merit (FOM) is proposed as:

$$P = \frac{A_{MOD}B}{P}[\frac{bit}{J}] \tag{4.2}$$

where A_{MOD} is the modulation gain of the TX, B is the bit rate, and P the power per driver channel. A_{MOD} is the ratio of the F_M with and without the driver for a 30 Ω TW-MZM. The FM without the driver is calculated assuming the driver input swing ($V_{ppd,in}$) is directly applied to the modulator, i.e., if the driver were removed from the TX. The $V_{ppd,in}$ was obtained from the cited papers or calculated from the small-signal gain, only in the case of the linear drivers indicated on Table 4.1, for which significant compression is not expected. The FOM is a measure of the driver gain, output swing, bandwidth, and power dissipation for a typical TW-MZM design. It also demonstrates the tradeoff associated with higher-order modulation formats, which enable higher bit rates at the cost of stricter linearity constraints, resulting in lower output voltage swings for a given power consumption. Our driver achieves a competitive FOM while maintaining a low Γ compared to open-collector designs.

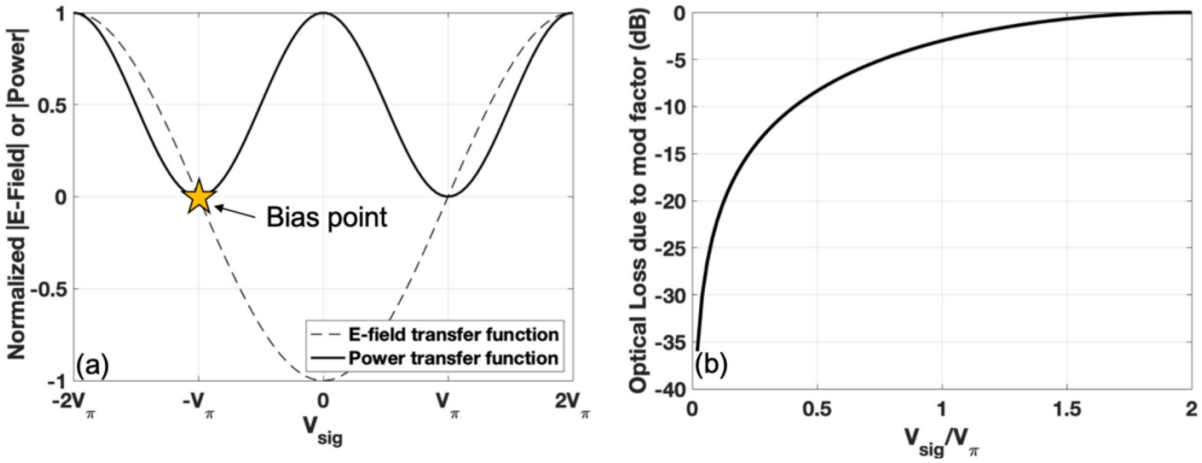

Figure 4.12: Electric field and associated output optical power of an MZM and the bias point of the MZM for QPSK modulation. (b) Optical loss in dB due to modulation factor plotted vs. the ratio of V_{sig}/V_π.

4.2.6 Conclusion

In this chapter we have presented a modulator driver consisting of a quasi open-collector cascode output stage. Two driver variants were fabricated to investigate the electrical and optical performance tradeoffs of operating at different TW-MZM biases. An analysis of the EIC/PIC packaging constraints was presented and the advantages of having large RC resistors versus open-collector output stages were discussed. The driver was tested electrically, and open eye-diagrams were obtained at up to 60 Gb/s. A FOM for TW-MZM drivers was proposed to compare drivers across different modulation formats. A comparison with the state-of-the art indicates that our driver has a competitive FOM while providing a better back termination match than OC drivers, which is expected to reduce the ISI effects of secondary reflections in TW-MZMs. The operation of this driver in PAM4 applications would likely be done at lower voltage swings due to linearity specifications.

Reference	**Technology**	**f_t/f_{max}**	**Mod. format**	**Bit rate (single channel Gb/s)**	**Power per channel (W)**	**Output swing to 50 Ω (V_{ppd})**	**Driver load (Ω)**	**Γ (30 Ω MZM)**	**F_M§**	**FOM (bit/pJ)**
This work	**130nm SiGe BiCMOS**	**250/340**	**NRZ**	**56**	**0.46**	**4.4**	**130**	**0.625**	**0.13**	**1.61**
[49]*	55nm SiGe BiCMOS	330/350	NRZ	96	1.1	5	OC	1	0.13	2.09
[49]*	55nm SiGe BiCMOS	330/350	PAM4	128	1.1	4.4	OC	1	0.1	2.18
[50]	250nm SiGe BiCMOS	190/190	NRZ	40	1.35	6	50	0.25	0.28	1.5
[47]	250nm SiGe BiCMOS	190/190	NRZ	30	1	7.6	OC	1	0.29	1.29
[51]	55nm SiGe BiCMOS	330/350	PAM4	112	0.82	4.8	30**	0	0.21	1.45

Table 4.1: Performance Summary and State-of-the-art Comparison

*Linear drivers. **Assumed to be 30 Ω, number not provided. § Assumes TW-MZM length of 3 mm and VπL = 19 V*mm.

Chapter 5

Optical transmitter equalization with mismatched terminations in a silicon photonic modulator

5.1 Introduction

Traveling-wave, Mach-Zehnder modulators (TW-MZM) are widely employed in optical communications because of the inherent broadband optical response and temperature insensitivity compared to ring-resonator modulators and lower power consumption than segmented MZMs [43]. The potential of silicon photonics (SiPh) for low-cost mass production has driven considerable research interest in SiPh TW-MZMs [52, 53].

As fiber optic link bit rates continue to increase, higher bandwidth SiPh TW-MZMs will be required. Typically, TW-MZMs are the BW bottleneck when they are utilized in intra-data center fiber optic links. The EO BW response of a TW-MZM with a matched

termination is given by [54]:

$$M(f) = e^{-\frac{\alpha L}{2}}[\frac{sinh^2(\frac{\alpha L}{2}) + sin^2(\frac{\xi L}{2})}{(\frac{\alpha L}{2})^2 + (\frac{\xi L}{2})^2}]^{\frac{1}{2}},\ where\, \xi = (n_\mu - n_0)\frac{2\pi f}{c}. \tag{5.1}$$

where n_μ and n_0 are the electrical microwave index and the optical index, respectively. α is the loss coefficient and L is the length of the electrode. f is the electrical frequency and c is the speed of light in vacuum. If the microwave and optical velocities are matched, the expression becomes:

$$M(f) = e^{-\frac{\alpha L}{2}}[\frac{sinh^2(\frac{\alpha L}{2})}{(\frac{\alpha L}{2})^2}]^{\frac{1}{2}} \tag{5.2}$$

and the 3 dB EO BW is the frequency at which the total electrode loss is 6.34 dB. Therefore, to increase the EO BW, the length of the electrodes can be reduced. However, decreasing the length increases the loss of the TW-MZM. The loss in a coherent optical link can be calculated by using the modulation factor (F_M):

$$F_M = \frac{1}{2}(1 - cos(\pi\frac{V_{sig}}{2V_\pi})) \tag{5.3}$$

Where V_{sig} is the peak-to-peak differential drive voltage, and V_π is the differential voltage required to produce a π phase shift in the modulator. The V_π is obtained by dividing the phase efficiency of the PN junction phase shifter, in units of rad/V/m, by the length of the electrode. Hence, there is a loss/BW trade-off associated with the TW-MZM electrode length. Intra-data center optical fiber links typically operate with a very reduced link budget. Therefore, equalization methods that allow for TW-MZM extensions without requiring a reduction in the electrode lengths can be very beneficial.

Electronic-photonic monolithic SiPh processes allow codesign of photonic devices and active circuits and eliminate parasitic capacitances and inductances such as a wirebond inductances. Consequently, mismatched TW terminations can be explored as a band-

width enhancement technique for the optical link. This technique can be employed in the nested TW-MZMs that compose a QPSK modulator, as shown in Fig. 5.1.

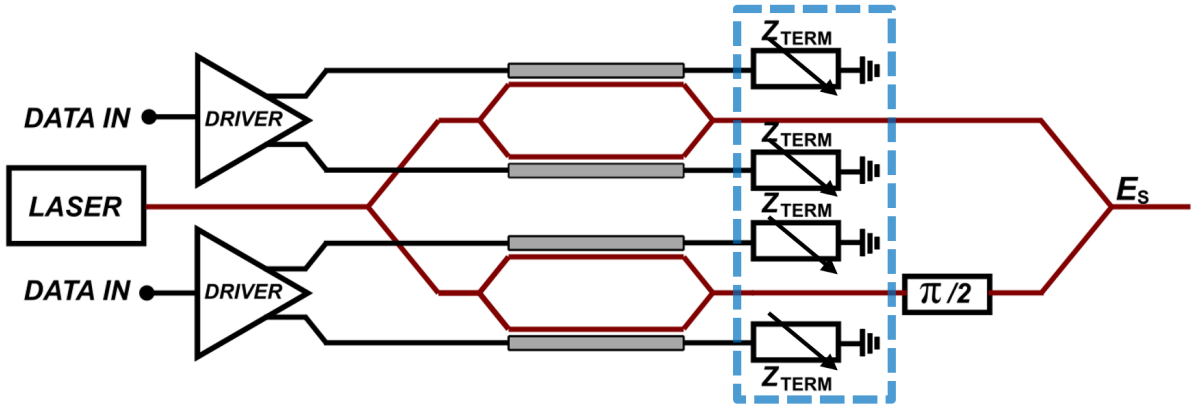

Figure 5.1: Optical QPSK transmitter. The QPSK modulator consists of two nested MZMs, each with a tunable termination.

TW-MZMs are commonly terminated with a resistance (R_{term}) that matches the electrode characteristic impedance Z_0 so that the incident electrical wave is absorbed, and minimal inter-symbol interference (ISI) is generated as no reflected electrical wave will interact with the incoming forward propagating optical wave that corresponds to the following symbols. However, termination mismatch can have a beneficial effect when $R_{term} < |Z_0|$ since a negative real reflection coefficient (Γ) produces inverted reflected waves. This mechanism can be understood by visualiZing a pulse response, as shown in Fig. 5.2. As the leading edge of a forward-traveling electrical pulse (FTEP) arrives at the end of the electrode, an inverted backwards-traveling electrical pulse (BTEP) starts to propagate. The BTEP produces a phase change in the forward-traveling optical pulse (FTOP) that is opposite to the one produced by the FTEP. In the case of a velocity-matched TW-MZM, the leading edge of the FTOP does not interact with the BTEP and the accumulated FTOP phase shift from the BTEP is largest at the trailing edge of the FTOP. This results in a modulated signal with emphasis at the bit transitions.

In this work, a 2.5 mm SiPh TW-MZM with a tunable termination was fabricated

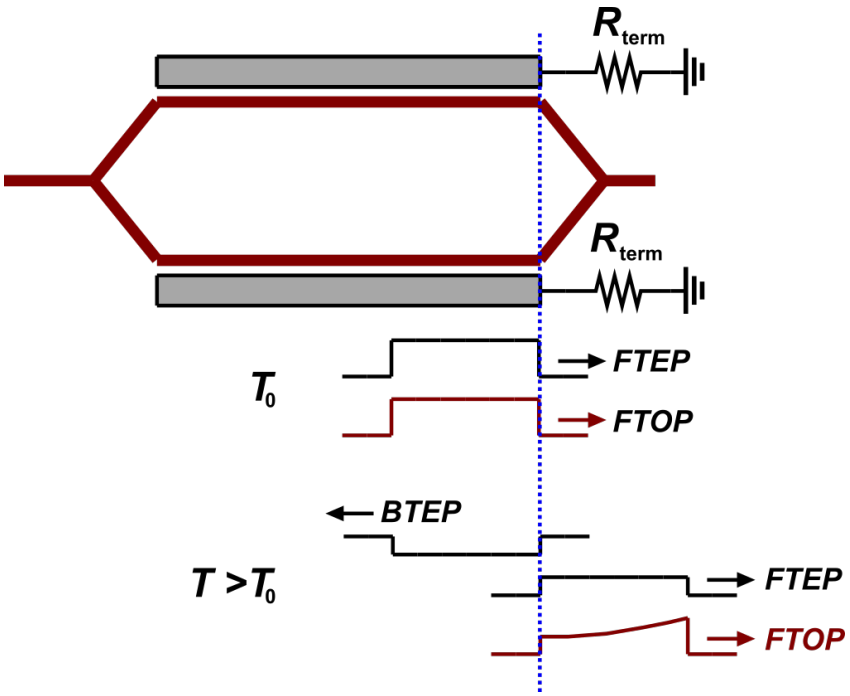

Figure 5.2: Pulse response of a mismatched TW-MZM when $R_{term} < Z_0$. This results in a modulated signal with emphasis at the bit transitions.

in the GlobalFoundries 9WG 90-nm CMOS electronic-photonic monolithic process. The TW-MZM was assembled on a PCB and time-domain reflectometry measurements, EO frequency response measurements, and 50 Gb/s eye-diagrams were taken at different PN junction biases and termination configurations to determine an optimum setting.

A photograph of the PIC is shown in Fig. 5.3 and the PCB assembly of the TW-MZM is shown in Fig. 5.4. Vertical grating couplers are used to couple light into and out of the TW-MZM. The PCB was milled to reduce the length of the RF wirebonds from between PCB and the TW-MZM. 1.2 nF Presidio wire-bondable bypassing capacitors were added to the heater biases. Mini SMP RF connectors rated for up to 65 GHz were used to connect the PCB to the RF test equipment.

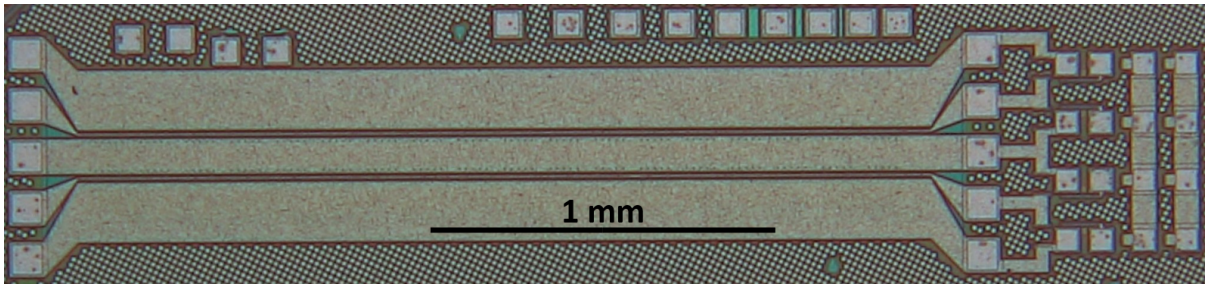

Figure 5.3: Micrograph of the TW-MZM with tunable termination. The SiPh TW-MZM electrodes are 2.5 mm, and have a GSGSG configuration. The RF bond-pads have a pitch of 150 µm.

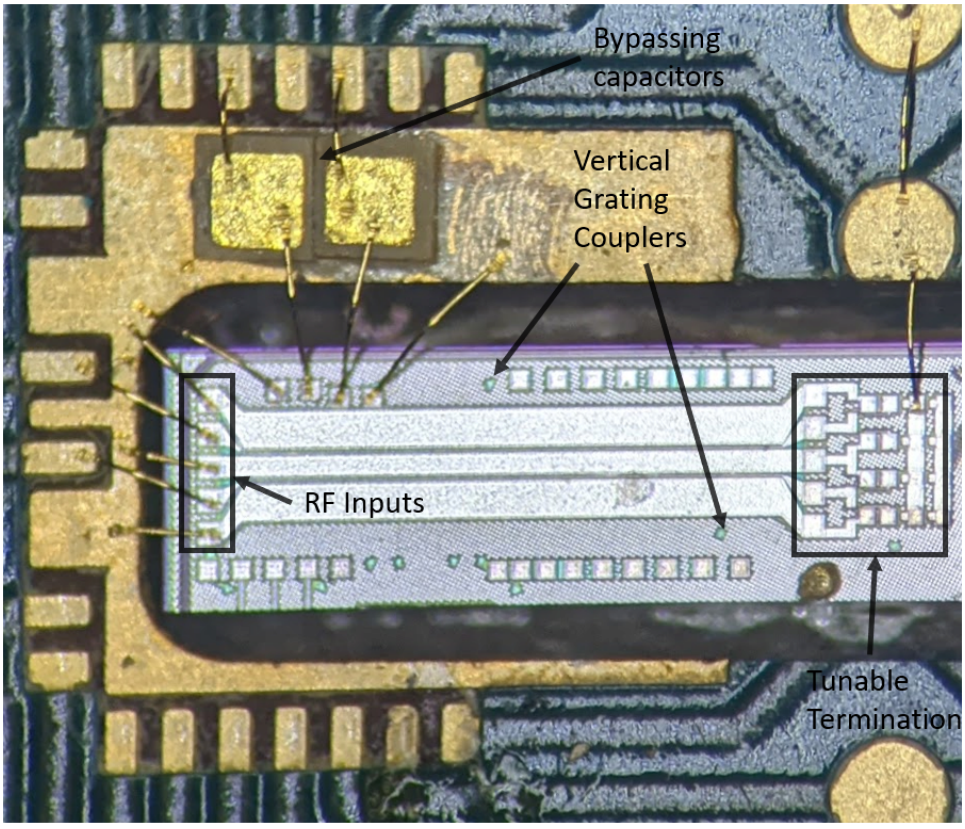

Figure 5.4: Assembly of the TW-MZM on a PCB. The PCB was milled to reduce the length of the RF wirebonds from between PCB and the TW-MZM. 1.2 nF Presidio wire-bondable bypassing capacitors were added to the heater biases.

5.2 Circuit Schematic and Simulations

Fig. 5.5 depicts the schematic of one of the two arms of the GSGSG co-planar waveguide (CPW) TW-MZM with the tunable termination circuit. The TW-MZM phase

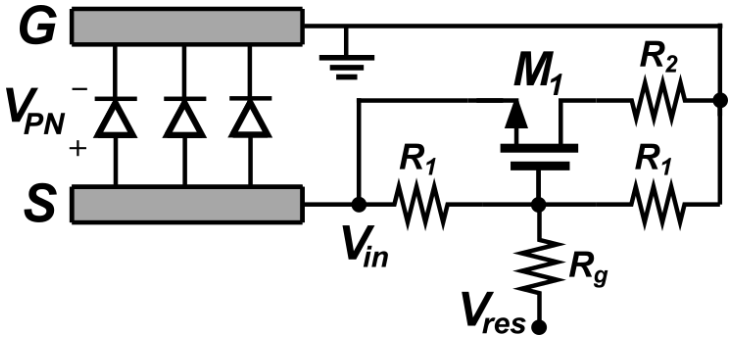

Figure 5.5: Schematic of one of the two arms of the GSGSG CPW with the tunable termination circuit. For each differential input, the phase shifter extends from the signal electrode to one of the two ground electrodes.

shifters are reverse-biased PN junctions that utilize the plasma dispersion effect, whereby the applied voltage changes the carrier concentrations in the waveguide, which modulates the refractive index and produces a phase shift. For each differential input, the phase shifter extends from the signal electrode to one of the two ground electrodes. The electrode widths are 2 µm, 172 µm, and 100 µm for the signal and grounds, respectively. The

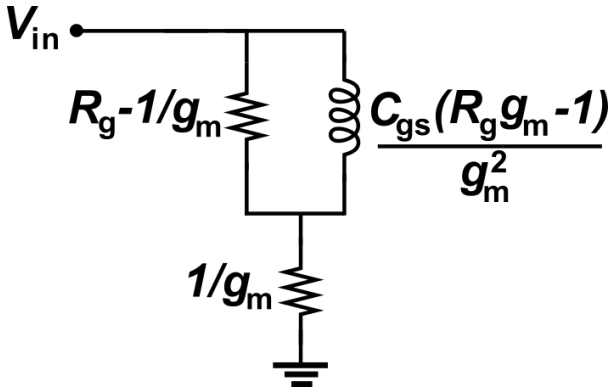

Figure 5.6: Small-signal model of the tunable TW-MZM termination. R_g produces an inductive response in Z_{term}, which results in a termination impedance that increases with frequency.

$V_\pi L$ is 15 V*cm at 2 V reverse bias. The low phase efficiency is due to a modification in the fabrication process. The tunable termination between the signal electrode and each adjacent ground electrode consists of an NFET in series with a 50 Ω resistor (R_2). A parallel branch of 8 kΩ resistors (R_1) provides ESD protection at the NFET gate. The termination impedance (Z_{term}) is determined by V_{res}, which sets the NFET V_{gs}. The gate shunt resistor (R_g) is 2 kΩ. The small-signal model is shown in Fig. 5.6. The small-signal model indicates that R_g produces an inductive response in Z_{term}, which results in a termination impedance that increases with frequency. The simulated Z_{term} vs frequency at various V_{res} values and a fixed V_{PN} of -1.8 V is shown in Fig. 5.7. The inductance

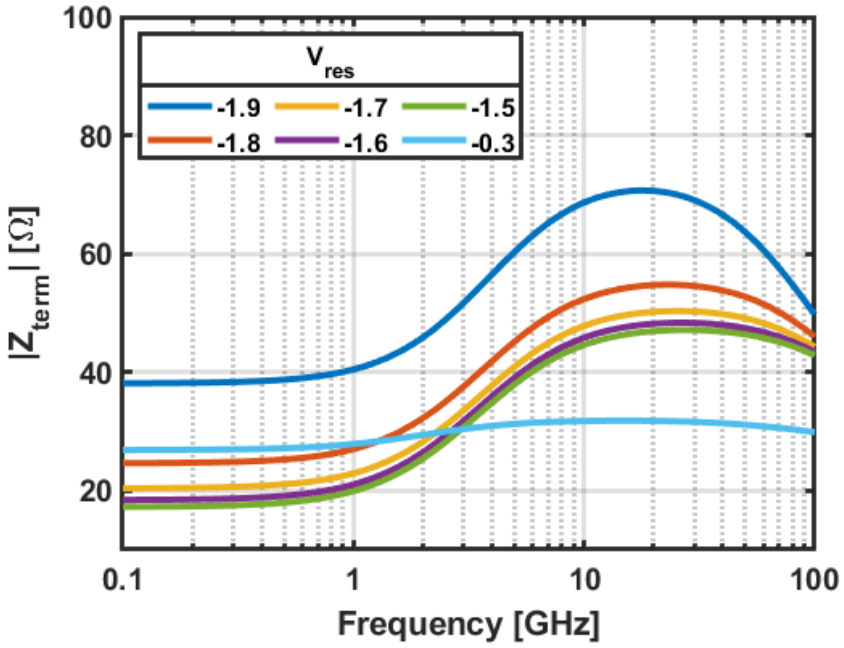

Figure 5.7: simulated Z_{term} vs frequency at various V_{res} values and a fixed V_{PN} of -1.8 V.

is proportional to $1/g_m^2$, so a higher V_{res} value results in a reduced inductance, which reduces the Z_{term} dependence on frequency. In agreement with the small-signal model, at low-frequency, $Z_{in} \sim 1/g_m$ and at high frequency $Z_{in} \sim R_g$, assuming $R_g >> 1/g_m$. The adjustable inductance can be beneficial, since this enables a tunable Γ. The inductance

can be tuned such that at DC $Z_{term} < Z_0$ and at high-frequency $Z_{term} = Z_0$. In this case the bit transitions, which are composed of high frequencies will not be attenuated. In contrast, the long runs of 1s or 0s, which have a low-frequency content, will be reduced in amplitude. This results in a signal with a midband gain that is de-emphasized with respect to the high-frequency gain, which produces a peaked response that can extend the TW-MZM bandwidth. The simulated low frequency Z_{term} vs V_{PN} and V_{res} is shown in Fig. 5.8. The simulated low-frequency termination impedance ranges from approximately 20 Ω to over 300 Ω for $|V_{res}| > 0.5V$.

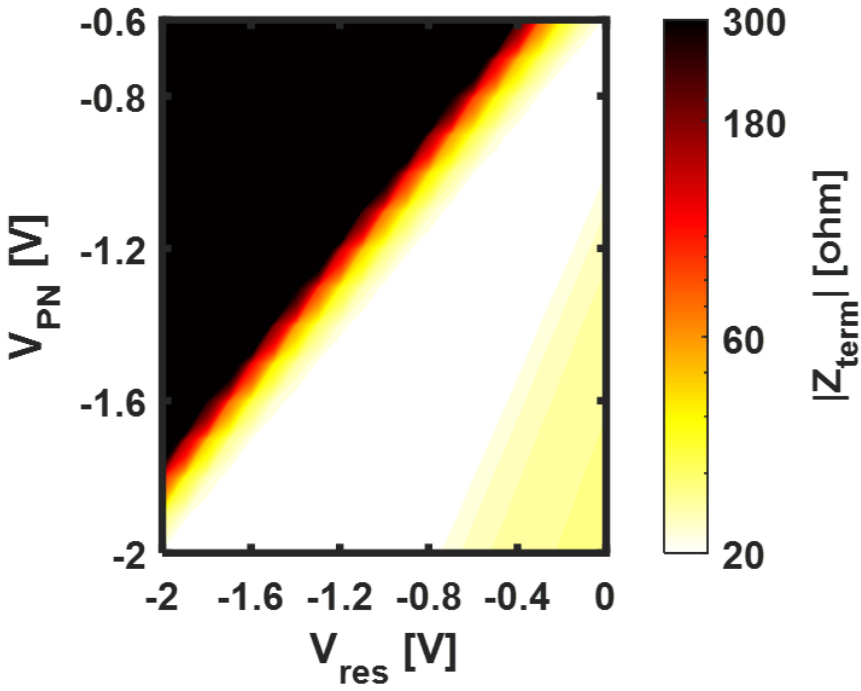

Figure 5.8: Simulated low-frequency Z_{term} vs V_{PN} and V_{res}

5.3 TDR Measurements

In order to characterize the effect of the tunable termination, time domain reflectometry (TDR) measurements were done on the TW-MZM at various PN junction biases and

V_{res} values. The measurements were done using the TDR module of a Tektronix sampling oscilloscope. A voltage step is introduced and the module measures the reflected transient voltage to determine the line impedance over time. The distance can then be calculated by multiplying the time by the known propagation velocity. Fig. 5.9 shows single-ended TDR data for various V_{res} values at a fixed V_{PN} of -1.8 V. The 6 TDR curves are identical from 0 to 350 ps. This segment corresponds to the end of the RF cable, mini-SMP RF connector, PCB transmission line, wirebonds and the TW-MZM electrode. The effect of the tunable termination can be observed after 350 ps. Fig. 5.10 shows a contour plot

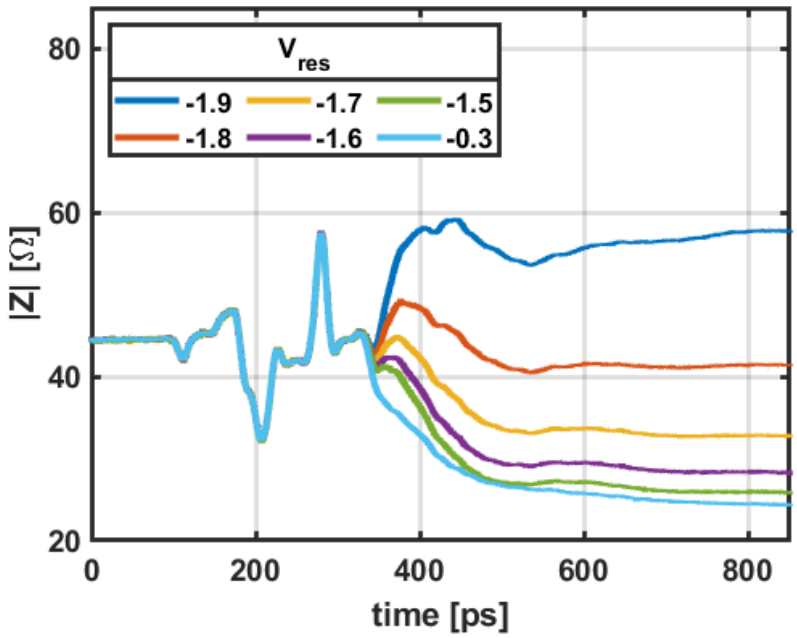

Figure 5.9: Single-ended measured TDR data for various V_{res} values at a fixed V_{PN} of -1.8 V.

of the measured Z_{term} vs V_{PN} and V_{res}. The measured low-frequency Z_{term} agrees with the simulated values, shown in Fig. 5.8. The TW-MZM Z_0 is around 45 Ω. For V_{res} = -1.9 V Z_{term} is significantly higher than the Z_0. As V_{res} is increased, Z_{term} decreases. For V_{res} = -1.8 V, the low-frequency Z_{term} is 40 Ω and it is approximately matched to the TW-MZM. For V_{res} = -0.3 V, the low-frequency Z_{term} is 23 Ω. The response becomes less

inductive with higher V_{gs}, in agreement with the small-signal model and the simulated $Z_{in}(f)$. The blue dashed line in the contour plot indicates the Z_0 at each V_{PN} value. For a V_{PN} of -1.6 V to -0.6 V, Z_{term} ranges from above to below Z_0.

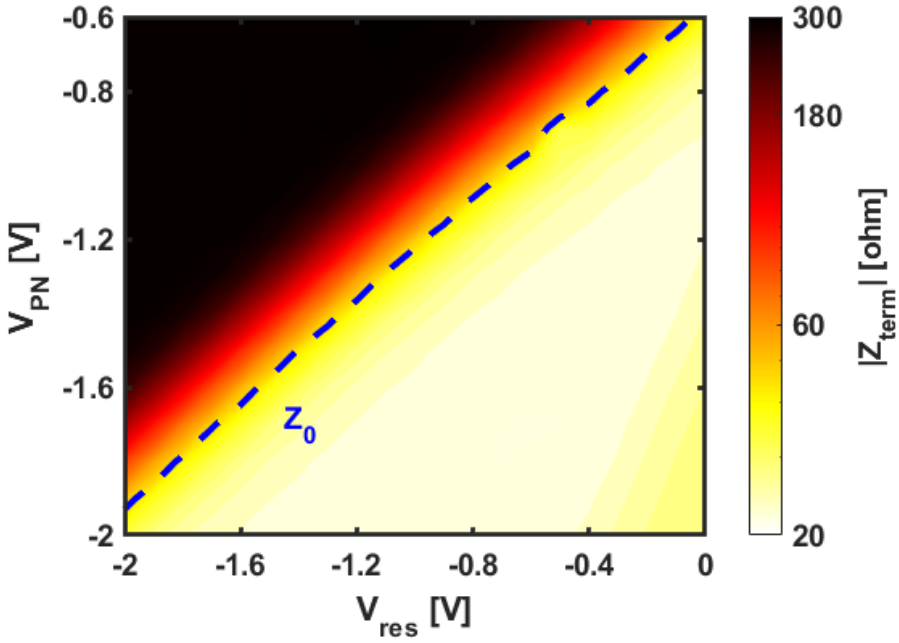

Figure 5.10: Contour plot of the measured Z_{term} vs V_{PN} and V_{res}.

5.4 Frequency Response Measurements

EO frequency response measurements were obtained using an Agilent PNA-X network analyzer rated for up to 67 GHz and a lightwave component analyzer (LCA), which contains a broadband photodiode that is calibrated out of the response. The TW-MZM was biased at quadrature to maximize the RF photocurrent of the LCA PD. The bias point was found to be sensitive to the V_{res} and V_{PN}, so the on-chip heater was adjusted for every V_{res}, V_{PN} pair to maintain the bias at quadrature. In order to minimize the effect of optical reflections the EO frequency response was filtered with an 11-point moving-

average filter. Fig. 5.11 shows the original normalized measured data and the filtered response for one V_{res}, V_{PN} pair. Fig. 5.12 contains the measured EO frequency response

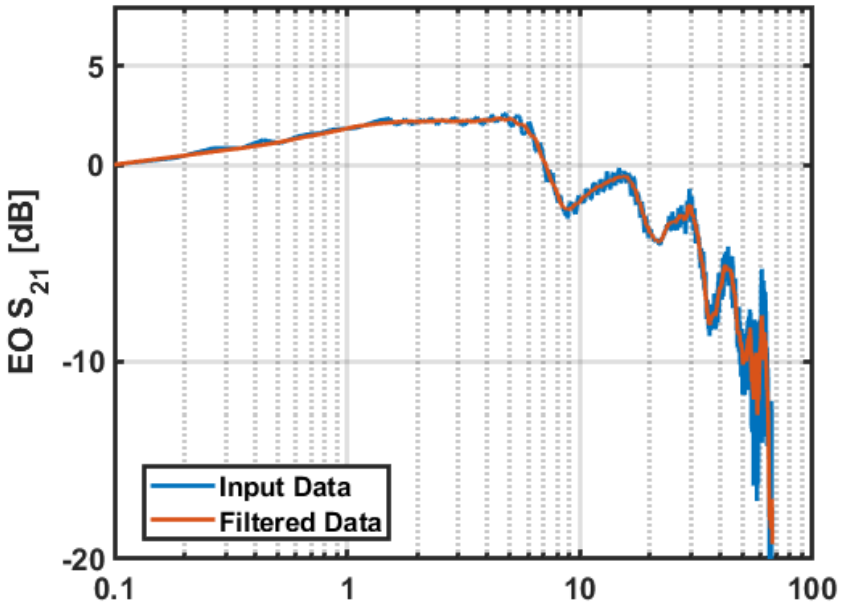

Figure 5.11: Measured and filtered EO frequency response data for one V_{res}, V_{PN} pair.

of the TW-MZM for V_{PN} = -1.8 V at various V_{res} values. A reduction in Z_{term} impacts the transmitter gain since the driver voltage swing is proportional to the parallel driver load resistance given by $R_D = 50\Omega||R_{term}$. The curves are normalized to 0 dB at 100 MHz. For V_{res} = -1.9 V, the detrimental effect of $Z_{term} > Z_0$, which produces positively reflected waves, results in a BW of 300 MHz. As V_{res} is increased to -1.7 V, the BW increases to 19 GHz. At V_{res} = -0.3 V the Z_{term} mismatch increases, and the BW increases to 34 GHz. The contour plot shown in Fig. 5.13 denotes the trend, across the entire V_{PN} range, of EO 3 dB BW enhancement as Z_{term} decreases.

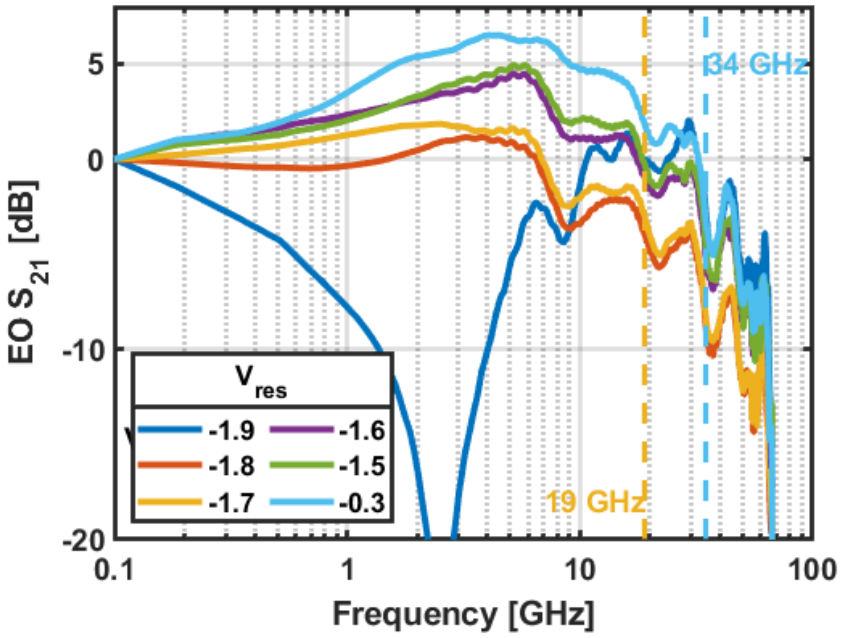

Figure 5.12: Measured EO frequency response of the TW-MZM for V_{PN} = -1.8 V at various V_{res} values. The curves are filtered using an 11-point moving-average filter and are normalized to 0 dB at 100 MHz.

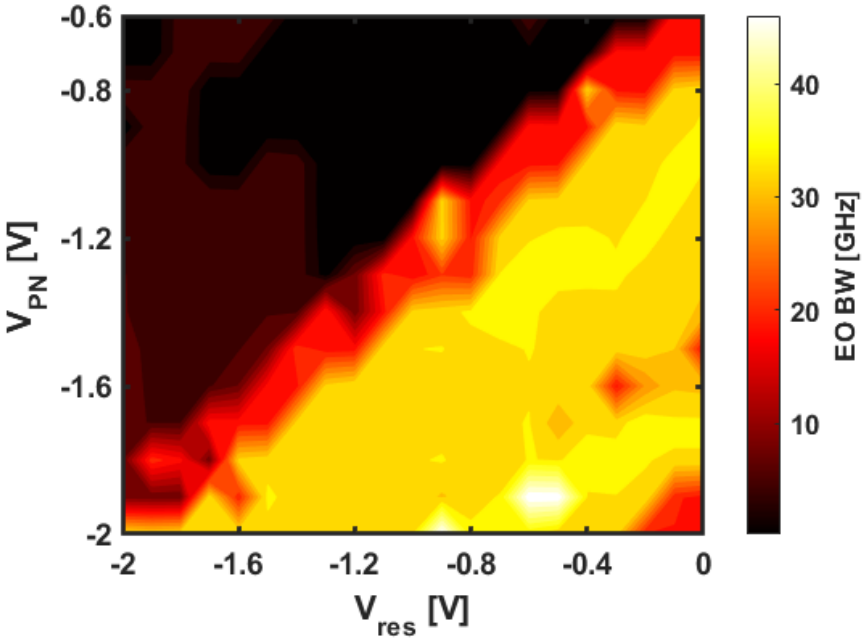

Figure 5.13: Measured TW-MZM 3-dB EO BW vs V_{PN} and V_{res}.

5.5 Time Domain Measurements and Mismatch Optimization

The time-domain measurement setup is shown in Fig. 5.14. A Centellax 50 Ω 4.5 V_{pp} driver and a Finisar receiver rated for 43 Gb/s with integrated limiting amplifiers were used to obtain the time-domain response of the full optical link. An SHF bit-pattern generator (BPG) was used to generate a PRBS7 400 mV_{pp} at the driver input and the receiver output was measured using a Tektronix sampling oscilloscope (SO). The signal was averaged 500 times in the SO by triggering on each PRBS7 word to reduce the effects of random noise on eye closure. This improves the SNR by 27 dB. In addition to improving the SO sensitivity to mitigate the effects of the low TW-MZM phase efficiency, the ISI of the eye is characterized.

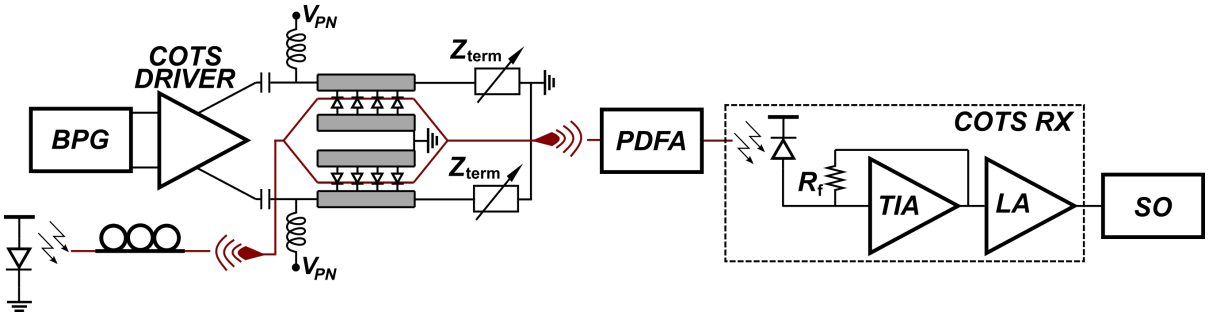

Figure 5.14: Measured TW-MZM 3-dB EO BW vs V_{PN} and V_{res}

Normalized horizontal and vertical eye openings at 50 Gb/s as a function of V_{PN} and V_{res} are shown in Fig. 5.15 and Fig. 5.16, respectively. The contour plots demonstrate the optimal vertical and horizontal eye openings occur with lower Z_{term}. The blue asterisks denote the setting with the largest vertical eye opening: V_{PN} = -1.8 V and V_{res} = -0.3 V, for which Z_{term} = 23 Ω and EO BW = 34 GHz. Compared to a matched 45 Ω termination, the reduced voltage swing for a 50 Ω driver results in a 3.3 dB penalty on the optical link. This modulation penalty is offset by the ISI penalty reduction due to

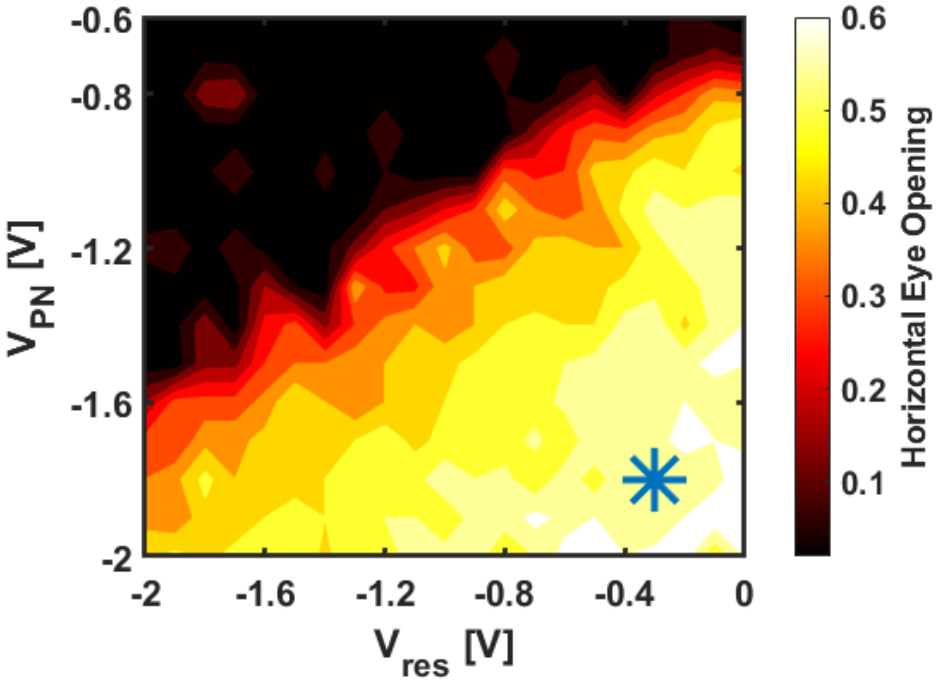

Figure 5.15: Measured normalized horizontal eye-diagram openings.

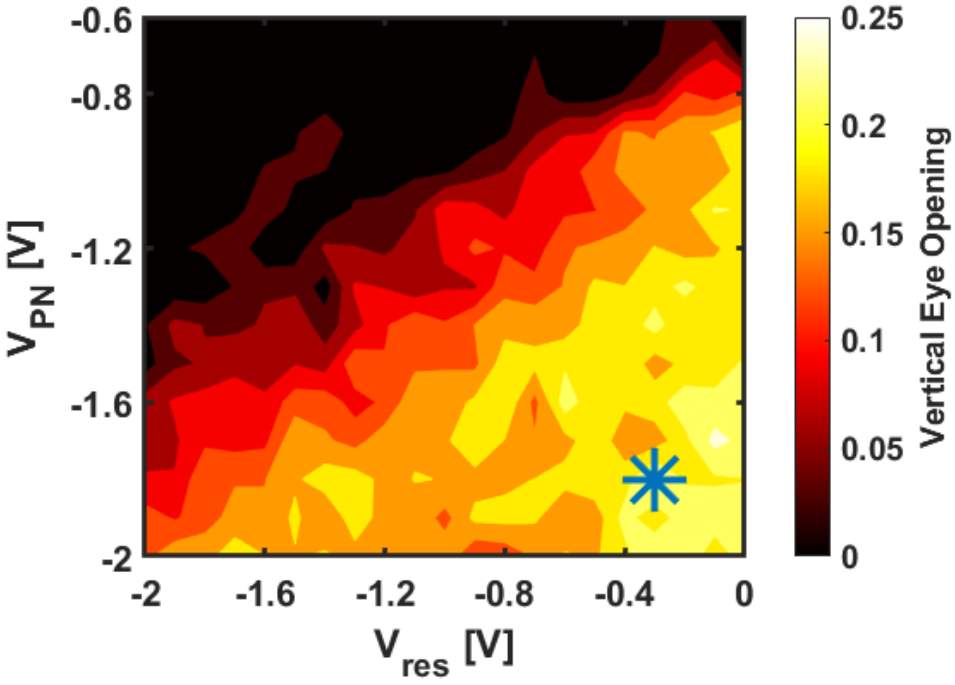

Figure 5.16: Measured normalized vertical eye-diagram openings.

BW enhancement. The power dissipation also increases, as it is inversely proportional to R_{term}. The power can be significantly reduced by enabling only differential termination for which no path to DC ground is required.

Fig. 5.17 a) is the pattern-averaged PRBS7 optical eye-diagram of the Fujitsu reference MZM at 50 Gb/s. The eye was obtained using the Tektronix SO optical sampling module. An electrical eye diagram was measured at the output of the Finisar receiver

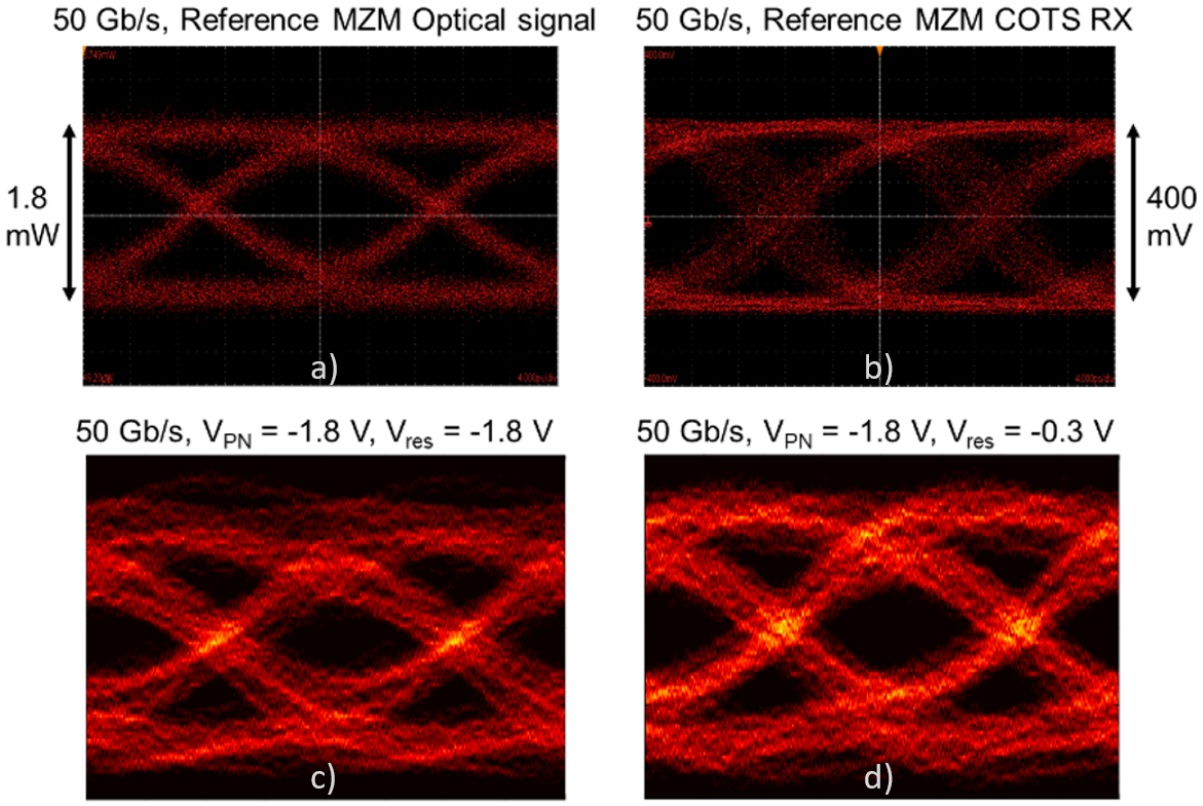

Figure 5.17: 50 Gb/s measured eye-diagrams. a) Optical eye-diagram of the reference MZM, obtained with an optical sampling module. b) Electrical eye-diagram of the reference MZM using a COTS Finisar receiver to an electrical sampling module. Normalized measured eye-diagram of the SiPh TW-MZM for c) V_{PN} = -1.8 V and V_{res} = -1.8 V; d) V_{PN} = -1.8 V and V_{res} = -0.3 V.

show the effect on eye closure produced by the receiver response. This eye-diagram is shown in Fig. 5.17 b). Eye diagrams for V_{PN} = -1.8 V, V_{res} = -1.8 V and V_{PN} = -1.8 V, V_{res} = -0.3 V are shown in Fig. 5.17 c) and 5.17 d), respectively. These measurements

demonstrate the improvement that results from optimizing the termination mismatch.

5.6 Conclusion

This work demonstrates a tunable mismatched termination can produce desirable equalization in an electronic-photonic monolithic process and reach data rates of 50 Gb/s. In TW-MZMs with passive resistor termination, process variations can result in a sub-optimal Γ, which can severely hinder EO performance. Furthermore, eye diagram measurements demonstrate that optimizing termination mismatch minimizes the overall ISI. The optimal mismatch configuration depends on the receiver characteristics. For these reasons, it can be advantageous to have termination tunability.

Chapter 6

Summary and Outlook

In this dissertation I have described how the enormous demand for next-generation power-efficient intra-data center optical links can be achieved by employing analog coherent detection. In our proposed transceiver implementation, the receiver and transmitter circuits account for the majority of dissipated power, which motivates the focus of this work. I then presented various circuit designs and techniques that can be utilized in low-power high-bandwidth analog coherent detection based links.

The advantage of monolithic electronic/photonic integration in optical receivers was described in the context of the transimpedance limit. Three different packaged front-end receiver topologies employing a Cherry-Hooper amplified were designed in IHP's monolithic 250 nm SiGe BiCMOS process, and demonstrated at 50 Gb/s operation with an energy efficiency of 1.08 pJ/bit at bit-error rate below 10^{-10}.

A packaged optical coherent receiver was also presented. The receiver consists of a 90 nm silicon photonics PIC and a 45 nm CMOS EIC. The PIC contains a 90-degree hybrid and high-frequency photodiodes. The receiver consists of an inverter front-end and source-coupled differential-pair limiting amplifiers. The receiver was characterized at up to 50 Gbaud QPSK (100 Gb/s) with a bit-error rate below the HD-FEC limit of

3.8 x 10^{-3}, with an energy efficiency of 0.98 pJ/bit. The on-chip phase-frequency detector and loop filter OpAmp were also briefly described, and a simulated post-layout open-loop phase-locked loop transfer function was obtained. The OPLL has a unity-gain bandwidth of >100 MHz, and a phase and gain margin of 15-degrees and 43 dB, respectively.

A silicon photonics TW-MZM driver, implemented in 130 nm SiGe BiCMOS, was described. Driver bit-error rate bathtub curves and eye-diagrams are shown at 56 Gb/s, with a corresponding energy efficiency of 8.2 pJ/bit. Two driver variants were implemented to evaluate the bandwidth/phase efficiency tradeoff at different modulator PN junction biasing voltages. Various modulator/driver co-design aspects were also discussed, such as the effect of packaging on the transmitter EO BW and group-delay variation, and the relation between the driver-side reflection coefficient and power dissipation for a given voltage swing.

Lastly, a TW-MZM equalization technique based on termination mismatch tuning was explored. Measurements show that the BW can be extended by adjusting the termination impedance well below the characteristic impedance of the electrode. A TW-MZM with tunable termination was implemented in a monolithic electronic/photonic 90 nm CMOS process. TDR measurements demonstrated the tunability of the termination impedance. The EO BW was extended from 19 GHz to 34 GHz by increasing the termination mismatch, and a map of horizontal/vertical eye openings were obtained for a PRBS7 word in order to determine the optimum PN junction bias and impedance mismatch.

6.1 Future Work

This work has described power-efficient high-bandwidth circuit blocks that can be utilized within next-generation intra-data center optical links based on analog coherent detection. The next step is to test the opto-electric receiver in closed-loop. In order

to do that, a receiver PIC with an on-chip tunable laser will be necessary. An interim measurement that can be performed is a closed-loop phase tracking test, as shown in Fig. 6.1, where a phase shifter on the PIC is used as a voltage/current controlled delay that tracks the phase reference signal generated by an external commercial phase modulator.

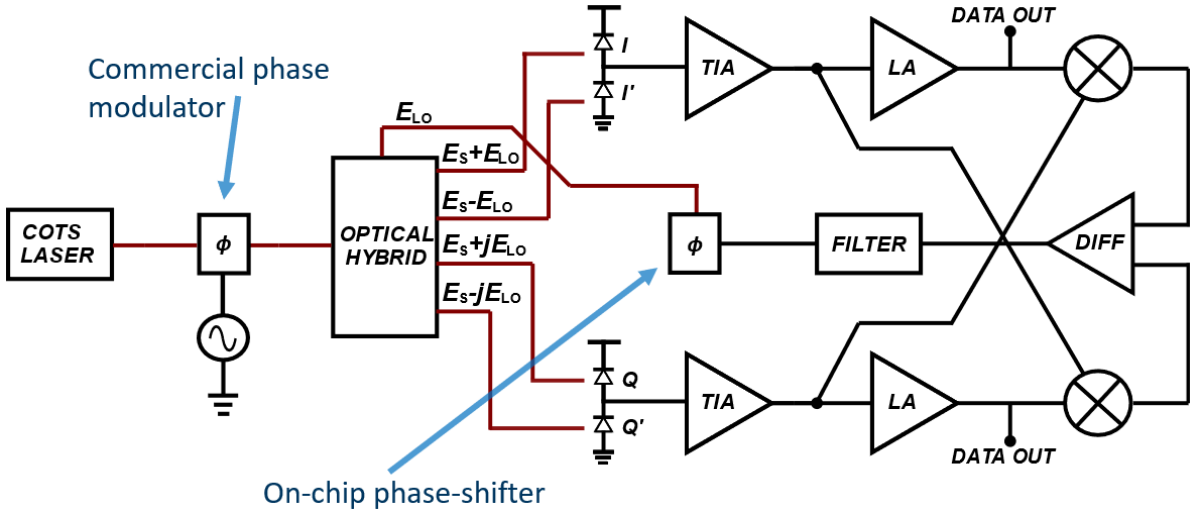

Figure 6.1: Closed-loop phase response test of the coherent receiver described in Chapter 3 using a phase shifter on the PIC. An external commercial phase modulator is used to introduce the reference phase stimulus.

In order to deploy analog coherent detection in the data center, polarization multiplexing will have to be demonstrated. As the signal propagates along the fiber, it undergoes random time-varying polarization rotations which must be compensated for. As theoretically described in [5], the original transmitted state-of-polarization can be recovered by adding a low-frequency pilot tone to one of the quadratures of one of the two transmitted polarizations. Reset-free polarization demultiplexing [55] may eventually be required for mass adoption ACD transceivers.

Perhaps the main challenge that needs to be overcome for ACD to become commercially viable is to implement architectures that do not require a cooled tunable laser. So far, in a research environment, OPLL closed-loop measurements have been done with a

TEC on the local oscillator laser. TECs are prohibitively power-hungry and cannot be employed in a commercial data center. One alternative to the Costas-Loop based OPLL is to transmit an unmodulated carrier on one of the two polarizations. This carrier bypasses the TW-MZM, which can have significant losses, and functions as the local-oscillator at the coherent receiver [56]. Future work can be done to explore such link architectures.

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