Chip-Last HDFO (High-Density Fan-Out) Interposer-PoP

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***Abstract*—Interposer Package-on-Package (PoP) technology was developed and has been in very high-volume production over the last several years for high-end mobile application processors (APs). This is due to its advantages of good package design flexibility, controllable package warpage at room temperature (25°C) and high temperature (260°C), reduced assembly manufacturing cycle time and chip-last assembly manufacturing availability. To date, the laminate-substrate based interposer-PoP has been employed for high-end mobile APs with very high-volume production. Recently, this interposer-PoP design has faced some technical limitations including the need to reduce: top and bottom routing layer thickness, copper (Cu) trace line/space and via size for next generation mobile APs. These reductions may require ultra-thin package z-height and high-bandwidth bottom and top routing layers. To address these challenges, a new interposer-PoP with High-Density Fan-Out (HDFO) redistribution layer (RDL) routing layer has been designed and demonstrated. It is part of an initiative to achieve an ultra-thin package z-height, interposer-PoP structure with high bandwidth and improved signal integrity/power integrity (SI/PI) routing layer using a chip-last assembly manufacturing process flow. This paper will discuss package-level characterizations on the interposer-PoP with HDFO RDL routing layer as well as package z-height evaluation, temperature-dependent package warpage measurements and package-level reliability tests conducted in accordance with JEDEC.**

Keywords—Interposer-PoP, HDFO RDL routing layer, ultra-thin package z-height, controllable package warpage, fine copper(Cu) trace line/space and via, chip-last assembly manufacturing

I. INTRODUCTION

The key technical requirements for continued Package-on-Package (PoP) success includes: thin package height capability to improve application processor (AP) systems z-form factor where the memory package is stacked on the top of PoP and achieve controllable package warpage at room temperature (25°C) and at high temperature (260°C) to improve memory package stacking yield and PoP board to surface mount technology (SMT) yield. Also, fine copper (Cu) trace line/space (L/S) and fine via routing layers are increasingly required for high bandwidth and improved signal integrity/power integrity (SI/PI) to accommodate logic AP die or future split-die integration. To satisfy these objectives, a chip-last assembly manufacturing process-flow is strongly prefered to minimize known good die (KGD) loss issues.

Figure 1 shows the typical package height trends and package routing layer Cu trace line width trends of the laminate-substrate based PoP and the fan-out redistribution layer (RDL) based PoP over the last nine years for the high-end mobile APs. Recent laminate-substrate based PoP package height in high volume production is roughly 0.6~0.5-mm and Cu trace line width is around 10~8-µm. RDL-based PoP package height in high volume production is roughly 0.38~0.36-mm and Cu trace line width is around 8~7-µm.

Figure 1 also shows some estimates on future requirements for next generation mobile APs area: 0.40~0.34-mm PoP height and 4~2-µm PoP routing layers line width. Consequently, RDL routing layer technology is highly considered as one of the key initiatives to meet the future PoP technical requirements. RDL routing with ultra thin and 2/2-µm line/space are already used for volume production. PoP package options that have been in very high-volume production for high-end mobile APs include: the laminate-substrate based flip chip Through Mold Via

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(fcTMV®) package (since 2012), the laminate-substrate based interposer-PoP (since 2014) and fan-out RDL based PoP (since around 2016) [1, 3]. Among them, laminate-substrate based interposer-PoP brought many technical benefits [1, 2]. By integrating separate laminate-substrate interposer on the die back side (top side) as an electrical interface to memory packages and, at the same time, electrically connecting it to the die front side (bottom side) laminate-substrate routing layer, better package design flexibility can be achieved. This design can accommodate various memory products having different memory ball grid array (BGA) terminal input/output (I/O) arrays and count, while providing a better supply chain for memory sourcing compared to non interposer-PoP designs.

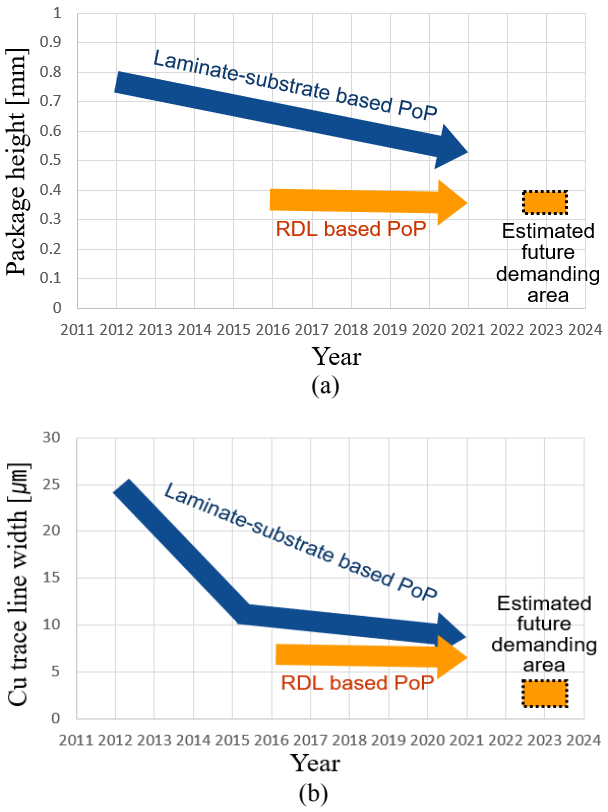


Figure 1. Typical PoP (a) height [nominal] and (b) Cu trace line width trends over the last nine years for high-end mobile APs and estimated future demanding area in PoP height and PoP routing layer Cu line width for next generation mobile APs.

The top and bottom laminate-substrate routing layer sandwich structure has proven to help manage PoP package warpage at room (25°C) and high (260°C) temperatures. Also, the top-side laminate-substrate interposer could be manufactured concurrently with the bottom-side laminate-substrate routing layer to shorten overall PoP assembly manufacturing cycle time. Importantly, with the assembly manufacturing proces-flow of the laminate-substrate based interposer-PoP, chip-last assembly manufacturing, which is strongly prefered to minimize known good die (KGD) loss during assembly, is available. It is achieved by conducting automated optical inspection (AOI) or electrical open/short (O/S) probe-testing to both the bottom laminate-substrate routing layer and the top laminate-substrate interposer routing layer, respectitively, prior to assembly.

By the way, recently, the laminate-substrate based interposer-PoP is increasingly expected to face technical limitations in reducing overall PoP package height further, considering current laminate-substrate dielectric and Cu conductor layer thickness reduction capabilities and the projected roadmap. Also, it is expected to have limitations in reducing Cu conductor trace line/space width and via size further for better bandwidth and SI/PI that might be increasingly required for next generation or advanced mobile APs.

To overcome the challenges, two interposer-PoPs with High-Density Fan-Out (HDFO) RDL routing layer instead of laminate-substrate routing layer will be discussed with the aim of leveraging the advantages of both interposer-PoP structure and process-flow (where chip-last assembly manufacturing and shortening assembly manufacturing cycle time are available) and HDFO RDL routing layer technology (where ultra-thin dielectric and Cu conductor layer and better bandwidth and SI/PI are available) for next generation mobile APs. For the two interposer-PoPs, the first is composed of bottom RDL routing layer and top RDL interposer routing layer and the second one is composed of bottom RDL routing layer and top laminate-substrate interposer routing layer. Both have been designed, demonstrated and characterized. The key features of the two interposer-PoPs with HDFO RDL routing layer will be compared.

II. Construction and Process-Flow

In this section, the package-construction and its process-flows for the two interposer-PoPs with HDFO RDL are discussed.

A. Interposer-PoP with bottom RDL and top interposer RDL

Figure 2 (a) shows a schematic diagram illustrating the interposer-PoP with bottom RDL routing layer and top interposer RDL routing layer. It has a 3-layer RDL for the bottom routing layer and 1 or 2-layer RDL for the top interposer routing layer. With high bandwidth and improved SI / PI, it can be applied to accommodate logic AP single die or future split dies and to integrate various memory products on the top of the PoP. With this structure, an ultra-thin PoP package height (< 380 μm including BGA ball height) can be achieved owing to the ultra-thin bottom and top RDL routing layer thickness, since bottom and top routing layer thicknesses are key contributor in reducing PoP height. Figure 3 (a) is a cross-sectional micrograph of ultra-thin 35~32-μm thick bottom 3-layer RDL routing layer and the Figure 3 (b) micrograph is an example of 2/2-μm line/space RDL Cu conductor trace which is available now for volume production.

The following shows one of the assembly process-flows for interposer-PoP with bottom RDL routing layer and top interposer RDL routing layer.

- Bottom RDL routing layer and top interposer RDL routing layer manufacturing and inspection.
- Mass Reflow (MR) bonding and under-fill or thermocompression with non-conductive paste (TCNCP) bonding for chip attachment on the bottom RDL routing layer (refer to Figure-4).
- Top interposer RDL routing layer solder joint interconnection to bottom RDL routing layer by thermocompression (TC) bonding tall Cu pillar or Cu-core solder ball.
- Transfer molding, BGA ball attachment and package singulation.

Figure 4 is a cross-sectional micrograph of daisy chain die, Cu pillar interconnected to the bottom RDL routing layer (a) by mass reflow bonding and (b) by TCNCP bonding. Since the bottom RDL routing layer and top RDL routing layer could be manufactured separately in parallel, a shortened assembly manufacturing cycle time over sequential RDL build-up type PoPs could be achieved. Also, with the assembly manufacturing process-flow, chip-last assembly manufacturing using known good bottom RDL routing layer and known good top RDL routing layer can be realized.

B. Interposer-PoP with bottom RDL and top interposer laminate-substrate

Figure 2 (b) is a schematic diagram illustrating interposer-PoP with bottom RDL routing layer and top interposer laminate-substrate routing layer. The 3-layer RDL for the bottom routing layer with high bandwidth and improved SI/PI can be used to accommodate a logic AP single die or future split dies. Also, a 2-layer laminate-substrate for the top interposer routing layer can be applied to integrate various memory products. This structure achieves a thin PoP package height (less than 420 µm) due to the ultra-thin bottom RDL routing layer, which is 35~32-µm thick, as shown in Figure 3 (a) and due to a top laminate-substrate routing layer, which is around 90-µm thick, as shown in Figure 3 (c).

The following is one of the process flows for the interposer-PoP with bottom RDL routing layer and top interposer laminate-substrate routing layer.

- Bottom RDL routing layer and top interposer laminate-substrate routing layer manufacturing and inspection.
- Mass reflow bonding and under-fill or TCNCP bonding for chip attachment on bottom RDL routing layer (refer to Figure 4).
- Top interposer laminate-substrate routing layer solder joint interconnection to bottom RDL routing layer by TC bonding tall Cu pillar or Cu-core solder ball.
- Transfer molding, BGA ball attachment and package singulation.

Since the bottom RDL routing layer and top laminate-substrate routing layer could be manufactured separately in parallel, the assembly manufacturing cycle time can be reduced over sequential RDL build-up type PoPs. Also, with the assembly manufacturing process flow, chip-last assembly manufacturing can be achieved by using a known good bottom RDL routing layer and a known good top interposer laminate-substrate routing layer. The interposer-PoP with bottom RDL routing layer and top laminate-substrate routing layer is expected to have better mechanical robustness or rigidity over fully RDL-based PoPs due to the properties of the laminate-substrate dielectric layer that has good mechanical robustness and is reinforced by glass fabric.

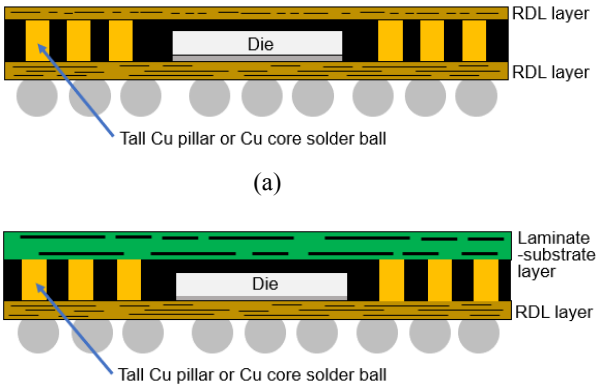
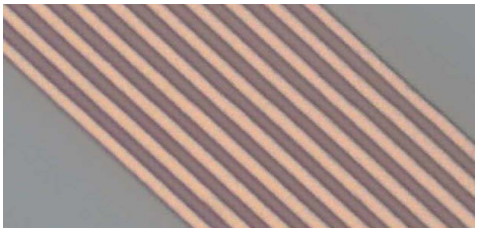
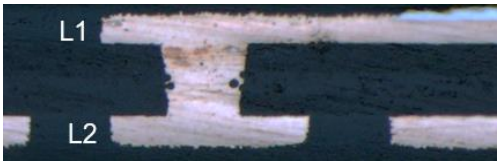


Figure 2. Schematic diagrams of (a) the interposer-PoP with bottom RDL and top RDL and (b) interposer-PoP with bottom RDL and top laminate-substrate.

(a)

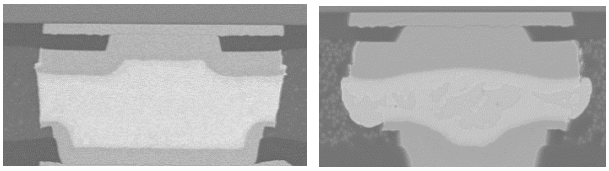


(b)



(c)

Figure 3. Micrographs of (a) a cross-section of an ultra-thin bottom 3-layer RDL, (b) an example of RDL Cu trace 2/2-µm line/space and (c) a cross-section of a 90-µm thick top interposer 2-layer laminate-substrate.



(a) (b)

Figure 4. Cross-sectional micrographs of daisy chain die Cu pillar interconnected to bottom RDL routing layer by (a) mass reflow bonding and (b) TCNCP bonding.

III. Package Z-Height

As shown in Figure 1, PoP package height reduction has been constantly occurring over the last decade in the industry since PoP height has a critical impact on mobile AP system z-height and might have an influence on thermal performance of PoP [4]. As discussed earlier, currently, the laminate-substrate based interposer-PoP is expected to face limitations in reducing package height below 450-µm considering current laminate-substrate thickness reduction progress and its thickness roadmap. Replacing the laminate-substrate routing layer with an RDL routing layer for interposer-PoP can overcome this challenge to achieve less than 400-µm package height. This section evaluates and addresses the package height performance of both interposer-PoP with bottom RDL routing layer and top RDL routing layer and interposer-PoP with bottom RDL routing layer and top laminate-substrate routing layer (see Figure 5).

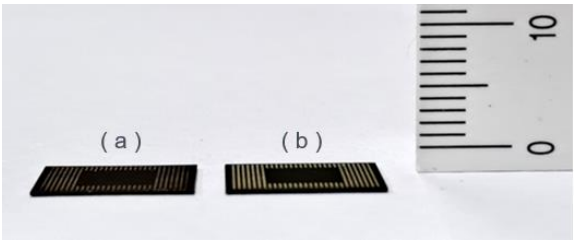
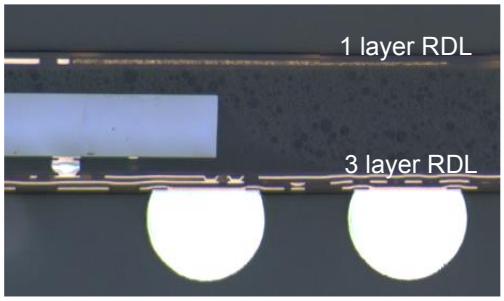


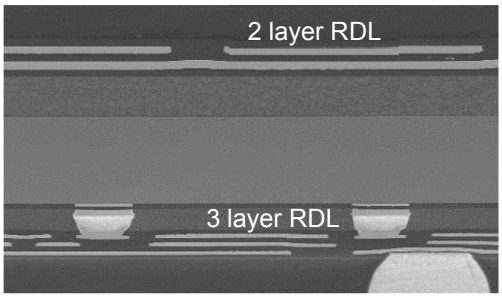
Figure-5. A package external photo of interposer-PoP: (a) with bottom RDL and top RDL (b) with bottom RDL and top laminate-substrate.

A. *Package height of interposer-PoP with bottom RDL and top RDL*

Figure 6 (a) is a cross-sectional micrograph of the interposer-PoP with a bottom 3-layer RDL routing layer and a top 1-layer RDL routing layer. It is around 360-µm in package height including BGA ball height, resulting from a combination of 32-µm thick bottom 3-layer RDL routing layer and 22-µm thick top 1-layer RDL routing layer. Figure 6 (b) is a cross-sectional micrograph of the interposer-PoP with a bottom 3-layer RDL routing layer and a top 2-layer RDL routing layer. It is around 375-µm in package height including BGA ball height, resulting from a combination of 32-µm thick bottom 3-layer RDL routing layer and 34-µm thick top 2-layer RDL routing layer. Both interposer-PoPs are less than 400-µm in package height which could provide an attractive package height for next generation mobile APs.



(a)



(b)

Figure 6. Micrographs of (a) cross-section of interposer-PoP with bottom 3-layer RDL and top 1-layer RDL and (b) interposer-PoP with bottom 3-layer RDL and top 2-layer RDL.

B. *Package height of interposer-PoP with bottom RDL and top laminate-substrate*

Figure 7 is a cross-sectional micrograph of the interposer-PoP with bottom 3-layer RDL routing layer and top 2-layer laminate-substrate routing layer, resulting from a combination of 32-µm thick bottom 3-layer RDL routing layer and 90-µm thick top 2-layer laminate-substrate routing layer. It is around 400-µm in package height including BGA ball height, which a fully laminate-substrate interposer-PoP has difficulty achieving. As a future plan for this interposer-PoP structure, an 80-µm thick laminate-substrate needs to be considered and discussed to reduce package height further by reducing laminate-substrate core layer and solder mask thickness.

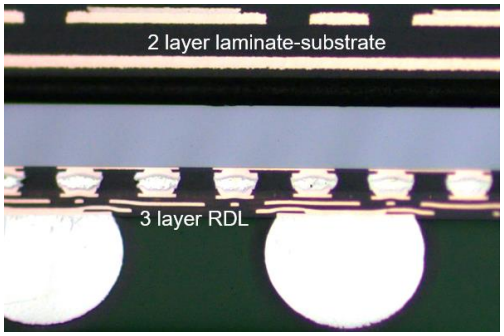


Figure 7. A cross-sectional micrograph of an interposer-PoP with bottom 3-layer RDL routing layer and top 2-layer laminate-substrate routing layer.

IV. Package Warpage

As the PoP package height gets thinner and thinner, controlling package warpage has become more challenging. Therefore, a lot of evaluations or tunings to control PoP package warpage at room temperature (25°C) and high temperature (260°C) have been tried to each new PoP product or design. By the way, interposer-PoP manufactured by interconnecting bottom routing layer and top interposer routing layer, and then by molding the gap between the bottom routing layer and top interposer routing layer which is like sandwich structure is expected to be a better package option in controlling PoP package warpage by balancing bottom routing layer features and top interposer routing layer features than over-mold structure PoP packages or sequential one side RDL build-up style PoP packages. In this section, time-dependent package warpage measurements conducted on the two interposer-PoPs with bottom RDL and top interposer RDL and with bottom RDL and top interposer laminate-substrate are discussed.

A. Interposer-PoP with bottom RDL and top RDL

The time-dependent package warpage measurements of a 12.5 x 12.5-mm body size interposer-PoP with bottom RDL routing layer and top interposer RDL routing layer were conducted. Figure 8 shows the results. This design showed +125-µm package warpage at 25°C with a cry package warpage mode and -56-µm package warpage at 260°C with a smile package warpage mode.

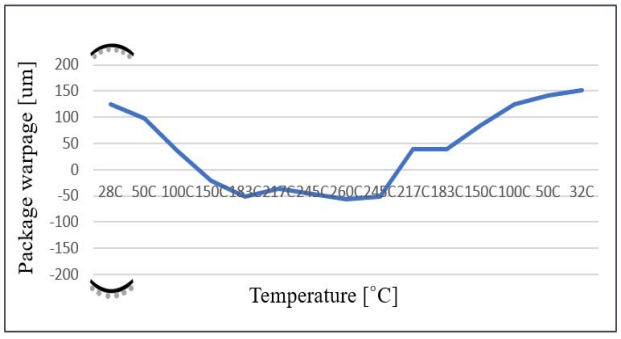


Figure 8. A time-dependent package warpage behavior and value of the interposer-PoP with bottom RDL routing layer and top interposer RDL routing layer.

B. Interposer-PoP with bottom RDL and top laminate-substrate

The time-dependent package warpage measurements of a 12.5 x 12.5-mm body size interposer-PoP with bottom RDL routing layer and top interposer laminate-substrate routing layer were performed. Figure 9 shows the results. This design showed +86-µm package warpage at 25°C with cry package warpage mode and -16-µm package warpage at 260°C with smile package warpage mode.

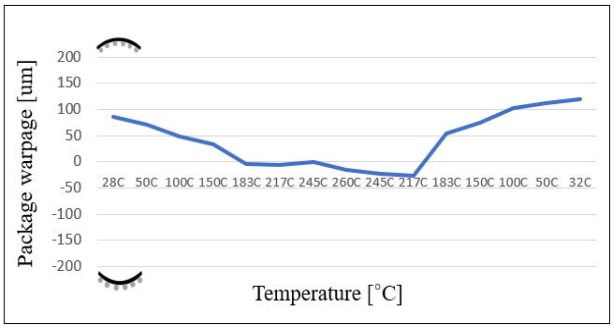


Figure 9. A time-dependent package warpage behavior and values of the interposer-PoP with bottom RDL routing layer and top interposer laminate-substrate routing layer.

Interposer-PoPs with bottom RDL and top interposer RDL, and with bottom RDL and top interposer laminate-substrate showed feasible package warpage behavior and value. Of course, further package warpage optimization or tuning could be considered by balancing the bottom routing layer features and top interposer routing layer features.

V. Reliability Test

To evaluate the package-level reliability performance of the interposer-PoP with bottom RDL and top RDL and interposer-PoP with bottom RDL and top laminate-substrate designs, reliability tests on a 12.5 x 12.5-mm body size daisy chain test vehicle were performed. These tests included unbiased high accelerated stress test (UHAST), temperature cycling (TC) test condition-B and high temperature storage (HTS) test with preconditioning. Table 1 presents the results of the tests on both interposer-PoPs. All samples passed the reliability tests.

Table 1. Package level reliability test items and its results on: (a) the interposer-PoP with bottom RDL and top RDL and (b) the interposer-PoP with bottom RDL and top laminate-substrate.

Reliability Test Items	Sample Size	Results
Pre-conditioning + UHAST (130°C / 85%RH for 96hrs)	33 units	Passed

Pre-conditioning + TC-B (-55 ~ 125°C, 1000x)	33 units	Passed
HTS (150°C for 1000hrs)	33 units	Passed

(Pre-conditioning: 30°C/60% RH for 192 hrs+260°C reflow 3x)

(a)

Reliability Test Items	Sample Size	Results
Pre-conditioning + UHAST (130°C / 85%RH for 96hrs)	33 units	Passed
Pre-conditioning + TC-B (-55 ~ 125°C, 1000x)	33 units	Passed
HTS (150°C for 1000hrs)	33 units	Passed

(Pre-conditioning: 30°C/60% RH for 192 hrs+260°C reflow 3x)

(b)

VI. SUMMARY

In summary, this work discussed the design, demonstration and evaluation of two interposer-PoPs with HDFO RDL routing layers with the goal of targeting next generation mobile AP or advanced 3D System-in-Package (SiP) designs requiring ultra-thin package z-height, high bandwidth and improved SI/PI routing layer. A comparison between the two interposer-PoPs is summarized and highlighted in Table 2. Based on the results, both interposer-PoPs with HDFO RDL showed promising package z-height, feasible package warpage, the possibility for a high bandwidth routing layer and the capability for assembly cycle time reduction and chip-last assembly manufacturing process-flow. All of these factors make either approach suitable for next generation mobile AP or advanced 3D SiP designs.

Table 2. Comparison between interposer-PoP with bottom RDL and top interposer RDL and interposer-PoP with bottom RDL and top interposer laminate-substrate.

	Interposer-POP with bottom RDL and top RDL	Interposer-POP with bottom RDL and top laminate-substrate
High bandwidth bottom routing layer for die split	Available	Available
Package height including BGA	385~350 um	410~ 390 um
Package warpage	Feasible	Feasible
Chip-last assembly	Available	Available
Assembly cycle time reduction	Available	Available

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