UNIVERSITY OF CALIFORNIA, SAN DIEGO

GaN-based Microwave Power Varactors for Wireless Base Station Applications

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Applied Physics)

by

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2013

The Dissertation of Wei Lu is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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2013

DEDICATION

To my beloved wife Wen Qiao.

EPIGRAPH

There are no secrets to success. It is the result of preparation, hard work, and learning from failure.

Colin Powell

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Section 3.4, is a rearrangement of the paper “Effects of surface micromesas on reverse leakage current in InGaN/GaN Schottky barriers,” Wei Lu, Tomoaki Nishimura, Lingquan Wang, Tohru Nakamura, Paul K. L. Yu, and Peter M. Asbeck, J. Appl. Phys., vol. 112, pp.044505, Aug. 2012. The dissertation author was the primary author of the paper.

Section 4.3, is a rearrangement of the paper “InGaN/GaN Microwave Varactors with High *Q*, High-Breakdown Voltage and High Linearity,” Wei Lu, Lingquan (Dennis) Wang, Siyuan Gu, David P. R. Aplin, Paul K. L. Yu, and Peter M. Asbeck, in Semiconductor Device Research Symposium (ISDRS), 2011 International,

IEEE, College Park, MD, 7-9 Dec., 2011. The dissertation author was the primary author of the paper.

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PUBLICATIONS

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FIELD OF STUDY

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ABSTRACT OF THE DISSERTATION

GaN-based Microwave Power Varactors for Wireless Base Station Applications

by

Wei Lu

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Professor Paul K. L. Yu, Chair
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With the development of wireless communication systems, the demand for providing tunability in the wireless communication circuits becomes more and more intense. Among the technologies, semiconductor varactor is the critical component that is capable of implementing tunable and adaptive characteristics, particularly for the frond-end components of the wireless communication systems. For base station applications, high voltage handling capability, typically of 100 V or greater, high

quality factor (Q), typically of above 100 at operation frequency, and high linearity, OIP3 > 65 dBm, are required. This work will mainly discuss in detail the design, fabrication and characterization to achieve the high-voltage high-Q and high-linearity microwave power varactors for wireless base station applications. Some preliminary varactor applications in the test tunable circuits will be demonstrated too.

In this dissertation, we first introduce the physics of the semiconductor varactors and the motivation for choosing GaN as the candidate material for this microwave power varactor. Then we elucidate the critical design considerations for achieving high breakdown voltage, high quality factor and high linearity. The novel Schottky barrier engineered design using a thin InGaN surface layer on top of GaN to enhance the breakdown voltage of GaN-based Schottky diodes is therefore introduced. We then show the theoretical and experimental studies on the suppression mechanisms for electron tunneling in the InGaN/GaN Schottky barriers. The detailed material characterization for the InGaN/GaN material system and its application for the enhancement-mode HEMTs are also presented. Next, we discuss the initial device fabrication procedure and the improving methods based on the initial DC and RF measurement results. Thereafter, we report the detailed characterizations of the fabricated devices including the high-voltage I-V and C-V, S-parameters for 1-port and 2-port devices, linearity and application in the tunable resonant circuits. Finally, we summarize the dissertation and outline the future work.

In this work, we achieved a high-performance GaN-based microwave power varactors with breakdown voltage > 100 V, quality factor > 100 and OIP3 > 71 dBm. It meets the initial goal of this project as well as the specifications in some practical

applications. To the best of our knowledge, this combination of breakdown voltage, *Q* and OIP3 represents remarkable advancement from any other reported varactors.

Chapter 1

Introduction

1.1 Introduction to varactors

Future generations of wireless base station systems need to respond to a wide variety of requirements concerning carrier frequency, output power, modulation bandwidth and peak-to-average ratio. To meet these requirements, the base stations need to be much more adaptive than they are at present. It is envisioned that the carrier frequency should be able to be controllably varied over a wide spectral range, to make use of different channels and different bands. The characteristics of the amplifiers should also be controllably variable in order to adapt to different environments and different specifications, such as output power level, antenna condition, and linearity specifications. Such adaptation requirements can provide new levels of performance to base stations utilizing the architecture currently in use; and even greater benefits can be obtained with future architectures based on software defined radio concepts, where a single RF front-end, under software control, can meet the requirements for all bands and signaling formats. Cognitive radio is a further development of this idea, in which "white spaces" in the RF spectrum are identified and utilized for opportunistic

transmissions. To permit this adaptability while maintaining satisfactory performance of high RX (receive) input sensitivity and high TX (transmit) output efficiency, very high performance tunable microwave filters and matching networks are required. In turn, new enabling components are needed in order to provide this tunability. One of the most promising avenues is to develop tunable capacitors (or varactors). For base station applications, however, the varactors must be able to handle very high voltage levels (peak RF voltages above 100 V), have very high *Q* (greater than 100), and have very high linearity. This combination of specifications has not been obtainable to date with available technologies - which include semiconductor varactors, MEMS, and ferroelectric-/piezoelectric- based [1] systems.

The key objective of this research is to develop varactor diodes capable of providing high *Q* in high power operation and to demonstrate them in adaptive microwave circuits. Comparing with MEMS, or ferroelectric-/piezoelectric-based varactor technology, semiconductor Schottky diode varactors provide faster tuning and higher reliability. Semiconductor varactors have traditionally been implemented with Si or GaAs-based diodes, for which the depletion region thickness (depletion capacitance) can be varied with applied voltage. The resultant devices, however, typically do not have sufficient voltage handling capability for the output of a power amplifier, or, if they are designed particularly for high voltage operation, then their *Q* values at microwave frequencies are too low, so that they cause significant loss of output power and efficiency. The linearity of the varactors is also a critical concern. SiC power varactors have been recently developed and reported [2]. This research

explores varactors based on GaN materials, which have dramatic new opportunities for improved performance in high-power microwave applications; the relevant figure of merit (see next section) for GaN is 40× larger than that of Si for this application. The new varactors are an enabling technology for wireless base stations, since for the first time, the varactors will be able to operate at the power levels required in the base station front-ends.

1.2 Figure of merit for GaN-based microwave power varactors

Microwave varactors provide the ability to tune the impedance matching of microwave components, and varying the operating frequency of amplifiers, oscillators and filters. They are important elements for the implementation of tunable and adaptive microwave systems and can assist in enabling efficient multi-band and software-defined radios. Critical considerations for the application of microwave varactors are: the maximum to minimum capacitance ratio (r), the maximum voltage handling capability (V_{max}), and the microwave loss (as represented by the Q value, defined below). In order to apply varactors to the tuning of microwave power amplifiers, it is typically necessary to have large capacitance ratios (r>2~3), high voltage handling capability (V_{max} >25V and up to 200V), and high Q values (Q>200). The proposed study is based on our observation that GaN has significant material

advantages for the implementation of varactor diodes. A figure-of-merit is derived below, and shown to be larger for GaN than for Si by a factor of more than 40.

A schematic diagram of a Schottky-diode based varactor is shown in Fig. 1. Under external bias control, the width of the depletion region is varied in the n^- varactor region. Underlying this region, an n^+ layer serves to provide contact to the backside. The *Q* value of the varactor under a given operating condition is the ratio of capacitive reactance to series resistance, and can be calculated by $1/(2\pi fRC)$, where C is the capacitance, and R is the resistance at the operating condition (when the overall impedance is considered as a simple series RC network). Both R and C vary as the depletion capacitance is changed with the control voltage. The worst case *Q* is Q_{min}, which occurs generally when C reaches its maximum value. We will consider Q_{min} in the following.

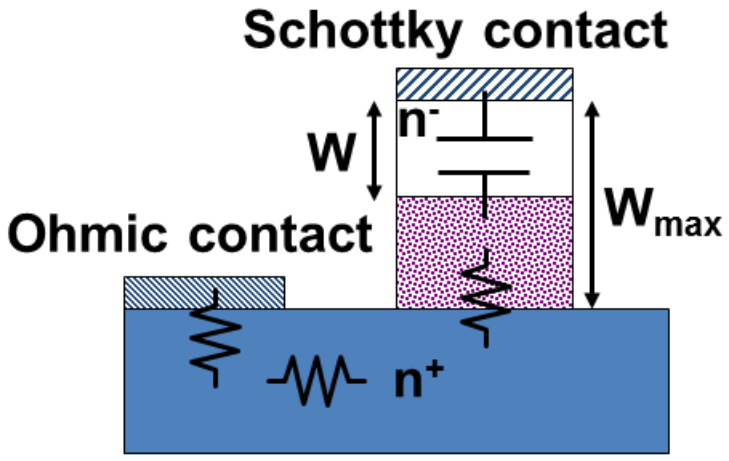

Figure 1-1 Schematic structure of Schottky-diode based semiconductor varactor.

For the varactor, the capacitance C is given by Aε/W, where W is the depletion region width at a given voltage bias, A is the junction area and ε is the dielectric constant of the semiconductor. Thus $C_{max}=A\varepsilon/W_{min}$ (which occurs at the lowest control voltages), $C_{min}=A\varepsilon/W_{max}$ (ignoring stray capacitances), and $r=W_{max}/W_{min}$. We will assume in the following that the doping level is constant in the lightly doped n^- varactor region. The series resistance R comprises various contributions. In the following we neglect series resistance from contacts and n^+ region, and assume that the undepleted portion of the "lightly doped" varactor region dominates the resistance. The width of this undepleted region (and hence the resistance) varies with the control voltage. R is then given by $\rho(W_{max}-W)/A$, where ρ is the n^- material resistivity, constant across the varactor region. Therefore,

$$Q_{min}^{-1} = \frac{2\pi f \varepsilon \rho (W_{max} - W_{min})}{W_{min}} = 2\pi f \varepsilon \rho (r-1)$$

Eq. 1-1

The resistivity in the undepleted varactor region, ρ, is given by $1/(n\mu q)$, where n is the carrier density, μ the carrier mobility and q the charge of the electron. The carrier density (and the corresponding doping density N_d) is limited by the need to keep the maximum electric field, E_{max}, below the critical breakdown electric field, E_{bk}, when the varactor region is fully depleted. Using the constant N_d (constant n) design, this constraint is given by

$$E_{max} = \frac{qN_d W_{max}}{\varepsilon} < E_{bk}$$

Eq. 1-2

The maximum voltage supported under these conditions is $V_{max}= E_{max}W_{max}/2$. It follows that $N_d <\varepsilon E_{bk}^2/(2qV_{max})$, and from the above it follows that

$$Q_{min} < \frac{\mu E_{bk}^2}{[4\pi(r-1)fV_{max}]}$$

Eq. 1-3

The factor μE_{bk}^2 constitutes a material figure of merit that indicates the potential of a given material for attaining high *Q* varactors, while the factor $1/[4\pi(r-1)fV_{max}]$ corresponds to varactor design parameters, independent of material. The equation illustrates that attaining high *Q* is particularly challenging for circuits in which the voltage level is high (as needed in high power amplifiers). It is of interest to compare the varactor figure-of-merit for different semiconductor material technologies. Table 1-1 below shows values appropriate to Si, GaAs, InP and GaN [3]. Values of Q_{min} are also calculated for a representative scenario (f=1 GHz, r=3, V_{max}=100 V). The figure-of-merit obtained for GaN is the highest in the table, higher than that of Si by a factor of more than 40×. This suggests that for microwave power amplifiers, designs based on GaN will be attractive.

Table 1-1 Comparison of properties and varactor figure of merit for various semiconductors. The calculated Q_{min} is shown for the materials for the condition f=1 GHz, r=3 and V_{max}=100 V.

Properties and Q_{min}	Si	GaAs	InP	GaN
μ (cm^2/Vsec)	1200	4000	3500	500
E_{bk} (MV/cm)	0.25	0.35	0.40	2.5
μE_{bk}^2 (10^{12} V/sec)	75	490	560	3125
Q_{min}	30	195	223	1240

Table 1-1 provides an upper bound to the Q_{min} that can be expected for a given material. In actual implementation, the series resistance will incorporate also portions corresponding to the n^+ regions, bond-wires and interconnects, and potentially from the ohmic contact regions.

1.3 Overview of the dissertation

This dissertation explores a technology to achieve high-voltage, high-Q and high-linearity microwave varactors in order to provide tunable and adaptive characteristics to the wireless base station systems. GaN with its high electron mobility and high breakdown electric field is used as the candidate material for this technology. In Chapter 1, the needs of microwave power varactors in the wireless base station applications are illustrated. The criteria for choosing the candidate semiconductor materials are also discussed. Chapter 2 details the design

considerations for achieving high breakdown voltage, high *Q* and high linearity. Epitaxial layer structure is designed to achieve the required breakdown voltage and *Q*. Optimized interdigitated and anti-parallel-diode device structures are used to improve the *Q* and linearity, respectively. Chapter 3 describes the invention of thin InGaN surface layer on top of GaN to enhance the Schottky barrier height and increase the breakdown voltage of the GaN-based Schottky diodes. InGaN/GaN material MOCVD growth, material characterization, thermal effects on Ni-InGaN/GaN Schottky junctions and its application in the enhancement-mode HEMTs are also presented. Chapter 4 discusses the fabrication procedure and preliminary DC and RF results of the microwave power varactors. Simulated and experimental results for various sidewall passivation methods to reduce reverse leakage current and maintain low leakage current during device fabrication are also reported. Chapter 5 demonstrates the final experimental DC and RF results and the corresponding simulations of the GaN-base microwave power varactors. Varactors with breakdown voltage of > 100 V, Q > 100 and OIP3 > 71 dBm (ACLR < -53 dBc) are achieved. Demonstration of the real application for the GaN-based microwave power varactors are also carried out by using the varactors in a tunable resonance circuit. Finally, Chapter 6 summarizes the entire dissertation and outlines the future work.

Section 1.1, is part of the project proposal “High Power Varactor Development for Adaptive Basestations”, Peter M. Asbeck. The dissertation author was the primary researcher of this project.

Section 1.2, is part of the paper “InGaN/GaN Schottky Diodes With Enhanced Voltage Handling Capability for Varactor Applications”, Wei Lu, Lingquan Wang, Siyuan Gu, David P. R. Aplin, Daniel M. Estrada, Paul K. L. Yu, and Peter M. Asbeck, IEEE Electron Device Letters, vol. 31, no. 10, pp. 1119–1121, Oct. 2010. The dissertation author was the primary author of the paper.

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Chapter 2

Design of GaN-based microwave power varactors

GaN-based varactors have been previously reported mainly fabricated with a GaN HFET process [1]-[3]. In this chapter, we discuss the design of the GaN varactors with vertical geometry as shown before in Figure 1-1 and illustrate that a higher voltage handling capability may be obtained with a suitable InGaN surface layer design. Designs and simulations for optimizing the device layout to achieve high *Q* and high linearity will be also presented.

2.1 Design for high breakdown voltage

Figure 2-1 schematically shows the structure of a GaN varactor with vertical geometry. In order to achieve a breakdown voltage of larger than 100 V, the varactor region (n^- GaN) thickness is designed to be $t = 2V_{max}/E_{bk} = 1$ μm, where $V_{max} = 100$ V

and E_{bk} is conservatively assumed to be 2 MV/cm. The doping concentration of the n^- GaN is estimated from 1-D Poisson equation: $N_d = \varepsilon E_{bk}/(qt) = 1\times10^{17}$ cm^{-3}. The thickness and doping level of the underlying n^+ GaN region should be thick and high enough, but without deteriorating the material quality, to minimize the series resistance coming from this layer. In this design, they are chosen to be ~1.5 μm and 5×10^{18} cm^{-3}, respectively. The material is grown on c-Sapphire substrates using metal organic chemical vapor deposition (MOCVD). Ni is used as the Schottky contact to ensure a high Schottky barrier height and Ti/Au/Pd/Au (Au is atop) metal stack is used as the ohmic contact.

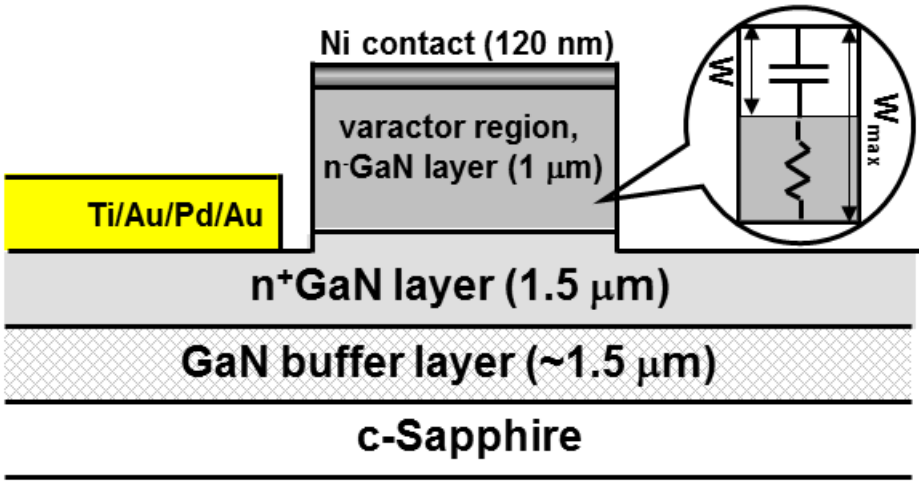

Figure 2-1 Schematic diagram of a GaN-based varactor and its layer structure.

Then devices are fabricated and measured to verify the breakdown characteristics of the designed GaN Schottky diodes. The fabrication procedure is as follows: a 120-nm-thick Ni Schottky contact was deposited immediately after the sample MOCVD growth and NH_4OH surface cleaning to minimize the interface

oxidation or contamination [4]. The Ni film was then patterned, and circular mesa diodes with diameters in the range of 80–300 μm were formed using BCl_3/Cl_2 in a Trion reactive-ion-etching/inductively-coupled plasma dry-etch system, which was followed by an ~90 ^{o}C KOH (0.1 mol/L) treatment to reduce the dry-etch residuals. A Ti/Al/Pd/Au (20 nm/80 nm/50 nm/100 nm) metal stack was used to form ohmic contacts to n^+ GaN. A scanning-electron microscopy (SEM) top view of the fabricated device is shown in Figure 2-2.

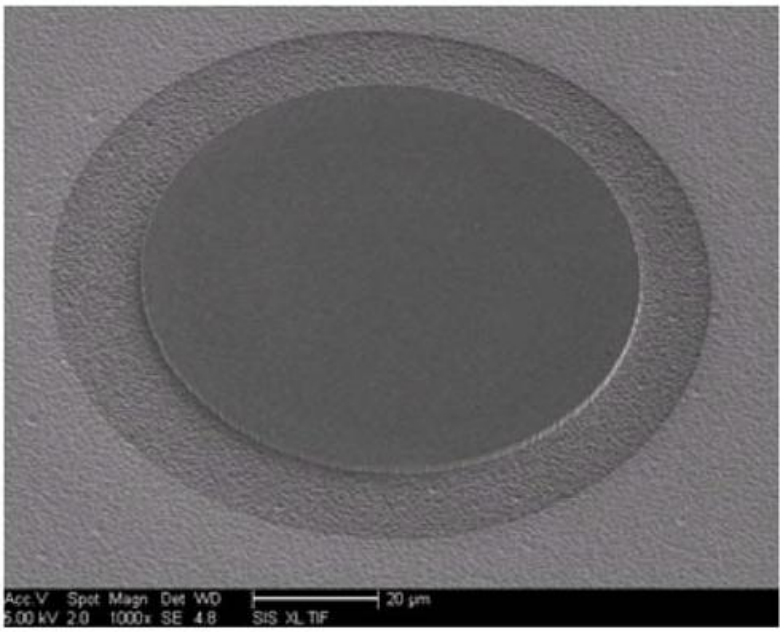

Figure 2-2 SEM top view of a fabricated diode with an 80-μm diameter.

The current-voltage (I-V) characteristics of these diodes were measured with an Agilent B1500 semiconductor device analyzer. The reverse I-V curve of a diode with an area of 5×10^{-5} cm^2 is shown in Figure 2-3. However, the breakdown voltage is lower and the reverse leakage current is higher than the expected values. The leakage

current under a high reverse bias has been attributed to the direct tunneling of electrons through the Schottky barrier [5], [6]. For a proper operation and low-power loss of the GaN varactors, the leakage current of the Schottky diode must be adequately low even at high operating voltages. Therefore an improved design is needed to suppress the electron tunneling.

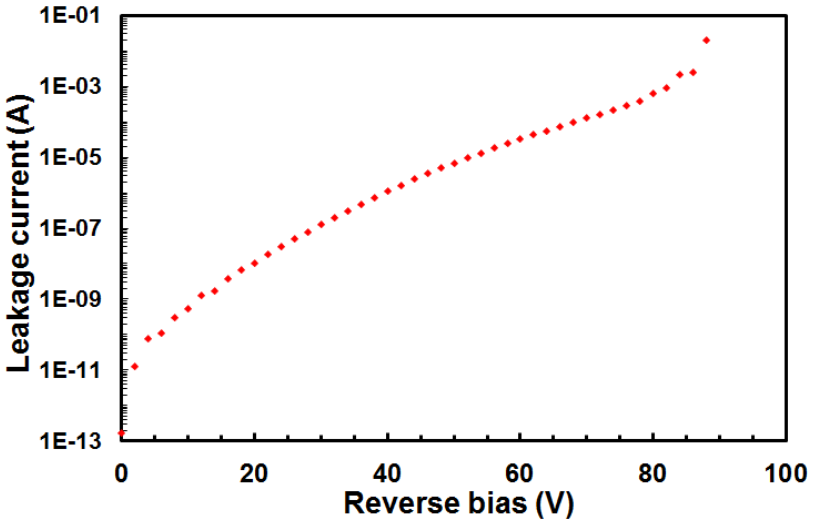

Figure 2-3 Reverse leakage current of a device with an area of 5×10^{-5} cm^2.

It is known that large polarization-charge densities present at III–nitride semiconductor heterojunction interfaces significantly affect the electric-field distributions in the semiconductors [7], providing opportunities for Schottky-barrier engineering. To suppress the tunneling current under a high reverse bias, we designed an InGaN surface layer to engineer the tunneling barrier by utilizing the polarization charges at the InGaN/GaN interface. The new design and its corresponding electric field and energy band diagrams are shown in Figure 2-4 and 2-5, respectively. As

shown in Figure 2-5(a), in comparison to the design with GaN only, the surface electric field is reduced for the InGaN surface layer design, which leads to an increased electron tunneling distance. The significant reduction (~50% at a 100-V reverse bias) of the surface electric field is primarily due to the presence of the negative polarization charges at the InGaN/GaN interface, although the slightly increased dielectric constant of the InGaN also favors the surface field reduction. The suppression of the leakage current is thus achieved because the tunneling probability sharply decreases with the increase of the tunneling distance. The indium concentration and the thickness of the InGaN layer are designed to be 10% and 15 nm, respectively, based on the considerations of obtaining high-quality InGaN layers and resultant energy barrier shape. Figure 2-5(b) shows the corresponding energy band diagram at reverse 0 and 100 V by solving a 1-D Poisson equation. In this computation, a 4.9×10^{12} cm^{-2} sheet polarization charge density and a 0.21-eV conduction band energy discontinuity [8] at the $In_{0.1}Ga_{0.9}N$/GaN interface were assumed. The Schottky barrier height of $In_{0.1}Ga_{0.9}N$ was also assumed to be 0.21 eV lower than that of the GaN. As seen, at reverse 100 V, the tunneling distance for the InGaN/GaN design is ~2 times larger than the design with GaN only.

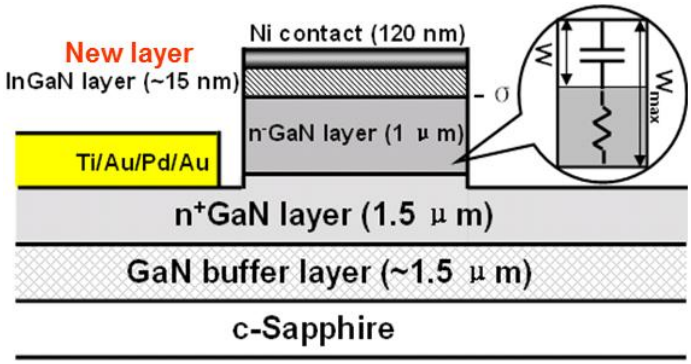

Figure 2-4 Schematic diagram of the GaN-based Schottky diode design with thin InGaN surface layer for breakdown voltage enhancement.

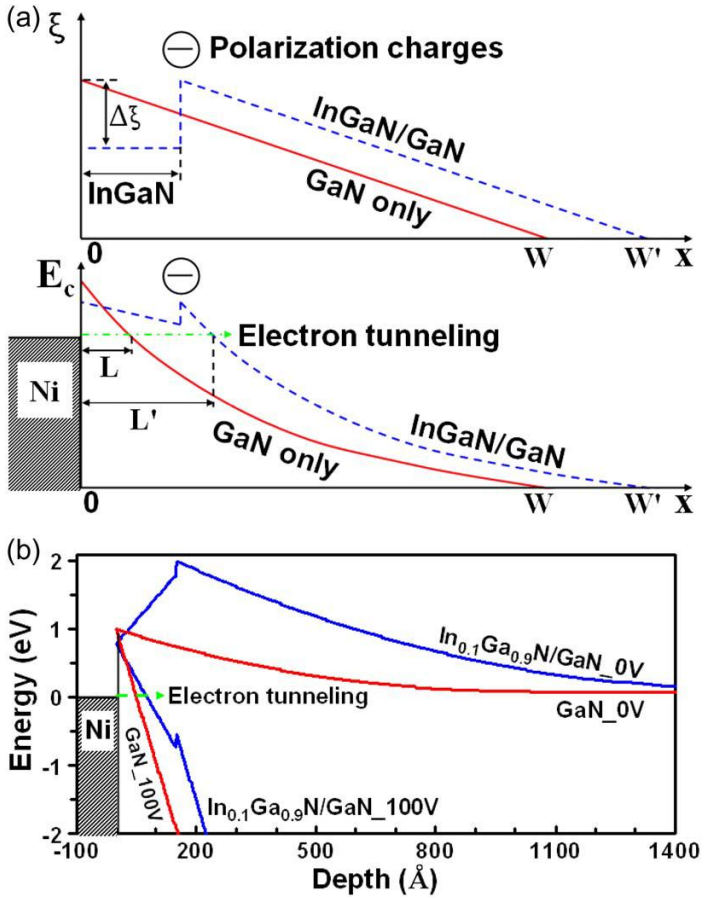

Figure 2-5 (a) Schematic diagrams of the (upper) electric field and energy bands under the same reverse bias for the designs with InGaN/GaN and GaN only. W and W': Depletion width. L and L': Electron tunneling distance. Δξ: Surface electric field reduction. (b) Representative energy band diagrams at reverse 0 and 100 V calculated by the 1-D Poisson solver [9].

The samples with and without InGaN surface layer design were grown using a Thomas Swan Close Coupled Showerhead 3×2 MOCVD system. For comparison purposes, three samples have been grown, with layer information and labels shown in Table 2-1. The Schottky diodes were then fabricated followed the same procedure stated above. The measured reverse IV characteristics are shown in Figure 2-6.

Table 2-1 Sample layer structures and labels.

Sample labels	Control	$In_{0.06}Ga_{0.94}N$	$In_{0.1}Ga_{0.9}N$
InGaN layer	N.A.	6 % indium, ~15 nm	10 % indium, ~15 nm
Common layers	n^- GaN (n~1×10^{17} cm^{-3}, 1 μm)		
	n^+ GaN (n~5×10^{18} cm^{-3}, 1.5 μm)		
	undoped GaN buffer (~1.5 μm)		
	c-sapphire substrate		

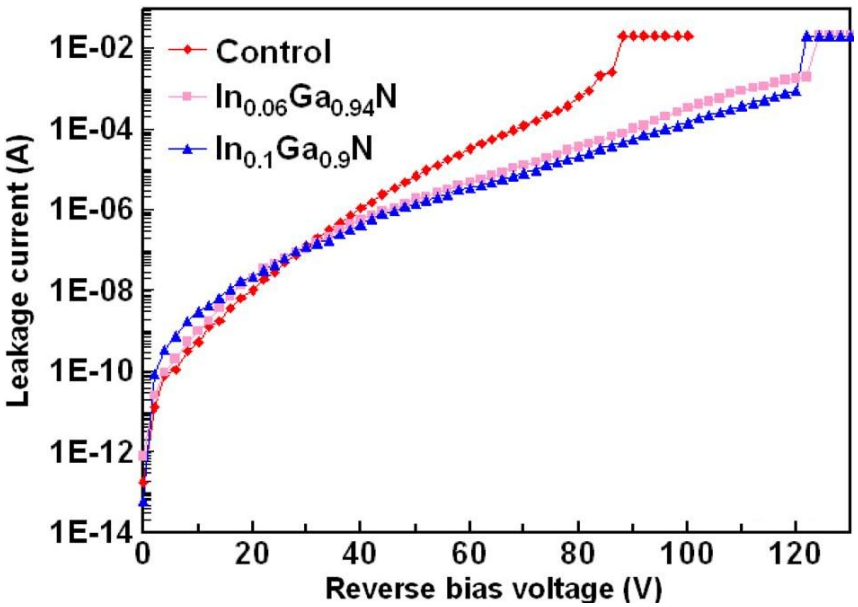

Figure 2-6 Reverse IV characteristics for samples with and without InGaN surface layers. Circular diodes have areas of 5×10^{-5} cm^2.

It is obvious that the inclusion of the InGaN surface layer significantly improves the breakdown voltage by up to ~40 V, in comparison with the control sample. Such improvement is consistently observed, for all of our InGaN-containing samples, as a result of the reduced surface electric field, as shown in Figure 2-5(a). These results validated the approach of implementing a thin InGaN surface layer on top of GaN is effective in achieving the GaN-based high-voltage microwave varactors. The detailed analysis including forward and reverse I-V, capacitance-voltage (C-V), material and thermal characteristics of the Ni-InGaN/GaN Schottky diodes will be discussed chapter 3.

2.2 Design for high linearity

In order to maintain adequate linearity in the amplifier, the effective varactor capacitance should not vary with the RF signal level. However, a single Schottky diode varactor has poor linearity due to the square root dependence of the capacitance on the applied voltage: $C \sim V^{1/2}$, for a uniformly doped junction. A well-established strategy to improve the linearity of diode-based varactors is to employ an anti-parallel (back-to-back) diode topology [10], in the geometry shown in Figure 2-7(b). In this circuit, the DC control voltage is applied to both diodes equally. The RF voltage swing, however, adds to the instantaneous voltage of each diode with opposite sign (such that the capacitance of one of the diodes is increased, while the other is decreased). The net capacitance under the application of DC voltage and RF voltage can be readily calculated; representative results for both two diode topologies are shown in Figure 2-7 for simple diodes with uniform n^- doping. It is seen that by using the anti-parallel diode topology, the RF signal induced capacitance variation is minimized. The linearity of the varactor diode is thus significantly improved. An optimal choice of semiconductor doping profile can improve linearity further [10].

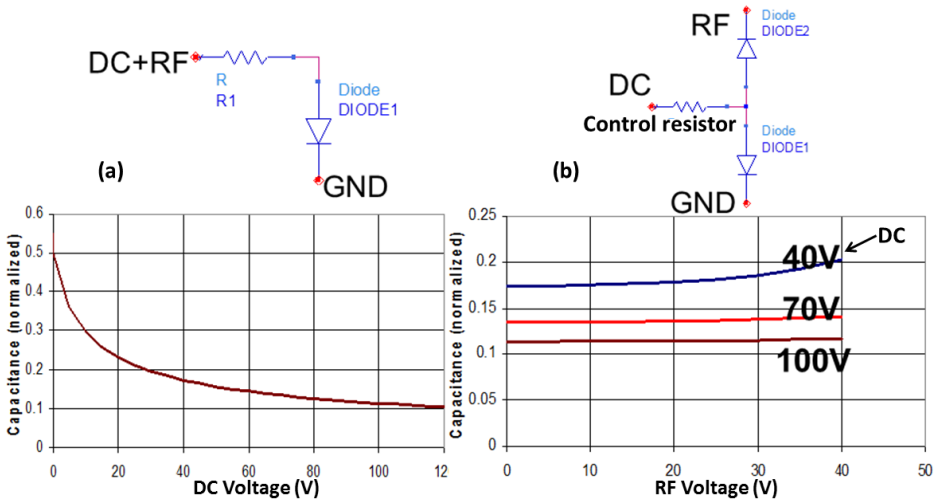

Figure 2-7 Simulated C-V curves for (a) single diode structure and (b) two anti-parallel diode structure.

In this design, a center resistor, also called "control resistor" is needed to maintain a high *Q* factor. The impedance of the control resistor should be high enough to prevent the loss of the RF signal through the DC path (maintaining high *Q* factor), but not cause too much voltage drop through the DC path (maintaining tuning characteristics). In our design, the resistance of the control resistor R_{ctrl} is typically > $10 \times \left| 1/j\omega C \right|$, where ω is the operation frequency and C is the capacitance of the anti-parallel varactor. More design considerations on improving the *Q* will be discussed in the following section.

2.3 Design for high *Q*

In order to achieve high *Q*, the series resistance of the structure needs to be minimized. The component of resistance associated with the undepleted n^- region is decreased by doping the n^- region as high as is feasible, as discussed in section 1.2. The component of resistance associated with the n^+ backside contact is decreased by increasing the doping and thickness of the n^+ layer, and by decreasing the separation of the varactor regions. As a result of these considerations, an interdigitated stripe geometry is adopted, as shown schematically in Figure 2-8. The dimensions of the stripes are made as small as possible, consistent with the lithography and etch techniques available. The serpentine resistor made by n^+ GaN is the control resistor for blocking RF signals in the DC path. The design constraint of the R_{ctrl} is described in the previous section.

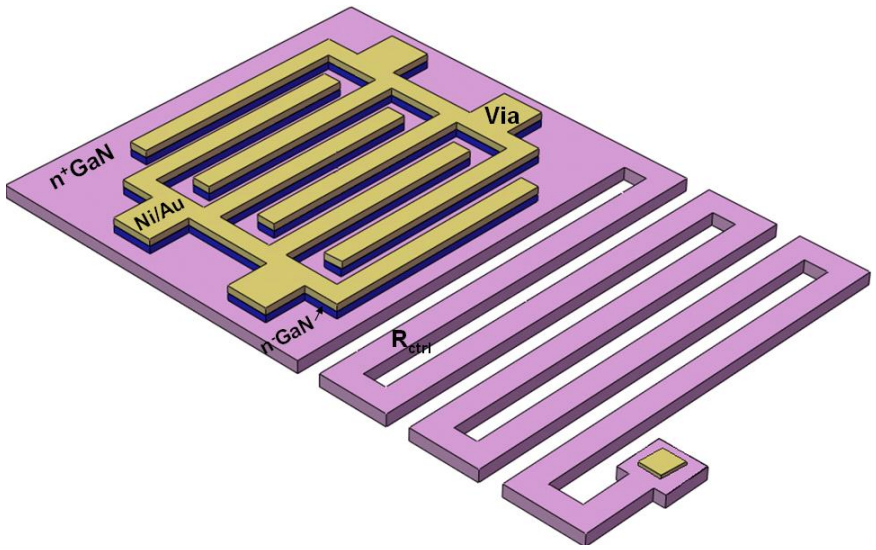

Figure 2-8 Schematic diagram of the anti-parallel diode structure with interdigitated strip geometry.

The series resistance expected from the n^+ regions under the diodes is the principal parasitic; by contrast, the resistance from the undepleted n^- GaN region is usually very small. Bondwires add additional series resistance, exacerbated by skin effect as the frequency increases. An additional concern of significance for *Q* is the series resistance of the stripe (interdigitated) Schottky metal contacts. The distributed resistance of these metals can add appreciably to the overall resistance if the fingers are too long. In order to find out the optimal geometry of the interdigitated structure for the purpose of achieving high *Q*, a transmission line method considering the corresponding lump components is used to estimate the overall contribution from different regions of the structure. Fig. 2-9(a) shows the schematic diagram of an interdigitated diode structure with its corresponding lump components. The transmission-line circuit model was represented by a distributed resistance and capacitance as shown in Figure 2-9(b).

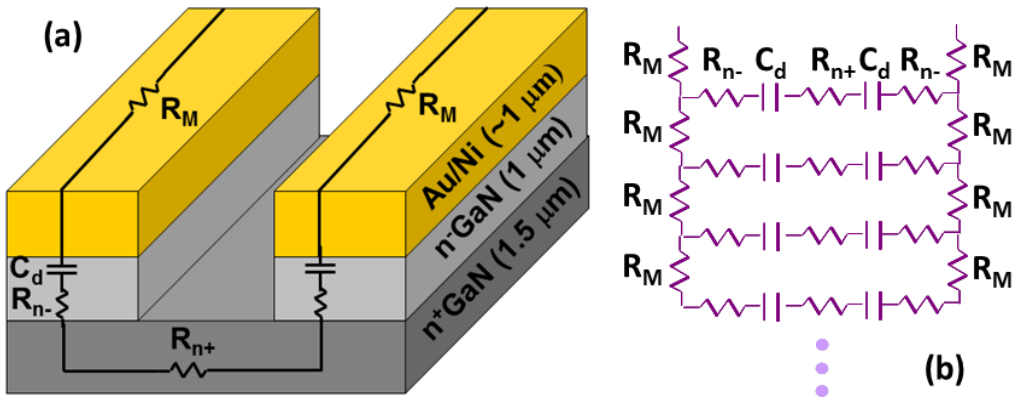

Figure 2-9 (a) Schematic diagram of the anti-parallel varactor diode with its corresponding lump components, and (b) the circuit model represented by a distributed resistance and capacitance.

The calculation result shows that the overall *Q* is a function of finger length, with maximum values that differed according to the metal sheet resistance used, as detailed in Figure 2-10. A maximum *Q* value is achieved for a finger length of ~ 50 μm under the assumption of 2.5-μm finger width and spacing and 1-μm metal stripe thickness. Too long or too short metal length will result in a lower *Q*.

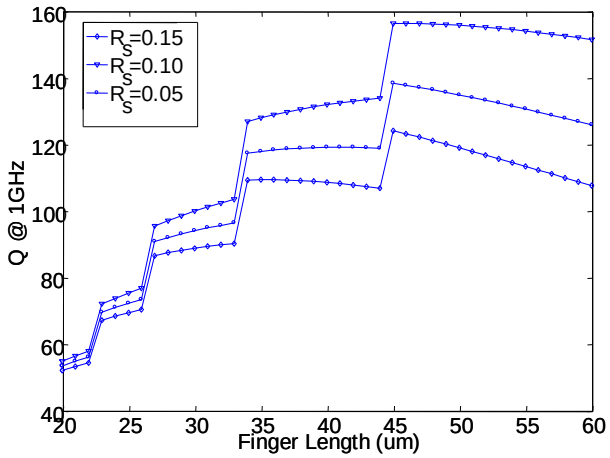

Figure 2-10 Simulated values of *Q* as a function of finger length.

Another lump component that is not considered in this model is the R_{leak} in parallel with the series R_{n-} and C_d, which represents the leakage path of the Schottky barrier. A small value of R_{leak} (corresponding to a leaky junction) will cause an increase of the series resistance so that the *Q* drops. The detailed analysis of reverse leakage current will be discussed in chapter 4.

2.4 Summary of the designs

This chapter covered the designs for achieving high-breakdown voltage, high-*Q* and high-linearity GaN-based microwave Schottky varactor diodes. A thin InGaN surface layer design is invented to increase breakdown voltage of the GaN-based Schottky diodes by ~40 V, from ~80 V to above 120 V. The anti-parallel diode topology will be adopted to improve the linearity performance of varactors. Interdigitated structure with small and optimized finger dimensions (upon the lithograph and processing techniques) and thick metal stripe will be used to maximize the *Q*.

Section 2.1, is a rearrangement of the paper "InGaN/GaN Schottky Diodes With Enhanced Voltage Handling Capability for Varactor Applications", Wei Lu, Lingquan Wang, Siyuan Gu, David P. R. Aplin, Daniel M. Estrada, Paul K. L. Yu, and Peter M. Asbeck, IEEE Electron Device Letters, vol. 31, no. 10, pp. 1119–1121, Oct. 2010. The dissertation author was the primary author of the paper.

Section 2.2 and 2.3, are a rearrangement of the project proposal "High Power Varactor Development for Adaptive Basestations", Peter M. Asbeck. The dissertation author was the primary researcher of this project.

2.5 References

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Chapter 3

Ni-InGaN/GaN Schottky diode technology

III–nitride-based Schottky diodes have achieved many applications, such as ultraviolet photodetectors [1], gas sensors [2], high-voltage rectifiers [3], and varactors [4]. One key factor to improve the performance of these devices is to minimize reverse leakage current, particularly under high reverse voltages. For microwave power varactors, excess leakage current can cause *Q* degradation, device heating and reliability issue. Many prior efforts have been reported to reduce the leakage current in GaN-based Schottky barriers, such as electrochemical surface treatment [5], SiO_2 dielectric surface passivation [6], capping with low-temperature GaN layers [7], and oppositely doped surface layers to increase the Schottky-barrier height (SBH) [8]. However, these studies do not discuss in detail the leakage-current-suppression mechanisms particularly under high reverse voltages, which is important in high-power applications. In this chapter, we present a detailed study of the reverse-leakage-current mechanisms in MOCVD-grown GaN Schottky barrier diodes as well as the leakage-suppression mechanism using InGaN/GaN Schottky barriers. We also report that the leakage current can be further significantly suppressed by using a high-

pressure (HP, near atmospheric pressure) MOCVD growth technique [9] for the GaN buffer layers (i.e., an HP GaN buffer). Additionally, extensive InGaN/GaN material characterization using Nomarski optical microscopy, scanning electron microscopy, and atomic force microscopy are performed to correlate between the material defects and the excess reverse leakage current in Ni-InGaN/GaN Schottky barrier diodes. The application of InGaN/GaN design in the enhancement-mode GaN-based high electron mobility transistors (HEMTs) is also introduced.

3.1 Theory of InGaN surface layer design

Based on the introduction of the InGaN surface layer design for enhancing the breakdown voltages of the GaN-based Schottky diode varactors, furthermore analytical studies on the reverse leakage current and leakage current suppression mechanisms in the GaN-based Schottky diodes will be discussed in this section.

3.1.1 Analysis of reverse leakage current in GaN Schottky barriers

The reverse leakage current of the Schottky barrier has been attributed to the electron tunneling directly through the Schottky barrier [10], [11]. In order to suppress the leakage current, it is necessary to re-examine the leakage current mechanisms in

GaN Schottky barriers. Figure 3-1 shows a schematic energy band diagram of a Schottky barrier under reverse bias. According to conventional analysis [12], for reverse biases greater than $3kT/q$ the current density J_r from semiconductor to metal through the Schottky barrier can be expressed by the following:

$$\begin{aligned} J_r &= \frac{A^*T}{k}\exp\left[-\frac{q\phi_b}{kT}\right]\times\int_0^\infty P(\zeta)\exp\left(-\frac{\zeta}{kT}\right)d\zeta \\ &+\frac{A^*T}{k}\times\int_0^{q(V_b-\Delta\phi)} F_m P(\eta)\left[1-F_s(V_r)\right]d\eta \\ &= J_A + J_B \end{aligned}$$

Eq. 3-1

where A^* is the effective Richardson constant, T is the temperature in Kelvin, k is the Boltzmann constant, q is the charge of an electron, $q\phi_b$ is the effective barrier height, V_b is the built-in potential at reverse bias V_r ignoring image force lowering, $q\Delta\phi$ is the image force lowering of the barrier height, F_m and F_s are the Fermi-Dirac distribution functions of electrons in the metal and semiconductor, respectively, ζ and η are the energy of the electrons above and below the top of the effective barrier, respectively, and $P(\zeta)$ and $P(\eta)$ are the tunneling probabilities of the electrons above and below the top of the effective barrier, respectively. Assuming $P(\zeta) = 1$ and $P(\eta)$ calculations using the Wentzel-Kramers-Brillouin (WKB) approximation [13], we find

$$P(E) = \exp\left[-2\frac{\sqrt{2m^*}}{\hbar}\int_{x1}^{x2}\sqrt{q\phi(x)-E}\,dx\right]$$

Eq. 3-2

where m^* is the electron effective mass, $\hbar$ is the reduced Planck constant, x is the distance measured from the metal-semiconductor interface, and x_1 and x_2 are the classical turning points, which determine the electron tunneling distance as $L = x_2 - x_1$. Measured from the Fermi level of metal, $\phi(x)$ is the electrostatic potential distribution and $E = q\phi_b - \eta$ is the energy of tunneling electrons. In Eq. 3-1, the first term J_A corresponds to the thermionic emission component; the second term J_B corresponds to the tunneling component which dominates at high dopings and low temperatures. Therefore, we need only to consider the second term for studying n^- GaN Schottky barriers at room temperature. Under low reverse bias $P(E)$ sharply decreases as E decreases based on Eq. 3-2; most of the electrons tunnel near the top of the effective barrier so that $1 - F_s \approx 1$, and F_m is given by

$$F_m = \frac{1}{1+\exp\left(\frac{E-E_{fm}}{kT}\right)} \approx \exp\left(\frac{-E}{kT}\right).$$

Eq. 3-3

Assuming the barrier has a triangular shape near the top of the effective barrier, the electrostatic potential distribution can be written as:

$$q\phi(x) = -q\xi x + q\phi_{b0}$$

Eq. 3-4

where ξ is the constant electric field near the top of the effective barrier. Then, Eq. 3-2 becomes

$$P(E) = \exp\left[-2\frac{\sqrt{2m^*}}{\hbar}\int_0^{\frac{q\phi_{b0}-E}{q\xi}} \sqrt{-q\xi x + q\phi_{b0} - E}\,dx \right]$$
$$= \exp\left[-\frac{4}{3}\frac{\sqrt{2m^*}}{\hbar}\frac{\left(q\phi_{b0} - E\right)^{\frac{3}{2}}}{q\xi} \right].$$

Eq. 3-5

Ignoring J_A, J_r can be approximated as:

$$J_r \approx J_B = \frac{A^*T}{k} \times \int_{-(V_r - V_n)}^{q\phi_{b0}} \exp\left[-\frac{4}{3}\frac{\sqrt{2m^*}}{\hbar}\frac{\left(q\phi_{b0} - E\right)^{\frac{3}{2}}}{q\xi} - \frac{E}{kT} \right] dE.$$

Eq. 3-6

Taking a derivative of the exponential factor in Eq. 3-6, we can find the energy E_m where the electron tunneling peaks:

$$E_m = q\phi_{b0} - \frac{\hbar^2 q^2 \xi^2}{8m^* k^2 T^2}.$$

Eq. 3-7

Assuming the semiconductor has a uniform doping concentration N_d, Eq. 3-7 becomes

$$E_m = q\phi_{b0} - \frac{\hbar^2 q^3 N_d (V_{b0} + V_r)}{4m^* \varepsilon k^2 T^2}$$

Eq. 3-8

where V_{b0} is the built-in potential at zero bias, and ε is the dielectric constant of the semiconductor. Eq. 3-8 is a decreasing function with the reverse bias V_r and valid as long as Eq. 3-3 is a good approximation ($E_m > 3kT$). With further increasing V_r, E_m eventually becomes almost constant when it reaches a few kT below the Fermi level of metal where F_m is almost constant at 1 but $P(E)$ decreases sharply as E decreases further. Therefore, under high reverse bias most of the electrons tunnel near the Fermi level of metal. For a Ni/*n*-GaN Schottky barrier with $N_d = 1 \times 10^{17}$ cm^{-3}, $T = 300$ K, and $q\phi_{b0} = 1$ eV, $E_m = 1 - 0.03 \times (0.92 + V_r)$ in eV. When $V_r > 33$ V most of the electrons tunnel near the Fermi level of metal. This finding suggests that the leakage current suppression under high reverse bias can be achieved by reducing the electron tunneling probability around the Fermi level of metal.

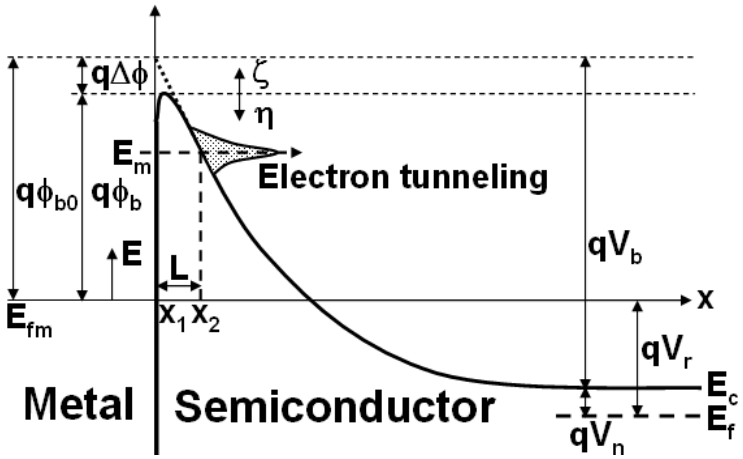

Figure 3-1 Schematic energy band diagram of a Schottky barrier under reverse bias. $q\phi_{b0}$ is the barrier height ignoring image force lowering, $q\Delta\phi$ is the image force lowering of the barrier height, $q\phi_b = q\phi_{b0} - q\Delta\phi$ is the effective barrier height, E_{fm} is the Fermi level of metal, E_f is the quasi-Fermi level of semiconductor, E_c is the bottom of the conduction band of semiconductor, $qV_n = E_c - E_f$, E is the energy of electrons measured from the Fermi level of metal, E_m is a certain energy where the electron tunneling peaks, V_b is the built-in potential at reverse bias V_r ignoring image force lowering, x is the distance measured from the metal-semiconductor interface, and $L = x_2 - x_1$ is the tunneling distance at E_m.

Anticipating the measurement results reported below, we find that the theoretical analysis outlined above agrees well with our experimental measurements. Figure 3-2 shows the measured reverse leakage current for a control sample (Ni/*n*-GaN Schottky diode with $N_d \approx 1\times10^{17}$ cm^{-3} confirmed by C-V measurement) with an area of 5×10^{-5} cm^2 and for comparison the calculated result based on Eq. 3-1 with $N_d = 1.1\times10^{17}$ cm^{-3}, $q\phi_{b0} = 0.95$ eV, $T = 300$ K, $A^* = 26.4$ Acm^{-2}K^{-2} [14], $m^* = 0.2m_0$ [15], where m_0 is the electron mass. Departures from the tunneling based curve occur at low bias (< 30 V) are possibly related to generation of minority carriers at defects within the depletion region, and at high bias (> 80 V). For $V_r = 80$ V, the calculated electric field at the surface reaches $\xi = 1.9$ MV/cm, where impact ionization effects are expected to become significant.

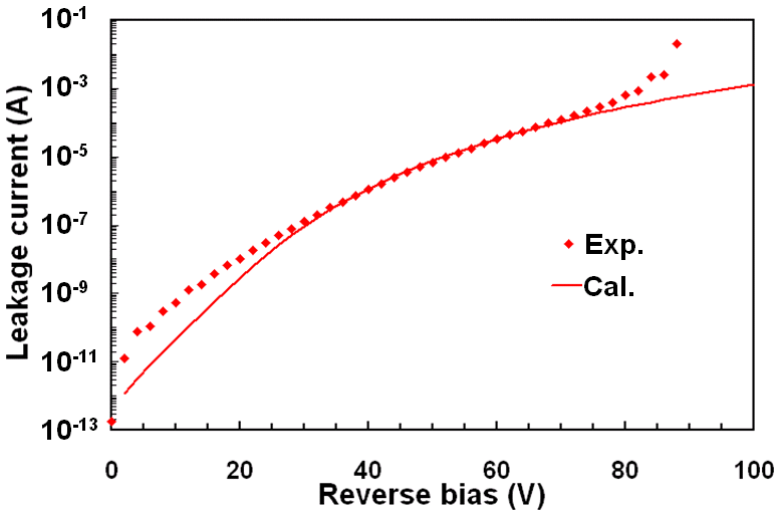

Figure 3-2 Experimental and calculated reverse leakage current of a Ni-GaN Schottky diode with an area of 5×10^{-5} cm^2.

3.1.2 InGaN surface layer design for reduced leakage current

Five samples have been grown using the conventional low-pressure (LP) MOCVD growth technique [16] for the study of InGaN surface layer design. Their labels and key growth details are shown in Table 3-1. The Schottky diodes were fabricated followed the procedure mentioned in section 2.1.

Table 3-1 Sample labels and key growth details used in this study.

Sample labels	Control	2nm/$In_{0.06}Ga_{0.94}N$	0nm/$In_{0.06}Ga_{0.94}N$	2nm/$In_{0.1}Ga_{0.9}N$	0nm/$In_{0.1}Ga_{0.9}N$
GaN cap layer	N.A.	UID, ~2nm, 400 mbar, 820 ^{o}C	N.A.	UID, ~2nm, 400 mbar, 808 ^{o}C	N.A.
InGaN layer	N.A.	UID, ~6% In, ~15 nm, 400 mbar, 820 ^{o}C	UID, ~6% In, ~15 nm, 400 mbar, 820 ^{o}C	UID, ~10% In, ~15 nm, 400 mbar, 808 ^{o}C	UID, ~10% In, ~15 nm, 400 mbar, 808 ^{o}C
Common layers	n^- GaN (n~1×10^{17} cm^{-3}, 1 μm), 200 mbar, 1040 ^{o}C				
	n^+ GaN (n~5×10^{18} cm^{-3}, 1.5 μm), 200 mbar, 1040 ^{o}C				
	Unintentionally doped (UID) GaN buffer (~1.5 μm), 300 mbar (900 mbar used for HP GaN buffer), 1040 ^{o}C				
	Low-temperature GaN nucleation layer (~20 nm), 600 mbar, 530 ^{o}C				
	c-Sapphire substrate				

Based on the analysis in the last section, an InGaN surface layer is introduced to reduce the electron tunneling probability around the Fermi level of metal by Schottky barrier engineering. As shown in Figure 3-3, the surface electric field is significantly reduced for the InGaN surface layer design (InGaN/GaN case) due to the polarization charge at the interface, leading to an increased electron tunneling distance near the Fermi level of metal where most of the electrons tunnel under high reverse bias as discussed above. The leakage current is thus suppressed because the tunneling probability *P(E)* given by Eq. 3-2 sharply decreases with the increase of the tunneling distance. In addition to the samples discussed in section 2.1, a 2-nm-thick GaN cap

layer was also designed (GaN/InGaN/GaN) in case there was indium out-diffusion during the cooling down process at the end of the MOCVD growth. The GaN cap could, however, weaken the effectiveness of the InGaN surface layers (less tunneling distance increase compared to that without GaN cap layer as shown in Figure 3-3(c)). In order to obtain high-quality InGaN layers and long tunneling distances, we designed the indium concentration and the thickness of the InGaN surface layer to be 10% and 15 nm, respectively. Higher indium concentration and thicker InGaN thickness might result in InGaN layer quality degradation and strain relaxation (less polarization effects). The corresponding energy band diagrams at 0 and reverse bias 80 V shown in Figure 3-3(b) and 3-3(c), respectively, were obtained by solving the 1-D Poisson equation. In this calculation, a 4.9×10^{12} cm^{-2} sheet polarization charge density and a 0.21-eV conduction band discontinuity were assumed at the $In_{0.1}Ga_{0.9}N$/GaN and GaN/$In_{0.1}Ga_{0.9}N$ interfaces [17]; the SBH (ignoring the image force lowering) of $In_{0.1}Ga_{0.9}N$ was also assumed to be 0.21 eV lower than that of the GaN, which corresponds with the expected conduction band energy difference ΔE_c between the $In_{0.1}Ga_{0.9}N$ and GaN. It is seen that the tunneling distance for the $In_{0.1}Ga_{0.9}N$/GaN design at reverse bias 80 V is nearly doubled compared to the GaN only design.

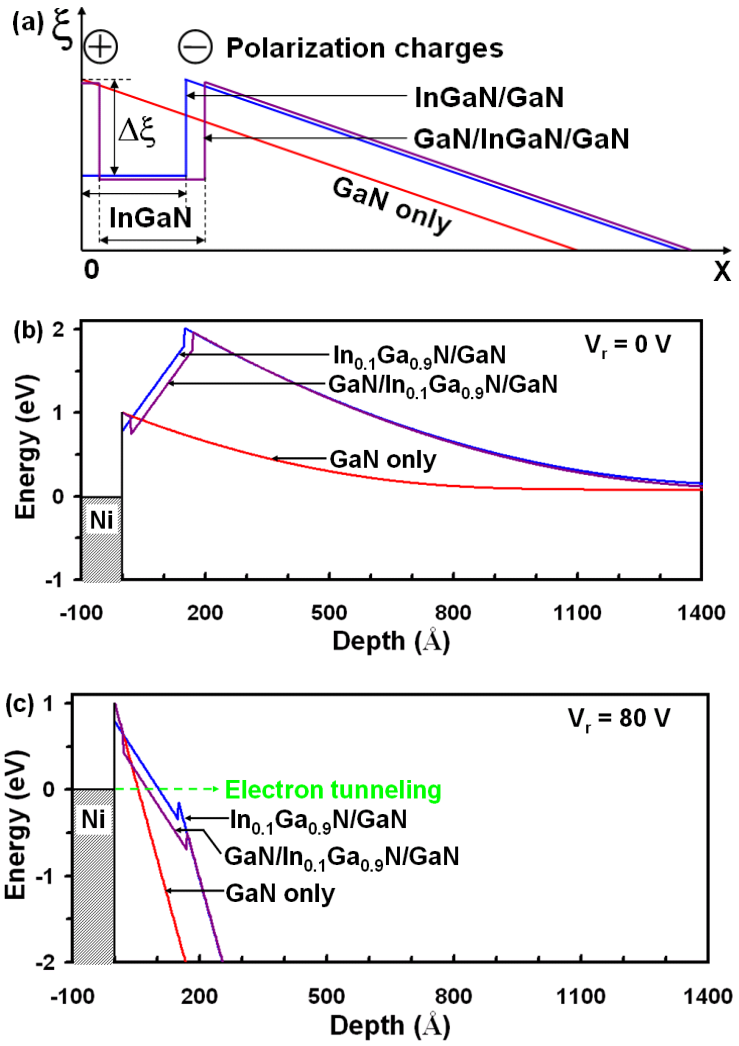

Figure 3-3 (a) Schematic diagram of the electric field under the same reverse bias for the designs with InGaN/GaN, GaN/InGaN/GaN and GaN only. $\Delta\xi$ is the surface electric field reduction of the InGaN/GaN design relative to GaN-only design. (b) Representative energy band diagrams (E_c only) at V_r = 0V and (c) V_r = 80 V by solving the 1-D Poisson equation.

3.2 Experimental results and discussions

Characterization of the Schottky diodes was carried out with C-V and I-V measurements.

3.2.1 C-V measurements and analysis

Capacitance measurements were carried out using 1 MHz signals. Figure 3-4 shows plots of $1/C^2$ versus reverse voltage V. Curves for different samples exhibit slight differences of slope due to small variations (< 1%) of the fabricated diode areas and the doping concentration N_d of the n^- GaN layers, which is approximately 1×10^{17} cm^{-3} (assuming complete ionization) extracted from the C-V results. It is noted that the curves of the InGaN-containing samples consistently show a voltage shift when compared to the control sample. This shift is due to the change in electric field distribution and electrostatic potential in the InGaN layers caused by the induced polarization charges, as shown in Figure 3-3(a). The voltage shift can be estimated by considering the integral of the electric-field reduction between the GaN and the InGaN layers, which is over the width of the InGaN layer. This estimate results in the expression:

$$\Delta V = \frac{t\sigma q}{\varepsilon_{InGaN}} + \frac{t^2 N_d q}{2\varepsilon_{InGaN}}$$

Eq. 3-9

where ΔV is the voltage shift, t is the InGaN layer thickness, σ is the sheet polarization charge density at the InGaN/GaN interface, and ε_{InGaN} is the dielectric constant of InGaN. As shown in Figure 3-4, ΔV are ~0.6 and ~0.8 V for $In_{0.06}Ga_{0.94}N$- and $In_{0.1}Ga_{0.9}N$-containing samples, respectively. Using Eq. 3-9, the polarization charge density at the $In_{0.06}Ga_{0.94}N$/GaN and $In_{0.1}Ga_{0.9}N$/GaN interfaces are estimated to be 1.9×10^{12} cm^{-2} and 2.7×10^{12} cm^{-2}, respectively. The estimated numbers are less than theoretical expectations (0.9×10^{12} cm^{-2} and 4.0×10^{12} cm^{-2} for the spontaneous and piezoelectric polarizations, respectively, in the $In_{0.06}Ga_{0.94}N$/GaN samples, and 1.5×10^{12} cm^{-2} and 6.4×10^{12} cm^{-2} for the spontaneous and piezoelectric components, respectively, for $In_{0.1}Ga_{0.9}N$/GaN) [17], [18] probably due to partial strain relaxation.

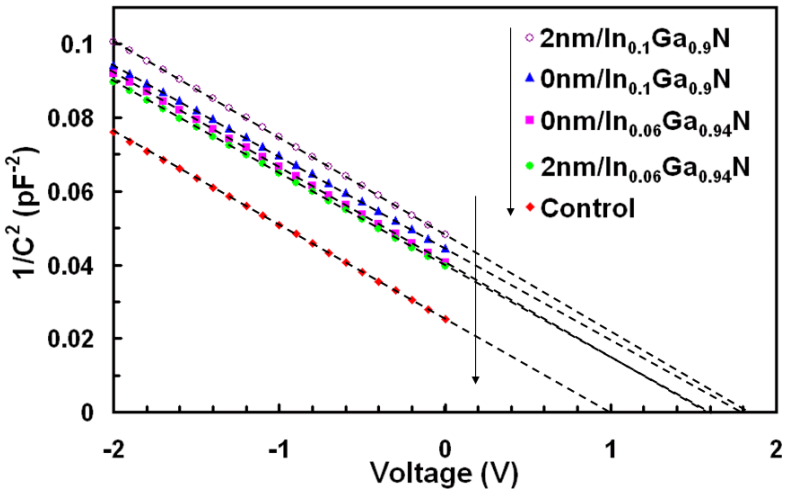

Figure 3-4 C-V results of the five samples with area of 7.85×10^{-5} cm^2, measured in the dark at 1 MHz. The colored dots are measurement data and the dash lines are fitting curves.

3.2.2 Forward I-V measurements and analysis

The polarization charges at the InGaN/GaN interfaces change the Schottky barrier shape and correspondingly the forward I-V characteristics. Figure 3-5 illustrates schematically the energy band diagram of an InGaN/GaN structure. The effective barrier height $q\phi_b$ is forward-bias (V_f) dependent and given by

$$q\phi_b = q\phi_{b0} + q\frac{\sigma q - W_d N_d q}{\varepsilon_{InGaN}} t + \Delta E_c$$

Eq. 3-10

where ΔE_c is the conduction band discontinuity at the InGaN/GaN interface and W_d is the forward-bias dependent depletion width measured from the InGaN/GaN interface. It may be calculated by

$$W_d = \sqrt{\frac{2\varepsilon_{GaN}(\phi_b - V_n - V_f)}{N_d q}}$$

Eq. 3-11

where ε_{GaN} is the dielectric constant of GaN. With Eqs. 3-10 and 3-11 the following equation holds

$$\frac{\partial \phi_b}{\partial V_f} = \frac{t\varepsilon_{GaN}}{t\varepsilon_{GaN} + W_d \varepsilon_{InGaN}}.$$

Eq. 3-12

Using the thermionic emission (TE) theory, the forward I-V characteristics may be described as

$$J_f = A^* T^2 \exp\left(\frac{-q\phi_b}{kT}\right)\left[\exp\left(\frac{qV_f}{kT}\right) - 1\right] \approx A^* T^2 \exp\left(\frac{qV_f - q\phi_b}{kT}\right).$$

Eq. 3-13

Therefore the ideality factor *n* (or inverse subthreshold slope) may be obtained as

$$n = \frac{q}{2.3kT}\left(\frac{\partial\left(\log_{10} J_f\right)}{\partial V_f}\right)^{-1} = \left(1 - \frac{\partial \phi_b}{\partial V_f}\right)^{-1} = 1 + \frac{t\varepsilon_{GaN}}{W_d \varepsilon_{InGaN}}.$$

Eq. 3-14

As shown by Eq. 3-14, the ideality factors for the indium-containing samples are expected to be bias dependent and greater than unity.

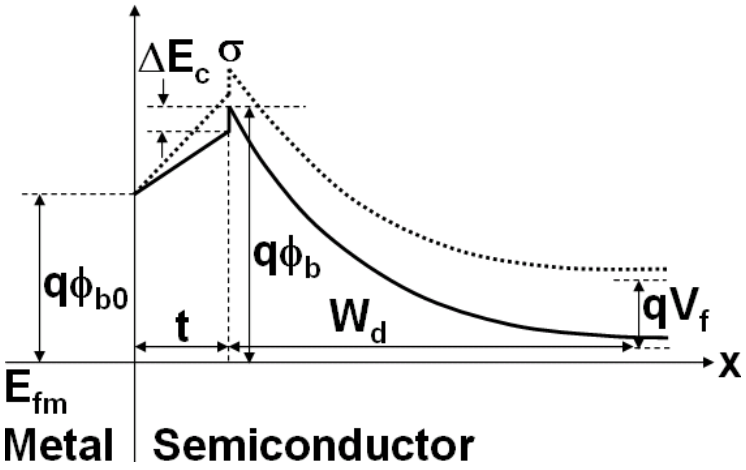

Figure 3-5 Schematic energy band diagram of an InGaN/GaN Schottky barrier under forward bias. E_{fm} is the Fermi level of metal, ΔE_c is the conduction band discontinuity, σ is the sheet polarization charge density at the InGaN/GaN interface, $q\phi_{b0}$ is the barrier height ignoring image force lowering, $q\phi_b$ is the effective barrier height, V_f is the forward bias, t is the InGaN thickness and W_d is the forward bias dependent depletion thickness measured from the InGaN/GaN interface.

Figure 3-6 shows the experimental I-V curves of the control and $In_{0.06}Ga_{0.94}N$-containing samples and the correspondingly theoretical calculations in the semi-logarithmic scale. The ideality factors are 1.08 for the control sample, and 1.33 and 1.30 for the 0nm/$In_{0.06}Ga_{0.94}N$ and 2nm/$In_{0.06}Ga_{0.94}N$ samples, respectively. These results agree well with the values computed from Eq. 3-14. The turn-on voltages for the same samples are ~0.8, ~1.1 and ~1.0 V, respectively, as a result of the increased effective barrier height. The forward I-V calculations are based on Eq. 3-13, and the image force lowering and bias dependent effective barrier height are considered as well. The values of the parameters used for all calculations (including forward and reverse I-V curves) in this work are summarized in Table 3-2.

The experimental I-V curves of the $In_{0.1}Ga_{0.9}N$-containing samples appear to consistently exhibit excess current in the low forward bias region as shown in Figure

3-6(b). The distinctive two-region like I-V characteristics may indicate two current mechanisms exist in the $In_{0.1}Ga_{0.9}N$-containing samples. One component is the TE current which dominates in the high forward bias region; the other may be defect-related tunneling (TU) current which dominates in the low forward bias region. Lower growth temperature for the higher-In-concentration InGaN layers may have induced more defects. The calculated TE current for the $In_{0.1}Ga_{0.9}N$-containing samples fits the experimental curves in the high forward bias region reasonably well. More discussions on the defect-related current will be discussed in the section 3.4.

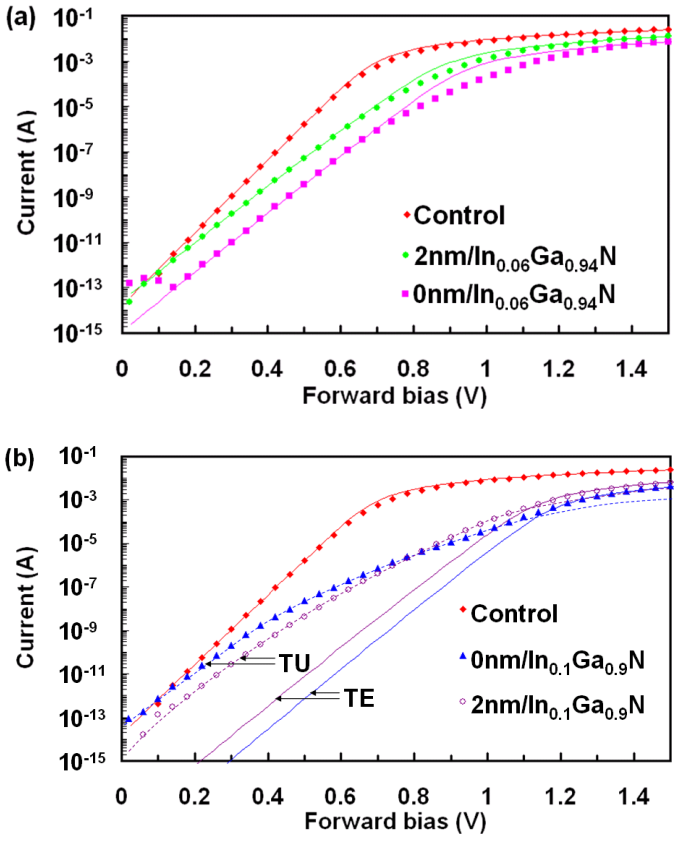

Figure 3-6 Forward I-V curves of the five samples with areas of 5×10^{-5} cm^2. (a) Control and $In_{0.06}Ga_{0.94}N$-containing samples, (b) Control and $In_{0.1}Ga_{0.9}N$-containing samples. The colored dots are measurement data, the solid lines are calculated TE currents and the dash lines are drawn TU currents.

Table 3-2 Values of the parameters used for all calculations (including forward and reverse I-V curves) in this work.[a]

N_d (n^- GaN)	$1.0\sim1.1\times10^{17}$ cm^{-3}	t (InGaN)	15 nm	ϕ_{b0}	0.95~1.05 eV
N_d (InGaN)	$3.5\sim4.5\times10^{17}$ cm^{-3} [b]	t (GaN cap)	2 nm	ΔE_c ($In_{0.06}Ga_{0.94}N$)	0.09 eV [k]
N_d (GaN cap)	5×10^{16} cm^{-3} [c]	σ ($In_{0.06}Ga_{0.94}N$)	$1.7\sim2.0\times10^{12}$ cm^{-2} [g]	ΔE_c ($I_{n0.1}Ga_{0.9}N$)	0.18~0.22eV [l]
ε_{GaN}	$8.9\times\varepsilon_0$ [d]	σ ($In_{0.1}Ga_{0.9}N$)	$2.6\sim3.0\times10^{12}$ cm^{-2} [h]	m^*	$0.2\times m_0$ [m]
$\varepsilon_{In0.06Ga0.94N}$	$9.28\times\varepsilon_0$ [e]	A^*	26.4 $Acm^{-2}K^{-2}$ [i]	R_s	30~70 Ω
$\varepsilon_{In0.1Ga0.9N}$	$9.54\times\varepsilon_0$ [f]	A [j]	5.0×10^{-5} cm^2	T	300 K

[a] The other parameters used in the calculations but not listed here are all theoretical physical constants, e.g. q and k etc.
[b, c] The UID InGaN and GaN are expected to be n-type doped. Reference [19].
[d, e, f] $\varepsilon_0 = 8.85\times10^{-14}$ F/cm is the dielectric constant of vacuum. $\varepsilon_{InxGa1-xN}$ is linearly interpolated values from $\varepsilon_{GaN} = 8.9\times\varepsilon_0$ and $\varepsilon_{InN} = 15.3\times\varepsilon_0$. Reference [15].
[g, h] Estimated values by C-V measurements discussed above.
[i] Reference [14].
[j] A is the diode area.
[k, l] Reference [17].
[m] Reference [15].

3.2.3 Reverse I-V measurements and analysis

Diodes with different areas for all different layer stack designs (as specified in Table 3-1) were fabricated and measured to study the reverse leakage current as a function of diode diameter at fixed reverse bias. The measurement results show that the leakage current is approximately proportional to the corresponding area of the diodes (instead of the diameters), indicating that the leakage current is not dominated by edge effects. Leakage currents of two representative cases (control and 0nm/$In_{0.06}Ga_{0.94}N$) measured at reverse bias of 50 V are plotted against diode areas, as

shown Figure 3-7. The curves suggest that there is a slightly superlinear increase of the leakage current with the diode area. We attribute this effect to a small change in effective Schottky barrier height (SBH) with the diode area. Such a reduction of effective SBH with diode area is also consistent with the experimentally observed forward I-V curves. This effect can be attributed to the fact that the effective SBH can be reduced by the presence of defects, and with increasing diode area (and correspondingly a wider range of defects) the distribution of local effective SBHs across the sample is likely to extend to lower values. More detailed analysis of the effects of the defects on the electrical characteristics of InGaN/GaN Schottky diodes will be discussed in the following sections.

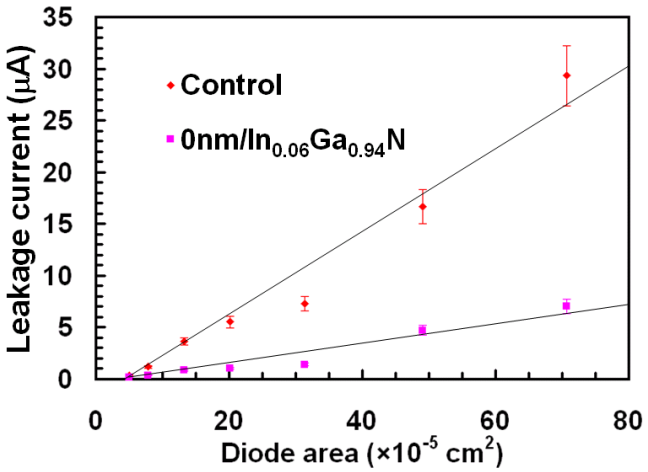

Figure 3-7 Currents at reverse bias 50 V as a function of diode area for the control and 0nm/$In_{0.06}Ga_{0.94}N$ samples. The colored dots are measurement data with 10% error bars and the solid lines are linearly fitting curves.

The experimental and calculated reverse I-V curves are shown in Figure 3-8. For the experimental results shown in Figure 3-8(a), the InGaN surface layer designs significantly reduce the leakage current under high reverse bias. Furthermore, it is

seen that the suppression of leakage current is more effective for layer designs without GaN cap (0nm/$In_{0.06}Ga_{0.94}N$ and 0nm/$In_{0.1}Ga_{0.9}N$) as predicted in Figure 3-3(c). However, it is also noted that the leakage current reduction of the $In_{0.1}Ga_{0.9}N$-containing samples is less than expected. This corresponds well with the less than expected polarization charge density at the $In_{0.1}Ga_{0.9}N$/GaN interface, as extracted from the C-V results. The calculated curves based on Eq. 3-1, fit the experimental curves well in high reverse bias regime as shown in Figures 3-8(b) and 3-8(c). In the cases of control, 2nm/$In_{0.06}Ga_{0.94}N$ and 0nm/$In_{0.06}Ga_{0.94}N$ samples, the last several experimental data points are higher than the calculated values, which is probably due to impact ionization effects at very high surface electric field conditions as mentioned before. In the lower reverse bias regime, the leakage current is expected to be dominated by mechanisms other than direct tunneling described by Eq. 3-1, such as trap/defect center-assisted tunneling and/or generation current.

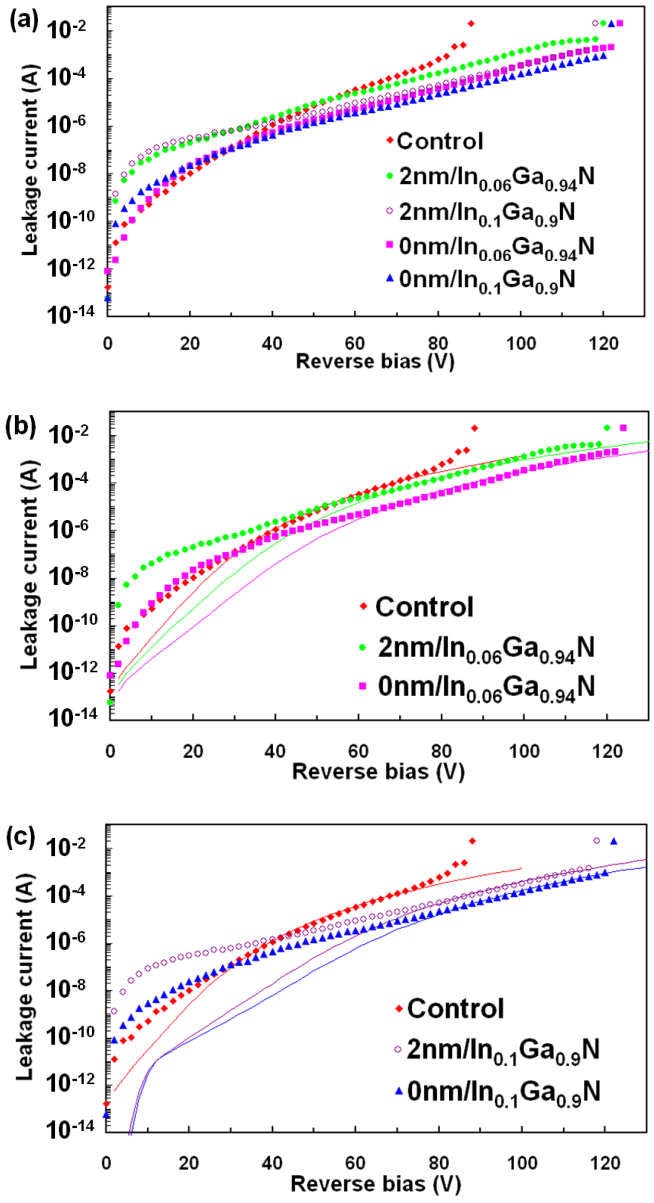

Figure 3-8 Reverse I-V curves of the five samples with area of 5×10^{-5} cm^2. (a) Experimental curves, (b) Experimental and calculated curves of the control and $In_{0.06}Ga_{0.94}N$-containing samples, (c) Experimental and calculated curves of the control and $In_{0.1}Ga_{0.9}N$-containing samples. The colored dots are measurement data and the solid lines are calculated curves.

Significant improvement is also observed in the breakdown voltages for the InGaN surface layer designs which exhibit an increase of ~40 V with respect to the control sample. A histogram of the breakdown voltages for the control and InGaN-

containing samples is shown in Figure 3-9. To ensure the validity of this statistics, the data of the control and InGaN-containing diodes shown here come from different fabricated samples and different grown wafers.

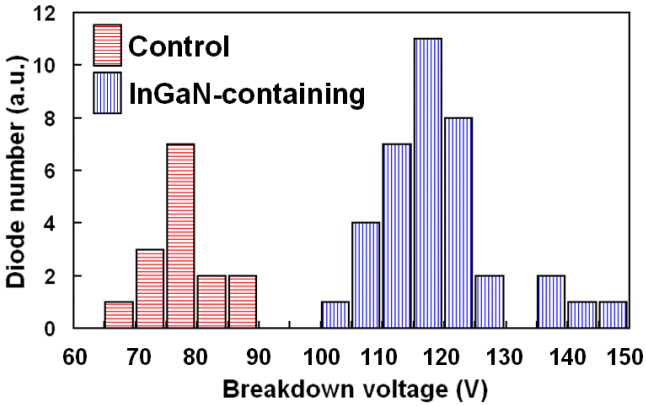

Figure 3-9 The histogram of the breakdown voltages for the control and InGaN-containing diodes.

3.3 Leakage current reduction using higher pressure GaN buffer

MOCVD grown III-N epitaxial layers suffer from high dislocation density due to the highly lattice-mismatched growth substrates, such as the sapphire used in this work [20]. The excess reverse leakage current of the III-N-based Schottky diodes has been reported to be dislocation related [5], [21]. It has also been reported that compared to conventional low-pressure (LP) MOCVD growth, the higher pressure (HP) MOCVD growth technique favors reduction of the dislocation density, and

growth of high-quality GaN layers, although there will be an increase in the gas-phase parasitic reactions [9], [22]. In our work, we applied the HP MOCVD growth technique to the GaN buffer layer to reduce the dislocation density but used the LP MOCVD growth for other layers to minimize the parasitic gas-phase reactions. For comparison purposes, a control and a 2nm/$In_{0.1}Ga_{0.9}N$ samples using HP GaN buffer were grown, labeled as Control_HP and 2nm/$In_{0.1}Ga_{0.9}N$_HP, respectively. The growth and fabrication details are the same as for the samples discussed above, except the higher growth pressure of the GaN buffer layer as shown in Table 3-1. The full width at half maximum (FWHM) of the (0002) XRD rocking curve of the samples using HP GaN buffer was ~284 arcsec, in comparison with the ~337 arcsec of the samples using LP GaN buffer, indicating lower dislocation density and the better layer quality [23]. As shown in Figure 3-10, the corresponding reverse I-V curves of the samples using HP GaN buffer exhibit significantly less leakage current and higher breakdown voltages compared to that of the samples using LP GaN buffer.

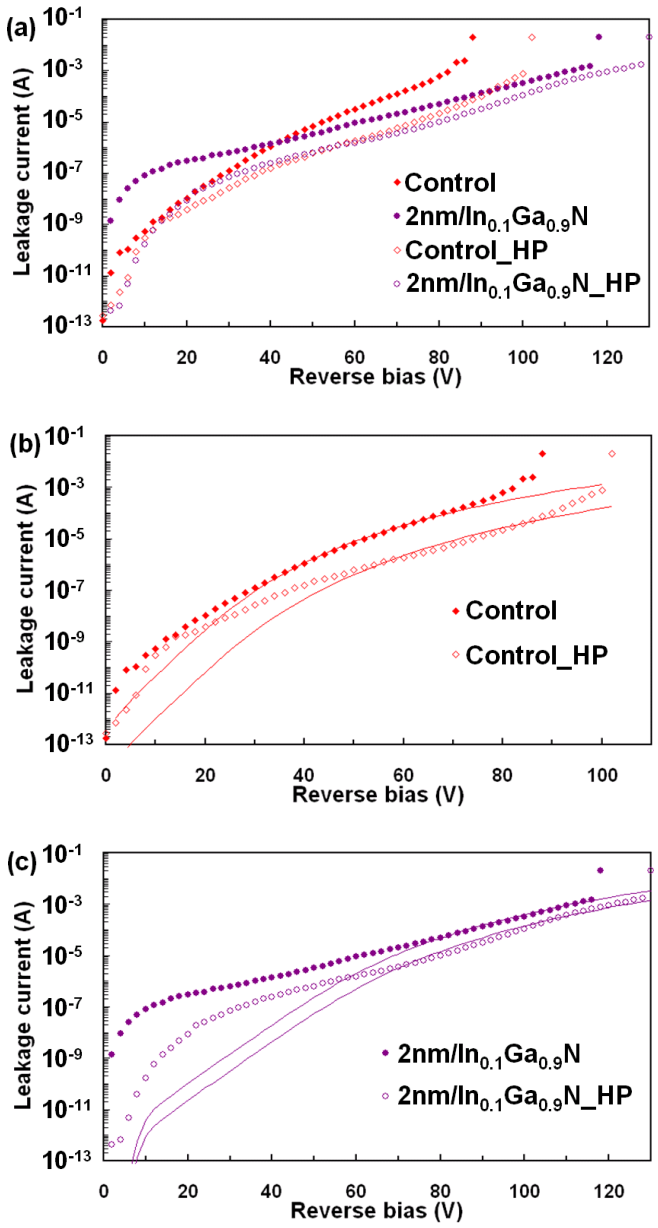

Figure 3-10 Reverse I-V curves of the samples using HP and LP GaN buffer layers with area of 5×10^{-5} cm^2. (a) Experimental curves, (b) Experimental and calculated curves of the Control and Control_HP samples, (c) Experimental and calculated curves of the 2nm/$In_{0.1}Ga_{0.9}N$ and 2nm/$In_{0.1}Ga_{0.9}N$_HP samples. The colored dots are experimental data and the solid lines are calculated curves.

We verified by C-V measurements that the improved characteristics are not the result of changed doping level, since we measured $N_d \approx 1\times10^{17}$ cm^{-3} for the n^- GaN

layer for the samples with both types of GaN buffers. As shown in Figure 3-10(b) and (c) and 3-11, the significantly reduced leakage current and the forward current for the samples using HP GaN buffer can be fit with the expressions outlined above, with only increasing SBHs by 0.1 and 0.05 eV for the Control_HP and 2nm/$In_{0.1}Ga_{0.9}N$_HP samples compared to the Control and 2nm//$In_{0.1}Ga_{0.9}N$ samples, respectively. In Figure 3-11, the defect-related current is not observed in the low forward bias region for the samples using HP GaN buffer, which indicates lower defect densities in these samples. This is consistent with our XRD measurement results. In Figure 3-12, the histogram of the extracted SBHs from the experimental forward I-V curves also exhibits an average of ~0.1-eV higher SBH for the Control_HP samples relative to the Control samples. The significant SBH increase of the samples using HP GaN buffer can be attributed to the different defects densities in the materials caused by the different buffer layer growth pressures. More detailed studies and explanations will be presented in the following section.

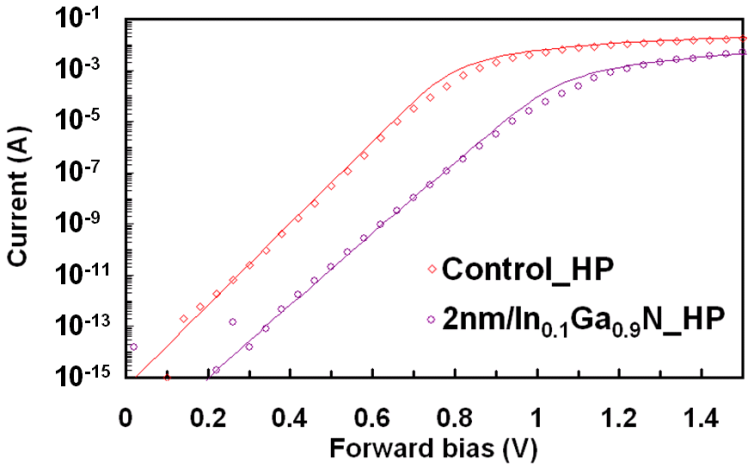

Figure 3-11 Forward *I-V* curves of the Control_HP and 2nm/$In_{0.1}Ga_{0.9}N$_HP samples with area of 5×10^{-5} cm^2. The colored dots are experimental data and the solid lines are calculated TE currents.

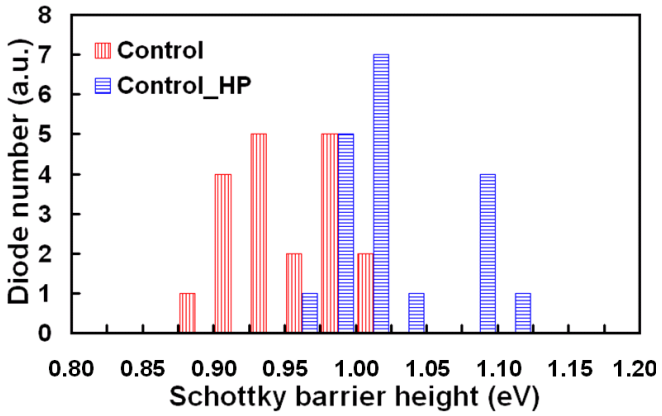

Figure 3-12 The histogram of SBHs extracted from the experimental forward I-V curves of the Control and Control_HP samples.

3.4 InGaN/GaN material growth and characterization

All materials were grown using a Thomas Swan close-coupled showerhead 3×2'' MOCVD system. Material characterizations including the investigations of surface morphology, defects, electrical and thermal properties were carefully performed.

3.4.1 InGaN/GaN MOCVD growth

Figure 3-13 shows the Thomas Swan close-coupled showerhead (CCS) 3×2'' MOCVD system. This commercial MOCVD reactor uses vertical laminar flow technology in which group Ⅲ (TMGa, TEGa, TMAl and TMIn) and group Ⅴ (NH_3) precursors enter separately into the reaction chamber through the showerhead. The precursors' pre-reactions are effectively avoided. The showerhead has a high density of 100 tubes/inch^2 with a tube diameter of 0.6 mm which ensures the uniformity of the gas flow into the reactor chamber. Moreover, the system provides the adjustment of the showerhead to susceptor gap in the range of 5 mm to 25 mm. With this adjustment, a better quality GaN film with lower threading dislocation density (estimated by XRD rocking curve) can be grown, which we believe is due to the reduction of the residence time of the precursors (less parasitic gas phase reaction) in the reactor chamber.

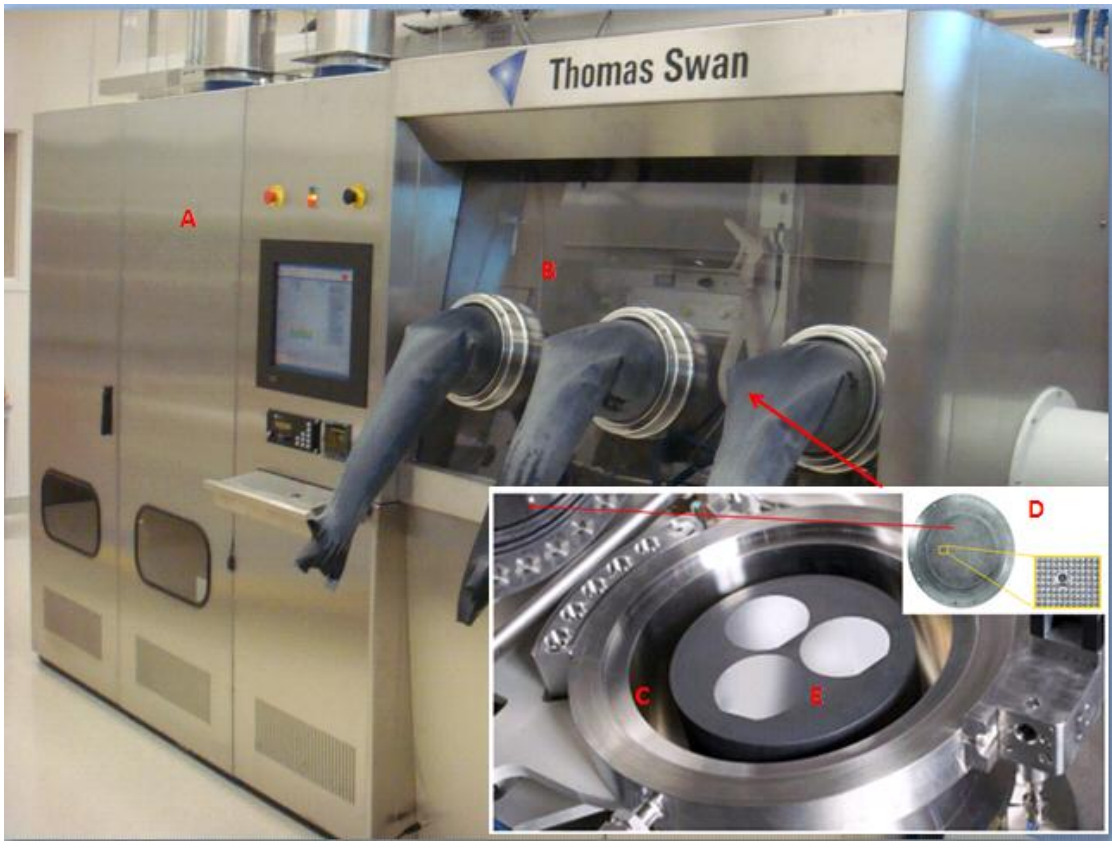

Figure 3-13 Thomas Swan close-coupled showerhead (CCS) 3×2'' MOCVD system. A: Metal-organic sources cabinet; B: Glove box; C: Reactor chamber; D: Showerhead; E: Susceptor.

For growing GaN on c-Sapphire using MOCVD, we used the traditional low-temperature (LT: 530 ^{o}C) GaN nucleation layer method followed by high-temperature (HT: 1040 ^{o}C) GaN buffer layer for the material growth [16]. The substrates used were 2-inch c-plane sapphire with a 0.1-degree off-cut towards the m-plane. Trimethylgallium (TMGa), ammonia (NH_3) and silane (SiH_4) were used as Ga, N precursors and n-type Si dopant, respectively; for InGaN growth, Triethylgallium (TEGa), Trimethylindium (TMIn) and NH_3 were used as Ga, In and N precursors, respectively. H_2 and N_2 were used as carrier gases for GaN and InGaN growth,

respectively. Thick InGaN samples (> 300 nm to ensure full strain relaxation [24]) were grown for estimating the indium concentration and optimizing the InGaN growth by X-ray diffraction (XRD) measurements. Figure 3-14 shows the dependence of indium percentage and FWHM of (0002) XRC on growth temperature and molar flow ratio of TMIn/(TMIn+TMGa). Based on these results and the design considerations discussed in section 3.2, the InGaN films used in the InGaN surface layer design were grown using TMIn, TEGa and NH_3 flows of 9.26 μmol/min, 8.16 μmol/min and 165 mmol/min, respectively, at 820 ^oC for the $In_{0.06}Ga_{0.94}N$ layer growth; 5.95 μmol/min, 5.25 μmol/min and 165 mmol/min, respectively, at 808 ^oC for the $In_{0.1}Ga_{0.9}N$ layer growth.

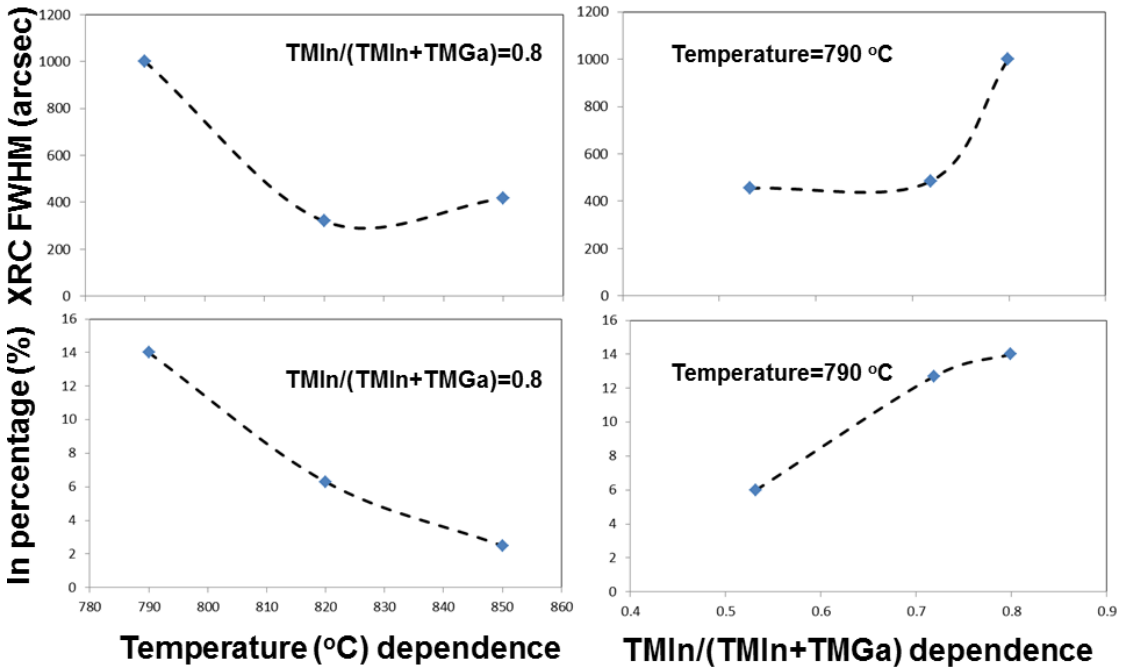

Figure 3-14 The indium percentage and FWHMs of (0002) X-ray rocking curve (XRC) of thick InGaN films for different growth temperatures and molar flow ratios of TMIn/(TMIn+TMGa) during growth.

3.4.2 InGaN/GaN material characterization

As we discussed above, InGaN surface layer design can offer great benefits in increasing breakdown voltage and decreasing reverse leakage current. Additionally, InGaN/GaN, as one of the prevalent III-nitride heterostructure combinations, has attracted intense interest in relation to light emitting diodes (LEDs) [25], [26], heterojunction bipolar transistors (HBTs) [27], [28], and high power electronic devices, including power varactors [4], [29]. However, the effects of film quality (especially defects) on the electrical characteristics of the InGaN/GaN Schottky diodes should also be investigated. Due to the large lattice mismatch and thermal expansion mismatch to the foreign (e.g., c-Sapphire and Si) substrates, epi-grown nitride materials suffer from a variety of defects, such as threading dislocations (TDs), stacking faults, inversion domain boundaries and nanopipes [30], [31]. Although not all defects are detrimental to device performance since long-lived LEDs and lasers can be fabricated on nitride materials even with 10^8-cm^{-2} dislocation density, the effects of these defects on device characteristics are still topics of considerable interest. This section reports the observation of surface micromesa defects in InGaN/GaN materials and addresses the relationship between dislocations and surface micromesas in the InGaN/GaN system and shows that micromesas are associated with excess leakage

currents in InGaN/GaN Schottky barrier diodes, especially at higher annealing temperatures.

3.4.2.1 Reported defects in GaN and InGaN materials

Previous work has elucidated many of the characteristics of GaN and InGaN defects. Nanopipes, with radii of 35 to 500 Å, in MOCVD-grown GaN epi-layers were first reported by Qian et al [31]. Their scanning force microscopy (SFM) and high-resolution transmission electron microscopy (TEM) studies revealed that the nanopipes are open cores of screw TDs [32]. These hollow pipes were predicted earlier by Frank, who noted that for a dislocation whose Burgers vector exceeds a critical value, there exists a local equilibrium state in which the dislocation core is an empty tube [33]. Similar defects, named micropipes (with sizes more than two orders of magnitude larger than those of the nanopipes observed in GaN), are frequently observed in SiC, another wide bandgap semiconductor with hexagonal crystal structure [34], [35]. The micropipes in SiC can be observed by optical microscope and have been reported to be detrimental to the performance of devices. Neudeck et al. reported that micropipes are the main source of electrical breakdowns in SiC p-n junction diodes and limiting factors for applications of SiC in high-power, high-frequency, and high-temperature electronic devices [36], [37]. In contrast to the micropipes in SiC, the nanopipes in GaN cannot be observed by optical microscopy because of their small sizes; usually TEM or wet chemical etching techniques are

required to observe them[32], [38], [39]. Therefore, it is difficult to study the direct correlation between the nanopipes and the electrical characteristics of the nitride devices.

In this section, we investigated the surface defects in MOCVD-grown InGaN/GaN materials by Nomarski optical microscopy (NOM), scanning electron microscopy (SEM) and atomic force microscopy (AFM). Different growth pressures for GaN buffer layers were used to vary the material defect density [9], [40]. After adding a thin surface layer of InGaN, micro-scale surface mesas were observed by NOM. We were able to use a large-scale defect mapping method before and after hot phosphoric acid (H_3PO_4) etching to analyze the origin of the surface micromesas and relate them to nanopipes. Direct NOM observation of the micromesas allowed us to study the effects of micromesas, and by inference, nanopipes, on reverse leakage current in Ni-InGaN/GaN Schottky barriers. Detailed surface topography of micromesas was investigated by SEM and AFM. We previously discussed the breakdown characteristics improvement of GaN Schottky diodes by adding a thin InGaN surface layer. Here we further study the reverse leakage current in InGaN/GaN Schottky barriers with extensive measurements of reverse leakage current versus diode dimension and micromesa number before and after thermal annealing at different temperatures. We show an increase of leakage current with thermal annealing, which is sometimes an essential step in device fabrication (e.g. thermally curing polymers for metal isolation). RBS measurements are also used to study the inter-diffusion between Ni and InGaN/GaN at different annealing temperatures. We conclude that the micromesas are the main source of leakage in these structures. We show that high

pressure epitaxial growth can significantly reduce micromesa density and thus leakage current.

3.4.2.2 Experimental procedures

The structure of the Schottky barrier diodes investigated in this section is shown in Figure 3-15(a). The materials were processed into circular mesa diodes of the form illustrated in Figure 3-15(b). The Nomarski micrograph of the diode illustrated shows the presence of surface micromesas.

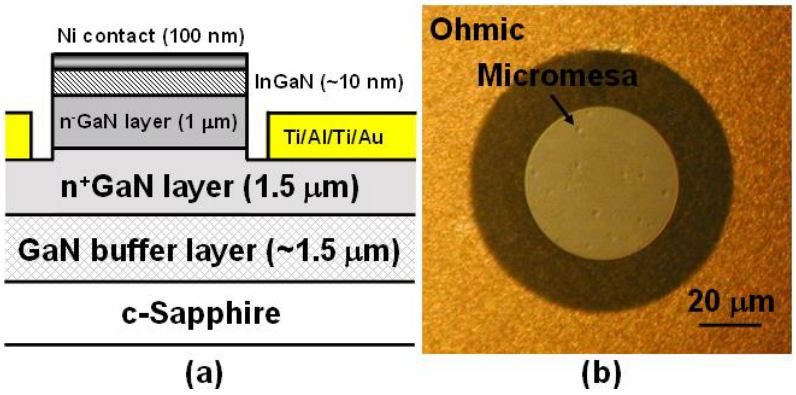

Figure 3-15 a) Schematic cross section of the InGaN/GaN Schottky diode and (b) the Nomarski optical microscopy top view of a real diode with surface micromesas.

Growth details and sample labels are summarized in Table 3-3. Low pressure (LP) growths utilized 300 mbar pressure for the buffer layer growth, while high pressure (HP) samples employed 900 mbar in this step. The HP (near-atmosphere pressure) buffer layer growth was found to reduce the defect density [9], [40]. For HP_InGaN/GaN and LP_InGaN/GaN samples, there were ~ 10-nm InGaN surface

layers grown on top. After the MOCVD growth, the wafers were diced into 1×1 cm^2 squares for various experiments.

Table 3-3 Sample labels and key growth details used in this work.[a]

Sample labels	LP_GaN	LP_InGaN/GaN	HP_ GaN	HP_InGaN/GaN
InGaN layer	N.A.	~6% In, ~10 nm, 400 mbar, 808 ^{o}C	N.A.	~6% In, ~10 nm, 400 mbar, 808 ^{o}C
Common layers	n^- GaN ($n \approx 1 \times 10^{17}$ cm^{-3}, 1 μm), 200 mbar, 1040 ^{o}C			
	n^+ GaN ($n \approx 5 \times 10^{18}$ cm^{-3}, 1.5 μm), 200 mbar, 1040 ^{o}C			
	GaN buffer (~1.5 μm), 300 mbar for low pressure (LP), 900 mbar for high pressure (HP) GaN buffer, 1040 ^{o}C			
	Low-temperature GaN nucleation layer (~20 nm), 600 mbar, 530 ^{o}C			
	c-Sapphire substrate			

[a] The coalescence time for HP buffer and LP buffer is ~50 mins and ~10 mins, respectively; the growth rate for HP buffer an LP buffer is ~0.52 nm/s and ~0.46 nm/s, respectively; and the InGaN growth rate is ~0.0326 nm/s.

3.4.2.3 X-ray diffraction measurements

Full width at half maximum (FWHM) of symmetric (0002) and asymmetric (10-12) x-ray rocking curves (XRCs) were measured to compare the threading dislocation densities in these four samples. The results are included in Table 3-4. It is known that the FWHM of the symmetric (0002) XRC is broadened by screw- and

mixed-type threading dislocations and the asymmetric (10-12) XRC is broadened by all TDs [41], [42]. Narrower FWHM of the samples (HP_GaN and HP_InGaN/GaN) using higher growth pressure for GaN buffer layers indicates lower edge-, screw- and mixed-type TD densities than those of the samples (LP_GaN and LP_InGaN/GaN) using low pressure growth for GaN buffer layers.

Table 3-4 FWHM of symmetric (0002) and asymmetric (10-12) XRCs, surface micromesa density estimated under Nomarski optical microscopy and nanopipe and TD densities estimated by EPD in all samples.

Sample label	FWHM of (0002)/(10-12) XRCs (arcsec)	Micromesa density by NOM (before etch) (cm^{-2})	Nanopipe density by EPD (cm^{-2})	TD density by EPD from AFM (cm^{-2})
HP_InGaN/GaN	276/325	1.6×10^{5}	1.9×10^{5}	1.5×10^{8}
LP_InGaN/GaN	347/476	5.8×10^{5}	6.8×10^{5}	2.8×10^{8}
HP_GaN	281/334	0	2.5×10^{5}	1.6×10^{8}
LP_GaN	338/440	0	9.1×10^{5}	3.0×10^{8}

3.4.2.4 Nomarski microscope imaging

Smooth surfaces are observed for the GaN-only (LP_GaN and HP_GaN) samples, while large surface mesas, with density in the range of 10^5 cm^{-2}, are optically observable on the LP_InGaN/GaN and HP_InGaN/GaN samples as shown in Figure 3-16 with only ~ 10-nm InGaN top layers. These surface mesas are typically 1~2 μm in diameter and less than 30 nm in height on our ~10-nm InGaN containing samples from NOM and AFM measurements. Corresponding with lower TD density estimated

by XRC measurements, the InGaN/GaN sample grown using higher growth pressure for the GaN buffer layer also shows a much lower surface micromesa density as shown in Table 3-4.

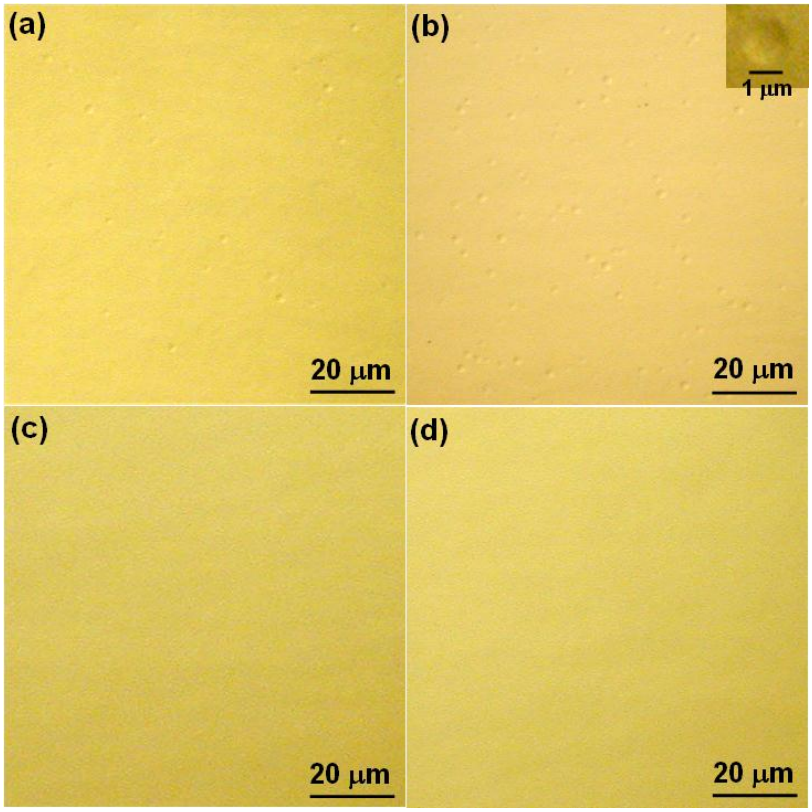

Figure 3-16 Nomarski optical microscopy images of (a) HP_InGaN/GaN, (b) LP_InGaN/GaN, (c) HP_GaN and (d) LP_GaN. The inset in (b) is a zoom-in image of one surface micromesa.

3.4.2.5 Surface topography investigation by SEM and AFM

Representative SEM and AFM micrographs of the surface micromesas on InGaN/GaN samples are shown in Figure 3-17. The micromesa shows spiral steps, which typically emerge from a nanopipe. By carefully examining the height of the

different resolvable steps showing in Figure 3-17(b), the step heights were found to be around several nanometers, roughly with a greatest common divisor (GCD) of 5.4±0.3 Å. This GCD is consistent with the expected value of c-lattice constant of InGaN (5.19 Å and 5.69 Å for GaN and InN, respectively) [43]. The measured step heights that are integer multiples (typically 2~4) of the GCD (~ c-lattice constant of InGaN) are consistent with the step sizes reported for growth spirals in other material systems, and can be attributed to step bunching [44].

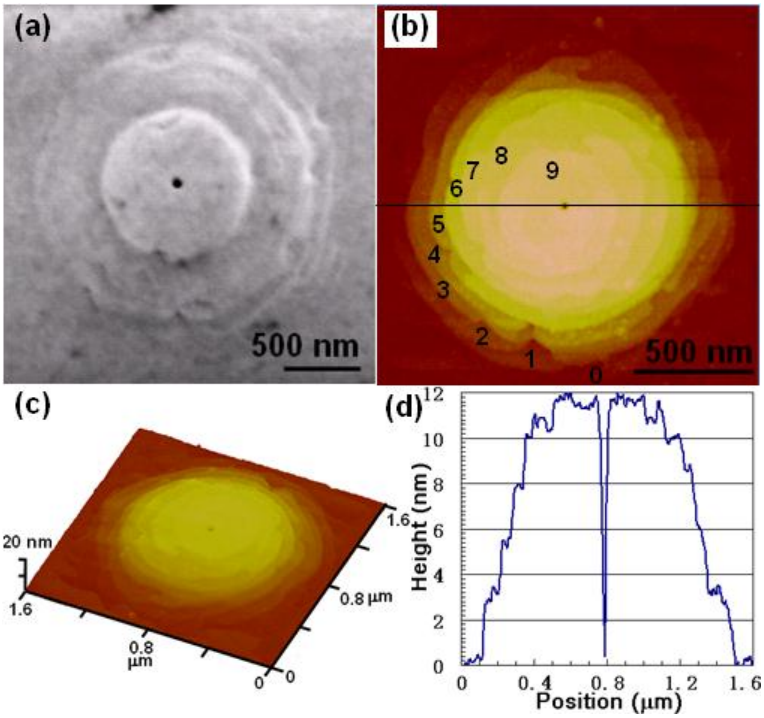

Figure 3-17 Representative SEM and AFM (tapping mode) micrographs of the surface micromesas. (a) A SEM micrograph; (b) An AFM micrograph; (c) 3-D AFM micrograph of (b); and (d) surface profile along the line shown in (b). (b), (c) and (d) are from the same micromesa and (a) is from a different one. Numbers in (b) indicate the resolvable spiral steps.

3.4.2.6 Etch pit density measurements

All samples were immersed into 180-^{o}C H_3PO_4 for 7 minutes to perform the etch pit density (EPD) measurements [45], and followed by NOM, SEM and AFM investigations to analyze the etch pit type and density. Figure 3-18 shows the AFM images of the etched HP_InGaN/GaN and LP_InGaN/GaN samples and their corresponding surface profiles. The TD densities in the range of 10^8 cm^{-2} in these samples can be estimated by counting the etch pits in these images.

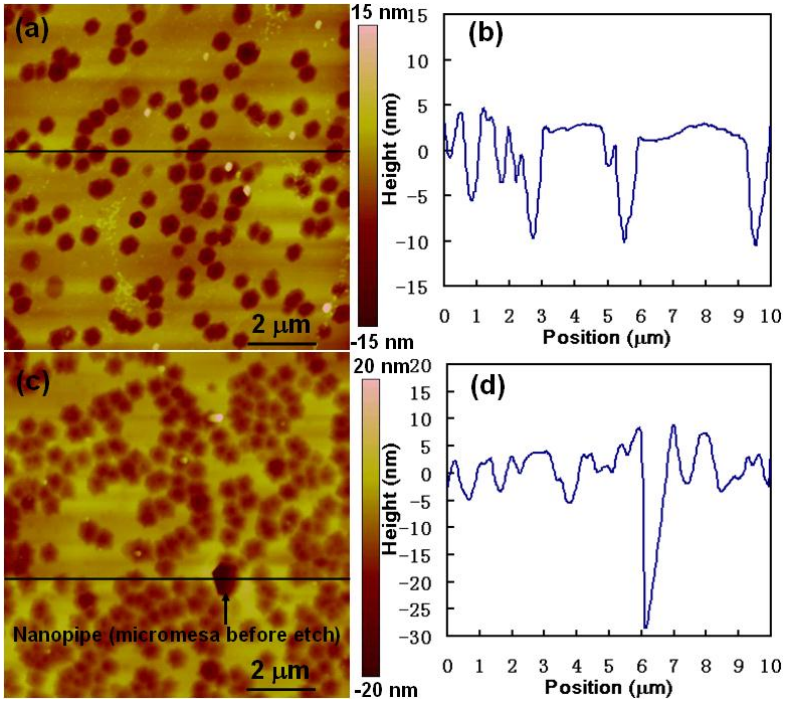

Figure 3-18 10×10 μm^2 AFM images of (a) HP_InGaN/GaN, (b) surface profile along the line in (a), (c) LP_InGaN/GaN, and (d) surface profile along the line in (c) after H_3PO_4 etch.

Although the SEM and AFM micrographs in Figure 3-17 show that the surface micromesas grow spirally around the nanopipes, the scanning areas for these two techniques are too small to conclusively identify the origin of the surface micromesas. Therefore, for the LP_InGaN/GaN sample, surface micromesas (before etch) and etch pits were mapped using NOM over a large area for further characterization. For better comparison, two representative small parts of the zoomed-in mapped images are shown in Figure 3-19. The small etch pits that correspond to the TDs shown in the AFM images cannot be observed by NOM. The observable etch pits (black dots) under the NOM shown in Figure 3-19(b) represent the same type of defect as the large etch pit shown in the AFM image in Figure 3-18(c) (indicated by an arrow), which is clearly different from the other small TD-related etch pits in the AFM images. These large etch pits have a density in the range of 10^5 cm^{-2}, which is three orders of magnitude lower than the TD density.

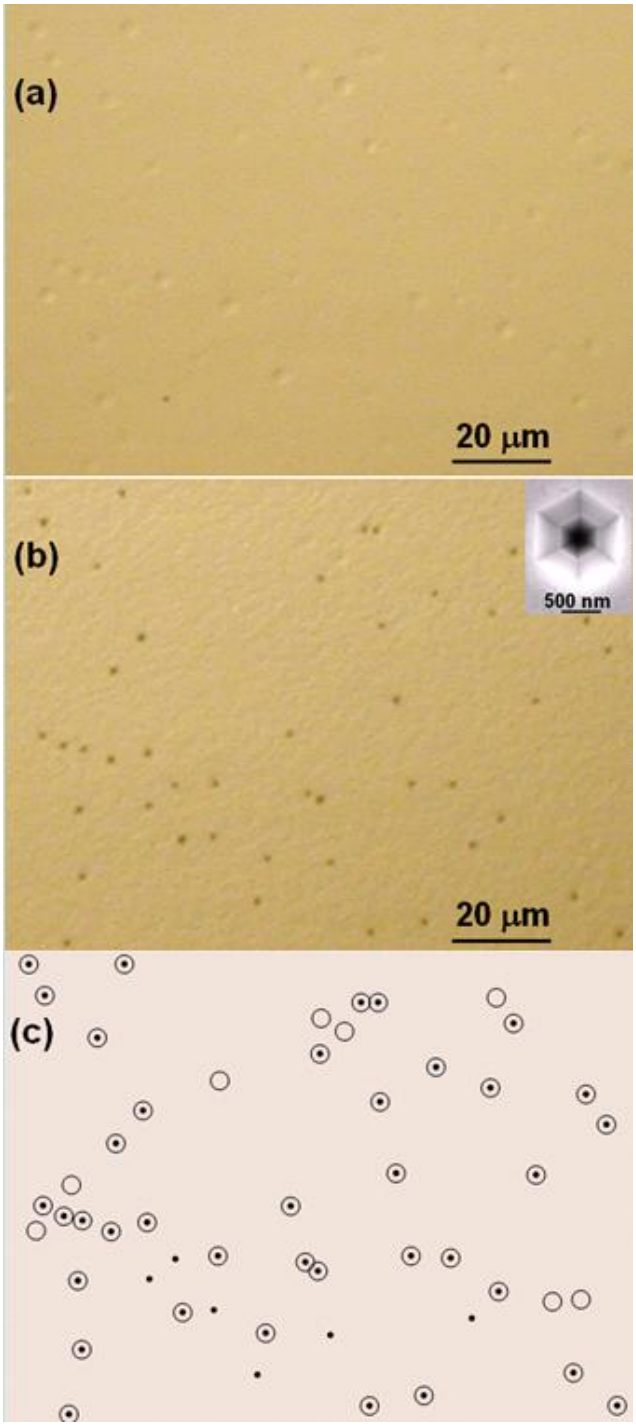

Figure 3-19 Surface micromesa mapping by Nomarski optical microscopy. (a) Surface micromesas before etch and (b) etch pits in the same area of a LP_InGaN/GaN sample. (c) A schematic superposition of image (a) and (b). The inset in (b) is a representative SEM image of a large etch pit shown in (b). The circles and dots in (c) represent the surface micromesas and nanopipe-related etch pits, respectively.

3.4.2.7 Discussion of material defect characterization

Hong et al. performed thorough TEM studies of the origin of the hexagonal-shaped etch pits in (0001) GaN films, and concluded that these etch pits with a density 2~4 orders of magnitude lower than the TD density originated from nanopipes (open-core screw TDs) [38], [46]. The 10^5 cm^{-2} EPD that was measured is also quite close to those reported nanopipe densities in MOCVD-grown GaN films [31], [32]. Based on our consistent observations with their TEM studies, we believe that the large etch pits in the AFM and NOM images originate from nanopipes.

Furthermore, from the mapping images shown in Figure 3-19, it can be clearly seen that most of the surface micromesas (~ 80%) form nanopipe-related etch pits. This is consistent with the micromesa observations under SEM and AFM shown in Figure 3-17. In accordance with the aforementioned TEM studies, the hexagonal-shaped etch pit shown in the inset of Figure 3-19(b) is formed by etching along the nanopipe at the center of the micromesa shown in Figure 3-17. Indium incorporation at lower growth temperatures is considered an important factor in the formation of surface micromesas, since no surface micromesas were observed on the GaN-only samples. Indium atoms have much higher surface mobility on the GaN surface than Ga atoms at the lower InGaN growth temperature, giving them higher probability to occupy the lowest energy sites and form spiral steps around the nanopipes [47], [48]. The roughly extracted c-lattice constant value of 5.4±0.3 Å from the AFM micrograph

of the surface micromesa also suggests a high indium concentration in the micromesa area. The indium segregation around nanopipes (open-core screw TDs) has also been observed by energy dispersive x-ray (EDX) measurements in InAlN/GaN systems [49]. Therefore, we may speculate that the surface micromesa is formed by indium-rich spiral growth around nanopipes at lower InGaN growth temperatures with a growth rate that is higher than that of the planar growth on the remaining GaN surface. As shown schematically in Figure 3-19(c) with the superposition of the two mapping images, some surface micromesas that do not form nanopipe-related etch pits and some nanopipe-related etch pits that do not correspond to optically observable micromesas were also observed. Figure 3-20 shows corresponding micrographs of the surface micromesas (with and without nanopipes at the center) and a nanopipe (without formation of a surface micromesa) that were found consistent with the observations in the mapping images in Figure 3-19(c). The former case could be attributable to the formation of surface micromesas around some defect other than a nanopipe (e.g. stacking fault within the InGaN layer due to strain relaxation) [50]; the latter case could be due to inhibition of spiral growth around nanopipes due to the local strain in the InGaN layer. These tentative explanations, however, need to be further investigated.

Table 3-4 summarizes the results of XRC measurements and surface micromesa and TD densities for the four samples. The surface micromesa, nanopipe, and TD densities in HP_GaN and HP_InGaN/GaN samples are lower as expected, which is consistent with their narrower FWHM of XRCs. In the InGaN/GaN samples, the surface micromesa density of ~10^5 cm^{-2} is close to the nanopipe density and much

lower than the TD density of ~10^8 cm^{-2}. This is also a good indication that the surface micromesas have a close relationship with nanopipes but little relationship with other TDs. In addition, the reduction of nanopipe-related EPD by adding a thin InGaN surface layer (9.1×10^5 cm^{-2} to 6.8×10^5 cm^{-2} between LP_GaN and LP_InGaN/GaN, and 2.5×10^5 cm^{-2} to 1.9×10^5 cm^{-2} between HP_GaN and HP_InGaN/GaN, respectively) is significant. However, the additional InGaN surface layer does not introduce too much TD density change. This observation is in agreement with Ono et al.'s work [39].

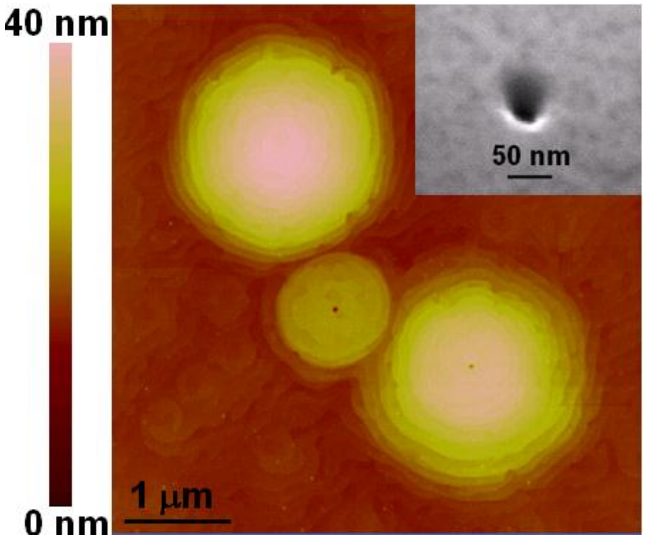

Figure 3-20 An AFM (tapping mode) micrograph of surface micromesas with and without nanopipes at the center. The inset is a SEM image of a nanopipe without formation of a surface micromesa on the InGaN/GaN sample.

3.4.3 Electrical characteristics of InGaN/GaN Schottky diodes

HP_InGaN/GaN and LP_InGaN/GaN samples were fabricated into Schottky diodes with different diameters in the range of 17 μm to 280 μm, followed the fabrication procedure mentioned in section 2-1, to investigate their electrical characteristics.

The I-V characteristics were measured on different sizes of diodes. The relation between leakage current at a reverse bias (V_r) of 30 V and diode diameter is shown in Figure 3-21. The data trend which follows the slope-of-two line (except for the smallest HP_InGaN/GaN diodes) on a logarithmic scale indicates that the leakage current is proportional to the corresponding area of the diodes, instead of being dominated by edge effects. The HP_InGaN/GaN Schottky diodes with lower surface micromesa and nanopipe density showed about two orders of magnitude lower leakage current than that of LP_InGaN/GaN diodes. From the estimated micromesa density shown in Table 3-4, the average area per micromesa is 625 μm^2 for HP_InGaN/GaN and 172 μm^2 for LP_InGaN/GaN, which in turn correspond to critical diameters D_c of 28 μm and 15 μm, respectively. Diodes without micromesas are expected to occur (on a probabilistic basis) when diode diameter becomes close to or smaller than D_c. As seen from Figure 3-21, the smallest LP_InGaN/GaN Schottky diodes with diameters of 17 μm (close to the value of D_c for this wafer of 15 μm), showed large scattering of leakage currents around their slope-of-two trend; the smallest HP_InGaN/GaN Schottky diodes with diameters of 17 μm (much smaller than the value D_c of for this

wafer, 28 μm) showed significantly lower leakage current than their slope-of-two trend. This suggests that the micromesas are likely a major leakage path in the InGaN/GaN Schottky diodes.

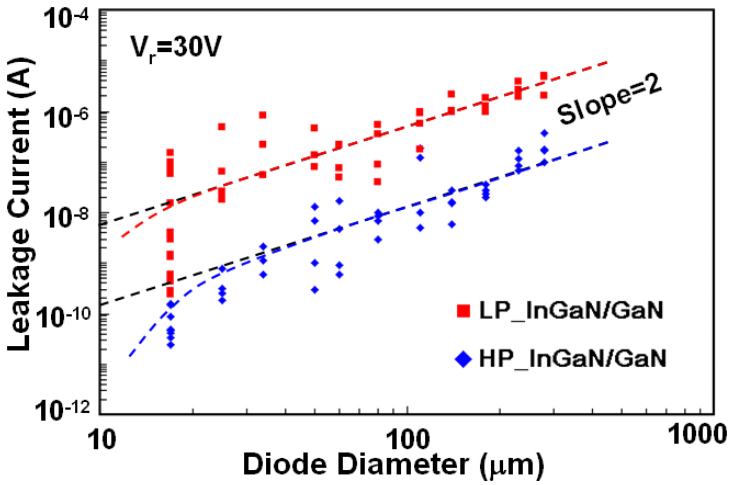

Figure 3-21 Leakage current at a reverse bias of 30 V versus diode diameter for LP_InGaN/GaN and HP_InGaN/GaN Schottky diodes. The black dashed lines have slope of two and the color dashed curves represent the trend of measured data points.

To confirm the relationship, the number of micromesas for each of the smallest (17-μm diameter) Ni-InGaN/GaN Schottky diodes was first counted under NOM and then a study of their forward and reverse I-V characteristics was performed. Figure 3-22 shows the relation between leakage current at V_r = 30 V and micromesa number on the smallest diodes. It is clear that the leakage current increases with the increase of micromesa number. Representative forward I-V curves for the smallest diodes without and with surface micromesas are shown in Figure 3-23. In Figure 3-23(a), the I-V curve for the diode without surface micromesa has an ideality factor of ~1.3, which is larger than unity due to the polarization charge (at the InGaN/GaN interface)-induced

Schottky barrier height (SBH) increase as forward bias increases as we discussed in section 3.2.2. The corresponding calculations based on thermionic emission (TE) theory fit the experimental curve well using Eq. 3-13. In Figure 3-23(b), I-V curves with two distinctive turn-on mechanisms were usually observed for the diodes with surface micromesas. The first turn-on mechanism in the low bias region can be modeled as due to the surface micromesa with lower SBH and higher series resistance (R_s) (due to its small area); the second turn-on mechanism, associated with the high bias region, originates from the normal InGaN/GaN Schottky barrier, with higher SBH and lower R_s. A simplistic equivalent circuit diagram for explaining this two turn-on phenomenon was also proposed in the Figure 3-23(b). In the TE-based calculations, using effective SBHs of micromesas 0.3~0.5 eV lower than effective SBHs of Ni-InGaN/GaN (~1.1 eV), and R_s of micromesa around two orders of magnitude larger (due to <1% micromesa area) than R_s of Ni-InGaN/GaN can match the experimental curves quite well. The lower effective SBH is likely caused by the lower conduction band edge (E_c) of InGaN and partial strain relaxation at the InGaN/GaN interface due to higher indium concentration and larger InGaN layer thickness (estimated by AFM) in the micromesa area.

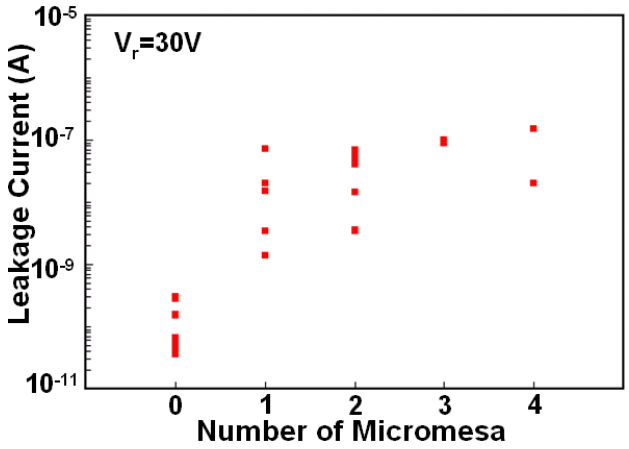

Figure 3-22 Leakage current at a reverse bias of 30 V versus micromesa number on the smallest (17-μm diameter) LP_InGaN/GaN and HP_InGaN/GaN Schottky diodes.

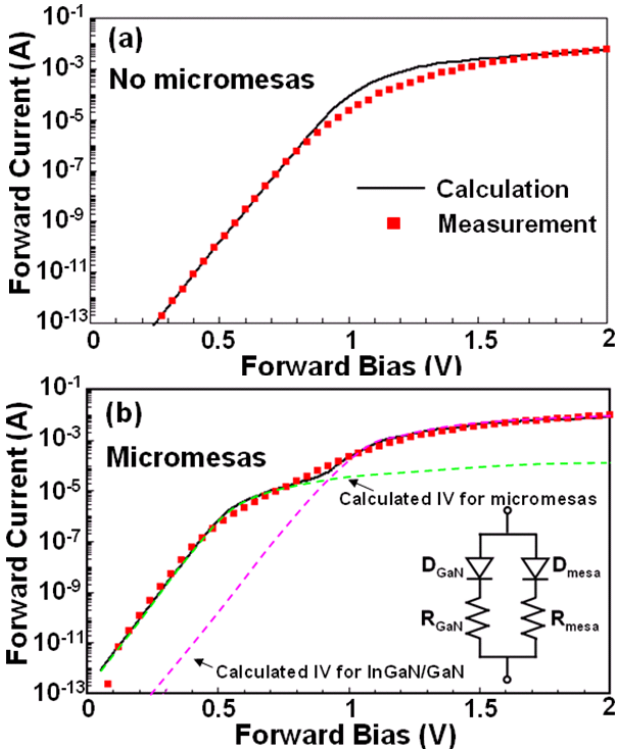

Figure 3-23 Representative forward I-V curves for the smallest (17-μm diameter) Ni-InGaN/GaN Schottky barriers (a) without surface micromesas and (b) with surface micromesas. The red dots are measured data and the solid black curves are calculated thermionic emission (TE) currents. In (b), the green and pink dashed curves represent the calculated TE currents for micromesas and InGaN/GaN, respectively. The black solid curve is the summation of the two dashed curves. The inset is the equivalent circuit diagram of the InGaN/GaN Schottky diodes with surface micromesas.

Representative reverse-bias I-V curves and the corresponding calculated curves for the smallest InGaN/GaN Schottky diodes are shown in Figure 3-24. The calculations based on electron tunneling through the Schottky barrier under reverse biases fit the experimental curves well in the high-bias regime as we discussed in section 3.1. In the low-bias regime, the tunneling current is much lower than the equipment noise current and is difficult to measure. In Figure 3-24(b), it is clearly seen that when miocromesas exist, the micromesas with effective SBHs 0.3~0.5 eV lower than that of InGaN/GaN were the main source of the leakage current even though they only occupy ~ <1% area of the diode.

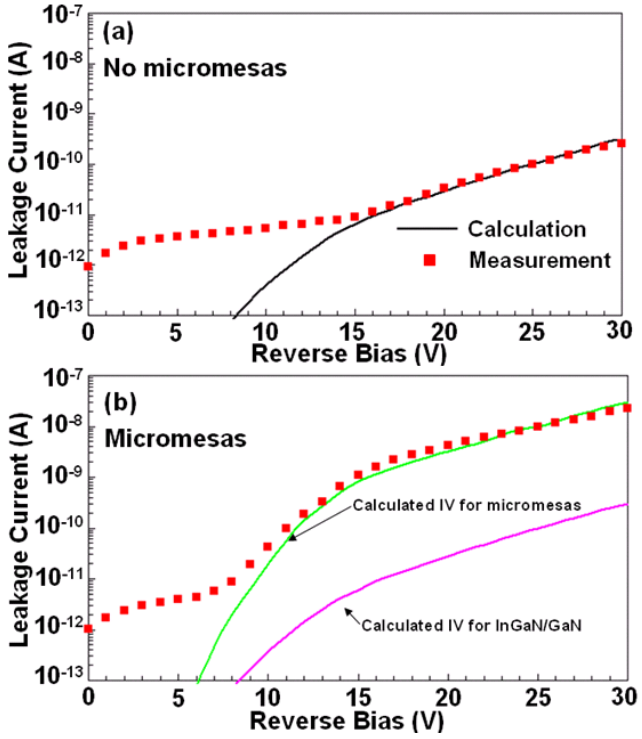

Figure 3-24 Representative reverse-bias IV curves for the smallest (17-μm diameter) Ni-InGaN/GaN Schottky barriers (a) without surface micromesas and (b) with surface micromesas. The red dots are measurement data and the solid curves are calculated tunneling currents. In (b), the green curve is calculated tunneling current for micromesas and the pink curve is calculated tunneling current for InGaN/GaN.

3.4.4 Effects of thermal annealing on Ni-InGaN/GaN Schottky diodes

The InGaN/GaN Schottky-diode samples were annealed in forming gas (5% H_2 in N_2) at different temperatures to study the effects of thermal annealing on reverse leakage current. In parallel, InGaN/GaN samples covered with ~ 100-nm Ni films were also annealed in order to study the Ni diffusion at the Ni/InGaN interface using RBS measurements. RBS measurements were carried out using 1.5 MeV $^4He^+$ ions with a scattering angle of 150 °. As shown in the measured RBS spectra in Figure 3-25,

for annealing at 200 ^{o}C for 60 minutes no diffusion was detected from RBS measurements; for annealing at 500 ^{o}C for 24 minutes, weak Ga and In out-diffusion were observed; for annealing at 625 ^{o}C for 15 minutes, extensive Ga and In out-diffusion and Ni in-diffusion were observed.

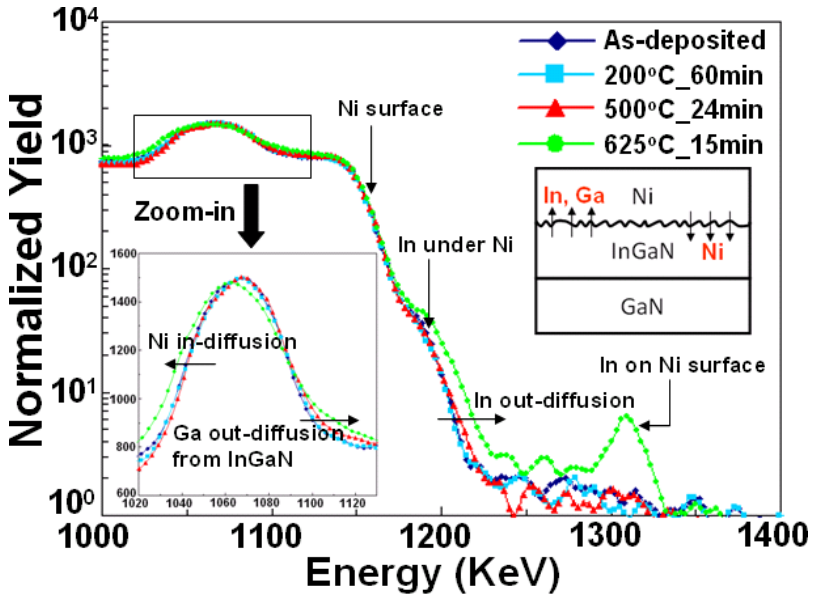

Figure 3-25 RBS spectra of as-deposited, annealed at 200 ^{o}C for 60 minutes, 500 ^{o}C for 24 minutes and 625 ^{o}C for 15 minutes Ni-InGaN/GaN samples. The inset on the left shows the zoom-in spectra and the inset on the right is a schematic diagram of the inter-diffusion at the Ni-InGaN interface.

The relation between leakage current at V_r = 30 V and the diode diameter before and after annealing at 200 ^{o}C for 1 hour and 500 ^{o}C for 24 minutes is shown in Figure 3-26. After 1-hour annealing at 200 ^{o}C, leakage current increase was significant for large-size diodes. However, the small-size diodes did not show significant leakage current increase. More data points were measured for the smallest diodes. It is seen that for the smallest HP_InGaN/GaN diodes with diameters of 17 μm much smaller

than their D_c of 28 μm showed little leakage current degradation after 200-^{o}C annealing. Although the RBS measurement did not detect any diffusion at 200-^{o}C annealing, the results of leakage current versus diameter (reverse leakage degradation only observed for larger diodes that contain surface micromesas) suggest that the surface micromesas with nanopipes at their center were likely an easy diffusion path at lower temperatures (e.g. 200 ^{o}C). This diffusion, however, is difficult to measure by RBS due to <1% diode area for the surface micromesas. Diffusion through surface micromesas would degrade the Schottky barriers, so the smallest diodes without surface micromesas would not be affected by the 200-^{o}C annealing. This was confirmed by experimental data. Similar metal diffusion through the cores of TDs in GaN-based LEDs was already observed at higher temperatures (> 600 ^{o}C) under TEM by Hsu et al [51]. The reverse-bias IV curves can be also fitted using tunneling current calculations (not shown) by lowering the SBH of micromesas by ~0.07 eV from the SBH value used before annealing.

After 24-minute annealing at 500 ^{o}C, all diodes showed significant leakage current increase and some LP_InGaN/GaN diodes suffered breakdown at V_r < 30 V. This suggests that extensive diffusion started at the Ni/InGaN interface and degraded the Ni-InGaN/GaN Schottky barriers (leading to ~0.25 eV SBH lowering relative to the SBH value used before annealing according to the tunneling current calculations). This is also consistent with our RBS measurements.

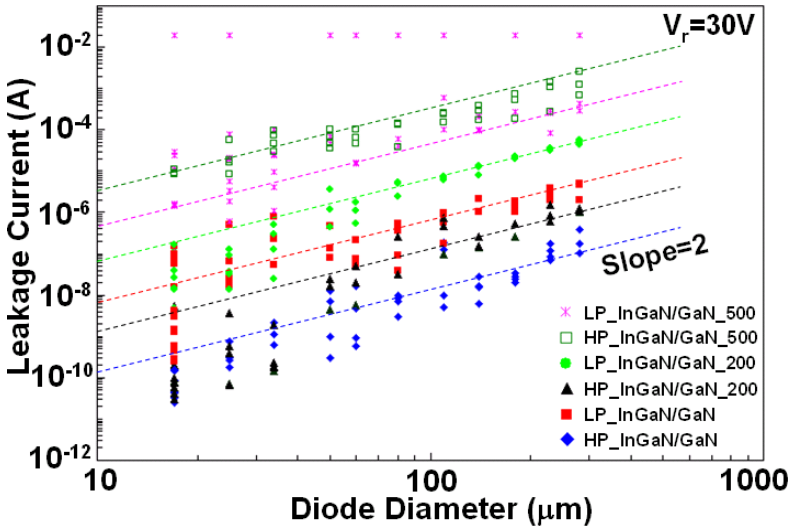

Figure 3-26 Leakage current at a reverse bias of 30 V versus diode diameter for LP_InGaN/GaN and HP_InGaN/GaN Schottky diodes before and after annealing at different temperatures.

3.5 Application for enhancement-mode HFETs

As we discussed above, the InGaN surface layer design can increase the effective Schottky barrier height, increase the electron tunneling distance under reverse biases and improve reverse breakdown and leakage characteristics. Also the design can be used to achieve enhancement-mode GaN-based HEMTs (conventional AlGaN/GaN HEMT is a depletion-mode device), which are more favorable in many circuit applications for reducing the circuit design complexity (e.g., eliminating the need for negative-polarity voltage supply) and fail-safe operations. In fact, the enhancement-mode GaN-based HEMTs have been reported using the InGaN surface

layer design on AlGaN/GaN HEMTs [52], [53]. Other than the InGaN surface layer design, an InGaN layer underlying the conventional AlGaN/GaN HEMT structure designed as an electron back barrier was also reported [54]. In this section, we also simulated the InGaN surface layer design in the AlGaN/GaN HEMT structure to illustrate the mechanism for enhancement-mode operations.

The simulated (with a Silvaco ATLAS 2-D simulator) structures for the conventional AlGaN/GaN HEMT and the AlGaN/GaN HEMT with InGaN surface layer design, as well as the corresponding energy band diagrams are shown in Figure 3-27. The polarization charges at the AlGaN/GaN and InGaN/AlGaN interfaces were assumed to be 1×10^{13} cm^{-2} and -2.1×10^{13} cm^{-2}, respectively [17], [18]. It is clearly seen that with the InGaN surface layer design, the effective Schottky barrier height of ~ 3.4 eV is much higher than that (~1.8 eV) of the conventional design. Therefore, the InGaN/AlGaN/GaN HEMT is more pinched off under the gate at zero bias with a 2-D electron-gas (2DEG) density of 1×10^{11} cm^{-2}, in comparison with the 2DEG density of 3×10^{12} cm^{-2} for the conventional AlGaN/GaN HEMT.

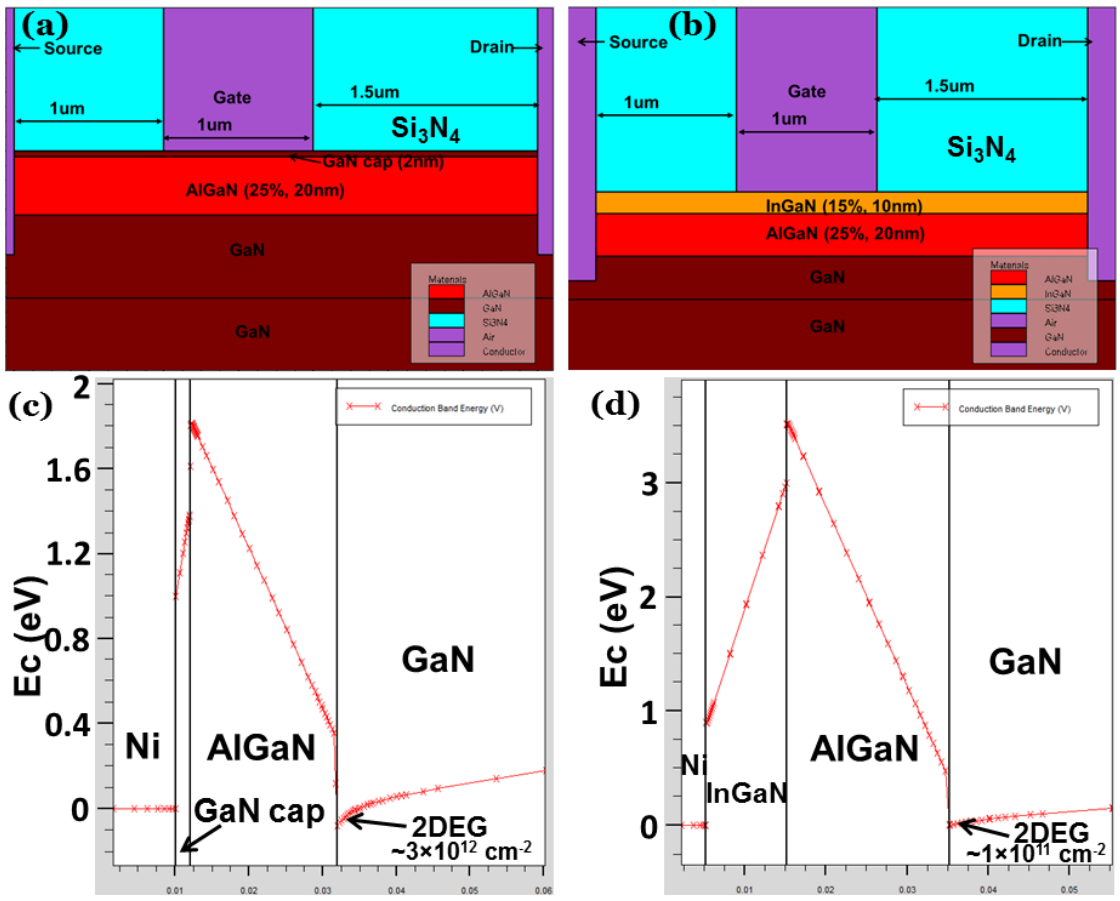

Figure 3-27 Simulated AlGaN/GaN and InGaN/AlGaN/GaN HEMT structures and the corresponding energy band diagrams. (a) Conventional AlGaN/GaN HEMT structure, (b) InGaN/AlGaN/GaN HEMT structure for enhancement-mode operation, (c) conduction band diagram under the Ni gate at zero bias for the structure (a) and (d) conduction band diagram under the Ni gate at zero bias for the structure (b).

I-V characteristics of these two devices were also simulated. Figure 3-28 showed the corresponding drain current (I_d) vs drain voltage (V_d) and drain current versus gate voltage (V_g) for both of AlGaN/GaN and InGaN/AlGaN/GaN HEMTs. It is observed from these curves that the threshold voltage (V_t) is increased by ~ 2 V (from ~-2 V to ~0 V) by using the InGaN surface layer. It can be expected that the enhancement-mode operation with even higher V_t (>0 V) can be obtained with more

optimized epitaxial layer structure and/or different gate schemes (e.g., a MISHFET structure).

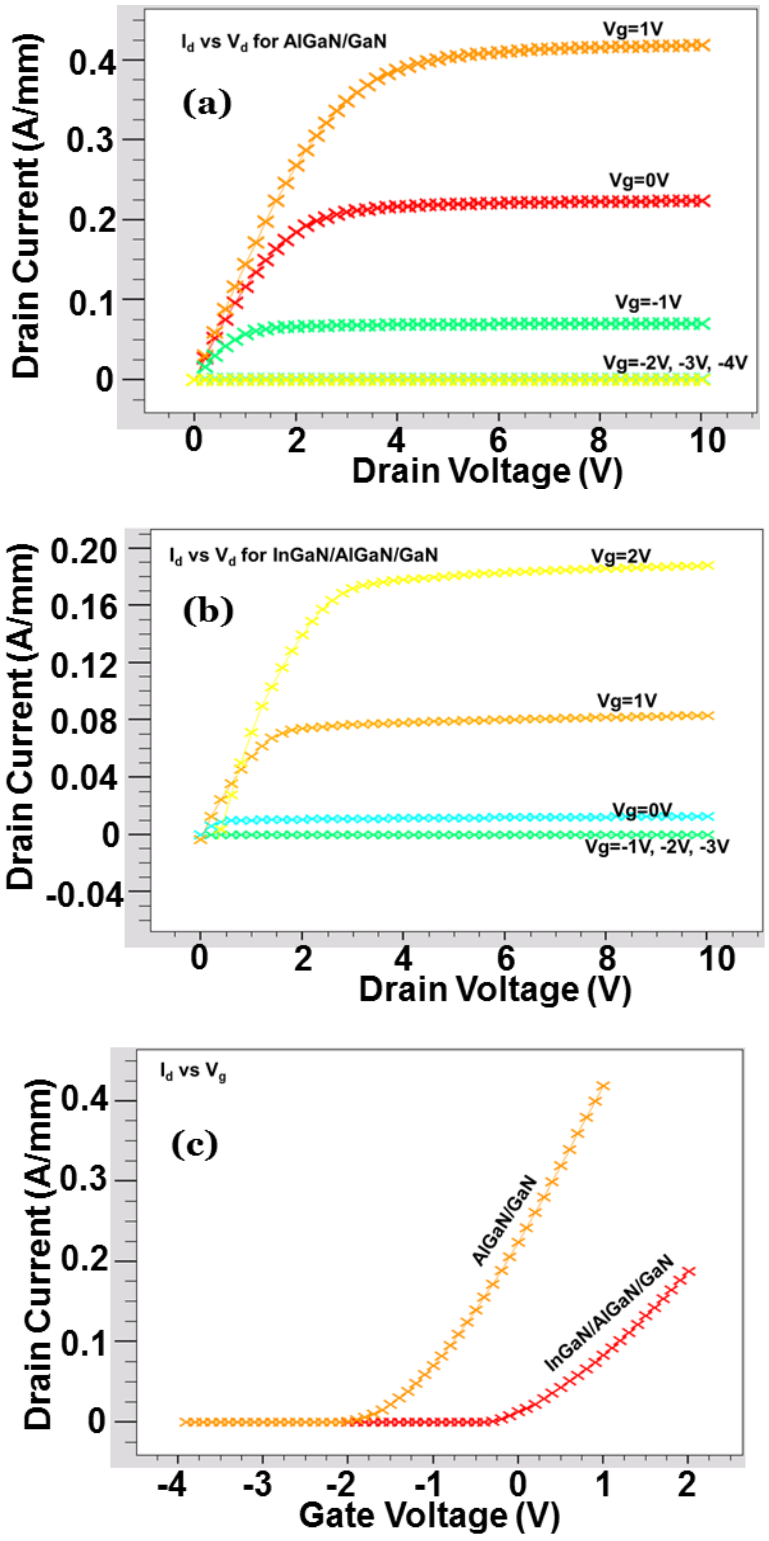

Figure 3-28 Simulated I-V characteristics for AlGaN/GaN and InGaN/AlGaN/GaN HEMTs. (a) I_d versus V_d for AlGaN/GaN HEMT, (b) I_d versus V_d for InGaN/AlGaN/GaN HEMT and (c) I_d versus V_g for both HEMTs.

3.6 Summary of InGaN/GaN technology

Leakage-current reduction and breakdown voltage increase in GaN Schottky barriers were achieved by the incorporation of suitable InGaN surface layers. Analysis shows that the InGaN surface layers change the electric-field distribution near the surface due to polarization-induced charges. Experimental *C–V* and *I–V* measurements confirm this analysis. The HP-MOCVD-growth technique of the GaN buffer layer was also found to be effective in reducing the leakage current and increasing the breakdown voltage of GaN Schottky barriers. Additionally, surface micromesas were observed on InGaN/GaN epi-layers, and their characteristics and origin were investigated by NOM, SEM and AFM. Large-scale mapping between surface micromesas and etch pits under NOM revealed that most of the surface micromesas originated from nanopipes in GaN. Studies of RBS and the electrical characteristics on corresponding Ni-InGaN/GaN Schottky barriers indicated that the surface micromesas with nanopipes at the center were the main source of reverse leakage current and caused an easy metal diffusion path, even in relatively low-temperature thermal annealings. This diffusion through nanopipes is detrimental to the electrical characteristics of Ni-InGaN/GaN Schottky barriers. The use of an HP GaN buffer layer effectively reduced the nanopipe and surface micromesa densities. However, in

order to further improve the electrical characteristics of the InGaN/GaN material, methods for further reducing or terminating surface micromesas on the surface (e.g. with thin surface dielectrics) are needed. Finally, the application of InGaN surface layer design in AlGaN/GaN HEMTs for achieving enhancement-mode operation is introduced.

Section 3.1, 3.2 and 3.3, are a rearrangement of the paper "Analysis of Reverse Leakage Current and Breakdown Voltage in GaN and InGaN/GaN Schottky Barriers," Wei Lu, Lingquan Wang, Siyuan Gu, David P. R. Aplin, Daniel M. Estrada, Paul K. L. Yu, and Peter M. Asbeck, IEEE Trans. Electron Devices, vol. 58, no. 7, pp. 1986–1994, Jul. 2011. The dissertation author was the primary author of the paper.

Section 3.4, is a rearrangement of the paper "Effects of surface micromesas on reverse leakage current in InGaN/GaN Schottky barriers," Wei Lu, Tomoaki Nishimura, Lingquan Wang, Tohru Nakamura, Paul K. L. Yu, and Peter M. Asbeck, J. Appl. Phys., vol. 112, pp.044505, Aug. 2012. The dissertation author was the primary author of the paper.

3.7 Reference

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Chapter 4

Fabrication procedure

4.1 Introduction

As we discussed the optimized device structures for achieving high breakdown voltage, high *Q* and high linearity in chapter 2, an anti-parallel (back-to-back) diode topology with interdigitated structures were employed. For convenience, Figure 2-8 is re-drawn here as Figure 4-1 to show the schematic structure of the designed device. Interdigitated finger dimensions were chosen to be 2.5 μm × 2.5 μm (finger width × finger spacing), considering the tradeoff between obtaining low series resistance and the limitation of photolithography technique (due to the need to lift-off >1 μm-thick metal by photolithography).

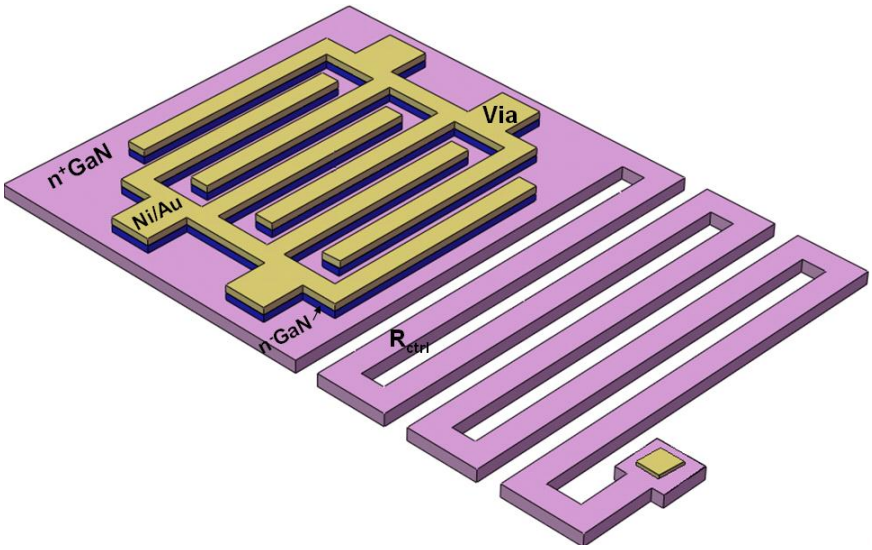

Figure 4-1 Schematic diagram of the anti-parallel diode structure with interdigitated strip geometry.

4.2 Initial fabrication procedure

Surface cleaning with NH_4OH for native oxide removal and 200-nm Ni thin film deposition by electron beam evaporation were first done immediately after the material MOCVD epitaxial growth to ensure a good interface between semiconductor and metal. 2-inch wafers were then diced into square samples for the following processing. Thick negative photoresist (with a thickness of ~2.4 μm after spin coating) was then used to realize the 2.5 μm × 2.5 μm interdigitated patterns for thick metal lift-off. The metal stack of Ti/Au/Ti/Ni (with a total thickness of ~ 1 μm) was then

deposited using electron beam evaporation and lifted off by acetone. Next, the wet etch mask for etching the first Ni layer was formed by another photolithography. Ni gate was then patterned by the commercial Ni etchant. A metal sidewall protection layer was then formed by sputtering a 100-nm SiO_2 and performing an anisotropic RIE dry etch. The sidewall SiO_2 is useful in protecting the Au from being damaged during the following GaN mesa dry etch. Then self-aligned GaN mesa etch to the n^+ GaN layer was performed by ICP/RIE etch using BCl_3 and Cl_2, followed by hot KOH (0.1 mol/L, 90 ^oC) treatment to remove the etch residuals left after the GaN dry etch. Next, the Ti/Al/Ti/Au ohmic contact was deposited by lift-off process. For device isolation, thick negative photoresist was first pattern by photolithography for hard mask lift-off. SiN_x (first) and Ni were deposited by sputtering and electron beam evaporation, respectively, as the hard mask for the following isolation etch (etch ~ 3 μm GaN to the insulating c-Sapphire substrate). Ni and SiN_x hard masks were then removed by Ni wet etch and SiN_x anisotropic dry etch. Benzocyclobutene (BCB) was then spun coat on the sample and cured at 190 ^oC for 45 mins. Photoresist was then patterned as the mask for the BCB via dry etch. Finally, the Ti/Au pad metal was deposited to contact the underlying metal through the vias for probing and external connections. The schematic diagrams for the varactor fabrication procedure are shown in Figure 4-2.

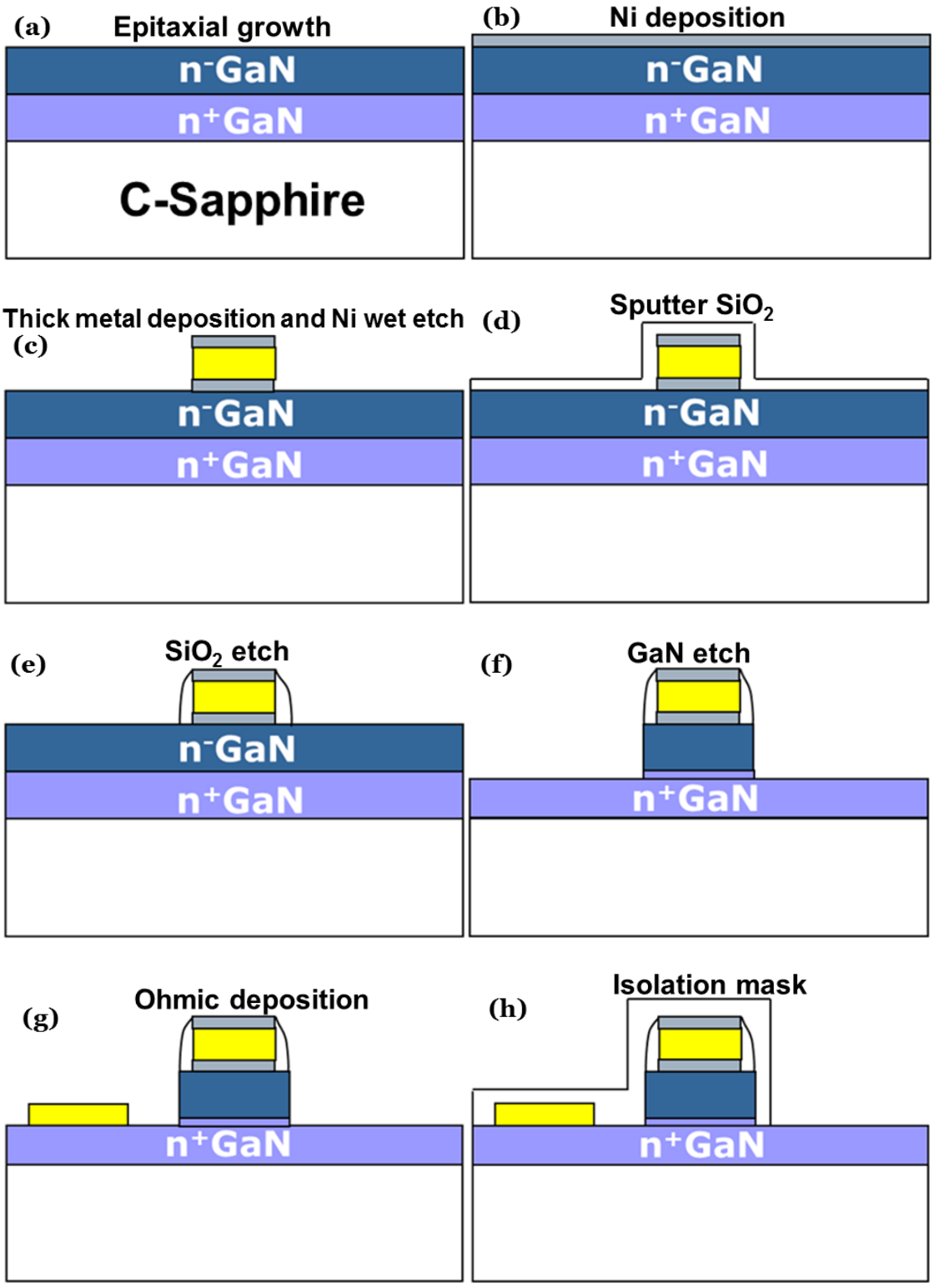

Figure 4-2 Schematic diagrams of the initial GaN-based varactor fabrication procedure. Continued on next page.

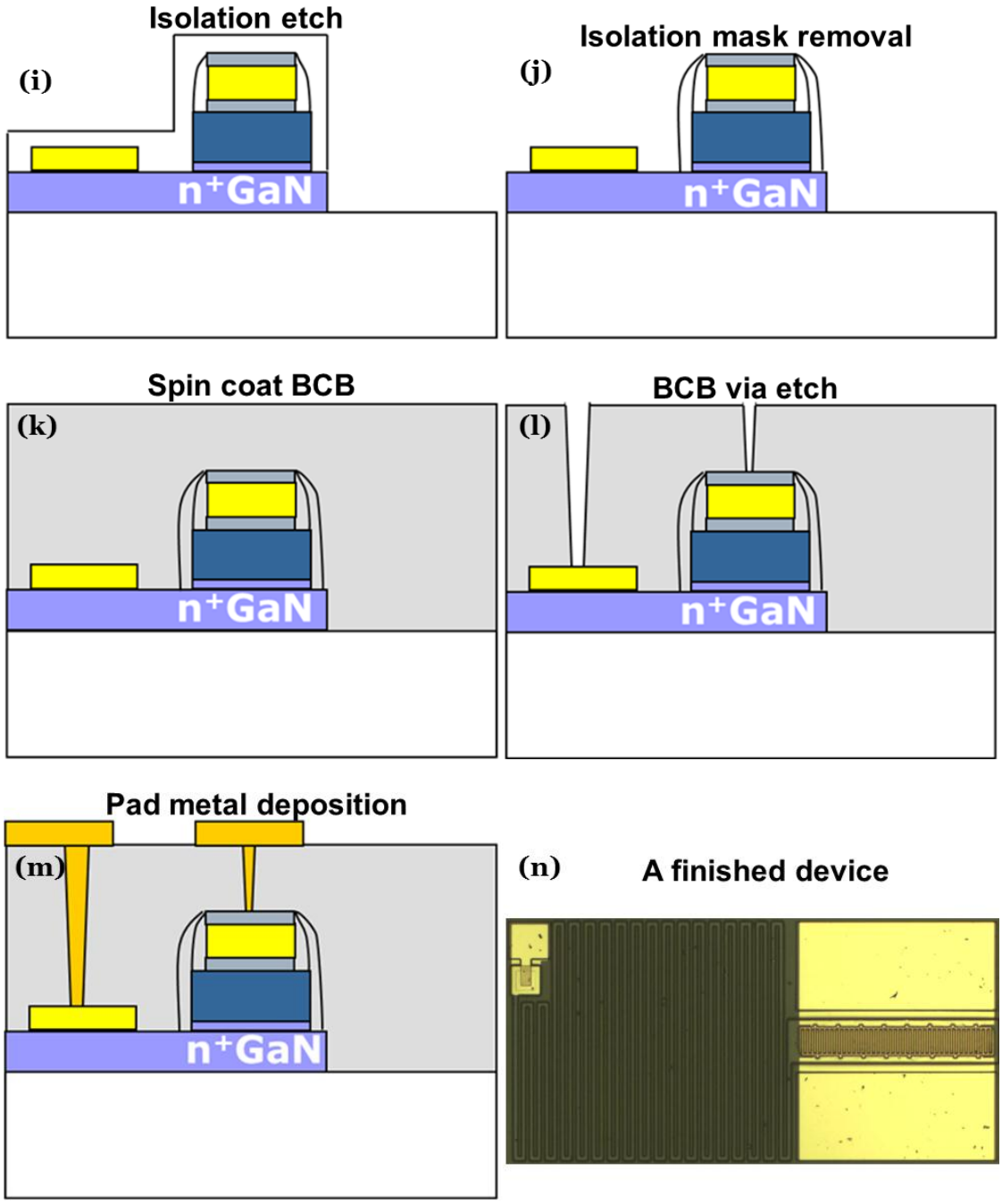

Figure 4-2 Schematic diagrams of the initial GaN-based varactor fabrication procedure. (a) Epitaxial growth by MOCVD, (b) first Ni deposition, (c) thick metal deposition and first Ni patterning, (d) SiO_2 sputtering, (e) SiO_2 anisotropic dry etch, (f) self-aligned GaN dry etch, (g) ohmic contact deposition, (h) isolation mask formation, (i) GaN isolation etch to Sapphire substrate, (j) isolation mask removal, (k) BCB spin coating and curing, (l) BCB via etch, (m) pad metal deposition and (n) an optical microscopy image of a finished device.

4.3 Preliminary results

DC and RF characteristics of the fabricated microwave power varactors were measured.

4.3.1 I-V measurements

In order to keep tracking the effects of the device fabrication on the device performance, I-V characteristics of the diodes were taken after every critical fabrication step.

Normal forward I-V characteristics were first confirmed by measuring the circular diode Schottky diodes in the sample. Then the reverse I-V characteristics were measured to verify the effects of fabrication step on the reverse leakage current. Two steps in the initial fabrication procedure were found to be detrimental to the device performance. The reverse leakage current was significantly increased after sputtering SiN_x (for isolation mask) and curing BCB, as shown in Figure 4-3. The leakage current increase caused by BCB curing is believed to be the defect-related thermal diffusion near the Schottky junction as discussed in section 3.4.4. The leakage current increase caused by sputtering SiN_x is likely attributed to the GaN mesa sidewall

damage by Ar plasma during the SiN_x sputtering. Therefore, high-temperature (>190 ^oC) process was avoided in subsequent fabrication procedure; a sidewall passivation step should be developed and added after the GaN mesa etch to protect the sidewalls. More detailed work on sidewall passivation will be discussed in the following section.

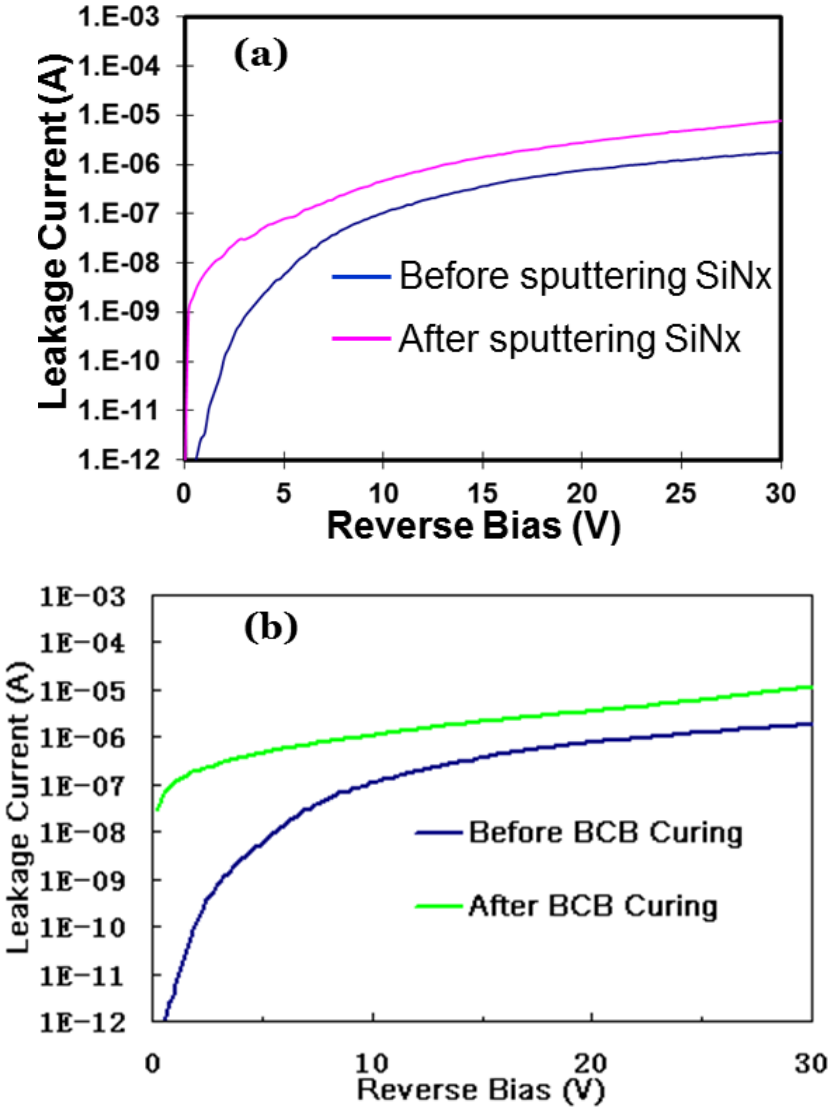

Figure 4-3 Reverse leakage current tracking after critical fabrication steps. (a) Before and after sputtering SiN_x and (b) before and after BCB curing.

4.3.2 RF measurements

The RF measurements were carried out to extract the S-parameters of the devices.

The S11 measurement setup is shown in Figure 4-4. The microwave network analyzer HP8753ES is connected to the varactor with a GSG probe. There is a bias Tee in between to protect the network analyzer in case the varactor diodes breakdown at high bias voltages. For the DC path, the device is biased by a voltage source through a DC probe. There is a 50-ohm resistor in parallel with a voltage meter to monitor the reverse leakage current under reverse biases. There is an optional external resistor in case the on-chip n^+ GaN serpentine resistor is not high enough in resistance to block the RF signals. Calibration to the GSG probe tips is done using an open/short/load scheme before device measurements.

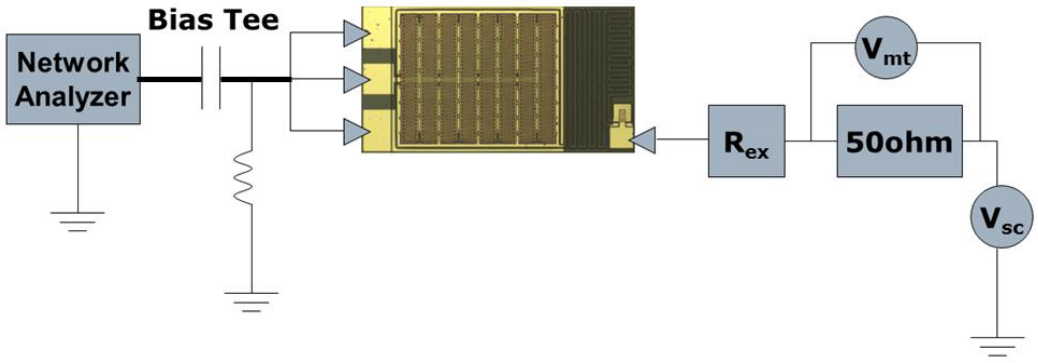

Figure 4-4 Measurement setup for S11. (The measurement data shown below do not necessarily come from the same device structure shown here.)

For parameter extractions from the RF measurements, with the varactor considered as a series RC network, the series resistance R_s can be extracted as R_s=Real(Z11); the series capacitance can be extracted as C_s=-1/Imag(ωZ11); the varactor *Q* can be extracted as *Q*=-Imag(Z11)/Real(Z11)=1/(ωR_sC_s).

A series of measurement results and analysis for a representative anti-parallel diode varactor are shown below.

The S11 in the Smith Chart of an anti-parallel diode varactor from 50 MHz to 5.05 GHz at an external reverse bias of 40 V is shown in Figure 4-5. A high *Q* factor of 104 at 1 GHz, corresponding to a low series resistance of 2.75 Ω, was obtained. The *Q* factor versus frequency *f* is plotted in Figure 4-6. The roll-off of *Q* at low frequency is due to RF current flow through the bias network resistors (R_{ctrl}), because the impedance of the varactor is higher at lower frequencies. A *Q* dip at frequencies near 1.6 GHz is observed. It is also notable that a high *Q* factor of ~40 was achieved at 5 GHz.

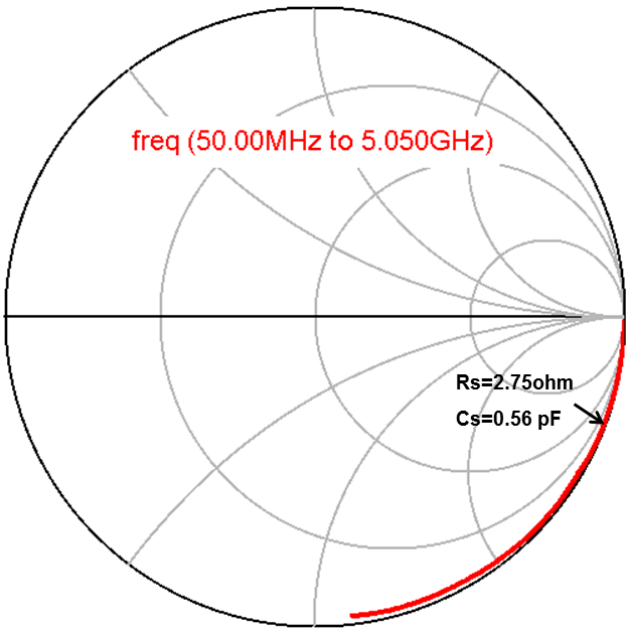

Figure 4-5 S11 measured from a device at reverse bias of 40 V from 50 MHz to 5.05 GHz shown in a Smith Chart. It corresponds to R_s=2.75 Ω, C_s=0.56 pF and Q=104.

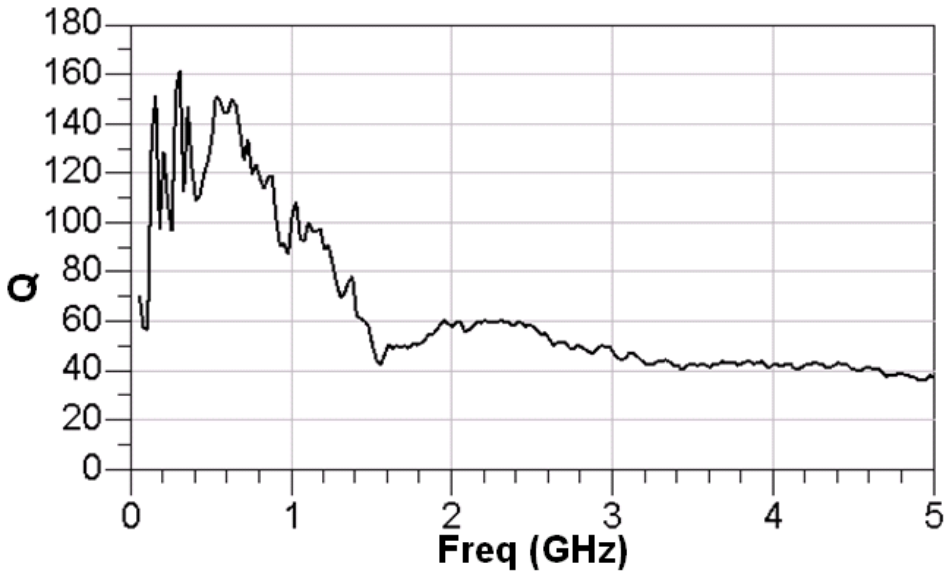

Figure 4-6 Q factor versus frequency at a reverse external bias of 40 V for an anti-parallel varactor diode. Each diode has an area of 3.8×10^{-5} cm^2.

In Figure 4-7, the reverse leakage current of the measured device was also monitored during the RF measurements by the 50-ohm resistor in parallel with a voltage meter. It is seen that the leakage current becomes significant when reverse bias exceeds 40 V (due to the possible sidewall damage and/or thermal diffusion near the junction as we mentioned in section 4.3.1). In order to fit the experimental curves with simulations and understand the device behavior better, a diode model considering the reverse leakage path is developed. Figure 4-8 shows the simple equivalent circuit model with R_{leak}, corresponding to the reverse leakage path.

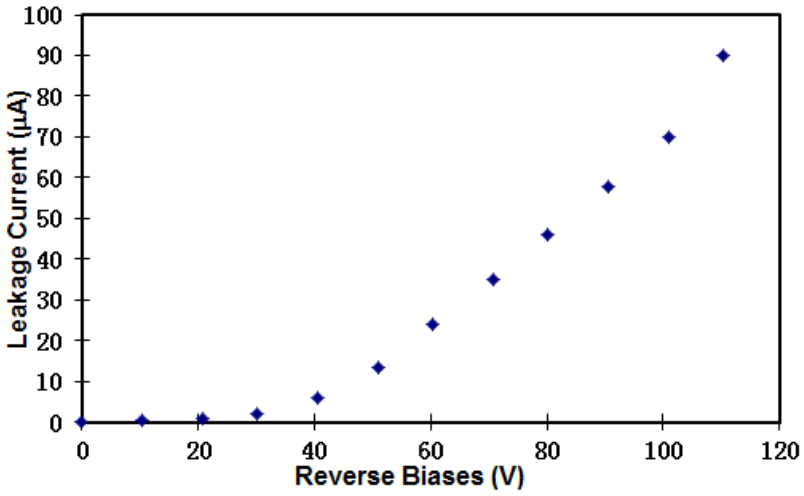

Figure 4-7 Reverse I-V characteristics of an anti-parallel varactor diode.

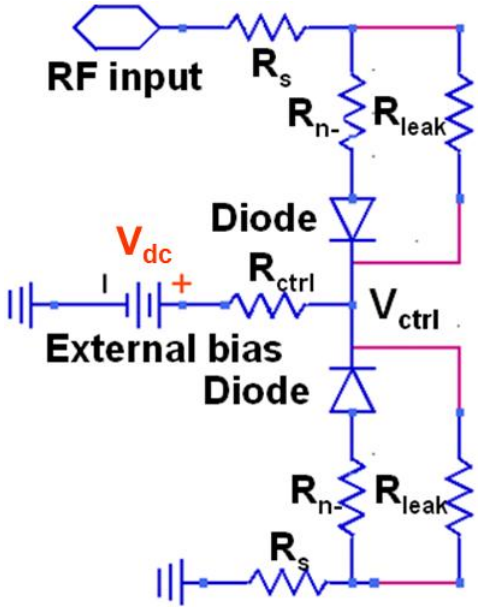

Figure 4-8 Equivalent circuit model for the anti-parallel varactors considering R_{leak} for the reverse leakage current.

The extracted series resistance and *Q* from the measured S11 parameters versus the reverse external bias are shown in Figure 4-9. It should be noted that the reverse external bias is different from the DC control voltage to the anti-parallel diodes due to the voltage drop across the R_{ctrl} (~160 KΩ here) when the leakage current becomes significant. At low biases, *Q* increases with the reverse external bias due to the reduction in C_s. The low-bias *Q* can be further improved by thickening the metal stripe. At high bias voltages (>40 V for this device), *Q* decreases due to the decrease of R_{leak} (diode is leakier). This can also be seen from the Figure 4-9(a), there is a significant R_s increase when reverse voltage exceeds 40 V where the reverse leakage current starts to become significant. A simple calculation was performed to confirm the relation between R_{leak} and equivalent R_s (when the parallel R_{leak} model is converted to the series RC network for *Q* computation) as shown in Figure 4-10. It is

found that the R_s increases as R_{leak} decreases while the C_s is almost independent with R_{leak}, Therefore when the device becomes leakier at high biases, there will be a *Q* drop caused by the decrease of R_{leak}. This suggests that reducing leakage and maintaining low leakage at high reverse bias are very important for achieving high *Q* factor as well as high breakdown voltage.

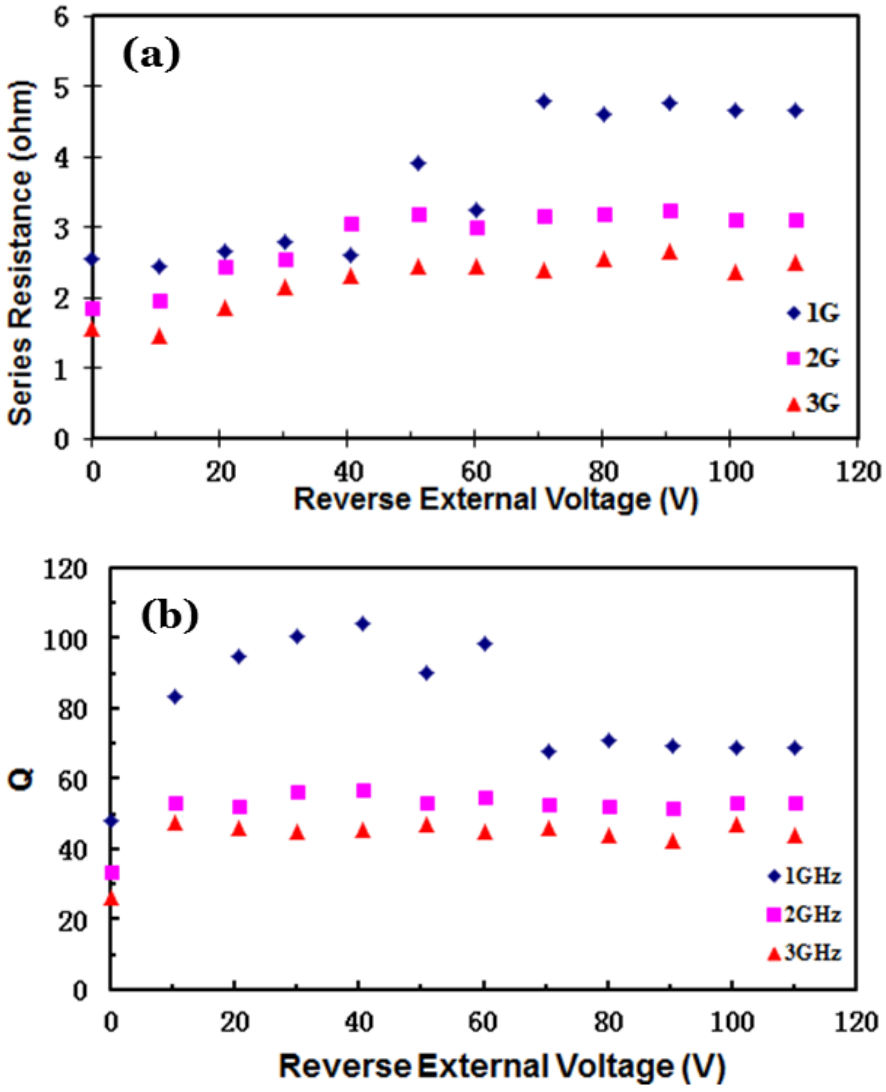

Figure 4-9 Extracted series resistance (a) and *Q* (b) versus reverse external biases for 1 GHz, 2 GHz and 3 GHz.

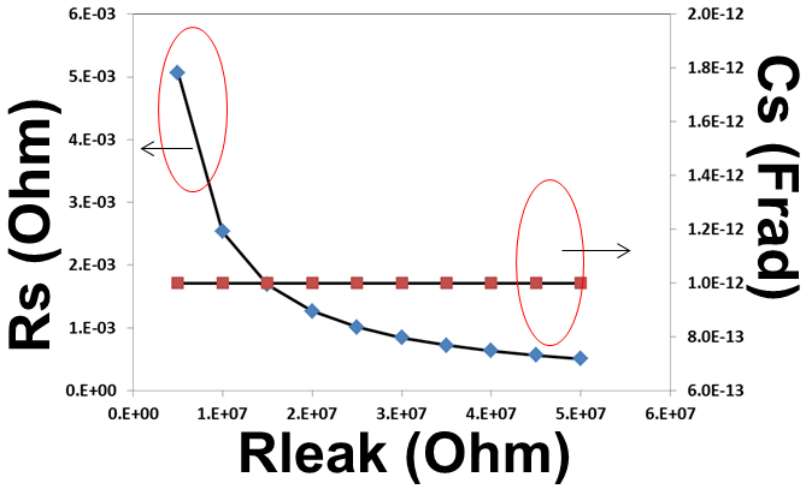

Figure 4-10 Relations between series resistance and R_{leak}, and series capacitance and R_{leak}.

The extracted capacitance from the S11 measurements versus the effective control voltage $V_{eff}=V_{dc}-I_{leak}\times R_{leak}$ (I_{leak} is the reverse leakage current) is shown in Figure 4-11. The capacitance varies with the effective control voltage as expected. The simulated C-V curve by 1-D Poisson solver fits the experimental curve well.

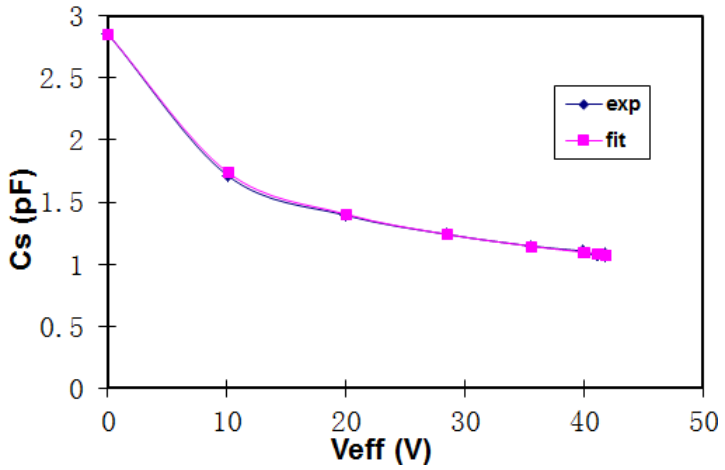

Figure 4-11 Experimental and simulated C-V curves for one of the diode in the two back-to-back diodes.

A microwave circuit model based on the equivalent circuit model shown in Figure 4-8 is built using Agilent ADS (a microwave circuit simulator [1]) to fit the experimental results and understand the RF characteristics of the device. A good match to the experimental results is shown in Figure 4-12. At high frequencies, measured *Q* values are slightly larger than the model, probably due to parasitic reactance not captured in the model. There is a resonance at ~1.6 GHz in the experimental data, which is believed to be due to a LC resonance and will be addressed in the next chapter. It is worthwhile to show the relation between *Q* and reverse biases in the simulation when assuming the leakage is low at high reverse biases. A clear trend of *Q* increase as the increase of reverse bias is shown in Figure 4-13. This result confirms again the importance of low leakage current to the device performance.

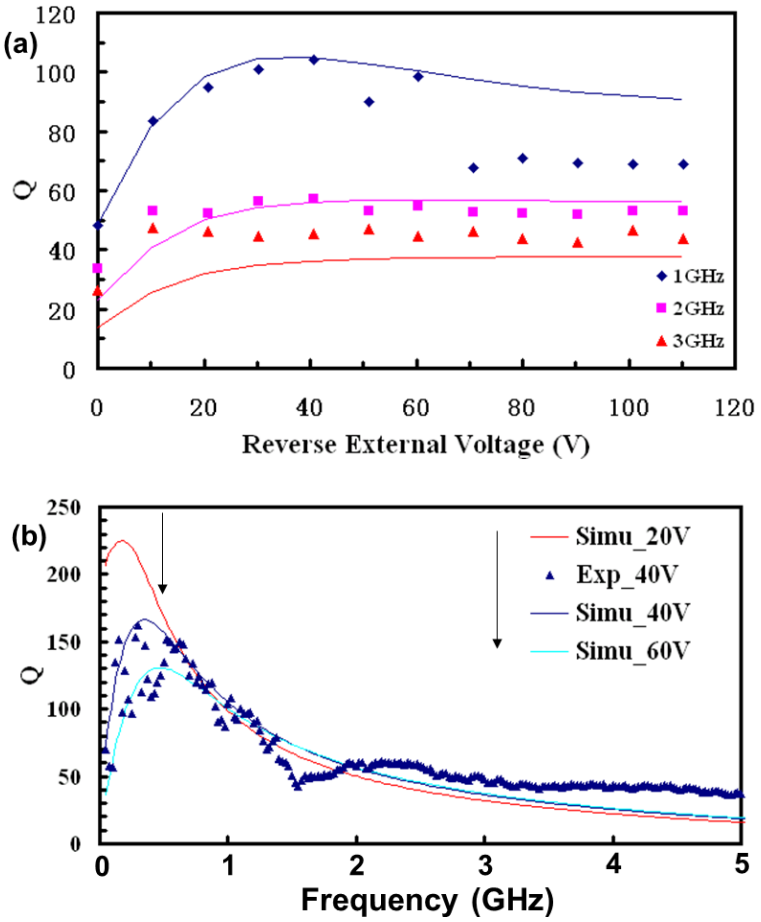

Figure 4-12 (a) Experimental Q (dots) and simulated Q (lines) versus the reverse external bias at f = 1 GHz, 2 GHz and 3 GHz; (b) experimental Q (dots) and simulated Q (at reverse external biases of 20 V, 40 V and 60 V) versus frequency.

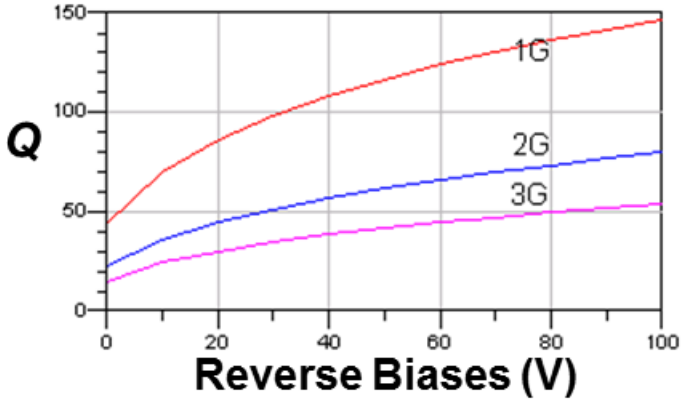

Figure 4-13 Simulated Q versus reverse biases assuming the reverse leakage is low at high biases.

4.4 Sidewall passivation in GaN-based Schottky diodes

As we discussed in the last sections, the reverse leakage current is important for the device performance and the GaN mesa sidewall damage might be the cause for the increased leakage current after sputtering SiN_x for the isolation etch mask. Therefore, a study on the GaN mesa sidewall passivation was carried out. In fact, sidewall passivation is important for power devices. Appropriate sidewall passivation can help reduce leakage current, avoid sidewall damages during later device processing and improve device reliability. This section explores the procedure for the sidewall passivation of GaN-based Schottky diodes by simulation and experiments.

4.4.1 Simulation of electric field distribution under reverse biases

In order to understand the importance of sidewall passivation and find the right materials for passivation on GaN sidewalls, simulations using a Silvaco ATLAS 2-D simulator [2] are performed. The simulated device structure is shown in Figure 4-14. The n^- GaN has a doping level of 1×10^{17} cm^{-3} and a thickness of 1 μm. The structure is almost the same as the structure discussed in section 2.1, except that there is a

passivation layer along the sidewall of the GaN mesa. The electric field distributions under reverse biases for various passivation materials with different dielectric constants were simulated. Besides the passivation by growing dielectric materials along the sidewalls, passivation by Mg^+ (p-type dopants in GaN) implantation through the sidewall is also simulated. These two types of structure are shown in Figure 4-15. In Figure 4-16(a), it is seen that the simulated electric field at the edge of the Ni-GaN Schottky junction (surrounded by the air) is intensified (~2 MV/cm) and much greater than the electric field in the middle of the junction (~1.7 MV/cm). It suggests that the sidewall (especially the edge) is a great concern for the reverse breakdown and leakage current. The peak electric fields at the edge of the Schottky junctions for didoes with different passivation dielectrics are shown in Figure 4-16(b). It is clearly shown that the peak electric field increases with the relative dielectric constant of the material. The peak electric field of the diode without passivation (in the air) has the lowest intensity compared to those passivated by other relatively high-dielectric-constant materials. The peak electric field of the diode passivated by Mg^+ implantation (sidewall surrounded by the air) shows even lower peak electric field at the edge. Although it seems that the intentionally added dielectrics increase the electric field at the edge of the Schottky diodes, it is still necessary to passivate the sidewalls. The reasons are: first, there are likely low-quality passivation materials stick to the sidewalls, e.g. moistures and/or GaO_x, when the GaN sidewalls are exposed to the air; secondly, sidewall passivation can physically protect the sidewall from damages during later device processing. Therefore, it will be valuable to conduct a series of experiments to find the appropriate passivation procedure for GaN mesa sidewalls.

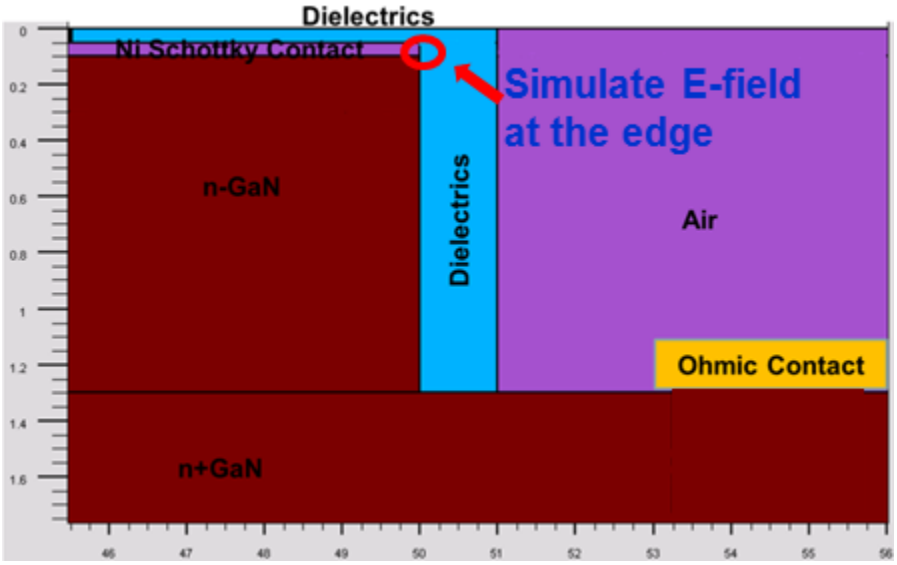

Figure 4-14 Simulated GaN Schottky diode structure with sidewall passivation in Silvaco ATLAS 2-D simulator for electric field distribution under reverse biases.

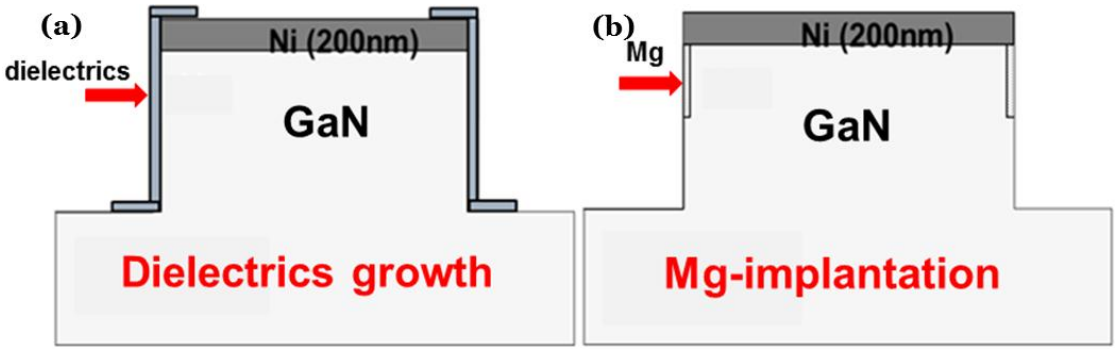

Figure 4-15 Sidewall passivation by (a) growing dielectrics along the sidewall and (b) Mg^{+} implantation through the sidewall.

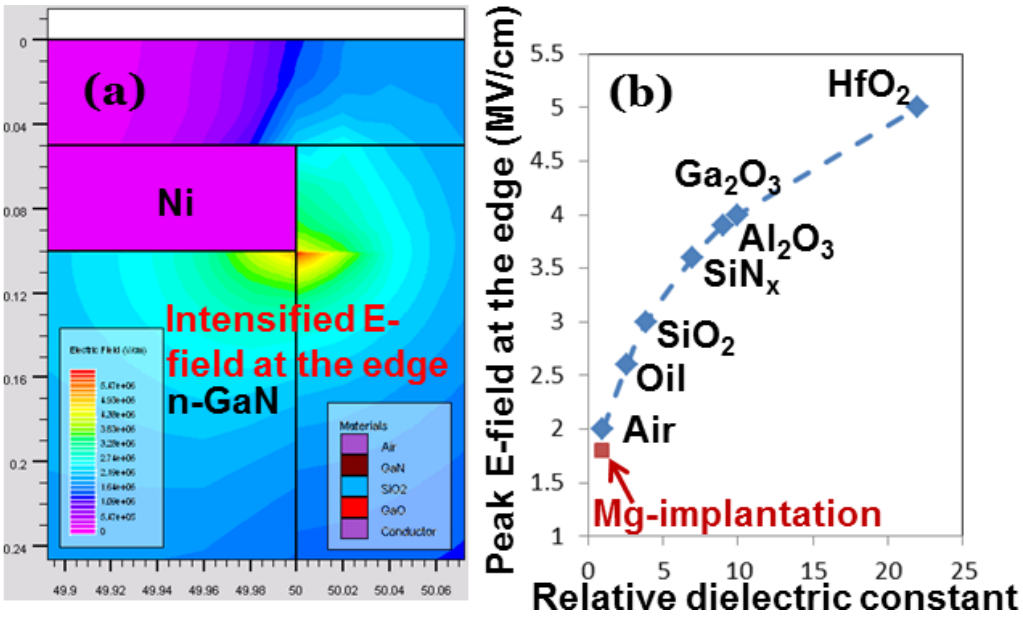

Figure 4-16 (a) Electric field distribution under a reverse bias of 85 V and (b) peak electric field at the edge of Ni-GaN Schottky junctions for different passivation materials along the GaN sidewalls. The relative dielectric constants of different materials shown here are from references [3], [4].

It is also worthwhile to show the electric field distribution for a device with a non-self-aligned gate process (where Ni Schottky gate is not or not aligned to the mask for the GaN mesa etch). The simulated structure and results are shown in Figure 4-17. There is a huge electric field (>7 MV/cm) at the edge of the Ni-GaN Schottky junction (surrounded by air) compared to that (~1.7 MV/cm) in the middle of the junction, which indicates that the non-self-aligned gate structure is not favorable for high power Schottky didoes.

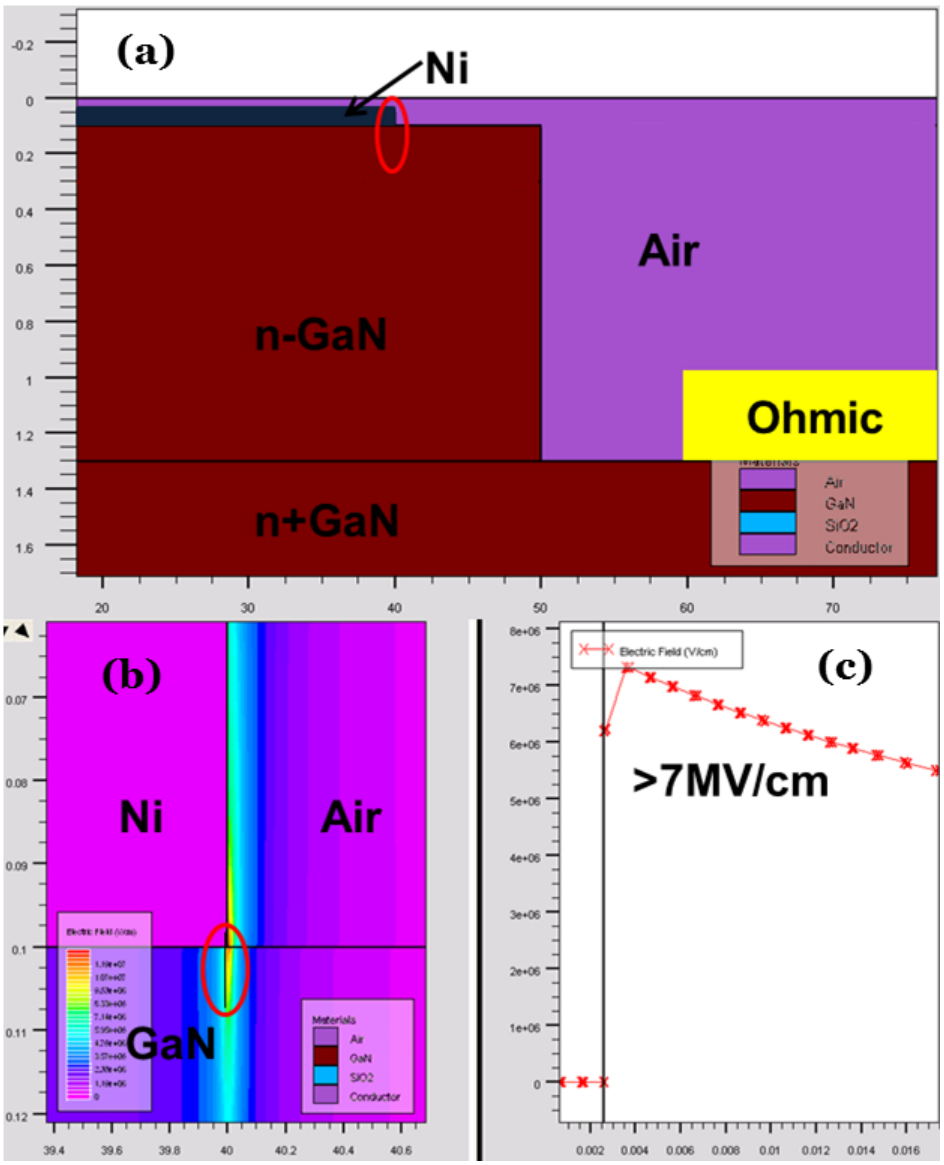

Figure 4-17 Electric field distribution for a device with a non-self-aligned gate process. (a) Simulated device structure, (b) electric field distribution near the edge of the Ni-GaN Schottky junction and (c) electric field along the black line (in the red ellipse) in (b) near the edge of the Ni-GaN Schottky junction.

4.4.2 Experimental procedure

Growth methods used in this study for the passivation dielectrics are atomic layer deposition (ALD) and sputter. Other methods which require high temperature during the growth (e.g. plasma enhanced chemical vapor deposition - PECVD) are excluded in this study due to the possible thermal damages to the Schottky junctions as we discussed in the section 3.4.4. The fabrication procedure is almost the same as described in section 2.1, except that there is additional sidewall treatments after the GaN mesa etch and passivation dielectrics removal (on the Schottky and ohmic contact regions) before ohmic contact deposition.

For passivation by dielectric growth, we used sputter at room temperature (RT) for SiO_2 (relative dielectric constant $\varepsilon = 3.9$) passivation and ALD at 175 ^oC and 210 ^oC for Al_2O_3 ($\varepsilon = 9$) passivation. Before the dielectric deposition, for comparison purpose, hot NH_4OH (~60 ^oC) or KOH (0.1 mol/L, ~80 ^oC) treatments were used as the chemical treatment to clean the GaN mesa sidewalls after the mesa etch. Measurements in corn oil ($\varepsilon = 2.6$) immediately after sidewall chemical treatment were also performed.

For passivation by Mg^+ implantation, the fabrication procedure is schematically summarized in Figure 4-18. Surface treatment with NH_4OH and 200-nm Ni e-beam deposition immediately followed the GaN MOCVD growth. The Ni film

was then patterned by photolithography and Ni wet etch. A 100-nm SiO_2 was sputtered on the surface as the implantation mask (photoresist was left un-removed on top of Ni as additional mask for Schottky junction protection). Two-step Mg^+ implantation with ion energy of 60 KeV and 90 KeV (obtained by SRIM simulations [5] for more uniform implantation profile and sufficient Mg^+ implantation at the edge of the Ni-GaN Schottky junction) was then conducted. The implantation dosage was both 1×10^{14} cm^{-2} with 90-KeV implantation first. After implantation, the SiO_2 mask and residual photoresist on Ni were removed. GaN mesa etch to n^+ GaN and hot KOH treatment were then performed. Finally, ohmic contact deposition on the n^+ GaN was done to finish the device fabrication. The schematic device structures for these two passivation methods are shown in Figure 4-15, except that the ohmic contacts are not shown.

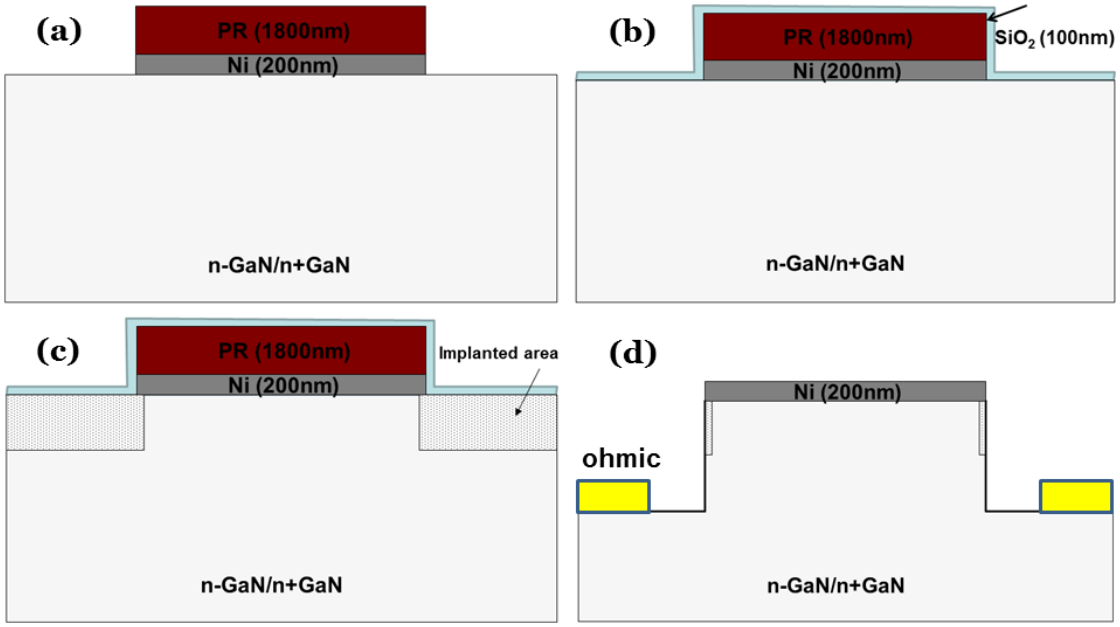

Figure 4-18 Fabrication procedure for sidewall passivation by Mg^+ implantation. (a) Ni patterning by wet etch, (b) SiO_2 sputtering for implantation mask, (c) Mg^+ implantation and (d) SiO_2 and photoresist removal, GaN mesa etch and ohmic contact deposition.

4.4.3 Results and discussions

GaN Schottky diodes fabricated with different sidewall processing procedures were labeled accordingly in Table 4-1.

Table 4-1 Samples treated with different sidewall cleaning and passivation methods.

Sample labels	Chemical treatment	Sidewall passivation
Control	KOH	No
NH_4OH_Oil	NH_4OH	Oil
KOH_Oil	KOH	Oil
KOH_ALD_Al_2O_3_175C	KOH	ALD Al_2O_3 at 175 ^oC
NH_4OH_ALD_Al_2O_3_210C	NH_4OH	ALD Al_2O_3 at 210 ^oC
KOH_ALD_Al_2O_3_210C	KOH	ALD Al_2O_3 at 210 ^oC
KOH_Sput_SiO_2	KOH	Sputter SiO_2 at RT
KOH_Mg_Imp	KOH	Mg implantation

The reverse I-V measurement results for all samples listed above are summarized in Figure 4-19. It is seen that hot KOH treatment is effective in cleaning GaN sidewall (possible GaN residuals caused by GaN mesa etch and/or GaO_x) before the passivation. After treated with hot KOH, dielectric passivation of corn oil and 175-^oC-ALD Al_2O_3 (sample KOH_Oil and KOH_ALD_Al_2O_3_175C) as well the passivation by Mg^+ implantation (sample KOH_Mg_Imp) work well as GaN sidewall passivation layers, showing significant reverse leakage current reduction in comparison with the Control sample. However, hot NH_4OH treatment seems to damage the GaN sidewalls (forming more sidewall states by physical and/or chemical damages) and cause excess leakage current, which can be observed from reverse I-V characteristics of the sample NH_4OH_Oil and NH_4OH_ALD_AL_2O_3_210C. These

observations confirm that appropriate sidewall passivation is a necessary for fabricating GaN-base power Schottky diodes in order to protect the sidewall from being damaged by other device processing. The sample passivated by 210°C-ALD Al_2O_3 showed excess leakage current too which is due to the thermal damage to the Ni-GaN Schottky junctions as discussed in section 3.4.4. For sidewall passivation by SiO_2 sputtering, the diode became very leakage too which we believe was caused by the sidewall damage due to the Ar plasma during the SiO_2 sputtering. In comparison, ALD is a more gentle growth technique which does not cause damage to the materials.

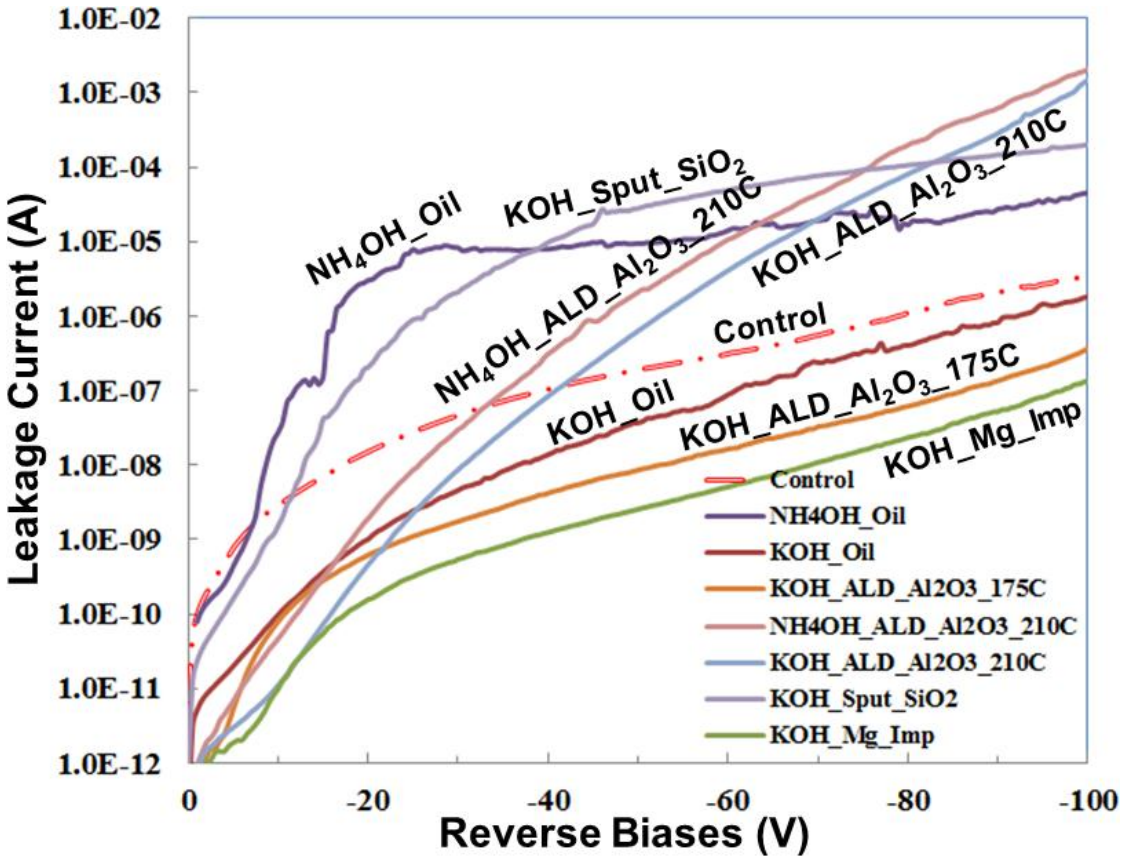

Figure 4-19 Reverse leakage current for samples fabricated with different sidewall processing procedures. The diode area is 2.8×10^{-5} cm^2.

4.4.4 Summary of sidewall passivation in GaN-based Schottky diodes

The importance of sidewall passivation in GaN-based power Schottky diodes was confirmed by simulations and experiments. In the simulations, we found that the electric field at the edge of Ni-GaN Schottky junctions under reverse biases was much greater than that in the middle of the junctions (due to geometric effect). It brings forth a concern of the mesa sidewalls for GaN-based Schottky diodes in high power applications. Experimentally, we tried different chemical treatments before sidewall passivation for sidewall cleaning as well as different sidewall passivation methods. KOH was found to be effective in cleaning GaN sidewalls and low-temperature-ALD Al_2O_3 and Mg^+ implantation were effective in passivating the sidewalls.

4.5 Improved fabrication procedure

The fabrication procedure is therefore adjusted based on our experiments and analysis. The main improvements are as follows: the interdigitated finger stripe

thickness is increased up to >1.8 μm by improving the photolithography and lift-off technique; a hot KOH treatment after the GaN mesa etch followed by an immediate ALD Al_2O_3 sidewall passivation at 170 ^oC are added; BCB curing temperature is lowered to 170 ^oC. (The reason for selecting low-temperature ALD Al_2O_3 instead of Mg^+ implantation is due to the equipment availability at UCSD). The adjusted fabrication steps and the resultant reverse I-V characteristics after the ohmic metal was formed and after all of the device processing were finished are shown in Figure 4-20. In comparison to the reverse I-V characteristics shown in Figure 4-3, the leakage current is greatly reduced and maintained at low levels after finishing the device fabrication. The RF measurements and the detailed analysis for the devices fabricated with the improved procedure will be discussed in the next chapter.

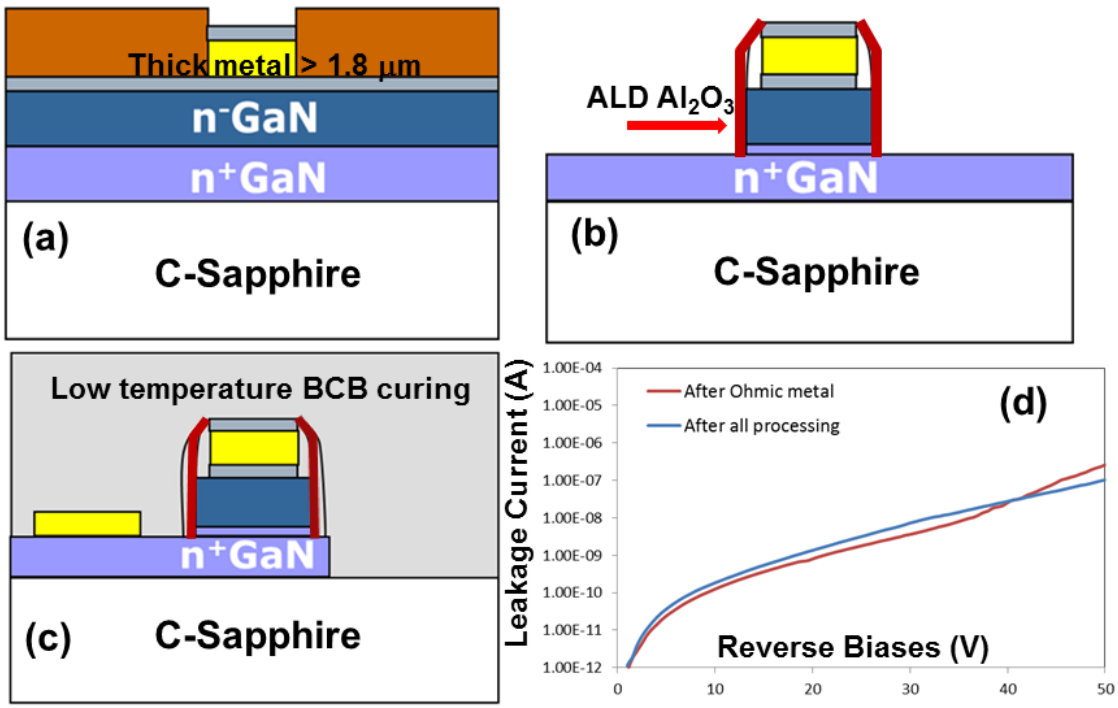

Figure 4-20 Improved fabrication procedure and the resultant reverse I-V characteristics. (a) Thick (> 1.8 μm) metal deposition and lift-off, (b) hot KOH treatment and ALD Al_2O_3 passivation at 170 ^oC for GaN mesa sidewalls, (c) low temperature (170 ^oC) BCB curing and (d) reverse I-V curves after the ohmic metal was formed (the I-V characteristics can be measured from now) and after all device fabrication was finished. The measured diode in (d) is a circular diode with diameter of 60 μm.

4.6 Summary of the fabrication procedure

The initial fabrication procedure is described in this chapter. DC and RF characterization were performed to extract the preliminary characteristics of the fabricated microwave power varactors. A high Q = 104 at 1GHz was obtained at a

reverse bias of 40 V. However, excess leakage current was found in the devices possibly due to the GaN mesa sidewall damage caused by Ar plasma during the SiN_x sputtering and the Schottky junction degradation caused by the defect-related thermal diffusion during BCB curing. Simulations and experiments were then carried out to improve the fabrication procedure. Hot KOH treatment after GaN mesa etch, low-temperature ALD Al_2O_3 (as well as Mg^+ implantation) sidewall passivation and low-temperature BCB curing were found to be effective in maintaining low leakage current throughout the entire fabrication process.

Section 4.3, is a rearrangement of the paper "InGaN/GaN Microwave Varactors with High *Q*, High-Breakdown Voltage and High Linearity," Wei Lu, Lingquan (Dennis) Wang, Siyuan Gu, David P. R. Aplin, Paul K. L. Yu, and Peter M. Asbeck, in Semiconductor Device Research Symposium (ISDRS), 2011 International, IEEE, College Park, MD, 7-9 Dec., 2011. The dissertation author was the primary author of the paper.

4.7 References

[1] http://edocs.soco.agilent.com/display/ads2009/Home

[2] http://www.silvaco.com/products/device_simulation/atlas.html

[3] J. Robertson, "High dielectric constant oxides," Eur. Phys. J. Appl. Phys., vol. 28, 265-291, 2004.

[4] M. Passlack, N. E. J. Hunt, E. F. Schubert, G. J. Zydzik, M. Hong, J. P. Mannaerts, R. L. Opila, and R. J. Fischer, "Dielectric properties of electron-beam deposited Ga_2O_3 films," Appl. Phys. Lett., vol. 64, No. 20, 2715-2717, 1994.

[5] http://www.srim.org/

Chapter 5

Experimental results and discussions

Complete characterization of the GaN-based microwave power varactors was carried out and the results are presented in this chapter, including high voltage C-V and I-V measurements, S-parameter measurements, linearity measurements and tunable resonance circuit measurements.

5.1 High voltage I-V and C-V measurements

The forward I-V characteristics were first measured on the circular diodes in the sample as shown in Figure 5-1. The extracted ideality factor and Schottky barrier height are 1.24 and 1.25 eV, respectively.

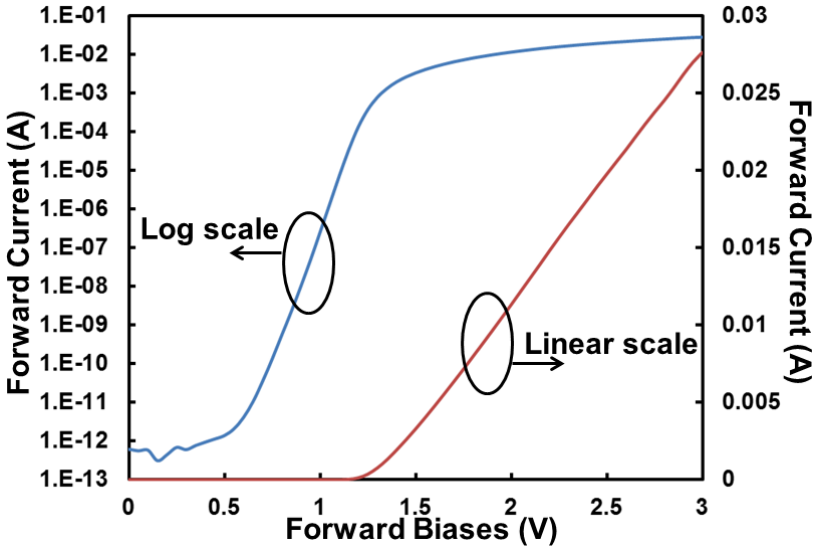

Figure 5-1 Forward I-V characteristics for a 60-μm-diameter circular diode in the sample.

In Figure 5-2, the reverse I-V characteristics show a breakdown voltage of above 100 V and much lower leakage current for the device fabricated using the improved fabrication procedure than those fabricated using the initial fabrication procedure (refer to Figure 4-3).

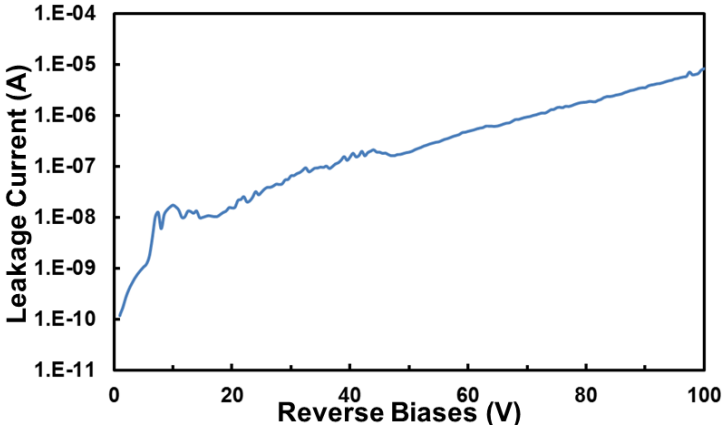

Figure 5-2 Reverse I-V characteristics for a 60-μm-diameter circular diode in the sample.

The high voltage C-V characteristics for a single circular diode varactor were then measured as shown in Figure 5-3(a). The capacitance varies with the reverse applied biases up to 100 V. The measured C-V curve is consistent with the simulated curve except that the last several points of the measured C–V curve are lower due to the large leakage current when the reverse bias approaches 100 V, which causes the unreliability of the capacitance measurement. Base on the measured high-voltage C-V curve, we then worked out the corresponding tuning ratio (C_{max}/C_{min}) of an anti-parallel diode varactor as shown in Figure 5-3(b). The tuning ratio is calculated based on the considerations that the summation of the DC and RF signal to the diodes does not cause any reverse breakdown or forward conduction. It is noted that a tuning ratio of 2 is still maintained for a RF peak-to-peak voltage of ~80 V.

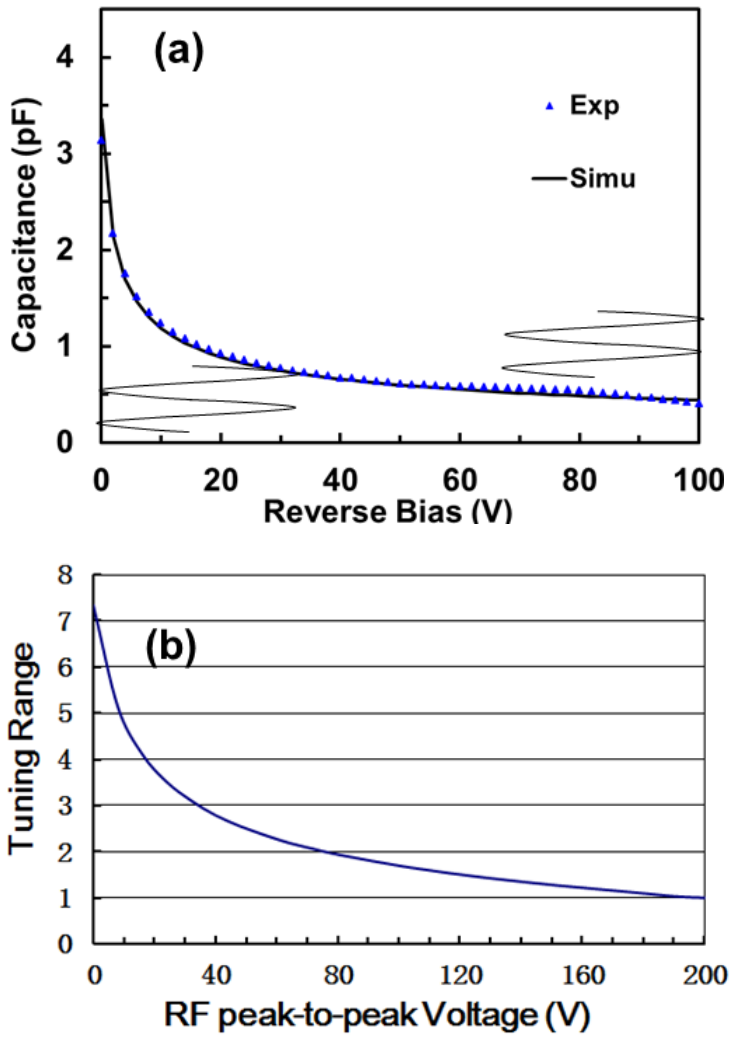

Figure 5-3 (a) High voltage C-V characteristics for a circular diode with an area of 5×10^{-5} cm^2 at f = 1 MHz and (b) the corresponding tuning ratio vs RF peak-to-peak voltage for the anti-parallel diode varactor, based on the considerations of not causing reverse breakdown or forward conduction. The waves shown in (a) denote the RF signals at the minimum and maximum DC bias voltages when calculating the tuning ratio.

5.2 S-parameter measurements

The RF characteristics of the microwave varactors were obtained via two measurement layouts for 1-port and 2-port measurements, respectively. Two representative microwave varactors under the optical microscopy and their corresponding equivalent LRC network are shown in Figure 5-4. Figure 5-4(a) shows the device for 1-port measurements, which have the ~1.8-μm-thick metal stripe and 2.5 μm × 2.5 μm interdigitated finger structures, same as the design we discussed in chapter 4. The 2-port device shown in Figure 5-4(b) has slightly different interdigitated structures. The fingers have a length of 120 μm, a width of 7 μm (50 μm and 2.5 μm, respectively, for the narrower finger design shown in Figure 5-4(a)) and a spacing of 2.5 μm between fingers. The reasons for the wider and longer finger design are to increase the capacitance density (per finger) and further thicken the finger metal stripe utilizing the final pad metal deposition (vias can be fully opened along the fingers when the fingers are wide enough).

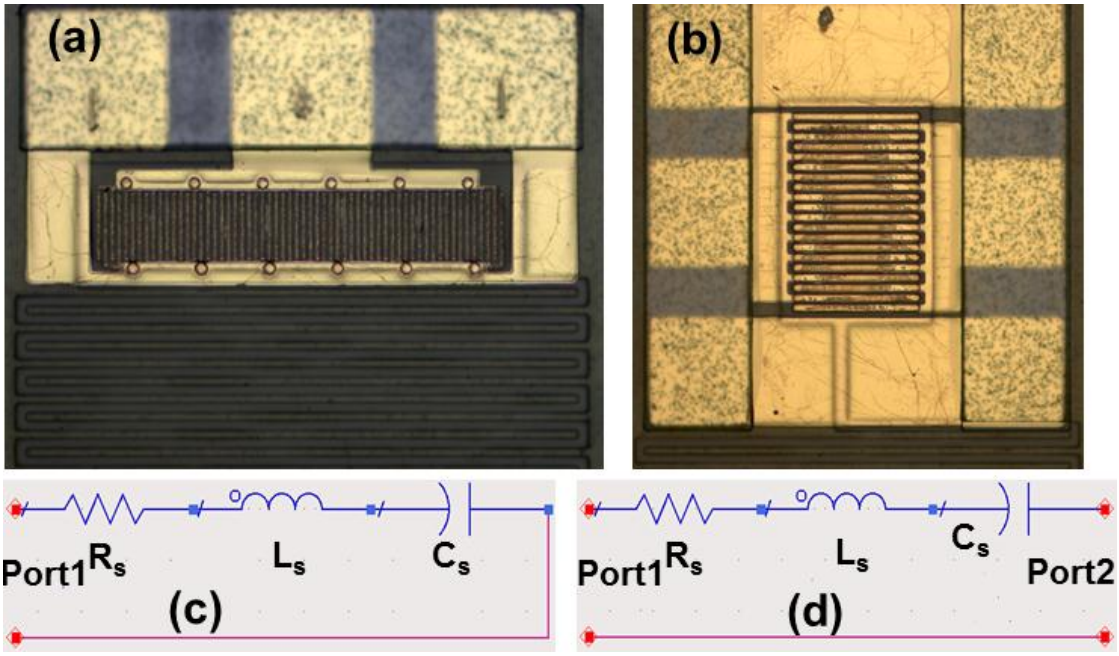

Figure 5-4 (a) An optical microscopy image of a device for 1-port measurements, (b) an optical microscopy image of a device for 2-port measurements, (c) the equivalent series LRC network for the 1-port device and (d) the equivalent series LRC network for the 2-port device.

The parameter extraction formulas for the equivalent series LRC network are as follows:

For 1-port measurements:

$$R_s = Real(Z11),$$

$$C_s = -1/(Imag(Z11 - jwL_s)w)\ ,$$

$$Q(w) = -Imag(Z11 - jwL_s\ )/Real(Z11)\ = 1/(wR_sC_s\ )\ .$$

Eq. 5-1

For 2-port measurements:

$$R_s = Real(-1/Y21),$$

$$C_s = -1/(Imag(-1/Y21 - jwL_s)w),$$

$$Q(w) = -Imag(-1/Y21 - jwL_s)/Real(-1/Y21) = 1/(wR_sC_s).$$

Eq. 5-2

The series inductance can be measured from a short de-embedding structure, which is usually a small value in the order of 0.1 nH. However, the extracted C_s and $Q(w)$ shown in the follow sections did not subtract the jwL_s term, which gives a lower but more accurate Q values for the devices.

5.2.1 Measurements for the 1-port devices

The anti-parallel diode varactor devices for 1-port measurements were measured up to a reverse bias of 70 V. The measurement setup is the same as the one shown in Figure 4-4. The reserve leakage current was recorded from the 50-ohm resistor in parallel with a voltage meter, as shown in Figure 5-5. The leakage current is much lower than that of the previous device fabricated with the initial fabrication procedure.

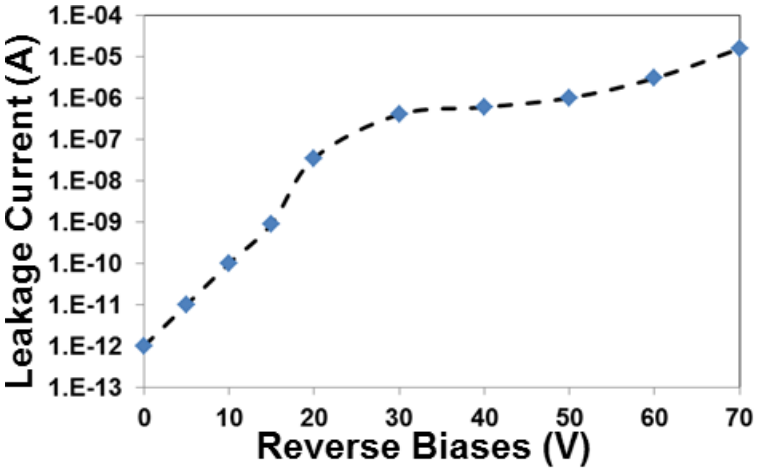

Figure 5-5 Reverse I-V curve for a 1-port anti-parallel diode varactor (see Figure 5-4(a)). The dots are the measurement data points.

Figure 5-6 shows the measured S11 in the Smith Chart from 500 MHz to 3.5 GHz for the same 1-port device at a reverse bias of 70 V. At 1 GHz, it corresponds to a capacitance of 0.55 pF, a series resistance of 2.4 Ω. Correspondingly, a high *Q* of 120 was obtained at 70 V for the fabricated 1-port device with the improved fabrication procedure.

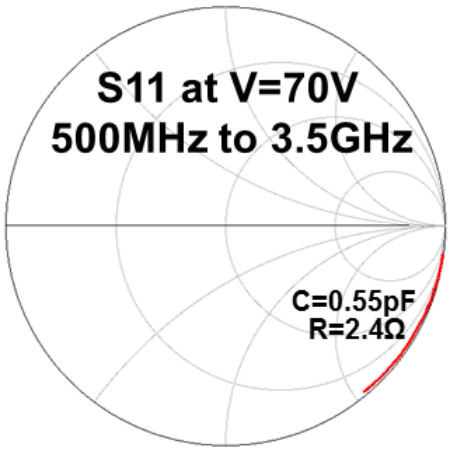

Figure 5-6 S11 from 500 MHz to 3.5 GHz for a 1-port device at a reverse bias of 70 V.

The relations of *Q* versus reverse bias, R_s versus reverse bias and C_s versus reverse bias are shown in Figure 5-7. In comparison with the same relations for a leakier device fabricated using the initial fabrication procedure shown in Figure 4-9, the *Q* does not drop in value at high reverse bias for the new devices (R_s does not jump up too much at high reverse biases either). Another improvement is that the *Q* at low biases (~90 at 1 GHz) is much larger than the previous results (~50 at 1 GHz) obtained from the device with the same structure. This is attributed to the thicker metal stripes which are almost doubled in thickness in the improved fabrication procedure. Figure 5-7(c) shows the C-V curves extracted from the S11 measurements. Although the capacitance decreases with the increase of the reverse bias, the curve cannot be fitted with the calculated C-V curve by running a simple 1-D Poisson simulation. This is probably due to some parasitic reactance and/or imperfection of the device fabrication which are not captured in the equivalent circuit model. More analysis will be discussed in the next section.

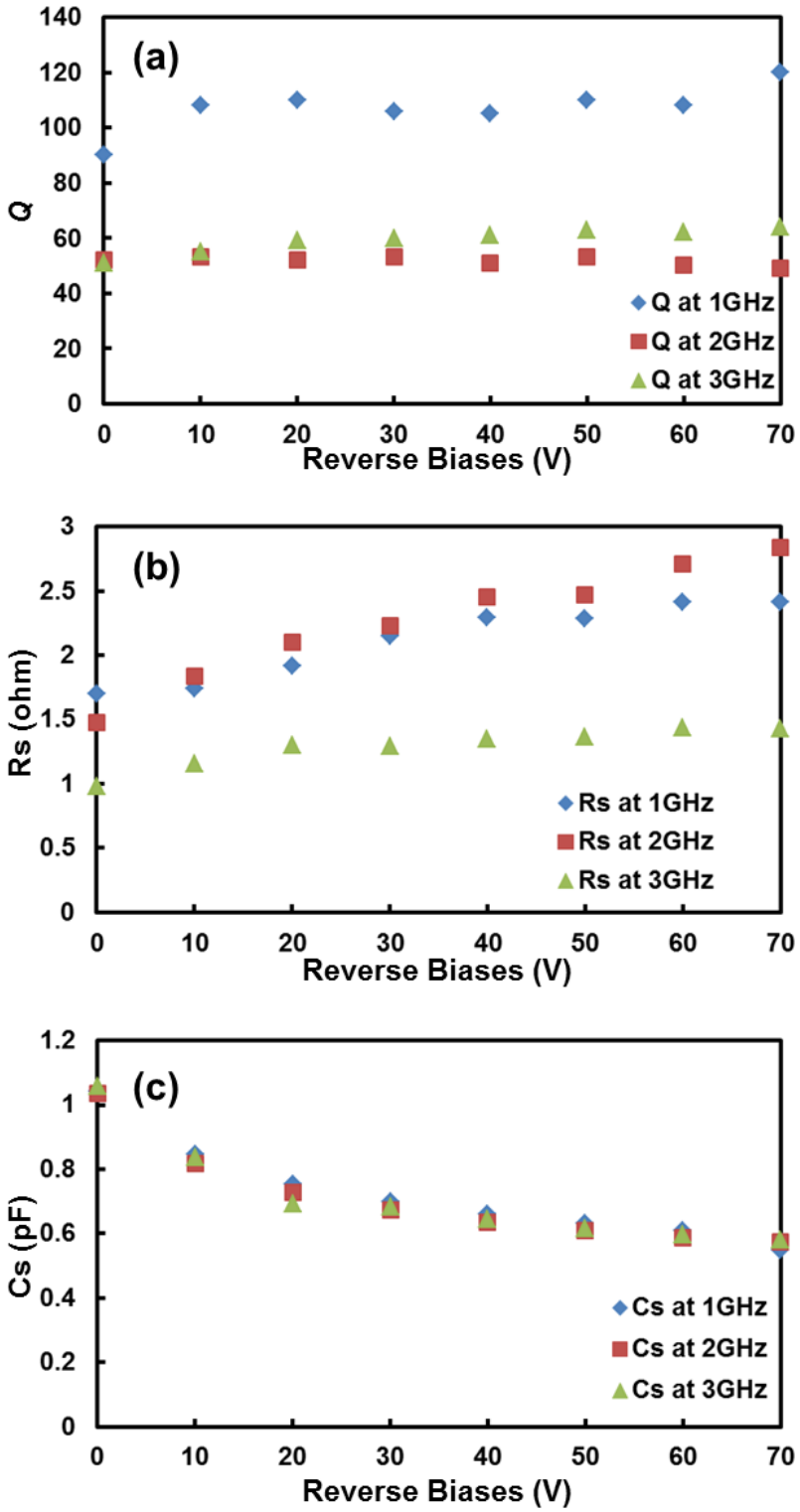

Figure 5-7 The relations of (a) *Q* versus reverse bias, (b) R_s versus reverse bias and (c) C_s versus reverse bias at 1 GHz, 2 GHz and 3 GHz for a 1-port device.

Figure 5-8 shows the relation between *Q* and frequency at different reverse biases. *Q* of above 100 (up to 120) at 1 GHz and above 50 at 3 GHz are obtained. Different from our expectation, the *Q* did not show the anticipated strong dependence on reverse biases, probably due to the effects of parasitic reactance in the device. Several resonances in the *Q* versus frequency curves are also observed at frequencies between 1 GHz and 2 GHz, which are believed to be attributed to the LC resonance in the DC path and confirmed by the following simulations.

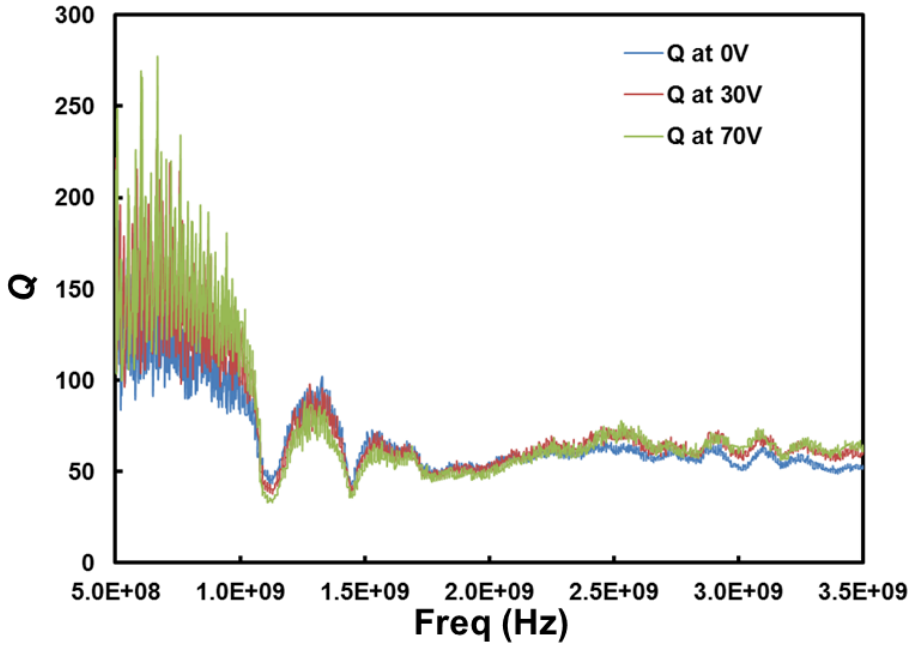

Figure 5-8 The relation of *Q* versus frequency at different reverse biases for a 1-port device.

As shown in Figure 5-9, a more detailed equivalent circuit model incorporating the parasitics from the device and measurement setup is simulated in ADS. In comparison with the simple model shown in Figure 4-8, the inductance from the DC needle probe (~1 nH/mm) and the coaxial cables (~ 300 nH/m for RG-58/U) in the DC

path is very large (770 nH used in this simulation, 750 nH from the coaxial cable and 20 nH from the DC needle probe) and cannot be subtracted in the RF calibration using a standard open/short/load calibration substrate. The parasitic capacitance (0.01 pF used in this simulation and confirmed by a SONNET electromagnetic simulation [1]) of the n^+ GaN control resistor is also included in this model. The stray capacitance shown in the model is mainly from the capacitance between fingers. The small capacitance to the ground is also included in this model.

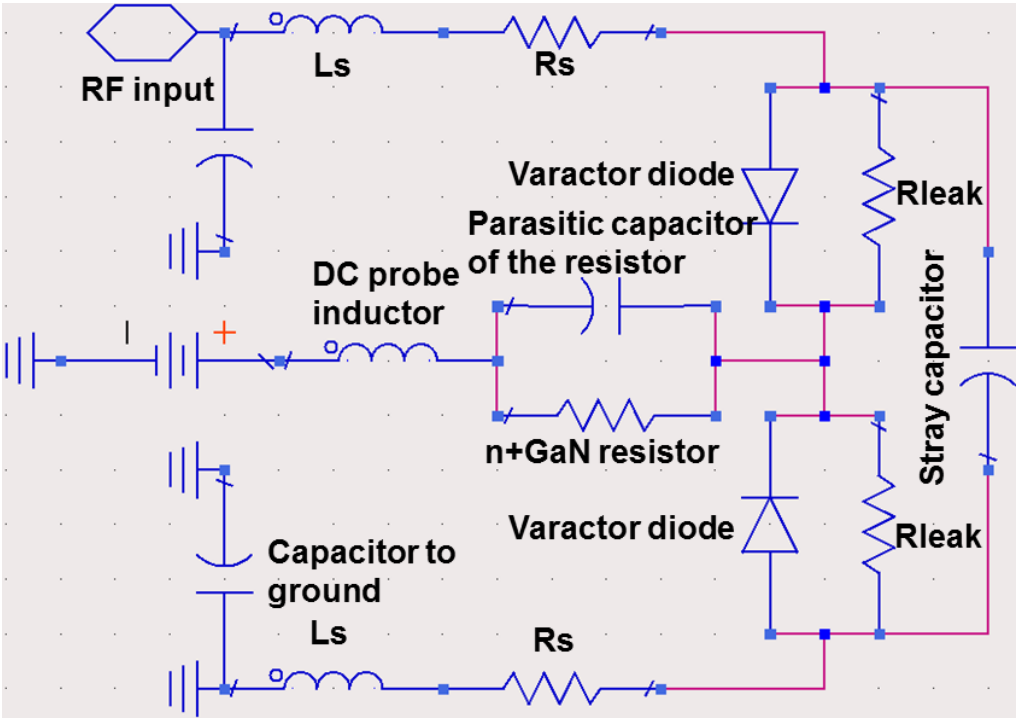

Figure 5-9 Equivalent circuit model considering the parasitics from the 1-port device and the measurement setup.

The simulation results based on the above model showed very good match with the experimental results as shown in Figure 5-10(a) (only match one of the resonances though). The LC resonance between the inductor from the DC probe and

coaxial cable (770 nH) and the capacitance from the n^+ GaN resistor (0.01 pF) caused a *Q* dip. This is due to the RF leak through the DC path at the resonant frequency (low impedance in the DC path). In practical package, the inductance from the DC path should be much smaller so that a resonance will be expected at a much higher frequency. The simulated *Q* vs frequency assuming the inductance in the DC path is small (10 nH) is also shown in Figure 5-10(b). No *Q* dip is observed in the simulated frequency range. Similar to the *Q* versus frequency curve shown before in Figure 4-12, the *Q* is also higher than the simulated values at higher frequencies in Figure 5-10, which is probably due to some parasitic reactance not captured in the circuit model.

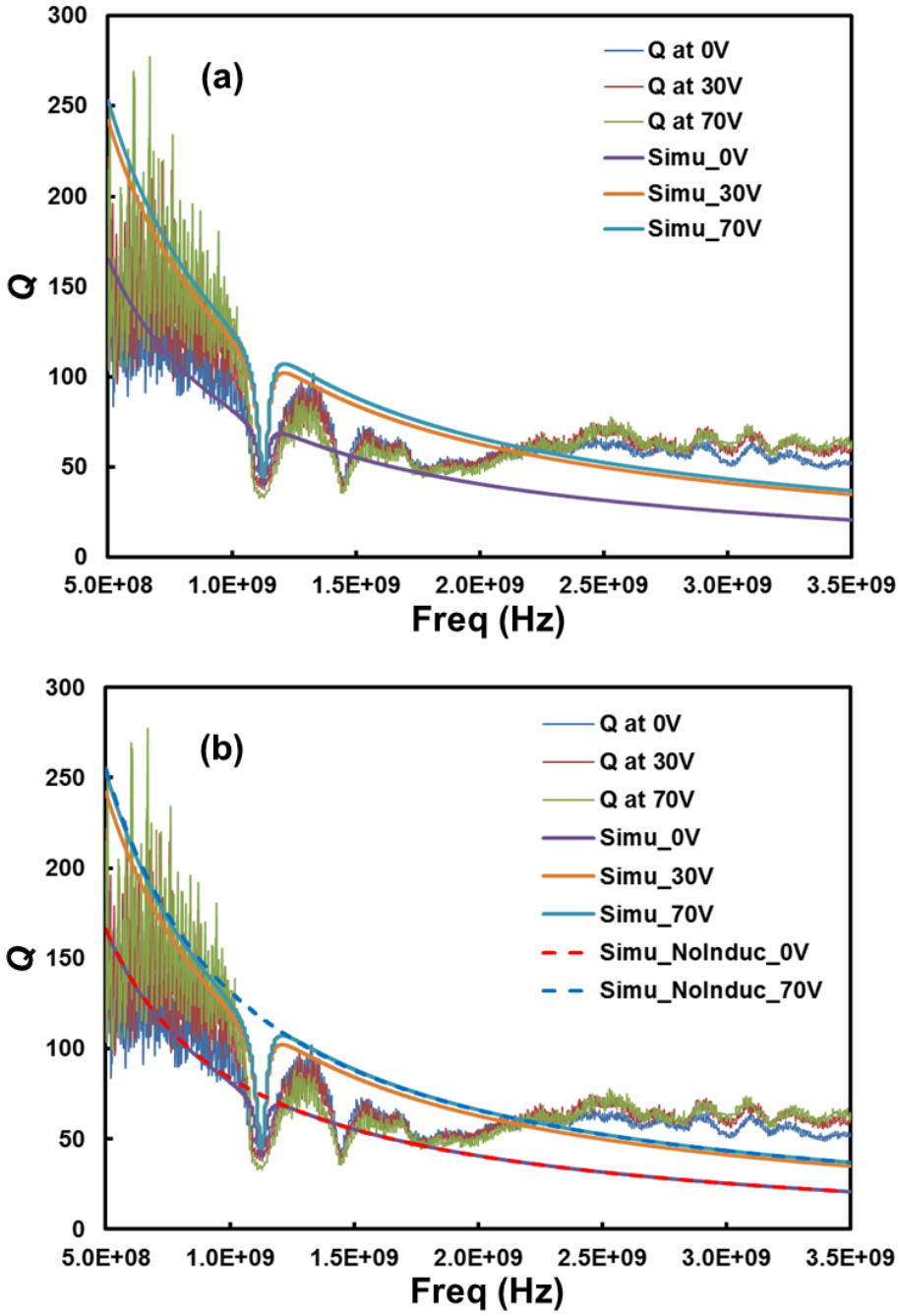

Figure 5-10 Experimental and simulated *Q* versus frequency curves at different reverse biases for a 1-port device. (a) The simulation considers the LC resonance in the DC path and (b) the simulation (dashed curves) does not consider the LC resonance in the DC path.

5.2.2 Measurements for the 2-port devices

The schematic diagram for the 2-port measurements is shown in Figure 5-11. Calibration to the two GSG probe tips using an open/short/load/through scheme was done before device measurements. Same as the 1-port measurement setup, there are bias-Tees in between the network analyzer and the GSG probe tips to protect the network analyzer at high reverse biases; the leakage current is recorded during the measurements through a 50-ohm resistor in parallel with a voltage meter.

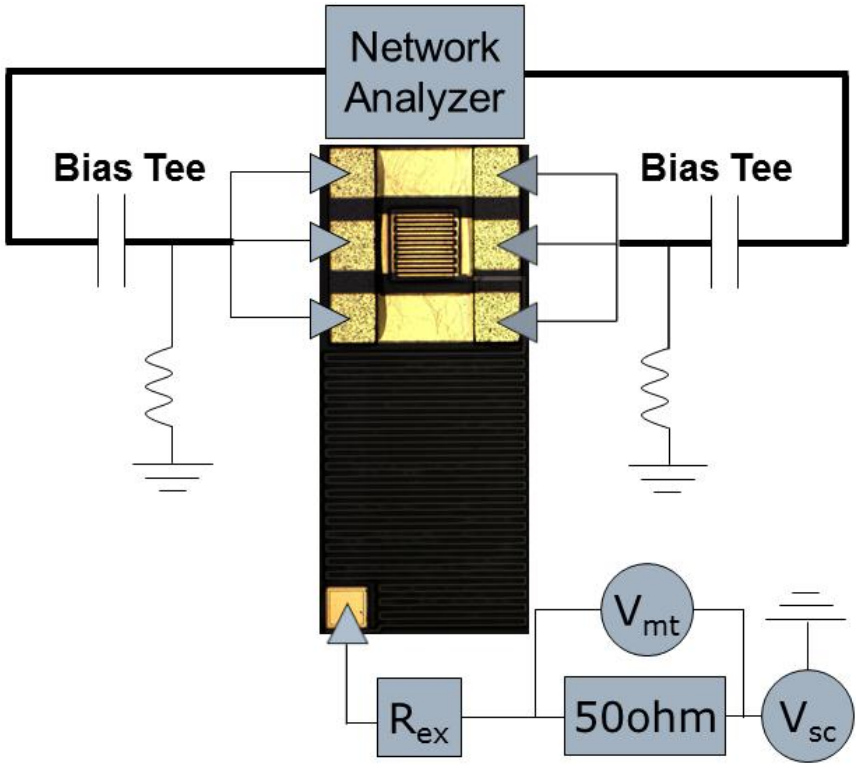

Figure 5-11 Schematic diagram for the 2-port measurements.

The improved reverse I-V characteristics by using the improved fabrication procedure are first shown in Figure 5-12. The leakage is slightly higher than the 1-port device shown above due to a larger diode area.

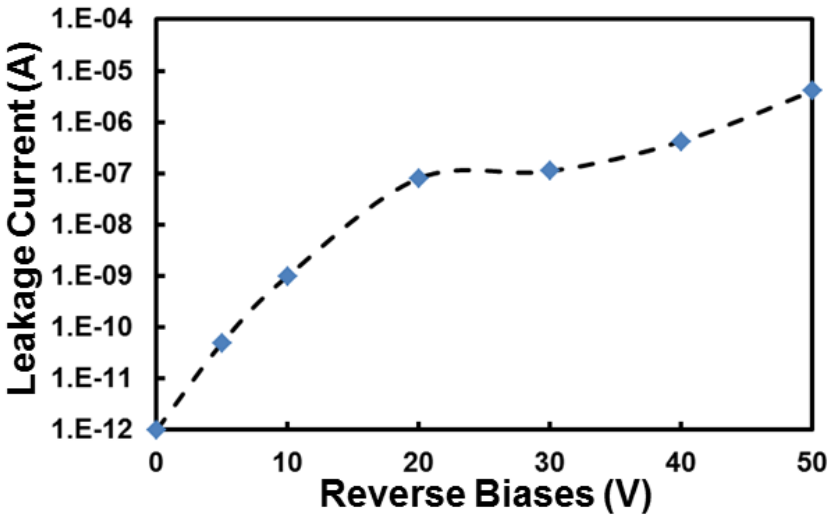

Figure 5-12 Reverse I-V curve for a 2-port anti-parallel diode varactor. The dots are the measurement data points.

The representative S-parameters from 500 MHz to 3.5 GHz for the varactor 2-port measurements are shown in Figure 5-13. The S11 in the Smith Chart goes from the open (high reflection) to the 50 ohms (low reflection) along the 50-ohm resistance circle from low frequency to high frequency, indicating a capacitor with a low-resistance series resistor from the device; the magnitude of S21 (along the 50-ohm resistance circle as well) increases with the frequency increase, indicating higher transmission at higher frequencies (due to the lower impedance from the device at higher frequencies).

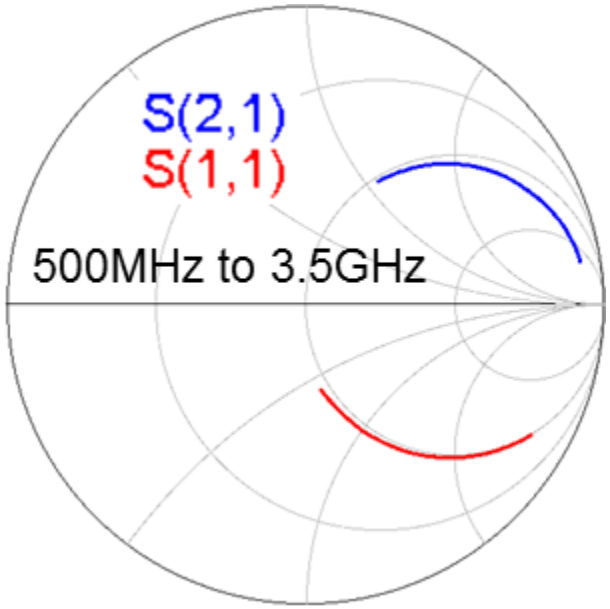

Figure 5-13 The representative S-parameters for the varactor 2-port measurements.

The relations of *Q* versus reverse bias, R_s versus reverse bias and C_s versus reverse bias are shown in Figure 5-14. The clear trends of *Q* increase and R_s decrease at 1 GHz with the increase in reverse biases are shown in Figure 5-14(a) and 5-14(b), respectively. This trend is consistent with the theoretical expectation: when reverse bias increases the depletion thickness in n^- GaN increases as well, which results in a lower C_s and R_s so that a higher *Q*. A high *Q* of >180 was thus achieved at 1 GHz. However, the trends for the data at 2 GHz and 3 GHz are not as clear as the data at 1 GHz, possibly due to the parasitic reactance from the device. Figure 5-14(c) shows the C-V curves extracted from the 2-port S-parameter measurements. The simulated C-V curve using a 1-D Poisson solver fit the experimental results very well. It indicates that the layout of the 2-port devices suffers much less parasitic components. In comparison with the C-V curves obtained from the 1-port devices shown in Figure 5-15, the

mismatch between the experimental results and theoretical simulations for the 1-port device is likely due to more parasitics and/or more processing errors during the fabrication for the narrower and shorter interdigitated finger structures. For example, a 0.25 μm undercut during the Ni wet etch represents 20% error for the 2.5-μm-wide fingers but only 7% for the 7-μm-wide fingers. The Ni undercut certainly reduces the actual area of the Schottky contact (the measured capacitance is lower than the simulated capacitance at zero bias as shown in the Figure 5-15) and changes the electric field distribution underlying the Schottky contact so that the C-V characteristics of the varactor diodes as well.

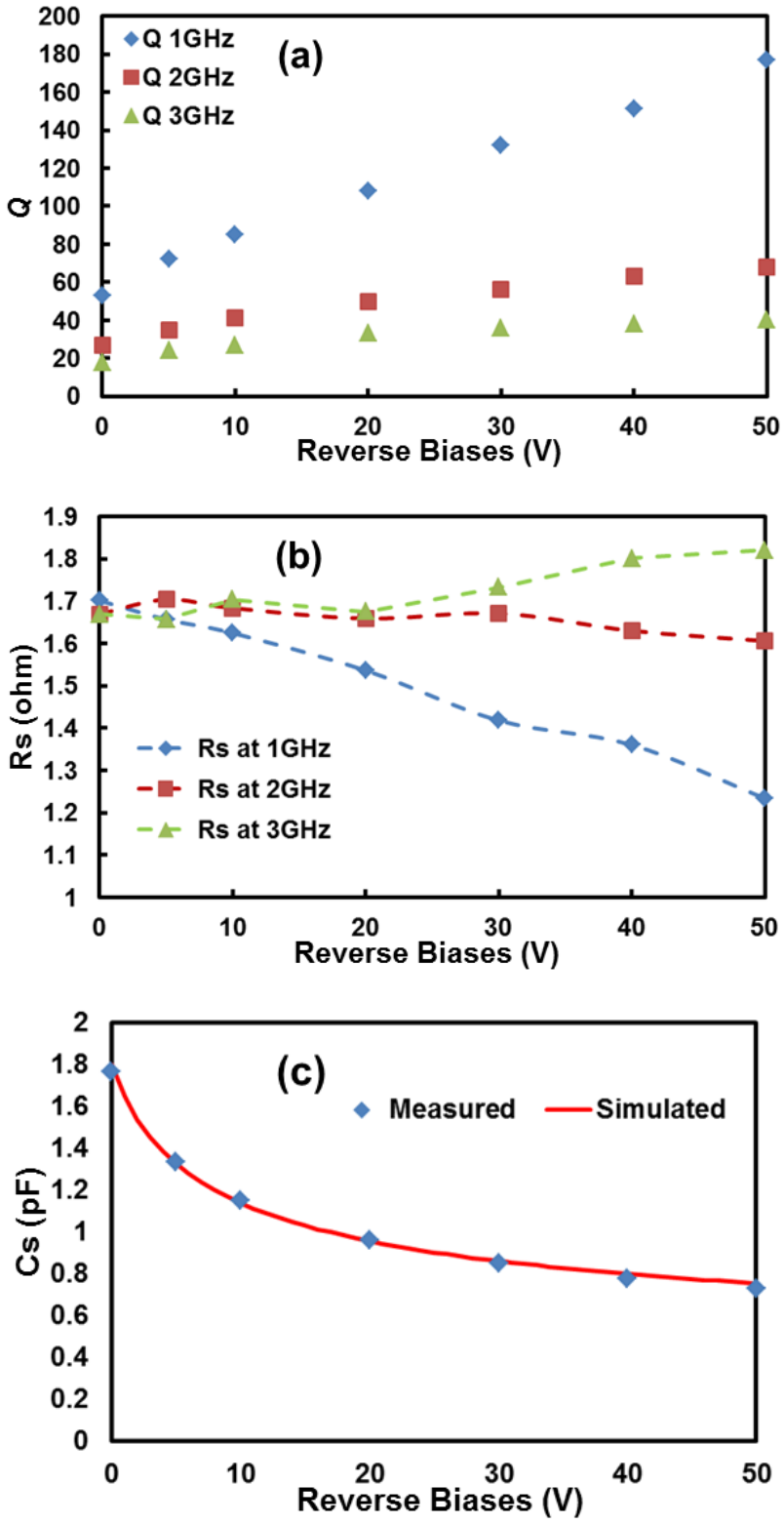

Figure 5-14 The relations of (a) *Q* versus reverse bias, (b) R_s versus reverse bias and (c) C_s versus reverse bias at 1 GHz, 2 GHz and 3 GHz for a 2-port device.

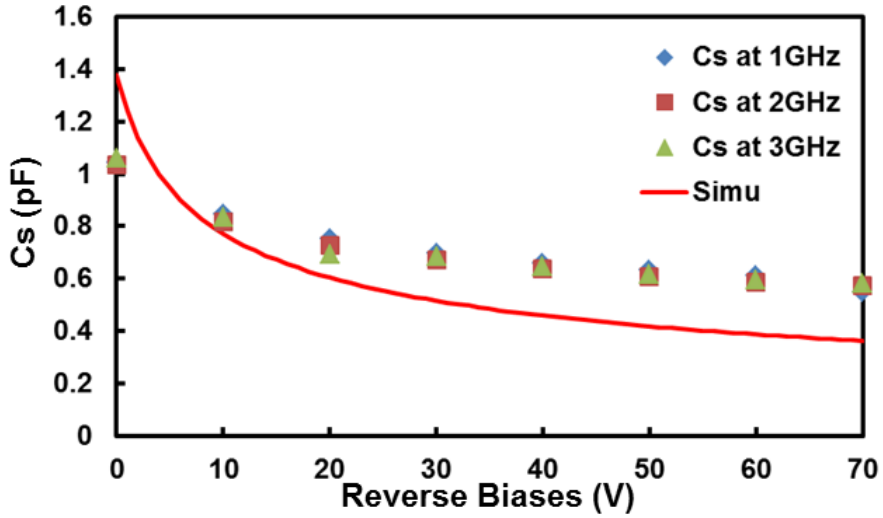

Figure 5-15 The experimental and simulated C_s versus reverse bias curves for a 1-port device.

The relation of *Q* versus frequency extracted from the S-parameter measurement is then shown in Figure 5-16. A *Q* of above 70 at 2 GHz was obtained. Unlike the measurements done on the 1-port device, the *Q* shows a strong dependence on reverse biases which is consistent with the theoretical prediction. Several resonances in the *Q* versus frequency curves are also observed at frequencies between 1 GHz and 2 GHz, which are attributed to the LC resonance in the DC path, same as the 1-port measurements.

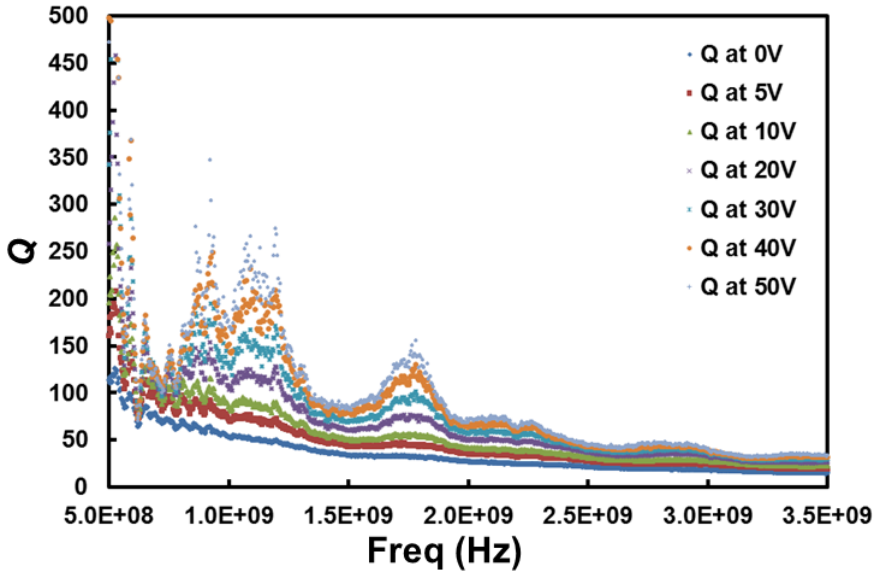

Figure 5-16 The relation between *Q* and frequency at different reverse biases for a 2-port device.

The ADS simulation results based on the same model shown in Figure 5-9, except that there is a port 2 symmetrically located at the other side of the varactor diode as the RF output, are shown in Figure 5-17. The inductance from the DC needle probe and the coaxial cable and the capacitance from the n^+ GaN resistor are identical with the values used in the 1-port simulations. The simulated curves fit the experimental curves reasonably well including the LC resonances from the DC path (only match one of the resonances though). The simulated curves without considering the LC resonance from the DC path are also included in the Figure 5-17(b).

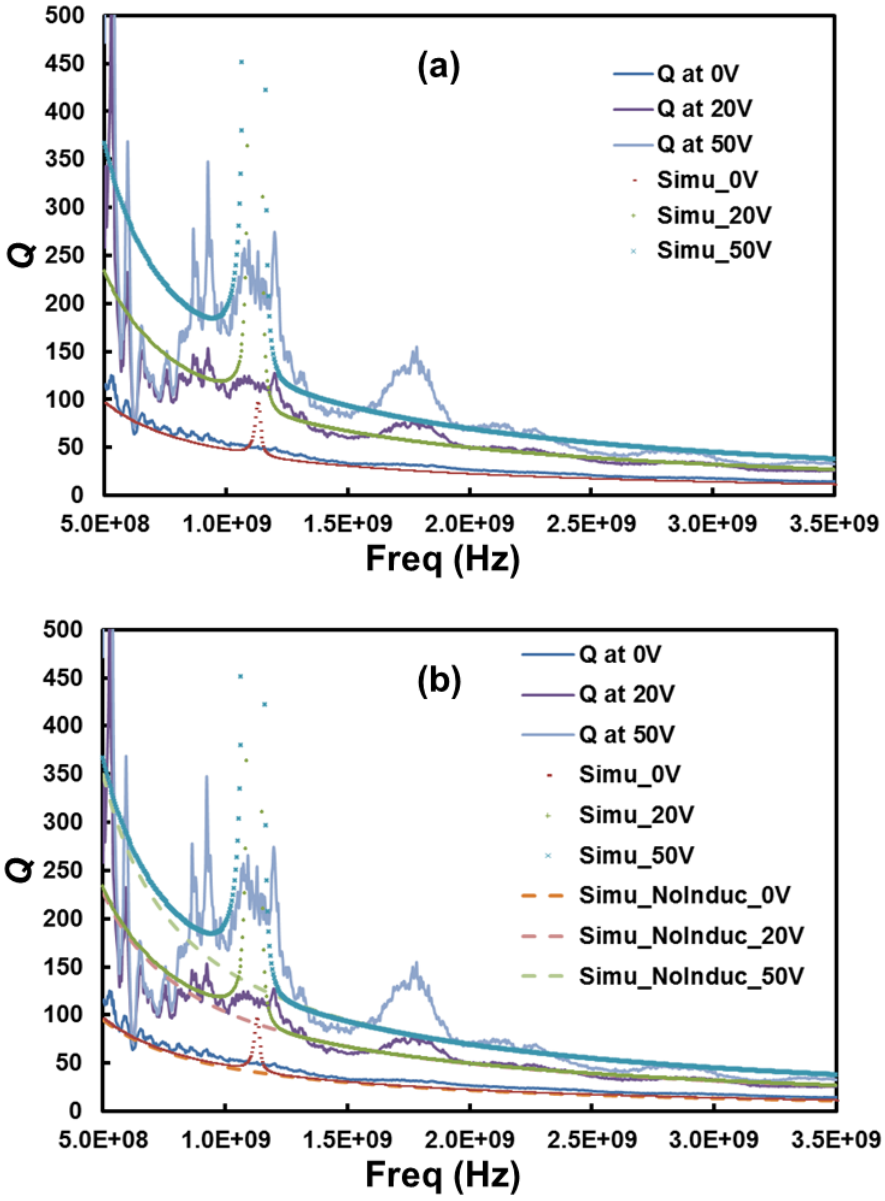

Figure 5-17 Experimental and simulated *Q* versus frequency curves at different reverse biases for a 2-port device. (a) The simulation considers the LC resonance in the DC path and (b) the simulation (dashed curves) does not consider the LC resonance in the DC path.

More 2-port devices with different areas and structures were also measured. Their optical microscopy images and the corresponding *Q* versus frequency curves (including the one discussed above) are shown in Figure 5-18. As theoretically

expected, a clear trend of *Q* increase with the increase of reverse bias is observed for all of the 2-port devices. In comparison, the *Q* does not show clear dependence on the reverse biases for the 1-port devices. It is also shown that the *Q* is higher for smaller devices: $Q > 250$ at 2 GHz was obtained for varactors with C_{max} (when reverse bias is zero) less than 1 pF. However, the high *Q* values at the low frequencies are not reliable because of LC resonance in the DC path. This unrealistically high *Q* values become more obvious for the very small device, e.g., the device shown in Figure 5-18(c). That is because when the capacitance of the varactor is low, the impedance of the varactor becomes high so that the RF signal leaks more through the DC path, especially near the LC resonance frequencies.

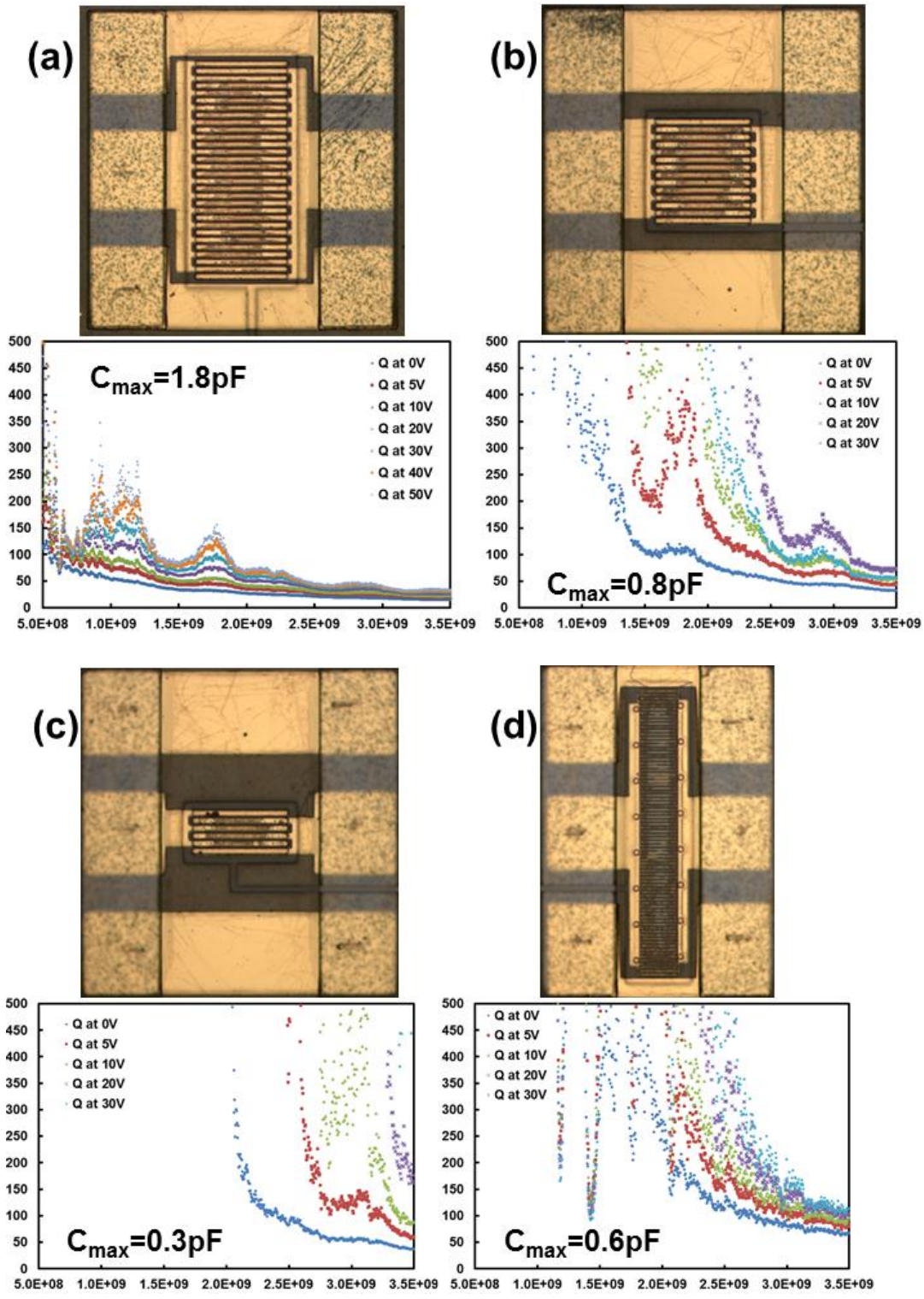

Figure 5-18 Optical microscopy images and the corresponding experimental *Q* versus frequency curves for the 2-port devices with different areas and structures. C_{max} corresponds to the capacitance of the varactor at zero reverse bias.

5.3 Linearity measurements

The linearity property of microwave power varactors was evaluated via a two-tone test and an experiment using a 2-W WCDMA signal input.

5.3.1 Two-tone test

The two-tone test measurement setup is shown in Figure 5-19. Power amplifiers are used after the two signal generators to increase the input power in order to obtain the measureable IM3 (third-order intermodulation) above the noise floor of the spectrum analyzer. Attenuators (not shown in the diagram) are used before the spectrum analyzer to minimize the IM3 generated from the spectrum analyzer. The anti-parallel diode varactor is connected in shunt to a 50-Ω line (spectrum analyzer). The frequencies of the two tones are 1.1 GHz and 1.115 GHz, respectively. Before the two-tone test for the varactors, the linearity of the measurement setup was first verified by measuring the OIP3 (third-order intercept point) without having the varactors in the measurement circuit.

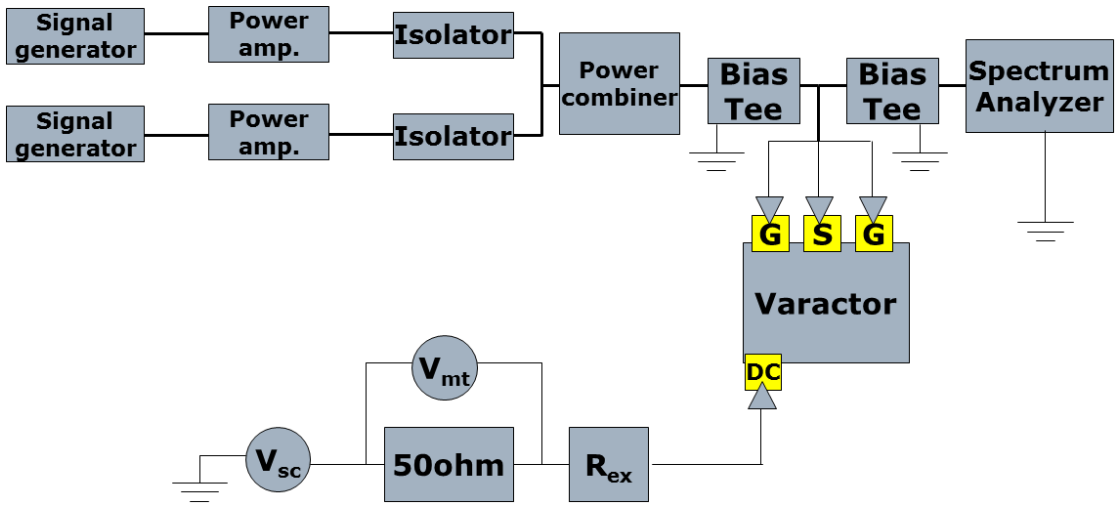

Figure 5-19 Measurement setup for the two-tone test.

As shown in Figure 5-20, at RF input power of 26 dBm to the measured varactor, the IM3 products were at a level of -90 dBc relative to the outputs at the input frequencies (for a control reverse bias voltage of 25 V). This corresponds to an OIP3 of 71 dBm. However, equipment limitations prevented obtaining accurate IM3 values for larger reverse biases (where much higher OIP3 values are expected): IM3 is buried under the noise floor of the spectrum analyzer. By contrast, for single varactor diodes, the measured OIP3 value was 36 dBm, for control voltage set to 0 V, showing much worse linearity.

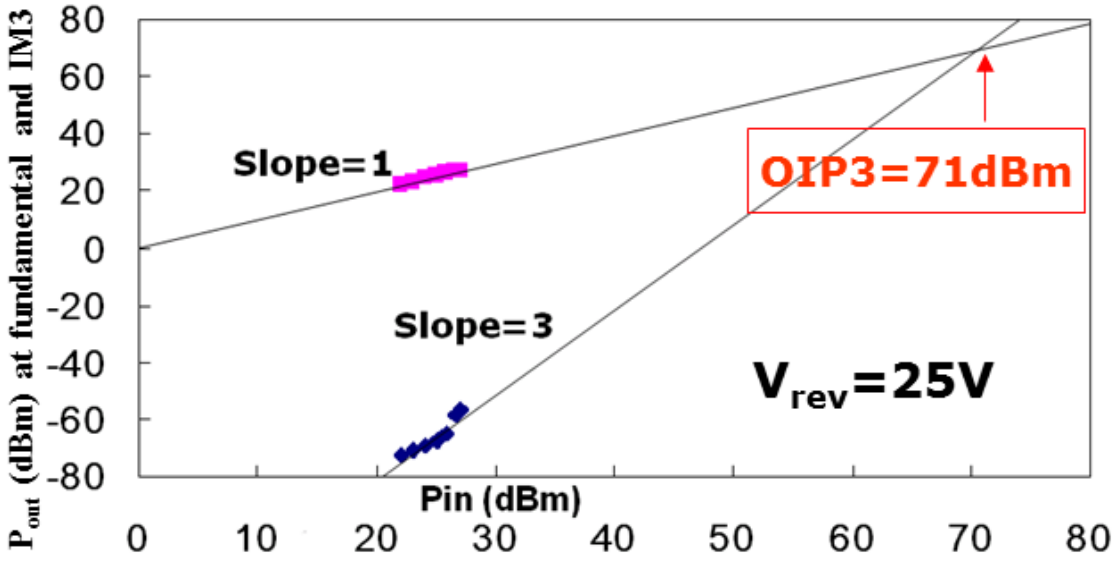

Figure 5-20 Output power at fundamental and IM3 frequencies versus the input power for an anti-parallel diode varactor (1-port) at a control reverse bias of 25 V.

The reverse voltage dependence of a single diode varactor can be usually expressed as

$$C(V) = K/(\phi + V)^n$$

Eq. 5-3

where K is the capacitance constant, ϕ is the built-in potential of the diode, V is the reverse voltage and n is the exponent of the voltage dependence of the diode capacitance. The linearity of the anti-parallel diode has a strong dependence on the n factor. Theoretically a distortion-free varactor diode can be achieved with n = 0.5, which corresponding to a Schottky diode with uniform doping [2]. An ADS simulation, assuming the varactor follows the C-V characteristics as Eq. 5-3, was performed to verify the OIP3 of the device. The n factor for the device (1-port) we

measured is 0.4, confirmed by the C-V curve fitting, although the doping in the varactor region is uniform. The deviation of the extracted n factor (< 0.5) is probably caused by the parasitic components in the device and/or the imperfection of the device fabrication (e.g., the formation of the Ni undercut during Ni wet etch). The experimental and simulated results including the ideal case of n = 0.5 are shown in the Table 5-1. The simulated OIP3 of 73 for the measured 1-port device (n = 0.4) at a reverse bias of 25 V is almost consistent with the measured value. The simulated OIP3 of 80.5 at a reverse bias of 25 V for the ideal case (n = 0.5) indicates that a much higher OIP3 can be obtained by further improving the device layout and fabrication procedure. A minimum OIP3 requirement in the wireless base station applications is also listed in the table. It suggests that the obtained OIP3 for our varactors already meets the linearity requirement in some practical applications.

Table 5-1 Measured and simulated OIP3 for the anti-parallel diode varactor with different n factors.

n	Meas_OIP3 (dBm) at 25V	Simu_OIP3 (dBm) at 25V	OIP3 requirement in wireless base-station applications (dBm)
0.4	70	73	>65
0.5	N.A.	80.5	

5.3.2 2-W WCDMA signal input

The linearity of the varactor was also evaluated by using a 2-W WCDMA signal input experiment. The measurement setup is shown in Figure 5-21. The linearity of the system was first calibrated by measuring without the varactor in the measurement setup. The maximum average power that the WCDMA signal generator can output without significant signal distortion (nonlinearity) is ~-17 dBm. The peak to average ratio (PAR) of this WCDMA signal is 7.8 dB. The power amplifier has a gain of 50 dB. Therefore, the maximum average and peak power (without significant signal distortion from the system) of the WCDMA input signal to the varactor are 33 dBm and 40.8 dBm (2 W and 12 W), respectively.

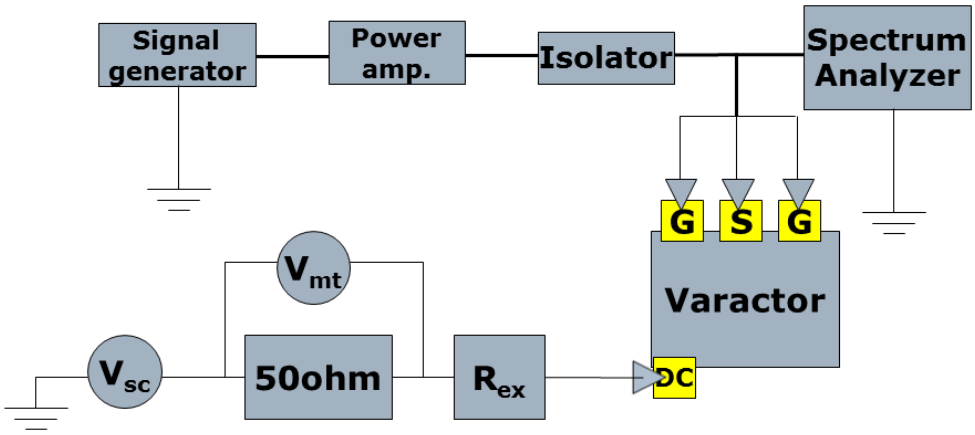

Figure 5-21 Measurement setup for the WCDMA signal input experiment.

The measured adjacent channel leakage ratio (ACLR) for a small 1-port device with a WCDMA signal input of 2 W (12 W peak power) is -53 dBc as shown in

Figure 5-22. It indicates that the IM3 is still negligible under such high input power levels.

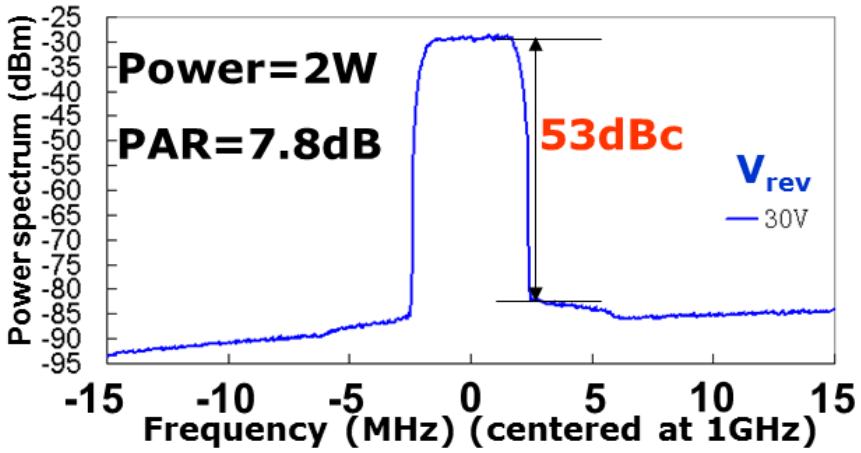

Figure 5-22 Adjacent channel leakage ratio (ACLR) for a small 1-port device with a 2-W (12-W peak power) WCDMA signal input.

A simulation was carried out to calculate the actual RF voltage (corresponding to the actual RF power) applied to the varactor diode. Figure 5-23(a) shows the equivalent circuit model of the measurement system. The RF cables were considered as transmission lines for more accurate simulations. As seen in Figure 5-23(b), the RF voltage applied to the varactor (named V_{cap} in the simulation) is almost identical to the RF voltage coming from the signal generator (named V_{sc} in the simulation). This simulation results confirmed the validity of the measurement system so that the measurement result: the anti-parallel diode varactor with a low ACLR of <-53 dBc under a 2-W (12-W peak power) WCDMA signal input has been achieved.

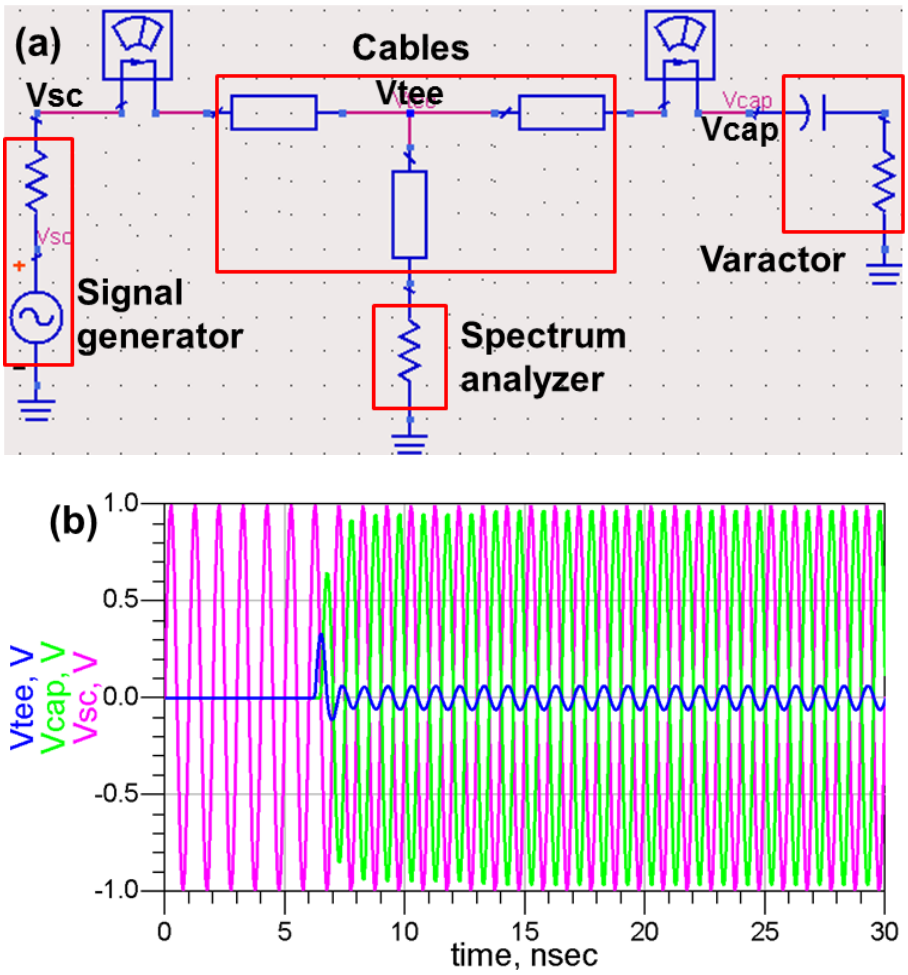

Figure 5-23 (a) Equivalent circuit model of the measurement system for the WCDMA signal input experiment, and (b) simulated instantaneous RF voltage at different nodes.

5.4 Application in the tunable resonant circuit

The preliminary application of the varactor is demonstrated by building a tunable resonant circuit using the varactor and transmission lines. The measurement setup up is shown in Figure 5-24.

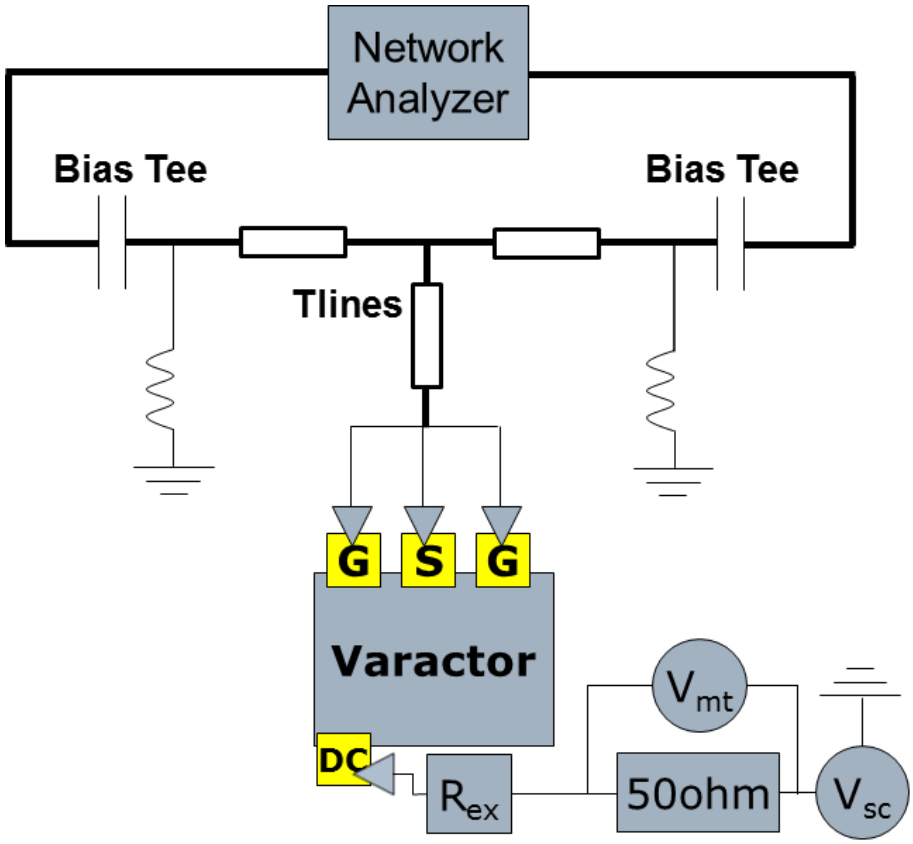

Figure 5-24 Measurement setup of the tunable resonant circuit using the varactor and transmission lines.

The resonance mainly comes from the varactor and the series transmission line. Different length of transmission lines (for the transmission line that is in series with the varactor) were used to see the resonance at different frequencies. Figure 5-25 shows the well matched measurement and simulation results with the series-transmission-line length of ~7 cm and ~11 cm.

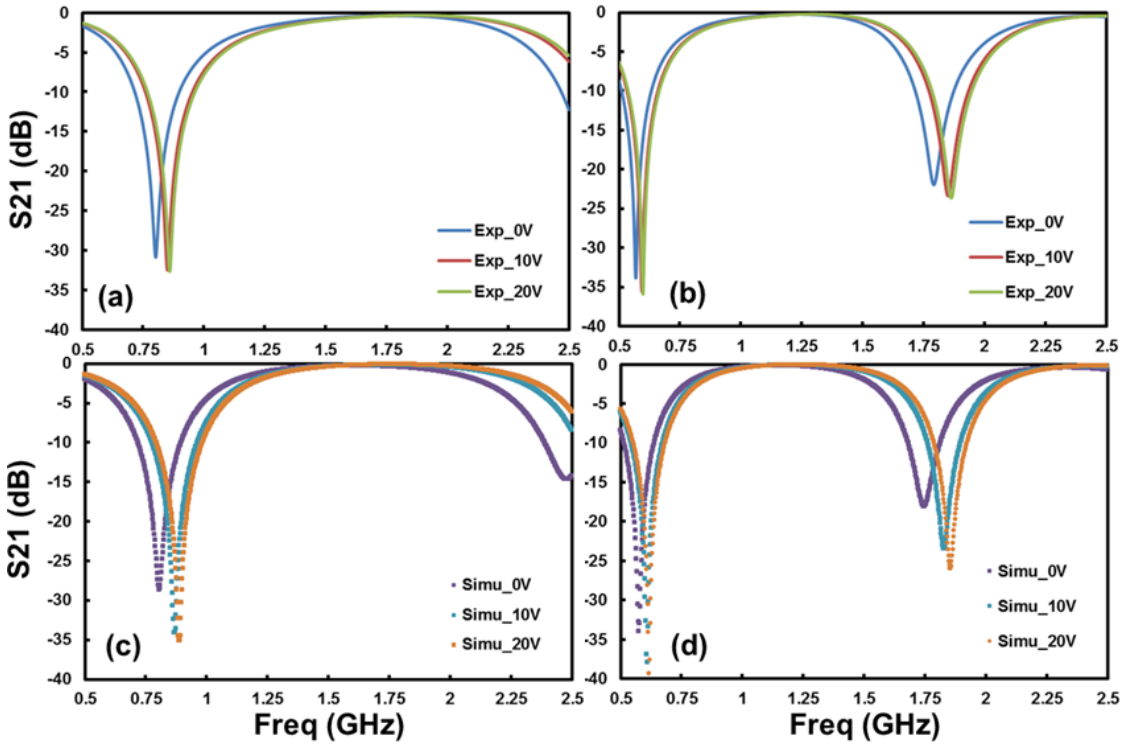

Figure 5-25 (a), (b) Experimental and (c), (d) the corresponding simulated S21 curves from 0.5 GHz to 2.5 GHz, for the tunable resonant circuit using varactor and transmission lines. (a) uses a shorter (~7 cm) transmission line in series with the varactor and (b) uses a longer (~11 cm) one.

Different resonance frequencies were observed for the resonance circuits using different length of the series transmission lines. It is also seen that the resonance frequency varies with the control bias voltage of the varactor. These results suggest that these varactors are already good for designing sharp tunable filters.

5.5 Summary

This chapter reported the experimental DC and RF measurement results and the corresponding analysis for the GaN-based microwave power varactors fabricated with the improved fabrication procedure. Benefited from the improved fabrication procedure (better reverse I-V characteristics, thicker metal stripe thickness, etc.), the breakdown voltage of greater than 100 V, *Q* of above 120 at 1 GHz for 1-port device and *Q* of above 250 at 2 GHz for small 2-port devices, and OIP3 of >71 dBm (ACLR of <-53 dBc under 2-W WCDMA signal input) were obtained. Real applications in the tunable resonant circuit were also demonstrated. The results indicate that the varactors already meet the representative requirements for some practical use.

5.6 References

[1] http://www.sonnetsoftware.com/

[2] K. Buisman, L. C. N. de Vreede, L. E. Larson, M. Spirito, A. Akhnoukh, T. L. M. Scholtes, and L. K. Nanver, "Distortion-free varactor diode topologies for RF adaptivity," in Proc. IEEE MTTS Int. Microwave Symp., Long Beach, CA, pp. 157–160, Jun. 2005.

Chapter 6

Conclusion and Future Work

The goal of this study was to develop material and device structures for high power, high *Q* and high linearity microwave varactors for the wireless base station applications. The detailed results demonstrated in this work potentially meet the specifications for practical use. However, more work is still needed in order to achieve better performance and possibly commercialization.

6.1 Summary of the thesis

This dissertation presented the design, fabrication and characterization of GaN-based microwave power varactors. The results and conclusion are summarized below:

1) The design rules for high power, high *Q* and high linearity microwave varactors have been developed. GaN, with its high electron mobility and high breakdown electric field, showed the highest figure-of-merit Q_{min} in

comparison with other common semiconductors, is therefore considered a prime candidate material.

2) InGaN surface layer has been designed to increase the breakdown voltage and reduce the reverse leakage current for GaN-based Schottky diodes. Experimentally, the breakdown voltage of the GaN-based Schottky diodes was increased to >120 V from ~80 V by employing the InGaN surface layer design.

3) Comprehensive studies on the Ni-InGaN/GaN Schottky barriers (using InGaN surface layer design) were carried out. Due to the polarization induced charges at the InGaN/GaN interface, the electron tunneling probability of InGaN/GaN Schottky barrier is greatly suppressed in comparison with the GaN-only design. As a result, the reverse leakage current and breakdown voltage of the InGaN/GaN Schottky diodes are improved. The polarization chargers at the InGaN/GaN interface influence the forward I-V characteristics of the InGaN/GaN Schottky diodes as well: a subthreshold slope of > 60 mV/decade is caused by the forward bias dependent Schottky barrier height (induced by the polarization charges at the interface). These forward and reverse I-V characteristics are different from those of the GaN-only design as confirmed by experimental measurements and theoretical simulations. The HP-MOCVD-growth technique of the GaN buffer layer was also found to be effective in reducing the leakage current and increasing the breakdown voltage of GaN Schottky barriers by achieving low-defect-density materials. Surface

micromesas were observed on InGaN/GaN epi-layers by NOM, SEM and AFM, mostly originated from nanopipes in GaN. Studies of RBS and the electrical characteristics on corresponding Ni-InGaN/GaN Schottky barriers indicated that the surface micromesas with nanopipes at the center were the main source of reverse leakage current and introduced an easy metal diffusion path, even under relatively low-temperature thermal anneal. The application of InGaN surface layer design in the enhancement-mode GaN-based HEMTs was also introduced.

4) An initial fabrication procedure was first developed. The DC and RF measurements performed on the devices fabricated using the initial fabrication procedure indicated that the device performance (*Q*, reliability, etc.) suffered from excess reverse leakage current which was caused by certain fabrication steps. Sidewall damage and defect-related thermal diffusion near the Ni-InGaN junction were found to be the reasons for the excess leakage caused during the device fabrication. An improved fabrication procedure was successfully developed. Avoiding any high temperature processing (> 190 ^{o}C) and ALD Al_2O_3 with KOH pre-treatment for GaN mesa sidewall passivation were found to be important in reducing leakage current and maintaining low leakage current during the device fabrication.

5) Benefited from the improved fabrication procedure, the reverse leakage current was maintained at low levels after the entire device fabrication. DC and RF

characterizations have confirmed high performance GaN-based microwave power varactors. The breakdown voltage of greater than 100 V, *Q* of above 120 at 1 GHz for 1-port device and *Q* of above 250 at 2 GHz for small 2-port devices, and OIP3 of >71 dBm (ACLR of <-53 dBc under 2-W WCDMA signal input) were obtained. The real application in the tunable resonant circuit was also demonstrated. The results indicate that the varactors already meet the representative requirements for some practical use.

6.2 Comparison of different varactor technologies

The performance parameters of different varactor technologies are summarized in Table 6-1. GaAs, Si-on-glass and MEMS varactor technologies can achieve very high *Q* at high frequencies, however, are usually used in low power levels. The *Q* would be expected to be significantly lower when these technologies are used for high operation voltages as we discussed in Chapter 1. Specifically for MEMS technology, it achieved a *Q* of > 80 at 40 GHz and breakdown voltage of > 34 V. However, due to its mechanical operation, the switching speed is slow (typically in MHz range) in comparison with the Schottky diode technology. The reliability is also a concern for the mechanical system (mechanical parts are prone to damage after certain number of operations).

For high power varactors, recently high-voltage and high-*Q* SiC microwave varactors have been reported. A *Q* of 160 at 2 GHz with breakdown voltage of >150 V was achieved. However, the reported SiC varactor was based on a single diode structure and the linearity of the device has not been reported yet. In our work, a *Q* of > 70 at 2 GHz with breakdown voltage of > 120 V for a large diode (with C_{max} = 1.8 pF for an anti-parallel diode varactor in comparison with the C_{max} = 0.9 pF reported for the SiC single diode varactor). For smaller varactors, a much higher *Q* of above 250 at 2 GHz has been achieved. For the linearity, by employing the anti-parallel diode device topology, an OIP3 of >71 dBm and an ACLR of <-53 dBc under a 2-W WCDMA signal input were obtained. To the best of our knowledge, GaN-based microwave power varactors currently show the best performance in terms of the combination of breakdown voltage, *Q* and linearity properties.

Table 6-1 The performance parameters of different varactor technologies.

Technology	*Q*	Breakdown (V)	OIP3 (dBm)
GaAs (2 GHz) [1]	62 (max)	28	57
Si-on-glass (2 GHz) [2]	100~300	>12	60
MEMS (40 GHz) [3]	>80	>34	N.A.
SiC (2GHz, C_{max}=0.9 pF) [4]	160 (max)	>150	N.A.
This work (GaN at 2GHz, C_{max}=1.8 pF)	>70 (max)	>120	70

6.3 Future work

In retrospect, there are a few areas of further investigation for advancing the GaN-based high power microwave varactors that employ Schottky barriers:

1) From the fabrication point of view, it is important to further improve the fabrication procedure to maintain low leakage current and high breakdown voltage during the device fabrication. This not only affects the *Q* factor but also the reliability of the device. Additionally, as discussed in section 5.2, Ni undercut formed by the Ni wet etch is a problem, especially for the narrower finger devices, causing non-ideal C-V tuning and possible nonlinearity to the anti-parallel diode varactors (due to the resultant $n \neq 0.5$ in Eq. 5-3). Therefore, improving the fabrication procedure to mitigate the Ni undercut is important for obtaining better performance. A straightforward method is to decrease the thickness of the first Ni layer (which is in contact with the semiconductor), in which less etch time is needed so that less undercut can be achieved. Another possible way to further improve the *Q* factor is to further increase the metal stripe thickness to achieve lower series resistance.

2) From the analysis point of view, it is important to further explore the reasons responsible for different characteristics of the 1-port and 2-port devices, although some analysis has been made in chapter 5. This can be valuable for the future device designs.

3) The LC resonance in the DC path should be considered in the future device/circuit designs. As for avoiding the LC resonance in the measurements, a big series inductor can be added into the DC path.

4) Demonstrate other circuit applications, e.g., tunable filters, high-efficiency, high power, tunable power amplifiers.

6.4 References

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Appendix A

GaN-based varactor fabrication procedure

Part I: Schottky contact and thick metal deposition

1. Grow material using MOCVD.
2. Immediately immerse wafer into NH_4OH for 1min (without DI water rinse) and dry with N_2 blow.
3. Immediately deposit Ni (Schottky contact) using E-beam evaporator.

Photolithography using NR9-3000PY for thick metal stripe deposition

4. Spin HMDS (adhesion promoter) at 3000rpm for 40s.
5. Spin NR9-3000PY at 5000rpm for 45s (~2.4μm photoresist thickness).
6. Bake at 150^{o}C for 70s.
7. Expose with MA6 at 11mW/cm^2 for 3~4s.
8. Bake at 100^{o}C for 70s.
9. Develop in RD6 for 10s without agitation. Rinse with DI water.

10. Bake at 100^{o}C for 70s.
11. Descum using O_2 plasma in P80 and dip into HCl (1:3 diluted) for 30s.
12. Bake at 100^{o}C for 70s.
13. Deposit thick metal (Cr/Au/Cr/Ni) using E-beam evaporator.
14. Lift off in acetone. Clean with IPA and DI water. Dry with N_2 blow.

Part II: Ni wet etch (Schottky gate patterning)

Photolithography using S1818 for Ni wet etch

1. Spin HMDS at 3000rpm for 40s.
2. Spin S1818 at 5000rpm for 45s.
3. Bake at 115^{o}C for 70s.
4. Expose with MA6 at 11mW/cm^2 for 15s.
5. Develop in MF321 for 45s with agitation. Rinse with DI water.
6. Bake at 100^{o}C for 70s.

Ni wet etch

7. Immerse into HCl (1:1 diluted) for 1min. Rinse with DI water.
8. Immerse into Ni etchant until etched areas are clear. Rinse with DI water.
9. Remove photoresist and clean with acetone and IPA. Rinse with DI water.

Part III: GaN mesa etch

1. Sputter ~100nm SiO_2.
2. Self-aligned etch SiO_2 in P80 RIE etcher using Ar and CHF_3 to form the sidewall protection layer for the thick Au.
3. Self-aligned etch ~1μm GaN in P80 RIE etcher using BCl_3/Cl_2 at 0^oC.
4. Remove GaN etch residuals in hot KOH solution (~90^oC, 0.1mol/L) for 1min. Rinse with DI water.
5. Grow Al_2O_3 using ALD as GaN mesa sidewall protection layer at 170^oC for ~70nm.
6. Self-aligned etch Al_2O_3 in P80 using $Cl_2/CHF_3/Ar$ (only left Al_2O_3 on the GaN mesa sidewalls).

Part IV: Ohmic contact deposition

1. Repeat the photolithography procedure from 4~12 in part I for ohmic metal deposition.
2. Deposit ohmic metal (Ti/Al/Ti/Au) using E-beam evaporator.
3. Lift off in acetone. Clean with IPA and DI water. Dry with N_2 blow.

Part V: Device isolation and the n^+ GaN serpentine resistor

1. Repeat the photolithography procedure from 4~12 in part I for isolation pattern (as well as the serpentine resistor pattern).
2. Sputter ~150nm SiN_x.
3. Deposit 200nm Ni using E-beam evaporator.
4. Lift off in acetone. Clean with IPA and DI water. Dry with N_2 blow.
5. Etch ~ 2.8μm GaN (n^+ GaN and the GaN buffer layer) in P80 RIE etcher using BCl_3/Cl_2 at 0^oC.
6. Remove GaN etch residuals in hot KOH solution (~90^oC, 0.1mol/L) for 1min. Rinse with DI water.
7. Remove the Ni mask using HCl (1:1 diluted) followed by Ni etchant. Rinse with DI water after every wet etch.
8. Self-aligned etch the SiN_x mask in P80 RIE etcher using CF_4/O_2.

Part VI: BCB curing and etch

1. Spin AP3000 (adhesion promoter) at 3000rpm for 30s.
2. Bake at 125^oC for 90s.
3. Dilute BCB with T1100 (optional).
4. Spin BCB at 500rpm for 10s, 1000rpm for 10s and 5000rpm for 45s.
5. Expose BCB using MA6 at 11mW/cm^2 for 30s.
6. Develop in DS3000 at 35~40^oC for 70s.
7. Stabilize in DS3000 at room temperature for 30s.
8. Spin dry at 2000rpm for 1min with N_2 blow.

9. Bake at 90^{o}C for 3min.
10. Soft cure in forming gas at 170^{o}C for 15mins. Ramp up temperature slowly to avoid BCB cracking.
11. Second layer of BCB: repeat the procedure from 1 to 9 in part VI.
12. Second cure in forming gas at 170^{o}C for 30mins. Ramp up temperature slowly to avoid BCB cracking.

BCB etch

13. Repeat the photolithography procedure from 4~10 in part I for BCB etch mask. Baking time and develop time should be increased in this step.
14. Etch BCB in P80 RIE etcher using CF_4/O_2.
15. Remove the photoresist mask (NR9-3000PY) using acetone when it is etched to very thin. Clean with IPA and DI water.
16. Repeat the above steps 13~15 until the smallest vias are all clear.

Part VII: Pad metal deposition

1. Repeat the photolithography procedure from 4~10 in part I for final pad metal deposition. Baking time and develop time should be increased in this step.
2. Descum in P80 RIE etcher using CF_4/O_2.

3. Immerse into Acetic acid (1:1 diluted) for 30s, HCl (1:3 diluted) for 30s and Ni etchant for 20s. Rinse with DI water after every wet etch.
4. Sputter Ti/Au (10nm/100nm) to improve the BCB sidewall coverage.
5. Deposit Au for 300nm using E-beam evaporator.
6. Lift off in acetone. Clean with IPA and DI water rinse.
7. To thicken the pad metal. Repeat the photolithography procedure from 4~12 in part I. Baking time and develop time should be increased in this step.
8. Deposit Ti/Au (10nm/700nm) using E-beam evaporator.
9. Lift off in acetone. Clean with IPA and DI water rinse.