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Permalink
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Journal
Journal of Microelectromechanical Systems, 7(4)

ISSN
1057-7157

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Publication Date
2007-04-01

DOI
10.1039/b615665g

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On-Wafer Monolithic Encapsulation by Surface Micromachining With Porous Polysilicon Shell

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***Abstract*—In this paper, we present a novel microfabrication technique that solves the main problems of existing monolithic on-chip encapsulation methods for polysilicon surface micromachining. The encapsulation technique includes the formation of a nanoporous polysilicon shell, creation of a cavity by removing the sacrificial layer through the pores in the shell, and sealing the cavity at a low pressure. Formed porous by postdeposition electrochemical etching on top of a sacrificial layer, the porous polysilicon is thick enough to free-stand when released, unlike the previously reported as-deposited permeable polysilicon. Benefiting from the dense pores through the polysilicon layer, the sacrificial material was removed in just one minute, and the vacuum sealing was achieved by a low-pressure chemical vapor deposition polysilicon as thin as 1000 Å with no sealing material detected inside the cavity. The pressure inside the sealed cavity, measured by an *encapsulated* polysilicon Pirani gauge, was around 130 mTorr and showed no noticeable leak (<30 mTorr) over one year. To showcase the applicability, the proposed process was demonstrated through the common Multiuser MEMS Process (MUMPs) foundry service. [1713]**

***Index Terms*—Integrated packaging, porous polysilicon, thin-film encapuslation, vacuum encapsulation.**

I. Introduction

ALTHOUGH microelectromechanical systems (MEMS) products have steadily gained a share in the markets, packaging of the free-standing microdevices is usually developed case-by-case in house and still remains as a significant roadblock in today's commercialization path. Due to the sensitive and fragile nature of the microstructures, the packaging process most often amounts to a major portion of the cost of a MEMS product. On-wafer encapsulation or packaging (also known as zero-level or wafer-level packaging), i.e., packaging all the MEMS devices on the wafer scale simultaneously rather than on an individual die, has long been recognized as a promising approach to simplify the subsequent packaging procedure. With all the moveable microelements housed inside a sealed cavity on wafer, the tools and protocols for mature microelectronics packaging steps, such as dicing, wiring, and molding, can be adopted with little modification, thus reducing the overall packaging cost of a MEMS product.

In general, the on-wafer encapsulation approaches fall into two categories: hybrid wafer bonding and monolithic thin-film encapsulation. In a hybrid approach (shown in the left column in Fig. 1), a separate substrate is bonded to the MEMS wafer to cap the MEMS components using a wide variety of bonding techniques, either in a form of direct surface bonding or using an intermediate layer [1]–[4]. While wafer bonding has been proven and is being widely used in industry, monolithic thin-film encapsulation has been considered to be potentially more cost effective. In the monolithic approach, the process is carried out on the same wafer where the MEMS devices are fabricated by adding extra thin-film processing steps. Illustrated in the right column in Fig. 1, an additional sacrificial layer is deposited on top of an unreleased device and then covered by a thin-film encapsulation layer. After the sacrificial layer is removed through the etch holes in the encapsulation layer, the etch holes are sealed by thin films deposited on top of the encapsulation layer in an appropriate pressure condition. Compared with hybrid wafer-bonding, monolithic thin-film encapsulation has several advantages.

1) It employs thin-film batch fabrication processes, avoiding the need for aligning two wafers and the challenges of bonding on processed (i.e., not smooth) surfaces.
2) It eliminates the seal ring, producing packages with small volume and therefore increasing the number of available dice per wafer.
3) It produces much lower topography, allowing for postencapsulation processes for additional MEMS or IC steps.

The earliest use of on-wafer monolithic encapsulation was by Guckel *et al.* [5] to fabricate an absolute pressure sensor. Ikeda *et al.* [6] used a p^{++} epitaxial silicon shell to encapsulate a silicon resonator. Mastrangelo *et al.* [7] encapsulated a free-standing filament inside a low-pressure chemical-vapor deposition (LPCVD) low-stress silicon nitride cavity to create a micro-incandescent light source. A similar technique was employed by Lin *et al.* [8] to seal a micro comb-drive resonator. Aigner *et al.* [9] demonstrated the vacuum encapsulation of a micromachined gyroscope by the standard passivation layers in the bipolar complementary metal–oxide–semiconductor (BiCMOS) process after fabrication of the BiCMOS circuits. Mei *et al.* [10] fabricated a microdiode device encapsulated inside a vacuum cavity sealed by evaporated silicon dioxide or aluminum. Similarly, Bartek *et al.* [11] used evaporated aluminum as well as LPCVD polysilicon to seal a diode device in a cavity. Recently, Stark and Najafi [12] developed a thin-film electroplated metal package featuring low process temperature (< 250 °C). Candler *et al.* [13] and Hochst *et al.*

Manuscript received October 19, 2005; revised November 5, 2006. This work was supported by the Defense Advanced Research Projects Agency MEMS Program. Subject Editor K. Böhringer.

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Digital Object Identifier 10.1109/JMEMS.2007.892797

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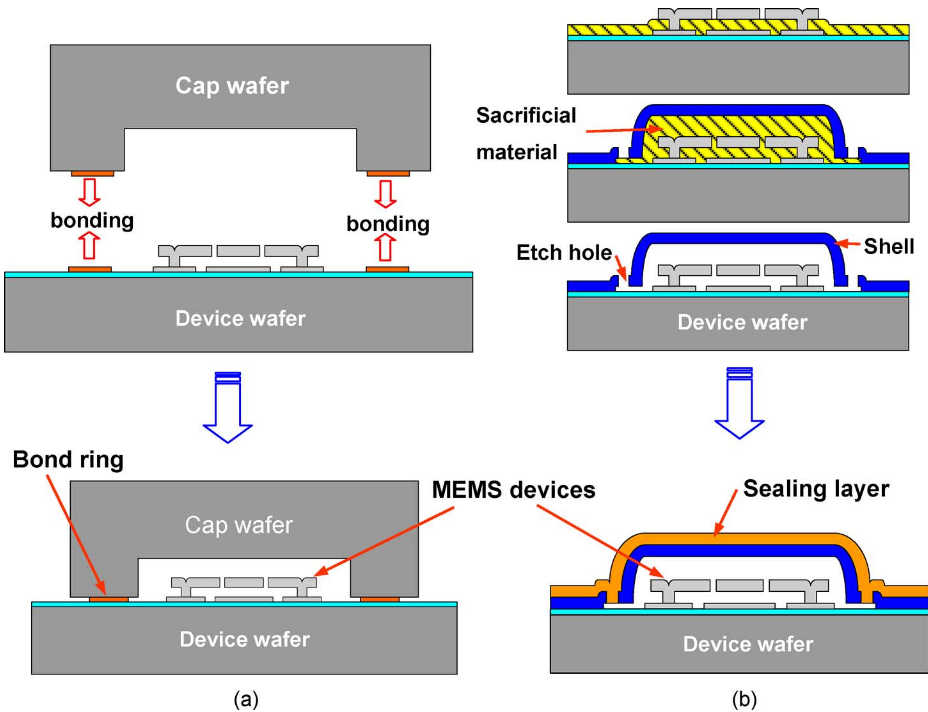


Fig. 1. On-wafer packaging approaches. (a) Hybrid by wafer-to-wafer bonding. The thick cap and the device wafer are bonded together through an intermediate layer or direct surface bonding. (b) Monolithic by thin-film encapsulation. The sacrificial material is removed through the etch holes opened in the encapsulation layer. The formed cavity is closed by a sealing layer.

[14] demonstrated the encapsulation of silicon microdevices using a thick epitaxial silicon thin film.

Despite the anticipated advantages over the hybrid approach using wafer-bonding, the existing monolithic thin-film encapsulation methods suffer from a few drawbacks. Limited by the lithography and etching techniques, the etch holes patterned in the encapsulation shell have a typical size of a few micrometers. Opening vertical etch holes in the encapsulation layer above the device area is not preferable, because a significant amount of sealing material can easily diffuse through the etch holes and deposit on the device surfaces inside the cavity, changing the device characteristics. While this issue can be alleviated by utilizing laterally directed etch channels [5], [8], [12], it takes a long time to remove the sacrificial layer from the cavity, potentially degrading the mechanical properties of the structure material [15]. Improperly designed lateral etch channels can also lead to excessive gas evacuation time during the sealing process [12].

An innovative approach to overcome the aforementioned issues associated with the use of lithographically defined etch holes is to use an encapsulation shell with numerous nanometer scale pores, as the porous shell over the entire cavity area would expedite the removal of the sacrificial layer while the diffusion of the sealing material through the nanopores would be limited. A very thin layer ($\ll 1\ \mu$m) of permeable polysilicon, deposited by LPCVD in a certain process condition [16]–[19], was discovered as the first nanoporous material for MEMS encapsulation application. However, the permeability property was in large part due to its thinness, and the permeable polysilicon was too weak to be a free-standing shell on its own, requiring an additional supporting layer (e.g., 2-μm-thick silicon nitride) with lithographically patterned etch holes. Further, a small amount (80 Å) of sealing material still penetrated the thin permeable layer during sealing. Unfortunately, this amount of sealant, negligible for many applications, would be problematic for such applications as the recent nanogap devices [20].

Desired is a thin film that is permeable yet thick enough (i.e., structurally strong enough) to free-stand as an encapsulation shell, as first proposed in [21]. The thick nanoporous layer also effectively prevents the diffusion of the sealing material through

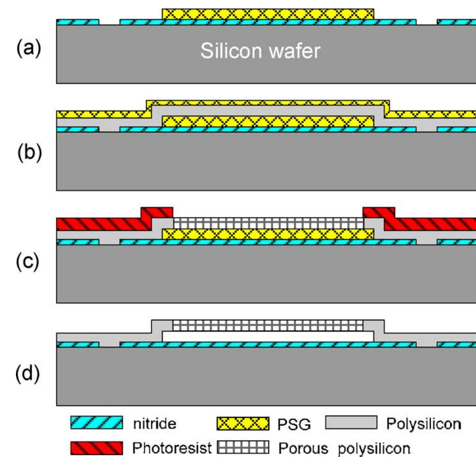


Fig. 2. Process flow of the fabrication of a free-standing porous polysilicon shell. (a) Deposit 0.6 μm Si_3N_4 and 1.5 μm PSG on a silicon wafer. Pattern PSG sacrificial layer and etch nitride insulation layer. (b) Deposit 1.5 μm polysilicon shell and 3000 Å PSG. Anneal at 1000 °C for 1 h. Remove the thin films on the backside of the wafer (not shown in the figures). (c) Selective electrochemical etching in 49% HF: ethanol= 1 : 1. (d) Remove the PSG sacrificial layer and dry in supercritical CO_2 to form porous polysilicon membrane.

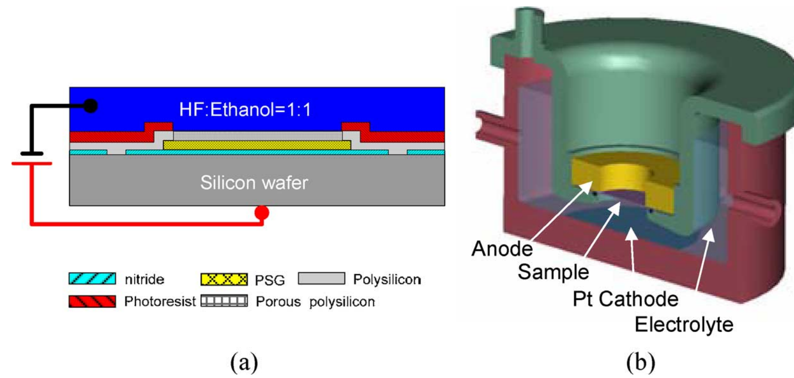


Fig. 3. Electrochemical etching. (a) Schematic cross-sectional figure (b) Schematic of the custom-made Teflon electrochemical etching setup [23].

its pores. In this paper, we first show that the typical thick structural polysilicon in surface micromachining can be made porous by electrochemical etching "after" it is deposited on sacrificial silicon dioxide, which makes the process compatible with typical polysilicon surface micromachining. We then proceed to show other key desired characteristics for monolithic encapsulation are satisfied—fast removal of sacrificial layer and effective sealing, while demonstrating the technique with an on-chip encapsulated polysilicon Pirani gauge.

II. Design and Fabrication

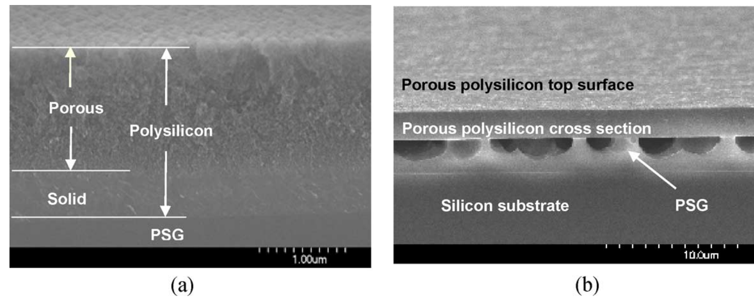
A. Fabrication of Free-Standing Porous Polysilicon Membrane

A critical question in developing the proposed encapsulation technique is whether a free-standing porous polysilicon shell can be fabricated. Traditionally, nonsuspending layers of porous polysilicon were formed on top of conductive silicon, which provides a current path from the backside for electrochemical etching. For the unusual case of a nonconductive surface, Anderson *et al.* [22] have reported that polysilicon sandwiched between two nitride layers can be turned porous laterally by electrochemical etching. However, the porous polysilicon layer was sacrificed by electropolishing to form a nitride channel, rather than being released as a free-standing porous structure. It was not clear whether the polysilicon deposited on top of an insulator such as silicon dioxide and silicon nitride—a typical configuration in the polysilicon surface micromachining—can be turned porous through the entire thickness by electrochemical etching. If this is feasible and residual stress is controlled, a free-standing porous polysilicon membrane can be subsequently obtained by sacrificially removing the insulator material underneath through the pores.

Fig. 2 outlines the process flow to fabricate the free-standing porous polysilicon membrane. The sample was prepared with the steps used for a typical polysilicon surface micromachining process. After low-stress nitride (0.6 μm) was deposited on a silicon substrate, a sacrificial phosphosilicate glass (PSG) layer (1.5 μm) was deposited and patterned. In order to create an electrical contact between the silicon substrate and the upcoming polysilicon for electrochemical etching, openings were made through the silicon nitride layer to the silicon substrate Fig. 2(a). A 1.5 μm undoped polysilicon layer was then deposited by LPCVD, followed by a 2000 Å PSG deposition Fig. 2(b). The polysilicon was symmetrically doped to 0.02 Ω·cm from the PSG layers on both sides by annealing at 1000 °C for 60 min in nitrogen. The annealing also helped release the intrinsic stress in the polysilicon layer. Next, the top PSG layer was stripped by buffered oxide etch (BOE), and all the thin films deposited on the backside of the wafer were etched away by reactive ion etching (RIE) to expose the silicon backside surface for electrical contact with the anode in the electrochemical etching setup [Fig. 3(a)]. After dicing the wafer into 1 $\times$ 1 cm^2 dice, a simple photoresist mask (NR9-8000) was patterned to define the area for electrochemical etching before each die was mounted in a custom-built Teflon cell [Fig. 3(b)] [23] for electrochemical etching. Liquid In-Ga was painted on the backside of the sample to provide good electrical contact between the sample and the copper jig in the Teflon cell. The electrochemical etching was performed in the dark at room temperature in an electrochemical etching solution of 49% HF:ethanol = 1 : 1.

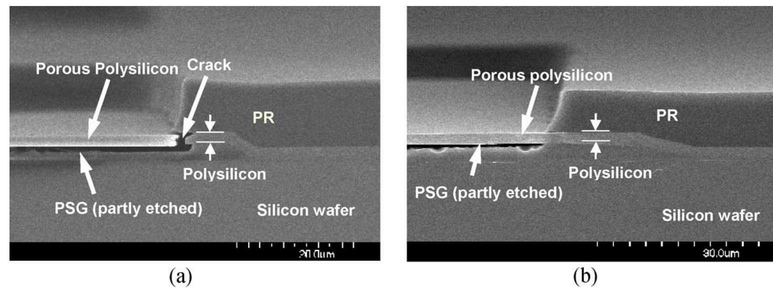
The process of pore growth during the electrochemical etching is displayed in the two scanning electron microscope (SEM) pictures in Fig. 4. Fig. 4(a) is the SEM cross-section of a sample after 200 s of electrochemical etching at 4 mA/cm^2. The porous region in the upper part of the polysilicon layer is visually distinguishable from the solid region underneath. Presented in Fig. 4(b) is the cross-section SEM of the sample after 250 s of electrochemical etching. Many trenches are present in the PSG sacrificial layer right underneath the polysilicon, signifying that the polysilicon layer was turned porous through the entire thickness and thus HF in the electrochemical solution diffused through the porous polysilicon to attack PSG. The irregular etching pattern in PSG indicates the pore growth inside the polysilicon was not uniform along the thickness direction. It was suggested that the electrochemical etching current flows mainly along the polysilicon grain boundaries, resulting in preferential etching and thus a higher pore growth rate at the grain boundaries [24].

The electrochemical etching current was carefully adjusted to prevent the occurrence of electropolishing in the polysilicon under the edge of the photoresist mask. In electrochemical etching, when the current density is higher than that of the first peak in the current-potential curve [25], electropolishing will take place instead of pore formation. However, higher current density and hence higher pore growth rate is preferred



(a) (b)

Fig. 4. The pore formation process in porous polysilicon. (a) The electrochemical etching front is visible after 200 s electrochemical etching at 4 mA/cm^2 constant current. (b) The pores are confirmed through the entire polysilicon thickness by the loss of PSG right under the polysilicon after 250 s etching at 4 mA/cm^2.



(a) (b)

Fig. 5. SEM cros-sections of the electrochemical etching samples. (a) After etching for 140 s at 10 mA/cm^2, a crack was observed in the polysilicon near the edge of the masking photoresist. (b) After etching for 255 s at 4 mA/cm^2, the process was successful.

in our process to prevent the photoresist from peeling off in the HF-ethanol electrochemical etching solution and to minimize etching undercut in the masked area. As shown in Fig. 5(a), a crack was observed in the polysilicon under the edge of the photoresist mask after 140 s electrochemical etching at 10 mA/cm^2, a value obtained by dividing the applied current over the *exposed* polysilicon area. This was because, once the polysilicon in the exposed area was turned porous, the cross-section right under the edge of photoresist was exposed to the etching solution. Suddenly, the same amount of current would be consumed for electrochemically etching the cross-section of the embedded polysilicon, leading to lateral electropolishing of the polysilicon. A high enough current density to keep the photoresist intact during electrochemical etching but low enough to prevent the lateral electropolishing was found, for our device design, when the current density was lowered to 4 mA/cm^2. As shown in Fig. 5(b), no electropolishing was observed after 255 s of etching, while the partly etched PSG indicated that pores are formed through the entire thickness of the polysilicon in the unmasked area.

However, wrinkles and cracks were observed on most of the porous polysilicon membranes once released free-standing, indicating high compressive stress is existent in the layer that had been proven to be low stress before turning porous. As discussed in [26], due to a large amount of H_2 generated during electrochemical etching, excessive hydrogen atoms tend to bond to silicon atoms, resulting in a lattice expansion of the Si-Si bond length and thus introducing the compressive stress in porous silicon. Although the hydrogen can be desorbed from the Si-H bond by annealing at medium temperature (above 400 °C) [26], our challenge was that the porous polysilicon starts to free-stand as a membrane soon after the electrochemical etching is

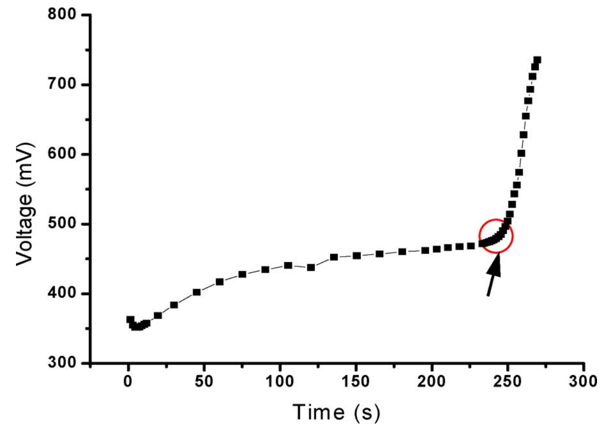


Fig. 6. Typical curve of electrode potential versus time during electrochemical etching when constant current is applied. Circle area indicates etching front has reached the interface of the polysilicon and the sacrificial PSG.

complete, i.e., before the annealing can be performed. In our process, the only window for annealing is after the electrochemical etching front reaches the interface of polysilicon and sacrificial PSG and before the HF-based solution attacks PSG enough to free the porous polysilicon. It was found that the moment when the pores reached the interface can be read by a sharp increase in electrode potential during the electrochemical etching.

Fig. 6 shows a typical plot of electrode potential versus time under a constant current, 4 mA/cm^2 for our sample. Initially, the electrode potential gradually increased and attained a relatively constant value. The time when the potential increased sharply coincided with the moment when the porous etching front reached the interface, confirmed by the cross-section SEM picture in Fig. 7. After the sample was taken out of the etching

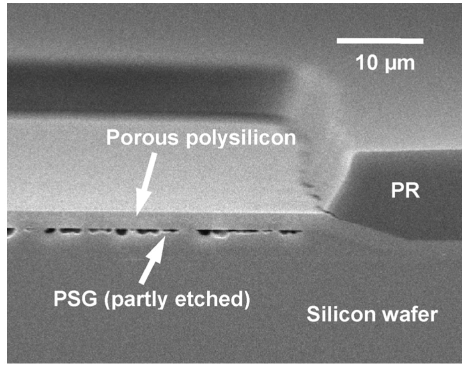
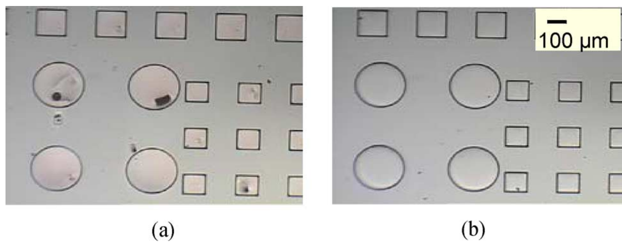


Fig. 7. Electrochemical etching successfully stopped at the interface of polysilicon and PSG, indicated by the porous polysilicon partly attached to the sacrificial PSG. Still partially attached to the substrate, the porous polysilicon can relieve the stress when annealed.



(a) (b)

Fig. 8. The effect of annealing on porous polysilicon. (a) Without annealing, cracks were observed in most of the released porous polysilicon membranes. (b) After 700 °C, 5 min RTA annealing in $\mathrm{N_2}$, membranes as large as 600 μm were obtained.

setup and thoroughly cleaned, the annealing was then performed in rapid thermal annealing (RTA) at 700 °C for 5 min in nitrogen. The effect of the annealing can be seen in Fig. 8 from the difference between the membranes fabricated without and with the annealing step. While porous polysilicon membranes up to only 100 μm in size survived without the annealing process, membranes as large as 600 μm were obtained without any crack after the annealing.

Because the HF-based electrochemical etching solution etches the PSG quickly after diffusing through the porous polysilicon, the window for annealing is quite small and an accurate timing is required to stop the etching. Although the process was successful for this report, which tested one die at a time, it may not be practical for an entire wafer under production conditions. Placing a barrier layer resistant to the electrolyte (e.g., silicon nitride) between the polysilicon and the sacrificial PSG layer or choosing an electrolyte that does not attack the sacrificial layer quickly may be a way to solve the problem.

B. Polysilicon Pirani Gauge Design

The vacuum level inside the cavity and the leak rate can be measured directly if a sensor is microfabricated and encapsulated in situ. One known way is to use a micromechanical resonator, based on the dynamics theory that the quality factor of a resonator is dependent on the air damping and thus the vacuum level [8], [17]. Recently, a micro Pirani gauge was used to characterize the vacuum level inside micro cavities [27]. Not only is the readout circuitry of a Pirani gauge much easier to build than that of resonators but also it can be fabricated by typical surface micromachining and conveniently represent free-standing microstructures that can be monolithically encapsulated.

The operating principle of the Pirani gauge is that the temperature-dependent resistance of the gauge is dependent on the ambient pressure, since a large part of the heat generated by Joule heating in the gauge is transferred through the air to the substrate (gaseous conduction) [28]. For a bridge Pirani gauge, the high and low detectable pressure limits of the linear pressure range it can detect, P_h and P_l, respectively, are given as follows:

$$P_h = \frac{2\eta k_g(\infty) T_s w}{\pi \alpha_E \overline{v} s d} \tag{1}$$

$$P_l = \alpha_E \left(\frac{k_b}{\eta k_g(\infty)} \right) \left(\frac{sz}{l^2} \right) P_h \tag{2}$$

where η is the excess-flux coefficient, which accounts for the fringing heat flux of the bridge element and can be obtained analytically, $k_g(\infty)$ is the thermal conductivity of the gas at atmosphere pressure, T_s is the substrate temperature, $\alpha_E(\leq 1)$ is the thermal-accommodation coefficient (typically O(1)), $\overline{v}$ is the average gas molecular velocity, d is the microbridge perimeter, and k_b is the thermal conductivity of the bridge material. s, w, z, and l are the distance above the substrate, width, thickness, and length of the microbridge, respectively. As the above equations indicate, the pressure detection range can be adjusted by changing the dimensions of the bridge as well as the gap between the bridge and the substrate. For the porous polysilicon encapsulation process to be demonstrated, serpentine polysilicon bridges with a width of 3 μm, length varying from 500 to 1000 μm, thickness of 1.5 μm, and gap of 1.5 μm from the substrate were designed.

C. Encapsulation of Pirani Gauge by Porous Polysilicon Shell: Fabrication Process

The fabrication process is illustrated in Fig. 9. The process started with a 5000 Å low-stress nitride deposition as the insulation layer, followed by an LPCVD deposition of 1.5 μm PSG, which was then patterned as the sacrificial layer between the Pirani bridge gauge and the substrate. Next, 1 μm in situ doped polysilicon was deposited by LPCVD and patterned to define the Pirani bridge structure [Fig. 9(a)]. A 5 μm PSG sacrificial layer was then formed by two LPCVD depositions. Each deposition was followed by a 1 h 1000 °C annealing in $\mathrm{N_2}$ to densify the PSG film. The thick PSG sacrificial layer is patterned and openings made through the nitride layer to the silicon substrate in order to allow for an electrical path between the polysilicon encapsulation layer and silicon substrate for electrochemical etching [Fig. 9(b)]. The 1.5 μm undoped LPCVD polysilicon was then deposited to form an encapsulation layer, followed by a 3000 Å LPCVD PSG deposition. This last polysilicon layer was also symmetrically doped to a resistivity of 0.02 $\Omega \cdot$ cm from the PSG layers on both sides by annealing at 1000 °C in $\mathrm{N_2}$ [Fig. 9(c)].

The top PSG layer was then stripped off in BOE, and all the insulating layers on the backside were removed by RIE. After the wafer was diced, each die was processed with a

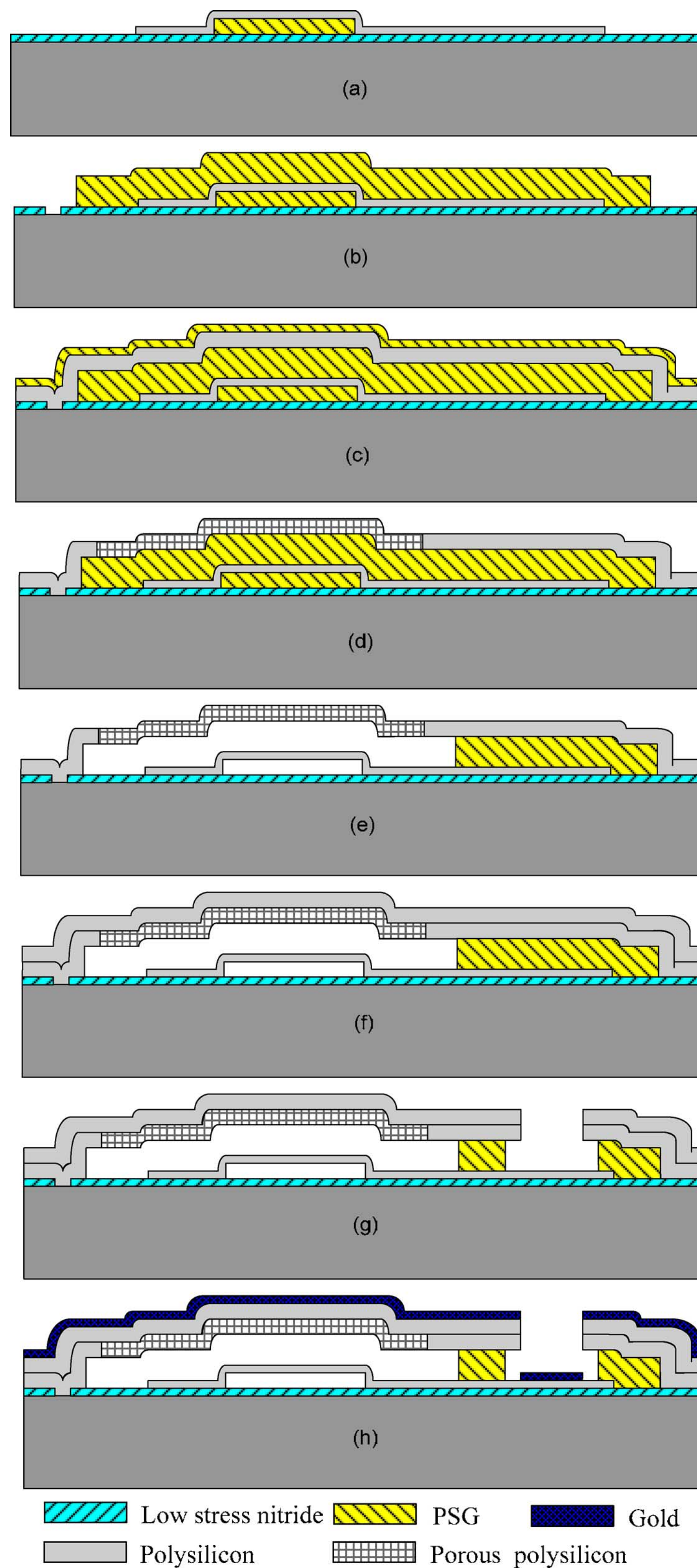


Fig. 9. Process flow for monolithic vacuum encapsulation of free-standing polysilicon Pirani gauge by postdeposition electrochemical etching of polysilicon. The thin films on the wafer backside are not shown.

NR9–8000 negative photoresist to define the area to turn the top polysilicon porous. Then the die was mounted in the Teflon cell for the electrochemical etching. After stopping the electrochemical etching at the interface of the polysilicon and the PSG using the method described in Fig. 7, the sample was taken out and cleaned in Piranha [Fig. 9(d)]. Next, a short RTA annealing (700 °C for 5 min) was performed to release the stress generated during the electrochemical etching. Then, the PSG sacrificial

TABLE I
MUMPs THIN-FILM LAYERS [31]

Material layer	Thickness (μm)
Nitride	0.6
Poly 0	0.5
First Oxide	2.0
Poly 1	2.0
Second Oxide	0.75
Poly 2	1.5
Metal	0.5

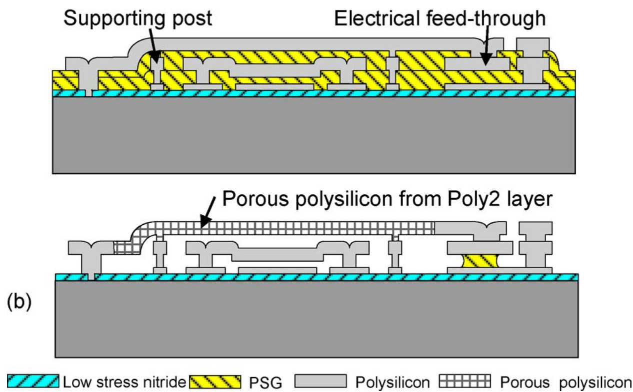


Fig. 10. Process flow of integration with MUMPs. (a) As received after polysilicon MUMPs. (b) After postprocess to release bridge structures.

layers were removed by concentrated 49% HF, which diffused through the nanopores in the 1.5-μm-thick porous polysilicon [Fig. 9(e)]. The release time was ∼1 min regardless of the size of the cavity. On the electrical feedthrough line, the remaining PSG was used to isolate it from the conductive polysilicon shell. The device was designed so that enough PSG is left by time-controlled etching.

The sample was then thoroughly rinsed in deionized water and methanol, followed by a supercritical CO_2 dry. Next, the device was sealed by depositing a polysilicon layer of different thicknesses (0.1–2.0 μm) in LPCVD with deposition pressure at 179 mTorr and deposition temperature at 600 °C. After sealing, the electrical contact pads were opened outside the cavity by etching away polysilicon in RIE and the exposed PSG in BOE [Fig. 9(f)]. A blank 100/1000 Å Ti/Au evaporation on the exposed polysilicon feedthrough lines, necessary for wire bonding, completed the fabrication process [Fig. 9(g)].

D. Integration With the MUMPs (Multiuser MEMS Processes) Process

To demonstrate the usefulness of this technique for common surface micromachining processes, the multiuser MEMS processes (MUMPs), a popular commercial foundry service that provides cost-effective and proof-of-concept MEMS fabrication, has been selected to fabricate a microbridge device encapsulated by the porous polysilicon shell. One of the standard processes in the MUMPs program is polyMUMPs, a three-layer polysilicon surface micromachining process, whose thickness data are listed in Table I. Illustrated in Fig. 10 is the schematic view of the encapsulation process. Poly0 and Poly1 layers were used to construct the microbridge resonator inside the Poly2 shell. Supporting posts were designed to reinforce the polysilicon shell of large size. The sacrificial oxide was used to isolate the polysilicon shell from the electrical feedthrough. The postprocess on the MUMPs chip started in-house with the removal of all the layers on the backside by RIE, a step necessary to create the electrical contact to the Poly2 layer through the substrate for electrochemical etching. Using photoresist as a mask, part of the Poly2 encapsulation layer was turned porous by electrochemical etching. The structure was then released in 1 min in concentrated 49% HF, followed by rinsing and supercritical CO_2 drying. Although the second oxide layer is only 0.75 μm thick, and therefore, unfortunately, does not provide enough space between Poly1 and Poly2 to accommodate the deflection of the encapsulation shell caused by pressure difference after the vacuum sealing step, the proposed encapsulation technique is still considered as commercially viable in a shared process.

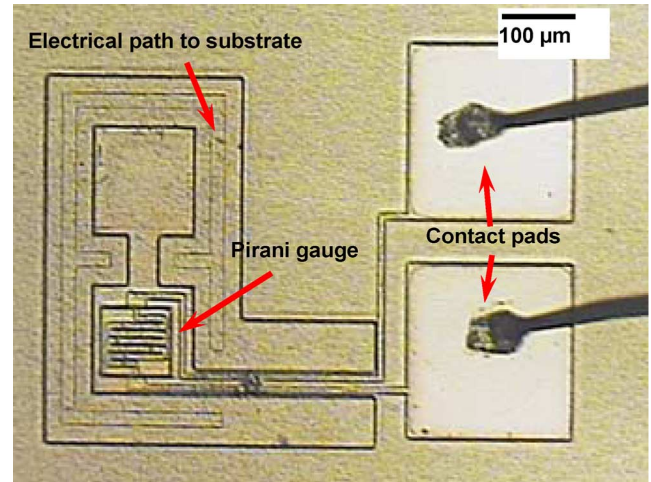


Fig. 11. An optical microscope picture of a packaged device, which has two cavities connected to each other. The Pirani gauge was encapsulated in the bottom cavity. Two Au wires were bonded to the Au contact pads.

III. RESULTS AND DISCUSSIONS

A. Encapsulation of Pirani Gauge by Porous Polysilicon Shell

Fig. 11 is an optical microscopic top view of a completed device, showing two square cavities connected to each other: one with a bridge Pirani gauge and the other empty. Although the encapsulating membrane is opaque, the gauge and feedthrough lines are noticeable by the transferred topography. Shown as the ring pattern around the cavity patterns is the electrical path connecting polysilicon to the substrate for electrochemical etching. Shown in Fig. 12(a) is a tilt SEM view of the device intentionally clipped to expose the free-standing Pirani gauge. In a cross-section view of Fig. 12(b), the serpentine Pirani gauge structure is clearly seen suspended above the substrate by approximately 1 μm. The encapsulation shell, composed of solid polysilicon sealing layer on the porous polysilicon layer, is magnified in Fig. 12(c). The porous and solid regions of the bottom polysilicon layer, defined by the photoresist mask in the electrochemical etching, are distinguishable in Fig. 12(d). Pore size

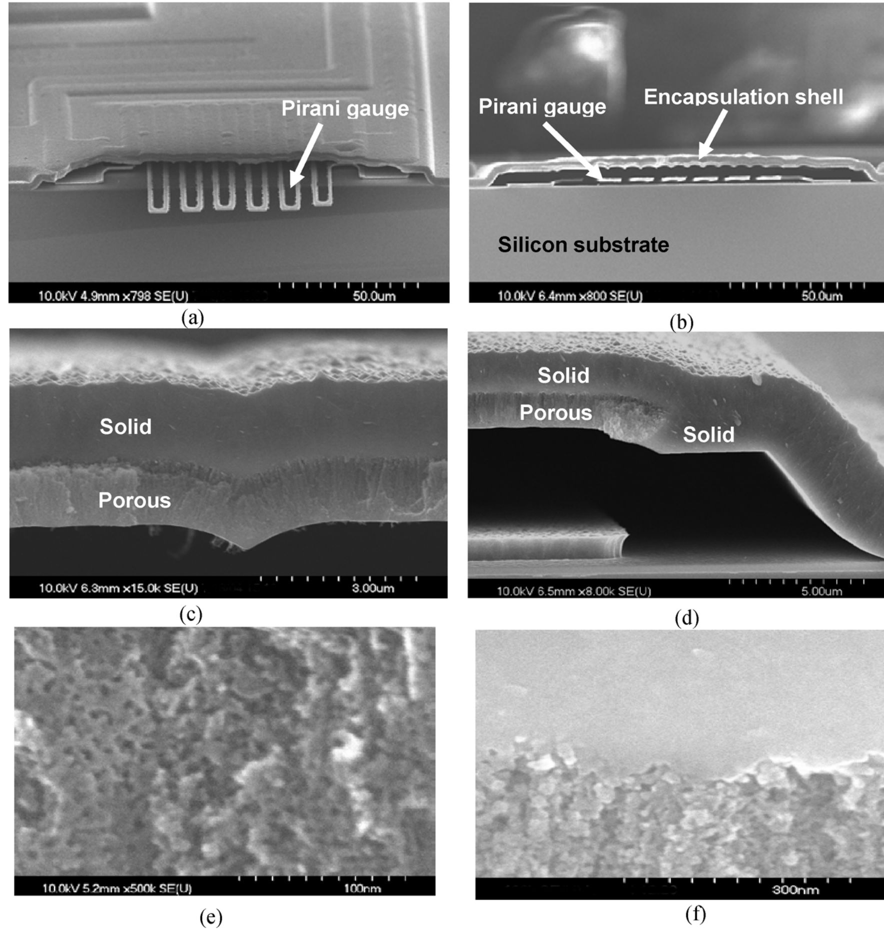


Fig. 12. SEM pictures of a polysilicon Pirani gauge encapsulated by porous polysilicon shell and sealed. (a) The encapsulation shell was intentionally clipped to expose the Pirani gauge inside the cavity. (b) The bridge gauge is seen free inside the cavity, suspended above the substrate and free from the shell as well. (c) Closeup picture of the shell layer shows both the porous polysilicon layer and the solid sealing layer on top. (d) Closeup of the edge shows the porous area and the solid area in the polysilicon layer, defined by photoresist mask during electrochemical etching. (e) High magnification SEM cross-section picture of the pore structure. (f) SEM cross-section picture at the interface between the sealing polysilicon and the porous polysilicon. The transition appears abrupt, which suggests no penetration of polysilicon into the nanopores.

of the porous polysilicon is estimated to be around 5 nm from Fig. 12(e).

The pressure inside the sealed cavity was measured from the encapsulated Pirani gauge. The thermal impedance of a Pirani gauge was first obtained while vacuum encapsulated. The thermal impedance is defined as [27]

$$T.I. = \frac{\Delta T_{\text{avg}}}{\Delta P_E} = \frac{1}{\xi \cdot R_0} \cdot \frac{\Delta R_b}{\Delta P_E},$$

where P_E is the electrical power, T_{avg} the average temperature across the Pirani gauge, ξ the temperature coefficient of resistance (1000 ppm/°C for polysilicon), and R_b and R_0 are the resistances of the microbridge at a given pressure and ambient pressure, respectively. Without affecting the performance of the Pirani gauge encapsulated in the bottom cavity, the seal on the top empty cavity was broken intentionally with a probe tip. The sample was then placed in a pressure-controlling chamber, where the gauge is calibrated against known pressures. It is noteworthy that the encapsulation shell is the other heat sink of the Pirani gauge besides of the silicon substrate, and its deflection, which changes the air gap between the Pirani gauge and the encapsulation shell, is dependent on the pressure of the environment. While the encapsulation shell of a vacuum-sealed Pirani gauge was deflected by approximately 1 μm when tested

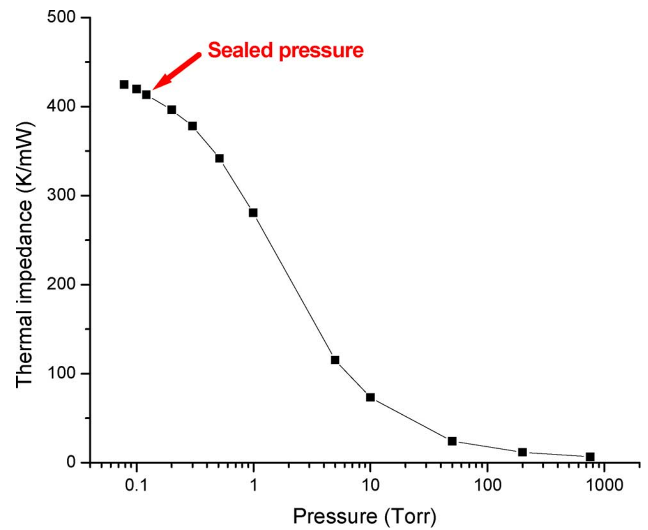


Fig. 13. Thermal impedance of a Pirani gauge at different pressure. The marked point is the thermal impedance of the sealed Pirani gauge.

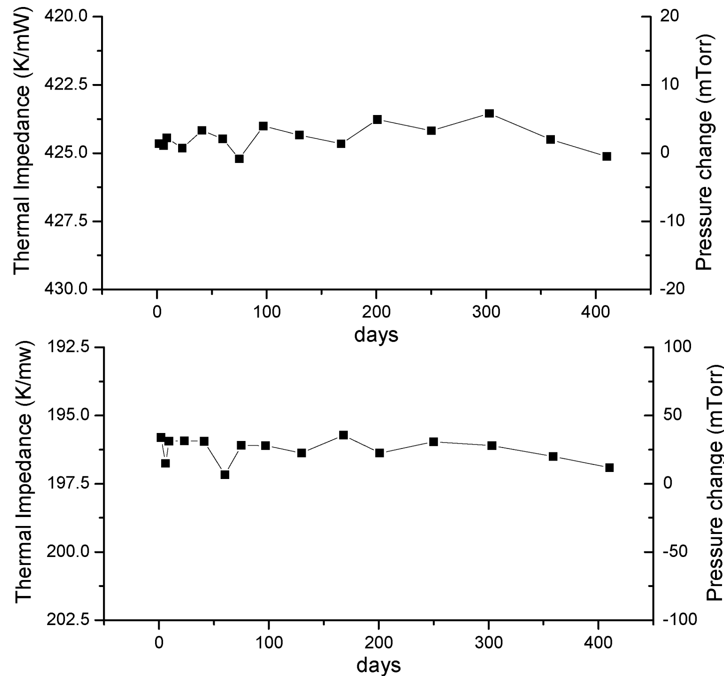


Fig. 14. Leak rate of two sealed cavities, each encapsulating a Pirani gauge of different design. The corresponding pressure change on the right axis was obtained from such a calibration as shown in Fig. 13.

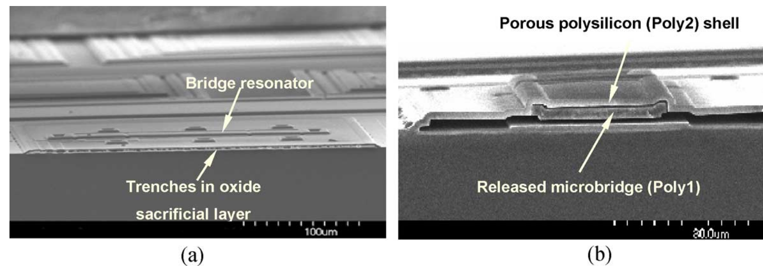
in atmosphere, no pressure difference was present on it during the calibration process as the seal was intentionally ruptured. To obtain a more accurate estimation of the sealed pressure, the sealed Pirani gauge was placed in a vacuum environment, where the deflection of the encapsulation shell is negligible, and its thermal impedance was measured to be 7.3 K/mW higher than that measured at atmosphere, which translates to a pressure difference of approximately 30 mTorr. By matching the thermal impedance of the Pirani gauge while sealed with the calibration data obtained in the pressure-controlling chamber, the pressure inside the sealed cavity was extracted to be around 130 mTorr (Fig. 13). The residual gas inside the cavity could be H_2 byproduct during the polysilicon deposition or from the outgassing of the remaining PSG plug in the feedthrough channel.

The long-term hermeticity was monitored by reading the thermal impedance change of the Pirani gauges over time. The thermal impedance changes of two sealed Pirani gauges with different gauge dimensions over one year are shown in Fig. 14. The result shows no noticeable pressure change (<30 mTorr) for a long period of time (>1 y).

The advantages of using thick nanoporous encapsulation shell for sealing—quick sealing and elimination of the diffusion of the sealing material into the cavity—were confirmed from the fabrication process and the completed devices. Polysilicon of different thicknesses was deposited to seal the device with the porous polysilicon shell. The device was successfully vacuum-sealed by a polysilicon layer as thin as 1000 Å, far thinner than any other reports [5]–[14], [29]. The amount of the polysilicon sealing material, which may have passed through the porous polysilicon shell and landed on the surfaces inside the cavity, was measured on the silicon nitride thin film on the silicon wafer. After breaking the seal and removing the encapsulation shell by a probe tip, the measurement was performed by Nanospec AFT with a measurement range down to 80 Å; the result was read "under range." In a separate test, a porous polysilicon cavity was fabricated on a bare silicon substrate and was then sealed by a 2 μm silicon oxide in LPCVD. The oxide thickness on top of the silicon surface inside the cavity, measured from the thin oxide program of Nanospec AFT with a measurement limit of 20 Å, was "under range." Adding to the arguments is the evidence of the void pores at the interface of the sealing layer and the porous polysilicon layer shown in Fig. 12(f). Should the sealing polysilicon have entered the cavity, those nanopores would have been filled with the polysilicon, Or, for the sealing polysilicon to have a chance to pass through, the transition from plugged pores to open pores would have been somewhat gradual at this scale. A more precise direct measurement, such as X-ray photoelectron spectroscopy and Auger electron spectroscopy [30], may be used, if necessary.

B. Integration With the MUMPs Process

Shown in Fig. 15(a) is an angled view of a device after post-MUMPs electrochemical etching. The device has been cleaved to reveal the cross-section details. The trenches in the oxide top imply HF in the electrochemical etching solution started to etch the sacrificial oxide layer through the pores, confirming the pore formation was complete through the Poly2 layer. The SEM picture in Fig. 15(b) shows the bridge was successfully released without any presence of stiction after the completion of the encapsulation process. The porous Poly2 layer has not been deposited with a sealing material because of the small gap (only 0.75 μm, defined by second oxide) between the main structural polysilicon layer (Poly1) and the encapsulating polysilicon shell (Poly2).



(a) (b)

Fig. 15. Monolithic encapsulation of a microbridge on a MUMPs chip. (a) Right after electrochemical porous etching of Poly2. (b) After the removal of the sacrificial oxide and supercritical CO_2 dry.

IV. Conclusion

Formed porous by electrochemical etching "after" deposition, the structural porous polysilicon thin film was demonstrated to be an effective encapsulation layer for monolithic on-wafer encapsulation of MEMS devices. A surface-micromachined process to fabricate the free-standing porous polysilicon structure has been developed. With no need for etching holes defined by lithography on the shell, the sacrificial PSG was removed through the nanopores in the porous polysilicon encapsulation layer quickly (in 1 min), and the nanopores were sealed by depositing a polysilicon layer as thin as 1000 Å. No sealing material was found on the inside surfaces of the cavity. A polysilicon Pirani gauge, representing a typical polysilicon surface-micromachined device, was successfully encapsulated and sealed in a vacuum. The pressure inside the sealed cavity, as in situ measured from the Pirani gauge, was around 130 mTorr and showed no noticeable change over 1 y. Integration of this novel on-wafer encapsulation technique with the common MUMPs process was also demonstrated.

Acknowledgment

The authors highly appreciate help from F. Chamran with the electrochemical etching and discussions with Prof. B. Dunn and M. C. Wu.

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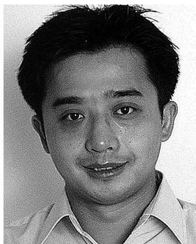

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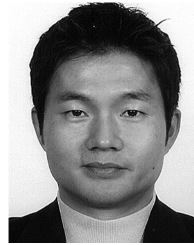

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