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***Abstract*—Recent activity in research surrounding electric vehicle propulsion has indicated that modular or segmented drives show promise for meeting the demanding performance and scalability targets set forth in industry road maps. Additionally, unconventional topologies, such as the flying capacitor multilevel topology (FCML), have demonstrated high-efficiency and high-specific-power—as well as reduction in output current distortion, dv/dt and filter size. This work highlights the technical challenges and performance benefits arising in the implementation of a segmented drive from an array of independent FCML inverter modules. Harmonic content in the ac phase legs and dc bus currents is analyzed and experimentally measured. Furthermore, a hierarchical control strategy with specific emphasis on the synchronization of both the carrier and fundamental across multiple modules is demonstrated. The work concludes with a demonstration of the paralleled, interleaved and multi-phase operation of a multi-module array, with conducted emissions measured on a CISPR-25 pre-compliance test fixture.**

I. INTRODUCTION

Aggressive technology roadmaps [1], [2] established by industry and government consortiums have indicated the need for high-efficiency, high-power-density drivetrains to facilitate next-generation electric vehicles. Recent work suggests that a segmented or modular approach may produce a more robust and scalable three-phase drive through the interconnection of individual inverter modules [3], [4]. Therefore, this digest explores the design of a multi-phase inverter array using modules based on the high-performance flying-capacitor multilevel (FCML) architecture. While single-phase experimental demonstrations have shown exceptional performance [5], and ample literature has been published on the design [6], startup [7] and operation [8] of the converter (and thus largely omitted here), multi-module, multi-phase operation represents a significant step forward for the technology. Further interleaving these modules will also reduce the harmonic spectra at the converter terminals, reducing filtering requirements necessary to meet vehicle electromagnetic compliance (EMC) standards.

The paper thus proceeds as follows: First, Section II illustrates a hierarchical control interface to coordinate between inverter modules so that multi-phase operation can be demonstrated in the ensemble. Next, interleaving of modules paralleled within a given line phase is proposed—with implementation strategy discussed in Section II-C, followed by analysis of corresponding input and output current spectra in Section III. Then, Section IV discusses some potential implications of unequal current sharing between interleaved phases. Finally, Section V presents experimental results validating the approach, measured on a CISPR-25 pre-compliance test fixture. Finally, Section VI provides concluding remarks.

II. HIERARCHICAL CONTROL

A drive based on a modular design scales output power through paralleling inverter modules. This increases the overall device count, and therefore gate signals, in the full converter—regardless of phase-leg topology chosen. For multilevel topologies, which feature numerous switches for even a single-phase (e.g., the 10-level FCML in Fig. 1), this gate signal count would be even higher: driving a 3-phase array of P-paralleled modules of N-level FCML inverters from a single microcontroller would require routing $3 \cdot P \cdot (N-1) \cdot 2$ high-frequency signals with low-latency in what is typically a high-noise environment. To address this signaling challenge, control tasks can be divided between a global array controller and local controllers across the individual inverter modules.

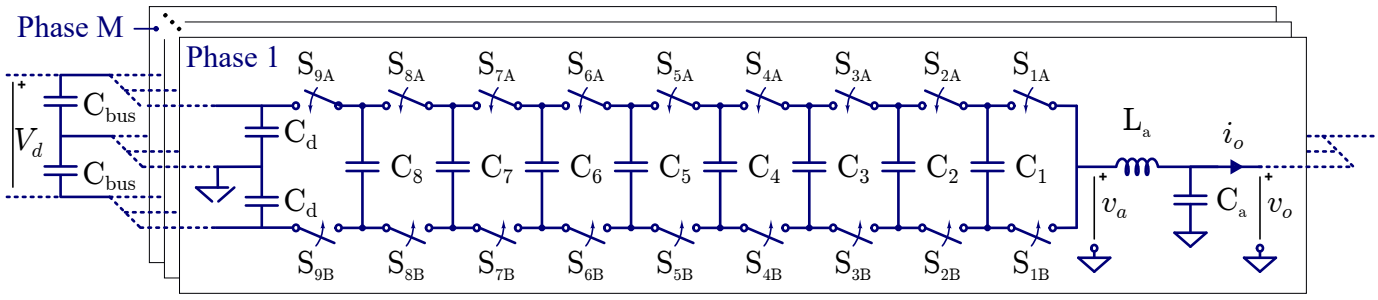


Fig. 1: Schematic representation of how M interleaved 10-level FCML inveters can be interleaved within a phase-leg.

A. Global & Local Control Domains

For pulse-width modulation (PWM), gate signal generation represents a relatively low-level task. This is especially the case with phase-shift PWM (PSPWM), where the carriers remain invariant under normal operation. As such, the carrier generation, as well as the comparison to an input reference, can be performed locally and independently on each inverter module. However, the input reference depends on states outside of the individual inverter domain (e.g., motor angle, speed reference, direct and quadrature currents, etc.), and must be computed at the system level. These two tasks serve to represent the local and global domains of the proposed hierarchical control structure for the segmented drive of this work, with the concept fully illustrated in Fig. 2.

B. Control & Measurement Scheme

In the scheme of Fig. 2, the local controller is responsible for generating switching signals and collecting output voltage and current measurements—which are both used locally for fast-acting fault mitigation and sent upstream to the global controller via a serial communication link. In turn, the global controller can receive the output current and voltage measurements from each inverter module and, in aggregate with any exogenous inputs, can send a corresponding closed-loop reference back down the communication link to each local controller. While an industry standard protocol may be able to provide this link [9], to simplify development a proprietary protocol comprised of 64 bit Manchester-encoded frames was implemented over a point-to-point optical link in this work. This also serves to defer any signal integrity challenges that may arise from electromagnetic interference (EMI) coupling into an electrical communication link (e.g., RS-485), with the temporary trade-off of higher cost and assembly effort.

Note that while the AFBR-59F2Z transceivers used can support up to 250 Mbit/s, the data-rate was limited to 6.25 Mbit/s to allow future tests using slower interfaces—meaning that the system update rate is just under 100 kHz. With this configuration, the multi-phase drive waveform at the fundamental can still be generated at the global level and distributed to local controllers digitally. However, any interleaving of inverters at the switching frequency requires a more nuanced strategy.

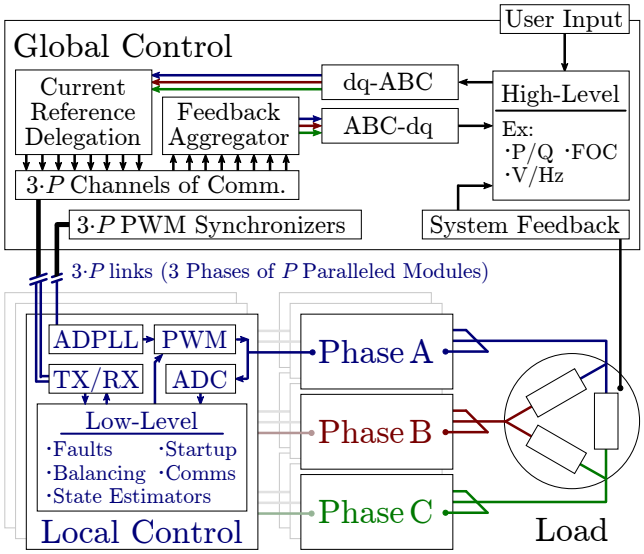


Fig. 2: High-level illustration of the hierarchical control structure, configured here to drive a three-phase load.

C. Carrier Synchronization

Interleaving of inverter modules provides an attractive method of reducing switching harmonics at the input (predominantly at the switching frequency, f_{sw}) or the converter output (predominantly at the effective output frequency, $f_{\mathrm{eff}} = (N-1) \cdot f_{\mathrm{sw}}$), lessening the impact of passive filters on power density. However, interleaving requires the modules to share a common frequency and phase reference around f_{sw}.

One common synchronization method utilizes a digital pulse to reset local PWM counters to a nominal value (associated with the requisite phase-shift) each switching period. Such a scheme is often employed to synchronize counters across PWM peripherals within a single microcontroller [10], and is indeed implemented within the local controller of this work for PSPWM generation. It is also possible to choose a source external to the microcontroller (via a configurable input pin) to synchronize PWM counters with an external system. Such a scenario is illustrated in Fig. 3, where the rollover of a global (signed) counter triggers a sync pulse that correspondingly resets the local (signed) counter used in PWM generation.

Here, when the two counters are initially unsynchronized at ①, the synchronization input at ② can lead to a gate signal of arbitrary pulse width on multiple devices instantaneously. In a system with a common clock source incrementing each PWM counter, or where the various global and local clock frequencies deviate only slightly, this may be the only abrupt correction that occurs. For example, if system clocks on both the local and global controllers are operating at 200 MHz and derived from 50 ppm oscillators, at most a single digital count of error may accumulate over counter periods used for kHz-range and above switching. Then, the system would maintain glitch free synchronism shown at ④. However, if there were significant frequency variation in system clocks, or if an (e.g., EMI-inducted) glitch occurred on the sync line, shown at ⑤, similar distortions of the switching waveform at ⑥ may continue to occur.

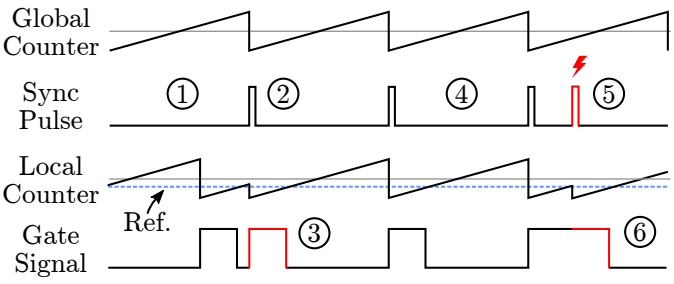


Fig. 3: Illustration of a time-base synchronization scheme common in microcontroller PWM peripherals.

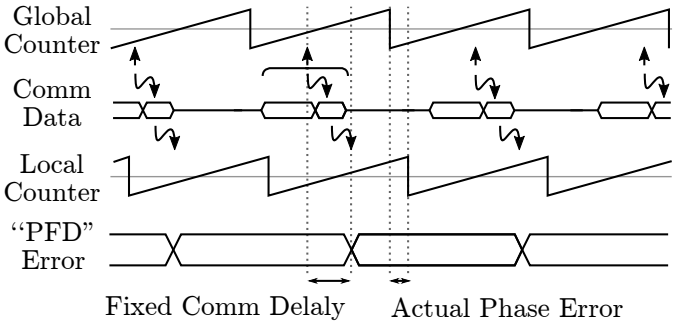


Fig. 4: Illustration of a synchronization scheme using a communication link and ADPLL.

To address these concerns, additional filtering or windowed-detection schemes could be employed on the synchronization line. However, this work instead employs an all-digital phase-locked loop (ADPLL) to provide both inherent filtering (via the loop filter), as well as more gradual correction mechanism that varies the counter increment value rather than abruptly reset the counter as described above. If the global reference is provided over a dedicated synchronization line, as shown in Fig. 2, implementation of the phase-frequency detector (PFD) is relatively straightforward [11] while design and analysis can be adapted from [12]. Note that if the system clocks only differ slightly, as described above, applying an integer number of extra (or omitted) increments to the local counter each switching period to speed up (or slow) the counter will overcorrect. As such, a fractional PLL [13] was implemented. This way, the discrete corrections can be spread over several switching periods to provide greater average frequency precision at the price of negligible instantaneous phase jitter.

While this implementation was verified in initial tests, the routing of these additional sync signals in tandem with the existing communication line—as well as ensuring their signal integrity at high-power operation—represented an additional barrier towards scalability. Therefore, the modified system shown in Fig. 4 was developed for further testing. Here, the global controller samples its counter value and appends the signed value to each communication packet. When the local controller receives each packet, the error between local counter value and that in the packet is directly calculated. This proposed solution nonetheless worked well for experiments in this work, with results detailed in Section V. Note that in either implementation of ADPLL, a delay will be introduced when transmitting the counter reference from the global controller to each local controller. However, this delay is common to each converter, with any differential delay limited to the nanoseconds of jitter or propagation delay across individual communication modules. As such, the differential phase between local controller PWM time bases is dominated by the phase induced from interleaving.

III. Multi-Module Harmonic Content Analysis

The benefits of multi-phase power, including the reduction of input current ripple at the *fundamental* and cancellation of *line frequency* harmonics at the output, are generally well understood and available in the literature. Therefore, this section focuses on reducing harmonics of the *switching frequency* in the input and output currents through the synchronization and interleaving of modules as previously discussed.

Prior work has shown that a PWM process can be described through the use of a double Fourier series [14]. Indeed, the Fourier coefficients and switching functions necessary to study the PSPWM operation of an FCML inverter can be readily found in [15]–[17]. As such, only a slight modification to these works is necessary to accommodate for interleaved operation. Essentially, to model a converter x where $x \in [0, P-1]$ in a group of P interleaved N-level FCML inverters, a phase shift term of $\frac{mx2\pi}{P}$, where m is a given carrier harmonic, is added to the switching function angles defined in [16], [17]:

$$\gamma_m = \frac{2m(N-2)\pi}{N-1} + \frac{mx2\pi}{P} \tag{1}$$

$$\theta_{k,m} = \frac{m(2k-1)\pi}{N-1} + \frac{pi}{2} + \frac{mx2\pi}{P} \tag{2}$$

The models described in [16], [17] then can be used* to provide harmonic content for the FCML output current given nominal DC bus and flying capacitor voltages. Then, summing across the resulting complex spectra for interleaved converter $0, 1, ..., P-1$ yields the output current harmonics of a given interleaved phase-leg. The resulting spectra for a single 10-level FCML inverter ($P = 1$), as well as the dual- ($P = 2$) and triple-interleaved ($P = 3$) cases, are shown in Fig. 5, with harmonic currents normalized to the total magnitude of the fundamental. Spectra shown are for the inductor current to emphasize harmonic cancellation; the load typically sees very little high-order switching harmonics.

Note that for PSPWM, where the effective output frequency is an integer multiple of the switching frequency (which is seen at the input), P and $N-1$ must be co-prime to simultaneously interleave the input and output. Otherwise, the phase shift that interleaves the input will wrap the phase at the output. This is illustrated with the unit circles representing the switching period in Fig. 5. The arrows show the phase of each interleaved converter, while the green ticks indicate the $N-1$ full cycles of the output frequency each switching period. The middle two spectra show interleaving at the output, as reflected in each subsequent cancellation of effective switching frequency harmonic. However, with $P = 3$, this cannot occur at the phase shift required for interleaving the input (indicated with gray arrows). The last plot shows that the phase shift corresponding to interleaving the inputs for $P = 3$ leads to no reduction in load current harmonics. Section V will also show that a similar case arises when $P = 6$ and $N = 10$, though repeated dual-interleaving at the output is possible.

To calculate the input current, the switching function for the DC side switch (i.e., S_{N-1}), containing the additional phase shift term, must be convolved with an expression for the

*Note, these models assume a double-edge PWM modulator, while this work employed a trailing-edge modulator. However, the Fourier coefficients describing the trailing-edge switching function are readily available in [14].

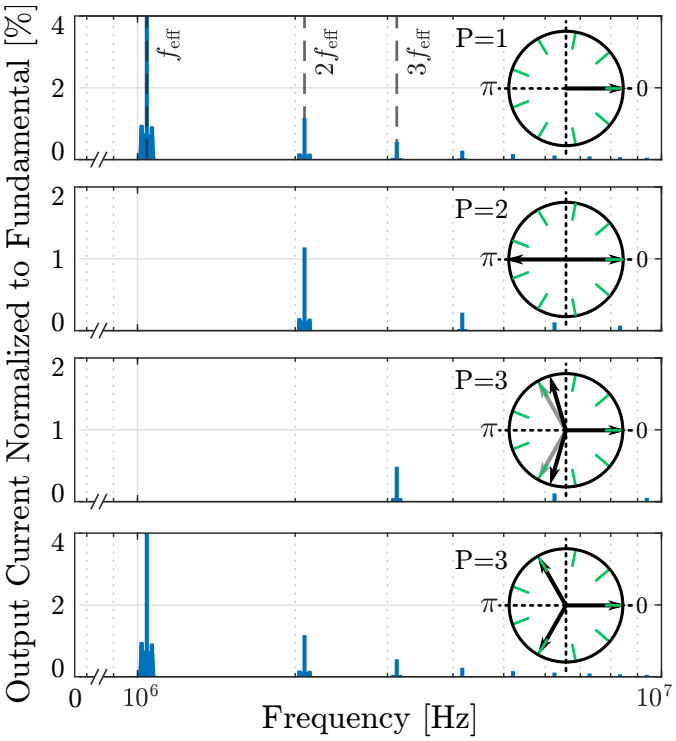


Fig. 5: Calculated output current spectra in the region of interest (i.e., harmonics of f_{eff} for $N = 10$. The unit circles are normalized to the switching period, where arrows indicate the phase shift of interleaved modules. Green ticks mark each full cycle at the effective output frequency per switching period.

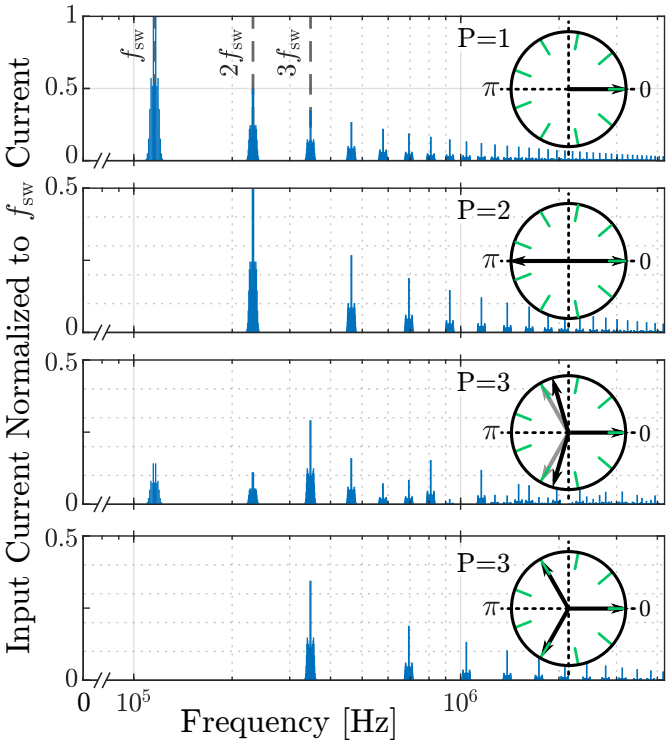


Fig. 6: Calculated input current spectra in the region of interest (i.e., harmonics of f_{sw}) for $N = 10$.

output current. Given the sinusoidal output of the converters under study [5], this convolution can be simplified when the output current is assumed to be sinusoidal at the fundamental frequency [18]. Then, summing across the resulting spectra for interleaved converters $0, 1, ..., P-1$ yields the input current harmonics of a given phase-leg, as shown in Fig. 6. Note that an appropriate choice of phase shift that interleaves the output can still significantly reduce input harmonics for $P = 3$.

The calculated input current spectra for a three-phase, segmented drive comprised of an array that is 6-fold interleaved in such a way is shown in Fig. 7. The simulated conducted EMI in dBμV was derived by applying the transfer function for the line impedance stabilization network (LISN) used in Section V to the calculated input current harmonic amplitudes for a specified output current. Additionally, for comparison, the input current for a single 6-fold interleaved phase-leg, as well as that for a single, constituent FCML converter, are also plotted. Here, the single converter is shown to contain a broad spectrum of switching harmonics. However, as expected from

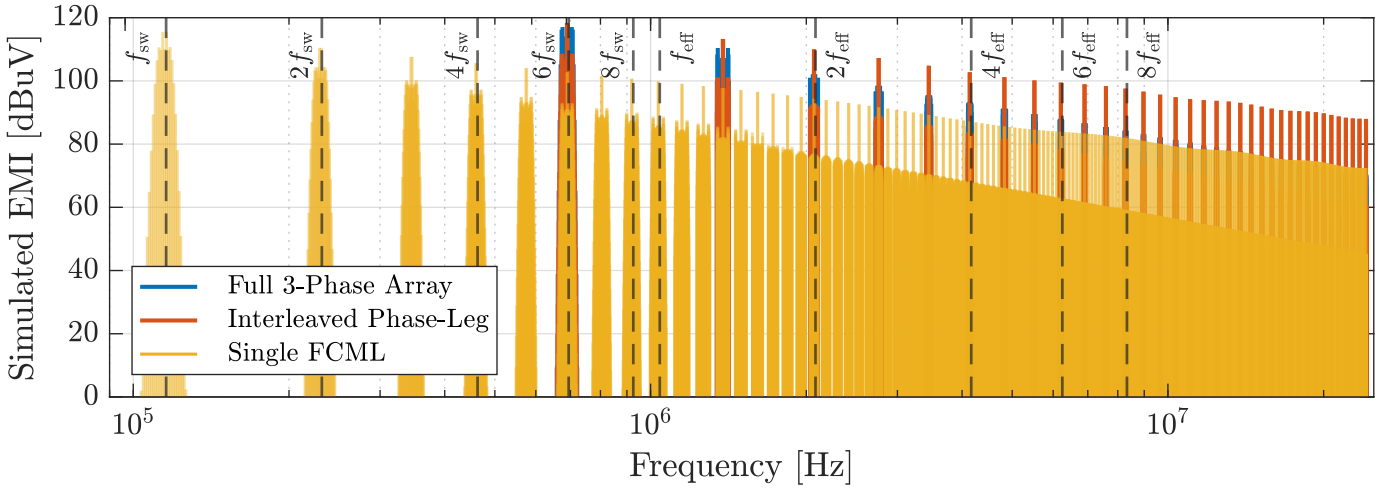


Fig. 7: Calculated input current harmonic content using double Fourier analysis and assuming sinusoidal output current.

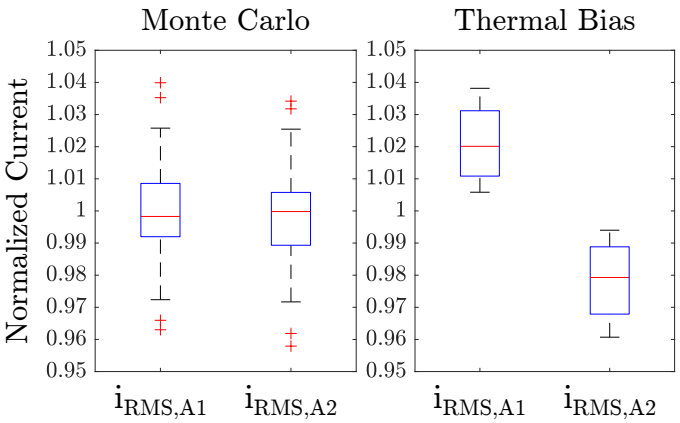


Fig. 8: Statistical results of simulations recording current sharing imbalance between phases of a dual-interleaved converter module given parameter variation.

the Fourier analysis, all but the $6m$ harmonics cancel in the interleaved phase-leg. Finally, although the full three-phase array spectra has greater peak magnitudes due to the higher total power output, it contains fewer harmonics in due to the cancellation of triplen sidebands—though this detail is not visible in the figure owing to the range of frequencies plotted.

IV. Current Sharing & Parameter Sensitivity

While control loops on the local or global controller may be employed to enforce current sharing, the open-loop behavior provides a worst-case scenario to analyze. This work examines two sources of open-loop imbalance in a dual-interleaved, 10-level FCML arising from parameter variation: component tolerances and bias consistent across an entire interleaved phase (e.g., from unequal cooling). The first case was examined through a Monte Carlo simulation, with component values treated as random variables parameterized around a nominal value using the manufacturer part tolerances. Fig. 8 shows the variation of *interleaved* phase current, normalized to that of non-interleaved FCML converter under commensurate load. Results of 100 simulations indicated that that current mismatch of only a few percent is likely to occur. The second case was examined by simulating a 5% to 25% reduction in mass flow of cooling air to one of the phases, with component resistances adjusted accordingly. Again, deviations from the nominal current stayed below 5%. In both cases, increased loss in one phase is largely offset by reduced loss in the other.

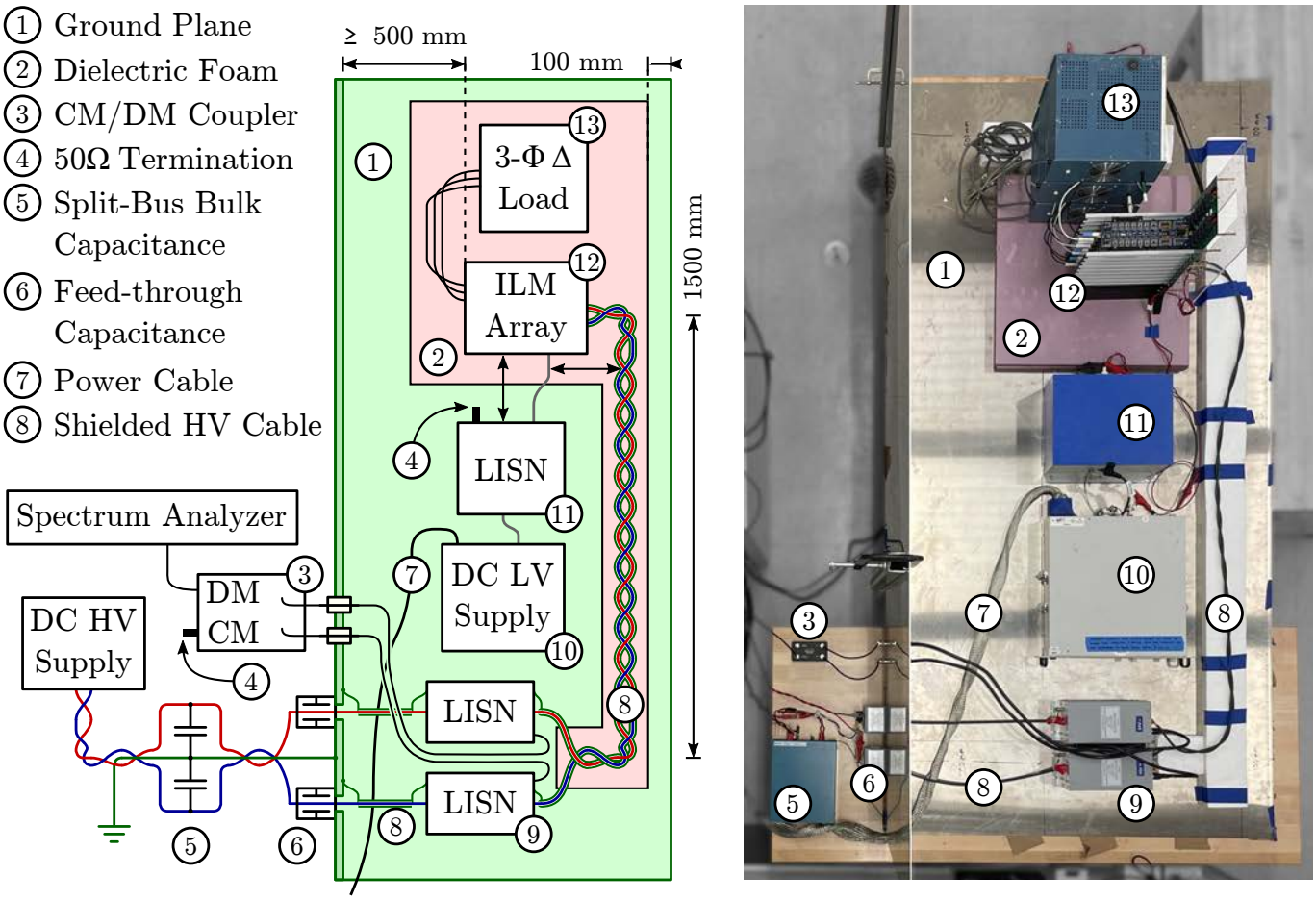


Fig. 9: Electromagnetic compatibility pre-compliance experimental setup for measuring CISPR-25 conducted emissions.

V. Experimental Results

To address the target application of electric vehicle drive-trains, the test setup of Fig. 9 was constructed to evaluate the interleaving strategy as applied to conducted emissions defined in the CISPR-25 standard. The two high-voltage (400 V to 1 kV) LISNs are 5 μH 21702-5-TS-50-N from Solar Electronics Company, and the low-voltage (5 V) LISN is a 50 μH LIN-115A from Com-Power Corporation. While the low-voltage (LV) interconnection and any associated filtering will influence overall EMC performance, this work focused solely on conducted emissions observed at the high-voltage (HV) connection. Additionally, a TBLM1 LISN Mate from Tekbox was used to separate emissions measurements at this node into common-mode (CM) and differential-mode (DM) to inform future filter design efforts.

Here, the device under test is a three-phase, segmented drive comprised of nine arrayed, dual-interleaved modules (ILMs), as shown in Fig. 10. This configuration corresponds to six paralleled ($P = 6$), 10-level ($N = 10$) FCML inverters per phase-leg, or 18 arrayed converters in total. Correspondingly, each inverter is labeled by phase and converter number: A1…A6, B1…B6, C1…C6. A full description of the individual inverter module hardware is available in [5], with the most recent performance metrics using EPC2034C devices and improved module cooling reported in Table I. Each converter module synchronizes phase-shifted fundamental and switching frequencies via optical communications from a global controller [19] (not shown) using the scheme from Section II-C.

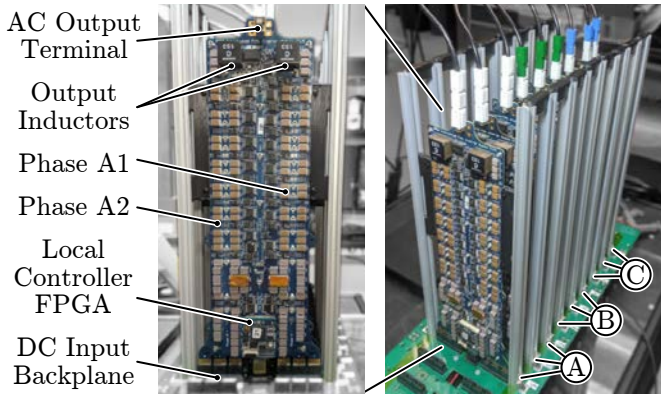


Fig. 10: Hardware photographs for the dual-interleaved module (ILM, on left) and three-phase, 18 converter array (right).

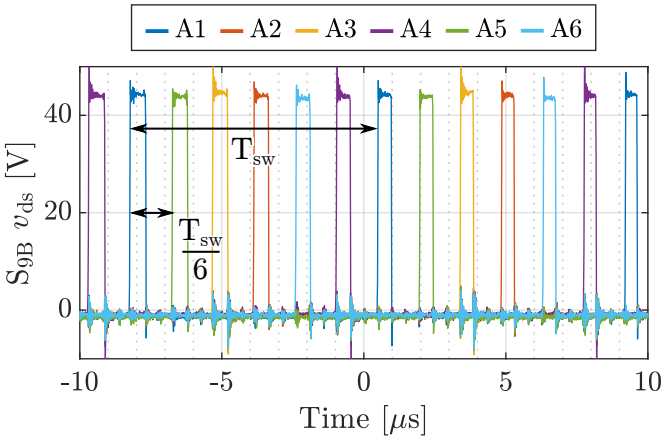
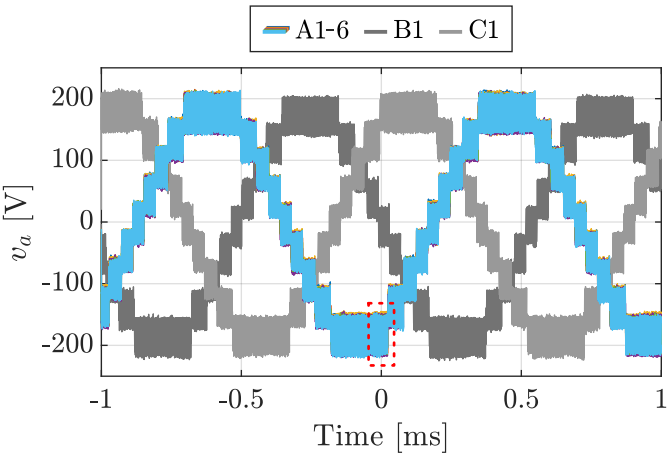
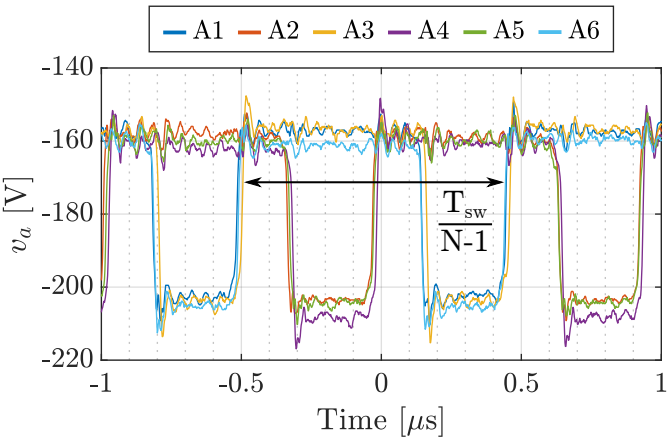


Fig. 11: Six v_{ds} waveforms of the S_{9B} low-side switches (closest to the DC bus) measured for the converters of Phase A illustrate that 6-fold interleaving is achieved at the input.

The inverter was supplied with a 400 V DC bus and commanded to drive a 950 Hz fundamental at 95% modulation into a 25 Ω balanced, delta load. This frequency serves as a convenient test case corresponding to high-electrical-frequency machines while also remaining in a high-accuracy regime for the WT5000 meter used to record DC-AC efficiency. Measurements of the drain-source voltages of the low-side switches closest to the dc bus (S_{9B} in Fig. 1) were used to

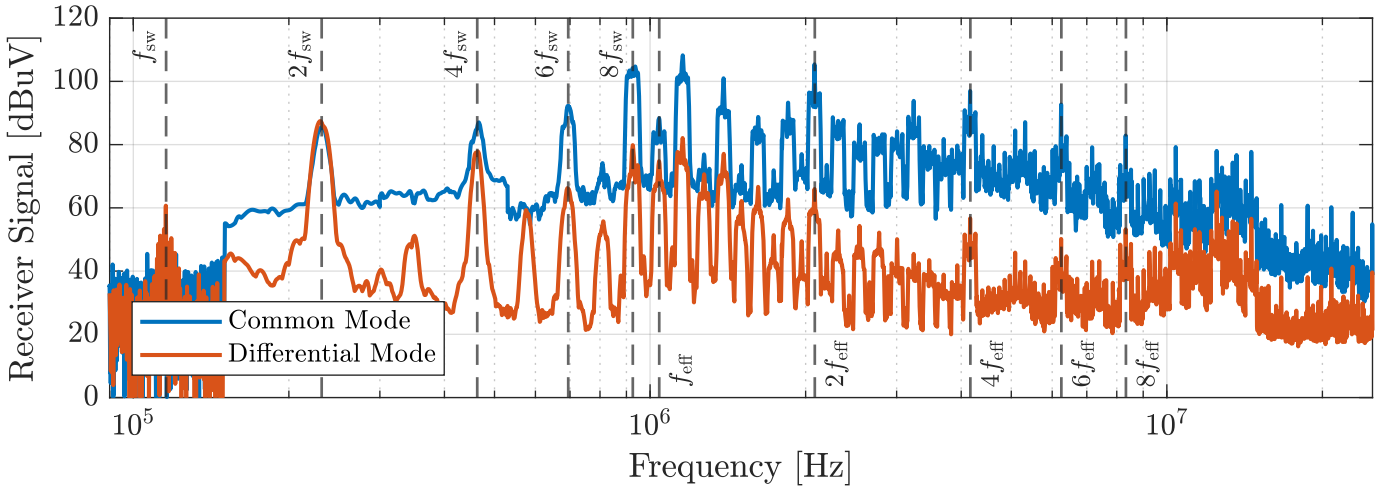


(a) Switch node (v_a) waveforms for eight of the individual converter legs: all six interleaved modules within Phase A, as well as one measurement each from Phase B and from Phase C for reference.

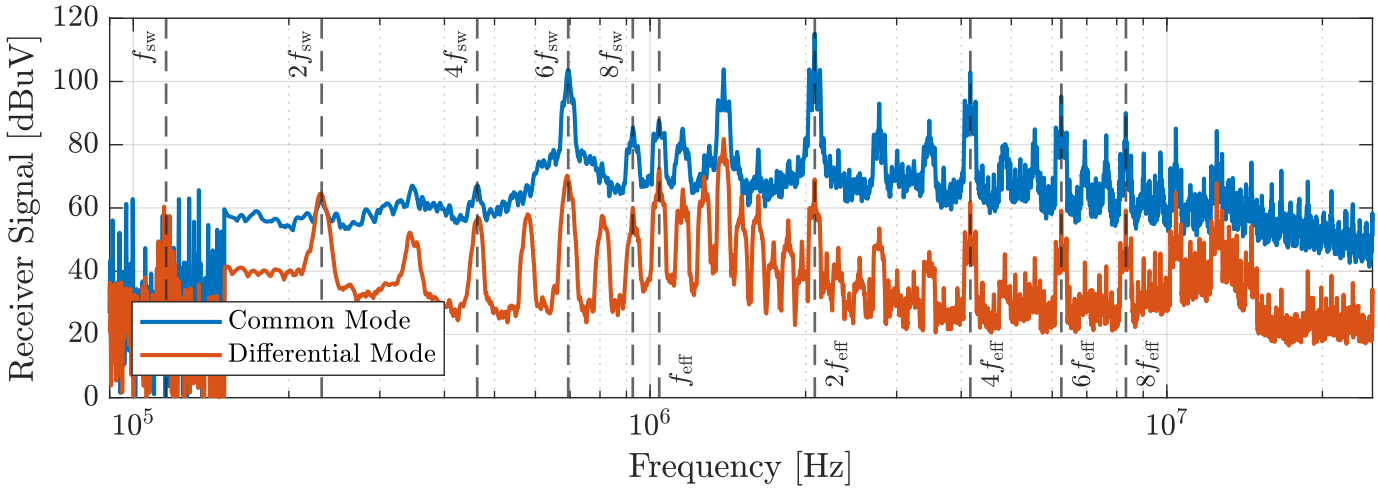


(b) Zoomed view from the highlighted region above. The two sets of three overlapping waveforms indicate that only dual-interleaving is achieved at the output in this configuration.

Fig. 12: Experimental waveforms at 400 V DC and 6 kW output power for the 3-phase array comprised of nine dual-interleaved FCML modules (16 arrayed converters).



(a) Measured conducted emissions with no synchronization across arrayed, dual-interleaved modules.



(b) Measured conducted emissions with 6-fold interleaving at the input and associated synchronization of dual-interleaved module outputs.

Fig. 13: Common-mode and differential-mode conducted emissions measurements of the three-phase segmented drive operating at a 400 V DC bus and 6 kW output power, measured at the HV terminals of the test setup.

validate correct interleaving at the input. Fig. 11 shows these measured waveforms for the six converters within Phase A with the correct phase shift of $\pi/3$. Additional measurements also confirmed the correct phase shift of $2\pi/3$ between the array phase-legs. Further measurements at the switch node (v_a in Fig. 1) verified both three-phase operation, shown in Fig. 12a, as well as repeated dual-interleaving at the output, shown in Fig. 12b. This confirms the limitations imposed by the choice of P and $N-1$ described in Section III.

As the array assembly in this test setup was designed to facilitate ease of access to electrical nodes for debugging, both thermal and emissions performance were limited in this work; Future packaging improvements are expected to facilitate the full 100 kW output power target, while integration of shielding and filters will support better EMC. Nonetheless, the conducted EMI measurements for this configuration in Fig. 13 will still inform design of such filters, and highlights the benefits of interleaving. For instance, without interleaving between modules, Fig. 13a shows that significant harmonic content is present at many of the harmonics of the switching frequency. Note that, given each module is still dual-interleaved locally, content at odd harmonics is nonetheless reduced or eliminated compared to the spectra of the single FCML converter in Fig. 7. This is expected from the analysis of the dual-interleaved case in Fig. 6.

TABLE I: Inverter module experimental performance.

Parameter	Value
Rated DC Bus Voltage	1 kV
Effective Output Frequency	1.035 MHz
Peak Efficiency	98.95 %
Peak Output Power	18.9 kW
Gravimetric Power Density	38.4 kW/kg
Volumetric Power Density	24.4 kW/kg

With 6-fold interleaving enabled across the arrayed modules, Fig. 13b shows that most non-$6m$ harmonics can be either eliminated or otherwise reduced by approximately 20 dBuV. As expected, the amplitude of the $6m$ harmonics increases slightly as the interleaving effectively shifts energy into these frequencies. The content at $2f_{\text{eff}}$ is particularly elevated as this is both a $6m$ harmonic of f_{sw}, and the repeated dual-interleaving at the output concentrates energy in this spectrum. Note that, for this converter setup, interleaving more significantly attenuates CM harmonics compared to DM harmonics. This is possibly due to the use of a split-bus DC supply.

VI. Concluding Remarks

This work reported progress on a 100 kW-scale segmented drive comprised of nine arrayed, dual-interleaved, 18.9 kW FCML inverter modules. These modules were commanded and synchronized using a hierarchical control and communication scheme to demonstrate the benefits of interleaving across independent inverter modules. Experimental results were collected on a CISPR-25 pre-compliance test fixture, with CM and DM spectral performance obtained across several bus voltage and output power operating points. Future work should consider the inherent restrictions on interleaving at both the input and output of the array when evaluating choice of levels and number of paralleled modules for the full system design.

VII. Acknowledgment

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References

[1] US Drive Electrical and Electronics Technical Team, "Electrical and Electronics Technical Team Roadmap," tech. rep., U.S. DRIVE (Driving Research and Innovation for Vehicle efficiency and Energy sustainability), October 2017.

[2] C. L. Bowman, J. L. Felder, and T. V. Marien, "Turbo- and Hybrid-Electrified Aircraft Propulsion Concepts for Commercial Transport," in *2018 AIAA/IEEE Electric Aircraft Technologies Symposium (EATS)*, pp. 1–8, July 2018.

[3] A. Shea and T. M. Jahns, "Hardware integration for an integrated modular motor drive including distributed control," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 4881–4887, 2014.

[4] E. Gurpinar and B. Ozpineci, "Loss Analysis and Mapping of a SiC MOSFET Based Segmented Two-Level Three-Phase Inverter for EV Traction Systems," in *2018 IEEE Transportation Electrification Conference and Expo (ITEC)*, pp. 1046–1053, June 2018.

[5] N. Pallo, S. Coday, J. Schaadt, P. Assem, and R. C. N. Pilawa-Podgurski, "A 10-Level Flying Capacitor Multi-Level Dual-Interleaved Power Module for Scalable and Power-Dense Electric Drives," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2020.

[6] T. Modeer, C. B. Barth, N. Pallo, W. H. Chung, T. Foulkes, and R. C. N. Pilawa-Podgurski, "Design of a GaN-based, 9-level flying capacitor multilevel inverter with low inductance layout," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, pp. 2582–2589, March 2017.

[7] P. Papamanolis, D. Neumayr, and J. W. Kolar, "Behavior of the flying capacitor converter under critical operating conditions," in *2017 IEEE 26th International Symposium on Industrial Electronics (ISIE)*, pp. 628–635, June 2017.

[8] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *PESC '92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*, pp. 397–403 vol.1, June 1992.

[9] F. Savi, G. Buticchi, C. Gerada, P. Wheeler, and D. Barater, "Information technologies for distributed machine drives: An overview," in *2019 IEEE International Electric Machines Drives Conference (IEMDC)*, pp. 1805–1809, 2019.

[10] Texas Instruments, "Enhanced Pulse Width Modulator (ePWM) Module," in *TMS320x2833x,TMS320x2823x Technical Reference Manual*, Literature Number SPRUI07, Sept. 2019.

[11] R. E. Best, "Mixed-Signal PLL Building Blocks," in *Phase-locked Loops: Design, Simulation, and Applications*, McGraw-Hill professional engineering, McGraw-Hill, 2007.

[12] V. Kratyuk, P. K. Hanumolu, U. Moon, and K. Mayaram, "A design procedure for all-digital phase-locked loops based on a charge-pump phase-locked-loop analogy," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 3, pp. 247–251, 2007.

[13] C. Barrett, "Fractional/Integer-N PLL Basics," Tech. Rep. SWRA029, Texas Instruments, 1999.

[14] D. Holmes and T. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. IEEE Press Series on Power Engineering, Wiley, 2003.

[15] R. H. Wilkinson, T. A. Meynard, and H. du Toit Mouton, "Natural Balance of Multicell Converters: The Two-Cell Case," *IEEE Transactions on Power Electronics*, vol. 21, pp. 1649–1657, Nov 2006.

[16] B. P. McGrath and D. G. Holmes, "Analytical modelling of voltage balance dynamics for a flying capacitor multilevel converter," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 543–550, 2008.

[17] B. P. McGrath and D. G. Holmes, "Analytical determination of the capacitor voltage balancing dynamics for three-phase flying capacitor converters," *IEEE Transactions on Industry Applications*, vol. 45, no. 4, pp. 1425–1433, 2009.

[18] B. P. McGrath and D. G. Holmes, "A general analytical method for calculating inverter dc-link current harmonics," *IEEE Transactions on Industry Applications*, vol. 45, no. 5, pp. 1851–1859, 2009.

[19] C. B. Barth, *High-density multilevel power converters for use in renewable and transportation applications*. Ph.d. dissertation, University of Illinois at Urbana-Champaign, Urbana, IL, Dec. 2019.