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A Comprehensive Loss Model and Comparison of AC and DC Boost Converters

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Abstract: DC microgrids have become a prevalent topic in research in part due to the expected superior efficiency of DC/DC converters compared to their AC/DC counterparts. Although numerous side-by-side analyses have quantified the efficiency benefits of DC power distribution, these studies all modeled converter loss based on product data that varied in component quality and operating voltage. To establish a fair efficiency comparison, this work derives a formulaic loss model of a DC/DC and an AC/DC PFC boost converter. These converters are modeled with identical components and an equivalent input and output voltage. Simulated designs with real components show AC/DC boost converters between 100 W to 500 W having up to 2.5 times more loss than DC/DC boost converters. Although boost converters represent a fraction of electronics in buildings, these loss models can eventually work toward establishing a comprehensive model-based full-building analysis.

Keywords: DC power transmission, Power converter, AC-DC power conversion, DC-DC power conversion, Losses

1. Introduction and Motivation

1.1. AC and DC Converters

DC microgrids have become a hot topic in research with the spread of internally-DC loads, solar generation, and battery storage. The total system efficiency is expected to improve from eliminating conversions between AC and DC. Previous works have compared the losses in AC and DC microgrids [1–8]. In typical commercial buildings, the modeled savings with DC varied from 2% [1] to as much as 19% [8], depending on the modeled converter efficiency and the respective voltage levels. Gerber et al. [3] conducted a side-by-side AC and DC building simulation with a parametric sweep of solar and storage capacity. The simulation showed that AC buildings suffer the most loss from low-power AC/DC converters [3]. For example, AC/DC LED drivers can achieve up to 94% efficiency, whereas DC/DC LED drivers are typically at least 98% [4].

These previous works all had a major shortcoming: the converter loss models were limited to efficiency curves or peak efficiencies from product datasheets. Product data varies considerably with component quality and manufacturer. An accurate study would require a substantial number of efficiency curves to establish typical operating efficiencies for each class of device. DC products are far less common than AC, and reliable efficiency data is even more rare. In addition, these works compare AC and DC systems that have different network voltages (e.g. comparing 120 V_{rms} AC to 380 V DC). Since converters are generally more efficient at higher voltage [3], it is unclear whether DC systems are inherently more efficient or are simply analyzed at a higher voltage.

This work is part of an effort to improve upon past full-building efficiency studies. It aims to replace modeled or simulated efficiency curves with a rigorous math-based converter loss model. In particular, this paper extends [9] to develop a formulaic model that can theoretically compare the efficiency and losses in equivalent AC (AC/DC PFC) and DC (DC/DC) boost converters. Such a normalized comparison can improve previous system-level studies and help to quantify the energy benefits of DC. While boost converters only account for a fraction of power converters in a building, this work presents a modeling method that can be extended to compare other types of converters, ultimately allowing a full-building loss analysis. This loss model is entirely equation-based and easy for engineers to apply in other types of academic and industrial projects.

1.2. Boost Converters

DC boost converters step-up the input DC voltage to a higher output DC voltage. AC boost converters, shown in Figure 1, step-up the input sinusoid and ensure unity power factor through a power factor correction (PFC) controller. Today's standards mandate PFC in most loads [10], and as such, AC boost converters are now present in many loads including EV charging, HVAC, heat-pump water heating, refrigeration, and data centers. This work models losses in the following components: the input inductor (L), the switch (Q), the boost diode (D), and the output capacitor (C). The AC boost converter has an additional loss component, the diode bridge (B). The model assumes a converter with (a) continuous conduction mode operation, (b) an input current that is in-phase with the input voltage, and (c) no voltage ripple at the output. This work develops two boost converter models: the simple model, and the model with ripple. The latter accounts for ripple current at the input, making it more accurate but more complex.

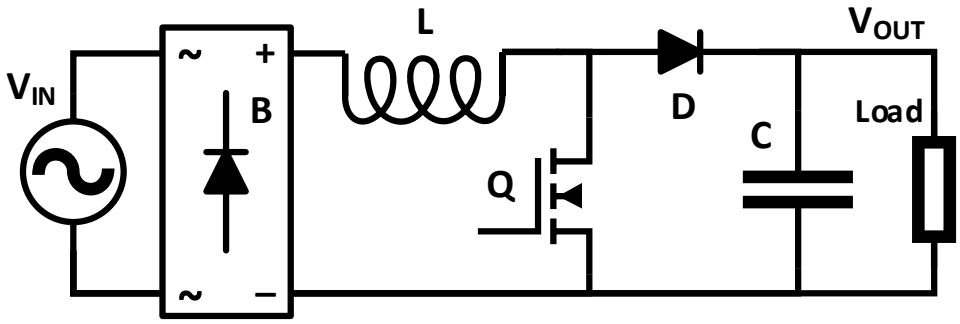

Figure 1. The modeled AC boost converter. The DC boost converter does not have a diode bridge (B).

Previous work derive loss models for DC [11–14] and AC PFC [15–23] boost converters. However, none of these models establish the necessary analytic framework for a side-by-side AC to DC comparison. Many previous works use a basic model for switching loss and neglect loss in the input diode bridge and output capacitor. This is the first work to develop a formulaic loss comparison between converters with identical components and an equivalent input and output voltage. These models calculate a complete loss analysis from the input voltage, output voltage, output power, and parasitic values easily found in component datasheets. DC converters have generally been known to be more efficient, but this work quantifies the exact difference in loss.

There are two main forms of loss in a converter: conduction loss and switching loss. Conduction loss models are derived in Sections 2 and 3 and switching loss models are derived in Sections 4 and 5.

Core loss is not modeled; it can be significant in some types of converters, but is negligable for continuous conduction boost converters with relatively small ripple [23–26]. Finally, Section 6 describes the model validation through simulation and experiment, and Section 7 shows how the model can be used to calculate the loss in AC and DC boost converters. For a quick reference to all the loss model formulae, see Appendices .1 to .4.

2. Deriving Conduction Loss Models

Conduction loss occurs when the components conduct current, and mostly impacts the converter efficiency at high power. When the switch turns on, the inductor is charged by a current path through the bridge, inductor, and switch, shown in Figure 1. When the switch turns off, the inductor discharges through the bridge, inductor, and boost diode. The output capacitor acts as a filter for the output power to the load.

For each component X, this work calculates the average conduction loss, $P_{X,cond}$, by solving for the component's RMS and average current. For the inductor ($I_{L,rms}$), switch ($I_{Q,rms}$), and capacitor ($I_{C,rms}$), the average resistive loss is

$$P_{X,cond} = R_X I_{X,rms}^2, \tag{1}$$

with R_L as the inductor copper resistance, R_Q as the switch on-state resistance, and R_C as the capacitor ESR. The average diode loss of the boost diode ($I_{D,rms}$, $I_{D,avg}$) and bridge diodes ($I_{B,rms}$, $I_{B,avg}$) is modeled as a constant forward-biased diode drop V_X and a linearized series resistance R_X:

$$P_{X,cond} = V_X I_{X,avg} + R_X I_{X,rms}^2. \tag{2}$$

Sections 2 and 3 derive the model for each $P_{X,cond}$, and the resulting formulae are organized in Appendix .2.

Each $I_{X,rms}$ and $I_{X,avg}$ can be calculated with an integration of the component's current waveform. For the AC boost converter in Figure 2, these currents are functions of the low-frequency AC angle, θ, and the high-frequency switching period T. At the switching time scale, θ is approximately constant as shown in Figure 3. Thus the model presents an independent two-stage integration, first of the instantaneous current, $i(\theta, t)$, from $t = 0$ to T, and then of the switching-period-RMS, $i_{rms,t}(\theta)$, from $\theta = 0$ to π. The total RMS current through component X is

$$i_{X,rms,t}(\theta) = \sqrt{\frac{1}{T}\int_0^T i_X^2(\theta, t)dt} \tag{3}$$

$$I_{X,rms} = \sqrt{\frac{1}{\pi}\int_0^\pi i_{X,rms,t}^2(\theta)d\theta}. \tag{4}$$

For the DC boost converter, $\theta = 0$ is constant, thus $I_{X,rms} = i_{X,rms,t}(\theta)$.

As shown in Figure 3, the component currents appear as triangles at the switching timescale, and the geometric methods shown in Figure 4 can be employed to integrate over the switching period, T. The currents for the inductor and bridge diode appear as a zero-centered bilateral triangle, Δ^B, whose average and RMS are:

$$\Delta^B_{avg,t} = 0 \tag{5}$$

$$\Delta^B_{rms,t}(A) = \frac{A}{2\sqrt{3}}, \tag{6}$$

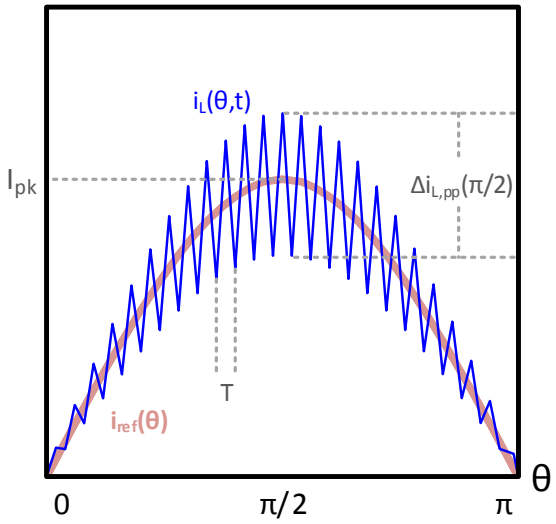

Figure 2. The inductor current $i_L(\theta, t)$ tracks a reference input current $I_{ref}(\theta) = I_{pk}sin(\theta)$.

where the triangle's peak-to-peak height, A, is shown in Figure 4. For the elevated right triangle, Δ^R,

$$\Delta^R_{avg,t}(B, D) = BD \tag{7}$$

$$\Delta^R_{rms,t}(A, B, D) = \frac{\sqrt{D}}{2\sqrt{3}}\sqrt{A^2 + 12B^2}, \tag{8}$$

where A is the triangular section's height, B is the elevation of the triangle's midpoint, and D is the fraction of time that the component is active. All of the component currents are derived from either Δ^B or Δ^R. For the simple model, inductor-current ripple is ignored, thus $A = 0$.

Finally, some RMS calculations can be simplified by leveraging the orthogonality of waveforms. If $i_1(t)$ is orthogonal to $i_2(t)$ and $i(t) = i_1(t) + i_2(t)$, then

$$I_{rms} = \sqrt{I^2_{rms,1} + I^2_{rms,2}}. \tag{9}$$

3. Conduction Loss Component Currents

3.1. Input and Duty Cycle

This research establishes a comparison between AC and DC boost converters subject to an equivalent power and voltage level. Both converters are modeled with an identical constant output power P_o and output voltage V_o. The AC and DC input voltage and current is respectively

$$v_{i,AC}(\theta) = V_{pk}sin(\theta) \tag{10}$$

$$i_{ref,AC}(\theta) = I_{pk}sin(\theta) = \frac{2P_o}{V_{pk}}sin(\theta) \tag{11}$$

$$v_{i,DC} = V_{pk} \tag{12}$$

$$i_{ref,DC} = \frac{P_o}{V_{pk}}. \tag{13}$$

The comparison considers the peak AC input, V_{pk}, as an appropriate equivalent DC input since most application-relevant specifications relate to V_{pk} (e.g. switch stress, breakdown voltage, safety, insulation).

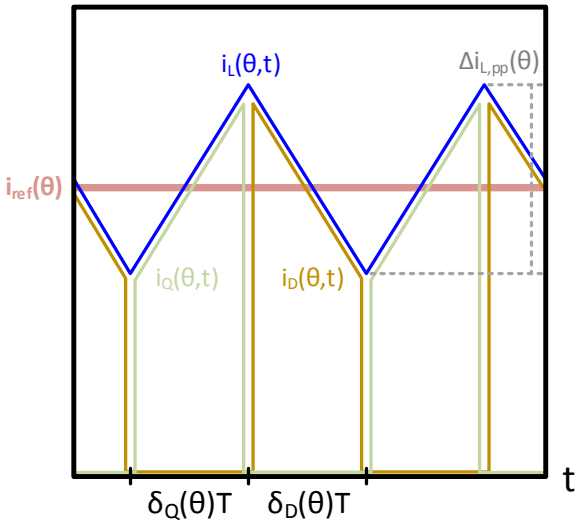

Figure 3. On the switching timescale, θ is approximately constant. The inductor current, $i_L(\theta, t)$, passes through the switch (green) during $\delta_Q(\theta)$, and the boost diode (orange) during $\delta_D(\theta)$.

For the DC converter, v_i and i_{ref} are constant and do not depend on θ. For the purpose of deriving component currents, the loss model assumes $P_{in} = P_o$ (i.e. 100% efficiency), which yields simple but accurate formulae for most boost converters [15,16].

The switching duty cycle for the switch, δ_Q, and the boost diode, δ_D, can be separately expressed as:

$$\delta_Q(\theta) = 1 - \frac{v_i(\theta)}{V_o} \tag{14}$$

$$\delta_D(\theta) = \frac{v_i(\theta)}{V_o}, \tag{15}$$

and are useful in calculating (5)–(8).

The following subsections explain the calculations of the RMS and average of each component current. Final expressions for the simple model are shown in Table A1. Final expressions for the model with ripple are shown in Tables A2 and A3.

3.2. Inductor Current

–*Simple Model*: When ripple is ignored, $i_L = i_{ref}$, and $i_{L,rms}$ is calculated as the RMS of the sinusoidal i_{ref}.

–*Model with Ripple*: Inductor ripple is geometrically represented as a bilateral triangle. On the switching timescale, the peak-to-peak inductor current ripple is

$$\Delta i_{L,pp}(\theta) = \frac{v_i(\theta)\delta_Q(\theta)}{fL}. \tag{16}$$

The RMS of $\Delta i_{L,pp}(\theta)$ is solved from (4) and (6) as

$$\Delta i_{L,rms,t}(\theta) = \Delta^B_{rms}\left(A = \Delta i_{L,pp}(\theta)\right) \tag{17}$$

$$\Delta I_{L,rms} = \sqrt{\frac{1}{\pi}\int_0^\pi i^2_{L,rms,t}(\theta)d\theta}. \tag{18}$$

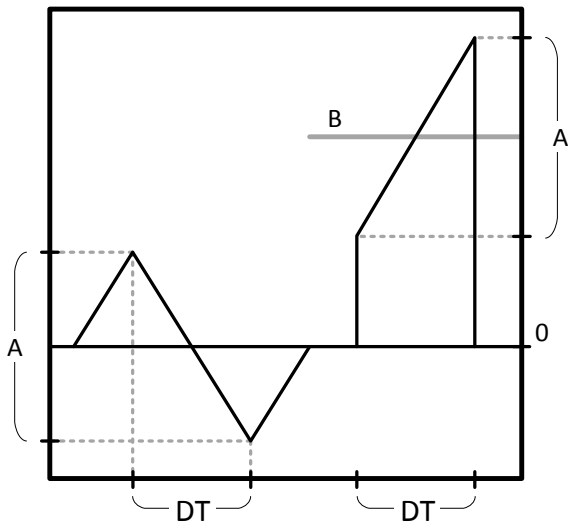

Figure 4. On the switching timescale, a bilateral triangle, Δ^B, (left) can model the current through the inductor and bridge diode. This triangle is not necessarily isosceles. An elevated right triangle, Δ^R, (right) can model the current through the switch and boost diode.

Figure 2 clearly shows the total inductor current, $i_L(\theta, t)$, to be the sum of $i_{ref}(\theta)$ and $\Delta i_L(\theta, t)$. Given (14) and (16), these waveforms are orthogonal, and can be combined through (9) as:

$$I_{L,rms} = \sqrt{I_{ref,rms}^2 + \Delta I_{L,rms}^2}. \tag{19}$$

3.3. Diode Bridge Current

–*Simple Model*: The inductor and diode bridge are in series, thus $i_B(\theta, t) = i_L(\theta, t)$ and $I_{B,rms} = I_{L,rms}$. $I_{B,avg}$ is calculated as the average of the sinusoidal $i_{ref}(\theta)$.

–*Model with Ripple*: A bilateral triangle has an average of zero regardless of the ripple. Thus $I_{B,avg}$ is the average of $i_{ref}(\theta)$.

3.4. Switch Current

–*Simple Model*: During $\delta_Q(\theta)$, the inductor current flows through the switch. Both the simple and ripple models integrate $\Delta^R_{rms,t}$. For the simple model,

$$I_{Q,rms,t}(\theta) = \Delta^R_{rms,t}(A = 0, B = i_{ref}(\theta), D = \delta_Q(\theta)). \tag{20}$$

–*Model with Ripple*: Evaluating (20) with $A = \Delta i_{L,pp}(\theta)$ accounts for inductor current ripple.

3.5. Boost Diode Current

Both boost diode models can leverage the analysis in Section 3.4 with $D = \delta_D(\theta)$ to solve the RMS current. The average current is indifferent to inductor current ripple, and is calculated from $\Delta^R_{avg,t}$.

3.6. Capacitor Current

The boost diode current is split between the capacitor and load, i.e. $i_D(\theta,t) = i_C(\theta,t) + \frac{P_o}{V_o}$. In both models, these orthogonal currents combine via (9) as,

$$I_{C,rms} = \sqrt{I_{D,rms}^2 - \left(\frac{P_o}{V_o}\right)^2}. \tag{21}$$

4. Switching Loss in the Switch (Q)

Switching loss most impacts a converter's low-load efficiency and occurs when the switch and diode toggle state between conducting and blocking. Instantaneous switching loss is determined on the switching time scale, and expressed as a function $P_{X,sw,yy}(\theta)$. For average switching loss:

$$P_{X,sw,yy} = \frac{1}{\pi}\int_0^\pi P_{X,sw,yy}(\theta)d\theta. \tag{22}$$

This section derives the switching loss models for hard switching, $P_{Q,sw,hs}$, and switch output capacitance, $P_{Q,sw,c}$. The resulting formulae are organized in Appendix .3. Although past works have rigorously characterized switching loss [27,28], their models rely on complex nonlinear equations and self-measured parasitics. This section presents a simple but accurate model based on parasitics easily found in datasheets.

4.1. Hard-Switching Loss

The switch has two states: blocking or conducting, with zero current or zero voltage, respectively. However, during a transition, the switch briefly experiences a simultaneous non-zero current, i_{DS}, and voltage drop, v_{DS}, across its drain-source terminals. The overlap of this non-zero voltage and current causes switching loss.

Figures 5 and 6 show the voltage and current waveforms for the boost converter, which is characterized by inductive switching as described in [29,30]. When the switch turns on, the i_{DS} must rise to its final value, $I_{DS,max}$, before v_{DS} can fall to zero. When it turns off, v_{DS} must rise to $V_{DS,max}$ before i_{DS} can fall. The overlap between i_{DS} and v_{DS} is the energy lost per cycle, which can be geometrically calculated. Although the overlap can be reduced by snubbing, this work models the worst-case hard-switched boost converter.

The loss calculation requires knowledge of the rise and fall times of the voltage and current: T_{VR}, T_{VF}, T_{IR}, and T_{IF}. These durations are heavily influenced by the gate drive, gate resistance R_G, and gate input capacitance C_{ISS}. The gate drive is modeled as a step function with amplitude $V_{GS,max}$. R_G includes both the internal device resistance and external drive resistance. C_{ISS} is defined by the gate-source (C_{GS}) and the gate-drain (C_{GD}) capacitances as:

$$C_{ISS} = C_{GS} + C_{GD} = C_{GS} + C_{RSS}. \tag{23}$$

Calculation of the rise and fall times begins with an understanding of how the gate driver charges the input capacitances in Figure 7 through the various stages of switching. When the switch turns on:

1. The gate driver charges C_{GS}. The gate voltage, v_{GS}, increases to the gate-threshold voltage, V_{TH}.
2. The gate driver continues to charge C_{GS}. v_{GS} continues to increase as i_{DS} rises to $I_{DS,max}$.
3. The gate driver now discharges C_{GD}. v_{GS} remains constant at the gate-plateau voltage, V_{GP}, as v_{DS} falls to near-zero.

When the switch turns off:

4. The gate driver discharges C_{GS}. v_{GS} decreases to V_{GP}.

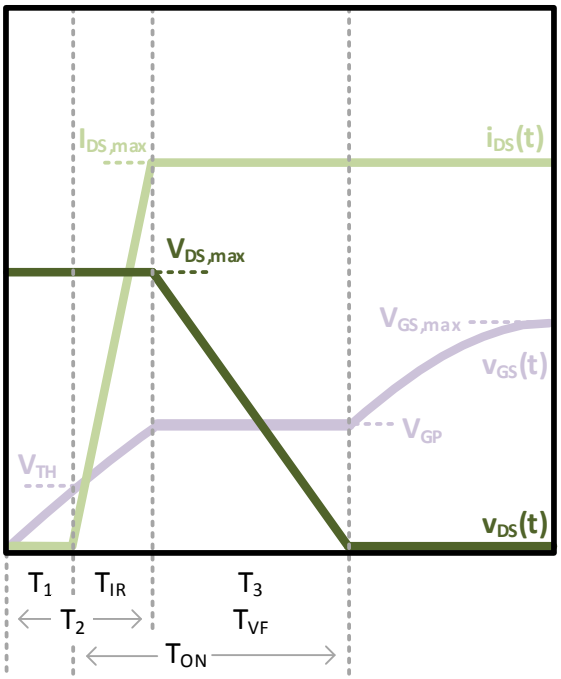

Figure 5. Switch turn-on transient.

5. The gate driver charges C_{DS}. v_{GS} remains constant at V_{GP} as v_{DS} rises to $V_{DS,max}$.
6. The gate driver discharges C_{GS}. v_{GS} decreases to V_{TH} and i_{DS} falls to near-zero.

The durations of these six phases can each be solved as a simple R-C circuit, following the appropriate charging paths in Figure 7. During T_1 and T_2, the gate current charges C_{GS}, and v_{GS} follows the typical negative-exponential curve of an R-C circuit. During T_3, v_{GS} is constant, thus injecting a constant current into C_{GD} and causing V_{DS} to fall linearly. The turn-on phase timings are:

$$T_1 = R_G C_{ISS} \ln\Big(\frac{V_{GS,max}}{V_{GS,max} - V_{TH}}\Big) \tag{24}$$

$$T_2 = R_G C_{ISS} \ln\Big(\frac{V_{GS,max}}{V_{GS,max} - V_{GP}}\Big) \tag{25}$$

$$\begin{aligned} T_3 = T_{VF} &= R_G C_{GD} \frac{V_{DS,max}}{V_{GS,max} - V_{GP}} \\ &\approx R_G \frac{Q_{GD,0}}{V_{DS,0}} \frac{V_{DS,max}}{V_{GS,max} - V_{GP}}. \end{aligned} \tag{26}$$

Similarly, the gate current discharges C_{GS} during T_4 and T_6, and charges C_{GD} during T_5. The turn-off phase timings are:

$$T_4 = R_G C_{ISS} \ln\Big(\frac{V_{GS,max}}{V_{GP}}\Big) \tag{27}$$

$$T_5 = T_{VR} = R_G C_{GD} \frac{V_{DS,max}}{V_{GP}} \approx R_G \frac{Q_{GD,0}}{V_{DS,0}} \frac{V_{DS,max}}{V_{GP}} \tag{28}$$

$$T_6 = T_{IF} = R_G C_{ISS} \ln\Big(\frac{V_{GP}}{V_{TH}}\Big). \tag{29}$$

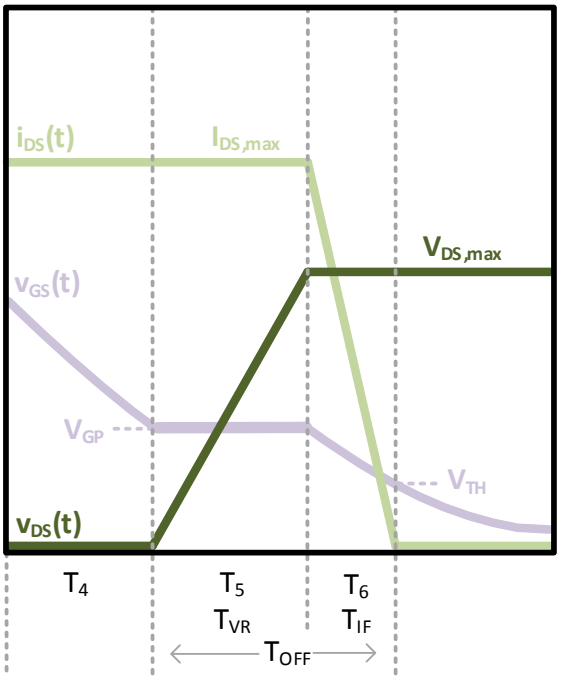

Figure 6. Switch turn-off transient.

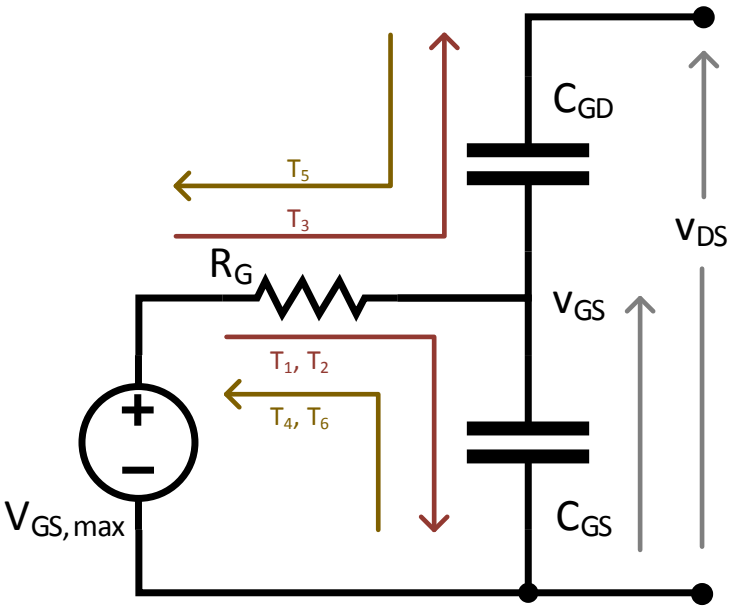

Figure 7. Parasitics circuit describing the switch switching-loss mechanism.

Although Figure 7 suggests to calculate T_3 and T_5 from C_{GD}, in practice C_{GD} actually varies considerably with v_{DS} [29,31,32]. As such, it is recommended instead to express T_3 and T_5 as a function of the gate charge, Q_{GD}, that is drained from C_{GD} during T_3 and added during T_5. The datasheet often lists Q_{GD} at a specific test point with gate-charge $Q_{GD,0}$ corresponding to drain-source voltage $V_{DS,0}$.

As shown in Figures 5 and 6, $T_{IR} = T_2 - T_1$, $T_{VF} = T_3$, $T_{VR} = T_5$, and $T_{IR} = T_6$. In addition, T_1 is turn-on delay and T_4 is the turn-off delay. Expressions for the the rise and fall timings are summarized in Table A5 (Appendix .3).

The energy lost over the turn-on and turn-off region of overlap is generally calculated as:

$$E_{Q,sw,hs} = \frac{1}{2} V_{DS,max} I_{DS,max} T \tag{30}$$

where T is either the turn-on time $T_{ON} = T_{IR} + T_{VF}$ or the turn-off time $T_{OFF} = T_{VR} + T_{IF}$. $V_{DS,max}$ and $I_{DS,max}$ depend on the circuit and model. For the simple boost converter model,

$$P_{Q,sw,hs}(\theta) = \frac{V_O I_{ref}(\theta) f}{2} (T_{ON} + T_{OFF}), \tag{31}$$

and for the boost converter model with ripple,

$$\begin{aligned} P_{Q,sw,hs}(\theta) = & \frac{V_o f}{2} \Big((I_{ref}(\theta) - \frac{\Delta i_{L,pp}(\theta)}{2}) T_{ON} \\ & + (I_{ref}(\theta) + \frac{\Delta i_{L,pp}(\theta)}{2}) T_{OFF} \Big). \end{aligned} \tag{32}$$

The average hard-switching loss can be derived from Table A5 and (22), (31) and (32). Formulae for the hard-switching loss models are shown in Table A6 (Appendix .3).

4.2. Output-Capacitance Loss

Every switching cycle, the switch's parasitic equivalent output capacitance, C_{oss}, stores charge and discharges through the on-resistance. This loss is derived from the energy stored on the capacitor every cycle [24]:

$$P_{Q,sw,c} = \frac{1}{2} C_{oss} V_o^2 f. \tag{33}$$

5. Switching Loss in the Diode (D)

This section derives the switching loss models for diode reverse recovery, $P_{D,sw,rr}$, and junction capacitance, $P_{D,sw,c}$. The resulting formulae are organized in Appendix .4.

5.1. Reverse Recovery Loss

The boost diode's reverse recovery occurs when the diode switches from conducting to blocking. As the diode becomes reverse biased, the depletion-layer's charge is injected into the system as the reverse-recovery current, and causes loss in both the diode and switch. The reverse-recovery current, shown in Figure 8, is approximated as a triangular function characterized by the peak reverse-recovery current, I_{rr}, and the reverse-recovery time segments, T_a and T_b, which sum to the total reverse-recovery time T_{rr} [33–35]. The diode's reverse-recovery transient is also determined by its forward current, I_F, prior to switching, and the slope of its switching current, $\frac{dI_D}{dt}$, where

$$\frac{dI_D}{dt} = \frac{I_{rr}}{T_a}. \tag{34}$$

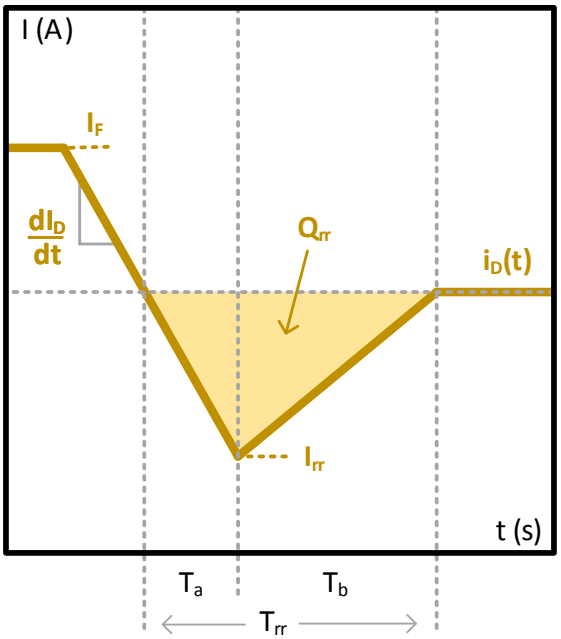

Figure 8. Diode reverse-recovery loss waveforms.

In addition, the reverse-recovery charge, Q_{rr}, is the area of the triangle and can be approximated as

$$Q_{rr} = \frac{T_{rr} I_{rr}}{2}. \tag{35}$$

Tables and charts in datasheets will often provide some combination of I_{rr}, I_F, T_{rr}, $\frac{dI_D}{dt}$, and Q_{rr}, but this data is usually constrained to a specific operating point. In order to derive a reverse-recovery model that holds over a wide operating range, the diode's intrinsic characteristics must be quantified. These include the diode's softness or snappiness factor, S, where

$$S = \frac{T_b}{T_a}. \tag{36}$$

In addition, the forward-biased charge coefficient, K_Q, can be approximated as

$$Q_F = K_Q \sqrt{I_F} \approx Q_{rr}, \tag{37}$$

since the junction's stored forward-biased charge, Q_F, is approximately equal to reverse-recovery charge, Q_{rr}, that is ejected upon switching [33]. As such, S and K_Q can be calculated from a datasheet using these formulae:

$$S = \frac{T_{rr,0} \frac{dI_{D,0}}{dt}}{I_{rr,0}} - 1 \tag{38}$$

$$K_Q = \frac{I_{rr,0} T_{rr,0}}{2\sqrt{I_{F,0}}}, \tag{39}$$

where the "0" indicates that each value is pulled from the datasheet, and has only been measured at a specific operating point.

The diode model uses S and K_Q to estimate the reverse-recovery characteristics I_{rr}, T_a, and T_b at any arbitrary operating point:

$$I_{rr} = \sqrt{\frac{2\frac{dI_D}{dt}K_Q\sqrt{I_F}}{1+S}} \tag{40}$$

$$T_a = \frac{I_{rr}}{\frac{dI_D}{dt}} \tag{41}$$

$$T_b = ST_a. \tag{42}$$

These formulae require knowledge of I_F and $\frac{dI_D}{dt}$ for the given power converter. For the simple boost converter model, $I_F = i_L(\theta,t) = I_{ref}(\theta)$. For the boost converter model with ripple, $I_F = I_{ref}(\theta) - \frac{\Delta i_{L,pp}}{2}$, which must be greater than zero in continuous conduction mode. In either case, $\frac{dI_D}{dt} = \frac{I_F}{T_{IR}}$, where T_{IR} is the switch's current rise time previously defined in Table A5.

The energy lost per switching cycle is geometrically calculated from Figure 9 as

$$E_Q = V_{DS}(\frac{I_{rr}}{2}T_a + \frac{I_{rr}}{4}T_b) \tag{43}$$

$$E_D = \frac{V_R I_{rr}}{4}T_b \tag{44}$$

$$P_{D,rr}(\theta) = (E_Q + E_D)f, \tag{45}$$

where $V_{DS} = V_R = V_O$ for a boost converter [36]. As it happens, S falls out of the equation, and only K_Q need be solved.

The average reverse-recovery loss power can be derived from (22) and (45). Equation (22) yields a simple result for the DC boost converter, shown in Table A7. However, the AC boost converter's expressions simplify to a non-integrable form, which can be closely approximated by a second-order taylor series:

$$\sqrt{Asin(\theta) + Bsin^2(\theta)} \approx \sqrt{A+B} - \frac{(\theta - \frac{\pi}{2})^2(A+2B)}{4\sqrt{A+B}}. \tag{46}$$

The AC converter's reverse-recovery loss model uses (46) to derive the results shown in Table A7 (Appendix .4).

5.2. Junction-Capacitance Loss

The diode's parasitic junction capacitance, C_j, discharges when the diode switches from blocking to conducting. This capacitance results from the parallel-plate characteristics of the insulating depletion layer and the conducting P and N regions. Similar to (33), the capacitive loss is carried by the switch and is modeled as [24]:

$$P_{D,sw,c} = \frac{1}{2}C_j V_o^2 f. \tag{47}$$

6. Model Validation

This work uses both simulation and experiment to validate the boost converter loss models.

6.1. Simulation Validation

Conduction loss is validated via a PSIM 11.1.5 transient simulation over a single AC cycle. The modeled ideal boost converter either has an AC PFC or a DC controller, and operates at $V_{pk} = 170$ V, $V_o = 350$ V, and $P_o = 250$ W. The simulated component currents are all within 0.5% of the simple model and 0.1% of the model with ripple.

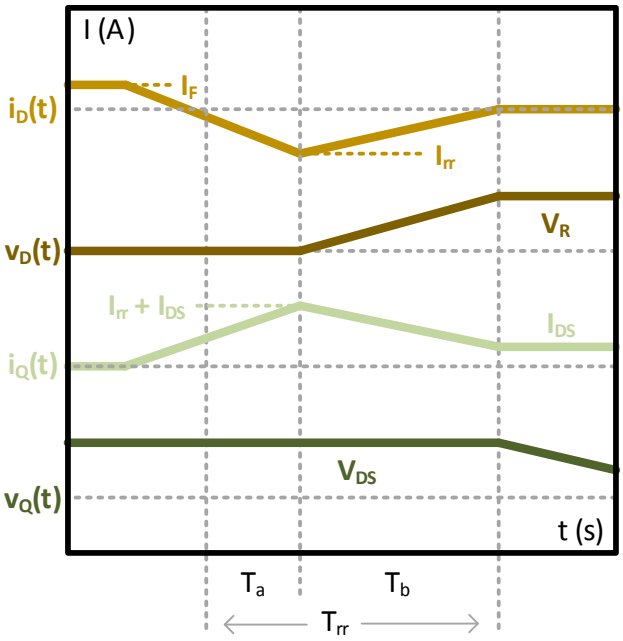

Figure 9. Diode and switch current and voltage waveforms for the boost converter. Note that for the boost converter, $V_R = V_{DS} = V_O$ and $I_F = I_{DS} = i_{ref} - \Delta i_{L,pp}$ at the time of transition.

This work uses LTSpice to validate the switching loss in the MOSFET since the PSIM level 2 simulation models do not account for the change in C_{DS} with V_{DS}. The STP8NM60 MOSFET is simulated in LTSpice with and without a 10 Ω gate-driver resistance. The simulation is run with $V_{IN} = 170V$, $V_O = 335V$, and $P_o = 775W$. Measurements of the rise and fall times are taken from the 10% to 90% levels. The simulated switching loss is within 9% of the simple model and 15% of the model with ripple. The discrepancy is mostly from the way in which LTSpice models the hard-switching overlap.

This work attempted to use the PSIM level 2 diode model to validate the diode reverse-recovery loss because LTSpice does not properly model T_b [37]. Simulations were performed in a standard inductively-switched 400 V reverse recovery test rig, with $\frac{dI_D}{dt}$ parametrically swept from 200 A/µs to 1000 A/µs and I_F swept from 2 A to 10 A. This work compares the both the model and simulation to the highly-detailed datasheet curves for a LQA08TC600 and RFNL5TJ6S diode. As it happens, the model's estimate of I_{rr} and T_{rr} was actually better than that of the simulation. The modeled diode calculated I_{rr} with 9-13% error, and T_{rr} with 10-14% error. The simulation calculated I_{rr} with 22-71% error, and T_{rr} with 11-22% error.

6.2. Experimental Validation

This work uses the DC boost converter prototype in Figure 10 as an experimental validation. The converter's components and lab equipment are listed in Table 1. This work focuses on validating the full end-to-end efficiency, which extends the previous component current validation [9]. The converter is operated in DC/DC mode with duty cycle of 50%, input of 24 V, 48 V, and 96 V, and output current swept from 0-2 A. The results in Figure 11 show a decent consistency between the experiment and model, with an efficiency difference of at most 3.4%. The model slightly under-estimates the loss at high current, indicating possible unaccounted resistive parasitics in the PCB and measurement equipment.

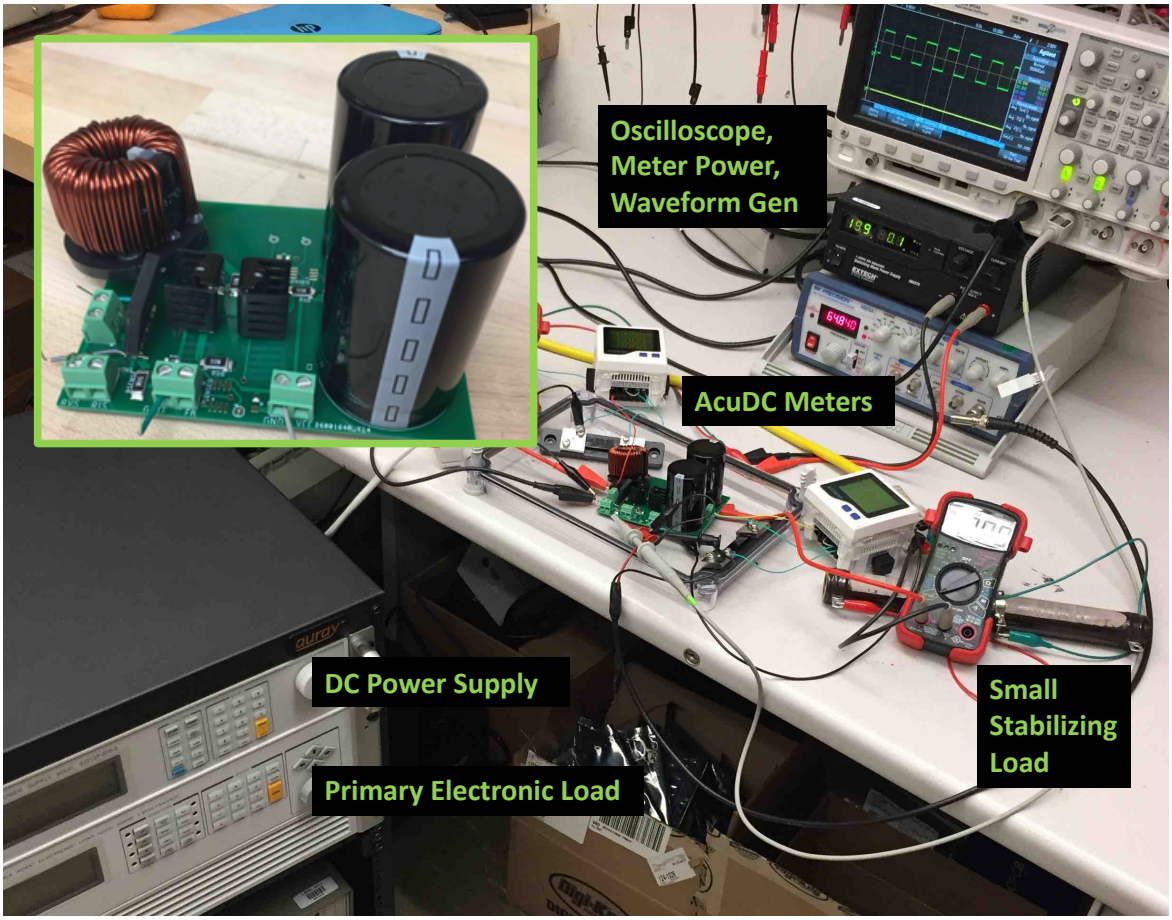

Figure 10. DC boost converter experimental validation prototype.

Table 1. Components in DC Boost Prototype

Component	Identification Number
Inductor	Premo PFCA500-8H
Diode Bridge	Diodes Inc. GBU804
Switch	STMicroelectronics STP9NK60Z
Boost Diode	Power Integrations LQA08TC600
Capacitor (2x)	TDK Electronics B43544A6477M000
DC Power Supply	Chroma 62024P-600-8
Electronic Load	Chroma 63802
Revenue-Grade DC Meter	AccuEnergy AcuDC 243-600V-A1-P2-C-D

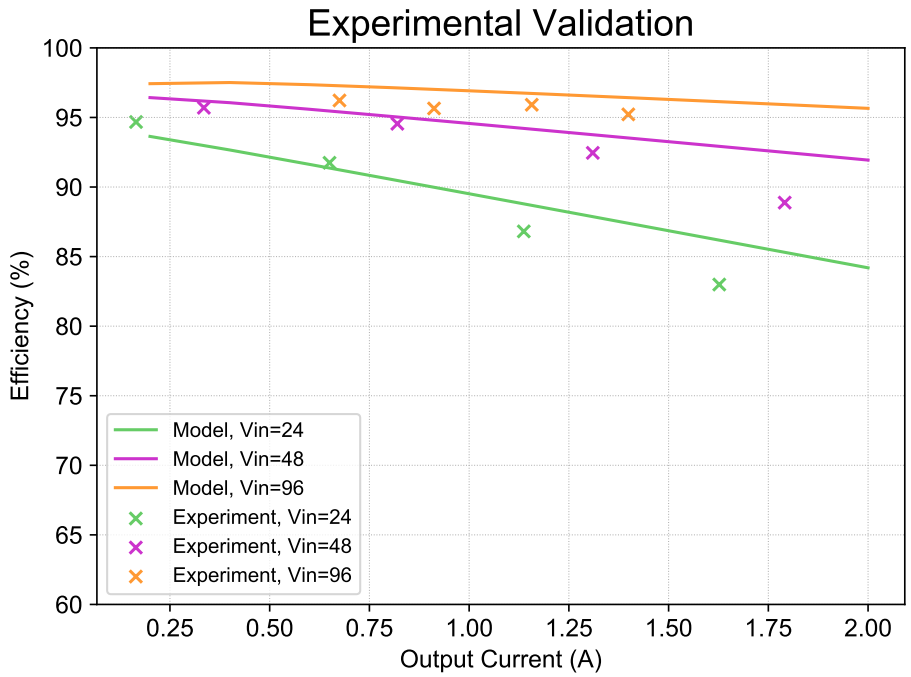

Figure 11. Comparison between experiment and model. Duty cycle is 50%.

7. Efficiency Comparison of AC vs. DC

This work compares AC and DC boost converters through a parametric analysis that applies parasitics from the components in Table 1 to the modeling formulae in Appendices .1 to .4, and sweeps the output power from 50 W to 500 W and the output voltage from 200 V to 400 V. The resulting modeled efficiency curves in Figure 12 illustrate how these models allow for a direct converter loss comparison. The AC boost converter may have up to 2.5 times the loss of its DC equivalent over the given output power and voltage range. Figure 13 presents a loss analysis that reveals the switch as the primary source of loss for this particular set of components.

8. Conclusion and Future Work

Past research compares the full-building efficiency between AC and DC systems, but these modeled systems rarely have equivalent voltage levels and power electronics. This work focuses specifically on comparing an AC/DC PFC and DC/DC boost converter. It develops a rigorous formulaic loss model, and validates this model via simulation and experiment. The loss model and simulation were compared over a range of values, and matched within 0.5% for conduction loss and 15% for switching loss. The loss model and experiment were compared for a DC/DC boost converter and found to match within 3.4%. A parametric loss analysis of modeled converters in the range of 200 to 400 V and 50 to 500 W shows AC/DC PFC boost converters to have up to 2.5 times the loss of DC/DC boost converters.

This study is part of a larger research effort to rigorously compare AC and DC buildings. While this study validates the efficiency benefits of DC/DC boost converters, there are many other types of power converters that can be developed in future work. A full-building efficiency study should at least develop two more converter loss models: (a) a flyback converter that represents small loads such as electronics and lighting, and (b) a half-bridge inverter that represents microgrid equipment such as solar and battery inverters. Future work would also study the variance in component parasitics to determine the most representative efficiency curve for each class of converter. An analysis of other methods of operation such as soft switching and discontinuous conduction mode may also prove valuable. These improvements can all work toward creating an accurate full-building energy model.

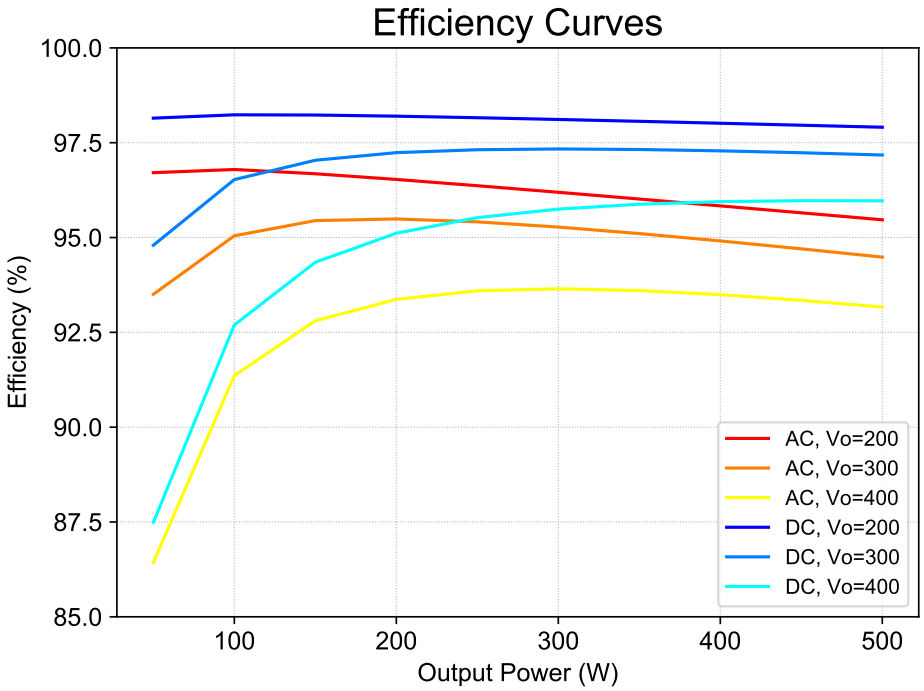

Figure 12. These efficiency curves are the result of a parametric analysis of AC and DC boost converters. The AC converters have slightly higher switching loss and much higher conduction loss than their DC counterparts.

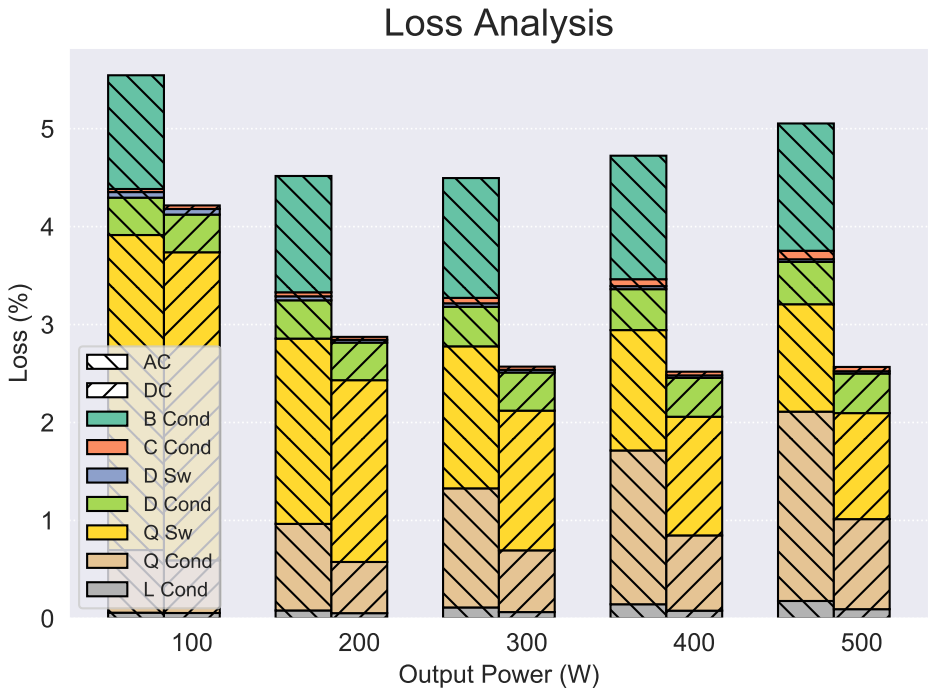

Figure 13. A loss analysis and itemized loss breakdown. The bar segments represent the percent loss (loss power divided by input power) that occurs in each component. Each pair of bars compares the loss in the AC (left) and DC (right) boost converters. The converters were modeled with an input voltage $V_{pk} = 170$ V and an output voltage $V_o = 250$ V

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Appendix .1 Model Equations

This work models conduction (cond) and switching (sw) losses in the following components: the input inductor (L), the output capacitor (C), the switch (Q), and the boost diode (D). The AC boost converter also has a diode bridge (B). The total converter loss is:

$$\begin{aligned} P_{loss} =& P_{L,cond} + P_{B,cond} + P_{C,cond} \\ &+ P_{Q,cond} + P_{Q,sw,hs} + P_{Q,sw,c} \\ &+ P_{D,cond} + P_{D,sw,rr} + P_{D,sw,c} \end{aligned} \tag{A1}$$

Appendix .2 $P_{X,cond}$: Conduction Loss

The component current formulas are shown in Tables A1 to A3 for the simple model and model with ripple, respectively. These component currents are used to determine the conduction loss power, $P_{X,cond}$, as shown in Table A4.

Table A1. Component currents in the simple model

Parameter	AC PFC Model Formula	DC Model Formula
$I_{L,rms}$ $I_{B,rms}$	$\frac{\sqrt{2}P_o}{V_{pk}}$	$\frac{P_o}{V_{pk}}$
$I_{B,avg}$	$\frac{4}{\pi}\frac{P_o}{V_{pk}}$	$--$
$I_{Q,rms}$	$\frac{P_o}{\sqrt{V_o}V_{pk}}\sqrt{2V_o - \frac{16}{3\pi}V_{pk}}$	$\frac{P_o}{\sqrt{V_o}V_{pk}}\sqrt{V_o - V_{pk}}$
$I_{D,rms}$	$\frac{4}{\sqrt{3\pi}}\frac{P_o}{\sqrt{V_o V_{pk}}}$	$\frac{P_o}{\sqrt{V_o V_{pk}}}$
$I_{D,avg}$	$\frac{P_o}{V_o}$	$\frac{P_o}{V_o}$
$I_{C,rms}$	$\frac{P_o}{V_o\sqrt{V_{pk}}}\sqrt{\frac{16}{3\pi}V_o - V_{pk}}$	$\frac{P_o}{V_o\sqrt{V_{pk}}}\sqrt{V_o - V_{pk}}$

Appendix .3 $P_{Q,sw,hs}$ and $P_{Q,sw,c}$: Hard switching and output capacitance loss

Switch timings are organized in Table A5. Final formulae for the hard switching loss, $P_{Q,sw,hs}$, are given in Table A6, noting that $T_{ON} = T_{IR} + T_{VF}$ and $T_{OFF} = T_{VR} + T_{IF}$. A negative-value result may imply the converter is not in continuous conduction mode. The switch output capcitance loss, $P_{Q,sw,c}$, is:

$$P_{Q,sw,c} = \frac{1}{2}C_{oss}V_o^2 f. \tag{A2}$$

Table A2. AC PFC component currents model with ripple

Parameter	Model Formula
$I_{L,rms}$ $I_{B,rms}$	$\frac{\sqrt{576\pi L^2 P_o^2 V_o^2 f^2+12\pi V_o^2 V_{pk}^4-64 V_o V_{pk}^5+9\pi V_{pk}^6}}{12\sqrt{2}\sqrt{\pi} L V_o V_{pk} f}$
$I_{B,avg}$	$--$
$I_{Q,rms}$	$\frac{\sqrt{\begin{array}{c}2880\pi L^2 P_o^2 V_o^3 f^2-7680 L^2 P_o^2 V_o^2 V_{pk} f^2+60\pi V_o^3 V_{pk}^4\cdots \\ -480 V_o^2 V_{pk}^5+135\pi V_o V_{pk}^6-128 V_{pk}^7\end{array}}}{12\sqrt{10}\sqrt{\pi} L V_o^{\frac{3}{2}} V_{pk} f}$
$I_{D,rms}$	$\frac{\sqrt{3840 L^2 P_o^2 V_o^2 f^2+80 V_o^2 V_{pk}^4-45\pi V_o V_{pk}^5+64 V_{pk}^6}}{12\sqrt{5}\sqrt{\pi} L V_o^{\frac{3}{2}} \sqrt{V_{pk}} f}$
$I_{D,avg}$	$\frac{P_o}{V_o}$
$I_{C,rms}$	$\frac{\sqrt{\begin{array}{c}3840 L^2 P_o^2 V_o^2 f^2-720\pi L^2 P_o^2 V_o V_{pk} f^2\cdots \\ +80 V_o^2 V_{pk}^4-45\pi V_o V_{pk}^5+64 V_{pk}^6\end{array}}}{12\sqrt{5}\sqrt{\pi} L V_o^{\frac{3}{2}} \sqrt{V_{pk}} f}$

Table A3. DC component currents model with ripple

Parameter	Model Formula
$I_{L,rms}$ $I_{B,rms}$	$\frac{\sqrt{12 L^2 P_o^2 V_o^2+T^2 V_o^2 V_{pk}^4-2T^2 V_o V_{pk}^5+T^2 V_{pk}^6}}{2 L V_o V_{pk}\sqrt{3}}$
$I_{B,avg}$	$--$
$I_{Q,rms}$	$\frac{\sqrt{\left(V_o-V_{pk}\right)\left(12 L^2 P_o^2 V_o^2+T^2 V_o^2 V_{pk}^4-2T^2 V_o V_{pk}^5+T^2 V_{pk}^6\right)}}{2 L V_{pk}\sqrt{3 V_o^3}}$
$I_{D,rms}$	$\frac{\sqrt{12 L^2 P_o^2 V_o^2+T^2 V_o^2 V_{pk}^4-2T^2 V_o V_{pk}^5+T^2 V_{pk}^6}}{2L\sqrt{3 V_o^3 V_{pk}}}$
$I_{D,avg}$	$\frac{P_o}{V_o}$
$I_{C,rms}$	$\frac{\sqrt{\left(V_o-V_{pk}\right)\left(12 L^2 P_o^2 V_o+T^2 V_o V_{pk}^4-T^2 V_{pk}^5\right)}}{2L\sqrt{3 V_o^3 V_{pk}}}$

Appendix .4 $P_{D,sw,hs}$ and $P_{D,sw,c}$: Diode reverse recovery and junction capacitance loss

Formulae for the boost diode reverse recovery loss, $P_{D,sw,rr}$, are given in Table A7, given that:

$$K_Q = \frac{I_{rr,0} T_{rr,0}}{2\sqrt{I_{F,0}}}. \tag{A3}$$

A complex-value result may imply the converter is not in continuous conduction mode. The diode junction capcitance loss, $P_{D,sw,c}$, is:

$$P_{D,sw,c} = \frac{1}{2} C_j V_o^2 f. \tag{A4}$$

Table A4. Conduction loss, $P_{X,cond}$

Parameter	**Model Formula**
$P_{L,cond}$	$I_{L,rms}^2 R_L$
$P_{B,cond}$	$I_{B,avg} V_B + I_{B,rms}^2 R_B$
$P_{Q,cond}$	$I_{Q,rms}^2 R_Q$
$P_{D,cond}$	$I_{D,avg} V_D + I_{D,rms}^2 R_D$
$P_{C,cond}$	$I_{C,rms}^2 R_C$

Table A5. Switch Rise and Fall Timings

Timing	**Formula**
T_{IR}	$R_G C_{ISS} \ln\left(\frac{V_{GS,max}-V_{TH}}{V_{GS,max}-V_{GP}}\right)$
T_{VF}	$R_G \frac{Q_{GD,0}}{V_{DS,0}} \frac{V_{DS,max}}{V_{GS,max}-V_{GP}}$
T_{VR}	$R_G \frac{Q_{GD,0}}{V_{DS,0}} \frac{V_{DS,max}}{V_{GP}}$
T_{IF}	$R_G C_{ISS} \ln\left(\frac{V_{GP}}{V_{TH}}\right)$

Table A6. Hard-switching loss, $P_{Q,sw,hs}$

Model	**Average Loss Power**
AC PFC (simple)	$\frac{2P_o V_o f\left(T_{off}+T_{on}\right)}{\pi V_{pk}}$
DC (simple)	$\frac{P_o V_o f\left(T_{off}+T_{on}\right)}{2V_{pk}}$
AC PFC (ripple)	$\frac{\left(\begin{array}{c}16LP_oT_{off}V_of+16LP_oT_{on}V_of+4T_{off}V_oV_{pk}^2\cdots \\ -\pi T_{off}V_{pk}^3-4T_{on}V_oV_{pk}^2+\pi T_{on}V_{pk}^3\end{array}\right)}{8\pi LV_{pk}}$
DC (ripple)	$\frac{\left(\begin{array}{c}2LP_oT_{off}V_of+2LP_oT_{on}V_of+T_{off}V_oV_{pk}^2\cdots \\ -T_{off}V_{pk}^3-T_{on}V_oV_{pk}^2+T_{on}V_{pk}^3\end{array}\right)}{4LV_{pk}}$

Table A7. Diode reverse recovery loss, $P_{D,sw,rr}$

Model	**Average Loss Power**
AC PFC (simple)	$\frac{K_Q\sqrt{P_o}V_o f\left(48-\pi^2\right)}{24\sqrt{2}\sqrt{V_{pk}}}$
DC (simple)	$\frac{K_Q\sqrt{P_o}V_o f}{\sqrt{V_{pk}}}$
AC PFC (ripple)	$\frac{K_Q\sqrt{V_o}\sqrt{f}\left(\begin{array}{c}-4\pi^2 LP_oV_of+192LP_oV_of-48V_oV_{pk}^2\cdots\\+\pi^2V_oV_{pk}^2-2\pi^2V_{pk}^3+48V_{pk}^3\end{array}\right)}{48\sqrt{2}\sqrt{L}\sqrt{V_{pk}}\sqrt{4LP_oV_of-V_oV_{pk}^2+V_{pk}^3}}$
DC (ripple)	$\frac{K_Q\sqrt{V_o}\sqrt{f}\sqrt{2LP_oV_of-V_oV_{pk}^2+V_{pk}^3}}{\sqrt{2}\sqrt{L}\sqrt{V_{pk}}}$