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3D Hybrid Integration for Silicon Photonics

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Doctor of Philosophy
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by

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To my parents and wife, Jingyi.

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Abstract

3D Hybrid Integration for Silicon Photonics

by

Bowen Song

Silicon photonics (SiPh) has emerged as a photonic integrated circuit (PIC) platform, especially for high volume applications. Integrated laser sources, however, remain a challenge. SiPh foundries have existed for more than 10 years but still don't offer a qualified process with integrated lasers. Direct heteroepitaxy of group III-V materials on silicon is still immature and suffers from reliability issues. Heterogeneous and hybrid integration techniques, however, have been pursued in research and by industry and present a practical near-term solution for laser integration. Heterogenous approaches based on wafer bonding involve the bonding of bare III-V epitaxial material to silicon on insulator (SOI), co-fabrication, and evanescent light coupling. The laser active medium is thermally isolated from the silicon substrate by the buried oxide layer limiting the laser efficiency at high temperature. Hybrid integration approaches, such as the butt coupling of fabricated III-V lasers to SOI waveguides, may address the thermal issue. However, the main limitation for butt coupling is the significant mode mismatch of the waveguides that imposes a strict alignment requirement.

In this thesis the novel 3D hybrid integration technique for SiPh, addressing the aspects of thermal performance and alignment tolerance, was proposed and demonstrated for the first time. This approach is based on the flip-chip integration of indium phosphide (InP) reflective semiconductor optical amplifiers (RSOAs) containing total internal reflection turning mirrors for surface emission. Light is coupled to the SOI waveguides through surface grating couplers. This technique yields increased alignment tolerance compared

to butt coupling. Flip-chip integration also allows the RSOA chip to be bonded P-side down directly to the silicon substrate. In this way, the heat generated in the active region can dissipate more efficiently in the silicon. 3D hybrid integration can be carried out at wafer level in a backend step for high throughput manufacturing, and also allow for the integration of InP PICs on silicon interposers for large-scale electronic-photonic integration.

A tunable laser was realized with 3D hybrid integration demonstrating a side-mode suppression ratio up to 43 dB. Greater than 4 mW of optical power was coupled into SiPh waveguide and more than 20 nm wavelength tuning range was achieved. A linewidth of 1.5 MHz and relative intensity noise of -132 dB/Hz were measured. A low thermal impedance of 6.2°C/W was extracted experimentally from a 3D hybrid laser that was bonded to the silicon substrate, demonstrating a factor of three improvement over a laser that was bonded above the SOI layer. To improve coupling efficiency, various advanced silicon surface grating couplers as well as dilute waveguide RSOAs were investigated. Coupling efficiency up to 85% can be achieved while also maintaining an alignment tolerant implementation.

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Chapter 1

Introduction

Photonic integrated circuits (PICs) integrate various optical functions, such as light generation, amplification, guiding, coupling and detection on a signal chip [1]. Following decades of development, PICs provide high performance optical systems by removing assembly complexity and variability, at the same time enabling size, weight, power and cost reduction. Large-scale photonics integration not only could boost the development of modern data communications but could also play an important role in applications such as sensing and biomedical. In this chapter, the review of state-of-art PIC material systems will be presented. Following this, the current integrated laser technology for silicon photonics (SiPh) will be summarized. Then, the concept of 3D hybrid integrated laser technology will be introduced. The thesis overview will be provided in the last section of the chapter.

1.1 Silicon Photonics

SiPh is being adopted as a mainstream optical technology to support large-scale integration of optical functions on a single silicon chip. The primary selling point of SiPh

is that it utilizes commercial state-of-the-art complementary metal–oxide–semiconductor (CMOS) foundries [2]. Firstly, a benefit of building PICs in CMOS foundries is reduced cost at large volumes. Larger wafers (up to 12 inches) and the mature CMOS integrated circuit (IC) facilities can bridge the gap between concept demonstration and volume production. Second, the high yield CMOS processes eliminate manual wafer handling. CMOS reliability and reproducibility outperform the group III-V integrated photonics where automated wafer handling is not commonly used. Lastly, compared to cleaving prior to testing, great enhancement of throughput is achieved with wafer scale testing and packaging [3]. Another significant advantage of SiPh is the merging photonic functions and CMOS; integrated photonics and electronics can be fabricated on the same wafer [4]. Large-scale chip-level optoelectronics integration enables high performance system with more complexity, functionality and reliability [5]. Silicon and silicon dioxide (SiO_2) provide high index contrast and the nano-wire waveguide provides relatively low loss and small footprint. Thus, the integration scale can be increased dramatically with controllable cost. The functionality of complex SiPh systems goes beyond the boundary of data communications applications [6]. Many novel applications have been reported including: biosensing [7], LIDAR systems [8], narrow linewidth lasers [9] and artificial intelligence [10].

1.2 Indium Phosphide Photonic Integrated Circuits

III-V compound semiconductors provide a monolithic integration platform for PICs that have undergone decades of development. Indium phosphide (InP) and gallium arsenide (GaAs) are most common. These direct bandgap materials provide high performance active components including lasers, modulators and photodetectors. Highly developed epitaxy techniques such as Metal-Organic Chemical Vapor Deposition (MOCVD)

and Molecular Beam Epitaxy (MBE) enable high quality, low-defect-density quaternary alloys [11]. InP-based quaternary alloys have played an enabling role in the critically important 1.1–1.6 μm spectral window for fiber-optic systems. Quaternary alloys allow for remarkable flexibility in the range of bandgaps and refractive indices. A wide range of optical waveguide devices with different direct bandgaps are now available on the same substrate, leading to a powerful class of InP PICs. InP based PICs have evolved from a simple distributed Bragg reflector (DBR) laser to complex on chip systems with passive components including optical splitters, filters, multiplexers, and combiners and active components such as semiconductor optical amplifiers, lasers, modulators, and photodetectors [12]. Figure 1.1 shows a mask layout and top view microscope picture of an InP PIC fabricated that includes a widely tunable laser, an integrated wavelength locking feature, and a coherent receiver. There have been significant achievements made in realizing relatively complex InP PICs in recent years, enabling new class of applications beyond telecommunication and data communications. A great deal of effort from both academia and industry has made the significant advances of this technology possible. This development has resulted in a positive and profound impact in many areas including data communication [13], free space comminutions [14], and consumer photonics [15]. Performance advances have been enabled through sustained technology developments for InP-based epitaxial and fabrication processes as well as device design innovations.

Despite of all the advantages, III-V based PICs still face challenges. The first drawback comes from wafer cost and size. The cost of an InP wafer is still higher than a silicon wafer, and wafer size is limited to 4 inches. The InP PIC process also cannot compete with the CMOS process in terms of yield and reliability. The optical confinement for the InP platform is significantly smaller than that for SiPh. The minimum bend radius of a deeply etched waveguide is greater than 10 μm whereas less than 2 μm has been reported for SiPh [16]. The packaging of InP devices still relies primarily on gold boxes and wire

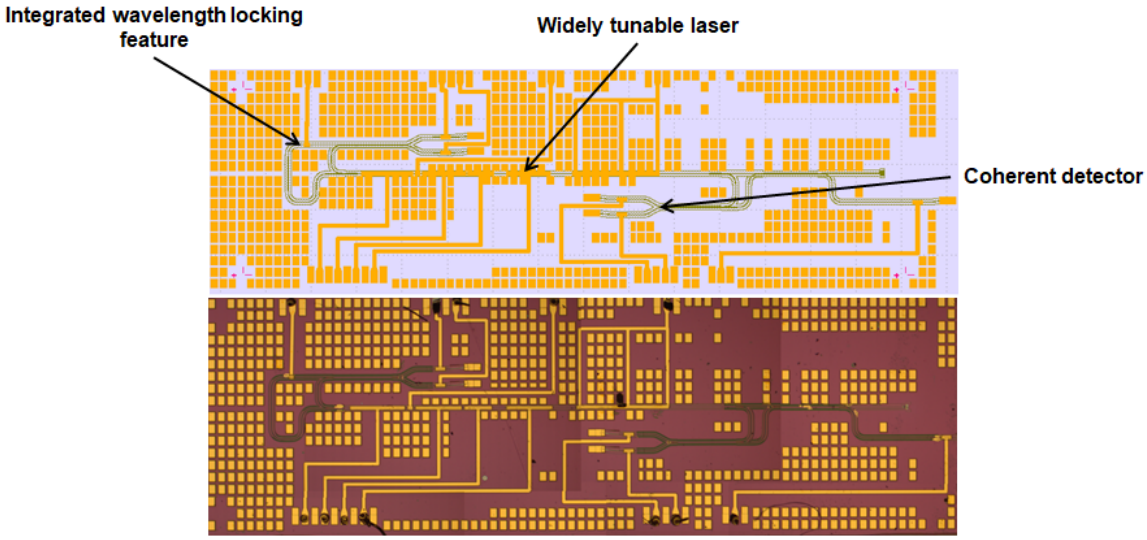


Figure 1.1: Example InP PIC with schematic (top) and top-view microscope picture (bottom)

bonding [17]. Low loss waveguide devices are also difficult to fabricate.

1.3 Lasers for Silicon Photonics

Although SiPh has undergone significant maturation in recent years, the integration of low-cost, high-efficiency laser sources remains an open problem. SiPh interposer technologies also require the integration of PICs with other platforms at low cost. For these integrations, high coupling efficiency with high alignment tolerance is critical. In this section, current laser integration technologies for SiPh are reviewed.

1.3.1 Monolithic Integration

Monolithic integration techniques based on heteroepitaxy are a natural and intuitive means of laser integration. Pulsed lasing has been demonstrated using strained germanium (Ge) as a gain material [18]. However, the efficiency of fabricated lasers based on

Ge on silicon are too low for practical applications. Another approach for a monolithically integrated laser source based on silicon is the epitaxial growth of direct bandgap materials, such as GaAs and InP. Quantum dot lasers on silicon [19] [20] and nanowire lasers [21] have been reported. However, epitaxial growth of GaAs and InP on silicon is not trivial, due to the large lattice mismatches of these materials with silicon [20]. A schematic illustration of defects generation for GaAs on silicon growth is shown in Fig. 1.2. The formation of defects is detrimental to the performance of lasers and needs to be addressed.

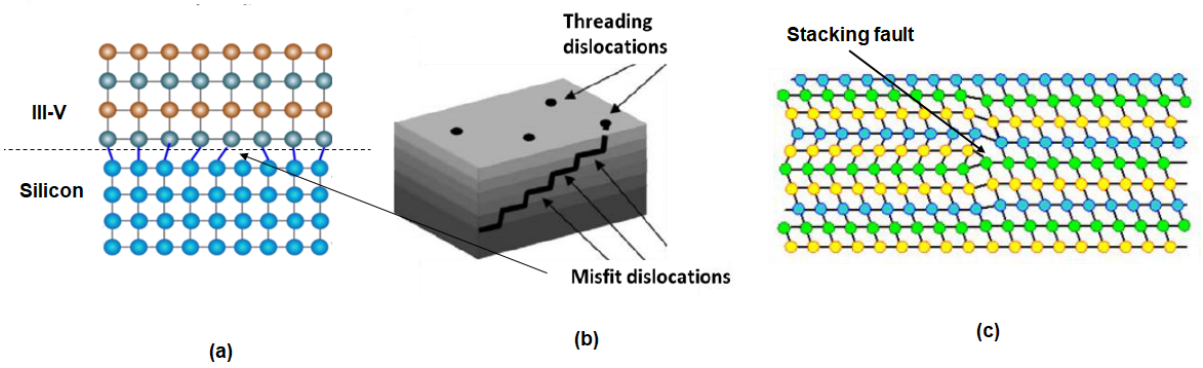


Figure 1.2: Formation of (a) misfit dislocations (b) threading dislocations and (c) stacking fault.

Many techniques have been developed to improve the quality of III-V films on silicon including Ge [22] or gallium phosphide buffer layers [23], nano patterned silicon substrate [24], confined epitaxial lateral overgrowth [25], thermal cycle annealing and strained superlattice filters [20]. The lowest defect density achieved is on the order of 10^6 cm^{-2} which is still significantly higher compared to films grown on native substrates. The thick buffer and filter layers also make it difficult to couple light to a silicon waveguide. In summary, monolithic integration approach is promising for future large-scale laser integration but is still at an early stage.

1.3.2 Heterogeneous Integration

An alternative method to add gain based on III-V materials to silicon is based on heterogeneous integration of bare III-V chips through wafer bonding and the subsequent co-fabrication of these materials to form laser structures [26] [27]. As shown in Fig. 1.3, the light in the active region of the III-V layer is evanescently coupled to the silicon waveguide. Depending on the material between the III–V wafer and the silicon waveg-

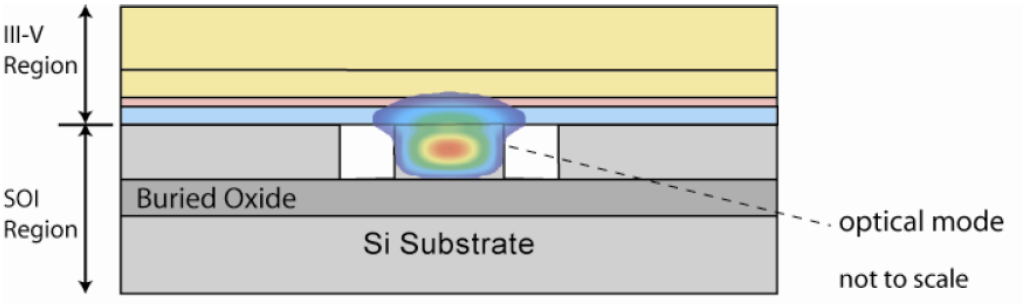


Figure 1.3: 2D schematic of wafer bonding approach [28].

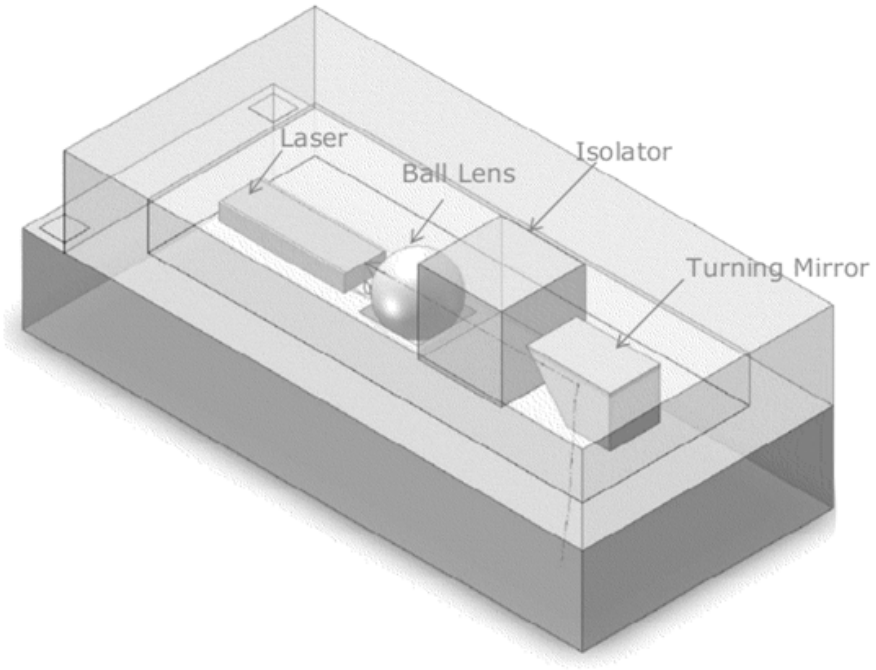
uide, two types of bonding have been demonstrated; molecular and adhesive. Molecular bonding utilizes a thin layer of oxide between the silicon waveguide and III-V wafer to form the molecular bond. The surface of the silicon chip needs to be flat and extremely clean. A chemical-mechanical polishing (CMP) is usually required for the silicon wafer before bonding. Adhesive bonding leverages a layer of polymer such as Benzocyclobutene (BCB) to form the bond between a silicon waveguide and III-V chips. In this case, the strict surface roughness requirement is relaxed. However, the polymer is usually not CMOS compatible and has a low thermal conductivity. Therefore, the molecular bonding approach is the most commonly used method for heterogeneous integration. The gain material can be bonded on top of the silicon wafer in the form of discrete die (instead of a whole wafer) to be efficient with the material. Individual die may come from different substrates to address various device performance requirements for lasers, mod-

ulators and photodetectors. This feature is particularly promising for PIC applications in which integration of multiple optical functions is required. The heterogeneous integration technique has yielded a host of novel active PICs on silicon [29] [30] and has been commercialized [31]. The heterogeneous integration approach is ideal for medium- to large-scale laser integration for SiPh, but a few challenges need to be addressed. First, the cost of the lasers and PICs made by heterogeneous integration are still higher than those on native substrates. This situation could change if the volume of lasers made with heterogeneous integration is significantly increased. Second, when the InP gain material is bonded on silicon on insulator (SOI) wafer, the gain medium is thermally isolated from the substrate by the buried oxide (BOX), resulting in high thermal impedance for the hybrid lasers. Therefore, these lasers do not dissipate heat effectively, limiting their efficiency and performance at high temperature. Finally, III-V alloys and silicon exhibit different coefficients of thermal expansion, therefore, reliability is a concern for devices realized by directly stacking these materials. Ultimately, much effort has been devoted to address these challenges [32] and heterogeneous integration will continue to play an important role in the medium- to large-scale SiPh PICs before practical monolithic lasers are matured.

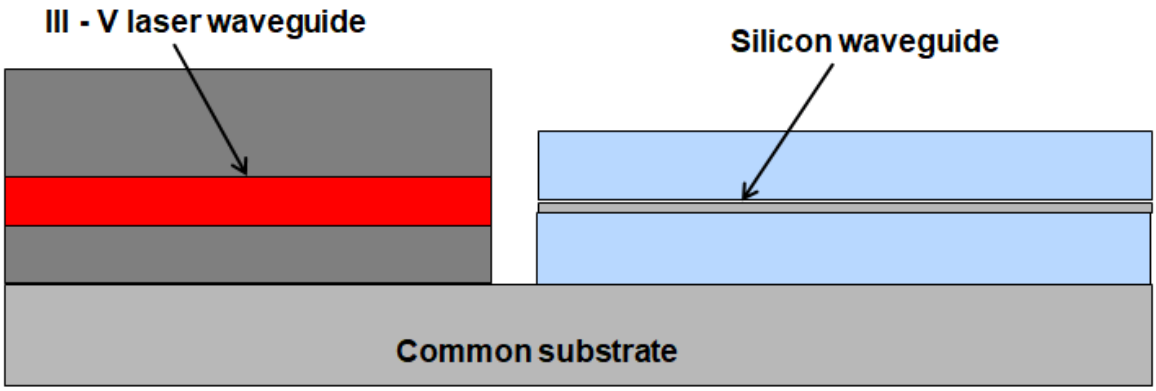
1.3.3 Co-Packaging and Butt Coupling

Although much progress has been made toward integrated lasers on silicon, the technology is still not mature enough for high yield and low cost. Intel has delivered transceivers with SiPh integrated lasers based on heterogeneous integration, but only in limited volumes. Current mainstream transmitters made by SiPh generally rely on externally integrated laser sources. Those sources are based primarily on III-V laser diodes, which can be integrated with the SiPh PICs [33].Figure 1.4(a) and (b) shows the

concept of co-packing and butt coupling. Diverse methods have been proposed to couple



(a)



(b)

Figure 1.4: (a) 3D schematic of co-packing [34]. (b) 2D schematic of butt coupling.

light from external laser diodes into SiPh waveguides. The first approach generally leverages micro-assembled systems in which discrete optical components, such as ball lenses, prisms, and mirrors, are co-packaged with the laser diode and SiPh chip. By using an integrated grating coupler on silicon, this approach offers a near-vertical coupling between a laser diode and a surface grating coupler formed in the SOI layer [35]. It has been used in several commercially successful products based on SiPh [36]. Another possibility is to use butt-coupling to directly couple light from the edge facet of a laser diode to the silicon waveguide. The mode profiles of the laser waveguide and the silicon waveguide have a significant mismatch, which could present large coupling loss and lower yield due the sensitive alignment process. To accommodate the mode mismatch between the output of the laser waveguide and the input of silicon waveguide, several methods have been proposed. A thin silicon device layer is used with a thick silicon dioxide cladding to create an expanded fiber-like optical mode for the silicon waveguide [37]. SOI wafers with much thicker silicon device layers (3μm-thick) can also be used for better matching [38]. The other approach based on advanced edge couplers or advanced alignment techniques have also been explored for external laser coupling to SiPh chips [39] [40]. Although an external laser offers a short-term light source solution for most commercial transceivers made with SiPh technology, it also presents several inconveniences. First, the solution based on the discrete optical components does not leverage the small-footprint feature of SiPh. Transceivers made with this approach are cumbersome and have limited scalability. Second, the butt-coupling scheme still suffers from a significant mode mismatch, which leads to non-negligible optical coupling loss between the lasers and SiPh chips. These losses result in a need to increase power from the lasers, raising the overall power consumption. The misalignment limitation for –1 dB additional coupling loss is generally below 1 μm. Bonding and assembling processes with this precision are time-consuming and the corresponding tools are costly.

1.4 3D Hybrid Integration for Silicon Photonics

1.4.1 Concept

In this thesis a novel 3D hybrid integration technique for SiPh, that addresses the aspects of thermal performance and alignment tolerance, was proposed and demonstrated for the first time, as shown in Fig 1.5. This approach is based on flip-chip integration of an InP reflective semiconductor optical amplifier (RSOA) containing total internal reflection (TIR) turning mirrors. Light is coupled to SOI through surface grating couplers.This technology demonstrates increased alignment tolerance compared to butt coupling. 3D hybrid integration also allows the processed lasers or InP PICs to be bonded directly to the SiPh chip for interposer applications. Using the 3D hybrid integration technique, a silicon photonic external cavity laser (SPECL) featuring narrowed laser linewidth, tunability and improved relative intensity noise (RIN) is also realized.

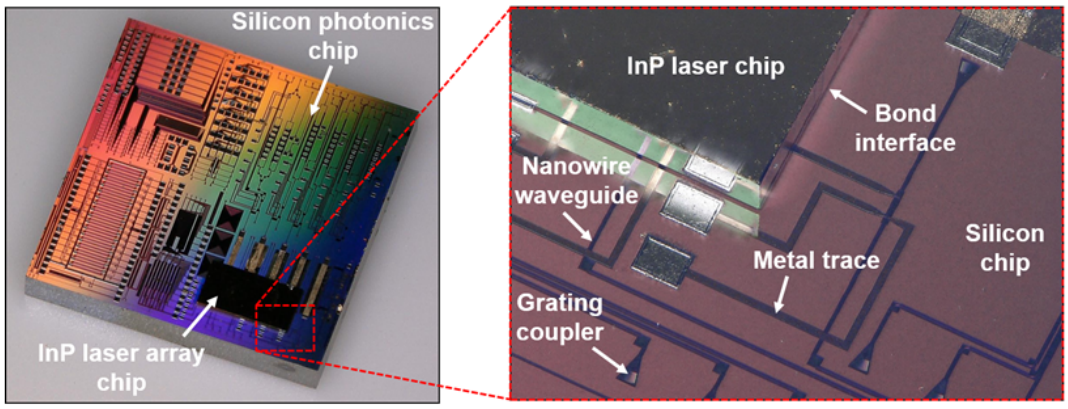


Figure 1.5: Tunable SiPh laser array demonstrated by 3D hybrid integration.

A side view illustration of the 3D integrated coupling structure is shown in Fig. 1.6. The RSOA structure consists of an indium gallium arsenide phosphide (InGaAsP) active waveguide with InP cladding layers. An anti-reflection (AR) coating was applied to the emitting surface of the RSOA to reduce unwanted reflections. The TIR turning mirror

angle was optimized for high coupling efficiency to the silicon waveguide. The light propagating in the RSOA waveguide is redirected vertically by the turning mirror and then exits the InP chip and couples into the silicon waveguide via the grating coupler.

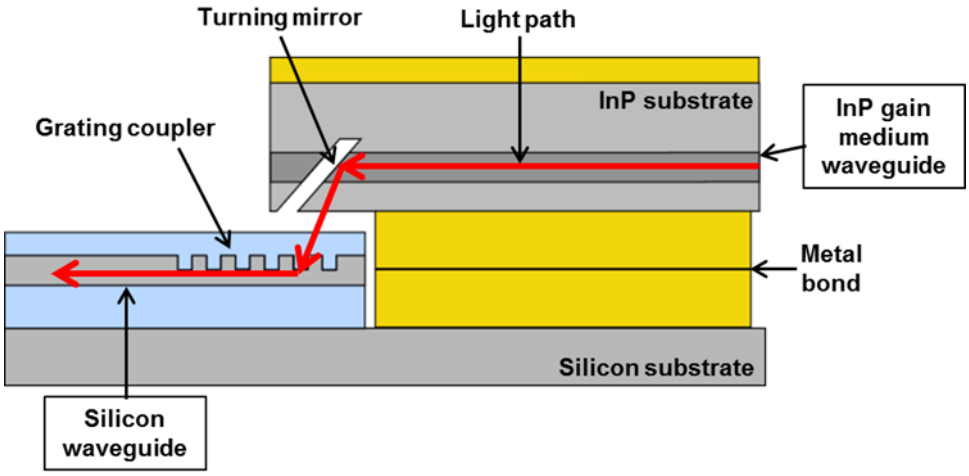


Figure 1.6: Sideview schematic of the 3D integrated hybrid integration.

1.4.2 Hybrid Integration Types

Three types of 3D hybrid integrated lasers have been investigated. Figure 1.7 illustrates the perspective view of a type A 3D hybrid laser. An InP RSOA array is integrated with an active SiPh chip with modulators and photodetectors to realize a multi-channel hybrid transceiver. The light modulation and detection functions can be realized using SiPh modulators and germanium on silicon photodiodes. In this case, the design and fabrication complexity are pushed to the SiPh chip. To create the laser cavity, one mirror is realized on the silicon waveguide using on-chip reflectors, such as Sagnac mirror or DBR waveguide mirror. A high relectivity (HR) coating applied on the backend of the InP waveguide can be used as the second mirror to close the laser cavity. The advantage of the type A approach is high yield because reducing the complexity of the InP processes can increase the overall fabrication yield of the hybrid integrated devices.

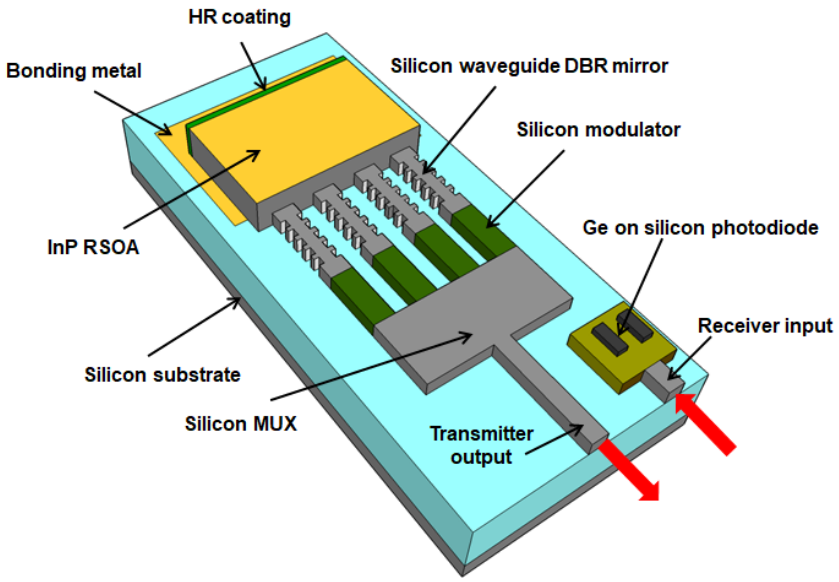


Figure 1.7: Type A hybrid transceiver realized with 3D hybrid integration of InP RSOA array integrated on fully active SiPh chip.

Figure 1.8 illustrates the perspective view of a type B 3D hybrid integration. A multi-channel hybrid transceiver is realized by integrating an InP laser array with an active SiPh chip with modulators and Ge photodetectors. In this case, the complexity for the InP is increased. Subwavelength gratings are used on the InP lasers for single wavelength operation. The grating coupler on the SiPh chip is used as an interface between the InP and the SiPh device. The design and fabrication complexity of the SiPh chips are identical compare to type A. However, the overall design process could be simplified because the external cavity silicon lasers are not as commonly used as InP lasers, and this approach removes the coupling loss within the laser cavity.

Figure 1.9 illustrates the perspective view of a type C 3D hybrid integration. A fully fabricated InP PIC is coupled to a SiPh chip to realize a multi-channel transceiver. The light modulation and detection functions are realized using InP modulators and hybrid integrated InP photodiodes on silicon. In this case, the fabrication complexity for the InP device increases dramatically. To integrate modulators with lasers monolithically, active-

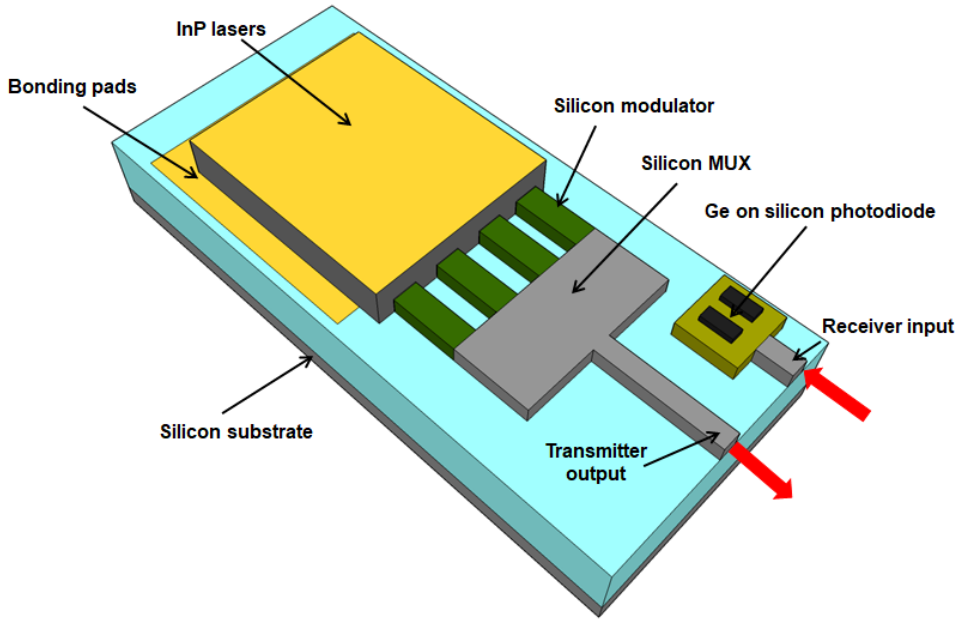


Figure 1.8: Type B 3D hybrid integration with InP lasers integrated on fully active SiPh chip to realize a multi-channel hybrid transceiver.

passive integration is required. The yield of InP PICs is lower than that of standalone lasers or RSOAs. Despite this, there are some advantages. First, the modulators and photodiodes on InP demonstrate superior performance in terms of power consumption and efficiency. Second, the SiPh chip used for type C 3D hybrid integration can be made with all passive components. The silicon chip here is used only for wavelength multiplexing or a low-cost interposer platform, where lasers and fully fabricated InP and SiPh PICs could be integrated together to form a large multi-function system. This strategy benefits from both the InP and SiPh platforms to achieve the most flexibility and functionality.

1.4.3 Thermal Advantages of 3D Hybrid Integration

As shown in Fig. 1.10, the InP chip can be flip-chip bonded p-side (epi-side) down on the silicon substrate, allowing for efficient heat removal from the active medium. A

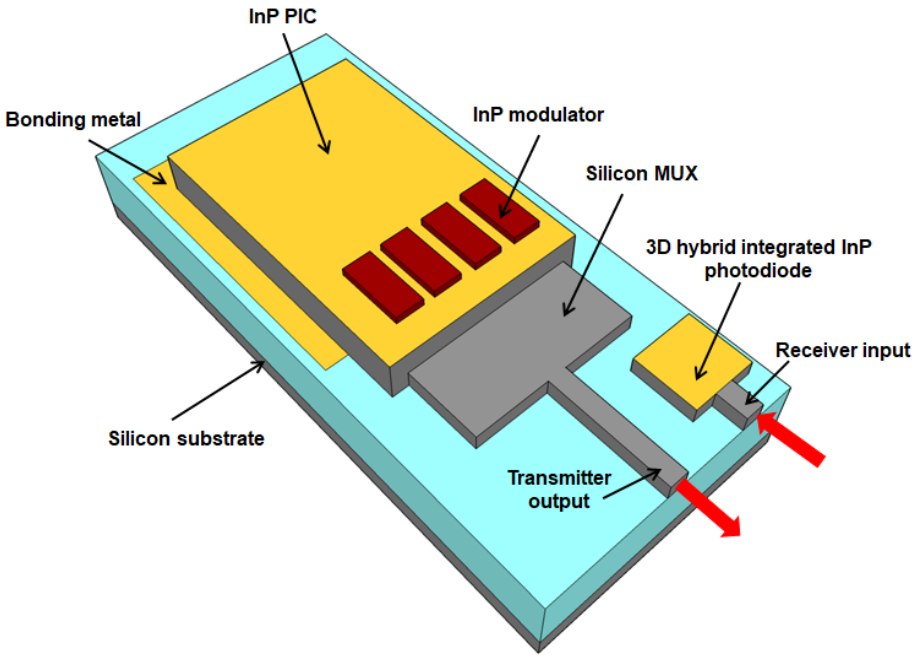


Figure 1.9: Type C 3D hybrid integration with InP externally modulated laser array integrated on passive SiPh chip.

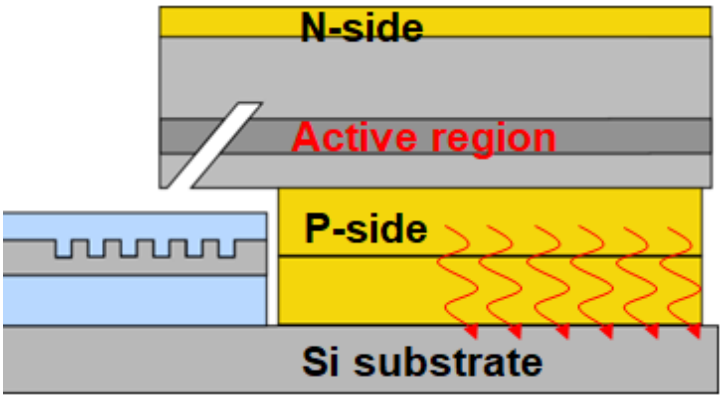


Figure 1.10: Illstration of thermal advantage of 3D integrated hybrid lasers.

shorter path for heat dissipation is realized in this way. For conventional InP ridge lasers or SOA devices, the active region (the major heat source) is within 2 μm of the p-type contact. The thickness between the n-type contact and active region, on the other hand, typically greater than 100 μm. Flip-chip bonding the InP chip p-side therefore provides significant improvement. down to the silicon substrate creates a shorter path for heat dissipation for the active region of the hybrid laser.The higher thermal conductivity of the silicon also provides better heat spreading. The thermal conductivity of silicon is 1.3 W/cm·k, which is approximately 10 times larger than that of silicon dioxide. In comparison to InP, silicon also demonstrates a 50% higher thermal conductivity [41]. Because of this, the overall thermal performance of the 3D hybrid lasers is better than that of lasers fabricated on native InP substrates. Finally, the 3D hybrid silicon integration technology relies on the metal bond to form the mechanical and electrical connection. For heterogeneous integration, the InP and silicon wafer are combined through molecular bonding to SOI layers beneath the laser active region. The BOX acts as a barrier. As a result, the heat generated in the active region of the hybrid laser cannot dissipate efficiently and remmains trapped in the InP. For 3D hybrid integration, the metal bond pad can be fabricated in a recess on the SOI wafer that thermally connects the active region of the laser directly to the silicon substrate, thereby dissipate heat efficiently.

1.4.4 Volume Production Perspective

The 3D hybrid integration approach embodies several features that make it promising for silicon laser integration in volume production. As illustrated in Fig. 1.11, the integration is based on mature IC assembly technology that is characteristic of low cost and high thoughtput. The 3D hybrid integration process can be directly transferred to production-level flip-chip bonding tools. The integration can also be carried out at

wafer level, meaning that InP chips can be attached within dies of a full SiPh wafer. Also, the 3D hybrid integration is carried out as a back-end process. That is, the InP gain or laser chips and the silicon wafer are fabricated and screened seperately before attachment, avoiding co-fabrication of these materials; InP and silicon are incompatible materials and co-fabrication requires significant investment and development. The metal used for bonding for 3D hybrid integration also alleviates the thermal expansion coefficient mismatch between the InP and silicon.

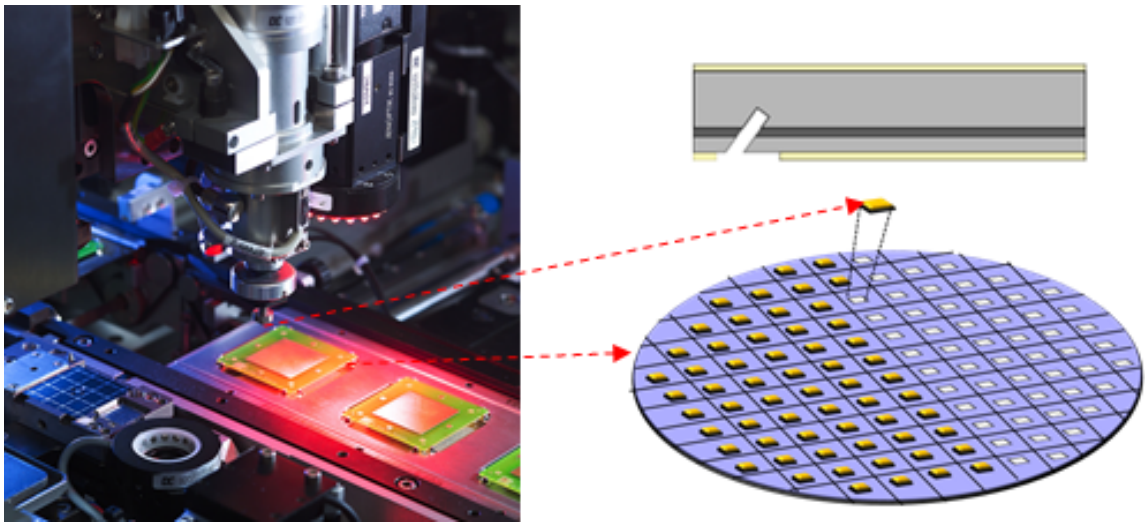


Figure 1.11: Wafer-scale 3D hybrid laser integration.

The 3D hybrid integration approach is as scalable as any other laser integration technique. Fig. 1.12 shows a 3D schematic of an array of four lasers integrated on a SiPh chip. In addition to laser and SOA chips, the 3D integration approach also enables the integration of fully fabricated InP PICs on SiPh chips for large-scale photonics-electronics integration.

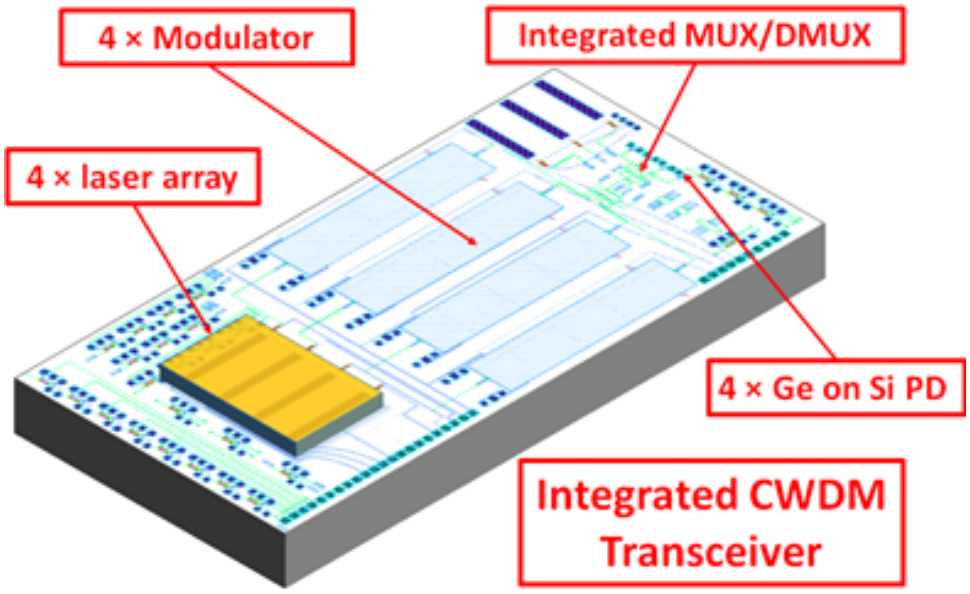


Figure 1.12: 3D schematic of multi-channel transceiver showing the scalability of the 3D hybrid integration approach

1.5 Thesis Overview

This dissertation focuses on the development of the 3D hybrid integration platform to realize electrically pumped lasers on silicon. In this chapter, a high-level review of PICs and integrated lasers for SiPh is presented. Then, the concept of the novel 3D hybrid integration approach is proposed and detailed. InP RSOA design is discussed in chapter 2 with emphasis on surface emission and dilute waveguide realization for higher coupling efficiency and alignment tolerance. Chapter 3 presents the design and simulation of the silicon grating coupler for coupling light from the InP RSOA into the silicon waveguide. Chapter 4 describes the InP device fabrication processes including TIR mirror fabrication, InP RSOA fabrication and InP PIC fabrication. In chapter 5, the fabrication of SiPh devices is introduced discribing the SiPh MPW processes and passive SiPh chip fabrication using electron beam lithography (EBL). Chapter 6 focuses on the flip-chip bonding process with emphasizes on self-alignment technology

and CMOS compatible metallization processes for the InP device. The measurement results are presented in chapter 7 covering the device performance of 3D hybrid lasers and InP device characterization. The summary of this work is given in chapter 8 with insight proposed for the future development of the 3D hybrid laser integration.

Chapter 2

Reflective Semiconductor Optical Amplifier

Due to its indirect band structure, silicon is a poor candidate to realize photon emission and amplification, which are necessary to form lasers [42]. Even though silicon is not suited for creating efficient light sources, researchers have investigated all silicon lasers. An optically pumped silicon laser in continuous operation based on Raman scattering was reported [43]. However, Raman scattering requires an external signal and pump laser to operate, which limits practical applications. Another option is using Ge on silicon as a gain material. Ge is commonly used in CMOS processing to build photodiodes in SiPh chips. A proposed compromise was to use limited tensile strain and free electrons brought by heavy n-doping to fill the indirect bandgap valley to increase the probability of occupation of the direct bandgap valley by injected carriers. However, results on Ge lasers have been limited and reliable performance has not been demonstrated [44].

For most on SiPh applications, the realization of light emission and amplification relies on compound semiconductors a with direct bandgap such as InP or GaAs. In this chapter, the design and simulation of conventional and dilute waveguide RSOAs are

presented. Section 2.1 reviews the ridge waveguide structure of InP ridge lasers. Next, the design and simulation of conventional waveguide RSOAs with surface emission are provided in section 2.2. Dilute waveguide RSOAs for alignment tolerant 3D hybrid silicon photonics integration are designed and analyzed in section 2.3.

2.1 Indium Phosphide Ridge Waveguide

Numerous methods of lateral confinement of current, carriers, and photons have been used to make optical amplifiers or lasers on InP material platforms [45]. Figure 2.1 illustrates the cross-section schematics of three different types of lateral InP waveguide structures and waveguide mode simulation results. These are generic lateral ridges, which will be described below: shallow surface ridges, deep surface ridges, and buried heterostructures. In this work, surface ridge RSOAs are used for fabrication simplicity and high yield.

2.1.1 Surface Ridge

Figure 2.1(a) illustrates a surface ridge waveguide and the corresponding optical mode. The ridge provides current confinement and weak optical confinement. The fabrication of the shallow waveguide involves wet etching, which provides an atomic-level smooth etched surface for low optical loss. The active core layers, usually containing quantum wells or indium gallium arsenide phosphide (InGaAsP) quaternaries, serve as a wet etch stop for the InP ridge fabrication. The carriers are not confined laterally in the core, as they are free to diffuse laterally and recombine without contributing to the gain. The ridge structure has been a popular choice because of its simplicity of fabrication. Due to the weak optical confinement, the surface ridge only allows for relatively large-radius waveguide bends. For sharper bends, a stronger lateral index step is needed.

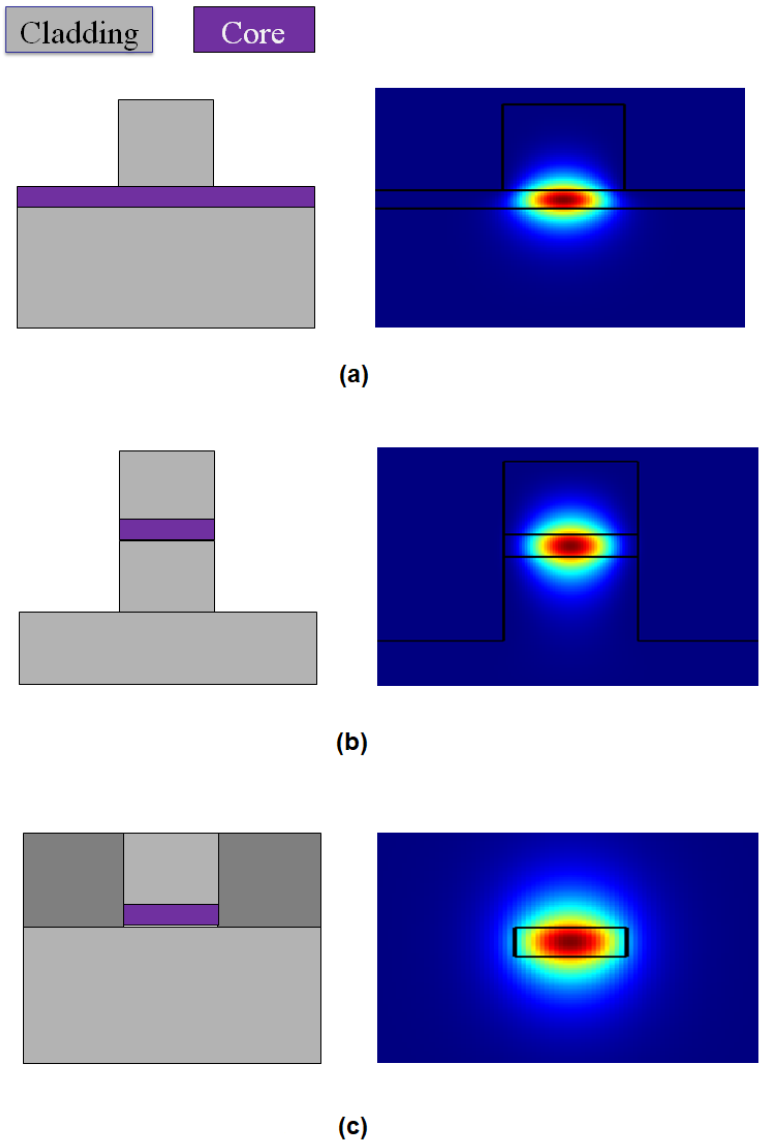


Figure 2.1: Lateral InP waveguide structures (left) and optical mode profile (right) for (a) shallow surface ridge, (b) deep surface ridge and (c) buried heterostructure.

2.1.2 Deep Ridge

Figure 2.1 (b) shows a deep ridge waveguide that provides strong lateral confinement of photons, carriers, and current. It provides smaller waveguide bends. In this case, however, it is important that the sidewalls be formed very smoothly to limit optical losses and to reduce the non-radiative recombination of carriers at the surface of the active region. The deep ridge waveguide will also need to be narrower than the surface ridge to support a single lateral optical mode. Thus, it may be more difficult to couple light in and out (to a single mode fiber) because of the resulting large diffraction angle when the lights exits the waveguide. The thermal impedance will also be higher for the deep ridge waveguide laser because of the narrowed contact area to the substrate.

2.1.3 Buried Heterostructure

Figure 2.1 (c) shows the cross-section of a buried-heterostructure waveguide. The narrowed active region is cladded by a higher-bandgap; low refractive index semiconductor material. This cladding is often made of semi-insulating semiconductors so that the current can flow only through the active region. The carriers and photons are confined laterally as well as transversely. If a semi-insulating substrate is used, parasitic capacitance from the p-n junctions at the buried layers can be eliminated. This structure beneficial for high-speed devices.

2.2 Surface Emission Active Device

2.2.1 Surface Emission Laser

Surface-emitting lasers (SELs) are advantageous over edge-emitting devices for photonic integration. Surface emission is attractive for wafer-level testing and packaging.

The fabricated devices can be tested with an automatic probing station without cleaving, which saves on cost of packaging and increases yield. So far, the vertical-cavity surface-emitting laser (VCSEL) is the most efficient solution for SEL. However, VCSELs for longer wavelengths, typically greater than 1.1 μm, are difficult to fabricate due the challenge of growing high-reflectivity and highly conductive mirrors [46][47]. VCSELs emitting at 1.55 μm are reported using micro-electro-mechanical technology with limited stability and high cost [48].

Novel surface emission InP lasers have been reported in [49]. The idea is to convert a ridge laser or SOA into surface emitting device by integrating a 45° mirror at the end of the active waveguide. The light in the waveguide is redirected at the turning mirror and emitted vertically from the chip surface. The dry-etched angled facet was achieved by reactive-ion etching (RIE) where the sample was mounted on an angled holder and loaded into the RIE chamber to achieve angled etching. In [50], a facet-free surface emitting distributed feedback (DFB) was fabricated. A similar integrated 45° total internal reflection (TIR) mirror was used in this work. However, the light was redirected toward the InP substrate. The beam exited the surface through an integrated lens for beam collimation. It is reported that light can be redirected off the optical axis of the waveguide by using integrated gratings. This method has been realized in [51]. The idea was to use the waveguide grating on the InP to bend the in-axis light by a few degrees off the optical axis of the waveguide. After the light reached the cleaved facet of the InP chip, it would be redirected down towards due to refraction. The RSOA used in this work is similar to the one reported in [52] where a horizontal cavity SEL was proposed with light emitting from the p-cladding surface of the device.

2.2.2 Surface Emission Reflective Semiconductor Optical Amplifier

Figure 2.2 shows a 2D schematic of a surface-emission RSOA. It has a horizontal cavity with a ridge waveguide in conjunction with a vertical etched facet on the back side with HR coating. A dry etched 48° TIR mirror is integrated at the other end of the waveguide for surface emission. The redirected light exits the chip from the p-cladding side through an AR coated surface.

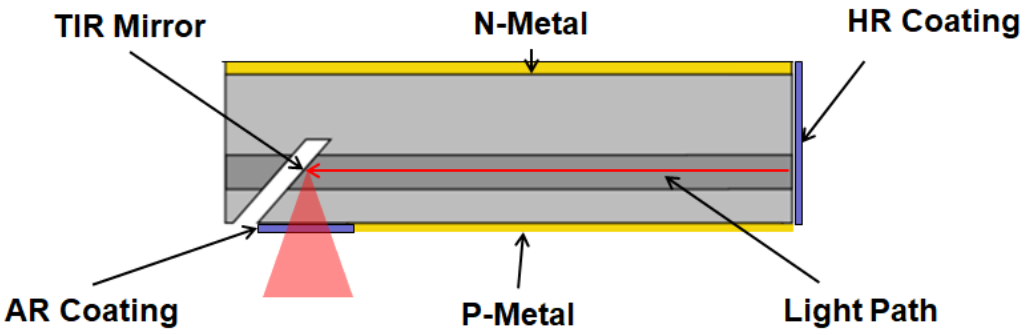


Figure 2.2: 2D schematic of surface emission RSOA.

The mode evolution and light coupling process can be simulated using the finite-difference time-domain method (FDTD). A fundamental transverse electric (TE) mode was launched into the InP waveguide of the RSOA. As shown in Fig. 2.3, the horizontally propagating waveguide mode reaches the turning mirror and is then redirected vertically through total internal reflection. The beam eventually exits the InP chip. A power monitor was used to collect all the light from exiting the surface.

To prevent the ridge structure from interfering with the beam upon out-coupling, the end of the waveguide of the RSOA was terminated with a rapid taper to create a quasi-free space region. The top view schematic of surface ridge structures with and without the rapid taper are shown in Fig 2.4 (a) and (b), respectively. 3D FDTD simulations were

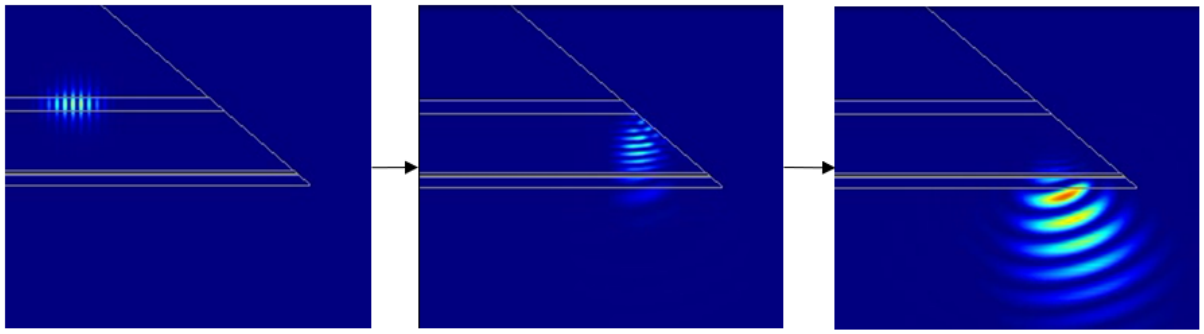


Figure 2.3: Screen shots of mode evolution and light coupling process for surface emitting RSOA.

used to estimate the surface emitting beam shape from both structures. The captured beam shape of the output light with/without rapid taper were shown in Fig 2.4 (c) and (d) respectively. Without the rapid taper the far field beam split into two parts due the interference with ridge after exiting the chip. The disturbed beam will have negative effects on the coupling process to the silicon grating coupler.

2.3 Dilute Waveguide Reflective Semiconductor Optical Amplifier

2.3.1 Overview

The mode profile of an optical fiber and an InP laser waveguide have significant differences. These differences increase the complexity of packaging and optical coupling. Laser waveguide with an expanded mode size are therefore attractive for low cost laser packaging with increased alignment tolerance. The expanded mode leads to slow divergence beam emission from the waveguide. This beam couples more efficiently to optical fiber or grating coupler.

The idea of using the expanded waveguide mode to increase coupling efficiency can

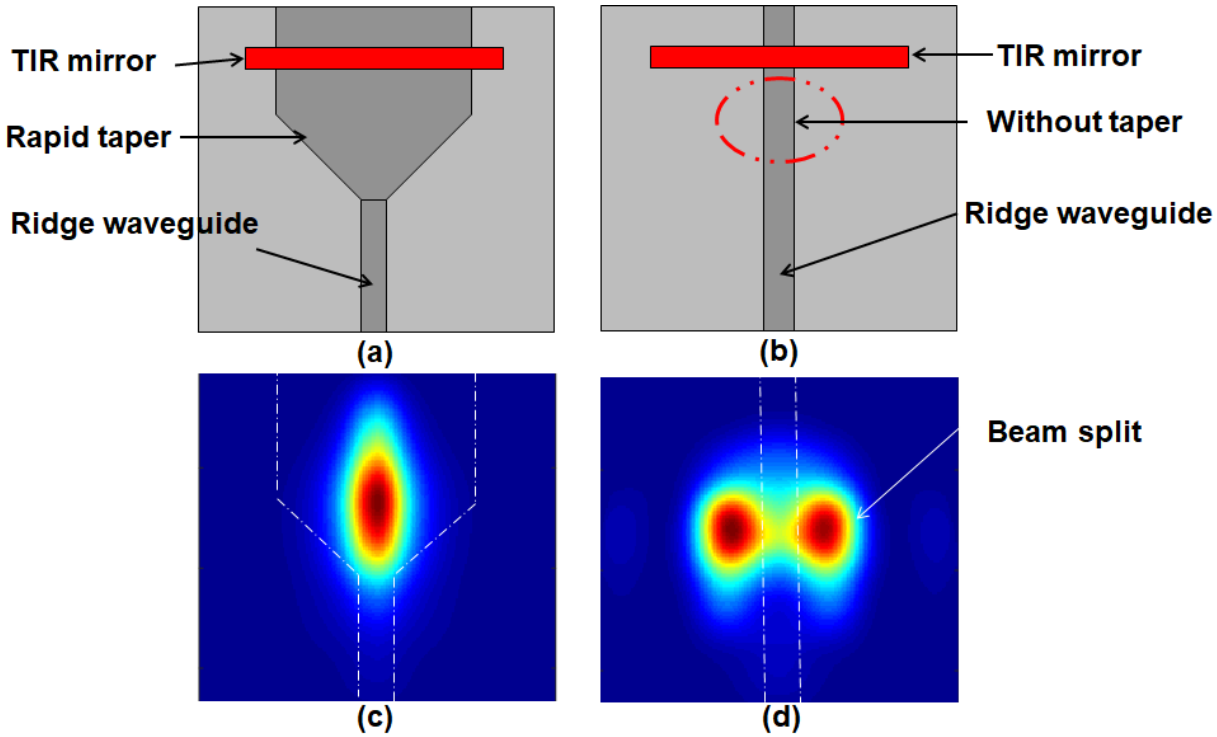


Figure 2.4: Top view schematic of surface ridge structures with (a) and without (b) rapid taper. Beam shape of the output light with (c) and without (d) rapid taper. The white dished lines indicate the corresponding ridge structure.

be applied to the 3D hybrid laser integration. In this section, a simplified version of a dilute waveguide RSOA is designed and analyzed. The mode conversion is based on a spot-size converter fabricated with a tapered InP ridge. The RSOA design was based on a conventional shallow ridge waveguide structure.

2.3.2 Dilute Mode Waveguide

2D cross-section of a passive conventional waveguide and a dilute mode waveguide are shown in Fig. 2.5(a) and (c), respectively. For the conventional waveguide, the waveguide core layer thickness is 0.4 μm. For the dilute waveguide, the waveguide core layer thickness is 5 μm. The conventional and dilute waveguide are based on the surface ridge structure. The waveguide core material is InGaAsP, which is used as a wet etch stop layer during InP ridge fabrication. Using Eigenmode expansion (EME) method, the mode profile as well as the mode area can be obtained. The ridge thickness used for both waveguides is 1.8 μm, however the ridge widths are different. For the conventional waveguide, the ridge width is 2 μm and the fundamental TE mode of the waveguide is shown in Fig. 2.5 (b). The mode size is 1.5 μm^2. For the dilute waveguide, an expanded fundamental TE mode is achieved by narrowing the ridge width to 1.25 μm. The mode simulation for the dilute waveguide is shown in Fig. 2.5(d). The mode size is 85 μm^2. The dilute waveguide mode shown in Fig. 2.5(d) is preferred to increase the alignment tolerance of the 3D hybrid integration process.

2.3.3 Spot Size Converter Integration

In [53], a reduced InP waveguide core was fabricated to expand the optical mode with complex multi-layer vertical tapered structure. Ultra-low insertion loss was achieved, however, high-resolution lithography and multiple regrowths were required for the device

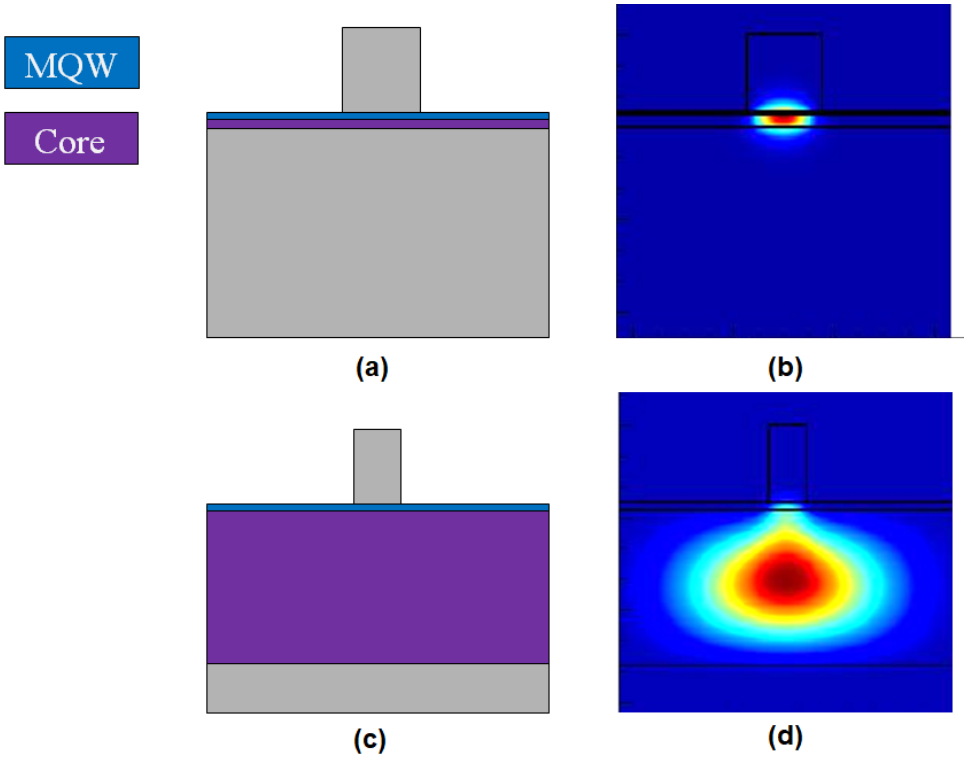


Figure 2.5: Passive InP ridge waveguide of (a) conventional surface ridge waveguide and (b) mode simulation results. (c) Dilute surface ridge waveguide and (d) corresponding mode simulation results.

fabrication which increases the complexity and cost. In this work, a spot-size converter with a simplified fabrication process is described. A similar design can be found in [54] where a thicker (up to 5 μm) InGaAsP waveguide core layer was used. The mode conversion is realized by inversely tapering the ridge waveguide width. As shown in Fig. 2.6(a), the dilute waveguide RSOA contains a wide ridge waveguide region ($\geq$ 4 μm), an inverse taper for a spot-size converter, a narrow ridge waveguide region ($\leq$ 1.25 μm) and a surface emission window region, which is a rapid taper, similar to the one reported in section 2.2.2. The mode simulation for a wide ridge waveguide region and a narrow ridge waveguide are shown in Fig. 2.6(b). Before the inverse taper, the optical mode is compact. The inverse taper serves as a spot-size converter that converts the compact mode into an expanded mode.

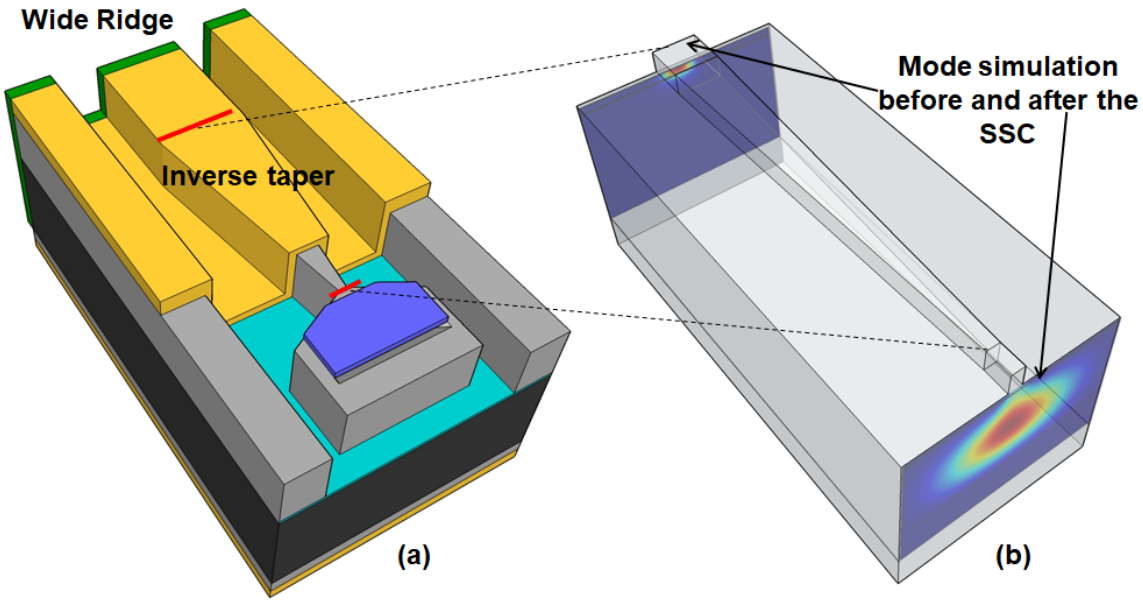


Figure 2.6: (a) Dilute RSOA design with integrated spot-size converter. (b) The mode simulation before and after the spot-size converter illustrating the mode expansion process

The length of the inverse taper needs to be chosen carefully to achieve efficient mode conversion with low insertion loss. The insertion loss with respect to the length of the

inverse taper can be estimated using the EME method [55]. Figure 2.7 shows the optical loss of a taper in which the width is tapered from 6 μm to 1.25 μm. The insertion loss given by EME simulations does not include the scattering loss introduced by waveguide roughness. The insertion loss may increase with enlarged taper length. The simulation shows that when the taper is 3 mm long, the insertion loss is approximately 1 dB.

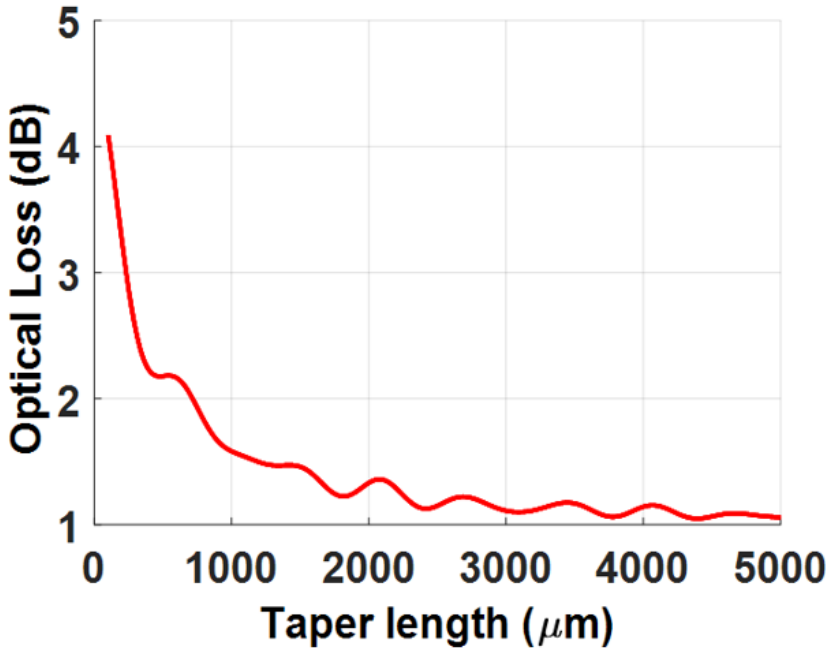


Figure 2.7: Insertion loss of an inverse taper as a spot size converter versus length.

The mode expansion process can be monitored using the eigenmode propagation function [56] that is integrated with the EME solver. This command calculates the resulting output mode profile of an arbitrary input mode after it has propagated through a waveguide structure for some distance. The resulting modes are then added coherently to give the final mode profile. Compared to the FDTD method, Eigenmode propagation is faster and relatively accurate for extra-long propagation simulations such as a taper structure [55]. Figure 2.8(a) and (b) show the simulation results of Eigenmode propagation illustrating a mode conversion process. The inverse taper used in this simulation has a length

of 3 mm. The ridge width was converted from 6 μm to 1.25 μm. Figure 2.8(a) show the mode conversion process along the vertical direction of the dilute waveguide and Fig. 2.8(b) shows the mode conversion process in the horizontal plane.

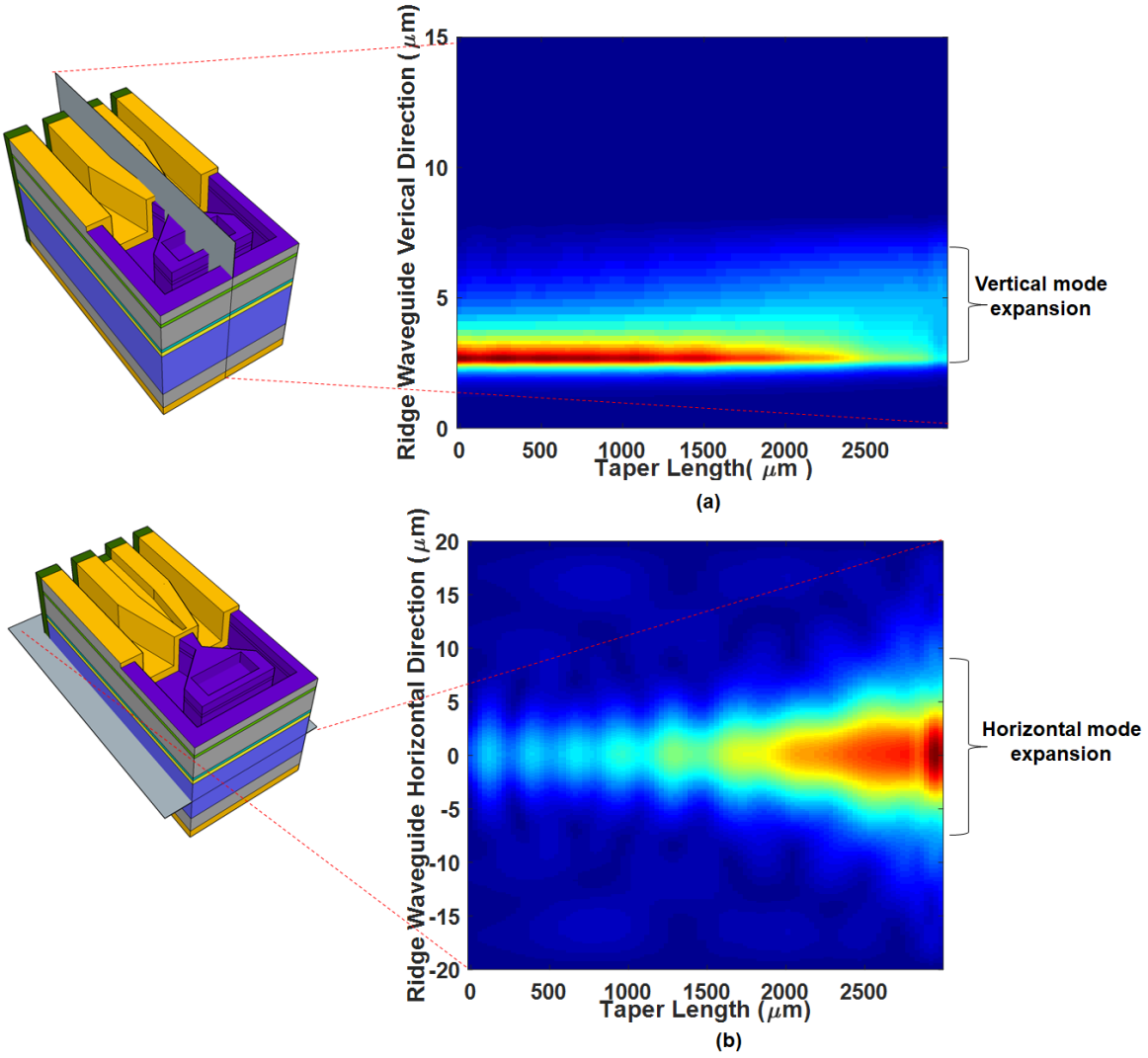


Figure 2.8: Mode conversion along the (a) vertical and (b) horizontal direction of the dilute ridge waveguide.

The interaction between the waveguide mode area and the MQWs region is another important design aspect for the dilute waveguide RSOA. The overlap coefficient (Γ) is defined as the ratio of the MQW area overlap with the entire mode area [1]. As shown

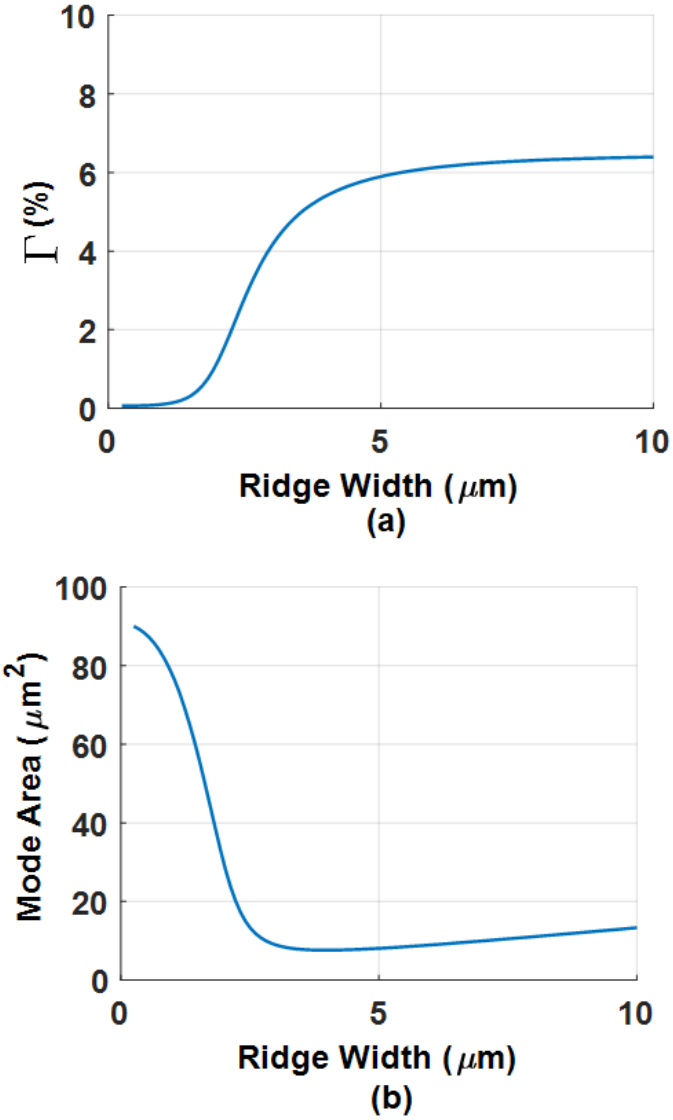


Figure 2.9: (a) Dilute waveguide mode size versus ridge width. (b) Γ versus ridge width for dilute waveguide.

in Fig. 2.9 (a) and (b), the mode size and overlap coefficient (Γ) between optical MQW region varies with the vertical ridge width. Based on the simulation results, when the ridge width is 1.25 μm, the Γ is 0.25 %. This number is too low for efficient lasing. When increasing the ridge width to above 4 μm, the Γ can be as high as 6%. As a result, for a 3D hybrid laser constructed with a dilute waveguide RSOA, the optical gain is mainly provided by the wide ridge waveguide region prior to the inverse taper. The inverse taper contains the MQWs which is also electorally pumped to reduce abortion.

A higher overlap of the MQW region and the waveguide mode is desirable to make an efficient laser. By increasing the width of the InP ridge, the Γ will increase accordingly. However, after the InP ridge is expanded above a certain width (4 μm), the Γ will be saturated as shown in Fig. 2.9(a). To further increase Γ , a InGaAsP quaternary layer with a high refractive index can be incorporated into the epitaxy design above the MQW region. This layer will increase the overall Γ if incorporated properly. Figure 2.10 shows simulation results for Γ as a function of ridge width of the dilute waveguide that contains none, one and two layers of InGaAsP. Based on the simulation, for a certain ridge width, the Γ increase with the number of InGaAsP high refractive index layers that are incorporated into the epitaxy design. This concept allows for achieving a better trade off between laser efficiency and coupling efficiency.

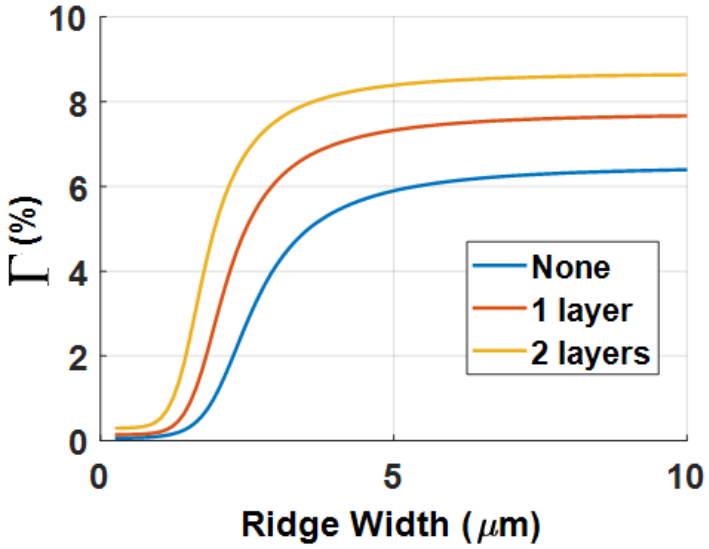


Figure 2.10: Simulation results of the Γ as a function of ridge width of the dilute waveguide that contains none, one and two layers of InGaAsP over the MQWs region.

Chapter 3

Grating Coupler for 3D Hybrid Integration

A material platform with a high index contrast allows for high-density PICs with smaller footprint. SiPh features a sub-micron waveguide core with a strongly confined guided mode. Figure 3.1 shows the optical mode simulation for a single-mode fiber and single-mode SiPh waveguide. The single mode fiber has a core diameter of 9 μm, and the core of the SiPh waveguide is 450 nm wide and 220 nm thick. The significant mode mismatch adds complexity and cost to the SiPh packaging. Advanced edge couplers can be achieved with inverted lateral tapers and a poly-silicon overlay [40] [57]. However, these methods often lead to increased fabrication costs.

The waveguide grating coupler was proposed in [58] to minimize cost and maximize performance for SiPh packaging. In comparison to edge couplers, the waveguide grating coupler is advantageous since it does not require facet polishing or AR coating. The grating coupler can also be placed anywhere on the die. With grating couplers, wafer-scale testing and device screening can be achieved using a highly automated probe station. The surface coupling scheme also allows for dense packaging. Lastly, 2D grating coupler

could be designed to control the polarization of the coupled light [59].

The advantages provided by the silicon grating coupler can be utilized for the 3D hybrid integration platform. The design and simulation of a silicon waveguide grating for coupling light from a surface emitting InP RSOA will be discussed in this chapter. The design consideration are different from fiber grating couplers since the optical beam of the surface emitting RSOA is more divergent than that of a single mode fiber. Section 3.1 introduces basic grating coupler theory, 2D grating coupler modeling and optimization workflow. Section 3.2 describes the design of advanced waveguide grating coupler for coupling efficiency enhancement and alignment tolerance. Section 3.3 presents the alignment tolerance analysis for 3D hybrid integration technology.

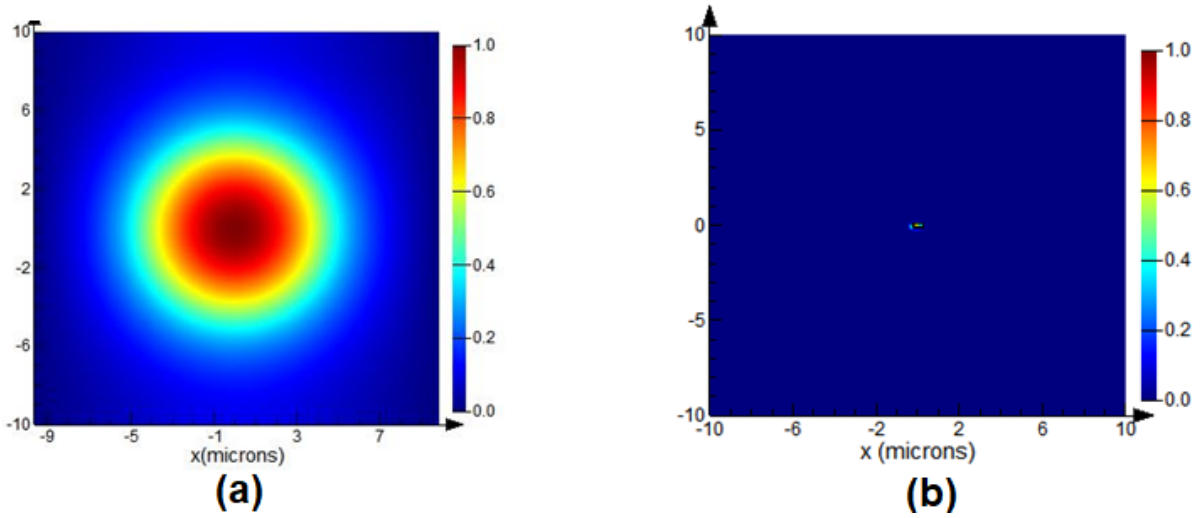


Figure 3.1: Mode simulation results of (a) a single mode fiber and (b) a single mode SiPh waveguide.

3.1 Grating Coupler Design and Optimization

3.1.1 Grating Coupler Theory

A grating coupler is a diffraction grating formed by periodically notching a waveguide. A 2D schematic of a waveguide grating coupler is shown in Fig. 3.2. Light that is diffracted off the grating teeth will constructively interfere at a specific upward angle. The constructive interference condition for a one-dimensional grating can be expressed as:

$$n_{eff} - n_c \cdot cos(\theta) = m \cdot \frac{\lambda}{\Lambda}$$

where n_{eff} denotes the effective refractive index of the waveguide, n_c denotes the refractive index of the top cladding material, θ is the diffraction angle for constructive interference, m is the diffraction order, λ is the target wavelength in free space and Λ is grating pitch. This expression provides a coarse estimation of the grating coupler parameters. To further optimize the grating design, numerical analysis is required.

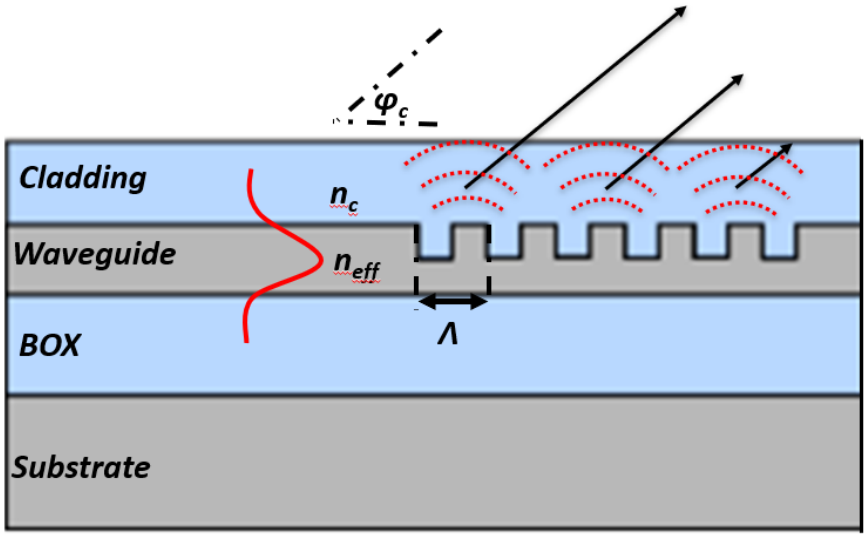


Figure 3.2: 2D schematic of a waveguide grating coupler.

3.1.2 2D Finite-Difference Time-Domain Method

The finite-difference time-domain (FDTD) method [60] is used for modeling light coupling from the surface emission RSOA to the silicon waveguide. The FDTD method is not appropriate for simulating long structures due the large computation workload, but it is ideal for simulating compact integrated photonics component such as grating couplers [61], polarization rotators [62] and SiPh filters [63]. The model was built with a commercially available software, Lumerical FDTD. Figure 3.3(a) shows a 2D schematic of the simulation setup. A conventional waveguide RSOA was coupled to a SiPh chip through a grating coupler. The fundamental TE mode of the RSOA waveguide was injected from the right and normalized so that the input power equals to 1. The mode source injected at the RSOA waveguide had a bandwidth of 100 nm to cover from 1.5 μm to 1.6 μm. The propagation of the optical mode within the entire structure is calculated using FDTD method. The power flux overlaping with the fundamental TE mode of the silicon waveguide will be calculated. The coupling efficiency is defined as the fraction of power overlap in the fundamental TE mode of the silicon waveguide versus to total power injected to the RSOA waveguide. This coupling efficiency is related to a number of parameters including the relative position between the RSOA and the SiPh chip, the turning mirror angle, the grating coupler pitch, top cladding thickness, BOX thickness and total thickness of silicon device layer. To optimize the coupling efficiency with a brute-force search is not feasible when the number of design parameters is greater than three. As a result, a multi-parameter optimization method was used to obtain the optimized design parameters.

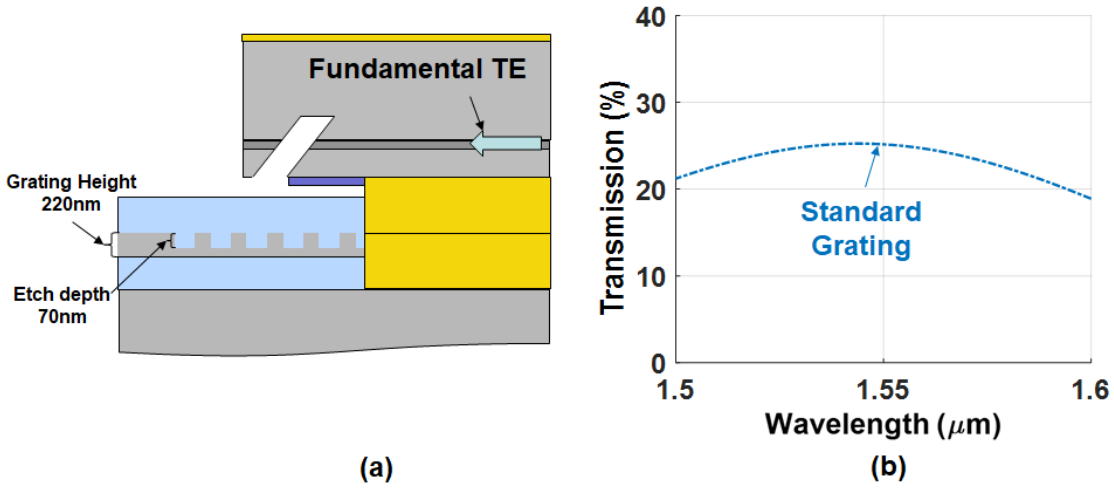


Figure 3.3: (a) 2D FDTD model of 3D hybrid integration with standard grating coupler design (b) 2D FDTD simulation of the coupling efficiency versus wavelength for a conventional RSOA coupling to standard grating coupler.

3.1.3 Particle Swarm Optimization

The multi-parameter optimization method used in this work is particle swarm optimization (PSO) [64]. The figure of merit is maximizing the average coupling efficiency over the wavelength from 1.5 μm to 1.6 μm. The number of parameters to be optimized depends on the technology used for making the grating coupler. If SiPh foundry service is used with an established technology, parameters such as a top oxide cladding, BOX thickness and grating etching depth are fixed. The only design parameters that need to be optimized are grating coupler pitch and filing factor. The rest of the parameters are defined by the foundry technology.

The coupling efficiency is also related to the offset position between the InP RSOA and the grating coupler. In the vertical direction, the highest coupling efficiency can be achieved where the lower surface of the RSOA touches the top cladding of the grating coupler. In the horizontal direction the optimized position could be achieved by sweeping the horizontal offset position between the InP RSOA and grating coupler. At each posi-

tion, the 2D FDTD simulation is used to calculate the corresponding coupling efficiency. The optimized horizontal offset position is the one that generates the highest coupling efficiency. Based on the optimized position, PSO is used to find the ideal grating coupler pitch and fill factor for a certain SiPh technology.

Figure 3.3(b) shows a 2D FDTD simulation result of the coupling efficiency vesus wavelength where a conventional InP RSOA couples to a silicon grating coupler. The grating coupler is based on a 220 nm silicon device layer on a 2 μm BOX. The top oxide cladding is 2.5 μm thick. The etch depth of the grating is 70 nm. This version of grating coupler is considered as the standard grating coupler in this thesis. The maximum coupling efficiency is approximately 25% based on the 2D FDTD simulation at a wavelength of 1.55 μm. This result will be used as a baseline to evaluate the coupling efficiency enhancement achieved with advanced grating coupler implementation.

3.2 Advanced Grating Coupler Design

The maximum coupling efficiency of a uniform pitch grating coupler is limited by two factors. First, in the case of a vertically symmetric grating (by etching completely through the silicon waveguide layer and applying the same top and bottom cladding materials) the diffraction pattern is identical in the top and bottom cladding. As a result, half of the light coming from the surface emission RSOA couples into the silicon substrate. Second, there is a mode mismatch between the optical field from a surface emission RSOA and the grating coupler, which also decreases the coupling efficiency.

The solutions to these problems lead to several advanced grating coupler designs. Different advanced techniques could be used in a single grating coupler design to achieve combined coupling efficiency enhancement. The first principle of advanced grating coupler design is to reduce the grating symmetry in the vertical direction. An elevated

grating coupler, or dual-layer grating coupler are good examples of breaking the vertical symmetry of the grating teeth [65]. To recover the light coupled to the substrate, a reflector made with a DBR mirror under the grating coupler is used, and can double the coupling efficiency [66]. A metal reflector can also be used below the grating coupler for efficiency enhancement [67]. The mode mismatch issue between the optical field from a surface emission RSOA and the grating coupler could be solved by using an apodized grating coupler [68]. In the follow subsections, different tpyes of advanced grating coupler designs are presented with the corresponding 2D FDTD simulation results.

3.2.1 Elevated Grating Coupler

By reducing the etch depth, the asymmetry of the grating structure is increased. However, this comes at the expense of a longer coupling length since the strength of the grating is reduced. To maintain a high grating coupling strength and high asymmetry, a layer of poly crystalline silicon (poly-Si) can be added on top of the silicon device layer. The poly-Si is introduced as an additional degree of freedom to the grating coupler structure, thereby allowing for an optimization of both the directionality and coupling length of the grating coupler. As shown in Fig. 3.4(a), the grating coupler region is elevated compared to the silicon waveguide by the poly-Si deposition. The ploy-Si overlay is CMOS compatible and has been standardized in SiPh foundries such as Interuniversity Microelectronics Centre (IMEC).

In this work, a total thickness of 160 nm poly-Si overlay is deposited on top of the 220 nm silicon device layer to form the elevated grating coupler. After the poly-Si deposition, the grating teeth are fabricated using dry etching. The etch depth is another parameter that will impact the coupling efficiency. Based on the practical swam optimization, the etch depth of 220 nm is chosen. It turns out this etching depth is ideal for both fiber

couplers and grating couplers for hybrid laser integration. As shown in Fig. 3.4(b), the maximum coupling was increased to 35% compared to the standard grating coupler design.

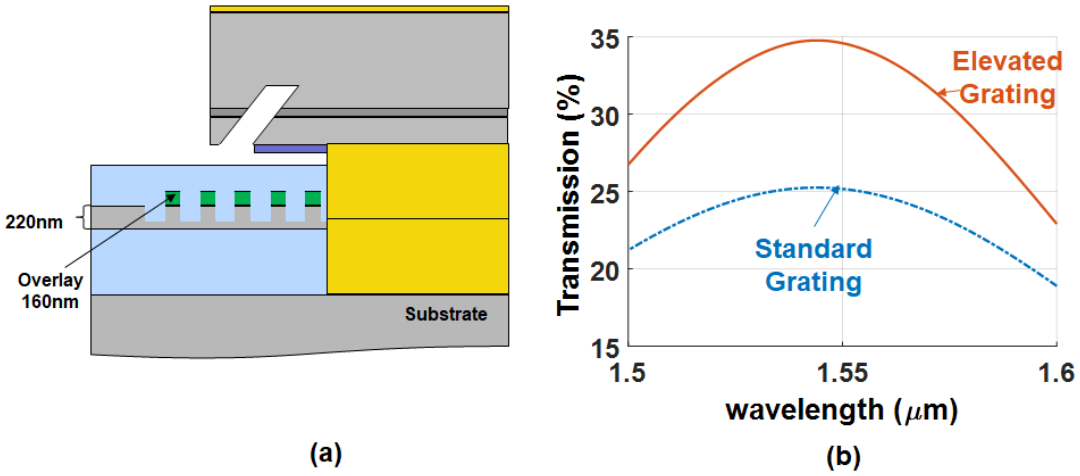


Figure 3.4: (a) Schematic for 2D FDTD simulation model of elevated grating coupler coupled with conventional RSOA. (b) 2D FDTD simulation results of the coupling efficiency versus wavelength for elevated grating coupler coupled with conventional RSOA.

3.2.2 Dual Layer Grating

Silicon nitride waveguides feature low propagation loss, a high nonelinear coefficient and insensitivity to the temperature changes [69]. Silicon nitride waveguides are widely used in the PIC industry. The fabrication of silicon nitride films relies on chemical vapor deposition (CVD). After decades of development, high quality silicon nitride films can be deposited at low temperature with low stress. The silicon nitride deposition process has been integrated into the process flow of SiPh chip fabrication. This silicon nitride waveguide layer is usually inserted on top of silicon waveguide layer for facilitating edge coupling.

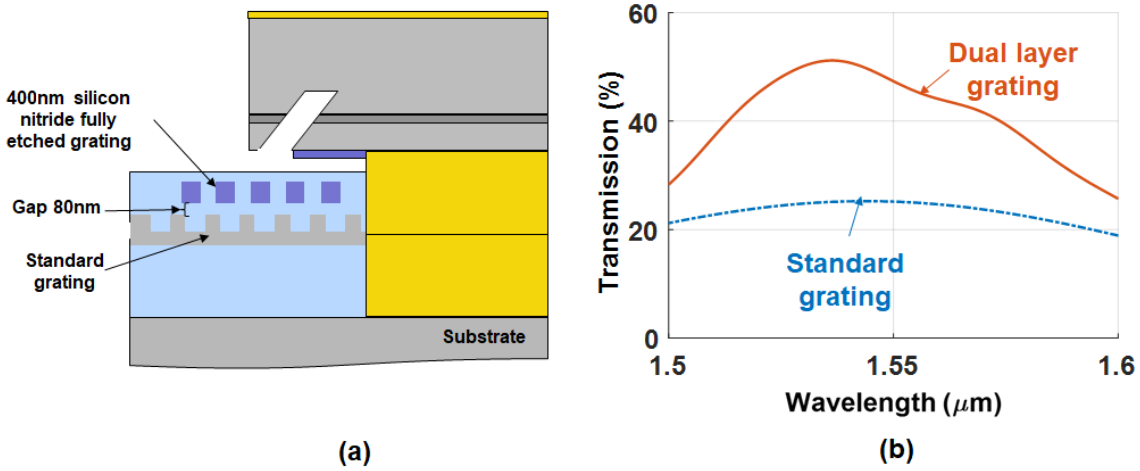


Figure 3.5: (a) Schematic for 2D FDTD simulation model of dual layer grating coupler coupled with conventional RSOA. (b) 2D FDTD simulation results of the coupling efficiency versus wavelength for dual layer grating coupler coupled with conventional RSOA.

A novel grating coupler utilizing both silicon and a silicon nitride layer has been proposed [69]. After silicon waveguide layer fabrication, high quality CVD oxide is deposited. The wafer then undergoes a CMP process to achieve a clean and smooth surface for the silicon nitride layer deposition. The combination of the silicon nitride and silicon device layer breaks the vertical symmetry of the grating structure. The gap between the silicon layer and silicon nitride layer is an important parameter. With proper design of the oxide gap, constructively interfering radiation from different scattering interfaces of the dual layer grating coupler can be achieved to further boost coupling efficiency. A partial-etched grating is used in the design of the silicon grating coupler. Due to the relatively low refractive index contrast between the silicon nitride and silicon dioxide cladding, a fully etched silicon nitride grating is used in order to maximize the grating strength. Thicker silicon nitride layer is also preferred for high coupling strength. Figure 3.5(a) shows the 2D schematic of the dual layer grating coupler. A 400 nm silicon nitride fully etched grating was fabricated over a standard 220 nm silicon grating coupler with

70 nm etch depth. The parameters to be optimized are the pitch and fill factor for both the silicon and silicon nitride grating. With optimized parameters, the coupling efficiency versus wavelength are simulated and the results are shown in Fig. 3.5(b). The maximum coupling efficiency was improved to approximately 50%.

3.2.3 Back Reflector

Due to the symmetric diffraction pattern of the grating coupler, the theoretical maximum coupling efficiency is limited to 50%. A significant amount of light from the RSOA is not coupled into the silicon waveguide but coupled down to the silicon substrate. In order to recover this otherwise lost optical energy, reflectors such as metal or DBR mirrors have been used below the grating coupler layer to boost coupling efficiency.

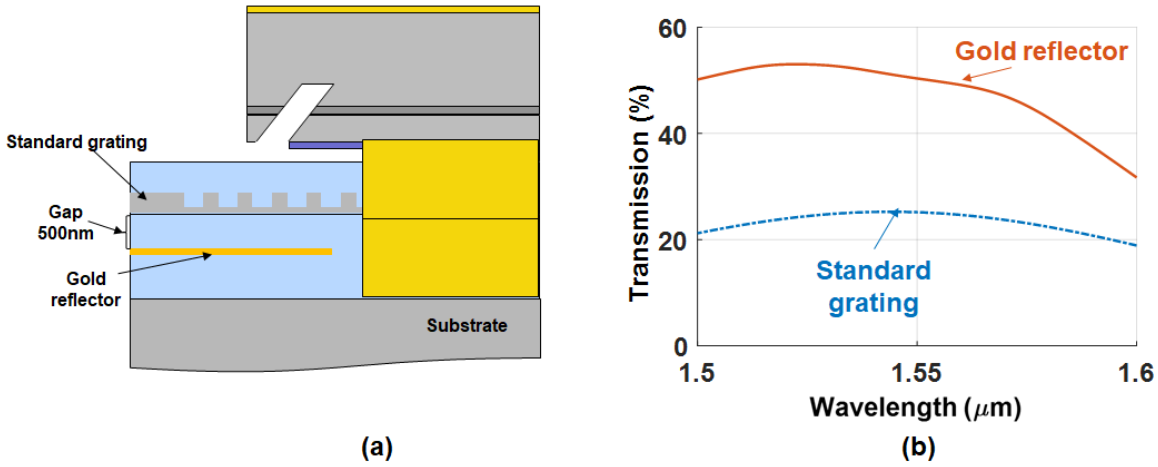


Figure 3.6: (a) 2D schematic of 3D hybrid integration using back reflector below grating coupler. (b) 2D FDTD simulation of the coupling efficiency versus wavelength for grating coupler with back reflector.

In [66], a DBR mirror made by a silicon dioxide and silicon nitride superlattice was used to double the coupling efficiency of a vertical fiber coupler. Aluminum or gold can

alternatively be incorporated beneath the grating layer with back side fabrication [70]. In this work, a layer of 100 nm gold was incorporated beneath the 220 nm grating coupler with 70 nm etch depth. As shown in Fig. 3.6(a), the grating pitch, fill factors and oxide gap between the gold mirror and silicon grating are optimized. The coupling efficiency versus wavelength is simulated and the results are shown in Fig. 3.6(b). The maximum coupling efficiency is achieved is greater than 50%.

3.2.4 Apodized Pitch Grating

The output of the uniform grating coupler has an exponentially decaying power described as

$P = P_0 \exp(-2\alpha z)$, along the propagation direction. α is the coupling strength factor, which is a constant for the uniform grating. For a nonuniform grating, the α can be expressed as a function of z. As a result, the shape of the output beam could be altered to match the beam from the surface emission RSOA. For example, to achieve a Gaussian output beam, $\alpha(z)$ is given by:

$$2\alpha z = \frac{G^2(z)}{1 - \int_0^z G^2(z)\mathrm{d}t}$$

where $G(z)$ is a normalized Gaussian profile.

To achieve this z-dependence of α, either the etch depth or the pitch of the grating can be varied. This equation is valid only for a long grating with small α, which is not the case for the grating coupler used in 3D hybrid integration. Therefore, we use the solution of the above equation as a starting point and perform a further numerical optimization for the grating structure. Figure 3.7 (a) shows the 2D schematic of an apodized grating coupler design using a 220 nm thick silicon waveguide layer with a 70 nm etch depth. As shown in Fig. 3.7(b), the maximum coupling efficiency is 38% for the apodized grating

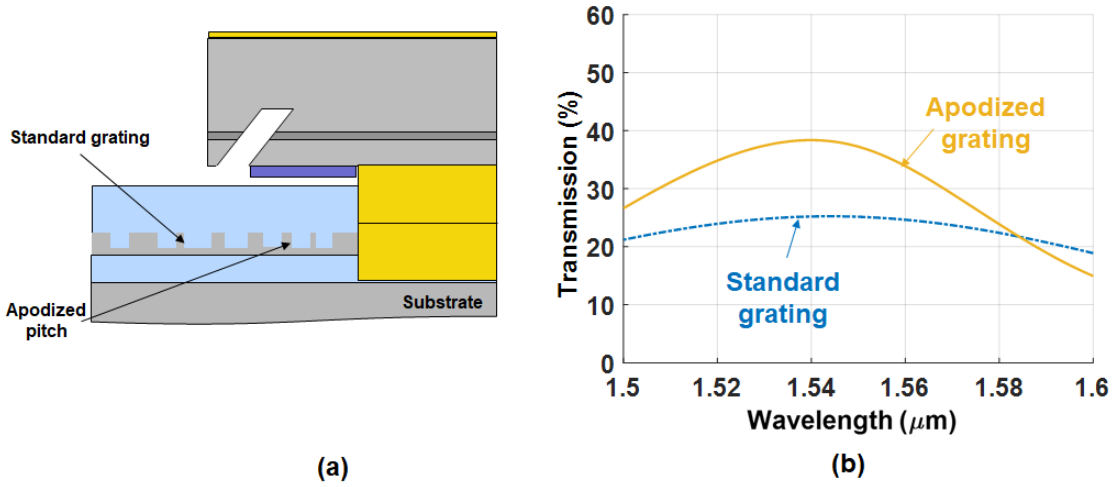


Figure 3.7: (a) 2D schematic design of 3D hybrid integration using apodized grating coupler. (b) 2D FDTD simulation of the coupling efficiency versus wavelength for apodized and standard grating coupler.

coupler.

3.2.5 High Coupling Efficiency Design

High coupling efficiency between the RSOA and silicon waveguide was achieved by combining several coupling efficiency enhancement techniques. The conventional RSOA design was replaced with a dilute waveguide RSOA. The dilute waveguide provides lower divergence output beam with increased beam size. The 220 nm thick silicon grating coupler layer is increased to 500 nm. A thicker silicon coupler provides high effective index that is helpful for coupling a divergent beam from the RSOA. The grating coupler and silicon waveguide are subject to different thicknesses. The total thickness of the grating coupler is 500 nm and the thickness of the waveguide is 160 nm. The etching depth of the grating, pitch and fill factor of the 500 nm grating coupler are optimized by PSO. Gold reflector was inserted beneath the grating coupler. A 2D schematic of the high coupling efficiency design is shown in Fig. 3.8(a). The coupling efficiency was simulated

by 2D FDTD. As shown, the maximum coupling achieved was 85%, a significant increase compared to other implementation.

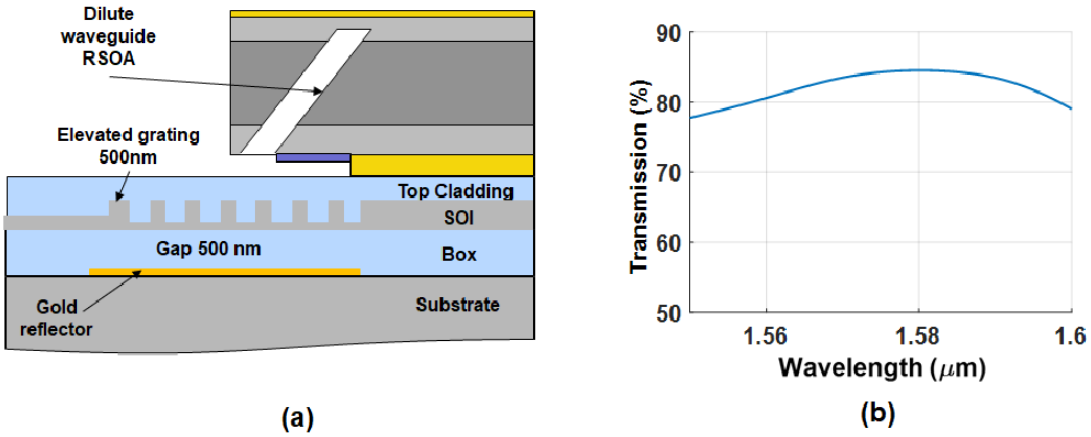


Figure 3.8: (a) 2D schematic of the high coupling efficiency design. (b) 2D FDTD simulation of the coupling efficiency versus wavelength for high coupling efficiency design.

3.3 Alignment Tolerance Analysis

Flip-chip bonding is used for the 3D hybrid integration technology. This is a mechanical assembly process where two chips are attached. The misalignment is inevitable due to mechanical movements of the equipment. The source of misalignment comes mainly from the pick-and-place mechanical displacement error. Another misalignment comes from the solder reflow process. To overcome the misalignment in the assembly process, high precision bonding tools are used. However, those tools are expensive and limit the throughput of the flip-chip process. Making the bonding process insensitive to the placement error is important for hybrid integration approaches on SiPh. In this section, the coupling efficiency variation with respect to the misalignment is studied. The bonding

process related misalignment mainly refers to the offset of the relative position offset between the RSOA and SiPh chips.

3.3.1 Vertical Offset

The coupling efficiency variation with respect to the vertical position offset between the lower RSOA emitting surface and the top of the grating coupler cladding is presented. The coupling efficiency calculation is based on 2D FDTD simulations. The grating coupler used here is based on 380 nm total grating thickness with 220 nm etching depth. In the simulation, the RSOA with a conventional waveguide design was fixed above the silicon grating coupler, and then the vertical position, or gap, was varied. An air gap was used for this simulation. At each vertical offset position, the coupling efficiency was calculated. The coupling efficiency drops almost linearly with the increasing vertical offset. Both conventional and dilute RSOAs were simulated. The results are shown in Fig. 3.9. The coupling efficiency at each offset position was normalized to the maximum value. The vertical offset that introduces 1 dB extra-loss for the dilute waveguide design is 1.79 μm. For the conventional waveguide design, the offset is only 0.9 μm. A large vertical offset tolerance suggests better alignment tolerance.

3.3.2 Horizontal Offset

The coupling efficiency variation with respect to the horizontal position offset between the RSOA emitting surface and the grating coupler was also studied. The simulation set up was identical to the model used in 3.3.1. The RSOA was fixed over the silicon grating coupler. The horizontal position of the silicon grating coupler varied with respect to the position of the RSOA. At each offset position, the coupling efficiency was calculated. Both conventional and dilute RSOAs were simulated. The results are shown in Fig. 3.10

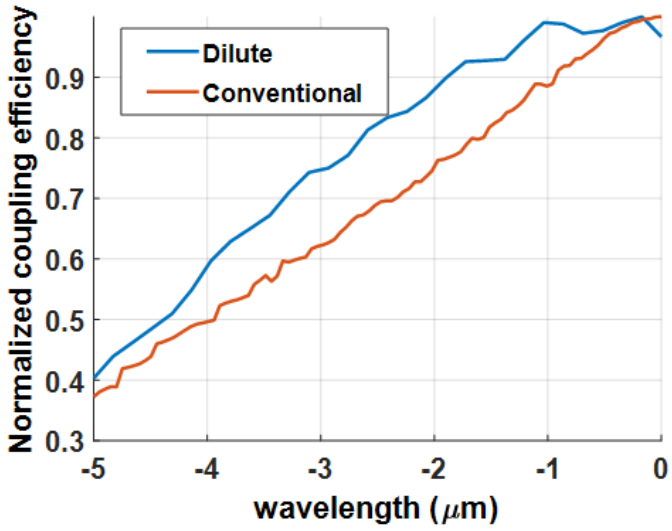


Figure 3.9: Vertical alignment tolerances. The coupling efficiency is shown as a function of the vertical offset for both the conventional and dilute waveguide RSOA.

with the coupling efficiency normalized to the maximum value. An alignment error of 1.74 μm in the horizontal direction results in an additional 1 dB coupling loss for the dilute RSOA design. For the conventional waveguide RSOA design, this offset is only 0.8 μm.

3.3.3 Horizontal and Verical Offset Combined Analysis

The 2D FDTD simulations allow for fast coupling efficiency calculations. The combined sweep of the grating coupler position both in the vertical and horizontal directions is presented here. The silicon grating coupler used in this simulation is identical to the one used in section 3.3.1. At each position, the coupling efficiency is calculated and normalized to the maximum value. The results are presented as a contour map. Each contour line indicates extra loss introduced by the spatial offset at a certain position. The area within a certain contour line can be used as an indicator for the alignment tolerance. The simulation results for coupling a conventional and dilute RSOA to the

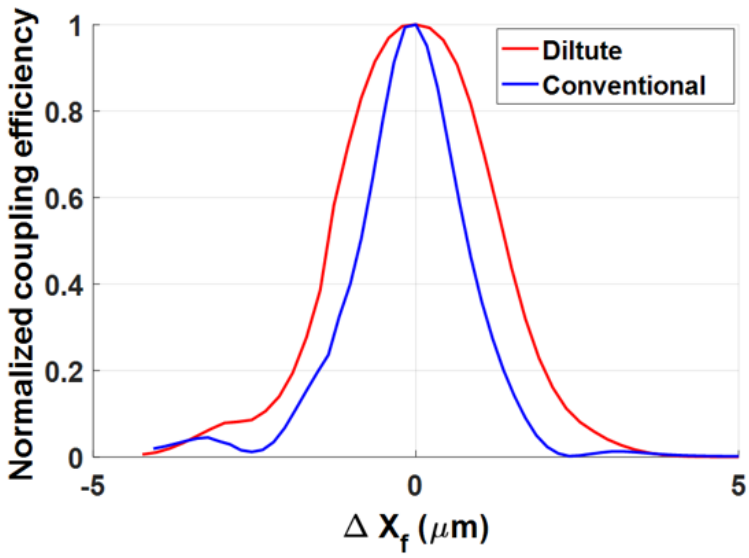


Figure 3.10: Horizontal alignment tolerances. The coupling efficiency is shown as a function of the horizontal offset for both the conventional and dilute waveguide RSOA.

silicon grating coupler are shown in Fig. 3.11 and Fig. 3.12 respectively. The simulation illustrates a significant alignment tolerance enhancement by replacing the conventional RSOA with a dilute waveguide design for the 3D hybrid integration platform.

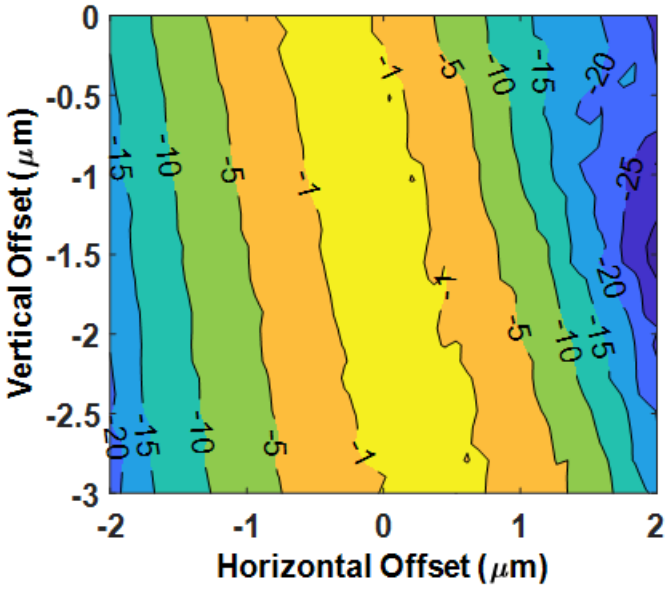


Figure 3.11: Contour plot of additional coupling loss introduced by horizontal and vertical misalignment offset (dB) of conventional RSOA couple to elevated grating coupler.

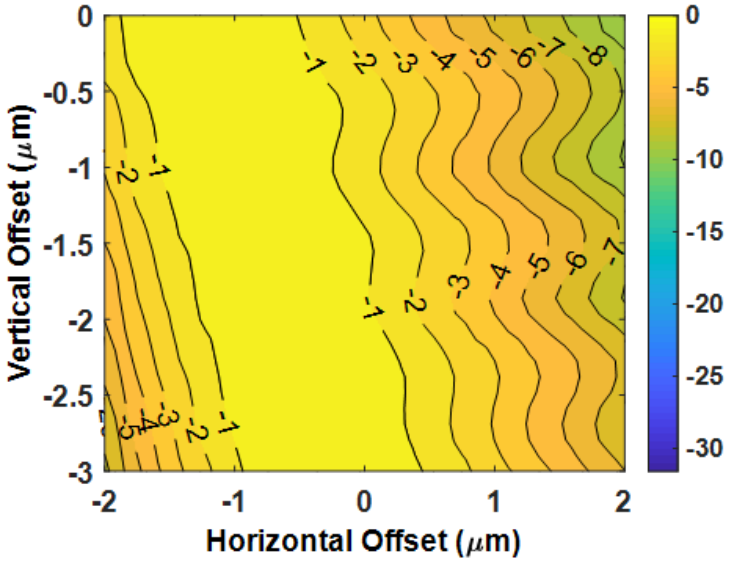


Figure 3.12: Contour plot of additional coupling loss introduced by horizontal and vertical misalignment offset (dB) of dilute RSOA coupled to elevated grating coupler.

Chapter 4

Indium Phosphide Device Fabrication

In this chapter, the InP device fabrication process is discussed. The fabrication starts with the epitaxy on a native InP substrate using reduced toxicity Metal-organic chemical vapour deposition (MOCVD). The samples then go through a series of fabrication steps including thin film deposition, etching, metal deposition and thermal processing. Some of the processing tools and techniques used are projection photolithography, dielectric film deposition, dry etching of dielectric and semiconductor films using reactive ion etching and inductively coupled plasma reactive ion etching, wet etching of dielectric and semiconductor films and electron beam evaporation of metals.

The fabrication processes for an InP RSOA, laser and PIC are similar, but the complexity of these processes is different. The fabrication of the RSOA has the lowest complexity. The regrowth can be eliminated for the RSOA [71]. InP lasers or PICs, however, generally require additional regrowth steps in order to achieve single wavelength operation or integrated device functionality [72]. For an InP laser, a mode selection structure must be incorporated, which might require a subwavelength grating. The subwavelength

structure can only be made by using EBL and interference lithography. The use of high order DBR gratings can reduce fabrication complexity but comes at the cost of limited slope efficiency for the lasers [73]. Subwavelength grating processes for the InP lasers reduce the overall yield and increase the cost for fabrication. InP based PICs demand the highest complexity in terms of fabrication [74]. Active devices such as lasers, SOAs, modulators and photodiodes must be linked by passive waveguides on a single substrate. Extra fabrication processes, such as active-passive definition, are required, adding to the complexity of the fabrication and decreasing the yield [75].

In this chapter, the fabrication of the integrated turning mirror will be reviewed first. Next, the step by step fabrication review of the dilute waveguide RSOA will be provided. Last, the fabrication process for InP PICs used for integrated frequency-modulated continuous-wave (FMCW) lidar application will be discussed. Active components on this PIC include a widely tunable laser, balanced photodiodes and a phaser shifter. Passive components are also integrated including an asymmetric Mach-Zehnder interferometer, a four-ports multimode interference (MMI) coupler, and deeply etched ridge waveguide for small bending radius.

4.1 Integrated Turning Mirror Fabrication

The RSOA deployed in the 3D hybrid integration technology features surface beam emission. To achieve this functionality, a total TIR mirror must be incorporated into the waveguide. The fabrication of the TIR mirror using chemically assisted ion beam etching (CAIBE) and focused ion beam (FIB) etching are introduced in this section. In this section, the state-of-art InP dry etching technologies are reviewed first. Then, the general principles of the CAIBE and its application for angled facet etch are discussed. In the last part of this section, TIR mirror fabrication using FIB etching is discussed.

4.1.1 Dry Etch Processes

Two types of dry etch processes are used in this work for InP fabrication: $CH_4/H_2/Ar$ reactive ion etching (RIE) and $Cl_2/H_2/Ar$ inductively coupled plasma (ICP) RIE. RIE of InP with the $CH_4/H_2/Ar$ plasma is able to produce a nearly vertical etch profile with smooth surfaces. The limitations of this approach for TIR mirror fabrication are devoted to micro-loading effect [76], which leads to a nonuniform etch profile in terms etch rate, sidewall angle and roughness. The performance of the TIR mirror is degraded in this way. Another challenge is the polymer formation, which without proper removal results in contamination and degraded anisotropy [77]. To achieve a tilted stage, extra parts need to be fabricated which increases the complexity of the process since most of the RIE tools do not have a tilted wafer holder [78].

Dry etch processes that produce highly anisotropic etch profiles with smooth surface morphology are critical for high performance InP photonics devices. ICP-RIE etching is important for dry etching, featuring a high density plasma with a low bias voltage and low chamber pressure [79]. The etch rate is much higher for ICP-RIE with improved anisotropy compared to RIE. The high process temperature is generally required for this process, attributed to the low volatility of $InCl_2$, which limits the chemical activity and leads to surface roughness through nonuniform desorption. When InP is etched at elevated temperatures above 200°C, however, the desorption rate of $InCl_2$ increases considerably, resulting in substantially increased etch rates, improved anisotropy, and smooth surfaces [80]. ICP is commonly used for InP waveguide fabrication and subwavelength grating etching. However, most ICP etchers are not equipped with an angled wafer holder, which makes it difficult to use for TIR mirror fabrication.

4.1.2 Chemically Assisted Ion Beam Etching

CAIBE is a novel dry etching technique for III-V material fabrication [81] [82] [83]. It is an enhanced version of reactive ion beam etching. In CAIBE, a collimated beam of reactive ions (and neutrals) is extracted from a plasma and directed at the sample. As a result, independent control of the ion energy, current density and background gas compositions is allowed. This is not achievable in RIE since etch parameters (flows, ion density, chamber pressure) are interdependent. The process can usually be adjusted to obtain high etch rates and anisotropic profiles in various materials. Compared to RIE, the CAIBE chemical flux is introduced into the etching chamber independent of the ion source operation. In also provides a wider range of control on top of ion energy, current and etching chemical composition. Dry etched mirrors have been fabricated with CAIBE with compatible performance of a cleaved facet [84]. Compared to RIE etching, CAIBE features less polymer accumulation and less loading effect. Like Cl_2 based ICP, the sample are usually heated up to 250°C for $InCl_2$ desorption for InP processes. Some of the commercially available CAIBE tools featured a tilted wafer holder inside the etching chamber. This is particularly attractive for the angled dry etching process. A hard mask, such as silicon nitride (SixNy) and silicon dioxide (SiO_2) is used. The CAIBE process relies more on physical bombardment of ions on the sample. The etch selectivity between the mask and target materials is based on the sputtering yield rate. Materials with higher sputtering yield are used to achieve high etch selectively for the CAIBE process.

In this work, for the conventional RSOA, the TIR mirror is etched by the CAIBE process. The mask material is Al_2O_3 grown by electron beam evaporation. The sample was mounted on a tilted substrate at a certain angle, an energetic Ar beam was directed to the sample concurrently with a neutral Cl_2 gas flowing onto the sample surface. The tilted angle is not necessarily equal to the TIR mirror turning angle so as to compensate

for the extra tilting introduced by the chemical etch. The back facet of the conventional RSOA is also fabricated by the CAIBE process. Figure 4.1(a) shows the top view of a etched trench by CAIBE. The red circle marks the surface emission window. Figure 4.1(b) shows the cross-section of the etched TIR mirror by CAIBE. The etching temperature is 250°C for $InCl_2$ desorption.

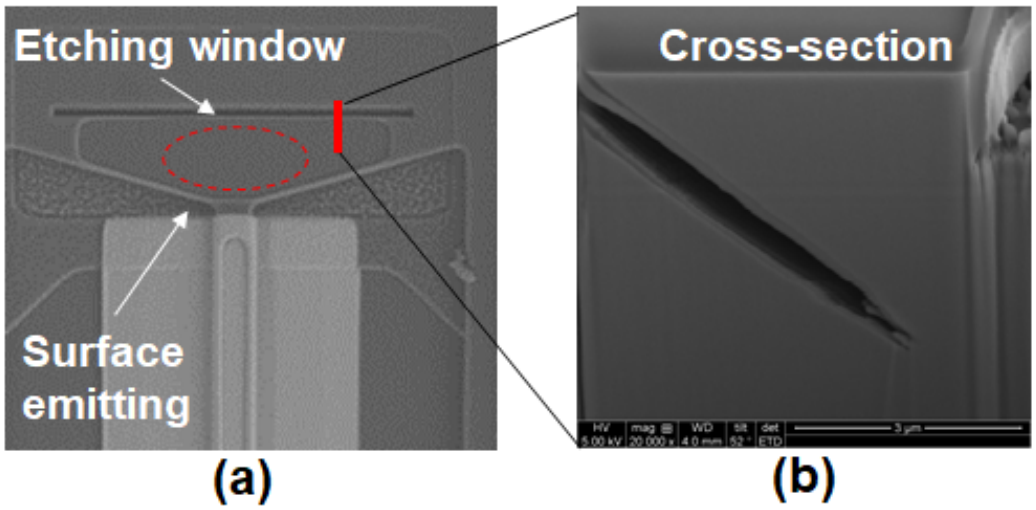


Figure 4.1: (a) Top view of a TIR mirror on conventional RSOA fabricated by CAIBE process (b) Cross-section of a etched TIR mirror.

4.1.3 Focused Ion Beam Etching

FIB has been used in semiconductor manufacturing for over 20 years. FIB systems operate in a similar fashion to a scanning electron microscope (SEM) except, rather than a beam of electrons, a beam of collimated ions is directed at the sample [85]. It uses a finely focused beam of gallium ions (Ga^+) that operates at low beam current for imaging or at high beam current for site specific sputtering or milling. Unlike an electron microscope, FIB is inherently destructive to the specimen. When the high-energy Ga^+ ions strike the sample, they will sputter atoms from the encountering surface. Ga^+ will also be implanted from the top surface, leaving the surface amorphous [86]. With a tiled

sample stage, FIB is an ideal process for angled etching at arbitrary locations on the wafer with arbitrary angles. In CAIBE, the plasma is formed uniformly across the whole chamber, whereas for FIB, the focused Ga^+ ions will only be applied to a specific region. Outside the defined region, the sputtering or milling will not take place so that a mask is not needed for the FIB process.

In this work, a FEI Helios Dualbeam Nanolab 600 system is used for TIR mirror fabrication by FIB. The system is equipped with a SEM for nanometer resolution imaging and a FIB column operating from 30 kV to 500 V. Ion currents range from 7 pA to 22 nA, which can be used for substantial milling tasks. A piezo-driven stage can operate within an area of 150 x 150 mm^2. The Ga^+ source can be used to image and nano machine down to 5 nm structures.

The TIR mirror is fabricated in a backend process for the RSOA. The cleaved RSOA chip was mounted on a carrier and mounted on a stage in the FIB chamber. No angle offset is needed. With a fixed operating voltage and etching area, the etching of the FIB process is related to the beam current. Generally higher beam current provides faster etching rate and more surface damage. To fabricate the TIR mirror, the angled trench is first opened using a higher current beam. Next, a clean-up etch with lower beam current is used. For the cleanup etch, the etching area is much smaller than the high-current etch. Figure 4.2(a) shows the top view of an etched trench by FIB for TIR mirror fabrication. The red circle marks the surface emission window. Figure 4.2(b) shows the cross-section of the etched TIR mirror fabricated with the FIB process.

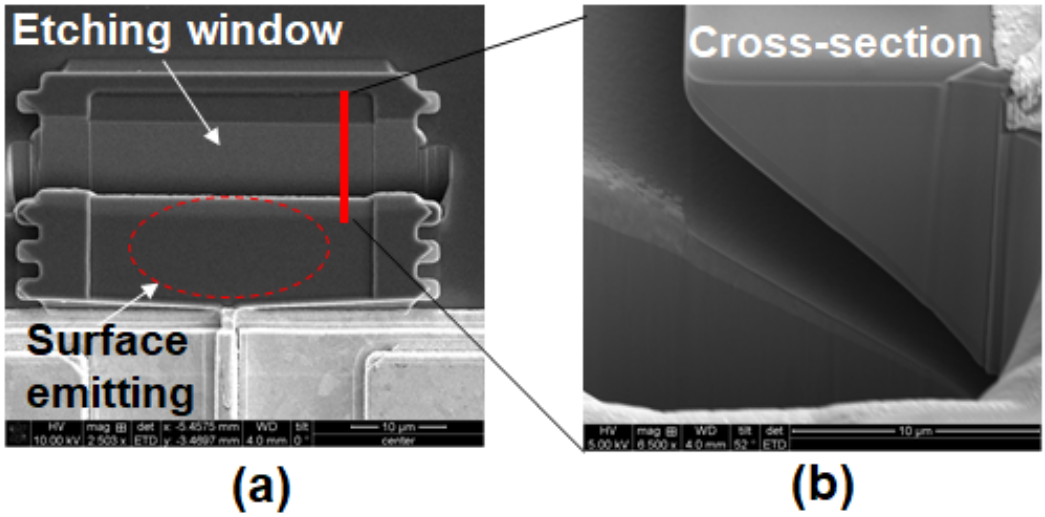


Figure 4.2: (a) Top view of etched trench by FIB for the TIR mirror. (b) Cross-section of the etched TIR mirror.

4.2 Overview of Surface Emitting Reflective Semiconductor Optical Amplifier Fabrication

The fabrication processes of an InP RSOA is significantly less involved than an InP laser or a PIC. There is no passive waveguide section on the RSOA so that the active-passive integration process is not required. The entire epitaxy structure can be realized with a single epitaxial growth. The RSOA does not require an in-plane grating for single wavelength operation. However, compared to a conventional InP RSOA, the fabrication of the RSOA for 3D hybrid integration needs to be optimized accordingly. The fabrication process for the InP RSOA includes ridge definition, surface window etch, via opening, metallization, wafer thinning and back-end processes.

Table 4.1: Dilute RSOA Base Epitaxy Layer Structure

Name	Layer	Thicknes s (nm)	Composition		Doping		
			x	y	Type	Dopant	Conc. (cm-3)
Substr.	*InP*	~	-		N	S	~3-5e+18
Buffer	*InP*	800	-		N	Si	1.00E+18
Buffer	*InP*	100	-		N	Si	8.00E+17
Buffer	*InP*	100	-		N	Si	6.00E+17
WG	*In(x)GaAs(y)P*	3000	0.903	0.213	N	Si	8.00E+16
WG	*In(x)GaAs(y)P*	2000	0.903	0.213	N	Si	5.00E+16
Mode Control	*In(x)GaAs(y)P*	[100]	0.7585	0.5324	N	Si	3.00E+16
Spacer	*InP*	20	-		N	Si	3.00E+16
Barrier	*In(x)GaAs(y)P*	8	0.735	0.513	UID	-	
QW	*In(x)GaAs(y)P*	6.5	0.735	0.845	UID	-	
Barrier	*In(x)GaAs(y)P*	8	0.735	0.513	UID	-	
QW	*In(x)GaAs(y)P*	6.5	0.735	0.845	UID	-	
Barrier	*In(x)GaAs(y)P*	8	0.735	0.513	UID	-	
QW	*In(x)GaAs(y)P*	6.5	0.735	0.845	UID	-	
Barrier	*In(x)GaAs(y)P*	8	0.735	0.513	UID	-	
QW	*In(x)GaAs(y)P*	6.5	0.735	0.845	UID	-	
Barrier	*In(x)GaAs(y)P*	8	0.735	0.513	UID	-	
QW	*In(x)GaAs(y)P*	6.5	0.735	0.845	UID	-	
Barrier	*In(x)GaAs(y)P*	8	0.735	0.513	UID	-	
SCH	*In(x)GaAs(y)P*	25	0.7676	0.504	UID	-	
InP	*InP*	10	-		UID	-	
Mode Control	*In(x)GaAs(y)P*	20	0.7585	0.5234	P	Be	1.00E+17
InP	*InP*	10	-		P	Be	3.00E+17
Mode Control	*In(x)GaAs(y)P*	20	0.7585	0.5234	P	Be	3.00E+17
InP	*InP*	10	-		P	Be	3.00E+17
Mode Control	*In(x)GaAs(y)P*	20	0.7585	0.5234	P	Be	3.00E+17
Cap	*InP*	30	-		P	Be	3.00E+17
Cap	*InP*	170	-		P	Be	5.00E+17

4.2.1 Base Structure

The details of the base epitaxial layer structure for the dilute RSOA are listed in Table 4.1. The name, composition, thickness and doping of each layer are presented. The base structure was grown on a sulfur doped n-type InP wafer. The N-contact of

the RSOA can be formed on the back side of the wafer after thinning. Compared to a conventional surface ridge design, the epitaxy design of the dilute RSOA features a significant thicker quaternary waveguide layer. Mode control layers are used to optimize the mode overlap with the MQW to achieve a high overlap coefficient. The base material is wet etched to the last layer of the InGaAsP (marked with a green dot in table 4.1). Then a 1.8 μm of p-type InP, a 100 nm thick InGaAs contact layer and a 200 nm InP capping layer is grown by the in-house MOCVD system. The final epitaxy structure for the dilute waveguide RSOA in this work is shown in Fig. 4.3.

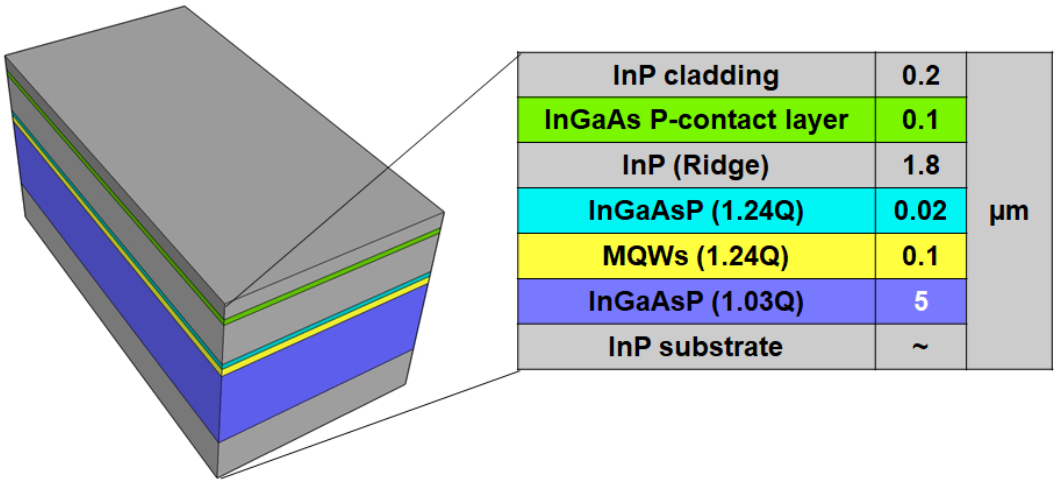


Figure 4.3: Final epitaxy structure for the dilute waveguide RSOA.

4.2.2 Ridge Waveguide Formation with Trench Etch

The waveguide formation process is the first step. As shown in Fig. 4.4(a), the shallow ridge was defined by etching away material in the trench area next to the mesa. The rest of wafer area is planar. For the RSOA used in 3D hybrid integration, it is important to maintain the rest of wafer area as planar as possible for the flip-chip bonding process. A combined SixNy and SiO_2 mask is used for the etching. A 50 nm of SixNy is used as seeding layer for a better hard mask adhesion followed by 500 nm SiO_2 deposition.

The ridge was etched in two steps. First, $Cl_2/H_2/Ar$ ICP-RIE was used to etch the InP ridge and stop within 0.4 μ of the quaternary layer. The rest of the InP was wet etched by using H_3PO_4:HCl 3:1. The advantage of the two step ridge etching process is that atomically smooth waveguide side wall can be achieved with minimum ridge undercut due to the crystallographic etch.

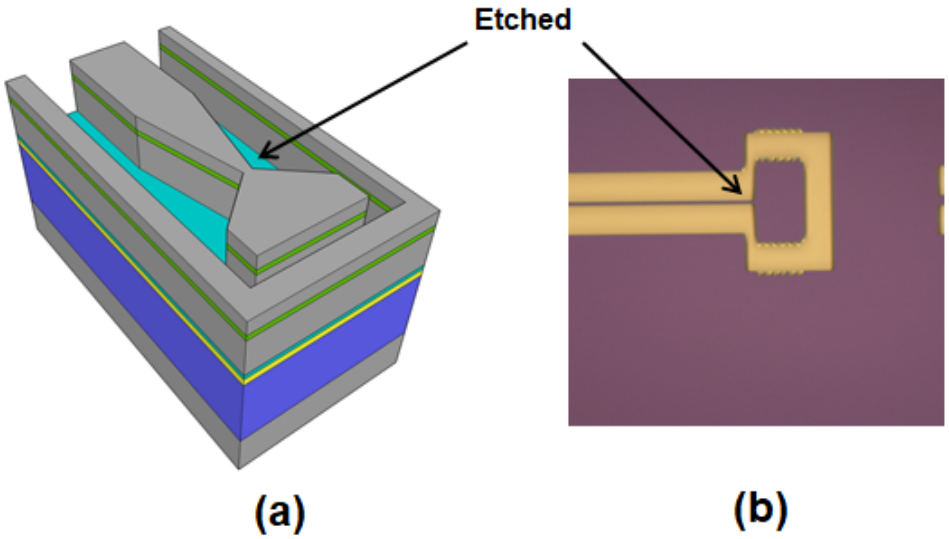


Figure 4.4: Ridge waveguide formation with trench etched for the dilute waveguide RSOA. (a) 3D schematic of the trench etch and (b) top view microscope picture of ridge waveguide after etching with hard mask.

4.2.3 Surface Emission Window Etch

The p-type contact layer is absorbing at the designed operation wavelength of the RSOA. For the edge emitting device, this layer of contact material is far away from the optical mode. However, for the surfacing emission RSOA, the InGaAs p-contact layer needs to be removed locally at the surface emission window (where light passes through). After the ridge waveguide etch, an extra 100 nm silicon nitride was deposited to cover the exposed InP. A Photoresist mask is then used to define the surface emission window. A

SixNy mask was dry etched in RIE to expose the top InP and photoresist remained during the wet etch for extra masking. The top InP cladding and InGaAs contact layers are wet etched by H_3PO_4:HCl 3:1 and H_2SO_4:H_2O_2:H_2O 1:1:10, respectively. Figure 4.5(a) shows a 3D schematic of a surface emission widow and Fig. 4.5(b) shows a corresponding top view microscope image of a fabricated surface emission window.

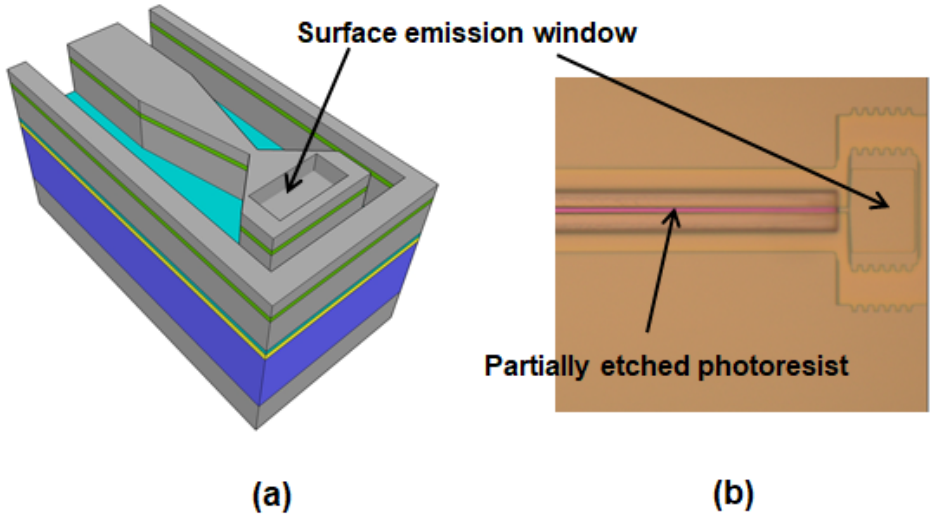


Figure 4.5: Surface window etch for the dilute waveguide RSOA. (a) 3D schematic and (b) top view microscope picture of surface window.

4.2.4 Via Opening and Metallization

A layer of 200 nm SixNy is used as a waveguide cladding for the dilute RSOA. The thickness is chosen based on a light extraction enhancement; the SixNy film deposited by the plasma-enhanced chemical vapor deposition (PECVD) with total thickness of 200 nm can be used as an antireflection coating for surface emission. The semi-self-aligned process [87] is used for the p-via opening, in which a thick photoresist is spun and is partially exposed with a mask area much wider than the real ridge, and dry etched until the top of the ridge is exposed. Figure 4.6(a) shows a 3D schematic of opened via on top

of the ridge. Figure 4.5(b) shows the partially etched photoresist, exposing the SixNy on top of the ridge with the rest of area is still covered by the photoresist.

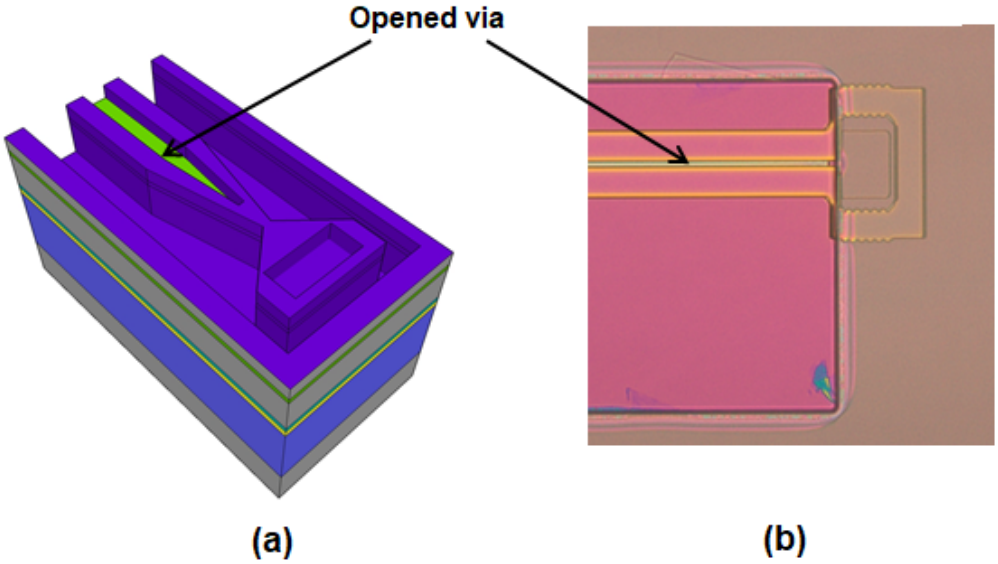


Figure 4.6: (a) 3D schematic of the via opening and (b) top view microscope picture of the lift-off mask for p-metal with via opened.

The SixNy is then etched in RIE to expose the InP cladding. To avoid photoresist contamination of the contact layer, the InP cladding is not etched until the p-type metallization lift-off mask is fabricated. The 200 nm InP cap layer is wet etched by the H_3PO_4:HCl 3:1 that stops at the InGaAs contact layer. The p-contact metal was deposited after the lift-off mask lithography. Figure 4.6(b) shows the top view microscope image of the lift-off mask for p-metal with the via opened. To achieve better sidewall coverage, the sample was mounted on a tilted stage with rotation in the electron-beam evaporating deposition chamber for contact metal deposition. The metal thickness is approximately 2.5 μm. After the p-type metal lift-off, the wafer was cleaned and annealed in forming gas to reduce the contact resistance. Figure 4.7(a) shows the 3D schematic of dilute waveguide RSOA after p-metal deposition and Fig. 4.7(b) shows the surface emission window under SEM with the TIR mirror fabricated by FIB. The red line in Fig.

4.7(a) indicates the TIR mirror trench to be fabricated by FIB etching.

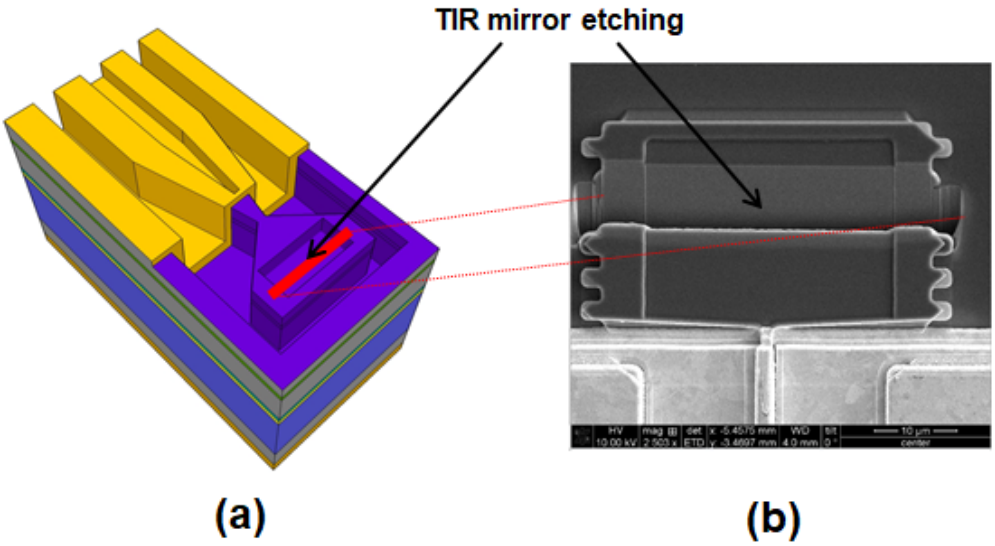


Figure 4.7: (a) 3D schematic of fabricated dilute waveguide RSOA and (b) surface emission window under SEM with turning mirror fabricated by FIB during a back end step.

The wafer was subjected to a brief diagnostic measurement for an initial evaluation after the p-metal fabrication and annealing. The main purpose of this test is to check the contact resistance; an extra layer of contact metal could be added if the contact resistance is higher than expected. Figure 4.8(a) and (b) shows the dilute RSOA ridge cross-section SEM image before and after the inverse taper with the metal contact layer on top of the ridge.

4.2.5 Backend Process Steps

After the evaluation, the wafer was thinned with a back-side lapping process. The wafer thickness after lapping is 150 μm. Before cleaving, the n-metal stack was deposited on the backside of the wafer. The backside surface was solvent cleaned prior to deposition. After the backside metalization, the wafer is cleaved into bars. The back facet of the

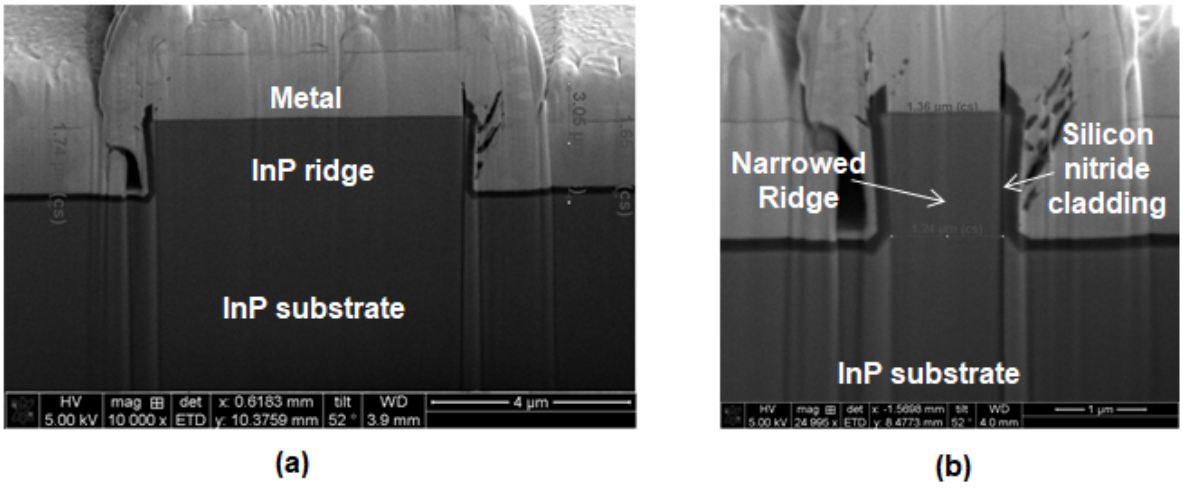


Figure 4.8: Dilute RSOA ridge SEM cross-section image (a) before and (b) after the inverse taper.

RSOA is subjected to a high-reflection (HR) coating to create one reflective mirror. The HR coating is deposited in house using electron beam evaporating using with two periods of SiO_2 and amorphous silicon. The thickness of the SiO_2 and amorphous silicon used are 250 nm and 110 nm, respectively. The HR coating increases the reflection of a cleaved facet from $\tilde{3}0$ % to $\tilde{9}5$ %. After the HR coating, the devices are cleaved into single bars and mounted for testing.

4.3 Overview of InP Photonic Integrated Circuit Fabrication

The fabrication processes of an InP PIC is significantly more complicated than the fabrication processes of an InP laser or RSOA. For example, the number of mask layers for the InP RSOA in section 4.2 is four. For the InP PIC that is introduced in this section, the number is twelve. Regrowth and multiple etching steps are incorporated

into the fabrication processes. Although the minimum features as well as the alignment control in InP PIC fabrication processes are not as critical as in SiPh, the challenges come from the handling of the fragile InP wafers. The wet processes include the InP ridge waveguide etch, the InGaAs contact layer removed for electrical isolation and the InP cap removed. These steps require care to prevent unwanted etching of important layers.

In this section, the fabrication process of an InP PIC is reviewed with the emphasis on the potential risk of failure at each step. Some of the issues can be solved with improved fabrication tools. However, for small volume prototype development both for research and production, those issues need to be addressed in order to achieve better yield. The InP PIC introduced in this section is used as a FMCW.

4.3.1 Active-Passive Integration

The active-passive integration is the most significant difference between the fabrication of an InP PIC and a RSOA. The active material is grown everywhere on the wafer during the epitaxial growth. When it is pumped, optical gain can be achieved. However, for passive devices, the active material is absorbing and would increase the insertion loss. Different integration platforms for InP PICs are often classified based on the active-passive integration technology [88]. In this work, the offset quantum well (OQW) technology as utilized [89] in Fig. 4.9. In the OQW platform, most of the p-type InP cladding and InGaAs contact layer are not deposited during the base material growth. The meaning of offset is that the optical mode center is not centered in active region, which will impact the device efficiency. Following the base material growth, the quantum wells (QWs) are removed where the passive device will be defined. The masked regions are active regions where QWs are protected by a hard mask during the wet etch.

The transition of the active regions is angled to reduce reflection. The OQW platform features high yield and a relatively simple fabrication process. However, this platform is not ideal for making low threshold lasers due to the reduced optical confinement factor [1].

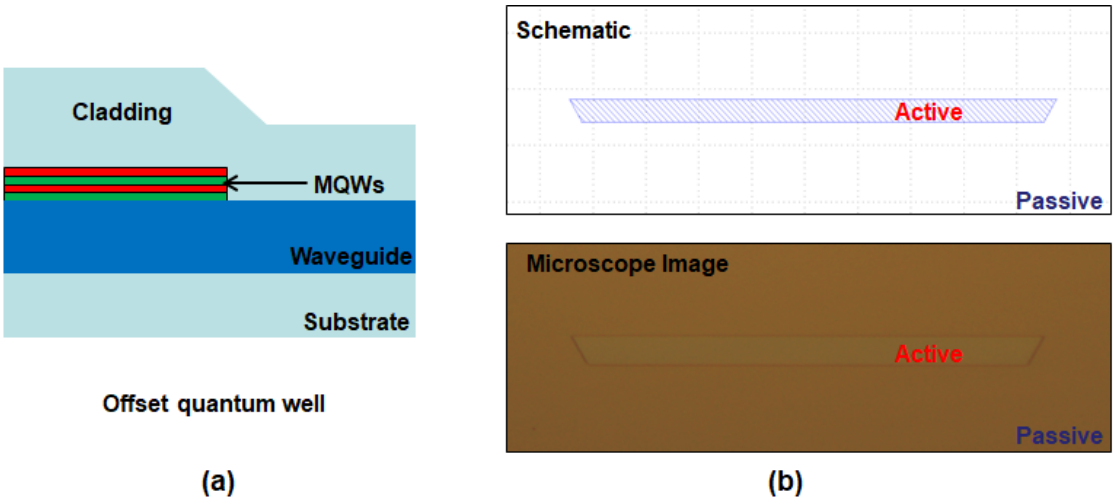


Figure 4.9: Active-passive integration with OQW. (a) 2D sideview schematic of the waveguide structure. (b) Schematic (up) and microscope image (bottom) of active–passive fabrication.

4.3.2 Grating Formation

Sampled grating DBR mirrors are used for wavelength selection for the widely tunable on-chip laser [90]. The gratings with 240 nm pitch were formed into the InGaAsP waveguide layer in a passive region. The fabrication of subwavelength gratings requires a minimum fabrication resolution of 120 nm. In this work, the gratings are defined by EBL. Compared to interference lithography, EBL features a minimum fabrication linewidth of 20 nm. SiO_2 deposited by PECVD is used as the mask material to etch the gratings. The positive-tone EBL resist (AR-P 6200) is used to pattern the hard mask.

After EBL, the grating pattern in the resist layer is transferred to the SiO_2 mask layer by ICP-RIE etching. After etching, the resist is removed by oxygen plasma ashing.

The dry etching of the grating is based on $CH_4/H_2/Ar$ RIE low bias voltage to ensure a slow etch rated, compared to the ridge etch, for better etch depth control. With the same RIE condition, the native oxide on the InP will be etched at a rate that is slow and nonuniform. This will greatly bias the grating etch and increase the roughness of the gratings, increasing loss in the mirror. To remove the native InP oxide, the wafer was dipped in $NH_4OH:H_2O$ 1:1 for 20 seconds before the RIE etch. Because of diffusion of the electrons during the a calibration process should be performed for the grating fill factor used in the design. The EBL calibration mask is shown in Fig. 4.10 targeting a 50:50 fill factor for a 200 nm pitch grating. Each burst group represents different filling factor of the grating as it is indicated in the figure insert.

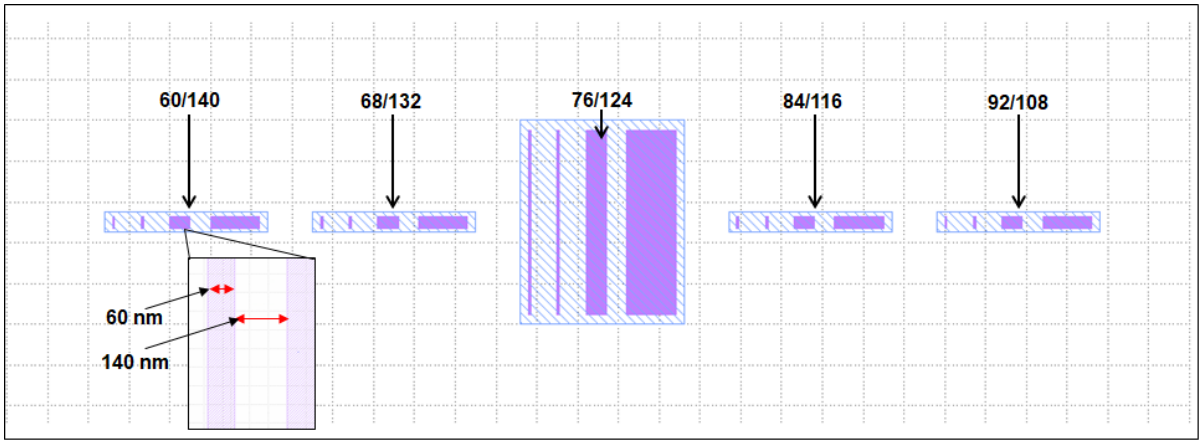


Figure 4.10: EBL grating calibration mask with different fill factors.

The pattern group shown in Fig. 4.10 will also be exposed under various electron beam dose conditions to further optimize the EBL process. Figure 4.11 shows the results of a calibration process targeting a grating optimization for 200 nm pitch after RIE etch. The grating groups with different fill factor are exposed with two different dose condition.

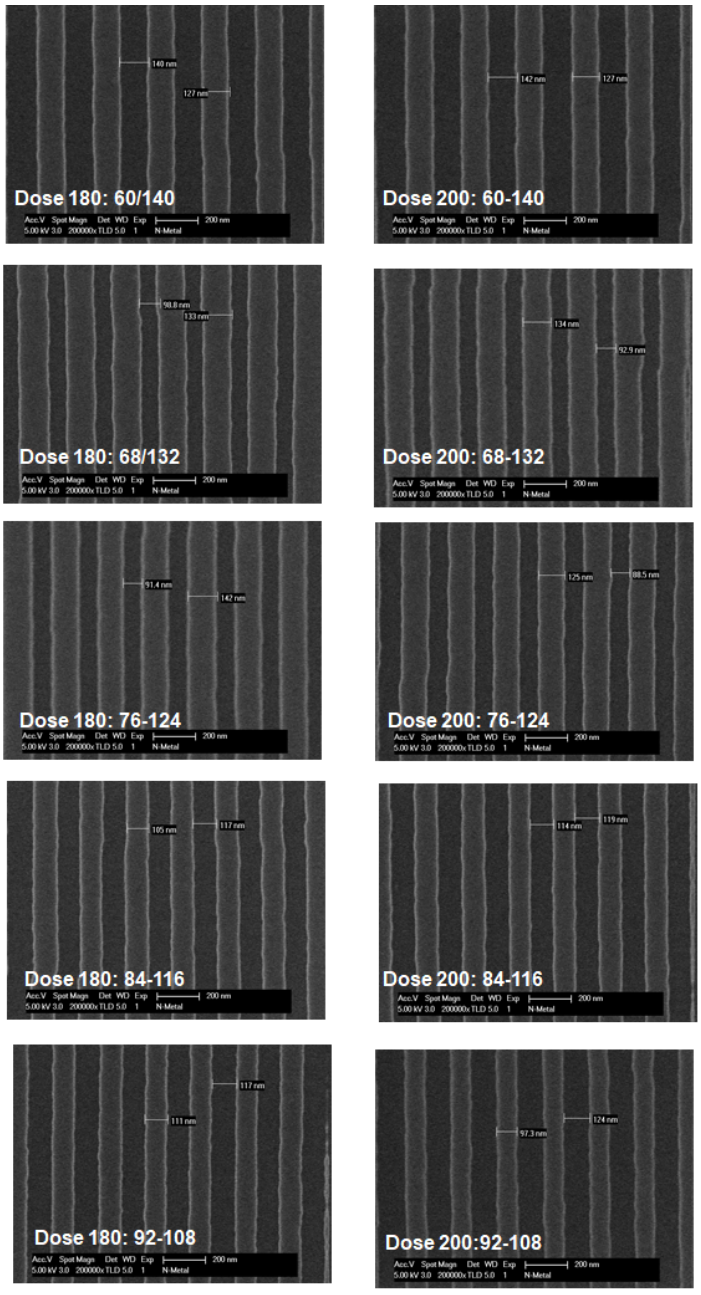


Figure 4.11: EBL grating calibration etch results. The number on each sub-figure indicates the dose and fill factor used on the mask.

4.3.3 Regrowth

The processed wafer after the active-passive and grating fabrication is loaded into the MOCVD chamber for regrowth. The surface preparation prior to regrowth is very important to achieve consistent and high-quality regrown films. After the $CH_4/H_2/Ar$ RIE etch, the hard mask is not removed immediately. To remove any photoresist and polymer residue, the wafer is first dipped into pure H_2SO_4. Then the sample is loaded into the UV ozone chamber to ash and oxide film on the surface. It is important to ensure the UV ozone chamber is clean and seasoned for this step. It is suggested to use a dedicated UV ozone chamber for regrowth preparation. Also, the chamber needs to be warmed up for one hour before the real process. The rest of the hard mask is removed by buffered HF (BHF) after the UV ozone treatment. Then the sample is immediately placed in a vacuum seal bag and transferred to the MOCVD system. After regrowth, the sample will undergo through a series of process steps beginning with waveguide definition.

4.3.4 Waveguide Formation

The waveguide formation process for PICs is significantly more involved than RSOA fabrication. To integrate both deep and shallow ridge waveguides on the same wafer, the waveguide formation fabrication process involves three steps [91]. First, both shallow and deep ridges are defined using a $Cl_2/H_2/Ar$ based ICP-RIE etch. A thicker hard mask is needed compared to the grating etch. Mask adhesion is critical because the hard mask will also be used as a wet etch mask in a later step. A combined SixNy and SiO_2 mask is used. SixNy demonstrates better adhesion than SiO_2 but lower etch selectivity in the ICP-RIE. A hard mask of 100 nm of SixNy and 550 nm of SiO_2 is used. The deep ridge region is then protected by the photoresist mask, and then the shallow ridge is etched in H_3PO_4:HCl 3:1. The fabricated cross-section of the shallow waveguide is shown in Fig.

4.12(a). In the final step, another hard mask is formed with lift-off process. The SiO_2 is deposited by the electron-beam evaporation. This layer of SiO_2 aims to provide a good side wall coverage for the shallow etched waveguide. Also, it is used to form the deep-to-shallow transition structure that is shown in Fig. 4.12(d). After the lift-off, another ICP-RIE step was used to define the deep etched ridge waveguide. The cross-section of the deep ridge waveguide is shown in Fig. 4.12(b). A perspective view SEM image of a curved deep ridge waveguide is shown in Fig. 4.12(c). The fabricated deep-to-shallow transition structure is shown in Fig. 4.12(d).

Another device that can realize the deep-to-shallow transition function is the one-by-two MMI. The taper region of one port can be defined in the shallow ridge layer. The multi-mode region is defined on the deep ridge layer starting at end of the taper region (where the multi-mode region starts). By defining the multi-mode region on the deep ridge, the MMI can be made with a compact footprint. A perspective view SEM image of a fabricated deep-to-shallow MMI is shown in Fig. 4.13.

4.3.5 Top n-Contact and Thermal Bump

After the waveguide etch, the remaining hard mask was removed by BHF. Another hard mask was deposited for the top n-contact and thermal bump fabrication. The thermal bump is designed for heat dissipation of the laser and SOAs on the PIC. ICP-RIE was used to dry etch to the middle of the InGaAsP waveguide layer. Wet etching based on H_2SO_4:H_2O_2:H_2O 1:1:10 is used to remove the InGaAsP on top of the n-type InP. N-contact metal was then deposit into the opening. It is important to leave a gap between the contact metal and contact opening during mask design. The InGaAsP layer is highly doped, therefore if contact metal touches the wall of the contact opening, a short between the p- and n-contact will be formed. The n-contact metal based on

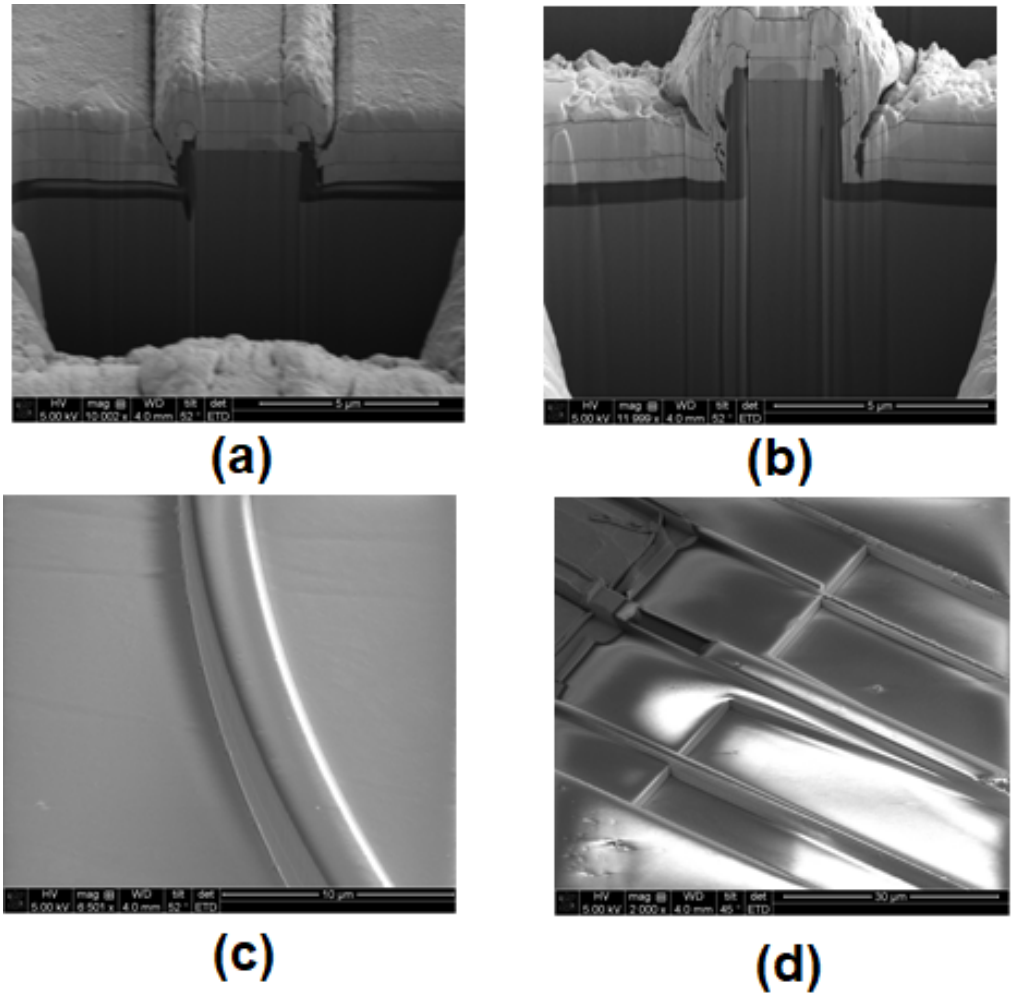


Figure 4.12: SEM image of (a) cross-section of shallow ridge, (b) cross-section of deep ridge, (c) curved deep ridge waveguide and (d) shallow-to-deep transition.

electron-beam evaporation of Ni/AuGe/Ni/Au is used. The composition of the AuGe is important for the contact quality. The AuGe has an optimized composition. After lift-off, the contact was annealed in forming gas to alloy and reduce resistance.

4.3.6 Passivation and Electrical Isolation

A high quality dielectric film was deposited for device passivation. The adhesion is crucial and one concern is the stress in the film deposited by PECVD. One solution to

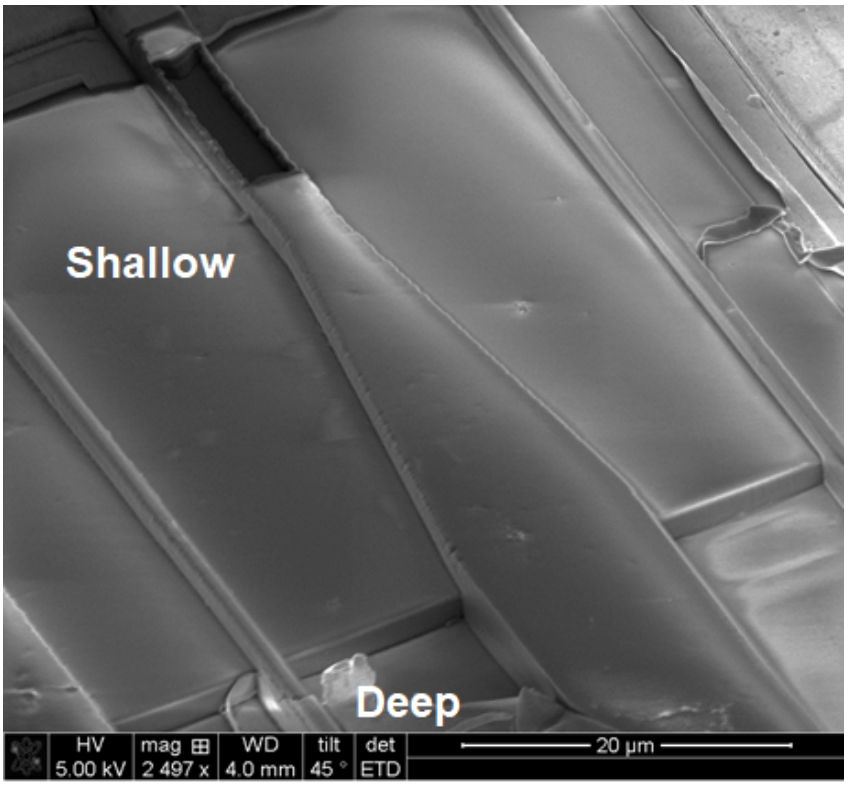


Figure 4.13: The deep-to-shallow transition MMI.

alleviate film stress is to use multiple layers of material that with opposite stress. It is reported that stress of SixNy deposited at 300 °C and 60 °C are -78.4 MPa (tensile) and -11.2 MPa, respectively [92]. For SiO_2, the stress is 51.78 MPa (compressive) at 300°C and 7.4 MPa at 60°C [92]. Based on these stress parameters, a layer of SixNy of 100 nm is first deposited at 250°C. Then 250 nm of SiO_2 is deposited immediately. Finally a layer of SixNy, which is 150 nm thick is deposited on top of the SiO_2. This provides good adhesion as well as sidewall coverage. Electrical isolation between different components on the PIC is required to ensure that all integrated devices operate independently. For the OQW platform, the isolation is realized by selectively etching the top InP cap and InGaAs contact layer between the different components.

The isolation lithography utilizes the SSA process that was described in section 4.2.4.

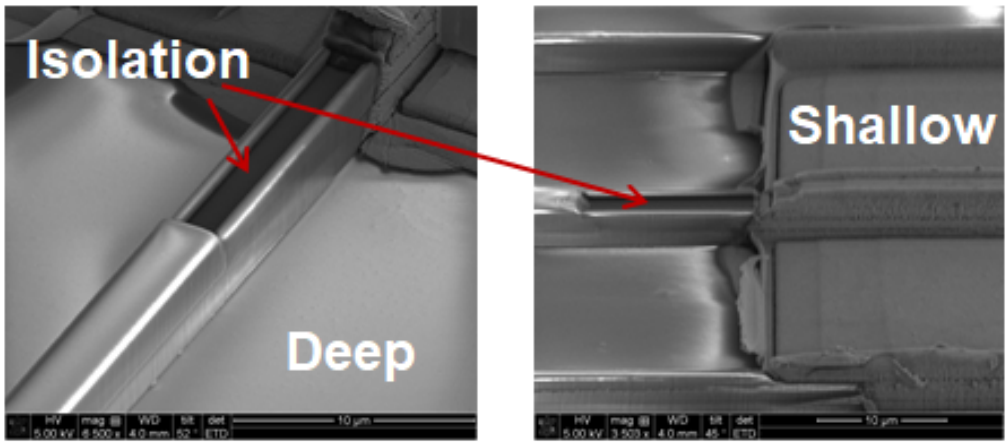


Figure 4.14: Example of isolation formed by selectively etching the top InP cap and InGaAs contact layer.

The waveguide isolation is shown in Fig. 4.14. The fabrication steps include p-via and metalization, which are similar to those used for the RSOA fabrication.

4.3.7 Photonic Integrated Circuit for 3D Hybrid Integration

The InP PIC fabricated in this section was designed for 3D hybrid integration on a SiPh chip for an integrated lidar system. This InP PIC has distinct features compared to the traditional InP PICs. First, the waveguide ridge is defined by etching a trench aside the ridge to ensure the wafer is nearly planar the flip-chip bonding process. Second, the PIC is populated with thermal bumps that share same layer structure with the n-contact metal for effective heat dissipation for the integrated laser and SOAs. The bonding pads on the silicon chip will match the thermal bumps on the InP PIC to provide extra mechanical stability for the system. Last, the termination of the output waveguide for the InP PIC is a rapid taper structure for surface emission. A TIR mirror is shown in Fig. 4.15.

The InP PIC was mounted on the custom designed carrier for initial calibration. Figure 4.16(a) shows the top-view image of the supper carrier with transmitter IC, InP

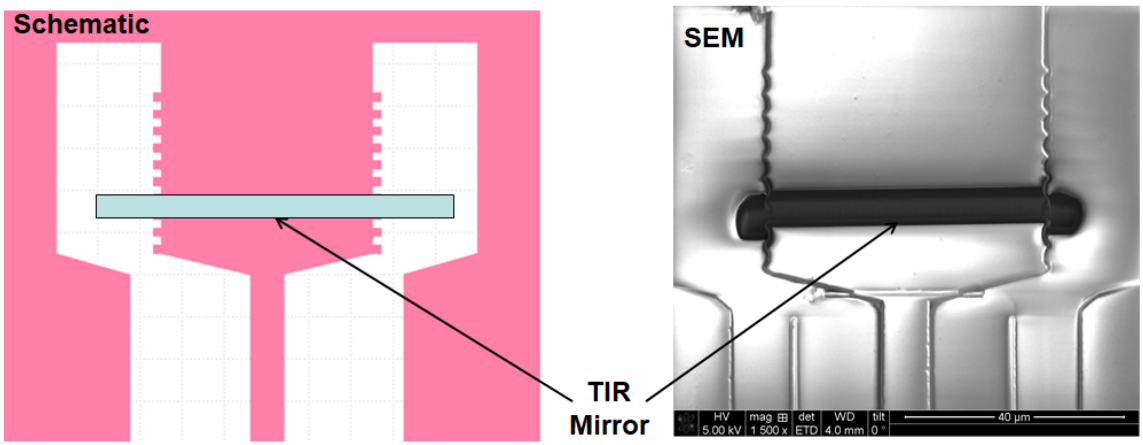


Figure 4.15: Schematic (left) and top-view SEM of surface emssision window (right) with TIR mirror fabricated.

PIC and receiver IC. The InP PIC was mounted on a small sub-carrier before bonding to the super carrier. The pads on the PIC are connected onto the supper carrier by wire bonding. Figure 4.16(c) shows the optical-electrical integration by wire bonding. The rest of the area on the supper carrier was reserved for the frequency locker IC and receiver IC. To illustrate the compact footprint, the entire integrated lidar transceiver system was photographed with a coin as shown in Fig. 4.16(d).

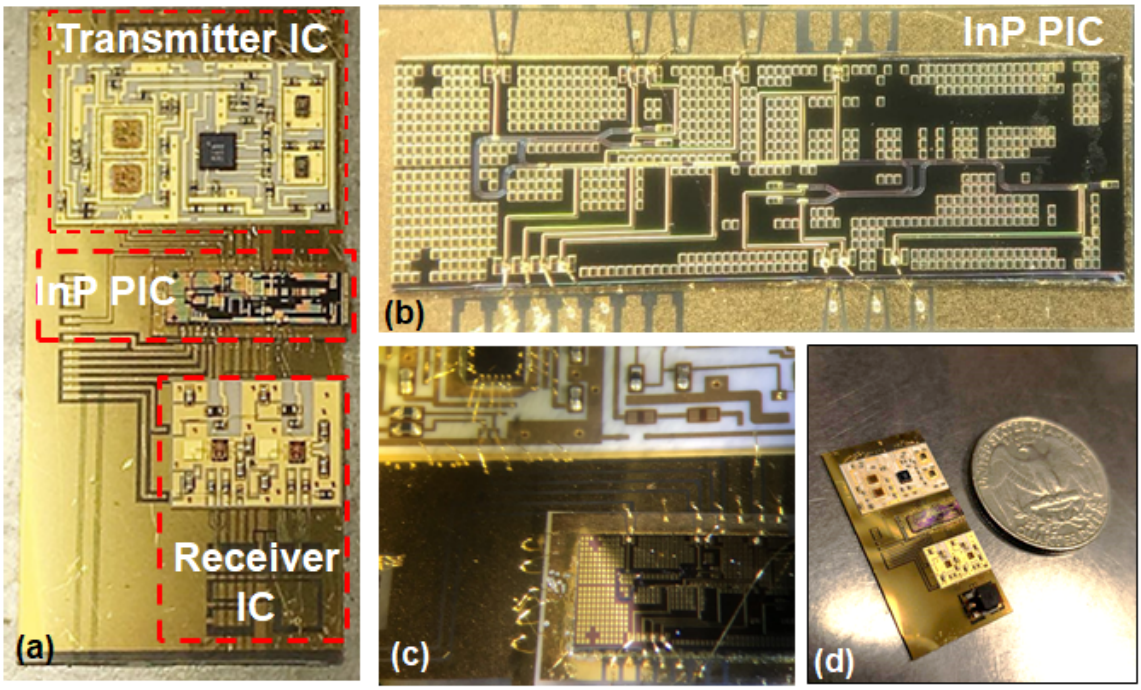


Figure 4.16: (a) Top-view image of the supper carrier with transmitter IC, InP PIC and receiver IC. (b) InP PIC mounted on small sub-carrier. (c) The optical-electrical integration by wire bonding. (d) Picture of whole integrated lidar transmitter system with a coin.

Chapter 5

Silicon Photonics Device Fabrication

SiPh has become a leading solution for PICs used for applications including high performance computing, communications, sensing [93], and on-chip interconnects [94]. The benefits provided by SiPh over other PIC platforms include the use of existing CMOS foundries, co-integration with micro-electronics and access to advanced fabrication equipment supporting nanometer scale control and heterogeneous growth of germanium on silicon [95]. Some products have been developed [96]. However, these mature CMOS foundries are offered only to a limited number of external users. There is a large demand for accessing these facilities to make SiPh devices at an affordable cost, both for research and commercial prototypes. To leverage the cost and performance of CMOS foundries, multi-project wafer (MPW) service were developed for SiPh to process aggregated designs serving multiple customers per process run. This is commonly done in the IC industry [97]. Several initiatives have been taken worldwide to set-up MPW platforms for SiPh. To name a few, OpSIS-IME from Singapore [98], AIM from the U.S. [99], IMEC from Europe [100].

In the first part of this chapter, SiPh designs based on MPW offerings will be reviewed. Different foundries feature different technologies. The process design kits (PDKs) are pro-

vided by the SiPh foundries. The users can design and simulate based on the PDK, tailoring it to their specific application. A mature PDK includes developed device building blocks, a set of design rules and technology description including layer names, dimensions and purposes. Some recently developed PDKs for SiPh MPW offerings also include simulation models for modulators and photodetectors for system-level modeling. The devices layers thickness, etching depth, metal and via opening rules may vary from foundry to foundry. This will lead to different grating coupler designs for 3D hybrid integration.

Although the MPW offerings offers access to state-of-the-art CMOS processes to make SiPh PICs, this concept poses several disadvantages. First, the lead time between the design submission and delivery of the fabricated chips is long; within a certain project development time, only one version of a design can be fabricated. Improving and fixing errors of a design (which is common for R&D projects) may not be possible with the extensive lead times. Second, the processes provided by the foundries are limited to fixed design rules. For example, the etch depth of the grating teeth is an important parameter for coupler designs because the grating strength is directly related to the etching depth. The etch depth could be tuned to achieve higher coupling efficiency between the RSOA to on silicon waveguide, but a fixed process from a foundry, such optimization is not possible. Last, the disadvantage of using SiPh MPW services for 3D hybrid integration is the limited chip real estate. The cost of real estate of current SiPh MPW is high. An InP RSOA array occupies a large area on the SiPh chip that could be used for other valuable devices such as modulators and photodiodes. To overcome these disadvantages, an in-house passive PIC process was developed. The details are described in the second part of this chapter.

5.1 Imec-ePIXfab SiPhotonics: Passives Technology

Some of the passive SiPh devices used in this work were developed with Imec-ePIXfab SiPhotonics: Passives Technology [101]. A simplified version of the device cross-section for this technology is shown in Fig. 5.1. The passive technology is based on SOI with a 220 nm silicon device layer and a buried oxide layer of 2 μm. Although ridge and full silicon etched strip waveguide are both available, the most commonly used waveguide is the fully etched strip waveguide. The platform features a partial etched layer on silicon with 70 nm and 160 nm etching depth. With the partial etch, a grating coupler can be made. This corresponds to the standard grating coupler design described in section 3.2.1. The primitive building blocks include fiber grating couplers with a insertion loss of 7 dB, MMI couplers and Y-splitters. The strip waveguide loss is 3 dB/cm and the rib waveguide loss is 0.5 dB/cm. There are two options for the top waveguide cladding, photoresist or oxide. The oxide cladding thickness is 1.25 μm with planarization. The minimum width of lines (and spacings) is 150 nm. Custom devices can be made that accord with the design rules. The imec-ePIXfab SiPhotonics Passives Technology is ideal for making passive SiPh devices such as resonators, filters and polarization rotators. This platform does not have Ge photodiodes or any other active devices. A metal layer is not offered by this platform. The bonding metal pads for 3D hybrid integration needs to be fabricated later with post processing. The foundry offers two dicing options for the passive chip runs. In this work, the die size is larger than the design region to facilitate the post processing.

Figure 5.2 shows the mask design of for passives imec-ePIXfab SiPhotonics platform. The bonding pads for the InP RSOA are reserved by using strip waveguide layer. A large area of silicon waveguide is defined to maintain a flat surface for the metal pads for the flip-chip bonding process.

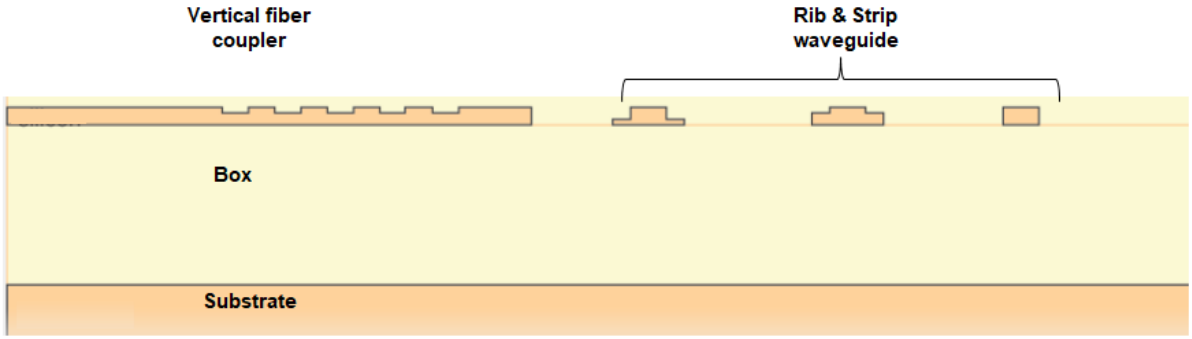


Figure 5.1: Schematic cross-section of the imec-ePIXfab SiPhotonics Passives Technology.

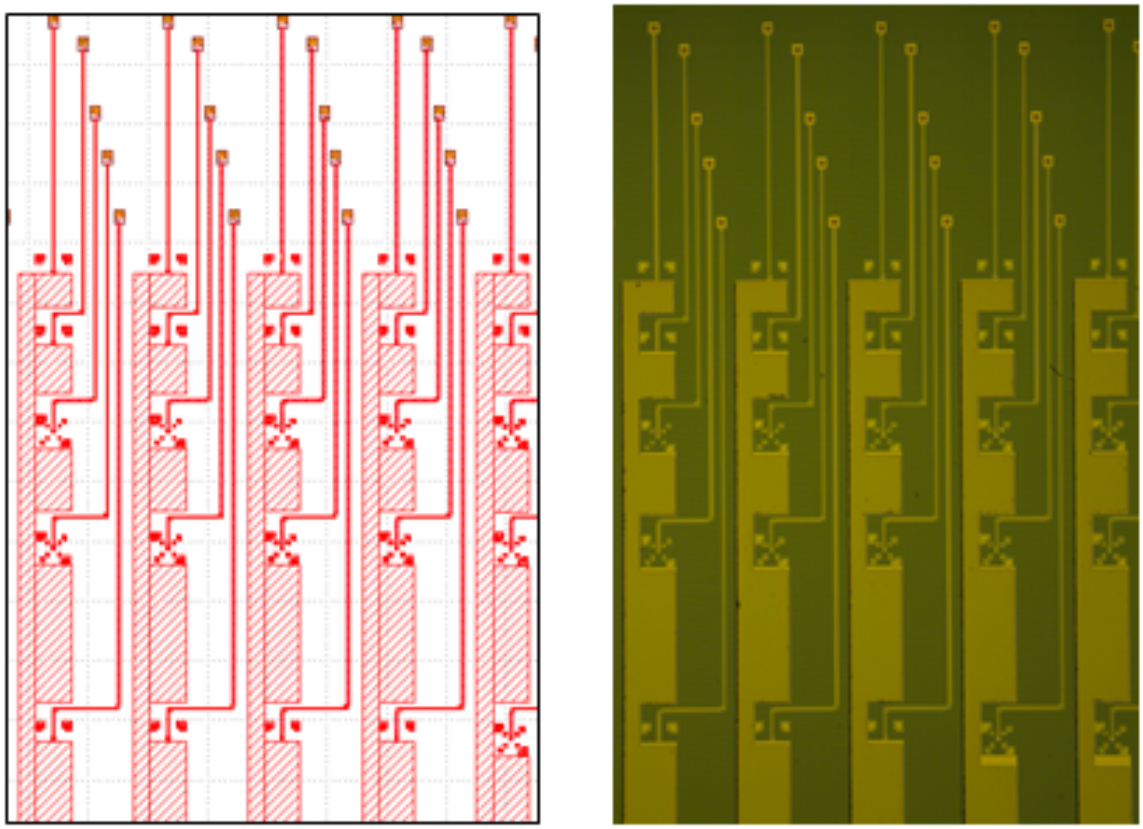


Figure 5.2: Top-view schematic layout of a passive SiPh chip for 3D hybrid integrated laser (left) and microscope image of fabricated chip (right).

5.2 Imec-ePIXfab SiPhotonics: Active technology

5.2.1 Imec-ePIXfab SiPhotonics: iSiPP25G

The active SiPh platform used in this work is the Iimec-ePIXfab SiPhotonics: iSiPP25G [102]platform. The SOI wafer is 220 nm silicon device layer with a 2 μm BOX. The 220 nm device layer is etched with three etch depths as shown in Fig. 5.3: fully etched strip waveguide layer, a deep etch layer with a slab of 70 nm left and a shallow etch layer where the silicon device layer is etched 70 nm. The variation of waveguide etching depth enable users to design based on three mode confinement conditions that support diverse trade-offs between bending radius and propagation loss. The silicon waveguide device fabrication utilizes 193 nm deep-UV lithography and RIE etching to e features as small as 150 nm. A high quality CVD oxide cladding is used to ensure low optical propagation loss. The cladding layer is planarized by CMP for poly-Si deposition. As explained in section 3.2.2, the poly-Si overlay is key for high coupling efficiency on 220 nm SOI. This layer of poly-Si was deposited directly on top of the silicon device layer. By fabricating the grating teeth in a region where the poly-Si is deposited, better coupling efficiency for the grating coupler can be achieved compared to the standard SOI 220 nm grating coupler. This technology is ideal 3D hybrid integration technology for the following reasons. First, the minimum line and space is 150 nm, which is suitable to make DBR mirrors for external cavity lasers. Second, the poly-Si overlay can enable high coupling efficiency grating couplers to couple light from the RSOA. Last, active components including modulators and photodiodes can be integrated with advanced passive devices such wavelength combiners and filters to build multi-channel transceivers.

Compared to the Passives platform, imec-ePIXfab SiPhotonics: iSiPP25G features various doping profiles to the silicon to realize heavily doped, medium doped and lightly doped regions. Both n-type and p-type silicon waveguide structures can be realized. It

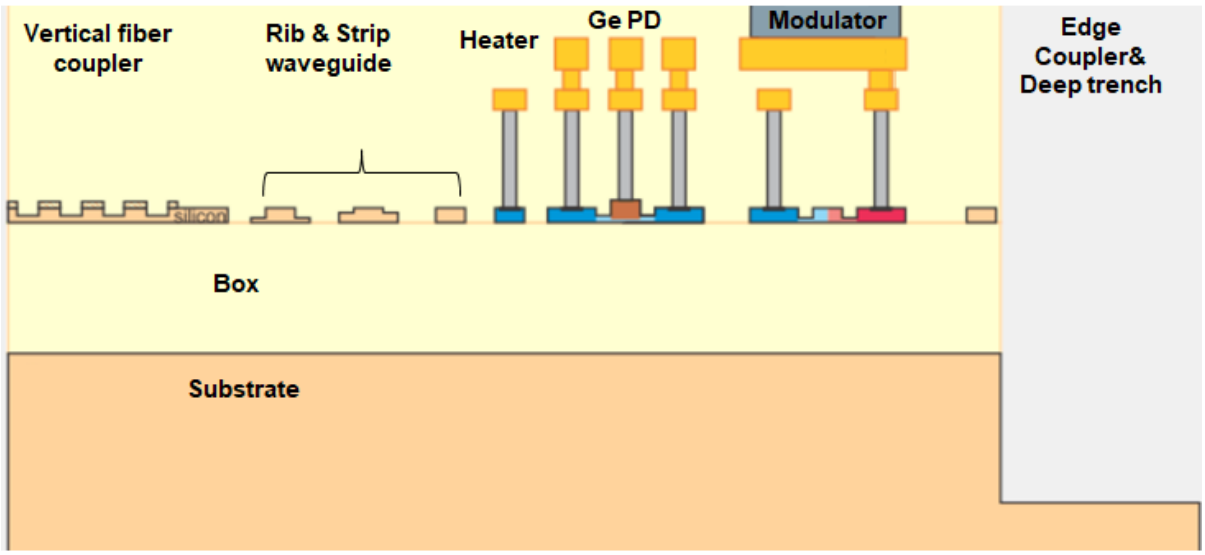


Figure 5.3: Schematic cross-section of the imec-ePIXfab SiPhotonics: iSiPP25G.

is important to have multiple doping profiles on silicon: high doping enables low contact resistance while medium to low doping enables diode p-n junctions for modulating the silicon waveguide refractive index with low insertion loss. Mach-Zehnder modulator (MZM) [103], ring modulators [104], optical phased arrays [105] and side waveguide heaters can be fabricated for various photonics applications [106] using the doping profiles available. Germanium is also included in this platform for photodiodes. Electro-absorption modulators can also be realized using the Ge as the absorbing medium [107]. The fabrication complexity for active SiPh platform is significantly higher than that for the passive SiPh platform. Via and metalization steps are incorporated into the fabrication process for making electrical connections. Some of the fabricated active SiPh components are shown in Fig. 5.4.

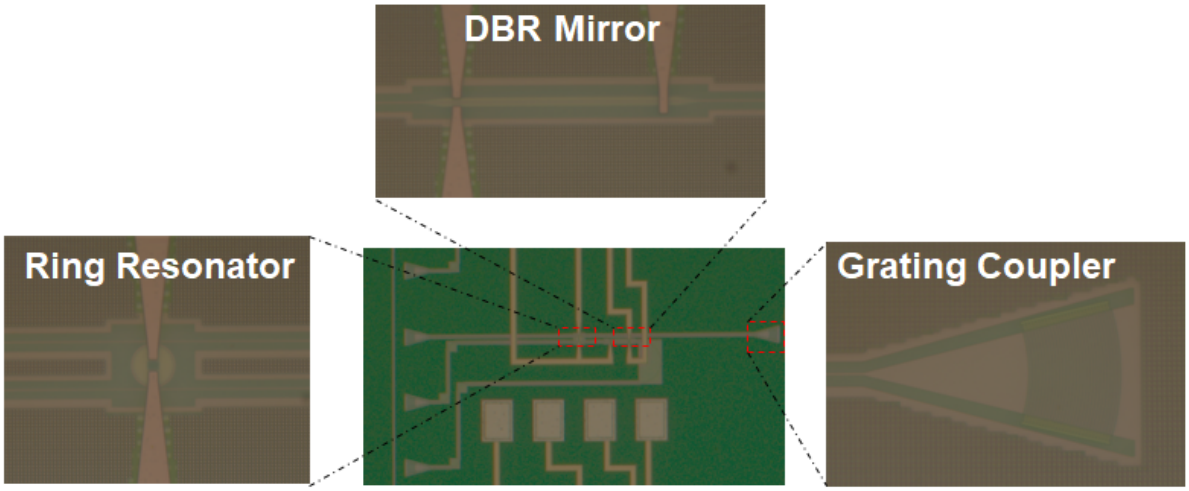


Figure 5.4: Top-view microscope picture of an external cavity fabricated by imec-ePIXfab SiPhotonics: iSiPP25G.

5.2.2 Other Silicon Photonics Foundries

There are other SiPh foundries around the world that provide MPW service. In the U.S., the American Institute for Manufacturing Integrated Photonics (AIM Photonics) provide fully SiPh platform based on 300 mm SOI wafers. The PDK from AIM Photonics includes extensive components (for modulation and detection, low loss passives, and fiber-to-chip couplers, etc.), Design rule check (DRC) is available across multiple software packages. A passive interposer is also available. Institute of Microelectronics (IME) in Singapore also provides a full SiPh platform. Both AIM and IME feature SixNy waveguide layer on top of silicon device layer. The SixNy layer can be used to build low loss waveguide aims for large scale interposer integration. The SixNy thickness varies from 100 nm to 400 nm. The oxide gap between the SixNy and silicon waveguide is typically 100 nm. Light can couple from one layer to anther with waveguide transitions. The loss of the transition can be as low as 0.1 dB. For the 3D hybrid integration platform, the SixNy layer is useful because high coupling efficiency gratings can be realized by combining both the silicon and SixNy device layers. The details of the design for such a

dual layer grating coupler can be found in section 3.3. The dual layer grating is not only useful for 3D hybrid integration but also beneficial for fiber couplers.

5.3 Passive Silicon Photonics Fabrication

Regarding the use of the deep-UV stepper for in-house passive SiPh chip fabrication, there are several considerations. First, only 4-inch wafers can be used. The cost of 4-inch SOI wafers is high. Although it is possible to use pieces in the stepper, the process development of using pieces is time consuming. Also, the masks for the deep-UV stepper are expensive. The lead time of the mask fabrication itself is long, which is not optimal for fast turn over for the rapid prototyping. The grating development for the 3D hybrid integration requires fast turn over between each iteration to optimize the fabrication process and design parameters.

To overcome these issues, EBL is used for in-house passive SiPh chip development. The EBL system used for SOI fabrication here is the same as the one used for grating fabrication for InP lasers from chapter 4. This system uses the vector scan approach for electron beam deflection within a field and repeats steps of stage movement between fields. The combination of vector scanning and repeating steps allows the entire area of up to 6 inches to be exposed. This feature makes this process suitable for small volume prototyping. Dynamic focus and stagnation control for improved writing performance across the entire scan field can also be achieved. A 20 nm minimum isolated line width is achievable, which is 10 times better than the deep-UV stepper, making it a good solution for high precision fabrication for waveguide gratings, polarization controllers and directional couplers with sub 100 nm waveguide gap. The fabrication process for SiPh using EBL includes wafer preparation, waveguide definition, dry etch and photoresist removal. The short process period makes this a good candidate for fast turn over between

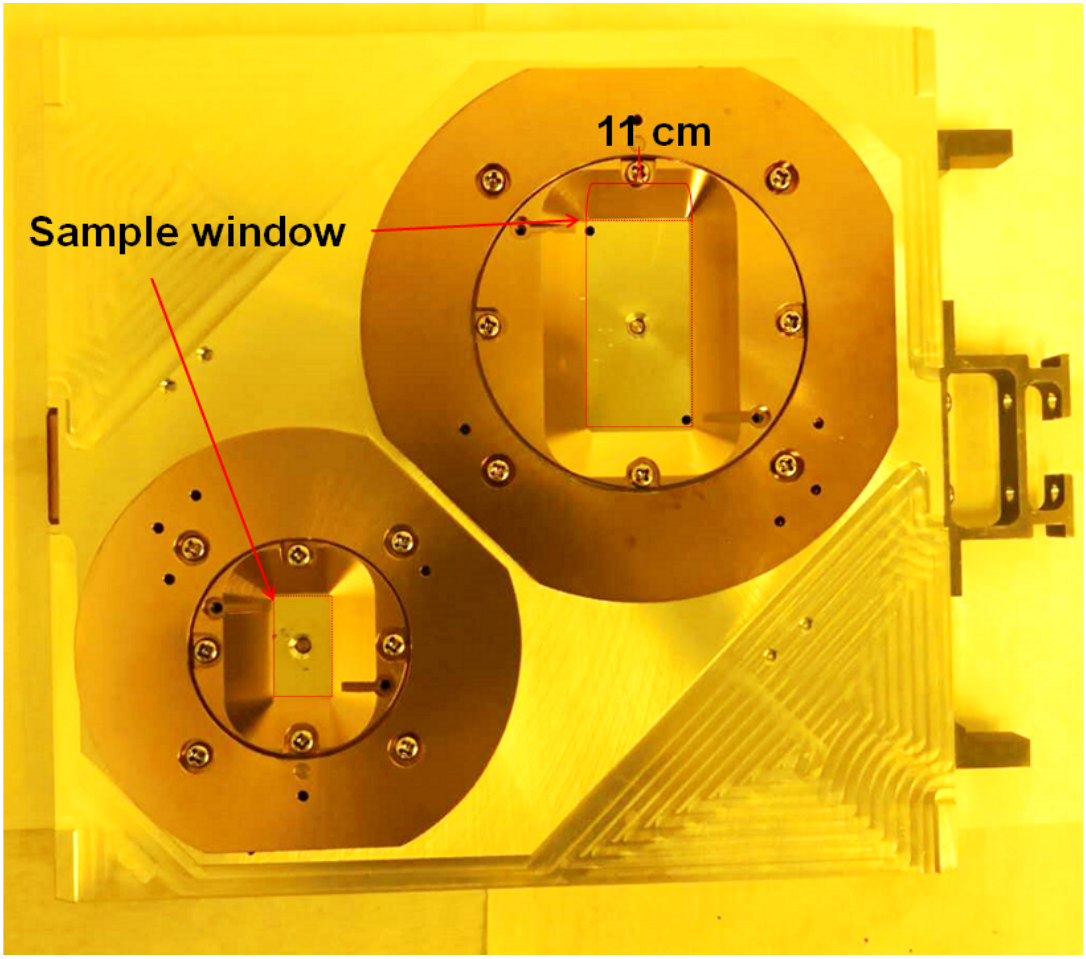


Figure 5.5: Picture of a sample holder in EBL for holding small pieces.

iterations for grating coupler development.

5.3.1 Wafer Preparation

The SOI wafer used in this work has a 500 nm thick silicon device layer and a 1000 nm BOX layer. Small pieces are used, which are diced from 8 inch diameter 1 mm thick SOI wafers. The size of the piece only needs to be large enough to be loaded in the EBL system wafer holder. Figure 5.5 shows a picture of the sample holder used in the EBL system in this work.

When purchased, the SOI wafers' surfaces are coated with photoresist for protection.

Following cleaving from 8 inches, solvent cleaning is used to first remove the photoresist from the surface. Then H_2SO_4:H_2O_2 3:1 in a heated bath is used to further clean the surface. The bath temperature is 160°C and the soaking time is 10 minutes. The last step of the wafer preparation is a BHF dip to remove the surface oxide and also to ensure the surface is hydrophobic. It is important to perform this step before the EBL resist spin process.

5.3.2 Negative Electron Beam Lithography Resist

To reduce the EBL exposure time, which is the most time-consuming part of the process, a negative EBL resist is used. For the strip waveguide fabrication, the waveguide region is exposed by the electron beam, this is a small region compared to the entire wafer area. The ma-N 2400 photoresist is used, which is an electron beam and deep-UV sensitive negative tone photoresist. The pattern resolution is 20 nm. The ma-N 2400 also features an aqueous alkaline development that is commonly used in fabrication processes. It is easy to remove with oxygen plasma or common solvent. The ma-N is available in a variety of viscosities for different thickness coatings. Dose optimization needs to be conduct prior to fabrication based on the substrate type and thickness of the resist. In general, the ma-N photoresist requires a higher dose compare the positive tone resist used in EBL. The optimized electron beam dose does not drift as much as the positive resist. After the BHF treatment, ma-N is spun coated on the sample and baked at 95°C for 1 minute. A layer of aluminum which is 9 nm, is deposited on the sample surface at room temperature. The layer of metal helps to spread the electron beam and prevent local charging in the EBL chamber. It is important to use a thermal metal evaporator for the aluminum coating to avoid UV expose before the EBL process. To reduce the oxidation of the aluminum film, the sample is loaded into EBL chamber immediately after being

removed from thermal evaporator.

5.3.3 Expose and Develop Processes

The EBL does not require a physical mask to project the design on to the wafer. Instead, the mask design file is converted by the commercial software BEAMER into the readable file for the EBL control system. Figure 5.6 shows the schematic design of the waveguide structures and the converted exposure map for the EBL system. The boxes around the waveguide structures in Fig. 5.6(b) represent the exposure sequence map. As shown in Fig. 5.6(b), the long waveguide structure is not contained within a single exposure field. Due to the limitation of the beam focusing system, the maximum exposure window size is 500 μm by 500 μm. Any structure that designed larger than 500 μm will be executed by a program-controlled stage movement and field splicing. The writing sequence within a field and in between the fields are adjustable and also requires optimization for a smooth waveguide surface.

After the exposure, the sample is developed in AZ 300 metal ion free developer for 70 seconds. The aluminum on top of the sample is dissolved by the developer at the same process. Figure 5.7(a) and (b) show a fiber grating coupler design and the corresponding resist pattern of the structure after the development process, respectively.

5.3.4 Inductively Coupled Plasma Reactive Ion Etching

The strip silicon waveguide features a very high refractive index contrast, which leads to strong light confinement in the silicon (n = 3.45) core for waveguide structures surrounded by SiO_2 (n = 1.45) cladding. To reduce insertion loss and the phase error for the strip silicon waveguide, a dry etch process with smooth and vertical sidewalls is critical. The ICP source generates a high-density plasma due to the inductive coupling from the

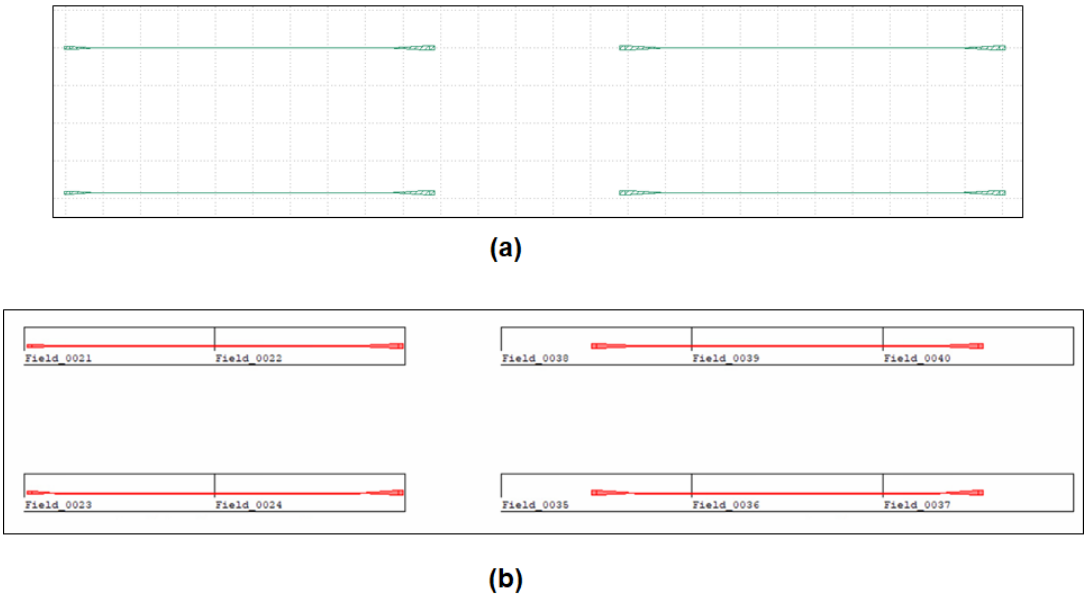


Figure 5.6: (a) Schematic layout of the waveguide structures for EBL and (b) converted exposure map for the EBL system.

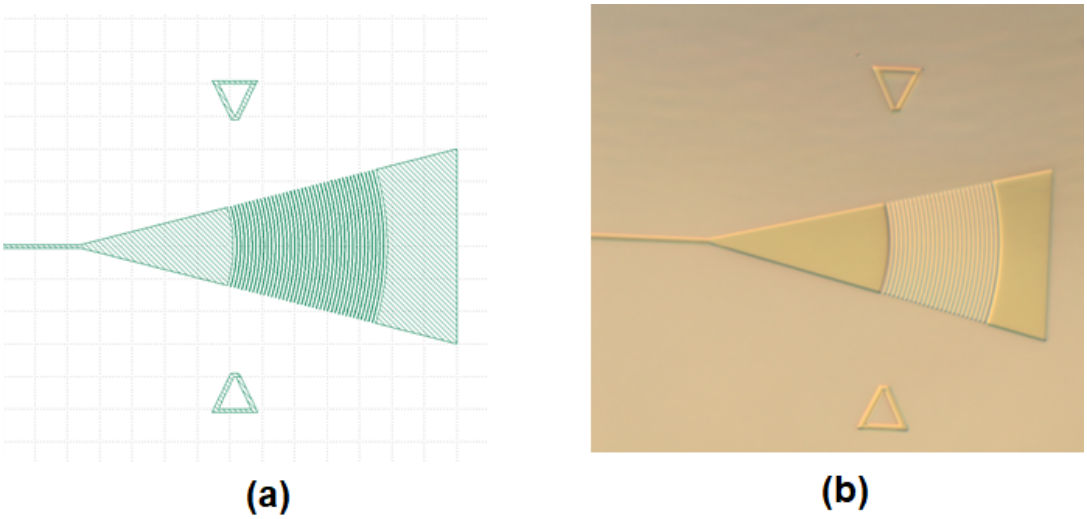


Figure 5.7: Conventional grating coupler fabrication using EBL. (a) Schematic design and (b) resist pattern after development.

RF to the plasma, which is ideal for etching the silicon waveguide. Fluorine-based ICP-RIE has been used for silicon waveguide etching for various applications [108][109]. It is reported that SF_6 generates an undercut etch profile [110] while CF_4 produce a sloped

sidewall profile [111]. To ensure a vertical the sidewall, a CF_4/SF_6 plasma is used. A vertical etch profile with smooth sidewall is achievable [112].

In this work, the following etch condition was used: C_4F_8 flow = 60 sccm, SF_6 flow = 24 sccm, CF_4 flow = 27 sccm, chamber pressure = 20 mTorr, RIE bias power = 100 W and ICP power = 950 W. The selectivity of silicon to ma-N using these process conditions is greater than 3:1. The etch rate for the silicon is approximately 300 nm/min, which is roughly 10 times faster than that for the SiO_2. TO etch the strip waveguide, a small amount of over etch is used (5 seconds), which does not disturb the waveguide structure. However, if the etch depth needs to be controlled precisely, the in-situ laser monitor can be used. By using the laser monitor, the etch depth can be controlled within the range of tens of nanometers. Before the heated bath strip, the sidewall is coated with a polymer that will potentially increase the waveguide loss. The etched sample is first soaked in NMP photoresist stripper for 2 minutes. To further reduce the etch residue on the waveguide, H_2SO_4:H_2O_2 3:1 heated bath is used for strong photoresist striping. Figure 5.8 shows a directional coupler structure under high magnification SEM after the photoresist is stripped, a clean waveguide side-wall profile is evident.

5.3.5 Elevated Grating Coupler

The elevated grating coupler can be fabricated by using the in-house develop EBL process. The elevated grating coupler features higher grating teeth than the adjacent waveguide layer. Compared to the elevated grating, the commonly used grating coupler in SiPh features identical thickness for the grating region and the waveguide region. As it shown in Fig. 5.9, the grating teeth and slab waveguide are both defined during same step. The grating trench and waveguide are fabricated within one dry etch. For a total silicon device layer that under 450 nm, this grating coupler can be used because higher order

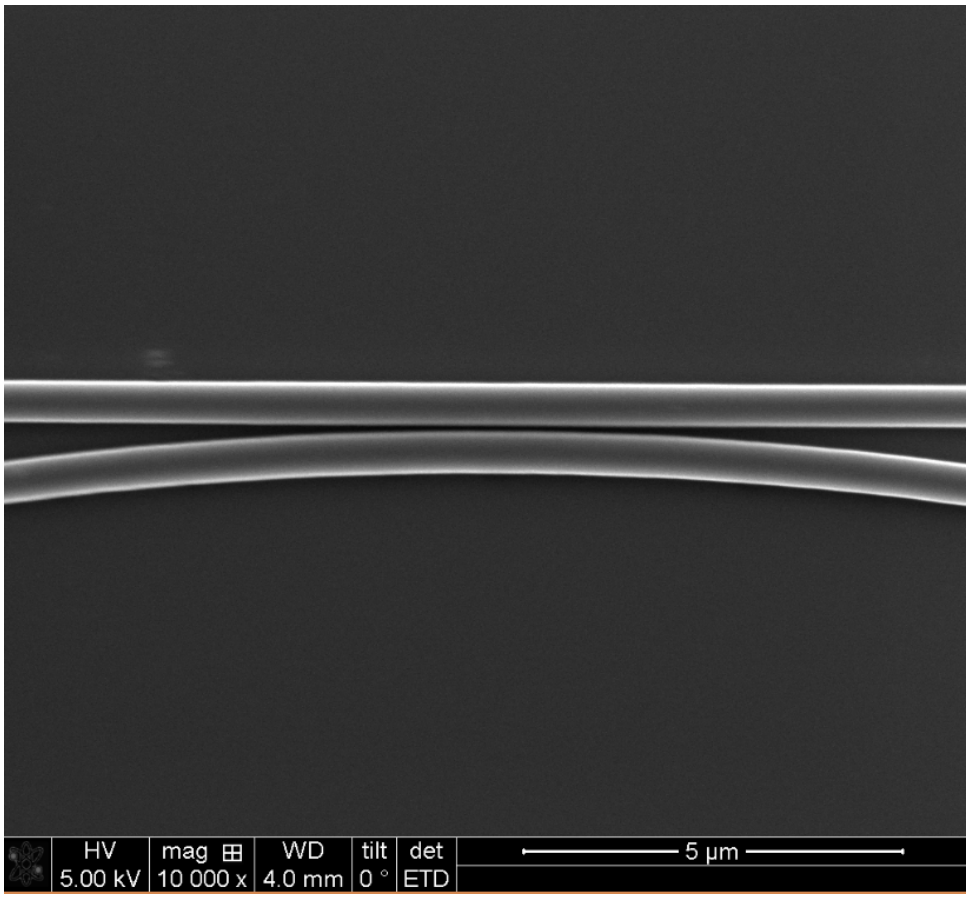


Figure 5.8: Directional coupler structure under high magnification SEM following resist stripping.

optical modes will not be excited for such thin [113]. However, for a total silicon device layer of 500 nm, this grating structure will introduce significant insertion loss because higher order mode will be excited in this thicker waveguide. The ideal grating coupler for SiPh both for 3D hybrid integration and fiber coupling is to have a thick grating region for high grating strength and a thin waveguide region for low insertion loss. To achieve that, the elevated grating based on the poly-Si overlay on silicon waveguide is used [114]. However, this approach can only be realized in a CMOS foundry and requires development time.

In this work, a novel way of realizing the elevated grating coupler is proposed based

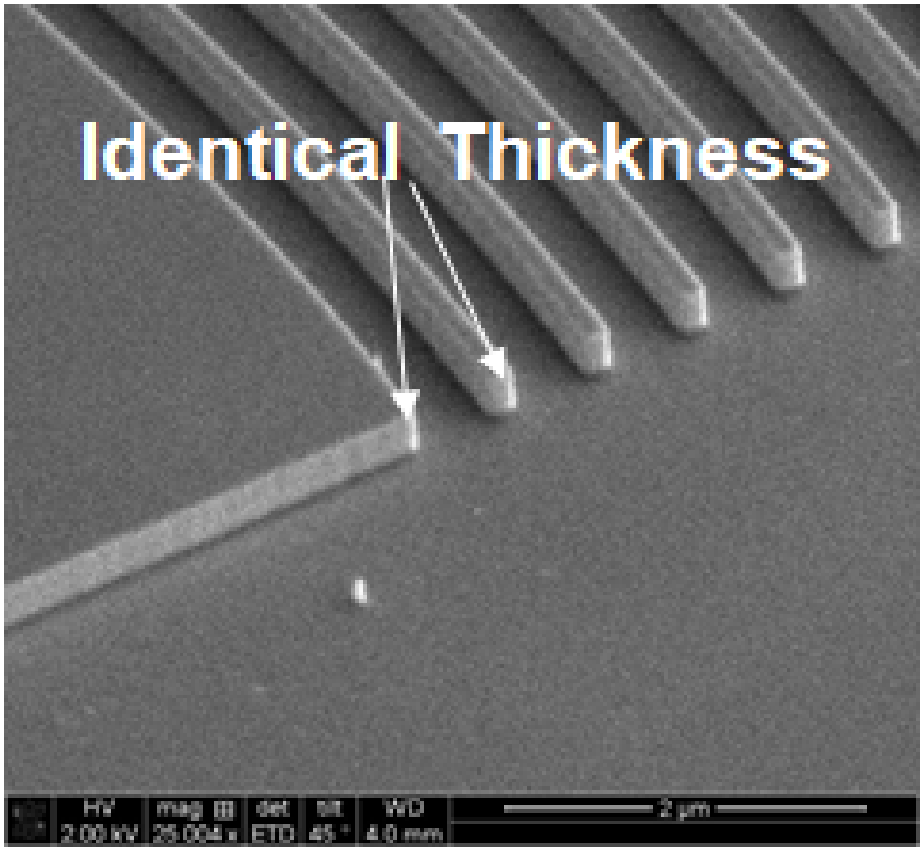


Figure 5.9: Grating coupler made with single etch step with top of the grating teeth and waveguide at same height.

on dual EBL and dry etches in ICP-RIE. The fabrication process is shown in Fig. 5.10. The first lithography step was used to define the grating and alignment markers as shown in Fig. 5.10(b). The depth of the of the first etch is controlled with the laser monitor so that the optimized etch depth for the grating coupler design can be achieved. As shown in Fig. 5.10(c), after the first etch, the top of the grating teeth has the total thickness of the silicon device layer while the other regions are etched. It is important to use negative tone resist for this step. The second lithography step defines the waveguide structure as shown in Fig. 5.10(d). The second ICP-RIE etch defines the waveguide structure. A perspective view SEM picture of a fabricated elevated grating coupler is shown in

Fig. 5.11. The elevated grating for the 500 nm silicon passive platform provides higher coupling efficiency from the RSOA. Simulation results show that for the elevated grating coupler, the coupling efficiency from the RSOA to the silicon waveguide can be as high as 70%.

5.3.6 Passive Silicon Photonics Components

The EBL process provides fast turn over time for passive SiPh components. The cost and lead time of each design-testing iteration using EBL is significantly lower than that using the deep-UV stepper process. Different passive components are fabricated by the in-house SiPh EBL process, as shown in Fig. 5.12. These passive components can be used to make an external cavity laser for advanced laser devices.

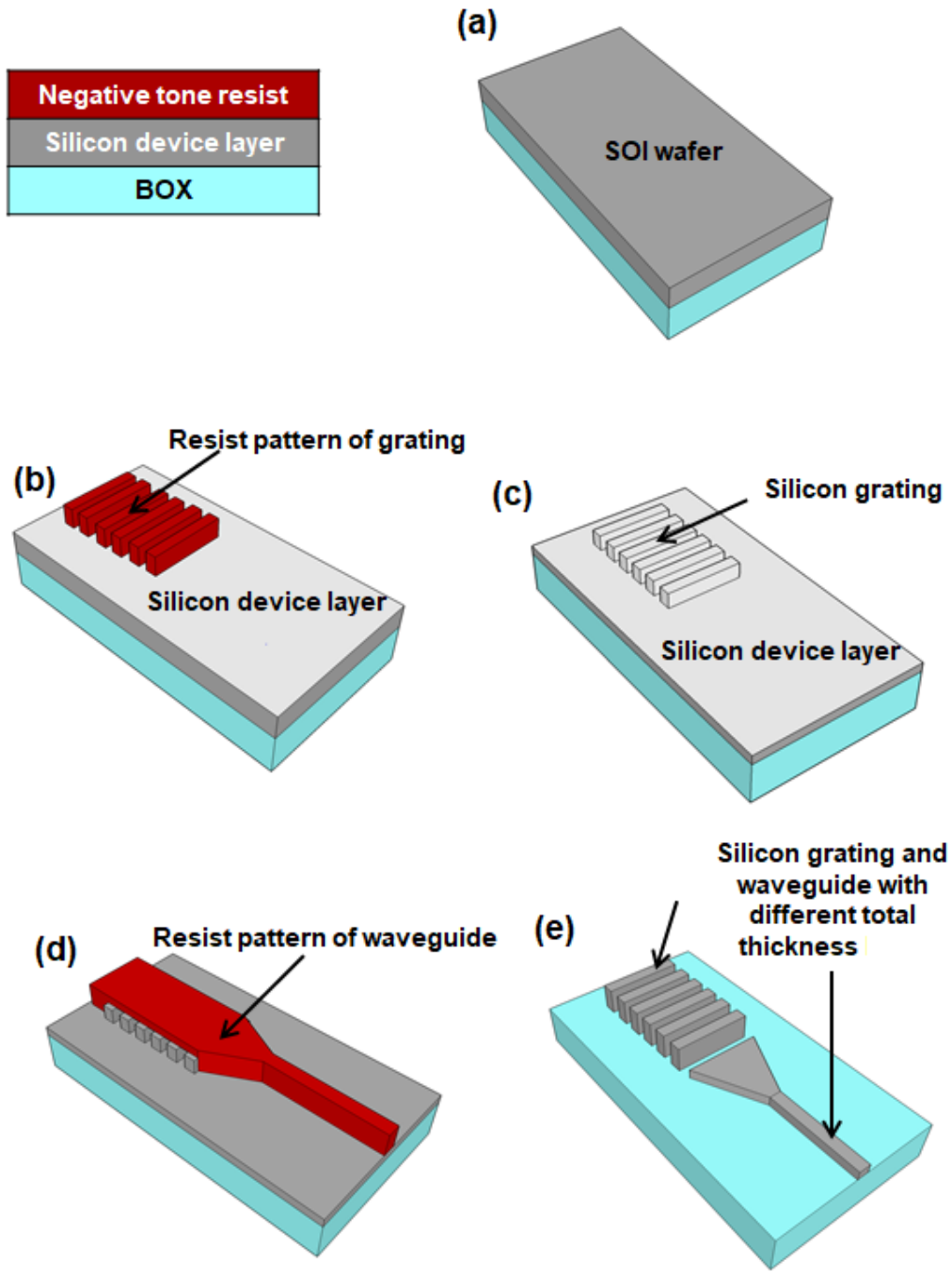


Figure 5.10: The fabrication process of the elevated grating coupler through dual EBL (a) SOI wafer (b) first EBL define the grating area (c) first ICP-RIE etch to transfer the pattern to SOI layer (d) second EBL to define the waveguide region (e) second ICP-RIE etch to make the elevated grating coupler.

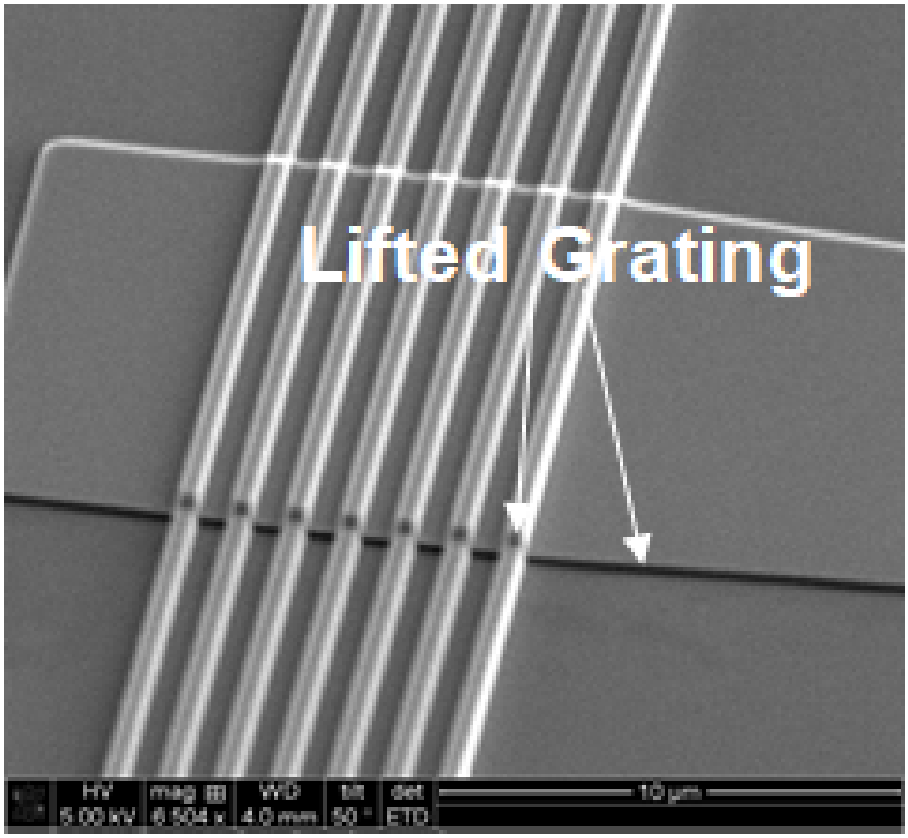


Figure 5.11: Perspective view SEM picture of fabricated elevated grating coupler

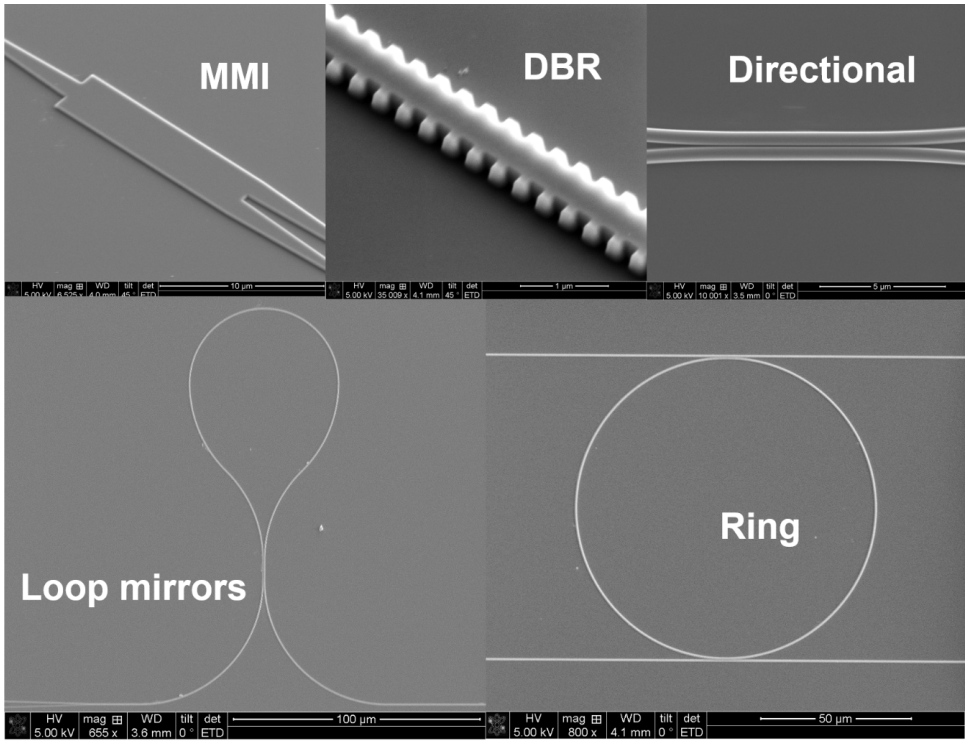


Figure 5.12: Passive components fabricated using EBL process including MMI coupler, in-plane waveguide DBR mirror, directional coupler, loop mirror and ring resonator.

Chapter 6

Flip-chip Integration

3D integration has been recognized as a promising solution to reduce the length of interconnects and, furthermore, to satisfy the demand for highly integrated optoelectronic systems [115]. Conventional photonics packaging relies on horizontal connects with long wires between substrates and pads through wire bonding, which is cumbersome and not cost efficient. It also suffers from low throughput since each wire end must be individually connected. Another disadvantage of wire bonding is the low integration density [116]. To solve the issues of wire bonding, 3D integration was pursed [117]. It provides an effective solution to vertically integrate different chips and devices [118] into the same package with compact footprint. By replacing the wire connections with vias, the size, weight, power and cost of the packaged device can be reduced [118]. 3D integration also allows for integration of different materials. The logic behind the 3D packaging matches with the motivation for 3D hybrid integration technology developed used in this work [119].

This chapter reviews flip-chip bonding related topics with emphasis on PIC where alignment tolerance is critical. Compared to conventional electrical interconnections, PIC packaging is more sensitive to misalignment between optical interfaces. Section 6.1 introduces the state-of-art packaging technologies including wire bonding and flip-chip

bonding. The concept of a photonics interposer is also described. Then the details of the implementation of thermocompression and solder reflow bonding is described in section 6.2. Bonding process that feature self-alignment features are discussed. Lastly, a novel metalization method for InP devices is discussed with emphasis on CMOS compatible contact fabrication in section 6.3.

6.1 State-of-Art Packaging Technology Review

6.1.1 Wire Bonding

Cost, performance and footprint need to be well balanced in photonics packaging. Wire bonding seems outdated but is still widely used since it is the most flexible and cost-effective method for packaging PICs [120]. In general, bond wires are made of gold (or copper [121]). Surface treatment can improve adhesion between wires and pads, but is not required [122]. Ball bonding and wedge bonding are widely used. Thermocompression and ultrasonic are conventional bonding techniques to establish mechanical adhesion between wires and pads. For thermocompression bonding, pads and wires are heated. A thermal hierarchy poses a restriction on those devices which cannot survive high processing temperatures. Ultrasonic wire bonding uses ultrasonic friction on pads' surfaces before the wires are attached. The adhesion and reliability are increased compared to untreated pads' surface [123]. Thermosonic wire bonding was later proposed to combine both advantages from thermocompression and ultrasonic bonding [124]. Nowadays, the thermosonic wire bonding is most common in industry for packaging.

Dense interconnects with a pitch of 35 μm are achievable using thermosonic wire bonding based on gold wires [126]. To further increase the integration density, low-profile wire bond loops are required. Bond loops with 50 μm loop height are reported

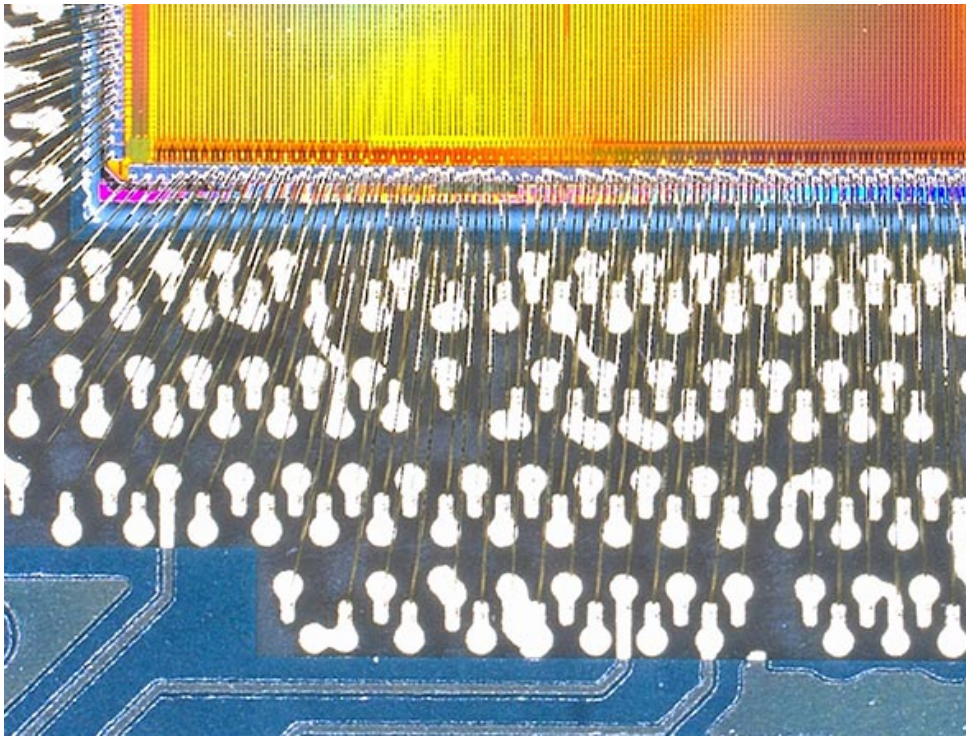


Figure 6.1: High-density wire bonding [125].

in volume production [127]. For high-speed applications, ribbon bonding attachment is used [128]. The rectangular cross section of the ribbon wires provides lower inductance and lower skin effect losses at high frequency [129]. As shown in Fig. 6.1, novel ideas and advanced technology improvements for wire bonding continue to increase the integration density [130]. However, a bond loop less than 20 μm is difficult to achieve, to further increase density, flip-chip technology is utilized.

6.1.2 Flip-chip Bonding

Flip-chip bonding is a standard packaging technology to make electrical interconnections between semiconductor devices. This face down assembly technique developed originally by IBM, is known as controlled-collapse chip connection technology [131]. Flip-chip bonding provides excellent performance and allows for cost-effective interconnections

with shortened electrical path lengths [132] [133]. Figure 6.2 shows the basic 3D schematic of the controlled-collapse chip connection.

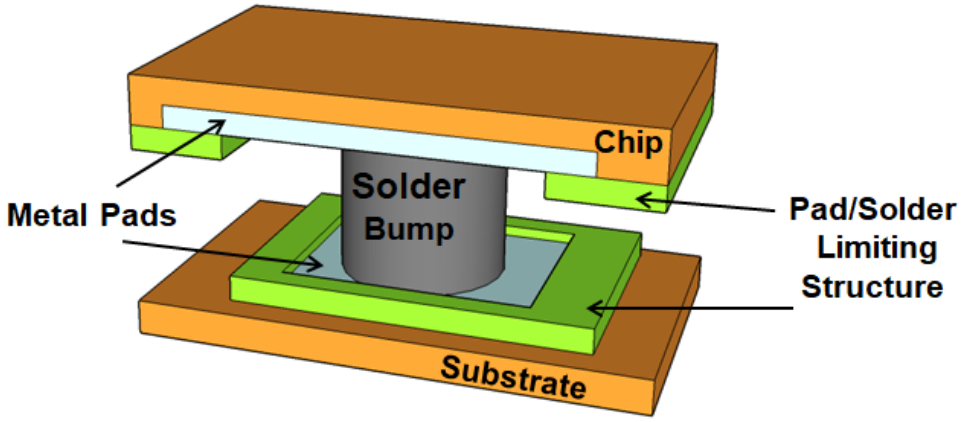


Figure 6.2: 3D schematic of controlled-collapse chip connection.

Gold is a commonly used material for pads (or bumps) fabrication in flip-chip bonding because of its supreme electrical and thermal conductivity. Also, gold is used as the final metallization layer for III–V semiconductors making it more promising for InP device packaging [134]. Solder bumps can be created on at wafer level for high throughput processes used for flip-chip bonding [135]. Solder materials used in flip-chip bonding processes include AuSn, SnPb, and SnAg. A typical bump diameter is 30 to 100 μm with a bump height of 30–60 μm for general photonics flip-chip bonding processes. Compact bumps with 20 μm diameter and a minimum pitch of 50 μm have been reported to increase pad density [136].

Another commonly used flip-chip bonding technique is thermocompression, where the formation of the connection does not rely on solder material. Thermocompression bonding also features self-alignment processes to enhance alignment tolerance during the bonding process, which is introduced next. The self-alignment process is important for volume production because the throughput of a commercial bonding tool is often

limited by the alignment process. High placement accuracy often comes as the cost of lowering throughput. For example, the NOVAPLUS flip-chip bonder made by ASM AMICRA offers bonding cycle-time down to 3 seconds for AuSn based solder reflow with an accuracy of ± 2.5 μm. When increasing the alignment accuracy to ± 1 μm, the cycle-time is increased to 25 seconds with AuSn solder reflow. The throughput is significantly reduced.

6.1.3 Silicon Photonics Interposer

Large-scale integration between photonics and electronics is beneficial for various applications [137]. Generally, there are two types of approaches for photonic and electronic circuits integration. Monolithic front-end integration [138] and back-end integration using hybrid integration on a silicon photonics interposer. Monolithic integration provides higher speed and lower assembly cost than hybrid integration, but requires very strict CMOS compatibilities in terms of design, fabrication, and testing between photonics and electronics devices. The monolith process still needs time to mature for volume production. Hybrid integration on a SiPh interposer allows for optimization, fabrication and testing of photonics and electronics circuits separately, both realized through well developed and verified processes. The through-silicon-via (TSV) interposer make it possible to integrate both PICs and ICs together at low cost and with small footprint [139]. Compact and flexible interconnections can be realized between different chips and utilizing a TSV interposer. 3D hybrid integration offers an advantageous solution for photonics interposer integration due to the surface emission and vertical coupling nature of this technology. It allows light to couple vertically from chip to chip. High speed, broad bandwidth and high density input/output (I/O) are enabled by a TSV interposer in a 3D SiPh architecture. Flip-chip bonding is the key assembly technique for making con-

nections between vertically integrated chips. In the following sections, flip-chip bonding with emphasis on the self-alignment process is discussed.

6.2 Thermocompression Bonding

6.2.1 Thermocompression Process

Thermocompression is also known as diffusion bonding. This process creates a solid bond between two separate metal surfaces using pressure and heat [140]. The diffusion of metal atoms occurs by contacting the bonding metals on both sides after applying force and heat simultaneously. Metal pairs of gold-gold [141], copper-copper [142] or aluminum-aluminum [143] have been used. Thermocompression bonding is a promising technique for making high density interconnections. The thermocompression bonding processes can be carried out at wafer level for high throughput packaging [144]. The process generally requires surface preparation such as solvent cleaning. Surface activation techniques are used to further increase the bond strength. The surface activation is required for a low temperature bonding process. For high temperature thermocompression bonding, only solvent cleaning is required.

In this work, a Finetech Fineplacer Lambda tool was used for thermocompression bonding. Figure 6.3 shows a picture of the Finetech Fineplacer Lambda. The tool is designed for flip-chip bonding of single microchip pairs with an alignment accuracy of approximately 0.5 μm. The system runs in a semiautomatic configuration with full computer-controlled bonding and integrated side cameras for monitoring. Chip size from 500 μm up to 50 mm can be bonded using this tool. The bonding force varies from 0.3 N to 500 N. Bonding temperature can be as high as 400°C. The system also has a formic acid module (reduced atmosphere environment) that is used to prevent oxide formation

during heated solder bonding.

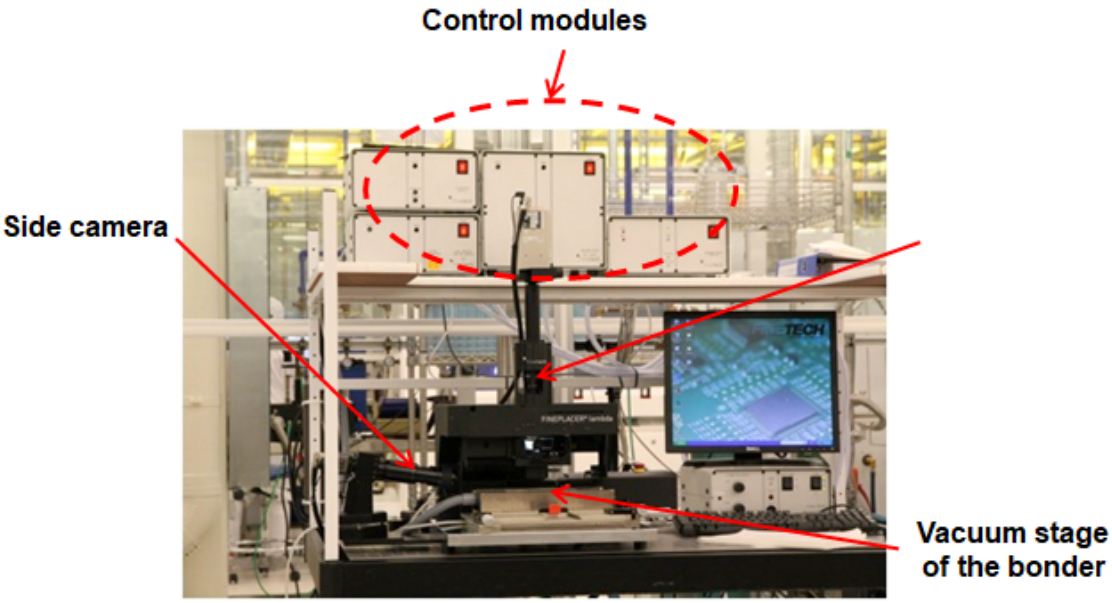


Figure 6.3: Finetech Fineplacer Lambda flip-chip bonder.

The 3D hybrid integration was carried out with this flip-chip bonder. The RSOA chip is picked up by the upper arm of the flip-chip bonder and the substrate (SiPh chip) is placed on the vacuum stage of the bonder. The coarse alignment of both chip and substrate is executed. Then the substrate is heated to an elevated temperature (half of the bonding temperature) to eliminate alignment error introduced by thermal expansion. A fine alignment process brings the chip and substrate to the final position. Then the pressure and heat are applied to the assembly by a computer-controlled program. In this work, thermocompression bonding with 350°C and 20 N force was applied. Figure 6.4(a) and (b) shows arrays of RSOA chips and the fabricated SiPh in a wafer box before they are bonded together. Figure 6.4(c) shows a plan view of a bonded InP RSOA chip. A top view microscope image of a 3D integrated laser structure with n-pad and p-pad is shown in Fig. 6.4(d). The n-pads of the 3D integrated laser are located on the backside

of the RSOA chip and the p-pads are on the SiPh chip.

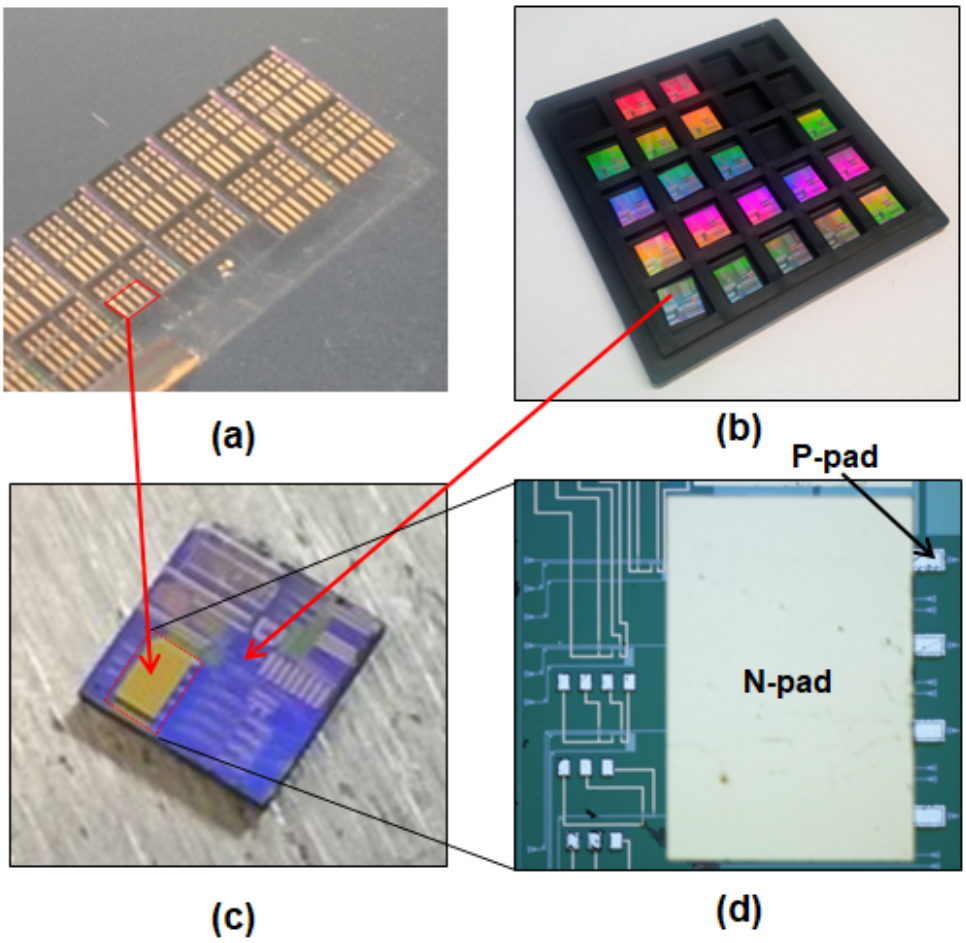


Figure 6.4: (a) InP RSOA array chip before bonding with p-contact facing up. (b) Fabricated SiPh chips before hybrid integration. (c) Plan-view image of a bonded RSOA chip on silicon. (c) Top view microscope image of a 3D integrated hybrid laser.

To evaluate the electrical quality of the metal bond, the current-voltage (IV) characteristics were measured both for a standalone InP RSOA and for a 3D integrated laser. The gain length was identical for both devices (1 mm). As shown in Fig. 6.5, the IV characteristics are nearly identical indicating that the metal bond makes a proper electrical connection and does not add resistance.

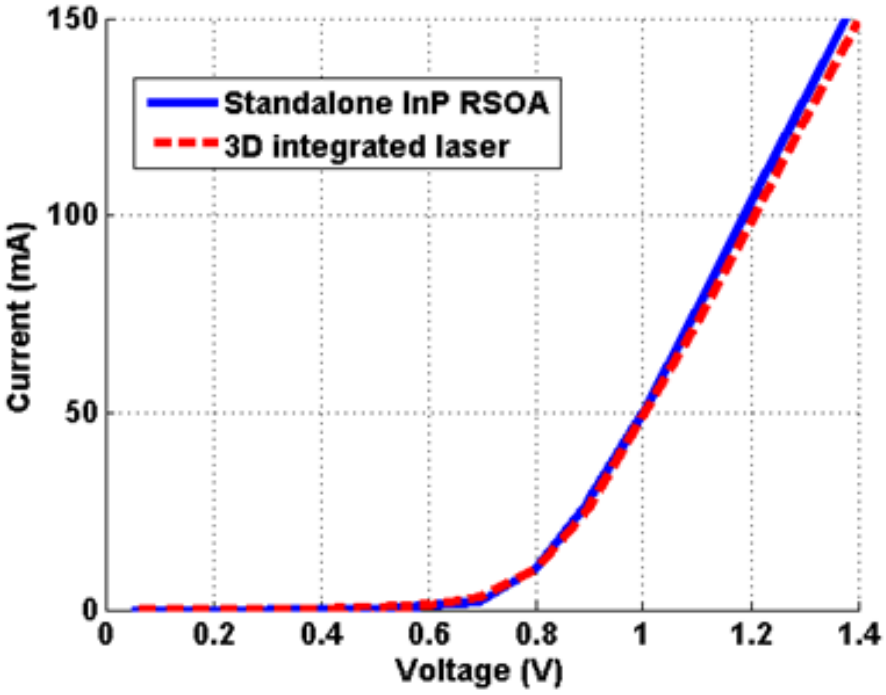


Figure 6.5: IV characteristics for 3D integrated laser and standalone InP RSOA.

6.2.2 Self-aligned Interconnection Elements

The placement accuracies of most commercial flip-chip bonding tools are limited to 2 μm – 5μm. The source of misalignment comes from thermal expansion between the bonding chip and substrate, and horizontal shifting of the chips due to the shear force generated during bonding [145]. For the 3D hybrid integration, the accuracy of the flip-chip bonding approach needs to be controlled without adding significant cost. Improving the alignment accuracy of the flip-chip bonding tool by simply increasing the resolution of the alignment stage mechanics and increasing the magnification of the monitoring camera are not cost effective for high throughput bonding.

A novel thermocompression bonding method was proposed to solve bonding accuracy issues while maintaining low cost [146]. Conventional bump and pad elements on the chip and substrate are modified to construct concave-convex pairs to form the self-aligned

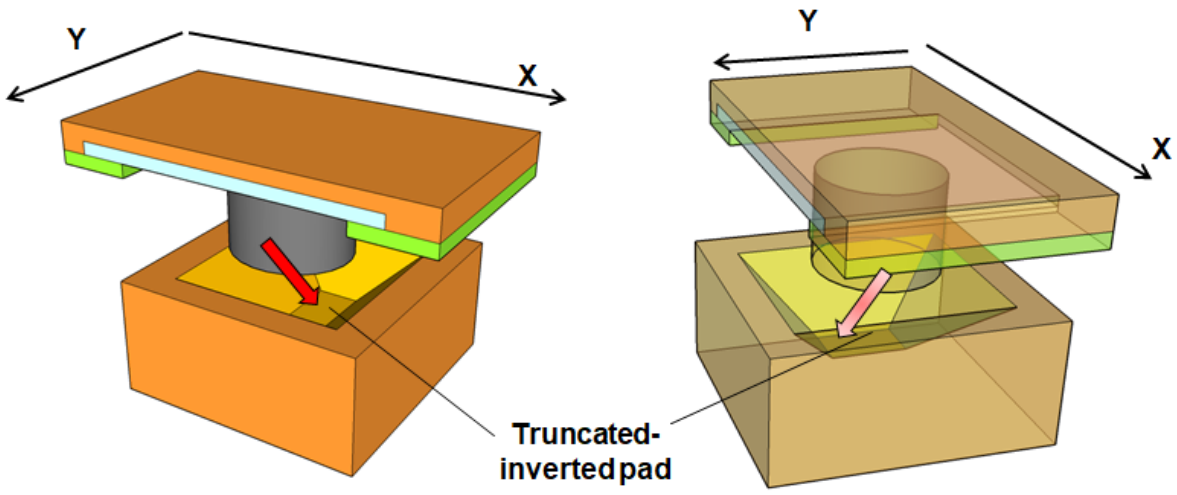


Figure 6.6: 3D schematic of self-aligned interconnection elements showing the process of self-aligning due to the mechanical force introduced by a concave-convex pair.

interconnection elements (SIEs). Under the coarse alignment condition together with the applied bonding force, the bumps tend to slide into the convex shape of the pads fabricated at the substrate due to sheer mechanical force. As shown in Fig. 6.6, the initial position of chip and substrate are offset from the optimized structure. With the force introduced, the chip will slide into the ideal position, which is confined by truncated inverted pads. The red arrow in Fig. 6.6 shows the movement of the chip to achieve self-alignment. Any misalignment that may have occured during the alignment process, is thus self-corrected.

6.3 Self-aligned Flip-chip Assembly with Solder Reflow Process

Solder reflow is the most commonly used method for low-cost assembly. With the development of flip-chip bonding technology, the application of the solder is extended to various optoelectronic packages. The solder reflow process demonstrates superior

electrical performance, high reliability, reduced footprint, high I/O density, low cost, efficient heat conduction and batch assembly. Self-aligned flip-chip assembly with solder process was proposed in [132]. The reflowed solder generates a lateral force in order to drag the chip to the optimal position. Figure 6.7 describes the self-alignment mechanism by solder reflow. The solder is heated above the melting point during the reflow process and becomes liquid. The liquid solder wets the metal pads surface and the chips will follow the surface tension force to minimize the surface area. To control the lateral and vertical offset, a hard stop during the surface tension movement is used. The idea is to lock the chip at the optimal position [147]. Chips move under the in-plane force and land at the lateral stops. In the perpendicular direction, the pressing movement is stopped vertically until chips butt against vertical stops. The vertical stops are pre-fabricated on the substrate with high position accuracy.

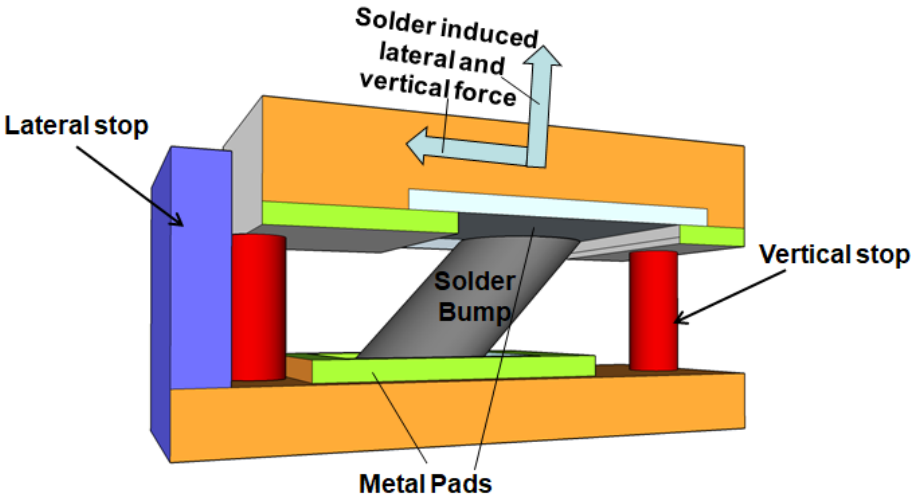


Figure 6.7: 3D schematic iof self-alignment process using solder reflow.

6.4 CMOS Compatible Contact for Indium Phosphide Device

Ohmic contacts for InP PICs are usually made with gold. However, the use of gold is forbidden in a CMOS process because it forms a deep level trap in silicon [148]. Gold-free low-resistance contact metal for InP devices has been studied. By simply replacing gold with aluminum, as reported in [149], gold-comparable pad resistivity was achieved. A metallurgy that includes a ratio of germanium and palladium was reported for making low contact resistance to both n-type InP material [150]. This enables a contact stack that does not include gold and is compatible with CMOS processes. The ratio of germanium and palladium can be achieved by stacking layers of the materials and annealing the stack, or simultaneously depositing the germanium and palladium on the material where the contact is to be manufactured. The contact metal on InP is based on the Pd/Ge/Ti/Al. As for flip-chip bonding, a solder reflow process is standard for most IC packaging facilities and relies on aluminum pads. Recently, thermocompression bonding based on aluminum-aluminum pairs are also reported. The InP metallization can therefore be configured to be gold-free for hybrid integration with CMOS devices.

Chapter 7

Device Characterization

In this chapter, the characterization of 3D hybrid integrated devices and InP devices are reported. In section 7.1, a novel tunable external cavity laser based on coupling a RSOA chip to a IMEC full platform SiPh chip is reported. The 3D hybrid integration approach provides a reliable laser source by leveraging the optical gain from an InP RSOA and the high precision process of SiPh. In section 7.2, an external cavity laser with supreme thermal performance is demonstrated by integrating an InP RSOA on a passive SiPh chip with a metal filled recess. In section 7.3, the characterization of standalone InP devices is reported including the dilute waveguide mode characterization, InP lidar transceiver measurement and a novel monolithically integrated narrow linewidth laser made with InP MPW process.

7.1 3D Silicon Photonic External Cavity Laser

7.1.1 Design Overview

Figure 7.1(a) shows the side view schematic of a 3D silicon photonic external cavity laser (SPECL), where the RSOA with a high reflectivity coated back mirror and a TIR

turning mirror was bonded to silicon. Light was coupled to the silicon waveguide through a vertical grating coupler. A perspective view of a tunable 3D SPECL is shown in Fig. 7.1(b). Cascaded tunable ring filters were used for wide wavelength tuning based on the Vernier effect. A tunable DBR mirror was also formed in on the silicon chip to provide filtered feedback and additional phase control. A separate silicon grating coupler was used to couple light generated from the SPECL to a vertically positioned single mode fiber probe for testing. The green ring shapes in Fig 7.1(b) represent doped silicon heaters for tunable devices.

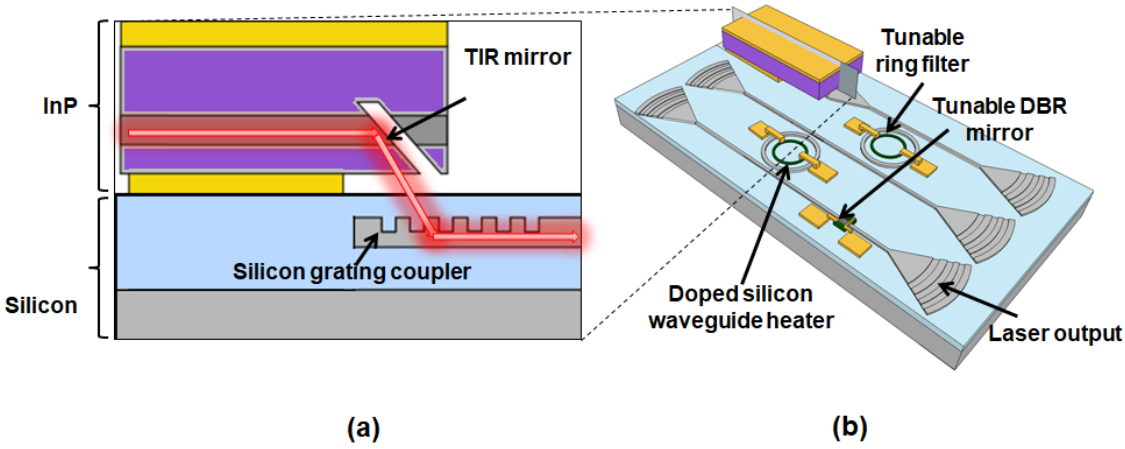


Figure 7.1: (a) Side view schematic of the 3D integration approach. (b) Perspective view of tunable 3D SPECL device.

A fabricated SPECL is shown in Fig. 7.2. This shows that an RSOA array with four RSOAs can be can be integrated on SiPh chip. The n-contact is the backside of the RSOA and the p-contact is on the silicon chip, which is intentionally extanded from under the RSOA chip. The SPECL is then mounted on carrier and wired bonded for electrical pumping. The output light was coupled into a single mode fiber for power and spectral analysis.

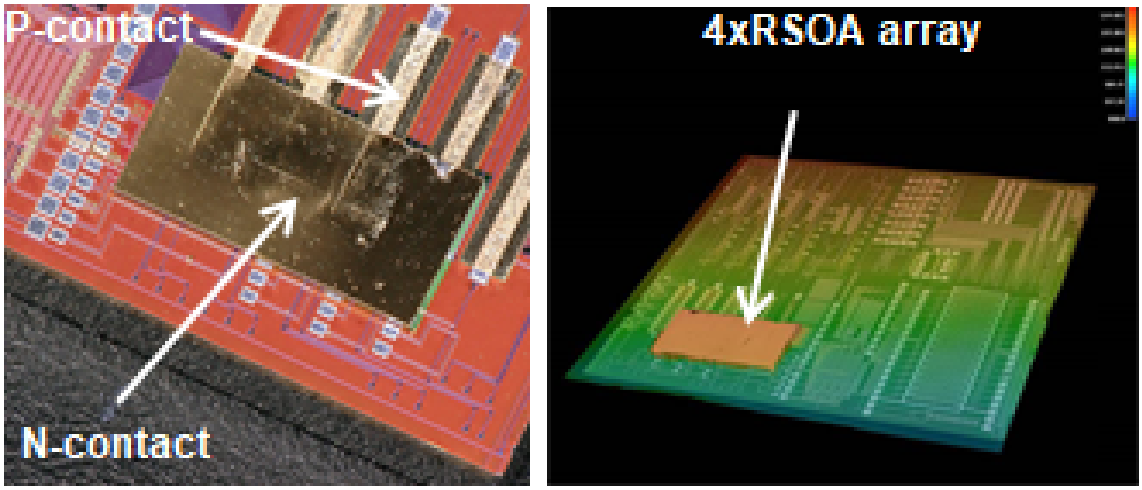


Figure 7.2: Microscope image of SPECL made with an RSOA array bonded on a SiPh chip

7.1.2 Lasing Characteristics

The SPECL was characterized with a temperature-controlled stage. The output power was collected by a cleaved single mode fiber (SMF-28 [151]) through an on-chip fiber grating coupler. The insertion loss from the grating coupler to the SMF-28 fiber was calibrated to be 6 dB. The power in the silicon waveguide accounts for the insertion loss of the coupler. Light-current-voltage (LIV) measurements were performed and the results are shown in Fig. 7.3. The threshold current at 15°C was 31 mA and up to 2 mW of power was coupled to the silicon waveguide.

7.1.3 Wavelength Tuning Performance

As shown in Fig.7.4(a), single-mode lasing was demonstrated over a range of 30 nm with side mode suppression ratio (SMSR) lager than 30 dB. Figure 7.4(b) and (c) show close up tuning characteristics where heaters the tunable rings were adjusted simultaneously. By tuning a single heater, a continuous tuning with a span of 0.5 nm was achieved. The contuious wavelength tuning results are shown in Fig. 7.4(d) as a contour map of

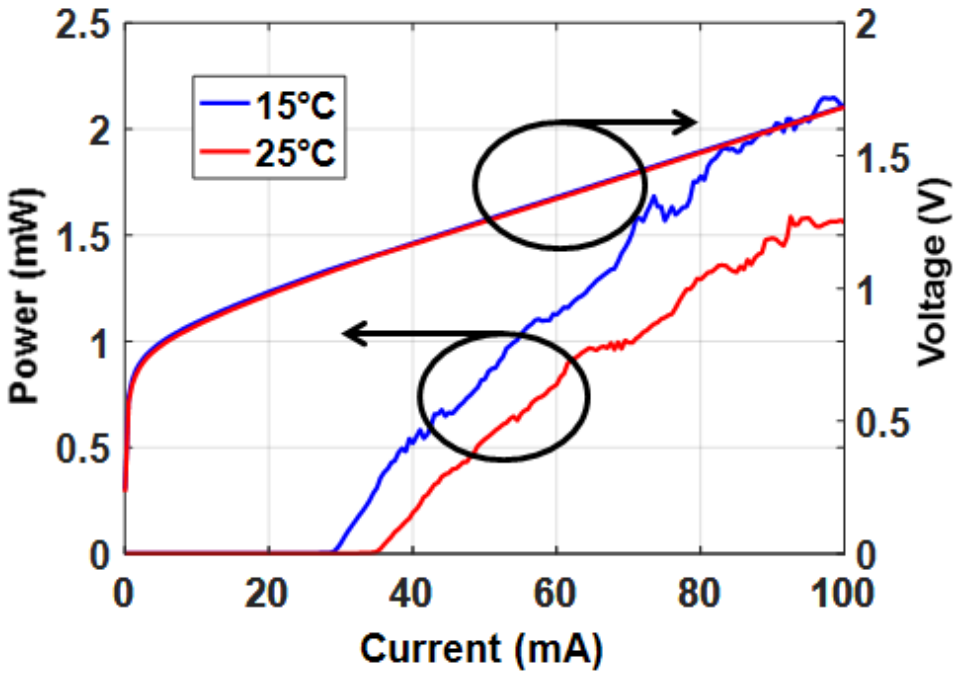


Figure 7.3: L-I-V characteristic of SPECL at 15°C and 25°C.

optical power as a function of the dissipated power in the heater and the wavelength.

7.1.4 Relative Intensity Noise Characteristics

The relative intensity noise (RIN) of SPECL was characterized at different pump currents and temperatures. The output of the SPECL was kept in the single mode state. The lowest peak RIN measured was -135 dB/Hz at a pump current of 60 mA with the RIN spectra shown in Fig. 7.5(a). The maximum RIN level shifts with increasing pump current to higher values in accordance with the theoretical relationship between relaxation resonance frequency and pump current, as shown in Fig. 7.5(b).

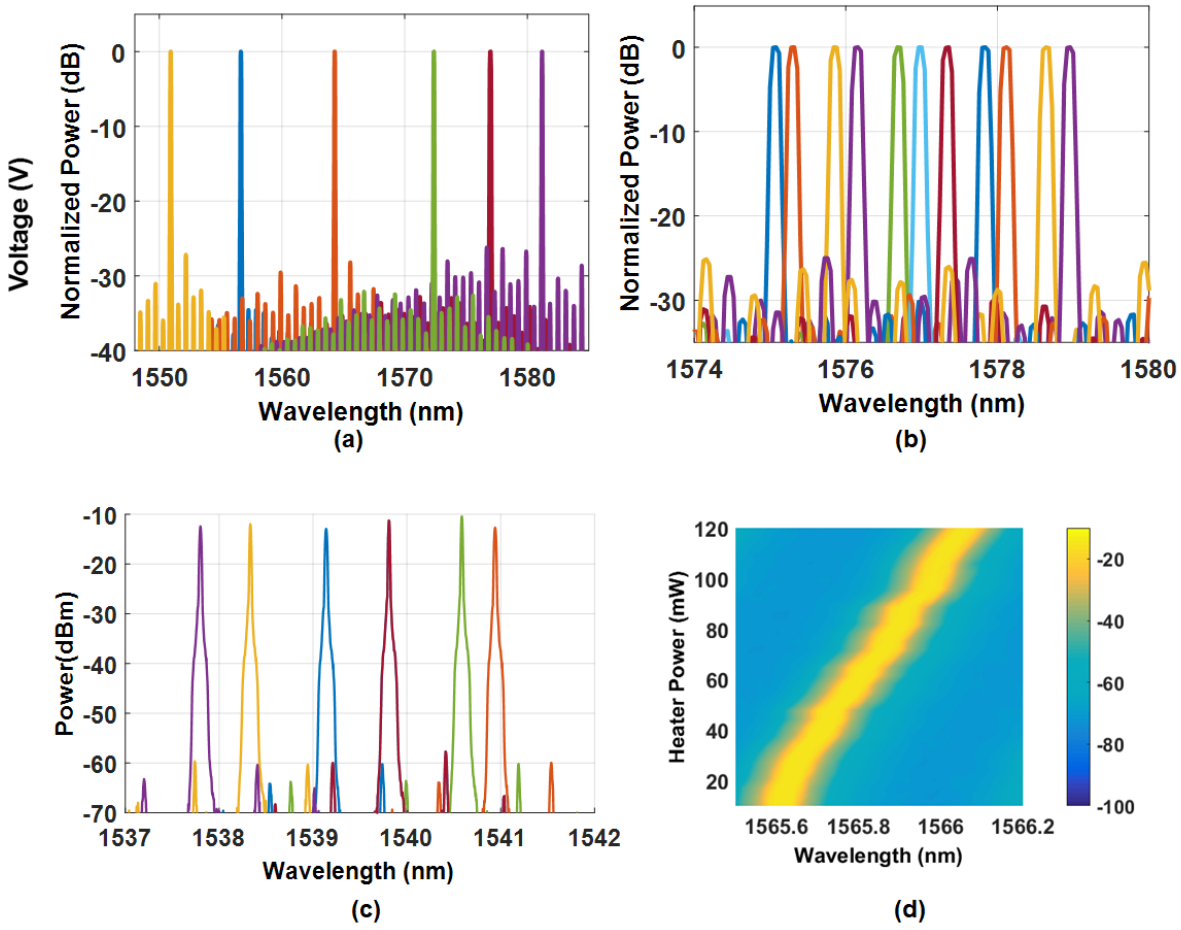


Figure 7.4: Superimposed spectra of the SPECL showing (a) a large step tuning over 30 nm and (b) a fine step tuning over 3 nm with a step of 0.3 nm.(c) One ring resonator showing tuning range of 5 nm. (d) Contour map of SPECL spectra.

7.1.5 Laser Linewidth

The self-heterodyne method [152] was used to extract the laser linewidth of the SPECL. The output optical power was amplified to 6 dBm with an erbium-doped fiber amplifier (EDFA) before being input to the heterodyne setup. The EDFA was set with a fixed pump current (60 mA) for all measurements. The acousto-optic modulator resonance frequency for the heterodyne measurements was 27 MHz. A 25 km single mode fiber delay was used, corresponding to a linewidth resolution of 12 kHz [153]. The beat

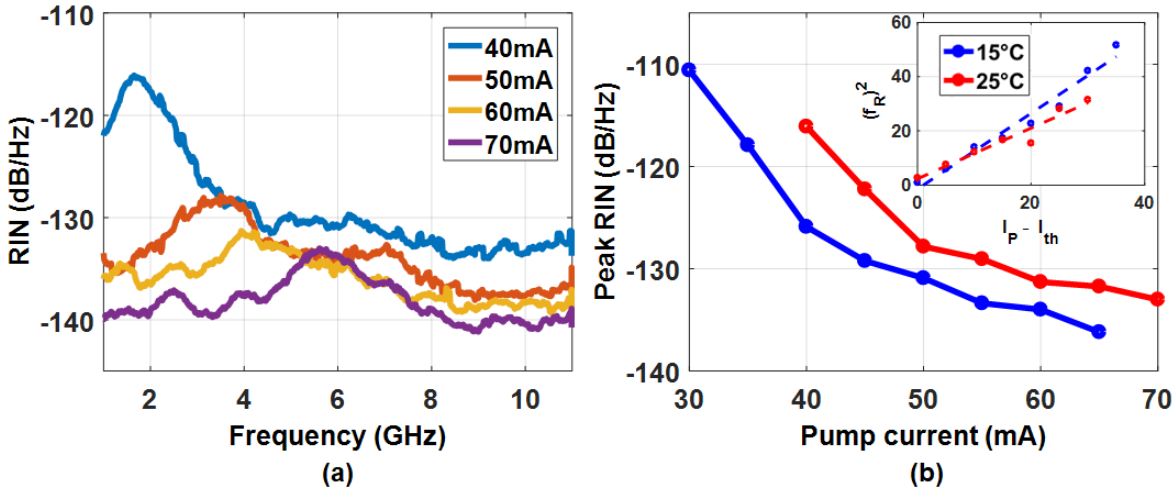


Figure 7.5: (a) RIN spectral of the SPECL at 25°C. (b) Peak RIN versus pump current minus threshold curent ($I_P - I_{th}$) and square relaxation resonance frequency ($f_R{}^2$) with respect to pump current minus threshold current (inset).

note was captured by a photodetector and the output signal was input to an electrical spectrum analyzer (ESA). The ESA output at various pump currents was measured while single-mode lasing was maintained. The linewidth results are shown in Fig. 7.6(a). A Lorentzian fit was applied to precisely evaluate the laser linewidth. A 3-dB beat frequency of 1.5 MHz was measured at a pump current of 104 mA as shown in Fig. 7.6(b). This is as good as or better than the linewidth performance of conventional DBR lasers.

7.2 High Thermal Performance Demonstration

To demonstrate the high thermal performance of the SPECL that is p-side down bonded to the silicon substrate, two SPECLs were fabricated in parallel with similar device structure with the only difference being the bonding metal placement.

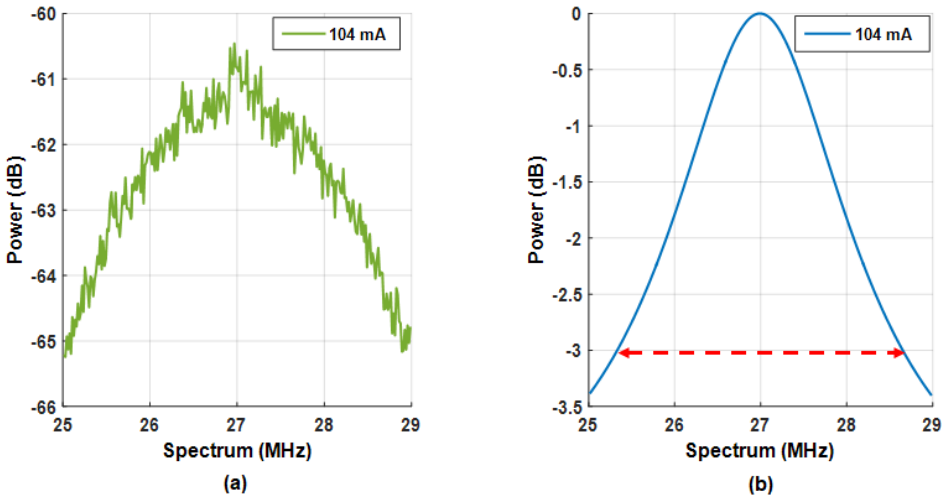


Figure 7.6: (a) Output spectra of the photodetector showing the beat note of the self-heterodyne measurements at 104 mA for SPECL with two ring resonators. (b) Lorentzian fits.

7.2.1 Design Overview

Two types of SPECLs devices were fabricated. For convention in this thesis, the two lasers are denoted as Laser A and Laser B. For Laser A, the RSOA was metal-bonded to the top oxide cladding. The RSOA for Laser B was bonded directly to the silicon substrate in a recess etched through the BOX layer. Both lasers demonstrated single-mode lasing as well as milliwatt (mW)-level optical power coupled to the silicon waveguide. The experimental results show that Laser B exhibits higher thermal performance. Figure 7.7 shows a general 3D schematic of the SPECL described in this section.

7.2.2 Buried Oxide Etching and Metallization

The SiPh chips were fabricated at IMEC using the passive SiPh process. SOI wafers with 220-nm-thick silicon were used. The DBR mirrors were realized with side-wall gratings. For Laser A, the metal bond pad was deposited directly on the top oxide cladding layer. The metal pad fabrication process for Laser B is reported in Fig. 7.8. A

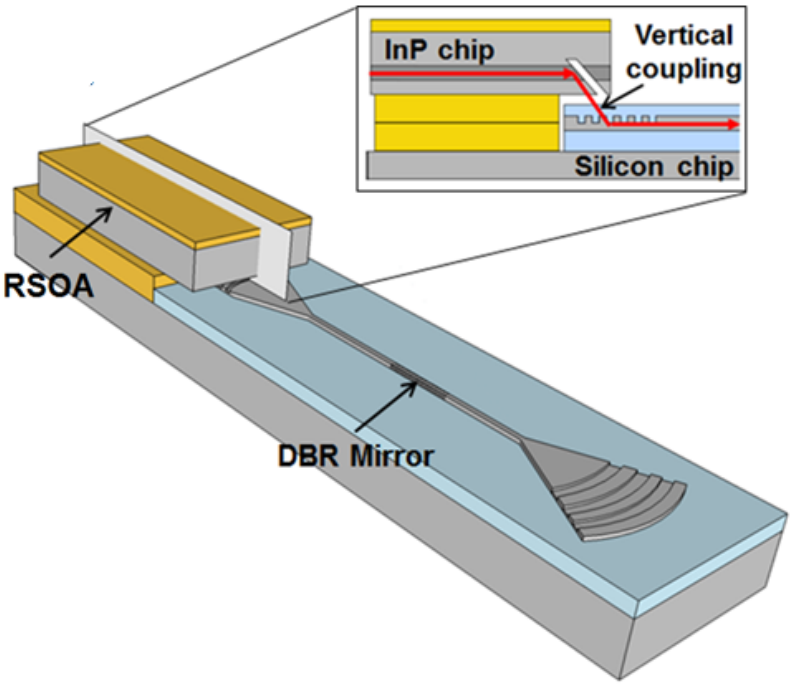


Figure 7.7: Plan-view schematic and side-view schematic (inset) of 3D integrated hybrid silicon laser (Laser B).IEEE©2016

recess is first formed in the silicon chip using ICP-RIE etching. A metal fill layer was then deposited inside the recesses on the silicon substrate, followed by the deposition of the metal bond pad.

Side-view schematics of Laser A and Laser B are shown in Fig. 7.9(a) and (b) and cross-section scanning electron microscopy (SEM) images of the bonded metal and bonded interfaces for Laser A and Laser B are shown in Fig.7.9(c) and (d) respectively. For Laser A, the active region of the laser is thermally isolated from the silicon substrate by the BOX layer. For Laser B, the BOX layer was replaced by the approximately 4-μm-thick metal fill. The gold-gold bonding interface is formed on top of the metal fill so that the heat generated in the InP active region can be dissipated effectively in the silicon substrate. The size of the InP RSOA array chip was typically 1.5 by 1.0 mm^2. The RSOA chips for Laser A and Laser B both have a gain section length of 1 mm.

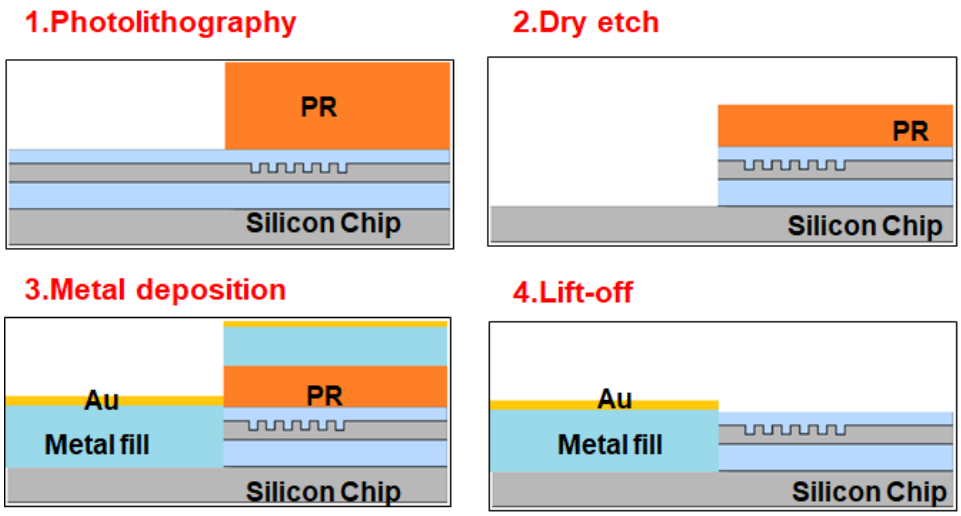


Figure 7.8: Post process of metal pad on silicon substrate.

The RSOA and silicon chips are attached together with thermocompression bonding. Both chips were cleaned with solvents prior to bonding. For both laser structures, the RSOA chips were bonded P-side down. The flip-chip bonding tool utilized in this work is capable of 1-μm alignment accuracy, however, with advanced implementations, such an alignment accuracy is not required for the 3D laser integration approach.

7.2.3 Lasing Characteristics

To characterize the fabricated SPECL chips, the bonded lasers were mounted on a temperature-controlled stage, which provides a temperature tuning from 20°C to 90°C. Pin probes were used to inject current into the RSOAs. A vertically oriented single-mode fiber probe was used to collect light from the output of the SPECL through a separate fiber grating coupler with an insertion loss of 6 dB. Figures 7.10(a) and (b) show the lasing spectra for Laser A at a bias current of 70 mA and for Laser B at a bias current of 60 mA, respectively. These measurements were performed at a stage temperature of 20°C. The SMSR was measured to be 30 dB or greater for both lasers.

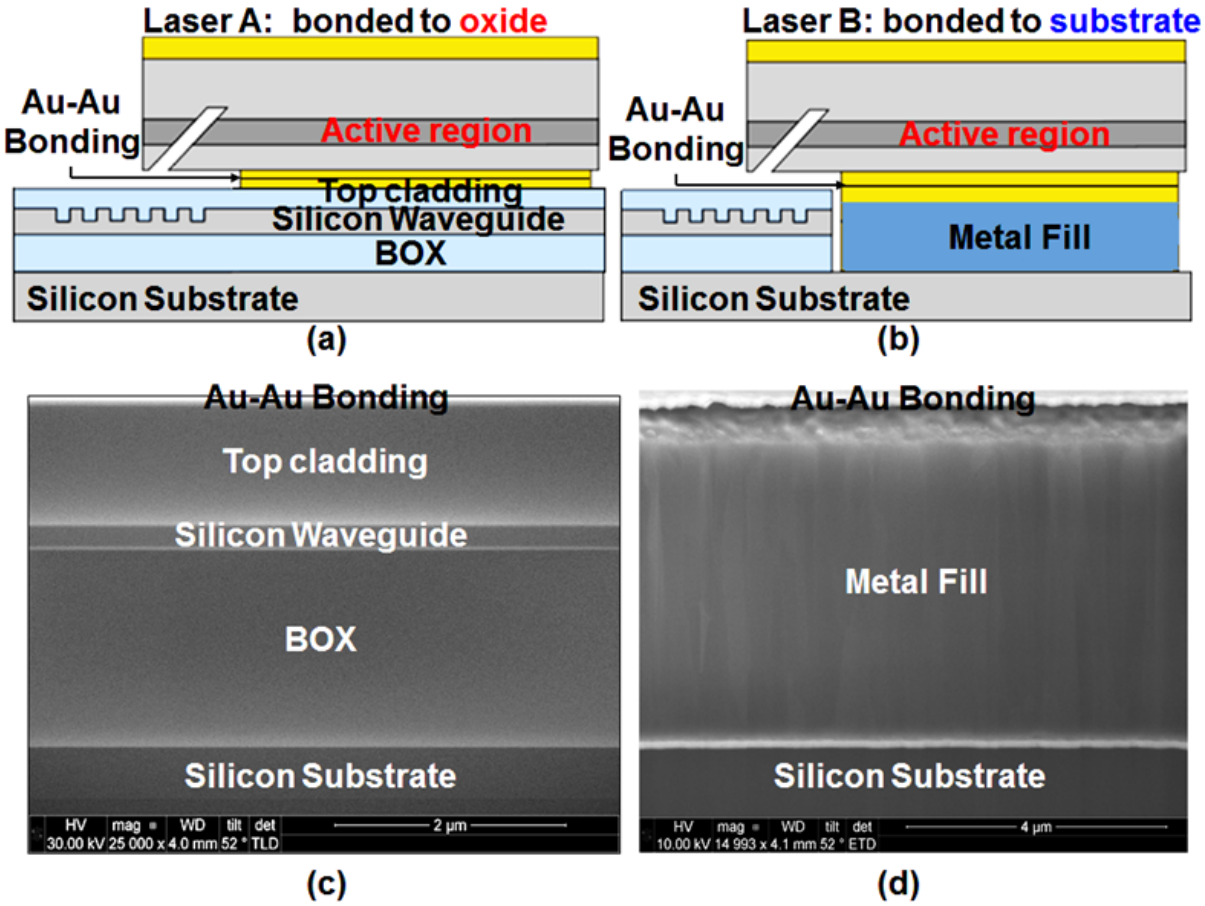


Figure 7.9: Side-view schematic of SPECL (a) Laser A and (b) Laser B. (b) Cross-section SEM pictures of the silicon chip in (c) Laser A and in (d) Laser B.IEEE©2016

Light-current characteristics were measured at different elevated temperatures with the results shown in Fig. 7.11(a) and (b). At lower temperatures, Laser A shows a higher wall plug efficiency (WPE) than Laser B. This is somewhat unexpected, but could be attributed in part to the higher series resistance measured for Laser B or the higher internal loss of the RSOA that is bonded to Laser B. The threshold current as well as WPE for both Laser A and Laser B were measured, with results shown in Fig 7.11(c). At 90°C, the WPE for Laser B was higher, due to the ability to dissipate heat more effectively. The thermal benefits were also quantified by extracting the thermal impedance of both lasers.

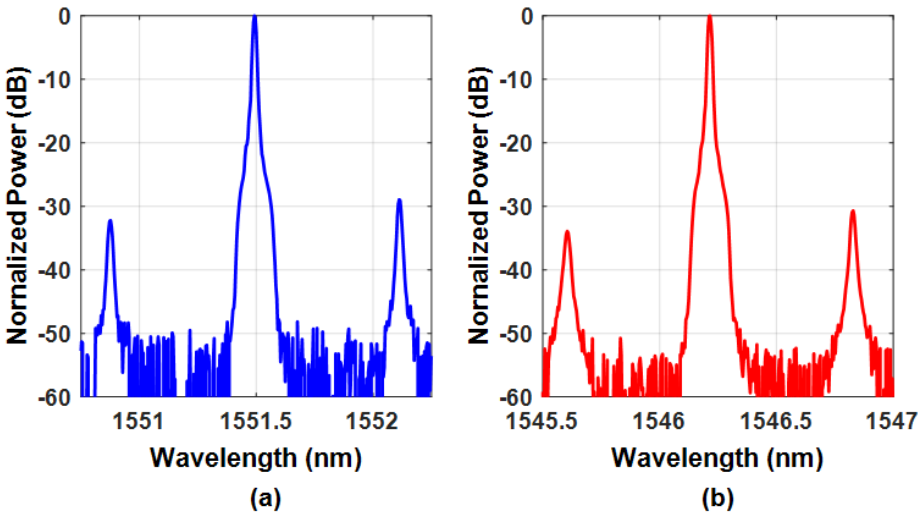


Figure 7.10: Lasing spectrum for (a) Laser A and for (b) Laser B. IEEE ©2016

7.2.4 Thermal Impedance Measurement

The extraction of the thermal impedance follows the methodology reported in [154]. As shown in Fig. 7.12(a) and (b), the lasing wavelength shift was first measured as a function of the stage temperature for both lasers. To ensure minimum device heating from parasitic resistance, the lasers were pumped with a pulsed current source (2.5 kHz repetition rate, 0.5% duty cycle). Next, the wavelength shift of the Fabry-Perot (FP) mode was measured under continuous-wave operation as a function of the applied electrical power. The results are shown in Fig. 7.12(c) and (d). The thermal impedance, Z_T, was calculated from the experimental results. The results show that Laser A demonstrates a thermal impedance of 18.3°C/W, whereas that for Laser B is 6.2°C/W. This factor of three improvement in thermal impedance is also in agreement with results obtained from finite-element method simulations. For Laser A, the simulated thermal impedance was 3.7°C/W and that for Laser B was 18°C/W.

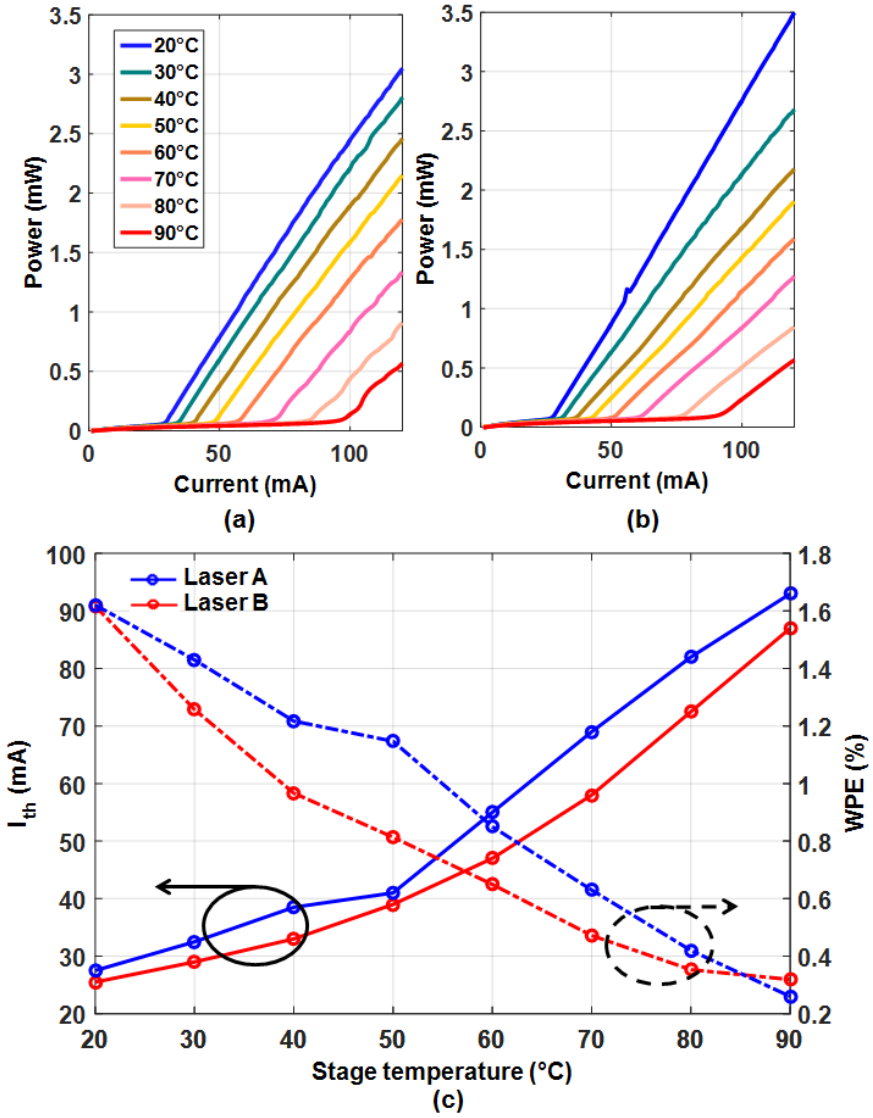


Figure 7.11: (a) Light-current characteristics for (a) Laser A and (b) Laser B. (c) Threshold current and maximum WPE as a function of stage temperature for both Laser A and Laser B. IEEE ©2016

7.2.5 Thermal Robustness Measurement

To characterize the thermal robustness of the 3D integration platform, a SPECL was subjected to a series of temperature cycles as illustrated in Fig. 7.13. An initial light-current (LI) measurement was performed at 20°C. Then the laser was ramped to an elevated temperature, held at that temperature while biased at 50 mA and then cooled

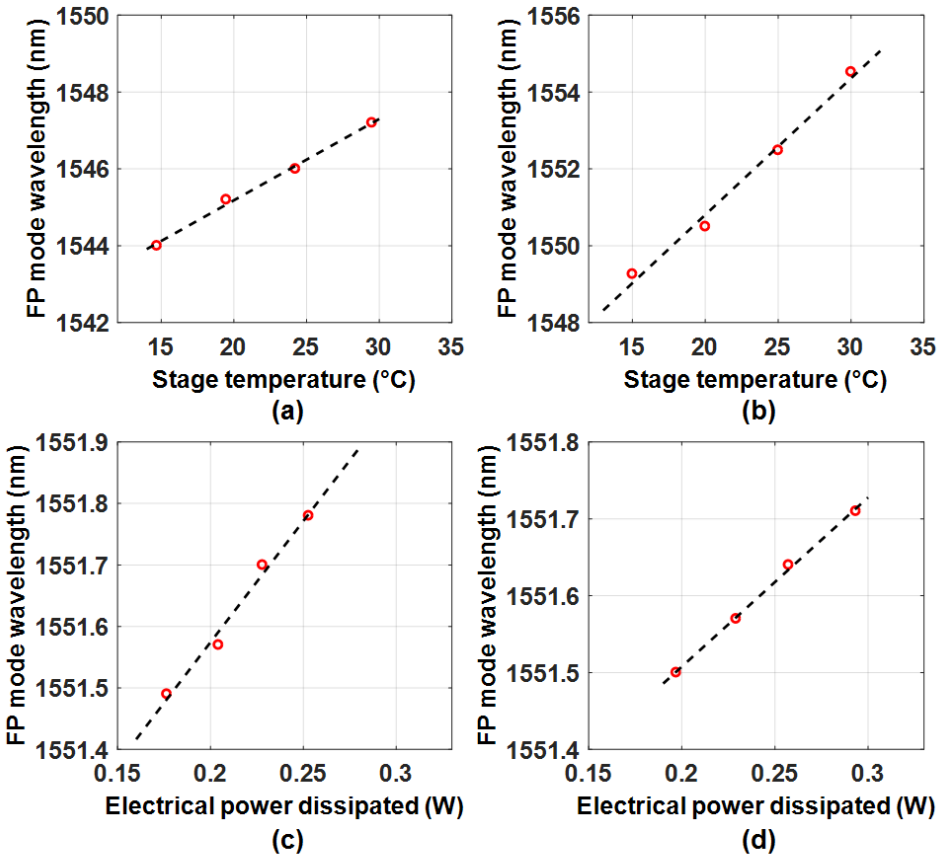


Figure 7.12: Thermal impedance measurement. Pulsed FP mode wavelength shift as a function of active region temperature for (a) Laser A and (b) Laser B. CW FP mode wavelength shift as a function of dissipated electrical power measured for (c) Laser A and (d) Laser B. IEEE ©2016

back to 20°C for subsequent LI characterization. As shown Fig.7.13, the LI characteristic was nearly identical after each cycle. Any variation in the results is attributed to measurement inaccuracy, perhaps induced by minor drift in the alignment of the output optical fiber collecting the light.

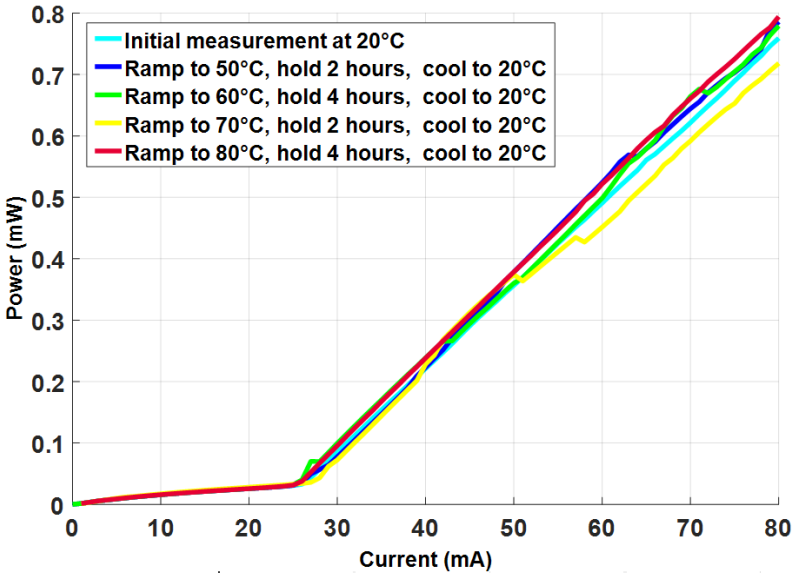


Figure 7.13: LI curves of the SPECL at an initial temperature and following temperature cycles. IEEE ©2016

7.3 Indium Phosphide Devices Calibration

7.3.1 Dilute Waveguide Mode Calibration

The dilute waveguide RSOA demonstrated continuous wave lasing at room temperature with a threshold current of 550 mA. The high threshold was partially due to uncoated facets. The LIV characteristic of a dilute waveguide RSOA is shown in Fig. 7.14.

The light was collected from a facet with an integrating sphere. The far field beams of the dilute and conventional RSOAs were characterized using an infrared camera. By moving the camera at a step of 20 μm, a series of beam profiles for the dilute and conventional waveguides were captured at around beam waist shown in Fig. 7.15(a) and (b), respectively. The divergence angle measured for the dilute waveguide is 11.8°, and that for the conventional waveguide was measured to be 28.2°.

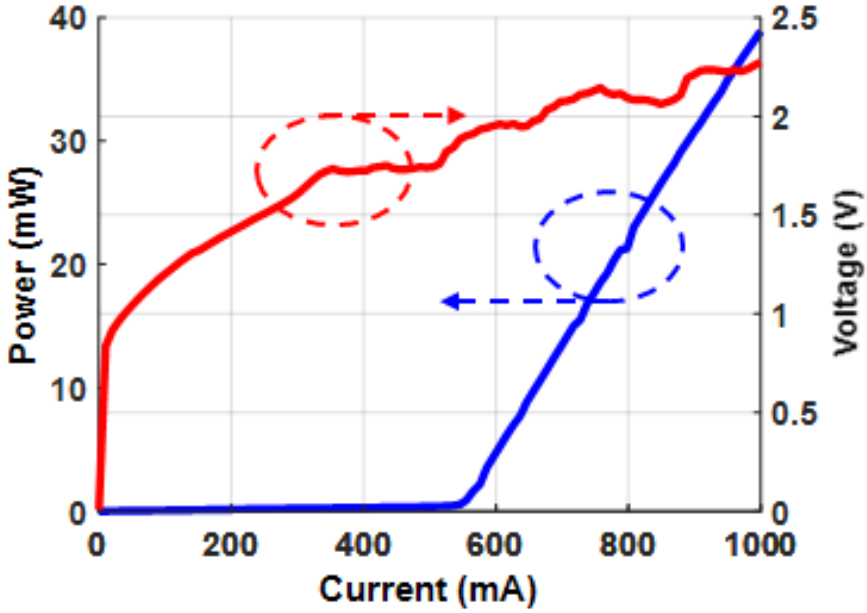


Figure 7.14: LIV characteristic of a dilute waveguide RSOA.

7.3.2 Noise Reduction of Integrated Laser Source with On-Chip Optical Feedback

Feedback techniques have been used to improve the quality of laser diodes by suppressing the phase noise as well as the amplitude noise. A laser diode with amplitude and phase noise reduction by feedback is reported in this section. The device is an InP based DBR laser that uses on-chip coherent optical feedback. Two type of laser (Type A and Type B) were designed and fabricated. The schematic diagram of Type A and Type B are shown in Fig. 7.16(a) and (b), respectively. Type A employs a straight DBR laser configuration. A high-reflectivity DBR and a 50/50 coupler designed as a broadband partially reflective/partially transmissive mirror terminate the gain region. To compare, the Type B laser contains a feedback loop whereby a portion of light from the 50:50 coupler is fed to the back of the DBR mirror and eventually returns to the gain

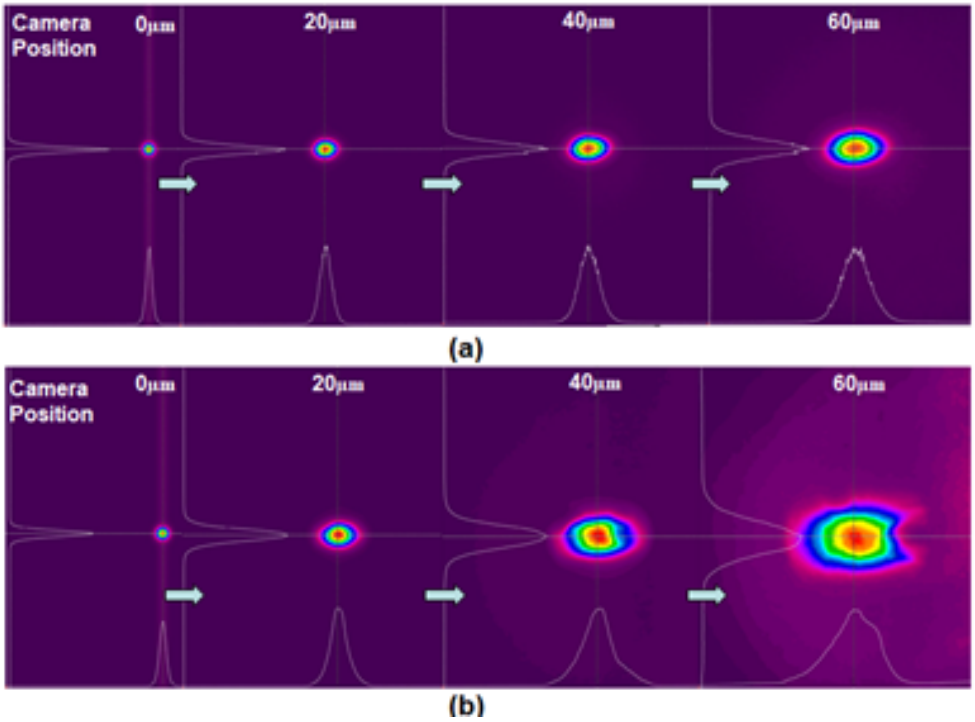


Figure 7.15: Beam profile evolution of (a) dilute waveguide and (b) conventional waveguide. IEEE ©2019

region. The lasers chip were fabricated with an InP MPW process offered by SMART Photonics. The gain region was an electrically pumped shallow-etched ridge SOA. The length of the SOA was 600 μm for both lasers. The on-chip 50/50 coupler was realized with a two-port MMI reflector (MIR) [155]. One port of the MIR was connected to the SOA to terminate the gain region while the other port was used to extract light from the cavity. The layouts and microscope pictures for both Type A and Type B lasers are shown in Fig. 7.17(a) and (b).

Both devices were wire-bonded to a custom printed circuit board (PCB) with heatsink capability. The PCB was mounted on a temperature-controlled stage. Light was coupled off-chip to a lensed fiber. A fiber isolator was used to reduce parasitic reflection. At 15°, LIV characteristics were measured and are shown in Fig. 7.18(a). The threshold currents for Type A and Type B lasers is 75 mA and 43 mA, respectively. The laser spectra are

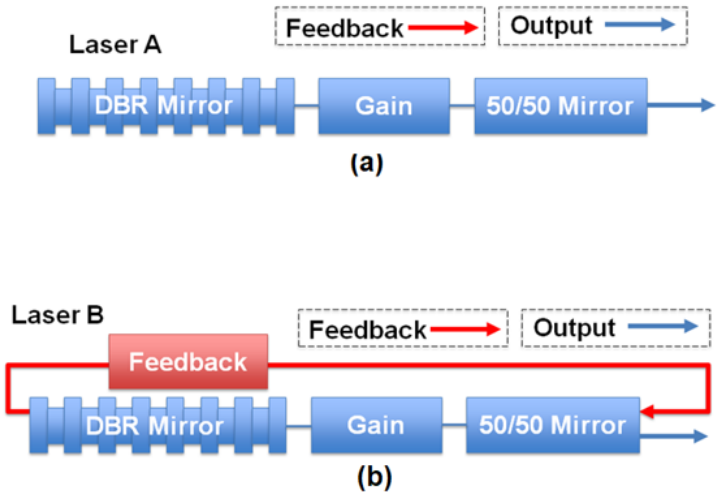


Figure 7.16: (a) Schematic of the laser cavity design (a) without (Type A) and (b) (Type B) with optical feedback.

shown in Fig. 7.18(b) for a pump current of 90 mA for both lasers. The SMSR for the Type A is 30 dB. For the Type B laser with the optical feedback, the SMSR is 47 dB.

The self-heterodyne method was used to extract the laser linewidth of for phase noise evaluation. The ESA spectrum for both devices were shown in Fig. 7.19(a) and (b) and the Lorentzian fit data were shown in Fig. 7.19(c). The linewidth for the Type A laser is 14 MHz, and for Type B it is 0.8 MHz, corresponding to an order of magnitude enhancement.

Figure 7.20 (a) shows the output RIN spectrum for the Type A laser at three pumping current with stage temperature of 15° C. Figure 7.20(b) shows the peak RIN value as a function of the pump current. The lowest peak RIN measured for Type A laser was -123 dB/Hz at a pump current of 95 mA. The maximum level shifts with increasing pump current to higher values in accordance with the theoretical relationship between relaxation resonance frequency (f_R) and pump current as shown in the inset figure. For the Type B laser, the RIN spectra are shown in Fig. 7.20(c). RIN spectra are extracted

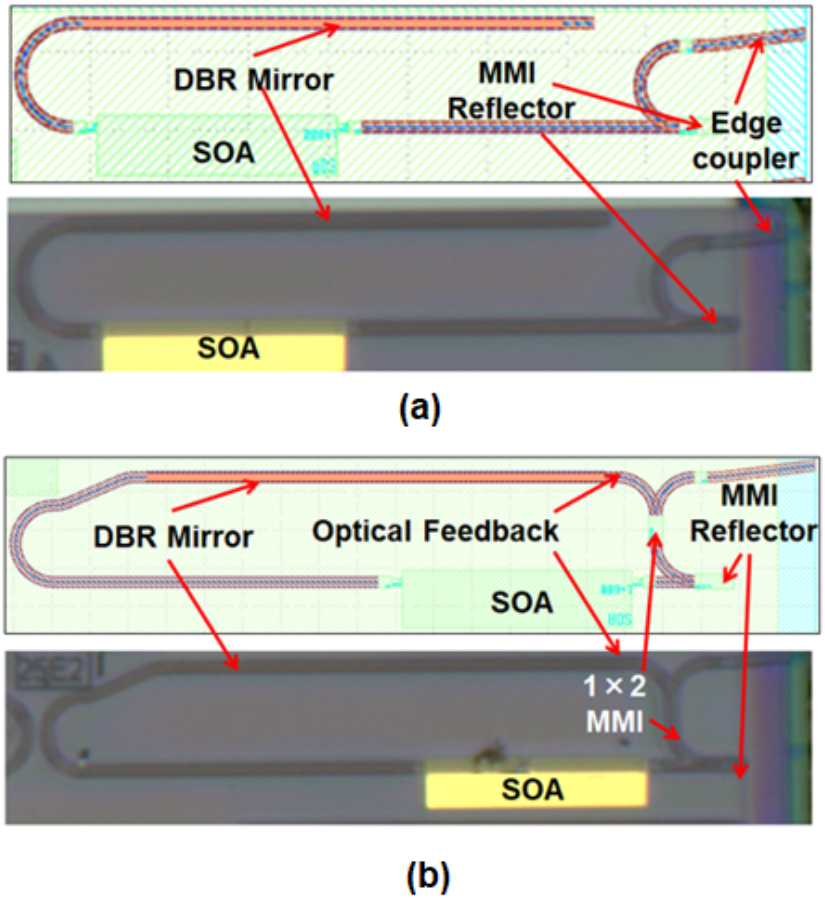


Figure 7.17: (a) Layout (top) and microscope image (bottom) of Type A laser. (b) Layout (top) and microscope image (bottom) of Type B laser.

at 20°C. As shown in Fig. 7.20(d), the lowest peak RIN measured for Type B at 20°C was -131 dB/Hz at only 80 mA. At this pump current, the peak RIN for the Type A laser was -117 dB/Hz.

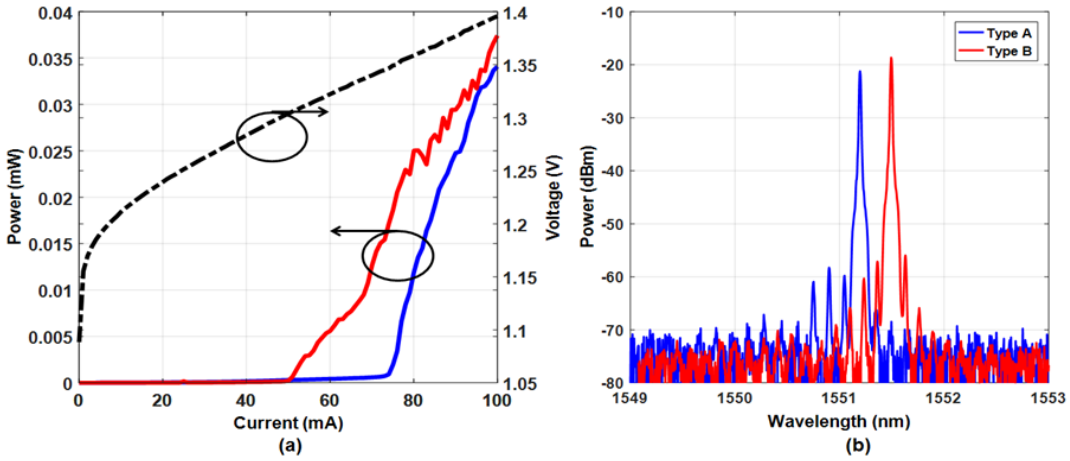


Figure 7.18: (a) LIV characteristics for type A and type B laser. (b) Lasing spectral of type A and type B laser.

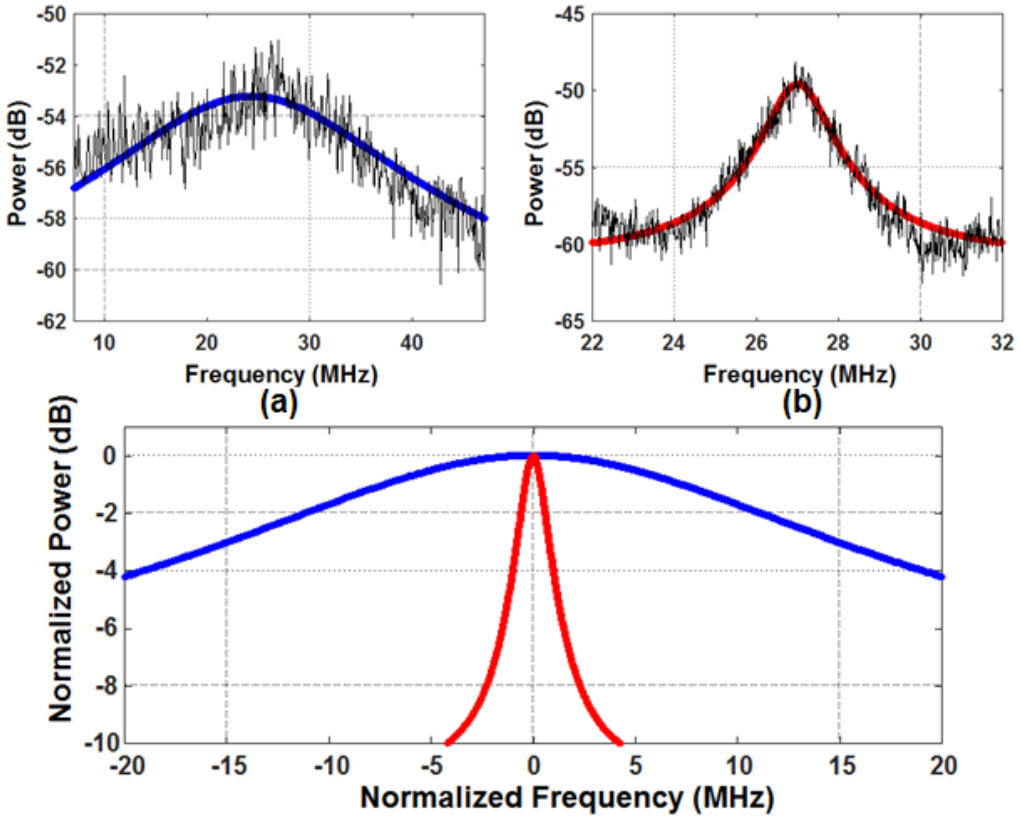


Figure 7.19: The output spectrum from the photodetector showing the beat note from the self-heterodyne measurement for (a) Type A and (b) Type B. (c) FWHM of the Lorentzian fit spectra for Type A and Type B lasers.

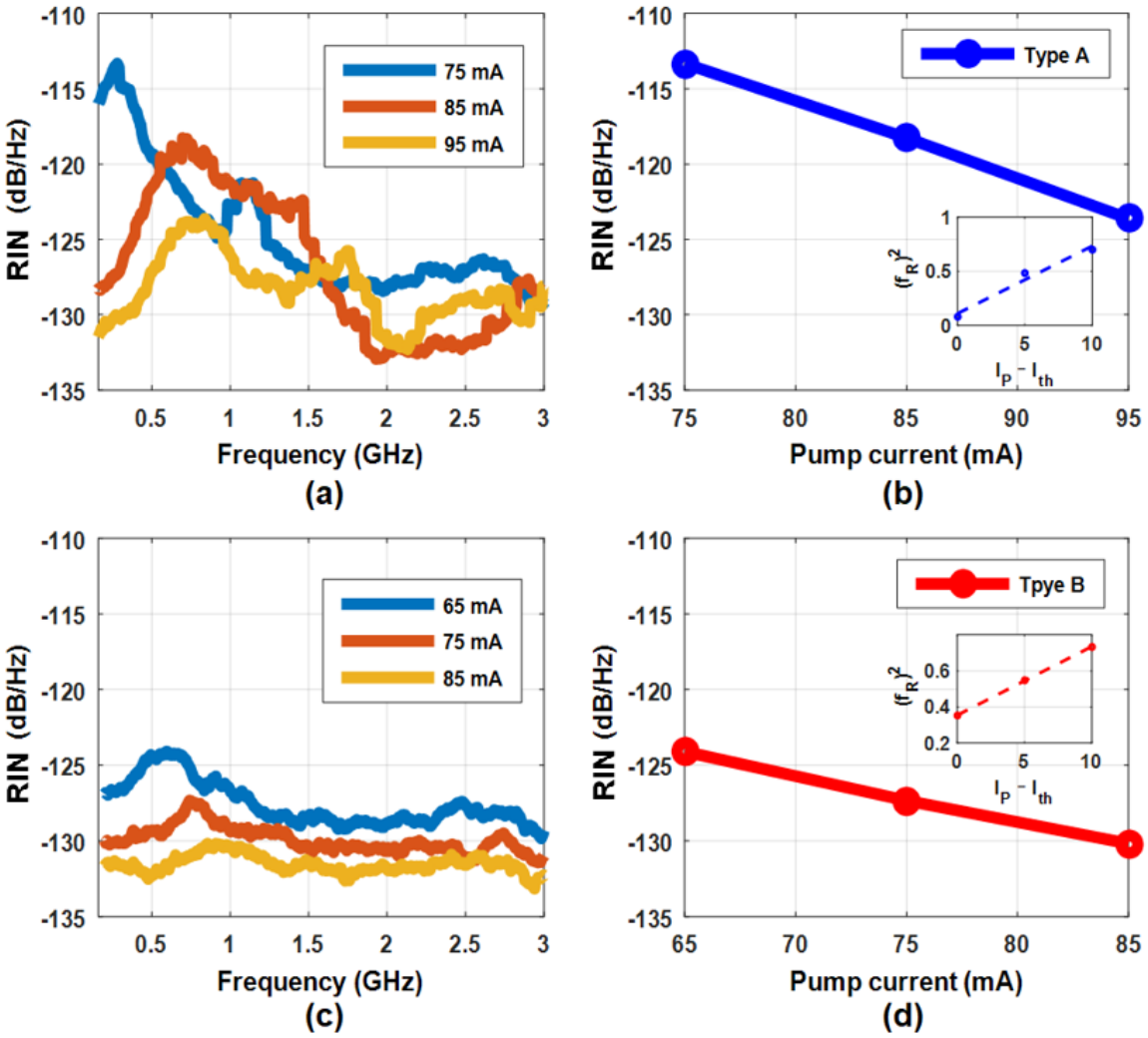


Figure 7.20: RIN spectrum at various currents for (a) Type A and (b) peak RIN versus pump current (IP) and relaxation resonance frequency squared (f_P^2) with respect to pump current minus the threshold current (inset). RIN spectrum for (c) Type B and (d) peak RIN versus pump current.

7.3.3 Integrated Lidar Transceiver Calibration

The fabricated lidar PIC characterization is reported in this section. The super carrier was mounted on a temperature-controlled stage for measurement. The test set-up is shown in Fig. 7.21(a). A vertical single mode fiber was used to couple light into the spectrum analyzer or optical power meter. The single mode fiber was mounted on a custom designed fiber holder. A 45°TIR mirror was fabricated by FIB, this is shown in Fig. 7.21(b). A probe card powered the part of the system for the laser frequency locker. To power the InP PIC, a hybrid probe card was used.

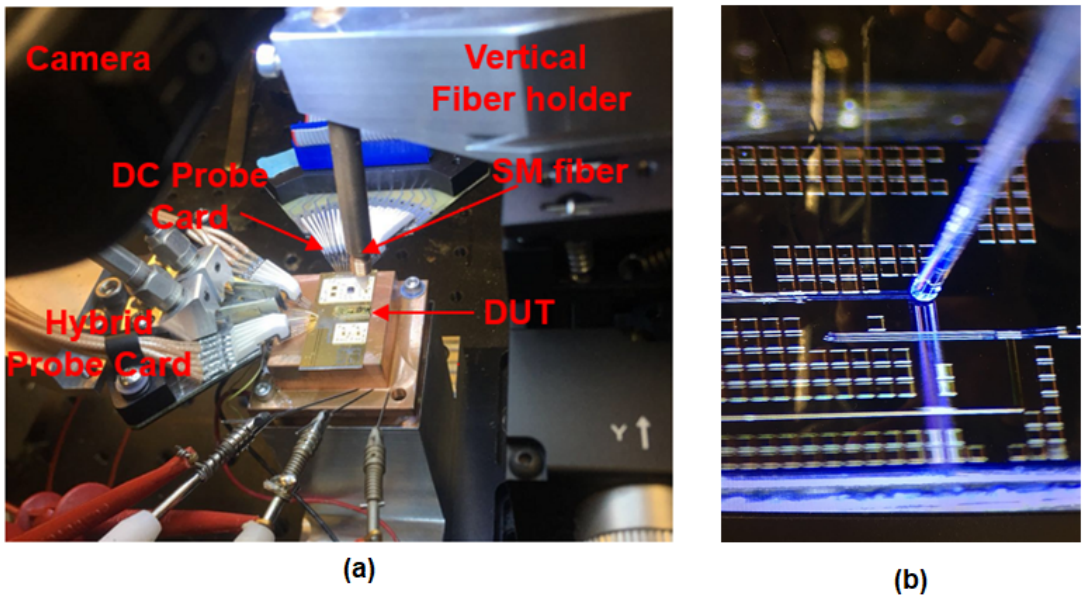


Figure 7.21: (a) Test setup for lidar transceiver. (b) The light is coupled vertically through a TIR mirror at the end of the InP waveguide.

The LIV characteristic of the sampled grating DBR (SGDBR) laser was measured. The SOA next to the SGDBR laser was reverse biased at -1 V to function as a photodiode. Then, the gain section of the laser was pumped from 0 to 100 mA. The measurement is shown in Fig. 7.22(a). The photocurrent measured with the SOA was converted to optical power in and is reported in Fig. 7.22(b).

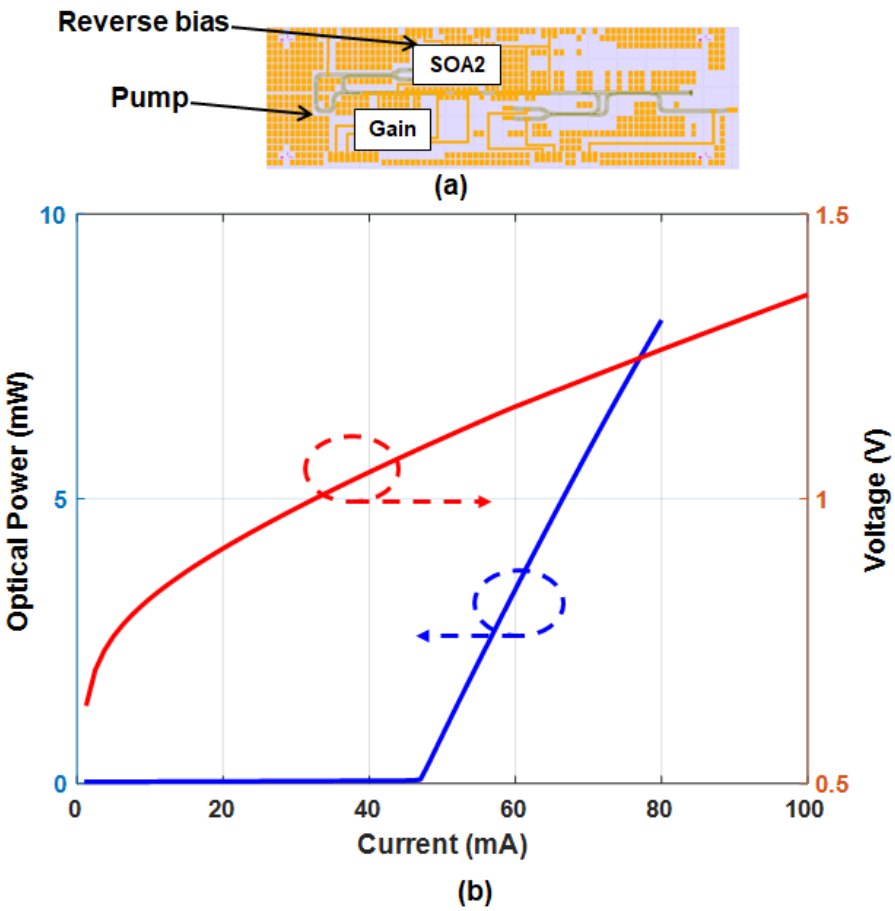


Figure 7.22: (a) LIV test setup for the SGDBR laser using on chip SOA as a photo detector. (b) LIV of a integrated SGDBR laser on lidar transceiver.

The SGDBR laser was then characterized for wavelength tuning. The two on-chip SOAs were pumped to boost the output power. The gain section current of the SGDBR laser was kept at 100 mA and the stage temperature was kept at 15°C. The light was coupled to the optical spectral analyzer through a single mode fiber. The maximum tuning range demonstrated is greater than 35 nm. The superimposed spectral of the tunable laser integrated on the lidar transceiver is shown in Fig. 7.23. The power isnormalized to the maximum power [156].

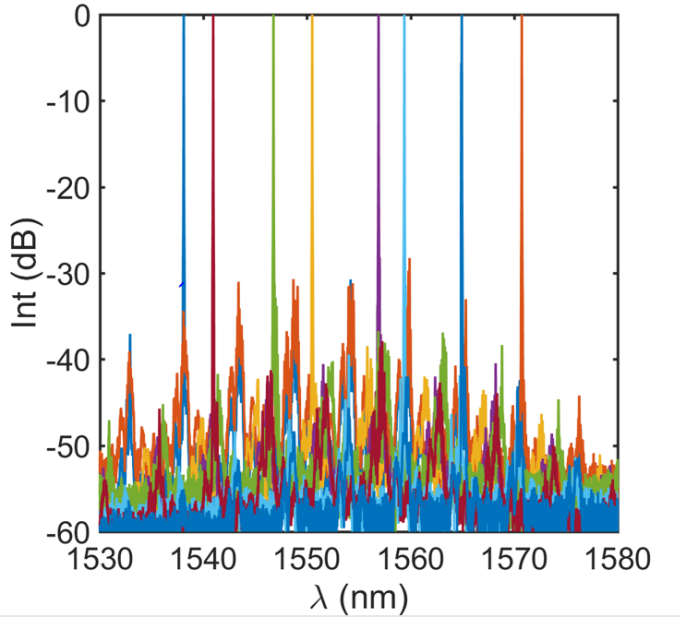


Figure 7.23: The superimposed spectra of the tunable SGDBR laser integrated in the lidar transceiver.

Chapter 8

Summary and Future Work

Integrated laser sources remain a challenge for SiPh. State-of-the-art SiPh foundries utilizing on CMOS process cannot provide integrated laser source with reliable performance at low cost. Direct heteroepitaxy of group III-V materials on silicon provides a promising long-term solution for large-scale PICs but is still maturing. Heterogeneous integration based on wafer bonding provides a sophisticated near-term solution. However, the need for co-fabrication of silicon with group III-V materials substantially increases cost. Lasers made with wafer bonding also suffer from limited thermal performance because the laser active region is thermally isolated from the silicon substrate by the BOX layer. CMOS processwa and hybrid integration techniques based on wafer bonding are being pursued in research and industry. Hybrid integration approaches, such as butt coupling of fabricated InP lasers to SOI waveguides, may address the thermal issue. However, the main limitation for butt coupling is the significant mode mismatch. In this chapter, a summary of this thesis is given section 8.1. Related future work is presented in section 8.2.

8.1 Summary of Accomplishments

In this work a novel 3D hybrid integration technique for SiPh was proposed and demonstrated. This addresses the aspects of thermal performance of lasers and increases alignment tolerance. This approach is based on the flip-chip integration of InP RSOAs containing TIR turning mirrors for surface emission. Surface grating couplers are used for light coupling into the SOI waveguides. The 3D integration approach provides increased alignment tolerance compared to butt coupling. Better than native InP laser thermal performance was achieved by flip-chip bonding the RSOA chip p-side down directly to the silicon substrate. The heat generated in the active region of the laser dissipates more efficiently into the silicon substrate. 3D hybrid integration is also suitable for high throughput manufacturing by carrying out the process at wafer level in a backend step. Lasers and fully fabricated PICs can be bonded on the silicon interposers for large-scale electronic-photonic integration.

A tunable laser was fabricated using 3D hybrid integration. An InP RSOA was integrated with an active SiPh chip with ring tunable rings and a tunable DBR mirror. Single mode lasing was demonstrated with SMSR up to 43 dB. Greater than 4 mW of optical power was coupled into SiPh waveguide. More than 30 nm wavelength tuning was achieved. Further laser characterizing demonstrated a linewidth of 1.5 MHz and RIN of -132 dB/Hz. Another external cavity laser was made by integrating a RSOA chip on a passive SiPh chip. A recess exposing the substrate was opened in the SiPh and metal was deposited in this recess. Gold was used for bonding and the RSOA was bonded P-side down. A low thermal impedance of 6.2°C/W was extracted experimentally from the 3D hybrid laser, demonstrating a factor of three improvement over a laser that was bonded above the SOI layer. To improve coupling efficiency, various advanced silicon surface grating couplers as well as a dilute waveguide RSOA was investigated.

The coupling efficiency enhancement was demonstrated by 2D FDTD simulations for an elevated grating coupler, dual-layer grating coupler, apodized grating coupler and grating coupler with lower metal reflector. By combining the use of a dilute waveguide RSOA, and elevated grating coupler with lower metal reflector, a coupling efficiency of 85% can be achieved along with high alignment tolerance. A novel RSOA and InP PIC was fabricated and calibrated. The alignment tolerance was increased by 45% for the fast divergence axis. The far field divergence angle of the dilute waveguide was 11.8°, approximately three times lower than that for a conventional design. Noise reduction for an integrated InP laser with on-chip optical feedback was also demonstrated. The introduction of on-chip optical feedback demonstrated a linewidth reduction to around 0.8 MHz and 10 dB improvement in RIN. A novel InP PIC for FMCW lidar was demonstrated. A widely tunable SGDBR laser was integrated monolithically with ab active frequency locker element and coherent receiver. The PIC was mounted on a super carrier with supporting IC. The PIC features surface emission that could be integrated to the SiPh chip to form a fully integrated lidar system. The initial characterization shows that the widely tunable laser demonstrates a 45 nm tuning range.

8.2 Future Work

Future works covers threes aspects of the 3D hybrid integration technology: the coupling efficiency enhancement, improved alignment tolerance and system demonstration using 3D hybrid laser to power the system on a SiPh chip.

8.2.1 Coupling Efficiency and Reflection Control

Coupling efficiency from the InP RSOA to the silicon waveguide could be as high as 85% according to the 2D FDTD simulations. Future work will focus on high coupling

efficiency experimental demonstration. The enhancement can be implemented from the SiPh side with the elevated grating coupler, the apozided grating and the bottom reflector. The elevated grating has been experimentally demonstrated in section 5.3.3. To achieve the best coupling efficiency, a bottom reflector needs to be incorporated into this design. The apodization of the grating pitch could be used together with metal reflector. From the InP side, the dilute waveguide RSOA could be used to improve the coupling efficiency. Another issue that needs to be addressed in the future is the parasitic reflection between the RSOA bottom facet and the grating coupler on the SiPh chip. The reflection at the interface of the grating coupler has been an issue for the fiber couplers. For the conventional edge coupler, parasitic reflection can be reduced by using a tilted waveguide orientation at the edge and an AR coating. Reflection control methods were proposed including a focused grating couplers with different waveguide angle [157], asymmetric grating trenches that change the angle of the reflected light [158] and subwavelength gratings with a fully etched silicon device layer [159]. These methods can be used in the grating coupler design for 3D hybrid integration.

8.2.2 Alignment Tolerance Improvement

The dilute waveguide design was demonstrated with increased alignment tolerance for the flip-chip bonding process. This feature is a key factor for cost saving for high throughput bonding processes. In addition to using a dilute waveguide RSOA, the alignment tolerance can be improved by adding advanced concepts to the bonding process. If passive bonding process used, alignment tolerance can be increased by using the V-shape notch on silicon and metal pillar on the InP RSOA for self-aligned thermocompression bonding. Solder reflow processes also provide self-alignment with the use of bonding stops.

8.2.3 Silicon Photonic Integrated Circuit by 3D Hybrid Integration

Monolithic SiPh PIC, have integrated light propagation and filtering, modulation and detection on a single chip. The functionalities of light generation and amplification, however, are not available for SiPh. The 3D hybrid integration technology proposed in this work directly address this issue, it allows InP gain and lasers chips to be integrated on fully fabricated SiPh chip at low cost. An InP RSOA, a laser and fully fabricated InP PIC can be bonded on the SiPh chip. Lasers and InP PIC can be bonded on SiPh for large-scale PICs. However, the yield of InP fabrication cannot compete with mature CMOS processes. The fabrication of the InP RSOA is a simple process compared to the fabrication of the InP lasers or PICs. The CMOS process for SiPh chip can leverage fabrication nodes of 65 nm, which is sufficient to fabricate first order DBR mirrors on silicon. By simply integrating the InP RSOA on a SiPh chip that has a grating coupler and DBR mirrors, low cost external cavity lasers can be realized. With high performance active components on silicon, transceivers and fully integrated solid-state-lidars can be fabricated with the 3D hybrid integration approach.

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