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Rutile films grown by molecular beam epitaxy on GaN and AlGaN/GaN

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Titanium dioxide (TiO$_2$, with the rutile structure) was grown on (0001) oriented GaN and (0001) Al$_{0.33}$Ga$_{0.67}$N/GaN heterostructure field effect transistor (HFET) structures by molecular beam epitaxy. X-ray diffraction showed $(100)_{TiO_2}\|(0001)_{GaN(AlGaN)}$ and $[001]_{TiO_2}\|\langle11\bar{2}0\rangle_{GaN(AlGaN)}$ with three rotational variants of the TiO$_2$. Transmission electron microscopy of 50 nm thick TiO$_2$ films on GaN and AlGaN/GaN showed sharp interfaces with no intermixing or reaction between the oxide and semiconductor. The TiO$_2$ exhibited a columnar film microstructure with a lateral domain size of a few nanometers parallel to $(101)_{TiO_2}$ and a few tens of nanometers parallel to $(10\bar{1})_{TiO_2}$. Metal–oxide HFETs with 50 nm thick TiO$_2$ dielectric layers under the gate were processed and compared to HFETs without the TiO$_2$ dielectric layer. The transconductance of the HFETs with TiO$_2$ was 140 mS/mm, approximately 20% less than HFETs with no dielecric, and the pinchoff voltages of the two stuctures were comparable. The dielectric constant of the TiO$_2$ was ~70. The gate leakage current of the HFETs with TiO$_2$, ~4×10^{-6} mA/mm at 50 V, was approximately 4 orders of magnitude lower than that of the HFETs with no dielectric. Band offset measurements were performed using x-ray photoelectron spectroscopy, and the valence band of the rutile TiO$_2$ and the GaN nearly line up. © *2005 American Vacuum Society.* [DOI: 10.1116/1.1868672]

I. INTRODUCTION

GaN-based transistors are promising for future generation microwave power electronics. Field effect transistors (FETs) will require low gate leakage both for low noise and reliability. Incorporation of an insulator into GaN-based transistors to make metal–oxide–semiconductor field-effect transistors (MOSFETs) or metal–insulator field-effect transistors (MISFETs) results in reduced gate leakage compared to metal–semiconductor field-effect transistors with a Schottky gate. To achieve such metal–insulator or metal–oxide–semiconductor structures, there have recently been studies of various insulators on GaN, including SiO$_2$,[1–8] Si$_3$N$_4$,[3,8,9] AlN,[9–12] Ga$_2$O$_3$(Gd$_2$O$_3$),[11,13–15] Ta$_2$O$_5$,[16] thermally grown Ga$_2$O$_3$,[17] SiO$_2$/Si$_3$N$_4$/SiO$_2$,[18] and Sc$_2$O$_3$.[15] These works have investigated the insulator/GaN interface through fabrication of MIS structures and have shown improved leakage characteristics by incorporating the insulators into MISFETs. An SiO$_2$ layer under the gate has been shown to reduce gate leakage current in AlGaN/GaN heterostructure field effect transistors (HFETs) by 6 orders of magnitude compared to that of a conventional HFET.[4,5]

Ideally the gate leakage current should be suppressed without affecting the transconductance g_m or pinchoff voltage V_p of the device. Adding an insulator under the gate adds a series capacitance to the device

$$\frac{1}{C_{gs}} = \frac{1}{C_{AlGaN}} + \frac{1}{C_{Insulator}}, \tag{1}$$

which in turn affects the transconductance of the device:

$$g_m = 2\pi C_{gs} f_t, \tag{2}$$

where C_{gs} is the gate-source capacitance, C_{AlGaN} is the AlGaN capacitance, $C_{Insulator}$ is the insulator capacitance, and f_t is the current gain cutoff frequency. High transconductance can therefore be achieved with a high gate capacitance, which can be realized by incorporating a high dielectric con-

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stant (high-k) dielectric as the gate insulator material or by decreasing the dielectric thickness. Conversely, using a low-k insulator results in a decreased transconductance and an increase in pinchoff voltage of the device. In the case of very thin dielectrics, tunneling may occur, resulting in increased leakage.

Titanium dioxide (TiO_2) has been investigated as a high-k gate insulator for Si-based devices[19,20] as well as for dynamic random access memory applications.[21,22] TiO_2 in the rutile phase (cassiterite structure, tetragonal $a=4.59$ Å, $c=2.96$ Å) has also been grown epitaxially on c-plane (0001) as well as a-plane (11$\bar{2}$0) and r-plane (01$\bar{1}$2) sapphire.[23,24] In addition to an amorphous phase grown at low temperature and rutile, TiO_2 has two other polymorphic forms: anatase and brookite. Brookite has a higher free energy, however, than rutile or anatase and has not been observed in thin films. A wide range of dielectric constants have been reported for TiO_2 films and the dielectric constant depends greatly on the phase of the films, with $k \sim 20$ for amorphous and anatase films to moderate values of ~ 50 for films with a mixture of anatase and rutile. The highest values of k, ~ 90, were for pure rutile phase films.[25–27] The rutile phase generally results from high temperature growth or annealing of an anatase film grown at lower temperature. In bulk form, the dielectric constant of rutile is 89 in the a direction and 173 in the c direction.[28] Thus, phase pure rutile films are desirable for high-k applications. In this article, we present an investigation of the structural characteristics of rutile films grown by molecular beam epitaxy (MBE) on GaN and AlGaN/GaN structures, the electrical characteristics of devices utilizing TiO_2 as a gate dielectric, and band offset measurements of TiO_2/GaN.

II. EXPERIMENTAL PROCEDURE

GaN and AlGaN/GaN HFET structures were prepared by metal organic chemical vapor deposition on c-plane sapphire substrates. The GaN samples used were standard 2 μm thick templates. AlGaN/GaN HFET structures consisted of a 2.6 μm thick semi-insulating GaN base layer, followed by a 0.5 nm thick AlN interfacial layer,[29] and a 30 nm thick $Al_{0.3}Ga_{0.7}N$ cap layer. The base layer was rendered semi-insulating by Fe doping during the first 0.6 μm of growth.[30] Titatium dioxide was grown on the samples using MBE. The samples used for structural characterization and growth optimization were cleaned using a standard degrease (acetone, isopropanol, de-ionized water) followed by an HCl dip. The samples were then mounted using silver paint. In the MBE chamber, the samples were heated to ~ 550 °C as measured by an optical pyrometer under vacuum to remove any remaining organic contaminants. Titanium metal was sublimated from a hollow Ti-Ball™ source (sublimation pump source), which was heated by radiation from a resistively heated filament inside the ball.[31] It is known from previous oxidation studies that titanium requires relatively high oxygen partial pressures to oxidize it completely.[32] Therefore we used an oxygen–ozone mixture ($\sim 10\%$ ozone) as the oxidant. Titanium was deposited in an oxygen–ozone back-

ground pressure of $(2-3) \times 10^{-6}$ Torr. The growth rate of TiO_2 was ~ 0.1 Å s^{-1}. Temperature was the main parameter varied during growth optimization studies. Reflection high energy electron diffraction (RHEED) was used to monitor changes in the surface structure during film growth. Following growth, the samples were cooled to 200 °C in the same oxygen/ozone pressure used for growth to minimize oxygen vacancies. X-ray diffraction (XRD) was performed using a Picker four-circle x-ray diffractometer using copper K_α radiation. Atomic force microscopy was performed using a Digital Instruments D3100, and cross-sectional and high-resolution transmission electron microscopy (TEM) were performed using a JEOL 2010.

The GaN and AlGaN/GaN samples used for electrical characterization were prepatterned prior to the deposition of the epitaxial TiO_2 gate dielectric. Ohmic contacts consisting of Ti/Al/Ni/Au (200/1500/300/500 Å) were first deposited and annealed in N_2 at 870 °C for 30 s. The devices were then defined and isolated using a Cl_2 reactive ion etch. On the AlGaN/GaN samples, gates (Pt/Au 1000/2000 Å) were deposited on some die for use as control standards allowing comparison between devices on the same sample with and without TiO_2 under the gate. These samples then underwent a 20 s oxygen plasma treatment to remove photoresist residue followed by the same cleaning procedure discussed above prior to oxide growth. Following oxide growth, gates (Pt/Au 1000/2000 Å) were deposited on the remaining die. Current–voltage ($I–V$) measurements were then performed using a curve tracer. Leakage current and transconductance measurements were performed using an HP 4145 semiconductor parameter analyzer. Capacitance–voltage ($C–V$) measurements were measured using a Keithley 590 $C–V$ meter and on-wafer Hall patterns allowed measurement of mobility and carrier concentration prior to and following oxide growth.

To investigate the band alignments between the oxide and semiconductor, x-ray photoelectron spectroscopy (XPS) was performed and the method of Kraut *et al.* was used to determine the valence band discontinuities.[33] Samples with 15, 30, and 50 Å TiO_2 on GaN as well as AlGaN were measured in addition to the bare semiconductor surface and a thicker TiO_2 layer (~ 400 Å on GaN) to use as a bulk TiO_2 reference. The analysis was performed using a Kratos Axis Ultra system using monochromatic Al K_α x rays. A two-point energy calibration was performed and the Au $4f_{7/2}$ peak and Ag $3d_{5/2}$ peak positions were determined to be 84.00 eV for a polycrystalline gold foil and 368.2 eV for silver paste, respectively. The difference between the commonly accepted value of 368.27 eV for the Ag $3d_{5/2}$ peak position and our measured value is 0.07 eV, giving us high confidence in the calibration scale given that there is almost a 300 eV separation between the two peaks. Additionally, the Axis Ultra system has a charge neutralization system that reduces charge buildup during the analysis of insulating materials that was utilized during the measurements.
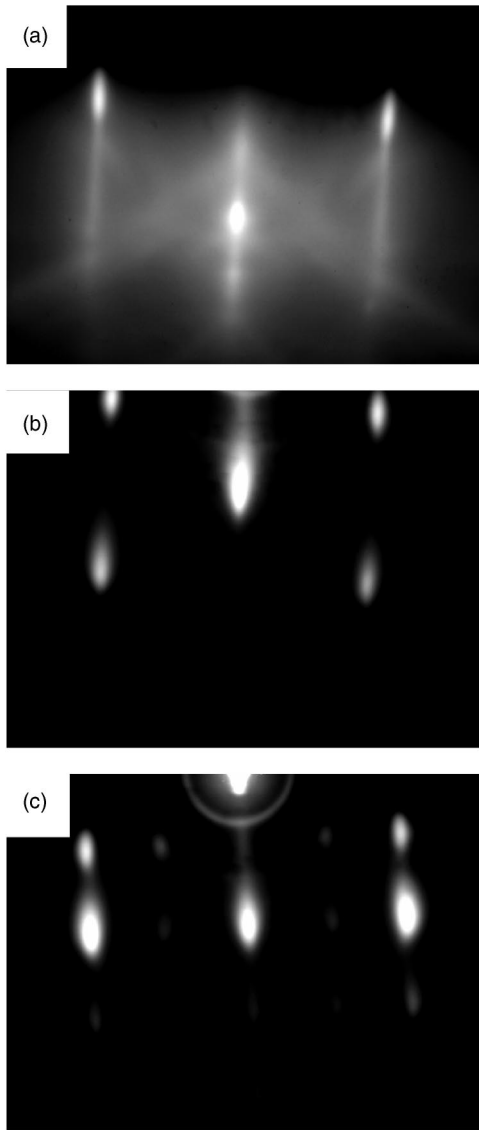
FIG. 1. RHEED patterns of (a) GaN along the $[11\bar{2}0]$ azimuth at T_{sub} =500 °C just prior to initiating oxide growth, (b) TiO_2 along its [001] azimuth (the $[11\bar{2}0]$ azimuth of the underlying GaN) after the growth of 500 Å of TiO_2 at T_{sub}=500 °C, (c) TiO_2 along its [010] azimuth (the $[1\bar{1}00]$ azimuth of the underlying GaN) after the growth of 500 Å of TiO_2 at T_{sub} =500 °C.

FIG. 2. θ–2θ scans of 500 Å thick TiO_2 films grown at T_{sub}=500 °C on (a) GaN and (b) AlGaN/GaN.

III. RESULTS AND DISCUSSION

A. Structural characteristics and epitaxy

Initial growths for structural characterization and growth temperature optimization were performed on GaN templates. It was found that phase-pure epitaxial rutile films were stable only in a small temperature window (~500–550 °C). Lower growth temperatures result in mixed-phase anatase and rutile films, as revealed by XRD. Figure 1(a) shows a RHEED pattern along the $[11\bar{2}0]$ direction of the GaN surface prior to growth. Figures 1(b) and 1(c) show the RHEED patterns along the [001] and [010] directions of the rutile film on GaN, respectively. The GaN surface was smooth, while the TiO_2 surface was slightly rough as indicated by the weak
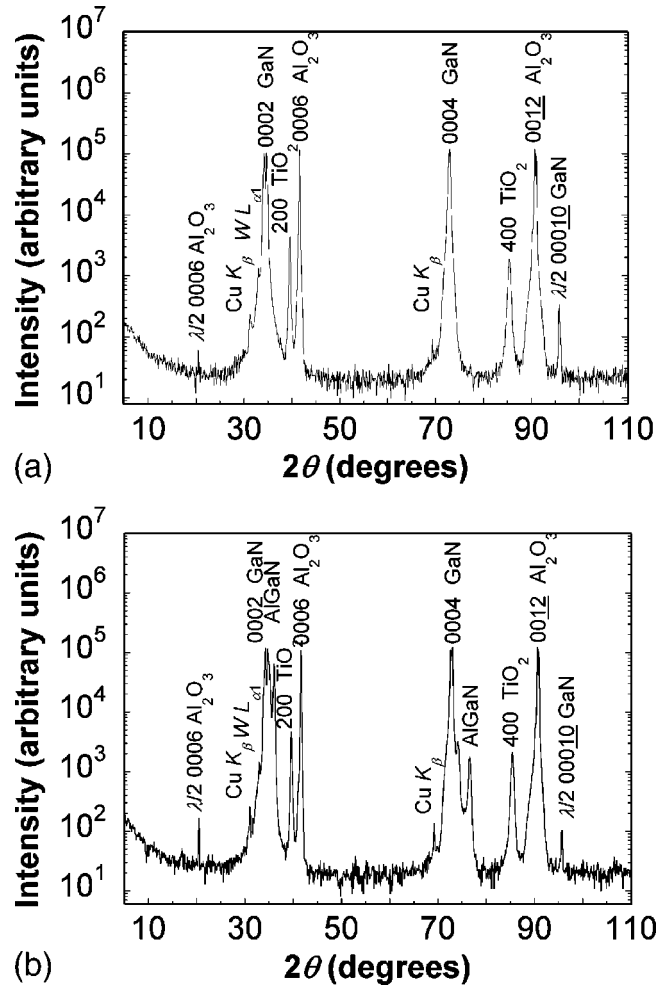
intensity modulation along the diffraction streaks, signifying a three-dimensional growth mode. The RHEED patterns showed $[001]_{TiO_2} \| \langle 11\bar{2}0 \rangle_{\text{GaN}}$ with three rotational variants as will be discussed below.

XRD was used to evaluate the phase purity of the films, determine the epitaxial orientation relationships, and assess their crystallographic perfection. Figure 2(a) shows a θ–2θ scan of a TiO_2/GaN sample. The presence of only diffraction peaks at 2θ=39.6° and 85.4°, corresponding to the rutile 200 and 400 reflections, respectively, in addition to the GaN and Al_2O_3 substrate peaks indicates that the oxide film was phase-pure rutile. The full width at half maximum (FWHM) of the 200 rutile peak was 0.31° in 2θ; the rocking curve FWHM was 0.78°. The out-of-plane lattice parameter (a) was determined to be a=4.55±0.01 Å. Comparison to the bulk value for rutile, a_{rutile}=4.59365 Å, indicates a very slight compression out-of-plane in the MBE-grown film. Figure 2(b) shows a θ–2θ scan of a TiO_2/AlGaN/GaN structure. Again, only peaks corresponding to rutile 200 (2θ =39.6°) and 400 (2θ=85.4°) were observed in addition to
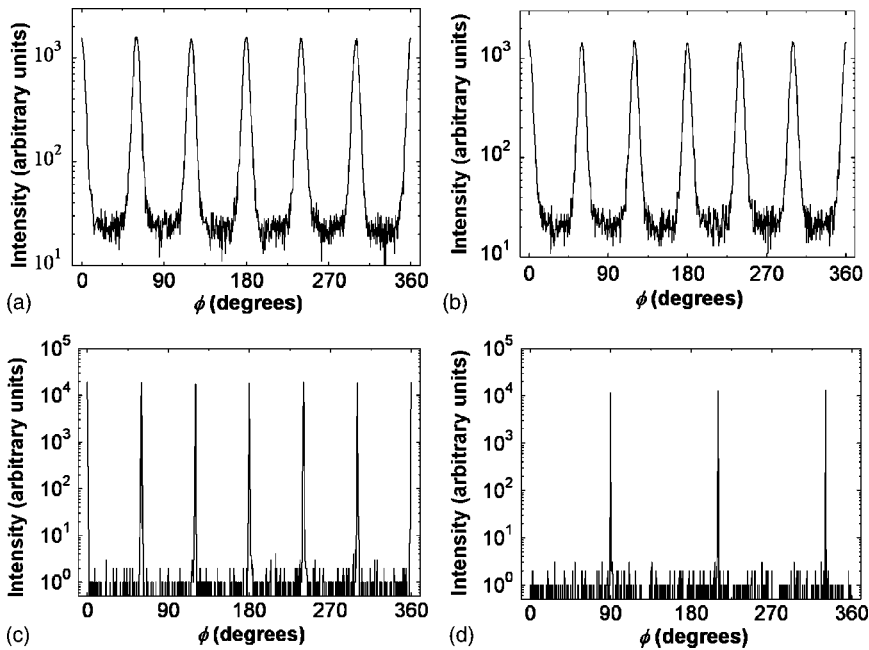
FIG. 3. ϕ scans of the 110 rutile reflection of films grown on (a) GaN and (b) AlGaN/GaN. (c) ϕ scan of the $10\bar{1}3$ GaN reflection and (d) ϕ scan of the $10\bar{1}4$ sapphire reflection. All scans are referenced with $\phi=0$ along GaN $[10\bar{1}0]$. The $\theta-2\theta$ scans of these same films are shown in Fig. 2.

the AlGaN/GaN peaks and Al$_2$O$_3$ substrate peaks. The FWHM of the 200 TiO$_2$ peak in 2θ peak was 0.29° and the rocking curve FWHM was 0.72°.

Figures 3(a) and 3(b) show ϕ scans of the off-axis 110 reflection of the (100) oriented TiO$_2$ film on (0001) GaN and (0001) AlGaN, respectively. The FWHM of the 110 rutile peak in ϕ was 6.5° for the film grown on (0001) GaN and 6.4° for the film grown on (0001) AlGaN. Figures 3(c) and 3(d) show ϕ scans of the GaN $10\bar{1}3$ peak and that of the $10\bar{1}4$ peak of the underlying sapphire substrate for this same sample. In all scans, $\phi=0$ was set along the GaN $[10\bar{1}0]$ in-plane direction. If the rutile films were single crystal films, two peaks separated by 180° would be present due to the twofold symmetry along the [100] axis of rutile. In contrast, six 110 peaks, separated by 60° were observed, indicating that the films had 120° in-plane rotation twins. Similar mosaic structures have been observed in epitaxial rutile films grown on *c*-plane sapphire, even though the sapphire surface has three-fold symmetry rather than sixfold as the GaN surface.[22,23] These ϕ scans indicate that the

epitaxial orientation between the film and substrate is $(100)[001]_{rutile} \| (0001)[11\bar{2}0]_{GaN}$ and $[010]_{rutile} \| [\bar{1}100]_{GaN}$.

The epitaxial orientation relationship between (100) oriented tetragonal TiO$_2$ and (0001) hexagonal GaN can be understood by considering the oxygen array of the film. The oxygen anions form an approximately close-packed structure with the cations in octahedral or distorted octahedral sites within the close-packed oxygen array. The close-packed oxygen network is similar to the hexagonal lattice of the GaN crystal, allowing heteroepitaxy of the TiO$_2$ films. There is approximately a -7.7% lattice mismatch between $[001]_{rutile}$ and $[11\bar{2}0]_{GaN}$ (with a 1:2 match) and approximately a -20.1% mismatch between $[010]_{rutile}$ and $[\bar{1}100]_{GaN}$ (with a 1:2 match). This poor match explains the relatively large in-plane FWHM in ϕ.

Figure 4(a) shows a plan-view TEM image and selected area diffraction pattern of a 50 nm thick TiO$_2$ film on GaN. Three variants are visible in the image, confirming the x-ray results. A schematic of the three rotational variants of TiO$_2$
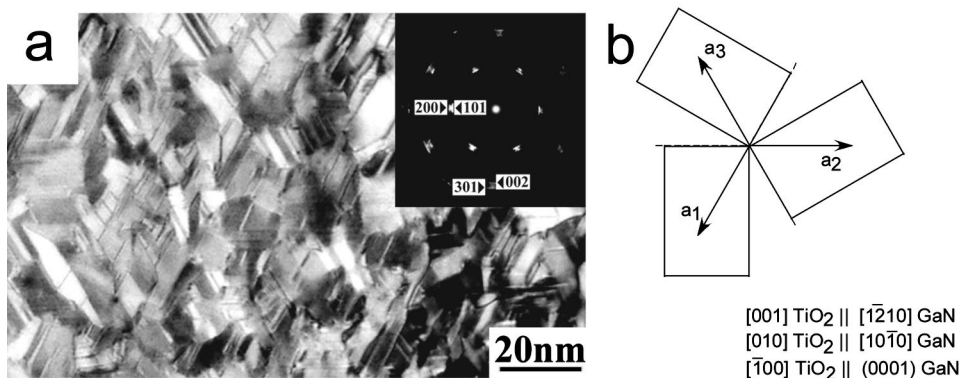

FIG. 4. (a) Plan-view TEM of a 500 Å thick TiO$_2$ film grown at $T_{sub} = 500$ °C on GaN and (b) schematic of the three rotational variants of (100) oriented TiO$_2$ on (0001) GaN. The orientation listed is for the lower left variant.
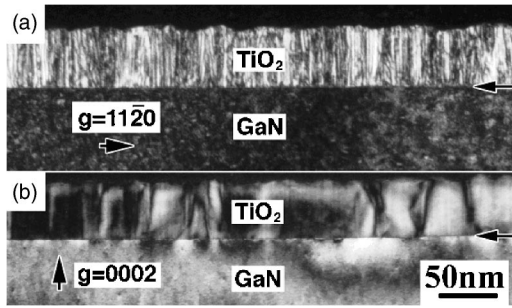
[001] TiO$_2$ ‖ [$\bar{1}2\bar{1}0$] GaN
[010] TiO$_2$ ‖ [$10\bar{1}0$] GaN
[$\bar{1}00$] TiO$_2$ ‖ (0001) GaN

FIG. 5. Dark-field cross-sectional TEM images of a 500 Å thick TiO$_2$ film grown at $T_{sub}=500$ °C on GaN with (a) $\mathbf{g}=0002$ GaN and (b) $\mathbf{g}=11\bar{2}0$ GaN.

FIG. 7. $C-V$ characteristics of capacitors on standard HFET structure and with a 500 Å thick TiO$_2$ film grown at $T_{sub}=500$ °C under the gate.

on the GaN surface is shown in Fig. 4(b). The grains are rectangular with widths of a few nanometers and lengths of a few tens of nanometers. Dark-field cross-sectional TEM images are shown in Fig. 5. A columnar grain structure is evident, indicating that the threefold mosaic structure was nucleated at the TiO$_2$/GaN interface and then propagated as the TiO$_2$ film grew.

High-resolution images corroborated the epitaxial relationship found in the x-ray scans. Figure 6(a) shows a high-resolution image of the TiO$_2$/GaN interface, and Fig. 6(b) shows a high-resolution image of the TiO$_2$/AlGaN interface. The in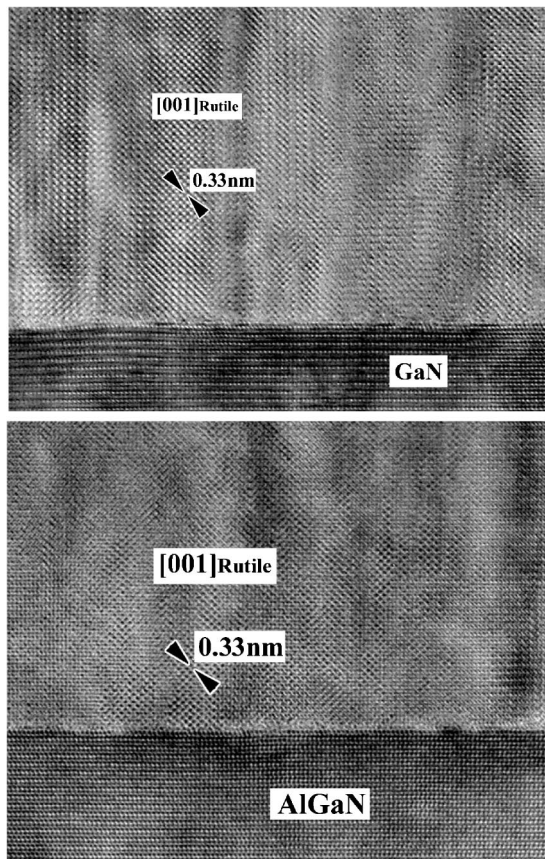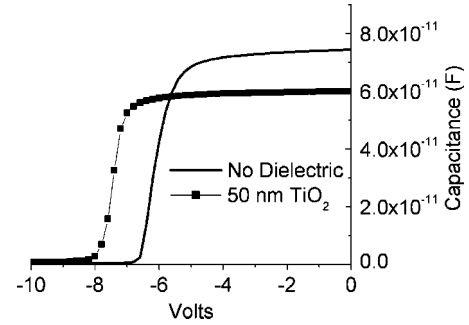terfaces appear smooth and the integrity of the semi-conductor surface appears to be preserved; no transition layer was evident. All of the cross-sectional and plan-view TEM results, including the electron diffraction patterns, show that there are a high density of twin lamellae in the film. Details of the microstructure of the TiO$_2$ films will be described in a forthcoming publication.

B. Electrical characteristics

$C-V$ curves (Fig. 7) were measured on devices with and without a TiO$_2$ gate dielectric layer. This sample was grown at the same time as that in Fig. 5, and the oxide thickness for this sample was 50 nm as measured by TEM, which was in good agreement with the calibrated growth rate (calibrated using a quartz crystal microbalance). The dielectric constant of the rutile film can be extracted by rearranging Eq. (1) to

FIG. 6. High-resolution TEM image of 500 Å thick TiO$_2$ films grown at $T_{sub}=500$ °C on GaN and AlGaN.

$$C_{oxide} = \left(\frac{1}{C_{MOS}} - \frac{1}{C_{MS}} \right)^{-1} \quad (3)$$

or

$$k_{oxide} = \frac{C_{MS} \cdot t_{oxide}}{\left(\dfrac{C_{MS}}{C_{MOS}} - 1 \right) \cdot \varepsilon_0 \cdot A}. \quad (4)$$

Here, C_{MOS} and C_{MS} are the measured zero-bias capacitance values (C_{gs} and C_{AlGaN} from Eq. (1), measured with and without TiO$_2$ under the gate, respectively), t_{oxide} and k_{oxide} are the TiO$_2$ thickness and dielectric constant of TiO$_2$, respectively, ε_0 is the permittivity of free space, and A is the capacitor area. The dielectric constant extracted for the rutile film from the data in Fig. 7 was $k \sim 70$, which is slightly lower than that of bulk rutile films in the a direction, but is in good agreement with reported values for rutile thin films.[24–26] As can be seen in the Fig. 7, even though the gate–channel separation increased by 50 nm, the threshold voltage of the metal-oxide-semiconductor heterostructure field effect transistor (MOSHFET) was only −1 V larger than that of the HFET (−7 V), due to the high k of the oxide layer. Neglecting interface charge and assuming that the charge in the channel was the same for the HFET and the MOSHFET, the threshold voltage of the MOSHFET can be related to the threshold voltage of the HFET by
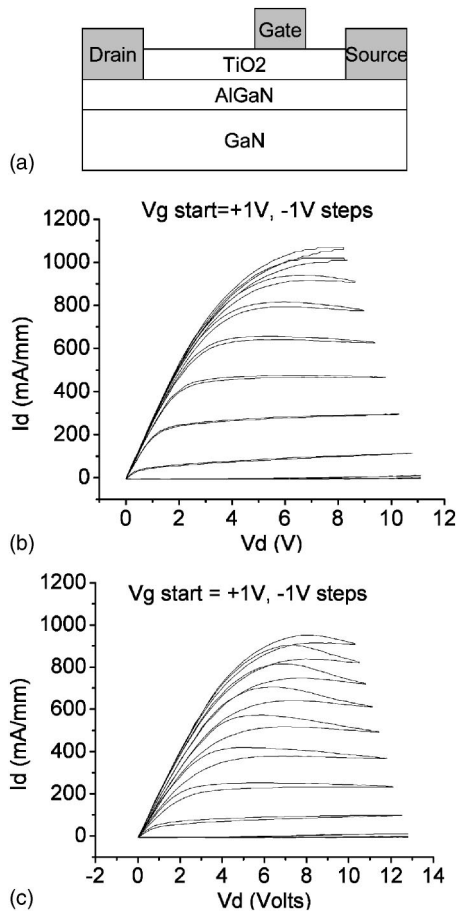
FIG. 8. (a) Device schematic of a MOSHFET with TiO_2 under the gate. (b) $I-V$ characteristics of a standard device with no oxide. (c) $I-V$ characteristics of a device with a 500 Å thick TiO_2 films grown at $T_{sub}=500\,°C$ under the gate.

FIG. 9. (a) Transfer characteristics and (b) transconductance curves for devices from Fig. 8.

$$Q = qn_s = C_{MS}V_{TMS} = C_{MOS}V_{TMOS}, \tag{5}$$

where V_{TMS} and V_{TMOS} are the threshold voltages of the standard HFET structure and the MOSHFET, respectively. The difference between this estimate and the data are related to the interface charge or oxide charge. Using the C_{MS} and V_{TMS} as well as C_{MOS} from Fig. 7, the threshold voltage of the MOS capacitor can be estimated to be approximately −8 V, which is in good agreement with the data and also indicates a low density of interfacial trap states. The data shown was for the best device measured and several other die showed a slightly lower threshold voltage, indicating a slight loss of charge. In this case the charge discrepancy was typically $(1-1.5)\times10^{12}$ lower than that of the standard devices. Hall data were taken prior to and following oxide growth on the same patterned die. The carrier concentration n_s was measured to be 1.40×10^{13} cm^{-2} and the mobility was 1707 cm^2 V^{-1} s^{-1} prior to oxide growth. Following growth these values were 1.36×10^{13} cm^{-2} and 1755 cm^2 V^{-1} s^{-1}, respectively. These results indicate that the AlGaN/GaN structure retained its integrity during oxide growth.

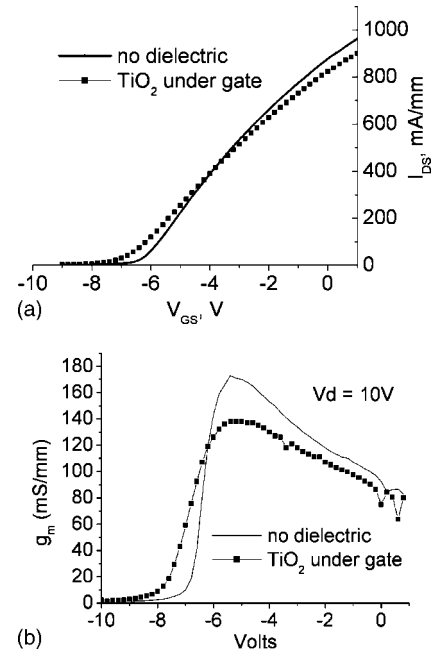Figure 8(a) shows a schematic of the devices on AlGaN/GaN structures with TiO_2 under the gate. The device dimensions were as follows: 75 μm gate width, 0.7 μm gate length, 0.7 μm source–gate spacing, and 2 μm gate–drain spacing. $I-V$ characteristics from a standard die measured prior to TiO_2 deposition and an adjacent die following TiO_2 deposition are shown in Figs. 8(b) and 8(c), respectively. The maximum current for the standard device was 1.1 A/mm, while the maximum current was 1 A/mm for the device with TiO_2 under the gate. Hysteresis in the $I-V$ characteristics measured with the curve tracer is the result of traps in the structure. The hysteresis in the device with TiO_2 under the gate is larger than that of the standard device, indicating trapping at the interface or in the film.

Figures 9(a) and 9(b) show the transfer characteristics and transconductance, respectively, of the devices from Fig. 8. The saturated current density of the MOSHFET was slightly lower than the measured value for the HFET at a positive gate voltage of 1 V. The high k of the oxide allows the transconductance to only drop to ~140 mS/mm as compared to ~177 mS/mm for the HFET, even though the gate to channel separation of the MOSHFET is increased by 50 nm as compared to the HFET. This increase in gate–channel separation also results in a more negative threshold voltage, although again the high k of the oxide results in a small impact, as can be seen in Fig. 9. The transconductance loss and threshold voltage shift are in good agreement with those expected from the capacitance ratios of the devices with and without a TiO_2 gate dielectric. Two terminal gate leakage measurements for devices with and without the TiO_2 gate dielectric layer are shown in Fig. 10. The gate leakage was reduced by about 4 orders of magnitude for devices with a TiO_2 gate dielectric.
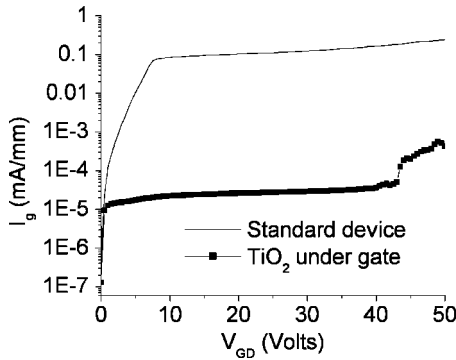
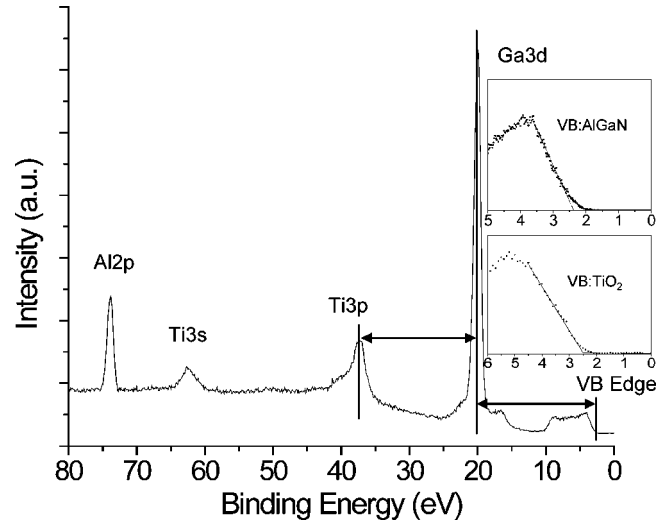FIG. 10. (a) Two terminal leakage characteristics of device from Fig. 8.

FIG. 11. XPS spectra showing core level peaks of 15 Å TiO$_2$ on AlGaN as well as AlGaN TiO$_2$ valence band leading edges (inset). The double arrows indicate separation between the core levels as well as an example of the core level-valence band offset used in the band offset calculations.

C. Band offset measurements

One possible drawback to using TiO$_2$ as a gate dielectric is that the band gaps of oxides typically decrease with increasing dielectric constant.[34] Rutile has a band gap of 3.0 eV, while that of anatase is 3.2 eV.[35] Given the wide band gap of GaN (3.42 eV), knowing the band offsets between the insulator and semiconductor is very important. The band offset can be determined by measuring the energy difference between a core level and the valence band edge $(E_{CL}-E_V)$ for each material in a heterojunction as well as the difference between the core level binding energy (ΔE_{CL}) across the heterojunction.[33] In the TiO$_2$/GaN(AlGaN) system $(E_{CL}-E_V)$ corresponds to $(E_{3p}^{Ti}-E_V)_{TiO_2}$ for the TiO$_2$ and $(E_{3d}^{Ga}-E_V)_{GaN(AlGaN)}$ for the GaN system, and ΔE_{CL} is given by $(E_{3d}^{Ga}-E_{3p}^{Ti})$ and is measured across the interface of the samples with thin TiO$_2$. The energy difference between the valence bands can be calculated by

$$\Delta E_V = (E_{3d}^{Ga} - E_{3p}^{Ti}) + (E_{3p}^{Ti} - E_V)_{TiO_2} - (E_{3d}^{Ga} - E_V)_{GaN}. \qquad (6)$$

The valence band edge is difficult to estimate with accuracy. Linear extrapolation of the valence band leading edge to the energy axis can be used with an estimated accuracy of ± 0.1 eV.[36] The resolution of this method can further be enhanced to ± 0.05 eV by performing a linear regression of the linear portion of the leading edge of the valence band as well as on a set of background channels between the valence band maximum and the Fermi level and taking the intersection of the two as the valence band maximum.[37] This method has been shown to agree well with the method of Kraut *et al.*[33] that consists of fitting the measured valence band spectra with the broadened theoretical valence band density of states by the instrument response function, which is determined by fitting the Au 4f core level with theoretical peaks.[36,37]

The linear regression method performed on the valence band edge of GaN resulted in the band edge energy of 2.95 ± 0.05 eV. The centroid of the Ga 3d peak was at 20 eV, making $(E_{3d}^{Ga}-E_V)_{GaN}=17.05\pm 0.1$ eV. Values in the literature have been reported as 17.7–17.8 eV[38,39] and 17.1 ± 0.1 eV.[40] Kočan *et al.* measured a GaN template grown at University of California, Santa Barbara (UCSB) (although on SiC) and from the valence band edge and the position of the Ga 3d peak shown $(E_{3d}^{Ga}-E_V)_{GaN}\sim 17.2$ eV can be deduced.[41] Sev-

eral samples were measured and a similar value of 17.1 ± 0.1 eV was obtained. The value of $(E_{3d}^{Ga}-E_V)_{AlGaN}$ was measured to be 17.16 ± 0.05 eV. $(E_{3p}^{Ti}-E_V)_{TiO_2}$ was measured to be 34.45 ± 0.05 eV, which is in reasonable agreement with the value of 34.38 ± 0.05 eV reported for anatase TiO$_2$.[36] The core level peak spectra of 15 Å TiO$_2$ on AlGaN as well as the "bulk" TiO$_2$ and AlGaN valence band leading edges are shown in Fig. 11. The values of $(E_{3d}^{Ga}-E_{3p}^{Ti})$ for the 15, 30, and 50 Å films were found to be -17.3 ± 0.2 eV for both the GaN and AlGaN samples. The valence band offset obtained for GaN from Eq. (6) is then $\Delta E_V = 0.09\pm 0.25$ eV. As discussed earlier, the band gap of (bulk) rutile is 3.0 eV and GaN is 3.42 eV. Using the equation

$$\Delta E_C = (\Delta E_G)_{\text{Rutile-GaN}} + \Delta E_V, \qquad (7)$$

where $(\Delta E_G)_{\text{rutile-GaN}}$ is the difference between the rutile and GaN band gaps, ΔE_C is estimated to be -0.34 ± 0.25 eV. A schematic of the proposed lineup is shown in Fig. 12. The composition of the AlGaN layer in this experiment was Al$_{0.33}$Ga$_{0.67}$N. Using the equation $E_g(x)=x6.2$ eV$+(1-x)3.4$ eV$-x(1-x)1.0$ eV to determine the band gap of
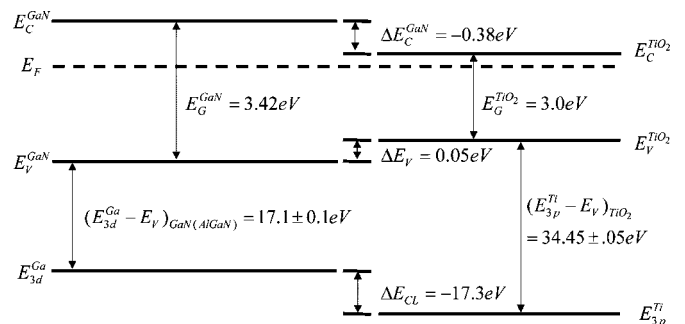

FIG. 12. Proposed band lineup (not drawn to scale) between TiO$_2$ and GaN based on data from XPS measurements.

AlGaN, $E_{g(AlGaN)} = 4.10$ eV.[42] The valence band offset obtained from Eq. (6) for AlGaN is 0.01. Using Eq. (7), the conduction band offset is -1.1 eV (from AlGaN to TiO_2).

We report these numbers with some caution, noting that if the commonly accepted value of $(E_{3d}^{Ga} - E_V)_{GaN}$ of 17.7 eV is used, the valence band offset becomes $\Delta E_V = -0.55 \pm 0.25$ eV and $\Delta E_C = -0.98 \pm 0.25$ eV for GaN. In either case, this band lineup is not ideal for an insulator on a semiconductor for forward bias of devices. In electrical testing of HFET structures it was found that the leakage behavior of the devices in forward bias behaved very similarly to that of the uninsulated gate structures, indicating that an unfavorable band lineup was also present for the TiO_2/AlGaN structures. Since AlGaN/GaN HFET structures are normally on devices, however, the reverse-bias gate leakage of the device is most important. The mechanism of leakage reduction in the reverse bias condition is not currently understood and is under investigation.

IV. CONCLUSIONS

In conclusion, phase-pure films of the rutile polymorph of TiO_2 have been grown by MBE on GaN and AlGaN/GaN structures. The (100) oriented TiO_2 oxide films were found to grow epitaxially with reasonable structural characteristics despite the large lattice mismatch. No reaction or intermixing at the TiO_2/GaN or TiO_2/AlGaN interface was detected by TEM. The oxide films were found to have a high dielectric constant of approximately 70. This resulted in a minimal effect on device properties such as transconductance and threshold voltage. Gate leakage was reduced by 4 orders of magnitude, but XPS investigations of the band offsets of the insulator on semiconductor indicated that the band lineup is not favorable.

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