University of California
Santa Barbara

Energy-Efficient High-Performance CMOS VLSI Design for Electronic-Photonic Integration and Biological Applications

A dissertation submitted in partial satisfaction
of the requirements for the degree

Doctor of Philosophy
in
Electrical and Computer Engineering

by

Mitra Saeidi

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To Navid, and my parents, Reza and Mahshid

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Publications

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J5 **M.Saeidi**, L. Theogarajan, "The Electronics Behind The Nanopore Sensor: Architectures, Design Methodology & Challenges," 2021 (submitted to Frontiers in Nanotechnology)

C5 **M.Saeidi**, L. Theogarajan, "A Current-to-Digital $\Delta\Sigma$ ADC for Low-Noise High-Precision Applications," 2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 667-670, 2020

C4 A. Malik, S. Liu, and E. Timurdogan, M. Harrington, A. Netherton, **M.Saeidi**, D. Blumenthal, L. Theogarajan, M. Watts and, J. Bowers, "Low power consumption silicon photonics datacenter interconnects enabled by a parallel architecture," 2021 Optical Fiber Communications Conference and Exhibition (OFC), 2021, pp. 1-3.

J4 T. Hirokawa, **M. Saeidi**, S. Pillai, A. Nguyen-Le, L. Theogarajan, A. A. M. Saleh, and C. L. Schow, "A wavelength-selective multiwavelength ring-assisted MachZehnder interferometer switch," in Journal of Lightwave Technology, vol. 38, no. 22, pp. 6292-6298, November 2020.

C3 T. Hirokawa, A. Netherton, **M. Saeidi**, H. Andrade, L. Theogarajan, J. E. Bowers, A. A. M. Saleh, C. L. Schow, "An all-optical wavelength-selective O-band chip-scale silicon photonic switch," 2020 Conference on Lasers and Electro-Optics (CLEO), PP. 1-2, 2020

C2 T. Hirokawa, **M. Saeidi**, L. Theogarajan, A. A. M. Saleh, C. L. Schow, "Ring-assisted Mach-Zehnder interferometer switch with multiple rings per switch element," Optical Interconnects XX, VOL. 11286, PP. 1128612, 2020

J3 P. Srinivasan, N. M Griffin, P. Joshi, D. Thakur, A. Nguyen-Le, S. McCotter, A. Jain, **M. Saeidi**, P. Kulkarni, J. T. Eisdorfer, J. Rothman, C. Montell, L. Theogarajan, "An Autonomous Molecular Bioluminescent Reporter (AMBER) for voltage imaging in freely moving animals," in BioRxiv, pp. 845198, 2020.

J2 A. S. P. Khope, **M. Saeidi**, R. Yu, X. Wu, A. M. Netherton, Y. Liu, Z. Zhang, Y. Xia, G. Fleeman, A. Spott, S. Pinna, C. Schow, R. Helkey, L. Theogarajan, R. C Alferness, A. A. M. Saleh, J. E. Bowers, "Multi-wavelength selective crossbar switch," in Optics express, vol. 27, no. 4, pp. 5203-5216, Feb. 2019.

C1 T. Hirokawa, **M. Saeidi**, A. Maharry, R. Helkey, J. E. Bowers, L. Theogarajan, A. A. M. Saleh, C. L. Schow, "A spectrally-partitioned crossbar switch with three drops per cross-point controlled with a driver," 2019 IEEE Photonics Conference (IPC), pp. 1-2, 2019.

J1 A. S. P. Khope, T. Hirokawa, A. M. Netherton, **M. Saeidi**, Y. Xia, N. Volet, C. Schow, R. Helkey, L. Theogarajan, A. A. M. Saleh, J. E. Bowers, R. C. Alferness, "On-chip wavelength locking for photonic switches," Optics letters, vol. 42, no. 23, pp. 4934-4937.

Awards

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Abstract

Energy-Efficient High-Performance CMOS VLSI Design for Electronic-Photonic Integration and Biological Applications

by

Mitra Saeidi

Data analysis, storage and communication has become a very important subject for research nowadays. Due to higher demand for data, power and area reduction have drawn more attention in recent research. In this dissertation we propose new system for data communication through optical links which is area and power efficient while maintaining high performance. We also propose a new approach for biosensing which also focuses on area and power efficiency with improved performance which enables analyzing huge amounts of data.

In the first part of this dissertation, a 1Tb/s transceiver system is introduced. This system is designed for microring resonator links. Therefore, a control loop design is also introduced in this part for wavelength locking. Two versions of the 1Tb/s transceiver with less than 90fJ/bit energy efficiency is implemented in 22nm FDSOI to achieve 5Tbit/(mm^2) and 0.8Tbit/(mm^2) densities. New system and circuit designs are proposed to achieve such low power and density at 1Tb/s. A closed loop wavelength locking control loop is also proposed consuming low power and area while locking the rings in less than 25μs. A 20 channel wavelength locking system is implemented in TSMC 65nm.

In the second part of this dissertation, we introduce biological sensors and sensor interfaces for biological applications. Nanopore sensors enable a wide range of sensors from DNA sequencing to polymer mass spectrometry by exploiting the resistive pulse technique. The small and high-speed sensor signal can make the electronics design chal-

lenging. The designer is often faced with a bewildering choice of architectures and circuit topologies. In this part, we review the most prominent circuits and architectures used in nanopore sensing highlighting the advantages and disadvantages of each approach. Additionally, noise analysis and SNR calculations are shown for each topology. We also provide a graphical method to allow the designer to narrow down their choice for a given set of requirements. As the need for large sensor arrays is continually increasing, we discuss the different approaches to scaling the system when using an array of sensors.

We also introduce the system design of a new high precision potentiostat. Our direct current-to-digital conversion is capable of sensing picoampere (pA) currents without a need for transimpedance amplifiers (TIAs). Our idea utilizes a $\Delta\Sigma$ modulator with one very important difference, current feedback via slope scaling. This feature allows us to utilize noiseless elements such as capacitors in the feedback loop to achieve high performance. We have validated the system using both theory and experiment. Performance improvement over current systems is first demonstrated by performing a theoretical analysis of the expected noise of the system. A 10×10 cm^2 PCB prototype was fabricated as a proof of concept. The slope scaling idea is applied to both first and second order $\Delta\Sigma$ Analog to Digital Converters (ADCs) with signal input bandwidth of 1.57 KHz with an oversampling ratio of 64. Signal-to-Noise-and-Distortion Ratio (SNDR) of 40 dB and 60 dB is achieved with 1$^{\text{st}}$ and 2$^{\text{nd}}$ order $\Delta\Sigma$ ADCs, respectively. The noise floor of the implemented circuit is 569 fA over a 1KHz bandwidth and was tested for input currents ranging from 100 pA to 1 μA.

In this part, we also propose a direct current to digital 125μW, area efficient ($0.042mm^2$) 81dB DR, 8KS/s current sensing ADC implemented in 45nm CMOS capable of sensing sub-pA currents. Our approach combines the TIA and ADC into a unified structure by folding a low-noise capacitive TIA into the first stage integrator of a 2^{nd} order Delta-Sigma ($\Delta\Sigma$) modulator. We mitigate the common issue of feedback DAC noise faced

by current sensing $\Delta\Sigma$ converters by using a low-noise current scaling technique. In our approach an integrator-differentiator pair scales the DAC feedback current using capacitors. Since the DAC is current based the integrator is simply a charge-pump, alleviating the bandwidth issues arising from the periodic reset required by the integrator. However, the periodic reset forces the converter to operate in an incremental mode lowering the dynamic range of the converter. We overcome this by using a floating correlated double sampling (CDS) technique. The correlated double sampling also enables the use of single stage common source amplifiers while achieving a high-gain resulting in a low-power area-efficient design.

The material in this dissertation has been partially appeared in the following publications:

- **M. Saeidi**, L. Theogarajan, "A 125μW 8kS/s Sub-pA Area-Efficient Current Sensing 45nm CMOS ADC for Biosensing," 2021 arxiv preprint
- **M.Saeidi**, L. Theogarajan, "The Electronics Behind The Nanopore Sensor: Architectures, Design Methodology & Challenges," 2021 (submitted to Frontiers in Nanotechnology)
- **M.Saeidi**, L. Theogarajan, "A Current-to-Digital $\Delta\Sigma$ ADC for Low-Noise High-Precision Applications," 2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 667-670, 2020
- A. S. P. Khope, **M. Saeidi**, R. Yu, X. Wu, A. M. Netherton, Y. Liu, Z. Zhang, Y. Xia, G. Fleeman, A. Spott, S. Pinna, C. Schow, R. Helkey, L. Theogarajan, R. C Alferness, A. A. M. Saleh, J. E. Bowers, "Multi-wavelength selective crossbar switch," in Optics express, vol. 27, no. 4, pp. 5203-5216, Feb. 2019.

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Chapter 1

Introduction

Due to the demands for higher data process and storage, in many applications, the electronic is moving towards compact, and low power VLSI circuit design. Therefore, new techniques and system and circuit innovations have been developed in order to move towards scalable, compact and low power design. This dissertation focuses on scalable, compact and low power CMOS VLSI design for two different applications. System and circuit design for electronic-photonic chip-to-chip interconnects are investigated first. The second application being investigated is system and circuit design for biological applications.

1.1 Chip-to-Chip Electronic-Photonic Integration

Communication networks and consumer devices have been developing continuously in the last few decades due to the high demands. As a result, data centers require to increase their data storage capacity which results in higher power consumption. It is anticipated that data centers will use around $3\% - 13\%$ of global electricity in 2030 compared to 1% in 2010 [1]. Over the past decade, data center electricity usage has remained almost

constant, mostly because of hyper-scale data centers which use super efficient computing servers [2]. Although hyper-scale data centers have played a huge role in power usage reduction, there has been an ongoing effort on other aspects to keep the electricity usage almost constant including several management techniques and improving processors. One of the recent challenges is that due to high data demand, there has also been increased data processing happening inside data centers which is limited by electrical cables even for short distances. As a result, optical signaling has replaced electrical signaling due to their high energy efficiency, compactness, immunity to electromagnetic interference, low channel loss and high bandwidth capacity per cable.

However, one of the challenges of adopting optical signaling over electrical signaling is integration of electronics and photonics. There has been efforts made through years developing different and efficient integration techniques. 2.5D co-packaged optics with electronics on an interposer, Monolithic integration of optics and electronics and 3D integration of optics and electronics are some of the integration achievements.

1.1.1 Transceiver Systems

Transceiver systems are composed of a transmitter and receiver. Central to transmitters is the photonic modulator. Two popular silicon photonic modulators are Micro ring Modulator (MRM) and Mach-Zehnder Modulator (MZM). MRMs are more compact than MZMs and have inherent wavelength selectivity.

One of the most attractive options for data center interconnects is the Wavelength-Division Multiplexed (WDM) silicon photonic links which enables placing many data channels on a single optical fiber. A WDM silicon photonic link is shown in Fig. 1.1 with 4 data channels. Main component in WDM links is Micro-Ring Resonator which enables small interconnect implementations. MRM is a resonant photonic device which modu-

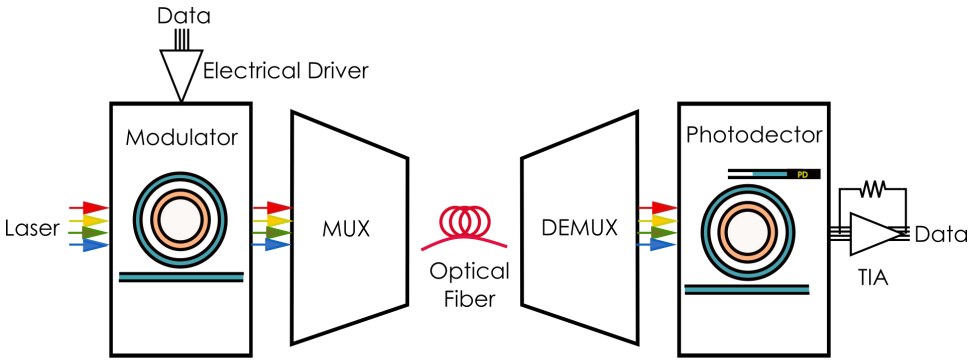

Figure 1.1: Micro ring resonator based transceiver system.

lates the light from laser by shifting its resonance. In order to shift their resonance, high speed voltage drivers with high data rate is designed. Insertion Loss (IL) and Extinction Ratio (ER) are key factors in optical transmitter design. Proper design can increase the optical modulation amplitude or decrease the laser power in the link. Optical receiver can use a microring filter to receive optical signal at a specific laser wavelength for WDM operation. As shown in Fig. 1.1 the drop port of the optical filter is connected to a photodetector to convert optical signals into electrical signals which then converts to voltage using Transimpedance Amplifiers (TIA).

1.1.2 Microring Resonator Control Systems

In order to change the desired wavelength, a heater is implemented inside the ring which its radius changes with temperature. Therefore, heating and cooling via changing the current flowing through the heater is one way to change the wavelength, named thermal tuning. Microring resonators' sensitivity to temperature however has a drawback. Microring resonators' resonance drifts around with temperature changes and process variations; therefore, locking the MRMs to resonance comes as a challenge. Electro-optic

tuning is another way to change the wavelength of the rings which is based on carrier depletion. Therefore, applying a voltage across the ring, the wavelength is changed.
In this dissertation we propose system and circuit solutions for transmitting and receiving data at low power and area while maintaining the speed and a high performance. We also propose solutions for locking micro ring resonators at a desired wavelength with minimized variations, area and power consumption thanks to the proposed closed loop techniques.

1.2 Biological Applications

As the demand for implantable devices increase, the need for compact, area-efficient developed sensor interfaces also increases. As a result, recent research has focused on improvement of sensor interfaces for biological application like physiological monitoring.

One of the most important research throughout decades has been on disease diagnostics and treatment. Since the discovery of Deoxyribonucleic acid (DNA) these studies have been continuously developing. DNA is a molecule which contains unique biological instructions for each individual. Therefore, reading each unique DNA can help diagnose any genetic disorder or find the genetic causes and rare diseases. DNA researches have been moved towards reading large arrays of DNA with higher speed and less cost which enables them to compare the DNA structures. These comparisons result in a large amount of information about the role of inheritance and environmental influences to diseases which leads to diagnostics and treatments. One popular technique for fast and low cost analysis of high throughput DNA is nanopore sequencing. The other interesting biological research is neural recording. Observing activity of large numbers of neurons in the brain simultaneously [3] is one ongoing research which requires more advances in sensor interfaces.

1.2.1 Nanopore Sensors

Inspired by biology, nanopores have emerged as a possible single-molecule electronic detection platform [4–6]. A nanopore is an extremely tiny hole, few nanometers in diameter, in an insulating membrane that separates two ionic reservoirs. An applied voltage across the nanopore results in an ionic current that flows through the nanopore. The principle of single-molecule detection using the nanopore is based on detecting the blockage of this ionic current by the target. The first application of nanopores to biosensing was performed using a biological pore, α-Hemolysin, for the possible sequencing of DNA [7]. Since then there has been steady progress in the use of nanopores for biosensing and has resulted in a commercial DNA sequencer, the MinIon by Oxford Nanopore Technologies [8, 9]. Apart from biological pores used for DNA sequencing, solid-state nanopores in a wide variety of materials, including 2D-materials, have been explored for various applications [10, 11].

The basic nanopore sensor consist of either a biological pore, such as an ion-channel (e.g. α -Hemolysin, α-HL) embedded in a lipid bilayer or a tiny hole in a solid-state membrane (e.g. SiN_3). Biological pores offer superior pore geometry, enable functionalization of the pore, and are easily wettable. However, they are not as stable as their solid-state counterparts. Solid-state pores offer precise control of the pore position and patterning but can be difficult to wet and are generally more noisy. From the perspective of the electronics, biological pores generally can only tolerate transmembrane voltages of $\approx$ 300mV, have a pore conductance in the order of 1nS and lipid bilayer capacitance of $1\mu F/cm^2$. Typical bilayer are $\approx 50\mu$m in diameter, yielding $\approx$ 20pF capacitance. Solid-state pores usually have lower capacitance for the same membrane diameter since they are fabricated on thicker membranes, and generally have larger pore currents, since the pore diameters are much larger (10's of nanometers) compared to biological pores

(around 1 nm). Solid-state pores normally require higher transmemebrane voltage to achieve analyte translocation. There are multiple noise sources, such as 1/f, thermal noise and dielectric noise at play in both biological and solid-state pores [12]. In general, solid-state pores show larger 1/f noise due to the introduction of trap states during fabrication, though membrane-protein interactions can also increase 1/f noise in biological pores [13]. Experiments on biological nanopores (MspA, α-HL and ReFrac) show 8-40pA rms noise at 10-30kHz bandwidth, while the experiments on solid-state nanopores (MoS_2 and SiN_x) show 100-130pA rms noise at 10-500kHz bandwidth [12].

1.2.2 Current Sensing

Amperometric sensing is a common method for biosensing [14–19]. Central to amperometric sensors are transimpedance amplifiers, which sense current while clamping the potential. Transimpedance amplifiers (TIAs) utilize an impedance in the feedback to convert the current into a voltage. Resistive feedback TIAs perform a direct conversion, while the lower noise integrator topology employs a capacitor in the feedback and requires a differentiation to counteract the frequency shaping of the integrator. Resistive TIAs suffer from low bandwidth due to the large feedback resistors necessary to convert small currents, while integrating TIAs requiring periodic resetting to avoid saturation due to DC currents. One method to avoid resetting the integrator utilizes a DC cancellation feedback network [14]. Some designs utilize the large input capacitance, as in the case of an electrochemical sensor, to implement an opamp-less integrator within a $\Delta\Sigma$ topology [17], [18]. However this approach is limited to first-order $\Delta\Sigma$ resulting in lower bandwidth and requiring higher sampling frequencies.

1.3 Contributions and Organization

This dissertation is divided into two parts proposing compact, area-efficient and high performance CMOS VLSI design for two different applications. In the first part, we propose a WDM based transceiver system to increase bandwidth while decreasing power and area. In WDM links, calibration of process variations and temperature fluctuations is required to guarantee the proper operation of MRMs. Therefore, we show our proposed high performance wavelength locking loops with their implementations. The second part of this dissertation is focused on design techniques for biological current sensing and we propose a direct current to digital conversion structure for smaller current detection in higher bandwidth while decreasing power and area consumption.

The organization of this dissertation is as follows.

Chapter 2 introduces a fully integrated transceiver system for the specifications dictated by the application. Conventional structures are analyzed along with their challenges. The circuits used and designed in the proposed system are introduced and the implementation in 22nm FD-SOI with simulation results are reported. The system operates at 1Tb/s while only consuming less than 90fJ/bit at 0.8v supply. Two variations of the system with $2mm^2$ and $\sim 0.6mm^2$ area are designed with the same data rate and power consumption.

Chapter 3 discusses different approaches for tuning of the rings. Two different implementations of open loop and closed loop are introduced with measurement results. The open loop implementation is a discrete voltage driver with 10v swing and $1\mu s$ time constant.

Closed loop scheme is designed with current and voltage driver option for thermal and EO tuning. Moreover, every circuit in the loop is analyzed with a focus on the current sensing front-end. A 20 channel control system is designed, fully integrated and implemented

in TSMC 65nm with 2.89mm^2 area and 0.7mW power consumption operating at 1.2v supply. The current driver is able to drive up to 1.3mA current and voltage driver's swing is 6v. The measurement results show about 25 μs time constant.

Chapter 4 introduces different current sensing approaches for biological applications. Different approaches are reviewed, analyzed and required equations are exploited. Then, a graphical design methodology is developed for ease of design choice depending on the specifications. This chapter introduces different arraying approaches and two design methodologies, one for current sensing front ends and one for Delta Sigma current-to-digital direct conversion.

Chapter 5 presents a novel direct current to digital conversion. The system is simulated in MATLAB and implemented on PCB and the measurement results are reported. The measurement results show 100 pA to 1μA current detection in 1.57 KHz bandwidth with an oversampling ratio of 64. Signal-to-Noise-and-Distortion Ratio (SNDR) of 40 dB and 60 dB is achieved with 1st and 2nd order $\Delta\Sigma$ ADCs, respectively. The noise floor of the implemented circuit is 569 fA over a 1KHz bandwidth.

Chapter 6 Discusses design and implementation of the developed direct current to digital converter integrated on chip implemented on 45nm RF SOI. The system and circuit is analyzed and the measurement results are reported. The implemented 125μW, area efficient (0.042mm^2) 81dB DR, 8kS/s current sensing ADC is capable of sensing sub-pA currents. Our approach combines the transimpedance amplifier (TIA) and ADC into a unified structure by folding a low-noise capacitive TIA into the first stage integrator of a 2^{nd} order Delta-Sigma modulator. The dominant DAC feedback noise is mitigated by utilizing current scaling via slope modification by an integrator and differentiator pair.

1.4 Permissions and Attributions

Part I

Energy-Efficient High-Performance CMOS VLSI Design for Electronic-Photonic Integration

Chapter 2

3-D-Integrated Silicon Photonic Microring-Based Transceiver

2.1 Introduction

Wavelength Division Multiplexing (WDM) links have been drawn attention for use in data center interconnects. High speed optical link interconnects require high speed, low power and area efficient transmitters and receivers. To achieve 1Tb/s with $0.8Tb/mm^2$ and $5Tb/mm^2$ density requirements, 40 MRM based optical links are used which puts less demand on each link (26.7Gb/s). Therefore, for area requirement, better performance and smaller parasitic capacitance between electronics and photonic devices, 3D integration is chosen over monolithic. This chapter presents a fully integrated chip-to-chip link implemented in 22nm CMOS SOI process.

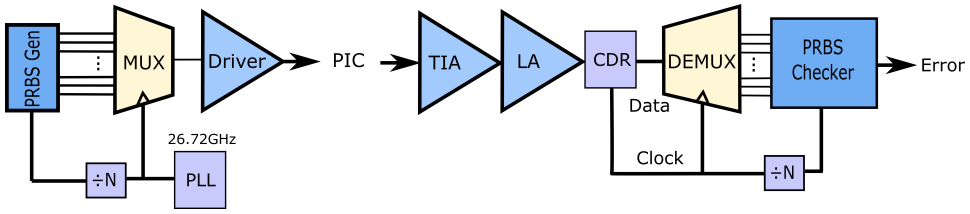

Figure 2.1: Illustration of a conventional transceiver system.

2.2 Chip Architecture

Two chips with 36μm and 75μm pad pitch are designed to satisfy $0.8Tb/mm^2$ and $5Tb/mm^2$ density requirements. Each chip is composed of 40 MRMs on transmit side and 40 Photodiodes (PD) on receive side. Both chips are designed to deliver maximum of 90fJ/bit energy efficiency. Each chip is composed of two sides: Transmitter and Receiver, but they are designed such that they are completely separate as in real life.

2.3 Transceiver System Design Challenges

The most challenging requirement at this speed is energy efficiency. To reduce the power consumption of such system, we investigate conventional systems and structures.

2.3.1 Conventional System Overview

A conventional Transceiver system is shown in Fig. 2.1. As it is shown, the transmitter side is composed of a $2^{31}-1$ bit Pseudo-Random Binary Sequence (PRBS) generator to imitate the data aggregator in data centers. For an 8 to 1 multiplexer, to generate a 26.7Gb/s signal, the PRBS generator must operate with a 3.34GHz clock. Therefore, the PRBS generator bit stream would be a 3.34Gb/s signal. The serializer with tree structure shown in Fig. 2.2 is composed of an 8:4, 4:2 and 2:1 multiplexers and a flip flop re-timing the signal at 26.7GHz. The multiplexed signal is followed by a high speed

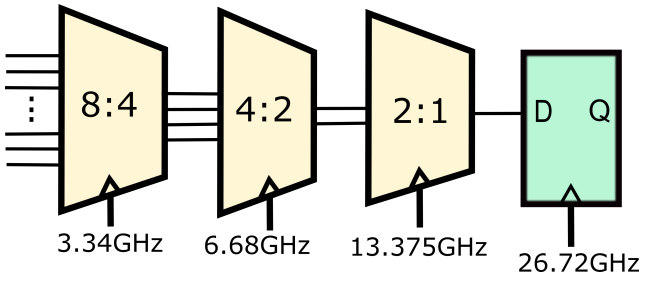

Figure 2.2: Tree structure serializer.

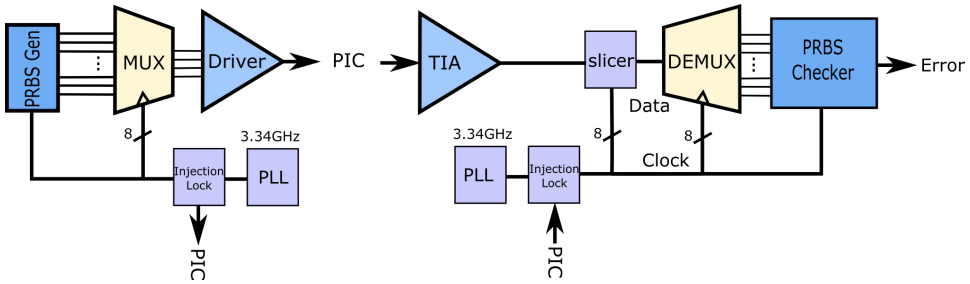

Figure 2.3: Illustration of the proposed transceiver system.

driver to drive the MRMs. Therefore, for a 40 channel transmitter a 26.7GHz PLL should be designed. The 26.7GHz clock gets distributed to each channel, and dividers to divide the clock down to 13.37GHz, 6.68GHz and 3.34GHz. On the receiver side, a high speed and low noise TIA receives the signal from the PDs, converts it to voltage, a Clock Data Recovery (CDR) recovers the clock, data gets re-timed with the clock and PRBS checker checks for its errors. On receive side also a divider is needed to divide down the clock from 26.7GHz same as the transmitter side to provide demultiplexer and PRBS checker clocks.

Therefore, 26.7GHz clock distribution and dividers, PLL and CDR operating at 26.7GHz, Driver and TIA would consume all the power and exceed the power budget.

2.4 Proposed System

In order to be able to implement a system with required specifications in terms of speed, power and area, as shown in Fig. 2.3 we modified the system such that the 26.7Gb/s signal and 26GHz clock would be present only at TIA and Driver. Therefore, the dominant blocks consuming most of the power would be only the Driver and TIA. To do this, all the clocks are divided down to the minimum clock required (3.34GHz) and therefore serializer, and deserializer structures are modified such that they would be able to operate with the 3.34GHz clock. The PLL now operates at 3.34GHz which relaxes its design complexity and power consumption. The other power hungry main block is CDR. We replace CDR with slicer which cuts the power by a huge amount. The details on designing each block will be discussed next.

2.5 Transmitter Design

In this section, the proposed transmitter architecture will be discussed and each block design will be investigated. Fig. 2.4, shows the proposed transmitter structure with more details for 40 channels. As it is shown, on transmitter side a PRBS generator is shared between 4 serializers. PLL sends the clock to injection lock and injection lock generates 8 phases of the clock which drives the serializers. The high speed data from serializer output is sent to the driver which drives the MRMs, one of the 8 phases of the clock also is sent to the clock driver which drives an MRM which is dedicated to clock. Therefore, data along with clock is transmitted. On receiver side, the data and clock are received by TIA which is sent to the slicer to select the desired channel.

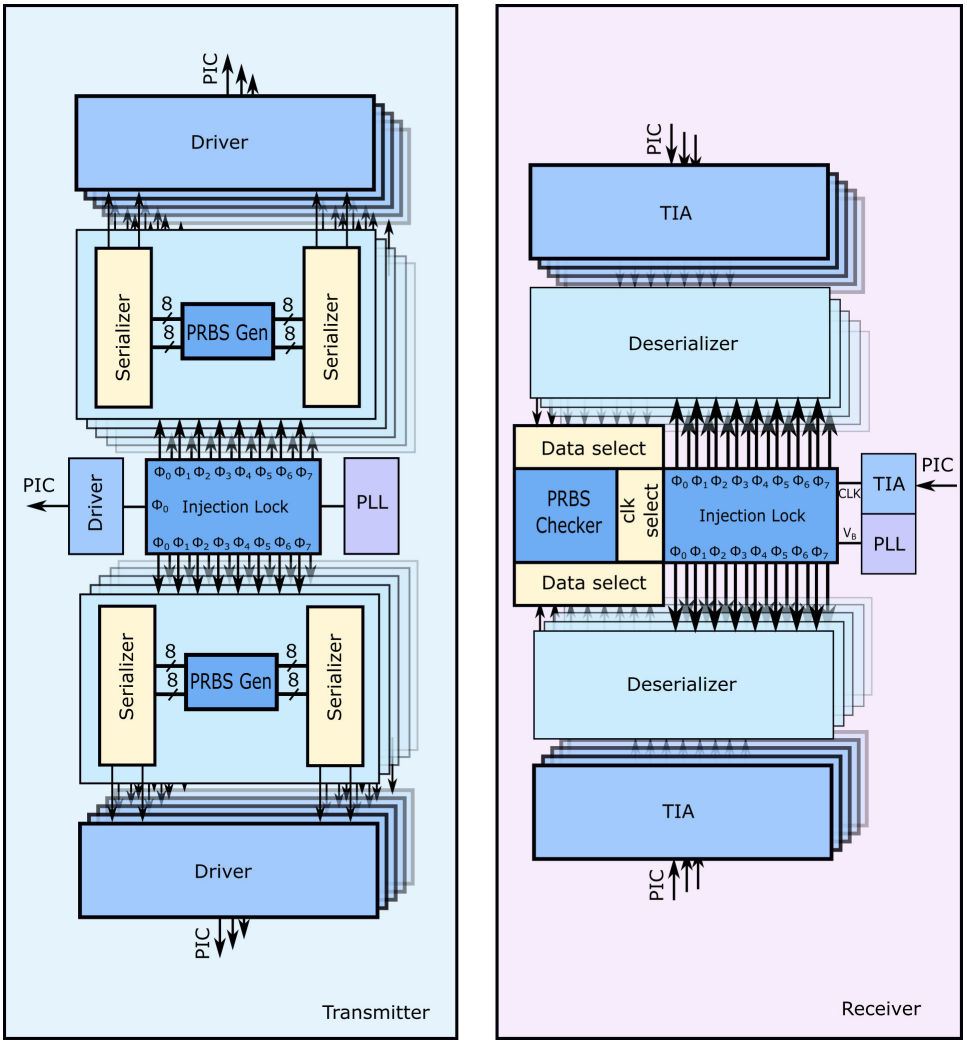

Figure 2.4: Illustration of the proposed transmitter and receiver for 40 channels.

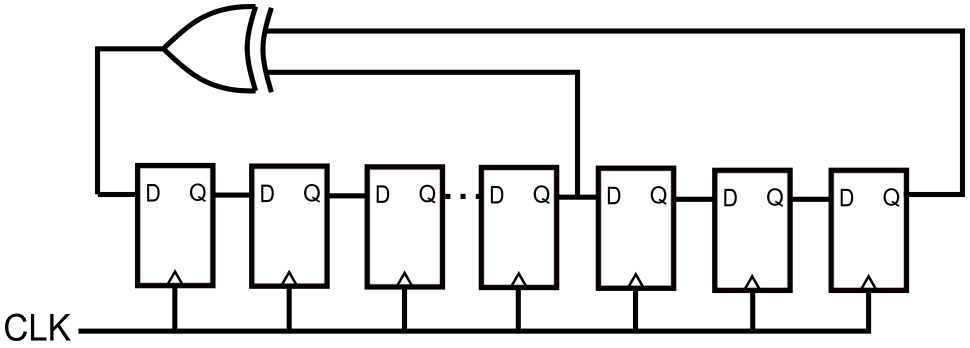

Figure 2.5: Series PRBS generator structure

2.5.1 PRBS Generator

As illustrated in Fig. 2.4, in the proposed system a $2^{31}-1$ bit PRBS generator with 32 outputs operating with a 3.34GHz clock is designed such that it can be shared between 4 channels. The series $2^{31}-1$ bit PRBS generator is shown in Fig. 2.5, which is a Linear Feedback Shift Register (LFSR) consisting of 32 flip flops and one XOR logic to implement the 31 bit PRBS polynomial, which is given as:

$$x^{31} + x^{28} + 1 \tag{2.1}$$

Now, to exploit 32 outputs in series structure, extra logic is required and another 32 flip flops are needed for re-timing the signal at each output [23]. A better structure would be the parallel PRBS generator shown in Fig. 2.6 in which the outputs are arranged such that they have 11.25 degree phase difference with each other and only 31 extra XORs are used. The other advantage of this structure is that it does not require another re-timing flip flop, all the outputs are re timed using the same flip flip.

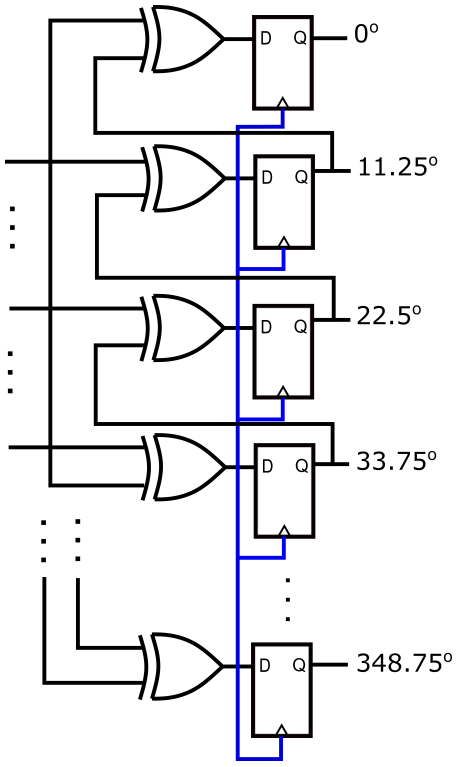

Figure 2.6: Parallel PRBS generator structure

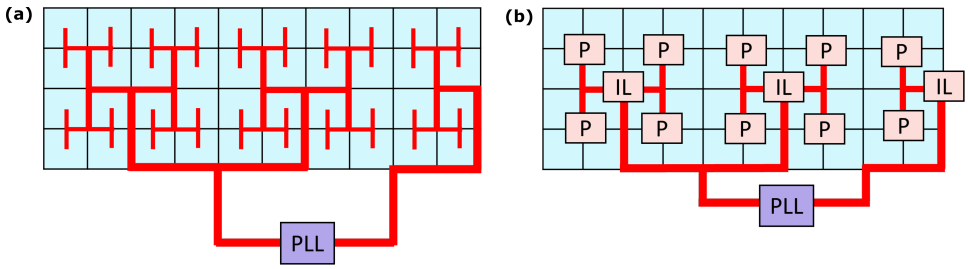

Figure 2.7: Clock distribution scheme for (a) conventional systems (b) proposed system

2.5.2 Clock Distribution System

Fig. 2.7(a) and (b), illustrate clock distribution system for conventional and proposed systems, respectively. In the conventional system shown in Fig. 2.7(a) as described in section 2.3.1, a 26.7GHz clock generated from the PLL is distributed to 40 modulators with H-tree configuration. However, the proposed system shown in Fig. 2.7(b) consists of one PLL operating at 3.34GHz, 3 injection locks shared between 40 transmitters and buffers in H-tree clock distribution. The need for injection locks arises from our proposed system modification. As we discussed earlier, for the transmitter to be able to operate at 3.34GHz clock, a different serializer structure should be used to generate 26Gb/s signal. Therefore, a multi-phase serializer architecture have been used, as will be discussed in detail later, for this serializer to operate, 8 different phases of the clock should be generated and this has been done utilizing injection lock.

2.5.3 Serializer

Due to chip pin count limitations, as the data bandwidth increases serializers are used as a solution to convert the parallel lower speed data into serial higher speed data. A serializer's basic function is shown in Fig. 2.8. In this figure a $2^7 - 1$ bit PRBS generator's output at 3.34Gbps is shown. To generate a 13.375Gbps signal with the same sequence, 4 PRBS sequences with 45 degree phase difference can be multiplexed at twice

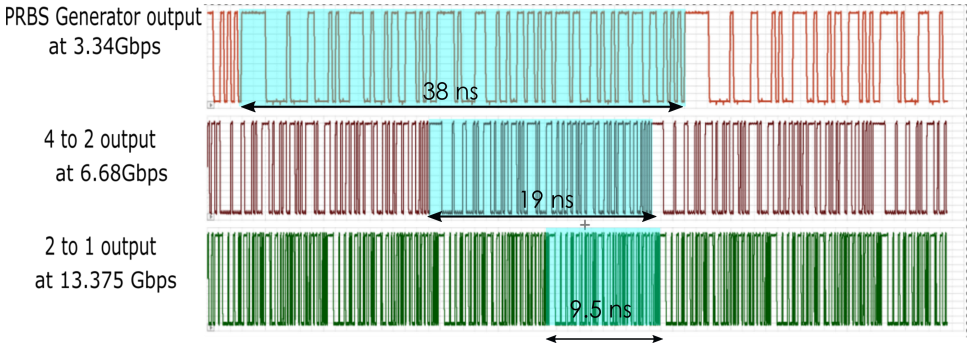

Figure 2.8: Serializer (Multiplexer) functionality

the clock frequency (6.68GHz) which would generate two outputs at 6.68Gbps rate. Then, multiplexing the generated streams at 13.375 GHz, a stream with 13.375Gbps is generated as shown and highlighted in Fig. 2.8. Two conventional serializer structures which are widely used are tree-type [24, 25] and single-stage [26] serializer structures. Tree-type structure was introduced and illustrated in Fig. 2.2. Some serializers use both concepts to benefit from low speed clock while avoiding large loads at the output [27]. However, other limitations of multi-phase serializers like skew and clock gating still exist. The proposed multi-phase serializer is illustrated in Fig. 2.9. The proposed structure benefits from advantages of conventional multi-phase multiplexer structures; which are low power consumption, area efficiency and single stage multiplexing feature. It also alleviates the issues with the conventional multi-phase multiplexer structures; skew, limited speed and clock gating. Therefore, in the proposed structure, instead of gating the clock to generate 26GHz pulse as conventional multi-phase structures, it benefits from latching and resetting data at the neighbor clock phases. Therefore, generating 26GHz pulses are not required. Also, it does not suffer from large parasitic loading; therefore, it removes the speed limitations to some extent. On the other hand, it is a latch based design; therefore, it is skew tolerant, unlike the Flip-flop based structures.

To further understand the proposed serializer, its operation is illustrated in Fig. 2.10.

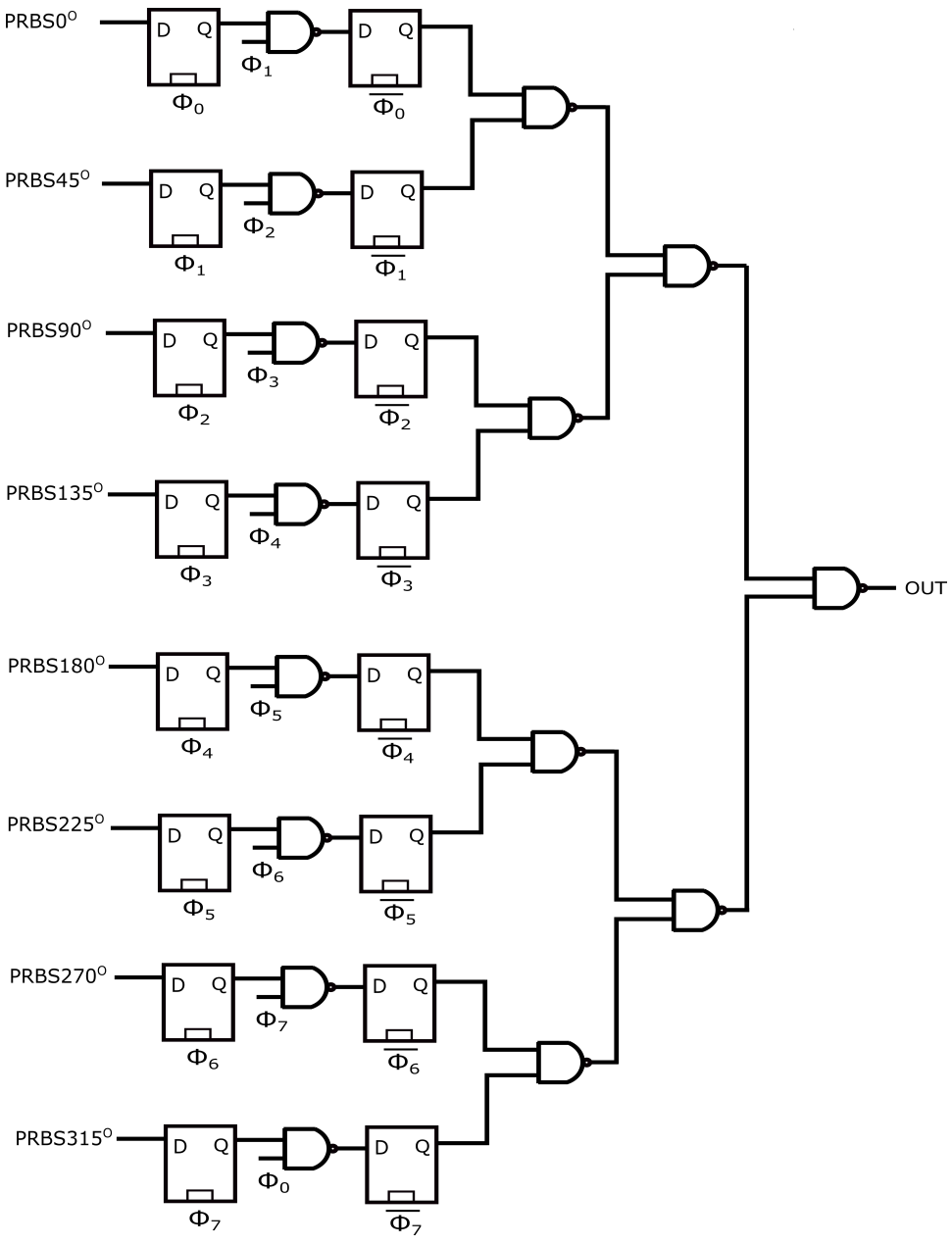

Figure 2.9: Proposed multi-phase serializer

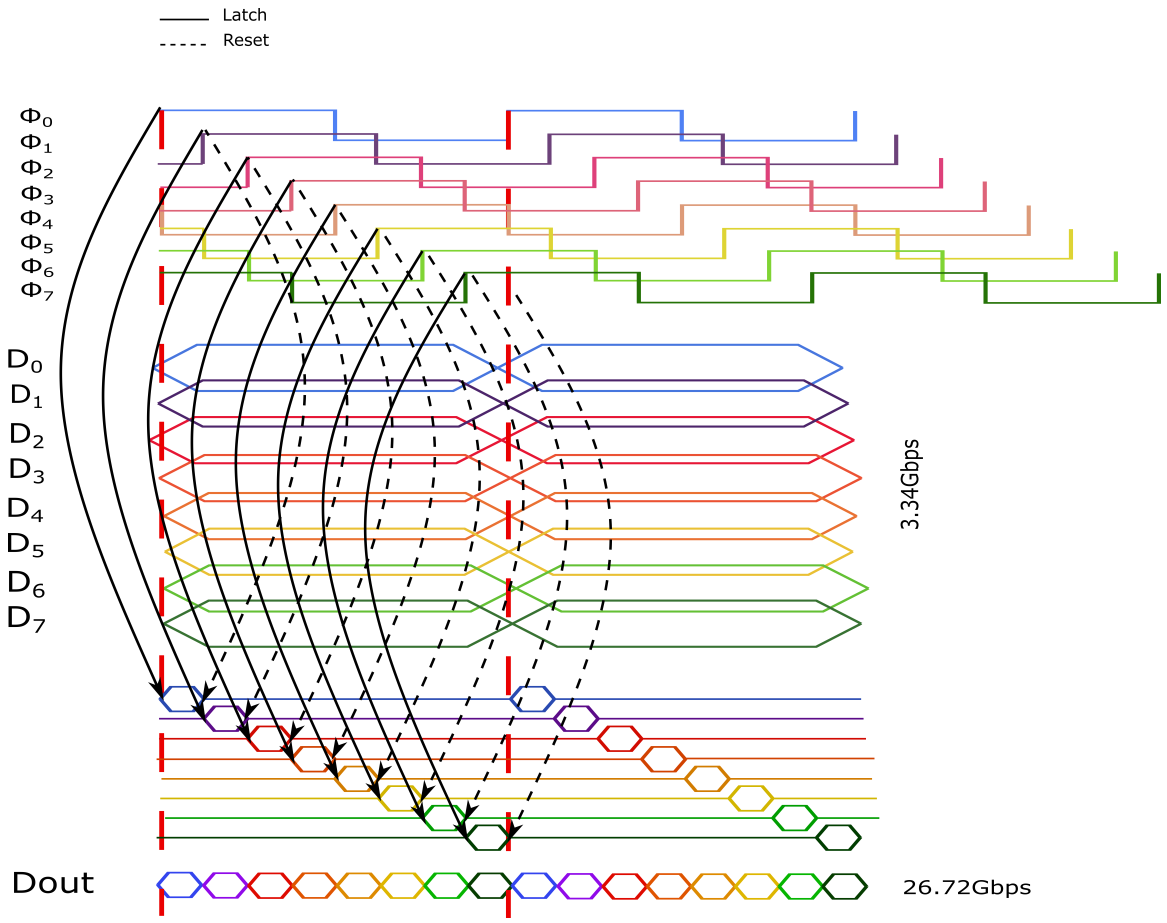

Figure 2.10: Proposed multi-phase serializer timing diagram

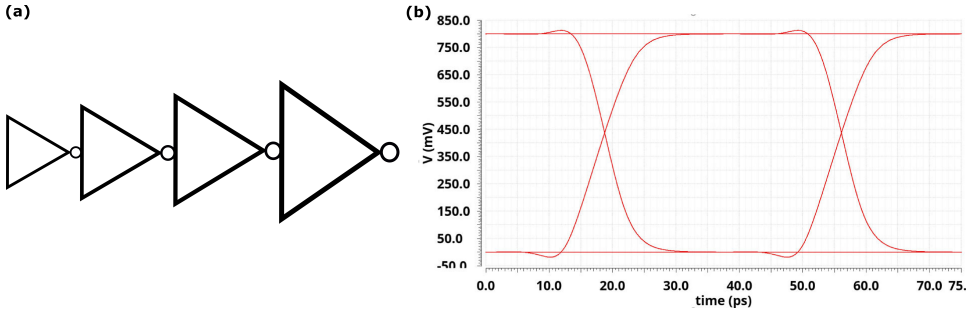

Figure 2.11: (a) Modulator driver schematic (b) Cadence spectre simulation result for driver output eye diagram

In Fig. 2.10, D_0-D_7 are serializer inputs which are PRBS signals with 45 degree phase differences provided by PRBS generator as also shown in Fig. 2.9. As it is illustrated, D_0 latches at Φ_0, then it resets at Φ_1 and again latches at Φ_4, and this goes on for the next inputs as shown in Fig. 2.10. Therefore, 26Gb/s data is generated with 3.34GHz clock, adding all 8 paths, D_{out} would be the 26Gb/s data stream.

2.5.4 Driver

Since the MRM electrical models are purely capacitive, we could benefit from using inverter based drivers which are the simplest, smallest and most power efficient architectures since they do not consume static power. However, the speed of the inverter is limited by the turn-on resistance of the devices. In our case, the 22nm CMOS devices' speed satisfies the speed requirements of the application. However, a multi stage inverter based driver is designed for the MRM capacitive load. The driver schematic with the simulated output eye diagram is shown in Fig. 2.11.

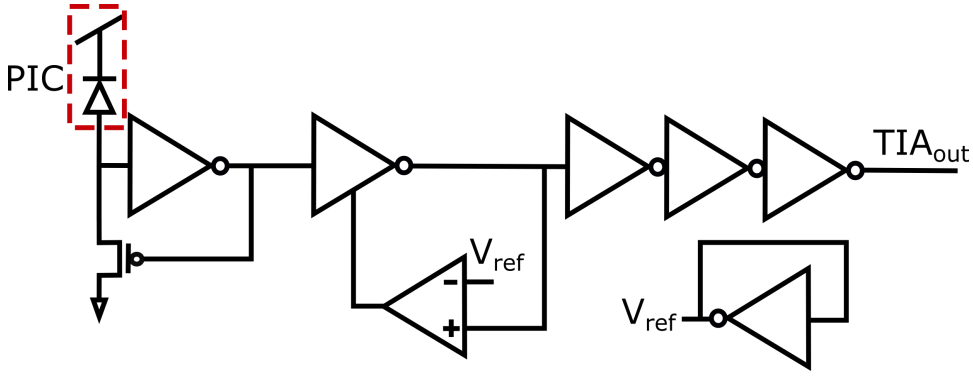

Figure 2.12: Proposed Transimpedance amplifier schematic

2.6 Receiver Design

This section describes the designed receiver system in detail. The receiver system is composed of TIA; to convert the received current to voltage, slicer; to align clock and data, and checker and Bit Error Rate (BER) calculation logic; to check the received signal for errors.

2.6.1 TIA

A Transimpedance Amplifier (TIA) is a gain stage which converts current to voltage. Sensitivity and link data rate demand the the TIA's required gain and 3-dB bandwidth. As illustrated in Fig. 2.12, Photodiode (PD) receives the signal and TIA converts the current sensed from the PD to voltage. This PD has a 10fF capacitance and 38μA peak to peak current. Accordingly, a low power high speed TIA is designed to convert this current to full swing voltage. For low power designs, an inverter-based TIA with resistive feedback has gained popularity due to their simple structure, ability to operate with low voltage supply, and good performance [28–30]. However, the speed would be limited to input capacitance and feedback resistance and there would be a trade-off between speed and output swing. On the other hand, there also exists an inverter gain limitation

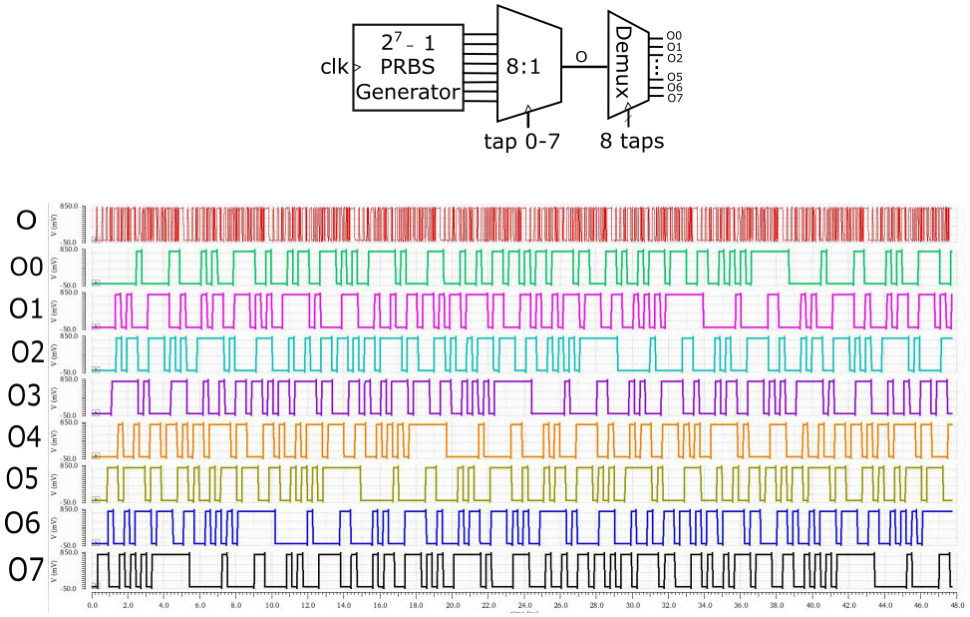

Figure 2.13: SERDES functionality

because of output resistance present due to resistive feedback. To solve these problems, a PMOS in feedback is used instead of a resistor. Therefore, we benefit from its low power and high bandwidth. However, the voltage at the output of inverter is still not large enough to be fed to an inverter to get full swing output. To solve this issue, we designed a feedback loop as shown in Fig. 2.12 to amplify the signal and control the threshold. The threshold can be changed with changing the V_{ref} which can be changed with back gate control of a unity feedback inverter. Then, the amplified signal with proper threshold is applied to few stages of inverters for achieving full swing signal. This low speed feedback also gives the added benefit of working across corners.

2.7 Deserializer

After converting the received current into full swing voltage through TIA, the lower speed signal has to be restored by the deserializers. Before discussing deserializers used

in this system it might be beneficial to first investigate SERDES operation. SERDES functionality is illustrated in Fig. 2.13 for a $(2^7 - 1)$ bit PRBS sequence. Using an 8:1 serializer with the proposed multi-phase structure discussed in section 2.5.3 the PRBS sequence O is generated at 8 times higher data rate. The deserializer (Demux) shown in the figure uses the 8 phases of the clock (tap0-7) to reconstruct the PRBS signals. In Fig. 2.13, O0-O7 signals show the reconstructed data streams. As it is illustrated each signal has 22.5 degree phase difference with its neighbor signal. This figure is simulated for illustration of the concept of serializing and deserializing. Deserialization structures are very similar to serializers but in a demultiplexing scheme. For example, [24] uses a tree structure with divided clocks to reconstruct the channels. In our system, since a multi-phase based structure was used with different phases of 3.3GHz clock, our deserializer is similar to the one shown in Fig. 2.13. This deserializer consists of 8 flip flops which each samples the high speed signal (26.7Gbps) provided by the TIA at one of the phases of the clock which will reconstruct the lower speed signal (3.3Gbps).

2.7.1 Slicer

After restoring the signals using deserializer (the 8 flip flops shown in Fig. 2.14 and Fig. 2.15), data needs to align with the clock. To do that, clock is sent along with the data going to the same delay as shown in Fig. 2.14 and Fig. 2.15. Therefore, clock and data are sent and received the same way. However, we have to know which data is being received and what is its corresponding clock. Thus, a clock and channel select architecture is designed to align the clock with the desired data as shown in Fig. 2.14 and Fig. 2.15.

To implement such architecture, two modes are defined. A test mode (see Fig. 2.14) and normal mode (see Fig. 2.15). In test mode, we select the correct clock. First, we

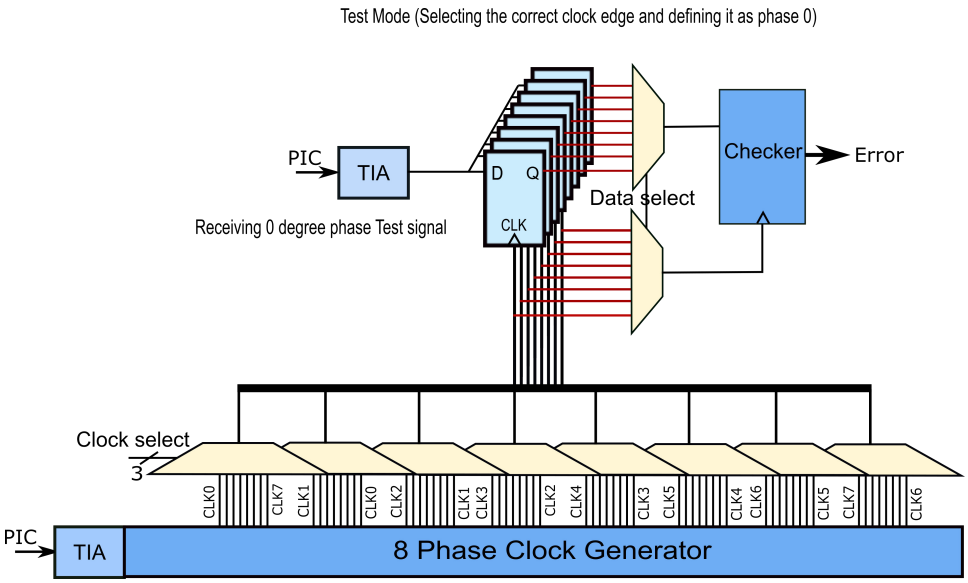

Figure 2.14: Slicer schematic at test mode

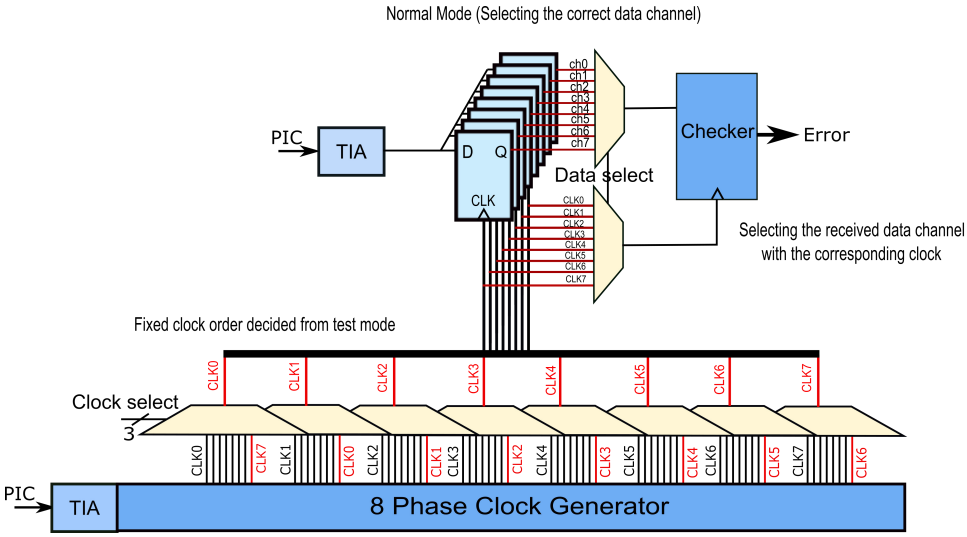

Figure 2.15: Slicer schematic at normal mode

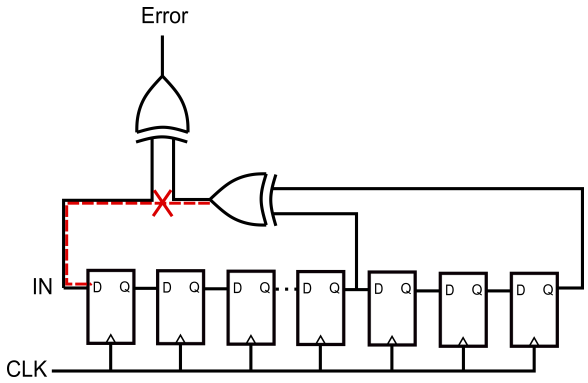

Figure 2.16: Conventional $2^{31}-1$ bit PRBS checker structure

send a test sequence using the PRBS generator with 0-degree phase difference, receive it through the TIA and at the same time we would receive the clock and select the clock phase order using the 3 bit clock select. Therefore, we redefine the clock order in test mode then we would switch off the PRBS in real life and operate in normal mode. However, here we would reuse the same PRBS generator and checker to test our system. In normal mode we would select the desired channel and the corresponding clock will be selected automatically (since the select pins of data multiplexer and checker clock multiplexer are tied together) and will check its errors with its corresponding clock.

2.7.2 PRBS Checker

As discussed earlier, the received signal needs to be compared to the transmitted signal to find out the number of errors in the the transmitted signal. Since, the transmitted signal is a $2^{31}-1$ PRBS signal, the signal can be checked for errors with a $2^{31}-1$ PRBS checker which has the same structure as a PRBS generator that its loop has been opened in the feedback and an XOR is applied between opened points as shown Fig. 2.16 and it checks for errors. Therefore, once the data has filled the pipe, the input and feedback output should be the same signals so ideally there would be no error unless the PRBS

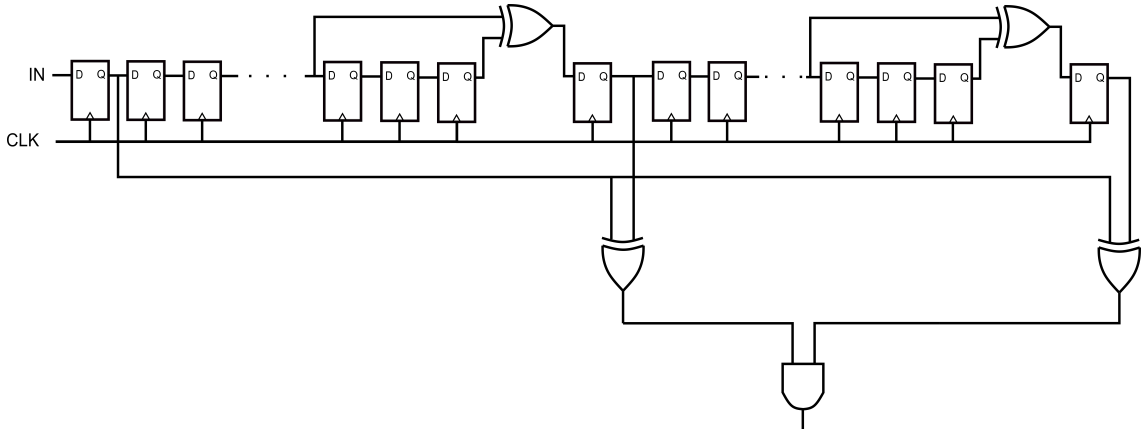

Figure 2.17: Modified $2^{31} - 1$ bit PRBS checker structure based on [23]

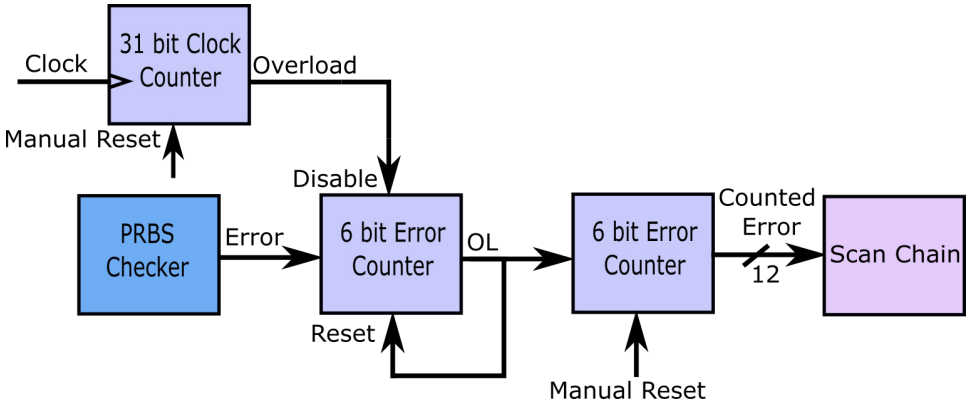

Figure 2.18: BER calculation logic

sequence has some errors from the channel. The problem with Fig. 2.16 is that as shown in calculations in Appendix A, if one error exists in the input, more than 1 error might appear at the checker output by mistake. To address this problem and guarantee that the checker shows only the errors that really exist, the checker structure shown in Fig. 2.17 is used [23]. The penalty from this structure is more flip flops used leading to more power and area consumption.

After finding the errors in checker, checker's output is further analyzed to find the BER. As shown in Fig. 2.18, a count system is designed to count the number of errors

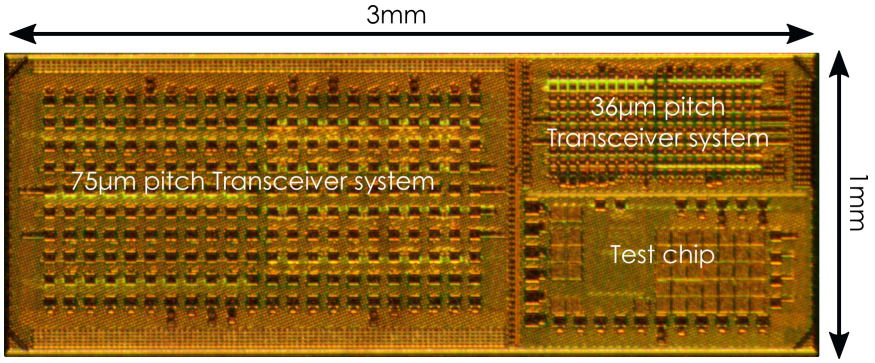

Figure 2.19: Chip micrograph.

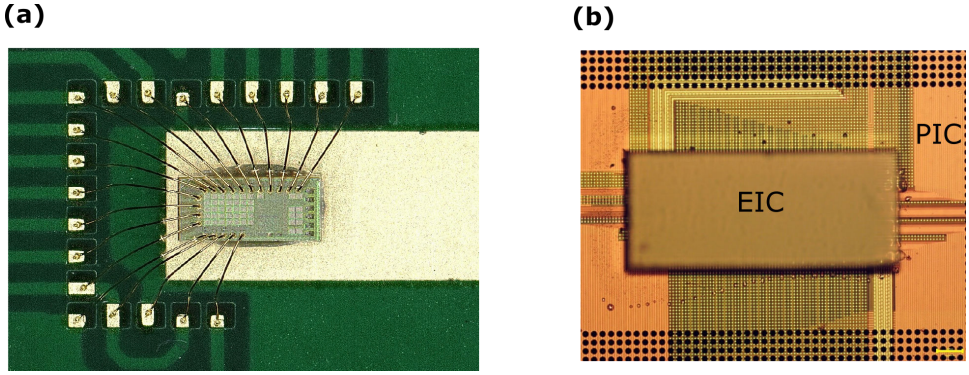

Figure 2.20: (a)Wire-bonded chip to PCB. (b) Flip-chipped EIC on PIC

from the checker. This system uses a 31 bit clock counter designed on chip and a 6 bit counter which counts the errors from the PRBS checker; whenever 31 bit counter overloads, the 6 bit counter stops counting and the bits will be read through a scan chain which is designed on chip. If the 6 bit counter overloads, it will reset itself and the next 6 bit counter counts the number of overloads and at last to reset everything we can manually reset both blocks.

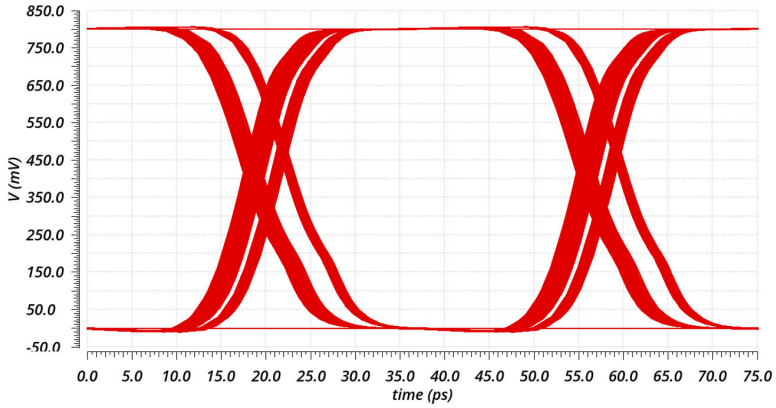

Figure 2.21: Cadence spectre simulation result for TIA output eye diagram

2.8 Chip Packaging

Fig. 2.19, shows the fabricated chip micrograph in 22nm FDX. The chip consists of one 75μm pitch chip, one 36μm pitch chip including the whole system and one test chip including only one channel of the transmitter. The 75μm pitch chip and 36μm pitch chip are flip-chipped to the Photonic IC (PIC) and test chip is wire bonded to a PCB for testing, as shown in Fig. 2.20.

2.9 Simulation Results

The Transceiver chip discussed so far is simulated in Cadence. Simulation results are reported in this section. As shown previously, Fig. 2.11 shows the modulator driver output eye diagram. This driver consumes 17.15fJ/bit, its output is full swing (0.8vp-p) and it has a back gate control to change the threshold if necessary.

Fig. 2.21 illustrates cadence spectre simulation result for the TIA output eye diagram. A 4.5 ps jitter in 38ps period can be seen from the eye diagram which is coming from the low speed feedback path. The threshold of the eye is controllable using the back-gate control.

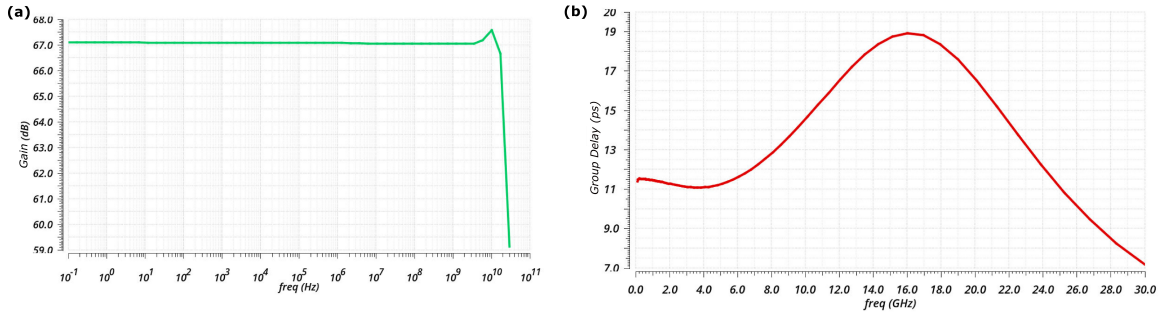

Figure 2.22: Cadence spectre simulation result for (a) TIA gain vs frequency (b) TIA group delay vs frequency

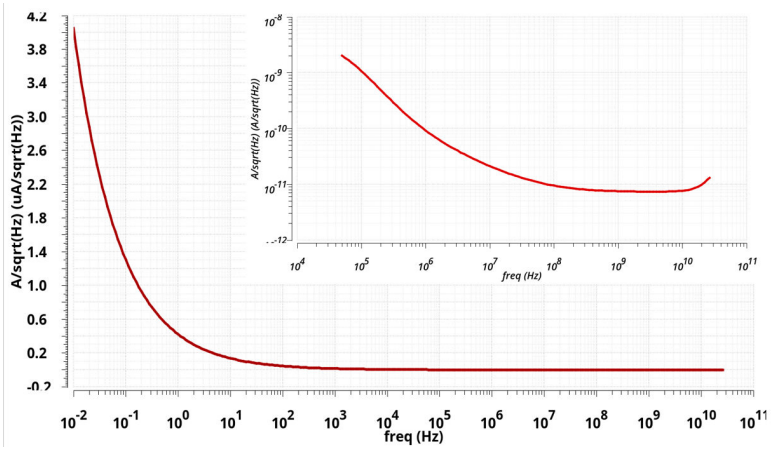

Figure 2.23: Cadence spectre simulation result for TIA input referred noise vs frequency

Further simulations on TIA are shown in Fig. 2.22. Fig. 2.22(a) shows a 67dB-Ω gain at $\sim$ 30GHz bandwidth and Fig. 2.22(b) shows a group delay of $14.5 \pm 4.5ps$. Therefore, the group delay is $\pm 12\%$ of bit rate over 26.8GHz bandwidth. Another important feature in TIA design is the input referred noise. As shown in Fig. 2.23, the input referred noise is $\sim 13.125 \frac{pA}{\sqrt{Hz}}$ which translates to 10.75 μA minimum detectable signal. As the input current from photodiode in this project is $\sim 38 \mu A$, this noise is low enough for detecting the desired signal.

The performance of transmitter and receiver is reported in Table 2.1 and Table 2.2. As it is shown, PRBS generator along with serializer and driver consume most of the

Table 2.1: Transmitter Power Consumption

Transmitter	Power (W)	Data Rate (Gbps)	Energy/bit (fJ/bit)
PRBS	2.2m	4×26.8	20.5
Driver	459.7μ	26.8	17.1
PLL	4.2m	40×26.8	3.9
IL	1.8m	(40/3)×26.8	5.1

Table 2.2: Receiver Power Consumption

Receiver	Power (W)	Data Rate (Gbps)	Energy/bit (fJ/bit)
Checker	1.7m	4×26.8	16.3
TIA	252.8μ	26.8	9.4
PLL	4.2m	40×26.8	3.9
IL	1.8m	(40/3)×26.8	5.1

power in transmit side and TIA and checker along with deserializer consume most of the power in receive side. The total transceiver energy efficiency is calculated to be less than 90fJ/bit. However, in real life the PRBS generator and checker are not going to be

present in the system since they are for test reasons only. Therefore, taking out their share of power consumption from calculations, the dominant blocks consuming power in the transceiver are modulator Driver and TIA. Therefore, the system designed is ultra low power operating at 1Tb/s.

2.10 Conclusion and future directions

In conclusion, a $1 \times 2\ mm^2$ and $0.6 \times 1\ mm^2$ 1Tbps transceiver system was designed and implemented in 22nm FDSOI technology. Novel system and circuit structures were designed to reduce power and optimize area while maintaining a high performance. The simulation results are reported. Work and testing is ongoing in our lab to verify operation of the transceiver.

Chapter 3

Electro-Optic and Thermally Tuned Systems

3.1 MRM Control Systems

As discussed, MRMs are the main elements in an WDM link. However, they suffer from sensitivity to temperature and process variations. Due to this sensitivity, their resonance wavelength shifts from their desired wavelength. There are many methods for tuning MRMs which among them the most popular are Electro-Optic (EO) and Thermo-Optic (TO) tunings. In EO tuning, the refractive index changes with injection or removal of charge carriers. In TO tuning, the refractive index changes with temperature. Therefore, usually control systems are designed to avoid the wavelength from deviating from its desired value. Control systems are usually either closed loop or open loop. In this chapter, closed and open loop thermal tuning and both EO and TO tuning for closed loop control systems will be discussed.

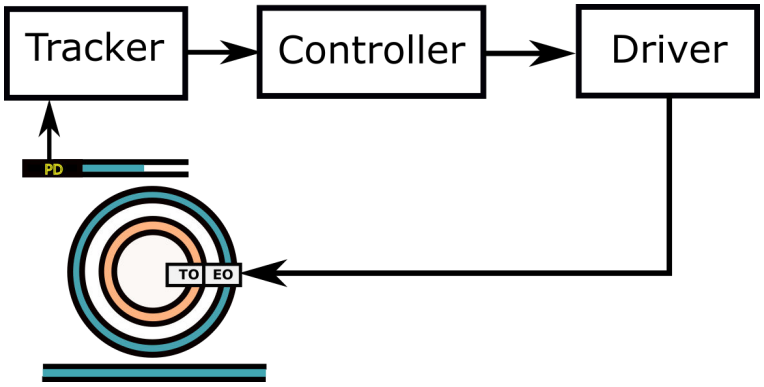

Figure 3.1: Closed loop MRM wavelength locking control block diagram

3.2 Closed loop approach

Fig. 3.1 shows the basic closed loop microring resonator tuning system. It mainly consists of a photocurrent tracker circuit, controller and driver. The microring resonator and an integrated heater is shown in Fig. 3.1. A weakly coupled waveguide terminated by a photodiode monitors the current. The system uses the integrated heater to change the microring's temperature which changes the the wavelength through thermo optic effect. The wavelength tuning can also be done by carrier injection or carrier depletion. In this dissertation, both TO and EO tunings are analyzed.

3.2.1 Photocurrent Trackers

There are many techniques to track the wavelength changes through the weakly coupled photodiode current. Averaging is one of the common techniques [31–33] which can average the current up to heater's time constant and sends the value to the controller. To do so, usually a transimpedance amplifier (TIA) is used to amplify the input and convert it to voltage for further processing through the controller. Another approach is implementing a peak detector after the TIA [34] to report when the drop port is locked to the input wavelength. Another technique implements a local receiver and converts

the photocurrent to digital values (0s and 1s). Then, it compares it to the data stream driving the modulator and outputs Bit-Error-Rate (BER), which dictates the direction of next change to the heater driver [35]. Other approaches [36], recognize the direction by separating 1s and 0s path and operating as a level detector. Another approach proposes a bit-statistical tracker which integrates the photocurrent and converts the voltage to digital to report the direction of change to the controller [37].

3.2.2 Controller

The controller receives a value from the tracker and makes a decision for the driver to apply the change to the heater. lock-to-reference controller is one of the approaches which compares the value from the tracker to a reference [31–33,35] if the value is higher, it outputs a decrease and if it is lower, it outputs an increase. Lock-to-maximum is an alternative approach which controller tries to maximize the tracker value. Therefore, it doesn't require a reference value since it always tries to lock to the maximum value. Alternatively, [38,39] multiplies the TIA output by the thermal dithering signal to stabilize the microring resonator.

3.2.3 Driver

Once the controller decides the direction, it increments or decrements the bits going to a Digital-to-Analog Converter (DAC) to convert the value to analog and the value is applied to a driver which drives the ring. There are two general forms of drivers, current driver and voltage driver. Current drivers are usually used for TO tuning since the heaters are resistors and the goal is changing the heater current and voltage driver are used for EO drivers since the goal is to change the voltage across the diode for carrier depletion.

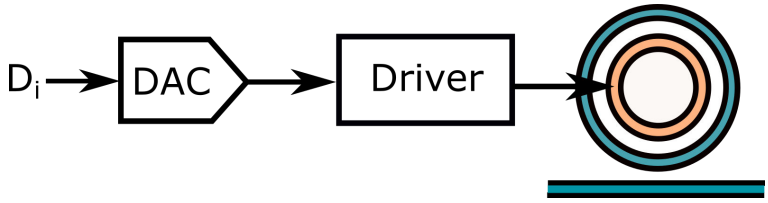

Figure 3.2: Open loop MRM wavelength locking control block diagram

TO Tuning

The DAC converting the bits to analog is usually a $\Delta\Sigma$ DAC which outputs a 1 bit stream of Pulse Width Modulated (PWM) signal and needs a lowpass filter to convert it to analog. Heater drivers usually rely on the slow response of heaters to be used as a low pass filter. The driver is usually an NMOS or PMOS which switches off and on with the PWM signal and gets averaged out with the heater. Therefore, the current flowing through the heater changes based on the change on the bits.

EO Tuning

For EO drivers the same $\Delta\Sigma$ DAC or higher resultion DAC with a different architecture can also be used. Since the EO driver is a voltage driver, it can simply be an inverter. If the DAC has a $\Delta\Sigma$ structure, the capacitance of the modulator can act as a low pass filter, if additional filtering is required, more capacitance or resistance can be added on chip.

3.3 Open loop approach

Open loop approach is based on choosing the desired value from a look-up table as shown in Fig. 3.2, through a Digital-to-Analog Converter (DAC) driving the MRMs, converting the digital value to analog. [40] uses an open loop structure for thermal tuning

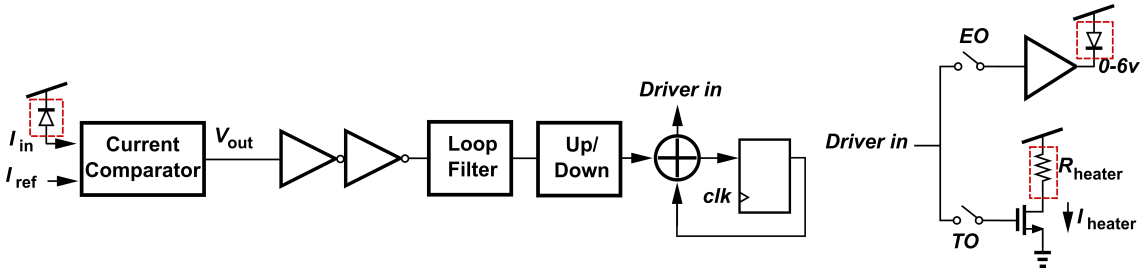

Figure 3.3: Closed loop MRM wavelength locking control system

of the MRMs. Open loop structure basically is the same as the Driver part of a closed loop system discussed in section 3.2.3 which gets its input from a look up table to tune the wavelength.

3.4 Proposed System

In this section two closed loop approaches are proposed and implemented in TSMC 65nm process.

3.4.1 Current Comparator based Control system

As discussed in section 3.2, conventional structures are composed of tracker, controller and driver. In this dissertation, we propose a control loop which combines the tracker and controller. Conventionally, the tracker converts the photodiode current and reports it to controller to compare it with a set point [41] either in analog domain or digital domain. In analog domain it requires a current set point at TIA input which then reports the difference. In digital domain, it converts it to digital first and then compares it with digital representation of the set point. In our structure the photocurrent is compared with a reference current directly using a current comparator and outputs 0s and 1s according to the value being higher or lower than the set point which saves area and

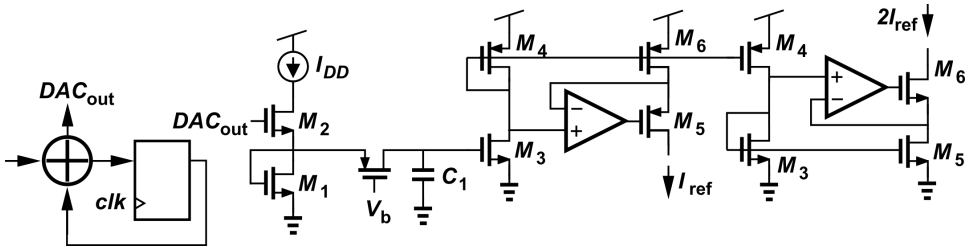

Figure 3.4: Refeference current generation circuit

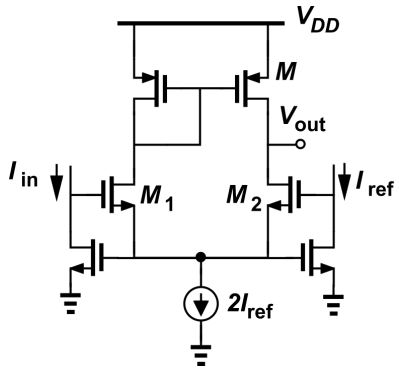

Figure 3.5: Current comparator circuit

power while maintaining a high resolution. The proposed system is illustrated in Fig. 3.3 which is designed for both TO and EO tuning of the rings.

As shown in Fig. 3.3, current comparator compares the photocurrent with a reference current which is set using an 8 bit $\Delta\Sigma$ based current DAC with structure shown in Fig. 3.4. The output of current comparator is a digital value which decides the direction of change that has to made to the ring. A low pass loop filter is designed for the loop stability and an up/down counter and Delta-Sigma DAC which implements an increase or decrease when driving the heater or microring resonator based on the comparison done through the current comparator in the front-end, to keep the current read from the PD close to the reference current. To select TO or EO tuning, a select pin is employed to select one path while deselecting the other.

Current comparator circuit is shown in Fig. 3.5. If I_{in} is greater than I_{ref}, the path

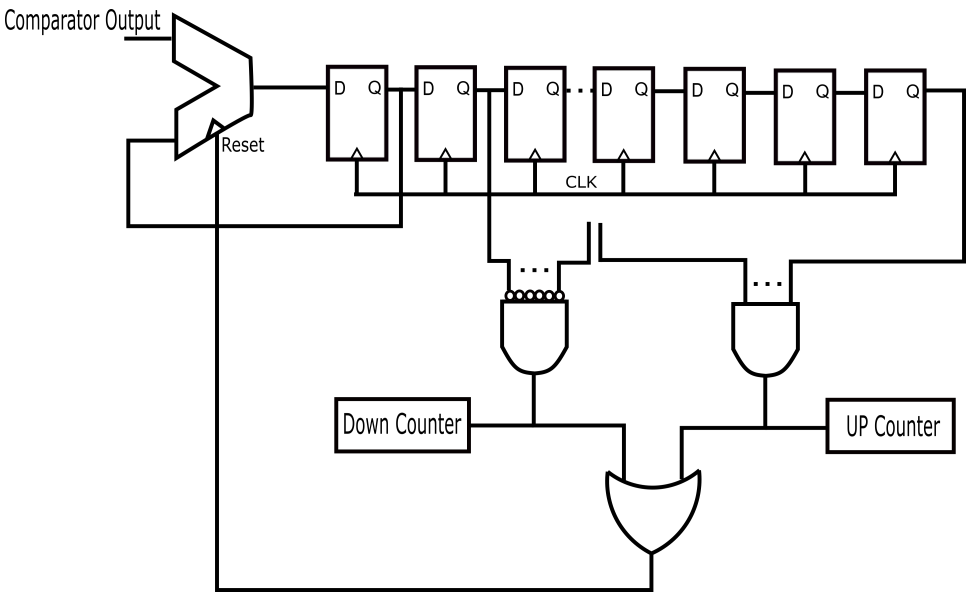

Figure 3.6: Digital low pass filter schematic

through the mirror would be on pulling V_{out} up to V_{DD}. If I_{in} is less than I_{ref}, the mirror path would be disabled and V_{out} would be pulled down to ground.

The reference current for current comparator is set digitally with an 8-bit Delta Sigma DAC which switches a current source on and off with its 1-bit output stream. Then it averages out through an RC filter which biases a current source and using current mirrors, I_{ref} and $2I_{ref}$ are generated as shown in Fig. 3.4.

Fig. 3.6, shows the digital low pass filter designed in the system to stabilize the loop. The accumulator adds its input (comparator output) to the delayed version of its output which applies a low pass filter to the comparator output. The value is then stored in shift registers and once all show 1s up counter would increment and once it shows all 0s down counter would decrement. When either one is counting 1 the accumulator will reset. Since the number of shift registers are constant in this implementation, the stability of the loop is controllable with changing the clock. Therefore, a clock divider is designed which is controlled digitally.

As shown in Fig. 3.3, the up/down counter output which is 8 bits, applies the 8 bit to the $\Delta\Sigma$ DAC input which it generates a bit-stream accordingly. If the TO tuning is selected, the bit-stream switches the NMOS off and on and gets averaged out with the heater which changes the heater current accordingly. In this dissertation, the maximum heater current needed was 1.3mA with heater resistance being 750Ω, a simple NMOS could be used as the driver. When gate of NMOS is at 1, for achieving 1.3mA at 750Ω, supply should be at $\sim$1.2v which is the nominal voltage in TSMC 65nm. When gate of NMOS is at 0, the drain of NMOS would sit at the supply voltage which is tolerable by the devices. However, since EO tuning requires 6v swing, using a simple inverter for EO driver is not suitable for this work in TSMC 65nm process. Therefore, a new high voltage EO driver is proposed which enables low voltage CMOS processes to drive higher voltages.

3.4.2 High Voltage EO tuning

Fig. 3.7 shows the proposed EO driver. Since the output of the $\Delta\Sigma$ DAC is 0-1.2v, a comparator with 3.3v devices is designed to compare the value with 0.6v and therefore amplifying the signal to 0-3v which follows a 3v inverter. As shown in Fig. 3.7, a level shifter is designed to shift the 0-3v signal to 3-6v which is applied to the gate of a PMOS in output driver with 6v supply voltage and since NMOS devices cannot tolerate 6v in this process a resistor is used instead. Therefore, the output swing is 0-6v. The bias voltages are applied using diode connected transistors as shown and also a feedback is designed to bias the NMOS pair in the level shifter comparing it with a reference voltage. All these techniques of biasing avoids the 3.3v transistors to break operating with a 6v supply.

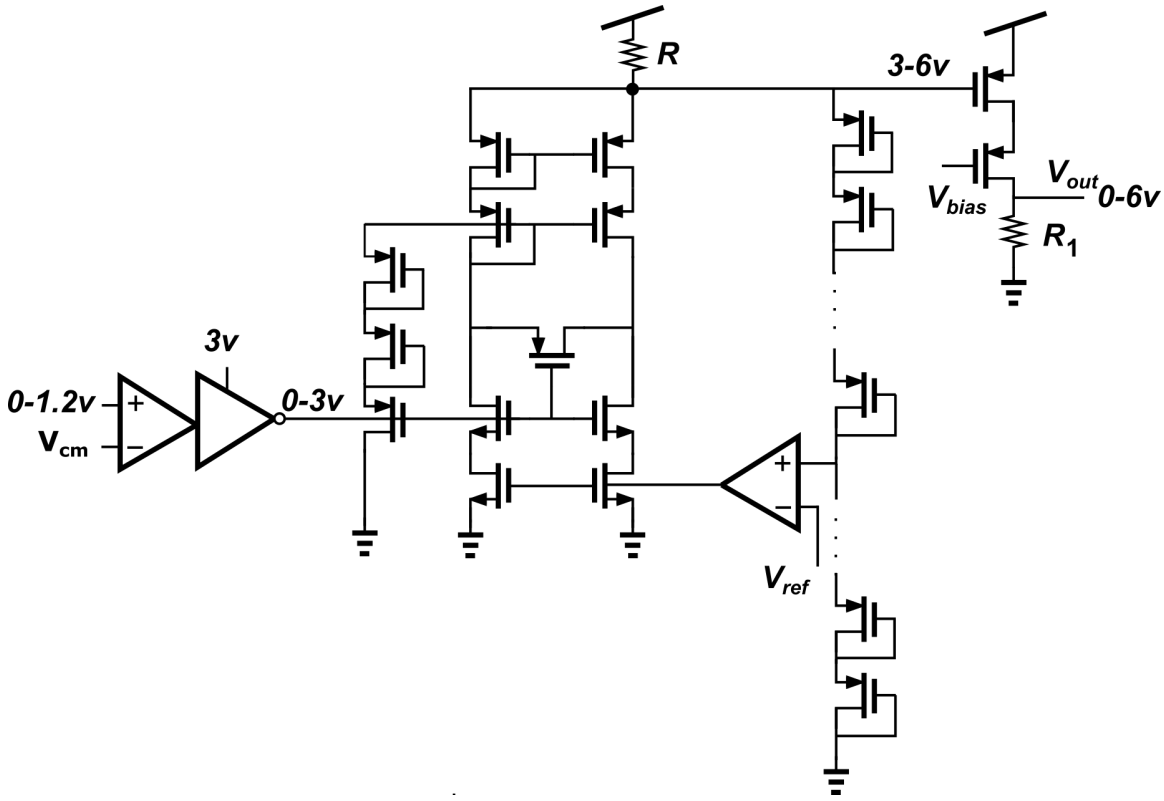

Figure 3.7: High voltage EO driver

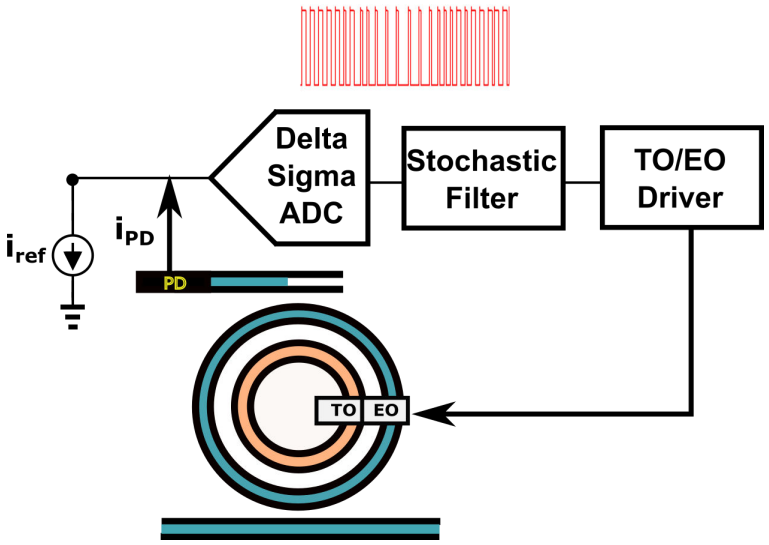

Figure 3.8: Stochastic-based control block diagram

3.4.3 Stochastic-Based Control system

Previously, we discussed the possibility of using a current comparator as the front-end. In this section, we propose a continuous-time $\Delta\Sigma$ ADC as the front-end. The photocurrent gets subtracted from the reference current at the input and $\Delta\Sigma$ ADC converts the difference to digital. The $\Delta\Sigma$ ADC's feedback DAC current operates as an inherent reference current for the input current difference and can be tunable. In this work, DAC current is designed to be 3μA. Since the output of $\Delta\Sigma$ ADC is a 1 bit stream, previous filter shown in Fig. 3.6 cannot be used without extracting the bits. Therefore, a stochastic filter is designed as a low pass filter for the $\Delta\Sigma$ bit-stream to stabilize the loop which can be directly applied to the EO or TO drivers without any additional logic blocks. Therefore, the need for a Delta-Sigma DAC is removed since the required changes are applied directly to the data stream which gets averaged out through the ring and changes the current or voltage accordingly. If the current difference is small, the average of the bit-stream would be close to zero which then the loop would be locked to the reference. If the difference is large, the driver would apply the average

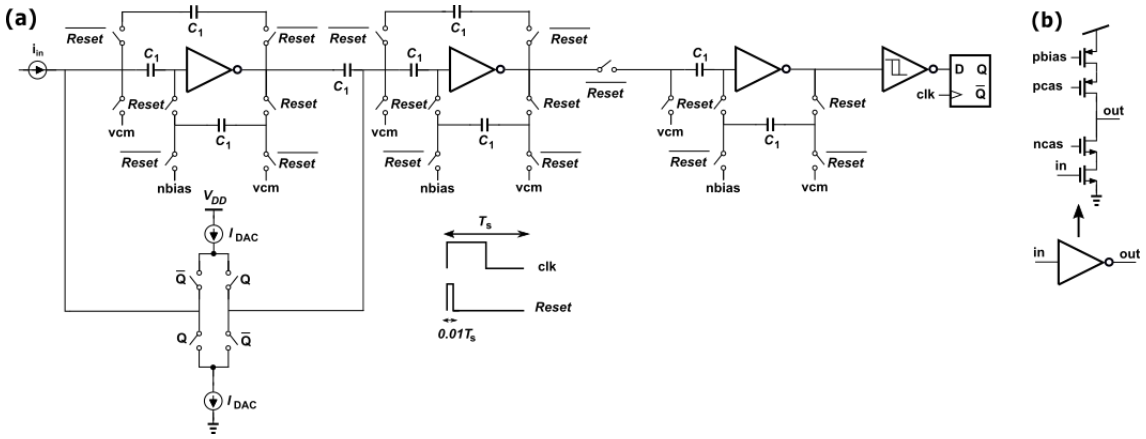

Figure 3.9: $\Delta\Sigma$ ADC used as the stochastic-based control sytem front-end

of the bit-stream to the ring and changes the current until the difference becomes small. The benefit from both this structure and current comparator based structure is that if the photocurrent is out of range ($> 3\mu A$), the output of the ADC would be saturated and will apply the maximum or minimum voltage or current to the ring until it gets into the range. Therefore, it would benefit from course and fine searches to lock to the set point faster. Fig. 3.8 shows the loop structure and Fig. 3.9 shows the $\Delta\Sigma$ ADC structure. As shown in Fig. 3.9, the ADC is a 2^{nd} order $\Delta\Sigma$ ADC with current DAC feedback designing to be 3μA. This structure is ultra compact and area efficient due to designing of a compact one stage cascode amplifier with 40dB gain which enhances to 80dB gain thanks to Correlated-Double-Sampling (CDS) technique. The comparator is also inverter based which makes the whole design area and power efficient. The details of integrator, amplifier and current DAC source designs are discussed in Chapter 6.

3.5 Measurement Results

In this section results from a PCB level open loop control and chip level closed loop control system with the structures discussed throughout the chapter are reported. Both

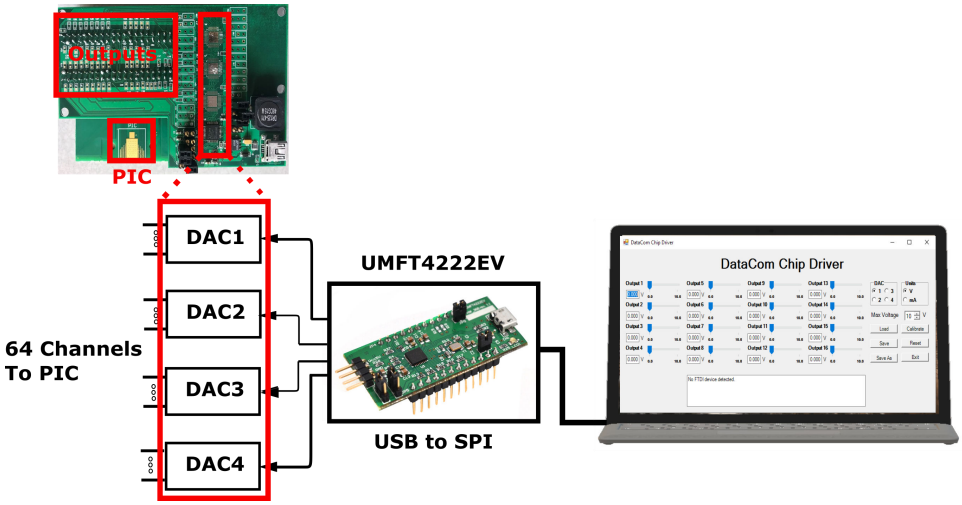

Figure 3.10: Open loop heater driver measurement setup

systems are tested with microring resonators.

3.5.1 Open loop approach

Fig. 3.10 shows diagram of a 64 channel open loop TO tuning system that was designed on PCB [20]. The heater driver was designed to control 64 heaters configured as four banks, each bank of 16 was driven by an off-the-shelf 16-channel DAC. A USB to Serial-Peripheral-Interface (SPI) converter IC (FT4222) was used for controlling the DACs. DAC outputs were connected to photonic IC via a 64-wide cable. Individual control of the DACs was achieved by configuration words sent to the DACs via the SPI. Since 4 separate ICs were used the FT4222 served as the master while the DACs were configured as slaves. A Graphical-User-Interface (GUI) was designed in Visual Basic to allow programmability and ease of use.

Since the ring heaters require a 10V drive and a current drive of 2mA, the LTC2668 4-channel 12-bit DAC was chosen. The 12-bit DAC yields a 2.44mV LSB step, which is more than adequate for the wavelength control required by the PIC. An additional

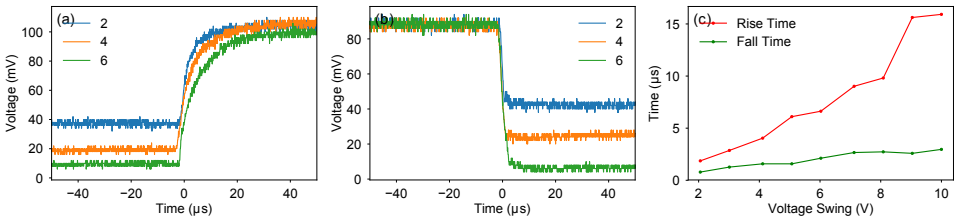

Figure 3.11: (a) rise time for three different voltage swing, (b) fall time for three different voltage swing and (c) rise time, and fall time vs voltage swing. Reprinted with permission from [20] ©The Optical Society.

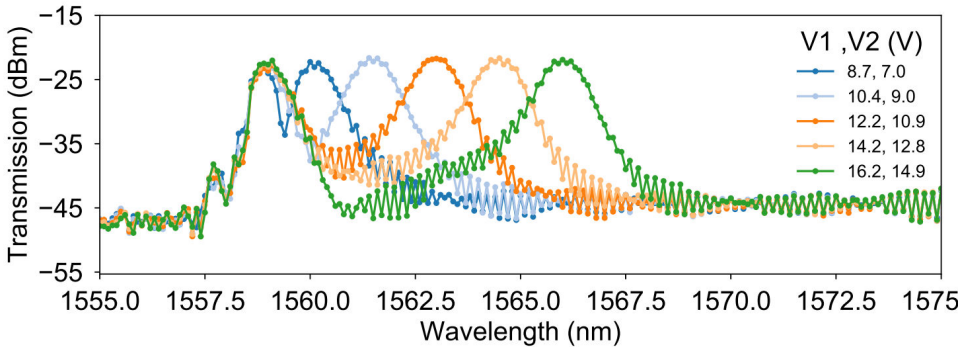

Figure 3.12: Tuning curve of a micro-ring resonator in a unit cell. Reprinted with permission from [20] ©The Optical Society.

consideration for the DAC was the bandwidth. Accurate switching characterization of the heater necessitates the DAC's bandwidth be at least an order of magnitude faster than the time constant of the heater. The DAC settling time was 8 μs , yielding a rise time of about 1.5 μs, adequate for measuring the PIC heater which has a 15.92 μs rise time. Careful design of the PCB, including separating the analog and digital signals and ground planes, ensured low coupling noise due to the electronic switching. Heater time constant was measured by using a photodetector (xpdv2120R) while stepping the heater driver. In the case of the double ring switching element, one ring is fixed at 10V or 0V (rise versus fall times) while the other ring was stepped via the heater driver. This procedure was repeated for different voltage differences and the switching time was recorded as shown in Fig. 3.11. The tuning curve of a double ring resonator is also shown

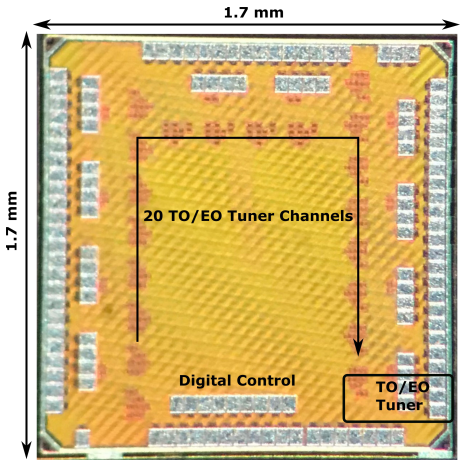

Figure 3.13: EO/TO tuner chip micrograph

in Fig. 3.12 for different voltages applied to each ring using the driver.

3.5.2 Closed loop approach

The proposed current comparator based closed loop EO/TO tuner is implemented in TSMC 65nm. The chip micrograph is shown in Fig. 3.13. As it is shown, 20 TO/EO drivers are implemented in 1.7mm×1.7mm area with SPI control to control the digital values. The active area consumed by the circuits is $\sim 0.024 mm^2$.

The measurement setup is shown in Fig. 3.14. The system clock is provided by signal generator and it is set to 8MHz for the results reported and since the MRM time constant is $< 100\mu s$, the $\Delta\Sigma$ DAC has an Oversampling Ratio (OSR) of <400. The clock frequency can be increased in order to increase OSR. The clocks of the DACs and low pass filter are tied on chip. However, a 4 bit divide ratio is designed for the filter which can be controlled digitally. For digital control , Digilent ZedBoard Zynq-7000 FPGA is used. The FPGA is programmed and as shown in Fig. 3.14, the digital signals are controlled by a GUI designed in visual studio for ease of use. The chip shown in Fig. 3.13 is packaged and soldered on a PCB and PD and heater connections are via header connectors.

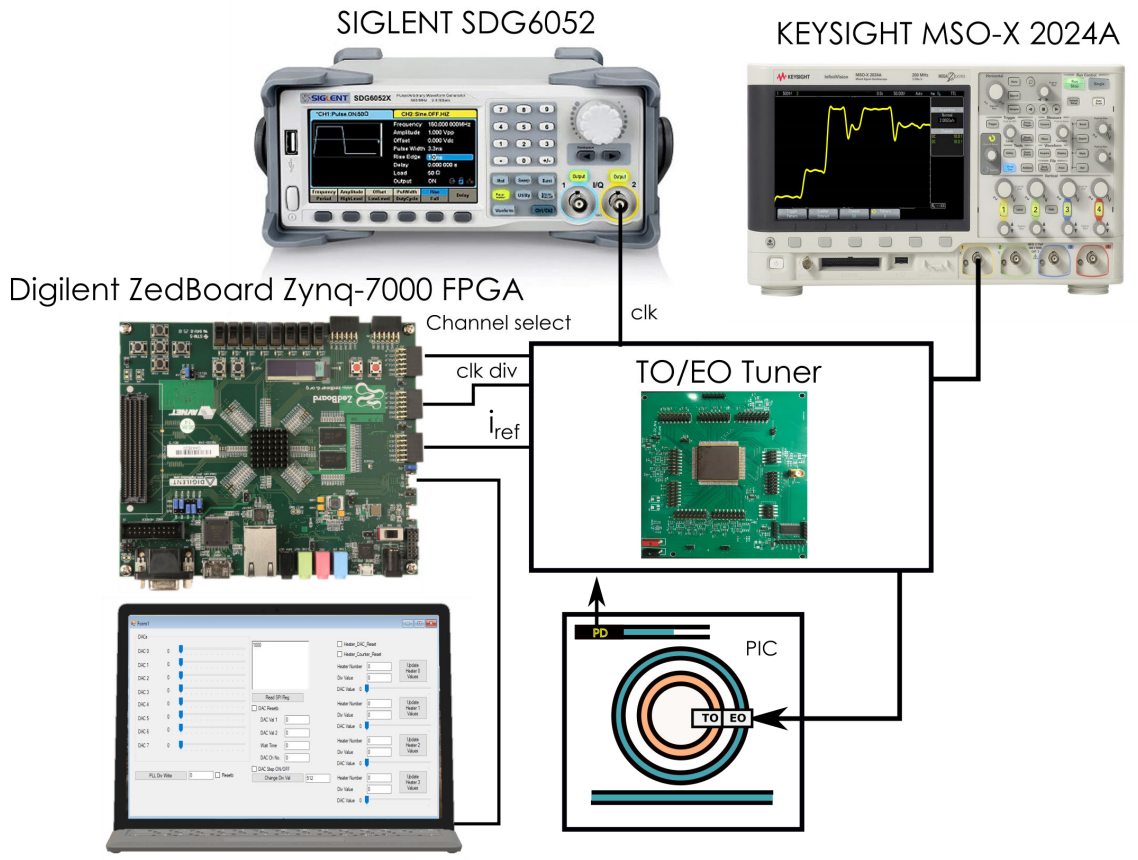

Figure 3.14: Closed loop MRM wavelength locking measurement setup

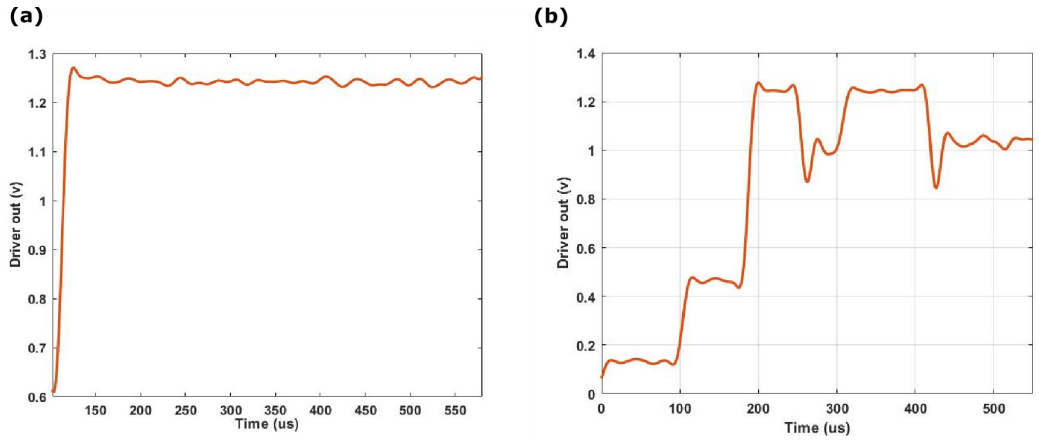

Figure 3.15: Changes in heater output voltage varying the set point from (a) 1.5μA to 3μA (b) 0 to 3μA with different steps

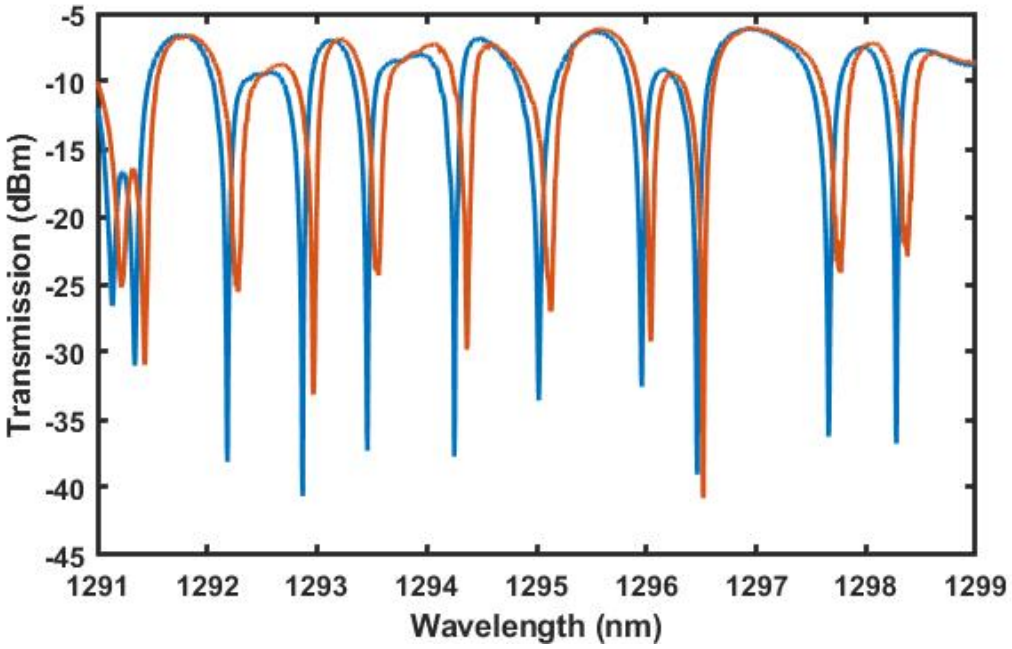

Figure 3.16: Tuning curve of a 11 micro-ring resonators on resonance and tuned with different set reference currents (red and blue traces).

Fig. 3.15 show the transient response of the heater to input current reference changes. Fig. 3.15(a) demonstrates the voltage applied to the heater when the reference current is changed from 1.5μA to 3μA using the 8bit current DAC and the time it takes to lock. It is controlled with an FPGA programming and a GUI which is designed to change the reference current value and divide ratio of the filter. Fig. 3.15(b) shows the heater voltage when the reference current is being changed for several set points and it shows wavelength locking after each change. As it is illustrated in the test results, the locking time is about 25μs. Fig. 3.16 shows the tuning curve of 11 micro ring resonators on and off resonance with different set reference currents using 11 channels of the 20 channel control chip.

The stochastic-based control loop is also implemented TSMC 65nm. The chip layout is shown in Fig. 3.17. As it is shown the chip is $425\mu m \times 345\mu m$. However, the $\Delta\Sigma$ ADC

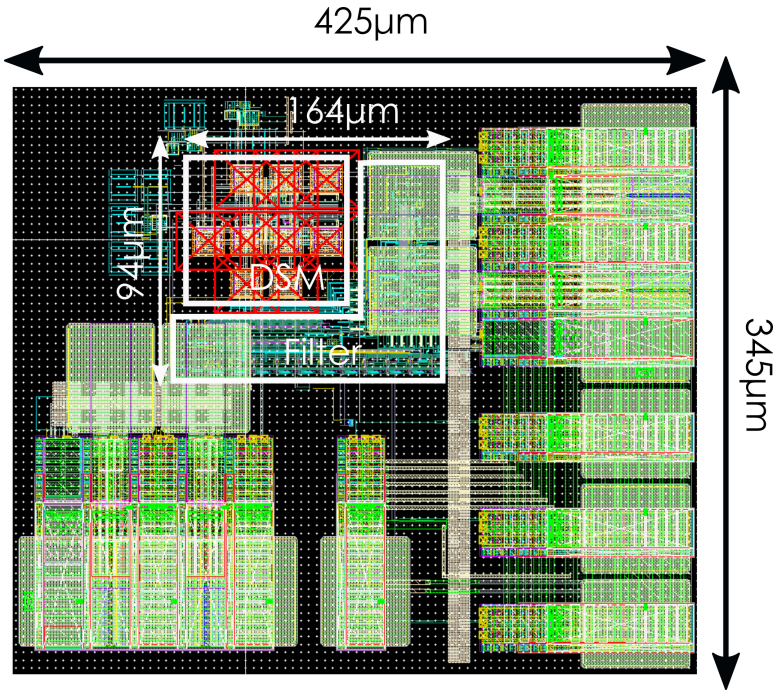

Figure 3.17: Stochastic-based system chip layout

and the stochastic filter in the loop only occupy $0.015mm^2$.

3.6 Conclusion and future directions

This chapter presented a comprehensive review of the control loop structures. It explains different approaches to tune and lock wavelength in MRMs. It proposes two different control loop structures and demonstrates an open loop structure measurement results from a discrete implementation and a $1.7mm \times 1.7mm$ integrated closed loop structure designed and implemented in TSMC 65nm and tested with MRMs implemented in PIC. The closed loop control chip was designed for power and area efficiency while maintaining high performance. Additional testing is being conducted in our lab to further verify operation of the control loops.

Part II

Energy-Efficient High-Performance CMOS VLSI Design for Biological Applications

Chapter 4

Current Sensing Approaches

4.1 Introduction

As the need for biosensors and point-of-care devices grow, there is an increasing need for ultra-low power area efficient analog front-end systems. Most biosensors utilize a current sensing modality and the front-end usually comprises of a transimpedance amplifier (TIA), followed by an analog-to-digital converter (ADC). While the detector plays a prominent role in the sensing, the processing system is critical in realizing the full potential of the sensor. For the nanopore sensor, some of the important specifications are dynamic range, bandwidth, power and area efficiency. Since each sensor and its respective application can have widely differing requirements for these metrics, the designer faces myriad choices in choosing the right interface electronics for a particular application. The goal of this chapter is two-fold: The first is to provide an overview of the existing approaches highlighting the advantages and disadvantages of each approach. The second is to provide some simple graphical methods to narrow down the topology for a particular application. The conceptual overview of the chapter is shown in Fig. 4.1. It is our hope this chapter will provide the novice researcher with the tools to get started and serve

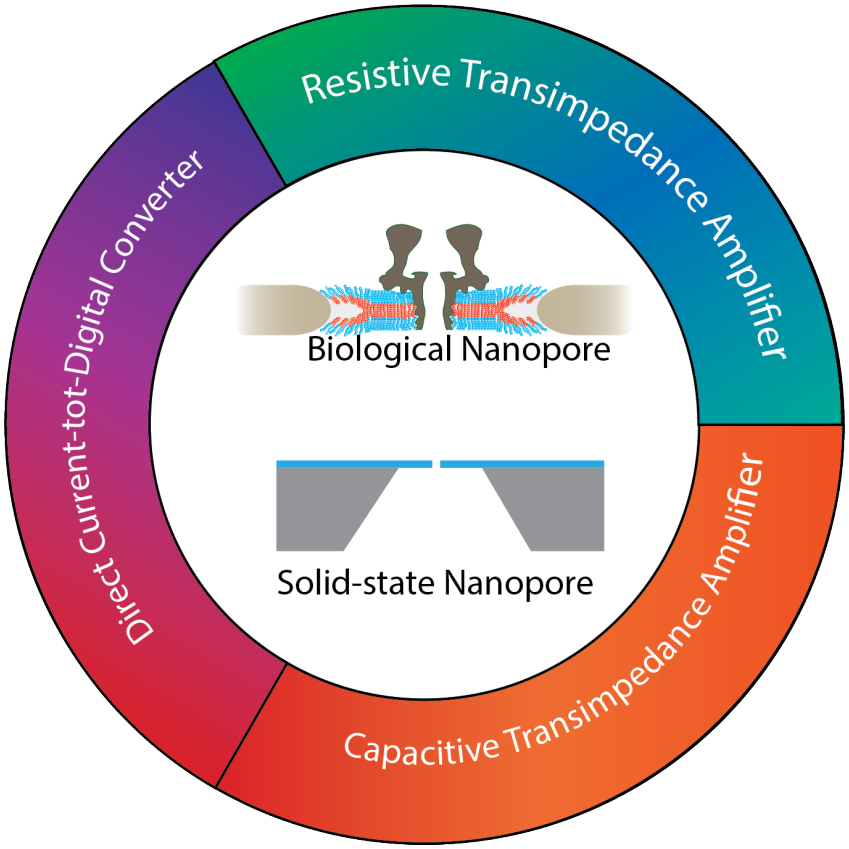

Figure 4.1: Conceptual overview of the chapter, illustrating the types of nanopore sensors considered and the various current sensing topologies reviewed in this chapter.

as a reference for the experienced designer. The chapter is organized as follows, we first review the intrinsic electrical parameters of nanopore sensors. Following this we discuss the various architectures and circuit topologies for current sensing used in nanopore sensors. We divide the approaches into two different sections one dealing with analog front-end circuits followed by an ADC and the second utilizing a direct current-to-digital approach. For each broad approach we illustrate the design methodology using a simple example. We then discuss the design challenges and solutions for nanopore sensor arrays and summarize the chapter.

4.2 Current-sensing Approaches

The forerunner to signal acquisition from the nanopore sensor was the characterization of biological ion channels using the patch-clamp technique. Many of the issues faced by nanopore sensor electronics are similar to those of the patch-clamp amplifier. Both systems operate using the potentiostat mode, where the voltage across the sensor is clamped while current through the sensor is monitored simultaneously. The clamping is usually facilitated by using an operational amplifier in feedback, providing a virtual ground. Virtual ground is the term used to describe the potential of the negative terminal which is maintained very close to the positive terminal due to the negative feedback used in such circuits. The positive terminal is usually (but not always) tied to the ground or a convenient reference potential and hence the terminology. Thus, the virtual ground provides a clamping action through feedback but does not sink current into the node, thereby allowing for the monitoring of current.

There are multiple approaches to designing the potentiostat with dynamic range, noise, and bandwidth being the main considerations. The current-to-voltage converters are generally termed Transimpedance amplifiers (TIAs). In the following section, we review the most common architectures used and also show a simple graphical design methodology.

4.2.1 Resistive Transimpedance Amplifier

The basic TIA structure for current-sensing is a resistive feedback TIA as shown in Fig. 4.2A. In Fig. 4.2A, R_f is feedback resistor and C_f is stray capacitance. The frequency domain output voltage of the TIA can be calculated as:

$$V_{out}(s) \cong -I_{sen}\frac{R_f}{1+sR_fC_f} \tag{4.1}$$

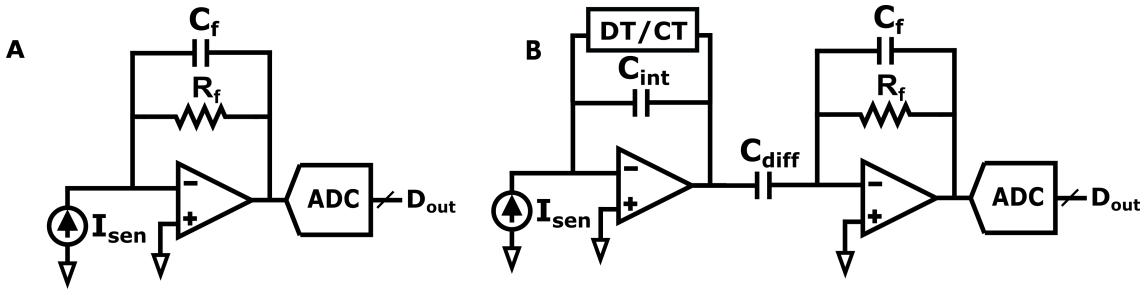

Figure 4.2: TIA based current sensing front-ends, (a) is resistive feedback TIA, (b) is capacitive feedback TIA.

In general, integrated circuit approaches use smaller resistor values since they occupy lesser area and also have a smaller stray capacitance. If the stray capacitance becomes negligible equation (4.1) simplifies to $V_{out} = -I_{sen}R_f$ (since $1 \gg sR_fC_f$). However, this precludes the sensing of small currents. For example, if the desired minimum detectable signal is 1nA, with a $1k\Omega$ feedback resistor, the output voltage would be equal to $1\mu V$ and will be swamped by the noise of the amplifier [42].

As a result most resistive TIA implementation use large resistors in the order of 0.01-$1G\Omega$. However, the parallel combination of the large resistor with the stray capacitance yields a low frequency pole limiting the bandwidth, and is given by:

$$f = \frac{1}{2\pi R_f C_f} \tag{4.2}$$

Therefore, there is a trade-off between minimum detectable signal and bandwidth in resistive TIAs. This bandwidth limitation can be partially mitigated using a Silicon-on-Insulator (SOI) process which introduces less parasitics when using large resistors [43]. The resistive TIA input referred noise is sum of shot noise (if BJT transistors are present

in the design), feedback resistor noise and opamp noise and given by [42]:

$$i_n^2 = 2qI_{in} + \frac{4kT}{R_f} + e_{n,op}^2(\frac{1}{R_f^2} + (2\pi f)2(C_f + C_{in})^2) \tag{4.3}$$

Where C_{in} is biosensor output capacitance and $e_{n,op}$ is opamp voltage noise power spectral desnity ($V/\sqrt{Hz}$) which for CMOS technology consists of flicker and thermal noise and is equal to:

$$e_{n,op}^2 = \frac{16kT}{g_m} + \frac{2K_F}{C_{OX}WL}\frac{1}{f} \tag{4.4}$$

where g_m is the trans-conductance, W and L are width and length of the MOS transistors, K_F is the flicker noise coefficient and C_{ox} is the oxide capacitance per unit area. Throughout the chapter, we use f_B and Δf interchangeably to denote the signal bandwidth since the signal acquisition is assumed to be from DC. For noise calculations we explicitly use Δf.

Improving the SNR requires minimizing the noise. In general though BJT devices provide less 1/f noise they are not readily available in most CMOS processes and hence are not widely used. Thus, the input shot noise contribution can be neglected from (4.3). On the other hand large area input MOS devices are required to minimize the 1/f noise contribution. However, this comes at the cost of increased input capacitance, which negatively affects the noise performance as shown in section 4.2.1. For the range of resistors under consideration the resistor noise contribution usually dominates and the minimum signal-to-noise ratio (SNR) is given by:

$$SNR_{min} = \frac{{I_{min}}^2 R_f}{4kT\Delta f} \tag{4.5}$$

I_{min} is the minimum detectable signal and assuming negligible stray capacitances, it is

defined as:

$$I_{min} = \frac{v_{out,min}}{R_f} \tag{4.6}$$

Therefore, (4.5) can be rewritten as:

$$SNR_{min} = \frac{{v_{out,min}}^2}{4kTR_f\Delta f} \tag{4.7}$$

If the noise is assumed to be Gaussian then the minimum SNR required is 5 to avoid any false positives. Therefore, the minimum output voltage is given by

$$v_{out,min} = \sqrt{20kTR_f\Delta f} \tag{4.8}$$

However, one must be careful in using the above equations since they were derived under the assumption of negligible stray capacitance. A simple constraint can be derived by ensuring that the required bandwidth f_B satisfies the following constraint:

$$\frac{1}{2\pi R_f C_f} \gg f_B \tag{4.9}$$

For example, practical on-chip stray capacitance is around 100 fF, which limits the feedback resistor to be $\ll 1.5G\Omega$ for a 1kHz signal bandwidth. Assuming an order of magnitude, the resistor values is limited to 150 MΩ yielding a minimum output voltage of 110μV requiring a very low noise amplifier design. Exact constraints of the amplifier noise performance can be derived from the input capacitance as shown in section 4.2.1

Effect of Input Capacitance

So far, the contribution of the opamp noise was considered to be negligible compared to other noise sources. However, this is only true under the assumption of low input

capacitance. Intuitively, the input capacitance and the feedback capacitance form a non-inverting charge amplifier for the input referred noise at the positive terminal. Thus, the effect of input capacitance must be taken into account.

Including the input capacitance, and assuming $e_{n,op}$ to be the opamp noise, the output noise is given by:

$$e_{n,out} \cong e_{n,op}\left(1 + \frac{R_f C_i s}{1 + sR_f C_{ft}}\right) \tag{4.10}$$

Where C_i is the input capacitance including the biosensor capacitance and opamp input capacitances. $e_{n,out}$ is the opamp output voltage noise and C_{ft} is the total capacitance in the feedback including the stray capacitance. According to equation (4.10) to reduce the contribution of opamp noise the feedback capacitance needs to be increased C_{ft} needs to be increased. This can be done by adding a capacitor in parallel to the feedback resistor. However, increasing the feedback capacitance would also reduce the signal bandwidth (see equation (4.9)), which is not ideal. Equation (4.10) also indicates that for high frequencies when the impedance due to the feedback capacitance, C_{ft}, is much smaller than the feedback resistor, R_f (i.e. $sR_f C_{ft} \gg 1$), there would be a noise gain peaking of $1 + \frac{C_i}{C_{ft}}$, which ties with the intuition of the system being a non-inverting charge amplifier for the input referred opamp noise. This noise gain peaking will occur until the assumption of the operational amplifier gain, $A(s) \geq (1 + C_i/C_{ft})$ is no longer valid. After this point the noise gain will follow the open-loop amplifier frequency response. Thus, when designing the operational amplifier the unity gain bandwidth does not have to be very large.

Alternatively, a low-pass filter can be added after the TIA to limit the overall noise bandwidth. If we consider a typical nanopore setup with an input capacitance in the order of 10 pF and considering only the stray capacitance of 100fF as we did earlier in section 4.2.1, the input noise gets amplified by approximately a factor of 100. The

output signal was calculated earlier to be 110μV, thus the amplifier input RMS noise needs to be less than 200 nV to meet the minimum SNR of 5. The input referred noise for this amplifier is 6.3 nV/$\sqrt{Hz}$ for the 1kHz bandwidth specification, which can be quite challenging to design.

Another consequence of the input capacitance is its effect on the stability of the operational amplifier, since the low-pass filter formed by the input resistance, R_i, and the input capacitance, C_i, results in a zero in the TIA transfer function. The location of this zero can jeopardize the phase margin of the amplifier and can be mitigated by increasing the feedback capacitance at the expense of bandwidth. The effect of the input capacitance on amplifier stability can be understood by adding a pole located at $(R_i||R_f)(C_i + C_{ft})$ and a zero located at $R_f C_{ft}$ to the amplifier transfer function. One option is to locate the zero close to the pole to effectively null it.

4.2.2 Capacitive Transimpedance Amplifier

As seen in the previous section, the resistive feedback TIA has many interdependent parameters making it challenging to design. One approach to mitigate this is to use a noiseless capacitor in the feedback instead of a resistor. This substitution converts the TIA into an integrator and the output voltage is given by:

$$v_{out} = -I_{sen}\frac{1}{sC_{int}} \tag{4.11}$$

Where C_{int} is the integrator feedback capacitor. From (4.11), it can be seen that at DC, the output of the opamp would saturate due to limited supply values. Therefore, in this approach, either the DC value should be cancelled (Continuous-Time (CT) approach) or the opamp has to be periodically reset (Discrete-Time (DT) approach) to

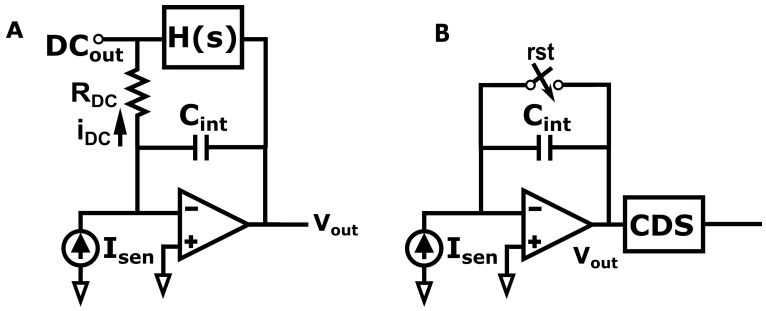

Figure 4.3: Capacitive feedback TIAs with different schemes for saturation prevention, (a) is capacitive feedback TIA with DC cancellation loop (CT scheme), (b) is resetting capacitive feedback TIA (DT scheme).

avoid saturation. The thermal noise contribution from the feedback resistor is eliminated in the case of the CT approach and has a kT/C contribution in the DT approach due to the resetting switch. However, the integrator frequency shapes the signal attenuating high-frequency signals and thus has to be restored. As shown in Fig. 4.2B, a differentiator is usually placed after the integrator to counteract its effect converting the output voltage to current as well. Therefore, the current in the differentiator capacitor C_{diff} is given by:

$$I_{out} = -I_{sen}\frac{1}{sC_{int}} \times sC_{diff} \tag{4.12}$$

$$I_{out} = -I_{sen}\frac{C_{diff}}{C_{int}} \tag{4.13}$$

From equation (4.13), it can be seen that the capacitance values can be chosen to amplify the current. The amplified current can then be converted using a resistive TIA with relaxed design constraints owing to the larger current, alleviating the noise-bandwidth trade-off.

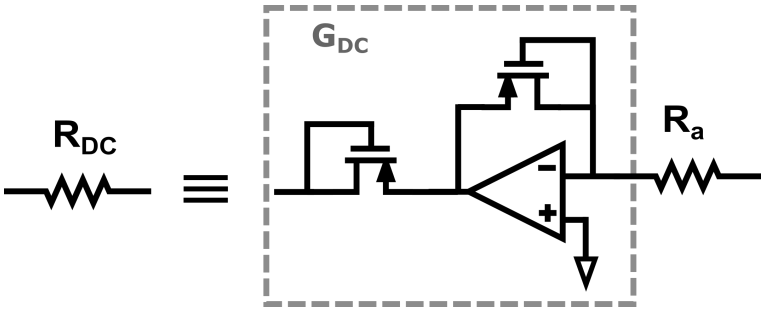

Figure 4.4: Current scaling scheme.

Continuous-Time capacitive feedback TIA

The continuous-Time approach involves removing the DC value of the input current so the opamp does not saturate. The principle of this approach is shown in Fig. 4.3A. The TIA output's DC value is extracted using an appropriate filter and using a resistor the voltage gets converted to current and fed back to input. Therefore, only the AC value flows through the feedback capacitor which avoids saturation. There have been different dc current removal blocks proposed. [44] implement a low frequency filter in the feedback path . However, adding this feedback path introduces several poles to the system, which might cause instability and requires placing additional zeros in the transfer function to guarantee stability. Several stages of amplifiers are required to guarantee the high DC gain of H(s) necessary for this approach. Overall, though this implementation is fairly complex it utilizes very clever techniques to overcome the challenges. A technique worth noting is the current-scaling approach shown in Fig. 4.4. Here a linear resistor of very high value is realized using scaled transistors. The non-linearity of the transistor is minimized by using a clever combination of a smaller linear resistor and feedback. Intuitively the voltage is converted into a linear current via a linear resistor which is then converted into a gate voltage by placing a diode connected transistor in the feedback path. By applying voltage output of the opamp applied to a scaled transistor a smaller current

(and hence a larger resistor) is realized. A key point to note is the opamp feedback ensures the matching of both gate-source and drain-source voltages ensuring very good current matching. The noise of the G_{dc} implementation is given by the device noise $2\gamma kT/g_m$, which at low currents typically used results in shot noise due to subthreshold operation of the devices(i.e $\gamma = 1, g_m = I_{dc}/kT$) and is given by $2qI_{dc}$. Alternatively, in [45] a less complex approach is introduced with a more relaxed stability problem due to its reduced number of poles. However, these DC feedback loops have limited bandwidth. Fast settling semi-digital feedback loops have been proposed to solve this problem,. In this approach, the TIA output is converted to digital using an Analog-to Digital Converter (ADC) in the feedback. Then, the DC value is extracted using a digital low-pass filter (LPF) and converted back to analog voltage with a Digital-to-Analog Converter (DAC) and finally into a current via a resistor [46, 47]. Though, a direct current output DAC could be used in the feedback the noise contribution from active devices is generally much larger than a comparable resistor. This approach also allows for a larger DC current cancellation since the feedback noise is not proportional to the DC current in the resistor implementation. In the dc cancellation approach, although the feedback resistor of the TIA is replaced with capacitor, since there is a resistor in the active feedback, the noise contribution is dominated by the feedback noise and results in almost the same noise as the resistive TIA [42]. Thus, the minimum detectable signal and SNR calculations remain the same as the resistive TIA discussed in section 4.2.1. However, the elimination of the charge injection from resetting the switch and the reduced opamp bandwidth requirements can make this approach attractive for certain applications. The DC cancellation loop also has the advantage of cancelling low frequency 1/f noise and offset.

Discrete-Time capacitive feedback TIA

In the discrete-time approach, instead of removing the DC value, the opamp is reset periodically to avoid saturation as shown in Fig. 4.3B. The sampled nature of this approach is generally more compatible with a digital interface. However, this approach introduces switch noise, clock feed-through, and charge injection to the system. There are also data discontinuities due to resetting, which can be rendered negligible by minimizing the reset time. If a differentiator follows the resetting integrator, the differentiator must be disabled to prevent it from amplifying the discontinuity. From (4.11), it is clear that for small current sensing C_{int} has to be small enough. With DT approach, small C_{int} would result in a larger $\frac{kT}{C}$ switch noise contribution. The most popular technique for flicker and reset noise reduction is Correlated Double Sampling (CDS) [48–50]. Chopper stabilization is another technique often used for flicker noise suppression [51]. As shown in (4.13), the integrator-differentiator scheme scales the current converted to a voltage using a resistive TIA, as shown in Fig. 4.2B, and finally to a digital signal using an ADC. Another approach is replacing the resistive TIA with a sample and hold switched capacitor [48] or another resetting capacitive feedback TIA [52] followed by a low-pass filter for high frequency noise reduction and converted to a digital signal using an ADC. In [49], using a CDS technique the differentiator output gets sampled and then it's applied to a charge-based $\Delta\Sigma$ ADC. The input referred noise for this types of capacitive feedback TIAs, assuming kTC reset noise cancellation by CDS, is given by [42]:

$$i_n{}^2 \cong 2C_T^2 \frac{\pi f_C}{T_S} e_{n,op}^2 \tag{4.14}$$

Where $e_{n,op}$ is opamp voltage noise and f_C is the 3-dB corner frequency for the noise transfer function. To ensure appropriate settling time, the gain-bandwidth product (GBW)

is chosen to be $\frac{5}{T_S}$, therefore f_C is given as:

$$f_C \cong GBW\frac{C_{int}}{C_T} \cong \frac{5}{T_S}\frac{C_{int}}{C_T} \tag{4.15}$$

Substituting (4.15) in (4.14), (4.14) simplifies to:

$${i_n}^2 \cong C_T\frac{10\pi}{T_S^2}C_{int}e_{n,op}^2 \tag{4.16}$$

Where C_T is the summation of the input and feedback(integration) capacitance, and $(C_T = C_{in} + C_{int})$, therefore (4.16) further simplifies to:

$${i_n}^2 \cong \frac{10\pi}{R_{sc}^2}(1 + \frac{C_{in}}{C_{int}})e_{n,op}^2 \tag{4.17}$$

Where $R_{sc} = \frac{T_S}{C_{int}}$. Therefore, from (4.17), SNR can be written as:

$$SNR = I_{min}^2\frac{R_{sc}^2}{10\pi(1 + \frac{C_{in}}{C_{int}})e_{n,op}^2} \tag{4.18}$$

Where I_{min} is:

$$I_{min} = v_{out,min}(\frac{C_{int}}{T_S}) = \frac{v_{out,min}}{R_{sc}} \tag{4.19}$$

Therefore (4.18) simplifies to:

$$SNR = v_{out,min}^2(\frac{C_{int}^2}{T_S^2})\frac{R_{sc}^2}{10\pi(1 + \frac{C_{in}}{C_{int}})e_{n,op}^2} = \frac{v_{out,min}^2}{10\pi(1 + \frac{C_{in}}{C_{int}})e_{n,op}^2} \tag{4.20}$$

One other important element for design consideration is Dynamic Range (DR) which is defined as the ratio of the maximum input signal power and the in-band noise power.

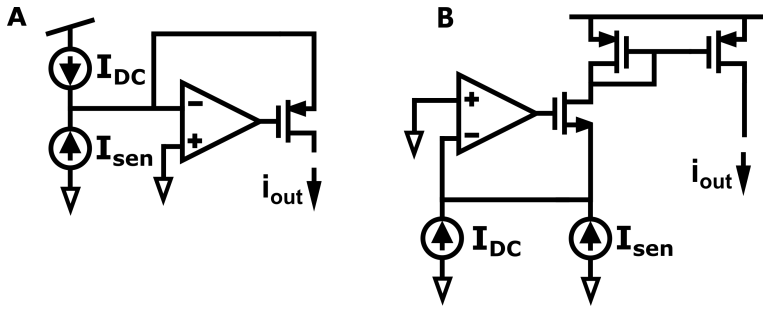

Figure 4.5: Current output front-ends, (a) is current conveyor basic front end, (b) current mirror front end.

Therefore can be written as:

$$DR = \frac{v_{out,max}^2}{R_{sc}^2 i_n^2 \frac{f_S}{2}} = \frac{2v_{out,max}^2 T_S}{10\pi(1+\frac{C_{in}}{C_{int}})e_{n,op}^2} \tag{4.21}$$

Thus, for the capacitive resetting TIA the trade-offs are slightly more complex since sampling time needs to be also taken into account. Also if the reset time is short the amplifier bandwidth has to allow for complete resetting of the capacitor, requiring a high-gain wide-bandwidth amplifier.

4.2.3 Current Output Front-Ends

Another common method for bidirectional current sensing is to use unidirectional current output circuits but subtract it from a DC bias current to enable bidirectionality and maintain linear operation [53], as shown in Fig. 4.5. However, this may cause current leakage, additional noise and requires a high resolution ADC. Therefore, other methods have been introduced to solve these issues [54, 55]. For digital conversion of these structures, the output current can be converted to voltage first [53] before A/D conversion. Alternatively, it can be converted directly to digital using current based

incremental delta-sigma ADCs [55] or using an I-F converter [56].

Current Conveyor

The basic current conveyor circuit is shown in Fig. 4.5A. It consists of a unity-gain current buffer and consequently it would need amplification afterwards. However, since there are no resistors and capacitors involved in its architecture, it would let higher bandwidth measurements while consuming less area makes it more suitable for biosensor arrays [57]. However, the noise is now determined by the noise of the transistor and the DC bias current flowing through it.

Current Mirror

The basic current mirror sensing circuit is shown in Fig. 4.5B. The idea behind using a current mirror as current sensing interface is the fact that it copies the sensor current therefore enables current measurement of the copied version instead. Therefore, it provides isolation of the sensing stage, area efficiency and higher bandwidth measurement.

4.2.4 Design Methodology

We have developed a simple design methodology for choosing the right front-end depending on the application. The first step towards choosing a current sensing front end design is properly defining the application requirements and choosing the appropriate structure based on the biosensor specifications as discussed in section 1.2.1. A minimum detectable current versus bandwidth relationship can be found in Fig. 4.6A for RTIA. Minimum detectable current versus bandwidth plots are derived from SNR equations of (4.7) and (4.18) for a minimum SNR of 5 and minimum output voltage of 1mV. Output

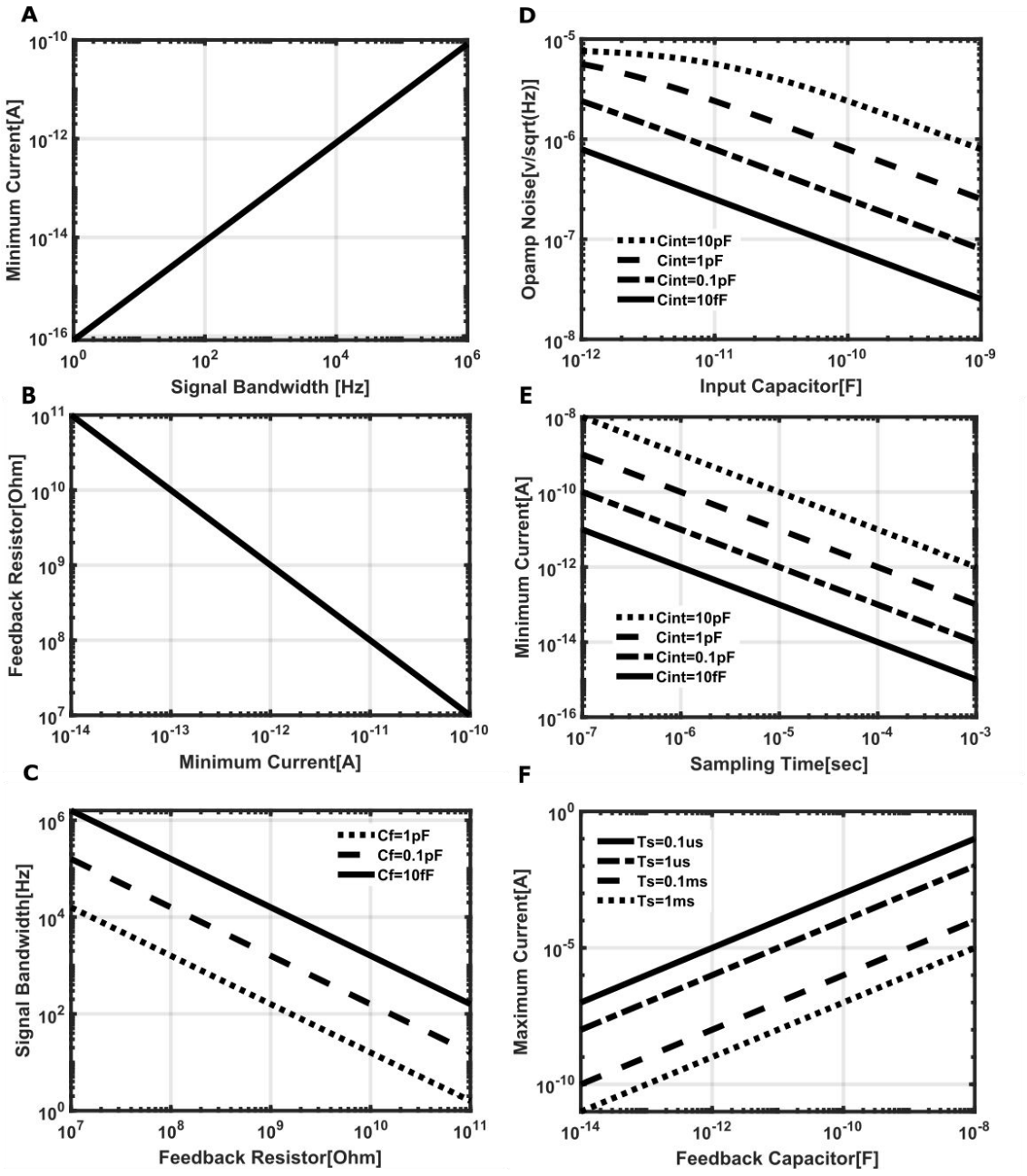

Figure 4.6: TIA based current sensing front-ends design plots, (a) resistive feedback TIA minimum detectable current vs. frequency, (b) RTIA feedback resistor values vs. minimum detectable current, (c) RTIA signal bandwidth vs. feedback resistor , (d) DT-CTIA opamp noise vs. input capacitor, (e) DT-CTIA minimum current vs. sampling frequency, (f) DT-CTIA maximum current vs. feedback capacitor.

voltage of 1mV is reasonable choice for modern CMOS nodes which have limited power supply voltages, for example a 1V supply would result in a dynamic range of 10-bits. Therefore it is assumed to be 1mV for ease of calculation and can be scaled if needed. Fig. 4.6, shows estimated plots based on equations (4.1)-(4.18). Fig. 4.6A, B and C, illustrate plots for resistive feedback TIA design and Fig. 4.6D, E and F, illustrate plots for discrete-time capacitive TIA design assuming a CDS following the CTIA as shown in Fig. 4.3B. The graphical design procedure for the resistive TIA is performed as follows: 1) Given the signal bandwidth specification, the minimum detectable current level can be read from Fig. 4.6A. Assuming this value meets specification, it can be used in Fig. 4.6B to determine the feedback resistor value (neglecting any stray or feedback capacitance). The value of feedback resistor can then be used in Fig. 4.6C and the appropriate curve for the feedback capacitor (either intentionally placed for stability or is the stray capacitance of the resistor) to determine the reduction in bandwidth. If the new reduced bandwidth is within the specification then the design procedure is complete, otherwise the specifications have to be altered until convergence. As an example consider a signal bandwidth of 10kHz, the minimum detectable current is 1pA, as shown in Fig. 4.6A. Fig. 4.6B then yields 1GΩ as the feedback resistor consistent with the 1mV minimum output signal requirement. If we assume the feedback capacitance is 100fF, the signal bandwidth is given as 1kHz, which was not our initial assumption. Now we have choice either we can decide to have a lower signal bandwidth and use the results, or we will have to increase the minimum detectable signal. If the design bandwidth is deemed the most important, then using Fig. 4.6C and the C_f=100fF curve, we see a feedback resistor value of 100 MΩ is needed, which increases the minimum detectable signal to 10 pA. Alternatively, if the feedback capacitance value can be adjusted to 10fF we can achieve the original specifications. Though it should be noted a stray capacitance value of 10fF is rather unrealistic.

The capacitive TIA requires a more subtle design procedure. It should be noted for this design it is assumed the integration-differentiator gain via the capacitance ratio is 10 and thus the voltage output of the integrator is 100μV. Furthermore, it is assumed the kT/C reset switch noise is eliminated by CDS. First the target input referred noise of the amplifier is used to determine the integration capacitance based on the sensor capacitance from the plot in Fig. 4.6D. As the integration capacitor begins to dominate the noise constraint asymptotically converges to $10\mu V/\sqrt{Hz}$. The value of integration capacitance can then be used to pick the constraint curve in Fig. 4.6E. A sampling time can then be specified and the minimum detectable current can be determined. Alternatively, one can also choose the minimum detectable current and determine the sampling time. Note the signal bandwidth is a factor of 2 smaller than the sampling frequency (i.e. $1/T_S$). Once the sampling time and integration capacitor are chosen the maximum detectable signal can be determined from Fig. 4.6F to ensure the signal range requirement is met. As an example, if we assume the nanopore capacitance to be 10pF, a C_{int}=1pF would give us a relaxed constraint of $2\mu V/\sqrt{Hz}$. However, if we wanted to detect 1pA the sampling time would be equal to 100 μs from Fig. 4.6E and thus the signal bandwidth would be 5 kHz. From Fig. 4.6F the maximum current is about 1nA.

4.3 Direct Current-to-Digital Conversion

Current-mode $\Delta\Sigma$ ADCs have been recently used as direct current to digital converters for biosensor interfaces. Since the TIA is inherent to their structures, $\Delta\Sigma$ ADCs are most suitable for current sensing. However, with conventional $\Delta\Sigma$ ADCs, the noise from feedback is large which limits the minimum detectable signal from input. Some solutions have been proposed to overcome this issue [21, 58]. Since the feedback noise is crucial, different feedback DACs for $\Delta\Sigma$ ADCs are investigated next followed by a design

methodology.

4.3.1 Current Source-Based DAC Feedback

In this architecture, a current source is used as a DAC [59]. The limit of detection can be determined by computing the signal-to-noise ratio (SNR). If the full scale reference current of the DAC is I_{ref}, then the minimum current (LSB) is defined as:

$$I_{min} = \frac{I_{ref}}{2^N} \tag{4.22}$$

Assuming the current source is shot-noise limited, the noise power of the DAC is given by:

$$P_{Ncf} = 2qI_{ref}\Delta f \tag{4.23}$$

$$SNR = \frac{I_{ref}}{2^{(2N+1)}q\Delta f} \tag{4.24}$$

According to (4.24), there are three degrees of freedom one can use to achieve this, bandwidth (Δf), reference current (I_{ref}), and number of bits (N). As expected there is the classical trade-off between the achievable bandwidth and minimum detectable signal.

4.3.2 Resistor DAC Feedback

An alternative to the current source, especially for discrete implementations, is the resistor. In this structure a reference voltage (V_{ref}) is used as a DAC and converted to

current (I_{ref}) using a resistor, R_{DAC}.

$$I_{ref} = \frac{V_{ref}}{R_{DAC}} \tag{4.25}$$

substituting (4.25) in (4.22), the minimum current can be derived, which is:

$$I_{min} = \frac{V_{ref}}{2^N R_{DAC}} \tag{4.26}$$

The thermal current noise power of the resistor is given by

$$P_{Nrf} = \frac{4kT\Delta f}{R_{DAC}} \tag{4.27}$$

The SNR for the minimum detectable signal is then given by:

$$SNR = \frac{{V_{ref}}^2}{4KTR_{DAC}2^{2N}\Delta f} \tag{4.28}$$

In this case there are four degrees of freedom; N, V_{ref}, R_{DAC} and Δf. However, there are limitations on V_{ref} and R_{DAC}. For example, for 1 kHz frequency and N=10, the LSB current is 10^{-14} A. For the fixed reference voltage of 1 V, the DAC resistor would be approximately $11.5G\Omega$ which is impractical for on-chip implementations and also limits the bandwidth due to the parasitic capacitance. Number of bits, N, and frequency (Δf) have the same effect as current source based DACs. In a conventional $\Delta\Sigma$ the LSB current value realizable is limited by the resistor. However, at the board level it is easy to use large resistors.

4.3.3 Switched Capacitor DAC Feedback

Alternatively, a switched capacitor can be used instead of a large resistor. A detailed noise analysis for switched capacitor DACs in CT-$\Delta\Sigma$ modulators has been reported [60]. Input-referred noise in this case would be [60]:

$$P_{Nsw}(f) = 4kT(1-\tau)^2 \frac{1}{R_{SC}} \tag{4.29}$$

$$R_{SC} = \frac{T_S}{C_{DAC}} \tag{4.30}$$

where τ and T_S are the duty cycle and clock period for turning switches on and off, respectively.

$$I_{ref} = \frac{V_{ref}}{R_{SC}} = \frac{V_{ref} C_{DAC}}{T_S} \tag{4.31}$$

$$SNR = \frac{{V_{ref}}^2 C_{DAC}}{4KT(1-\tau)^2 T_S 2^{2N} \Delta f} \tag{4.32}$$

As shown in (4.29), to reduce the noise from feedback, either τ should be designed to be small or R_{SC} must be very large. In most implementations τ is fixed and it is usually half (i.e. 50% duty-cycle). From (4.30), it can be seen that, in order to make R_{SC} very large, either sampling time (T_S) has to be large or C_{DAC} has to be very small. Increasing T_S limits the design to very low bandwidths and low oversampling ratios negating the noise reduction benefits resulting from a high OSR. The constraint on the minimum value of C_{DAC} is imposed by the fabrication process.

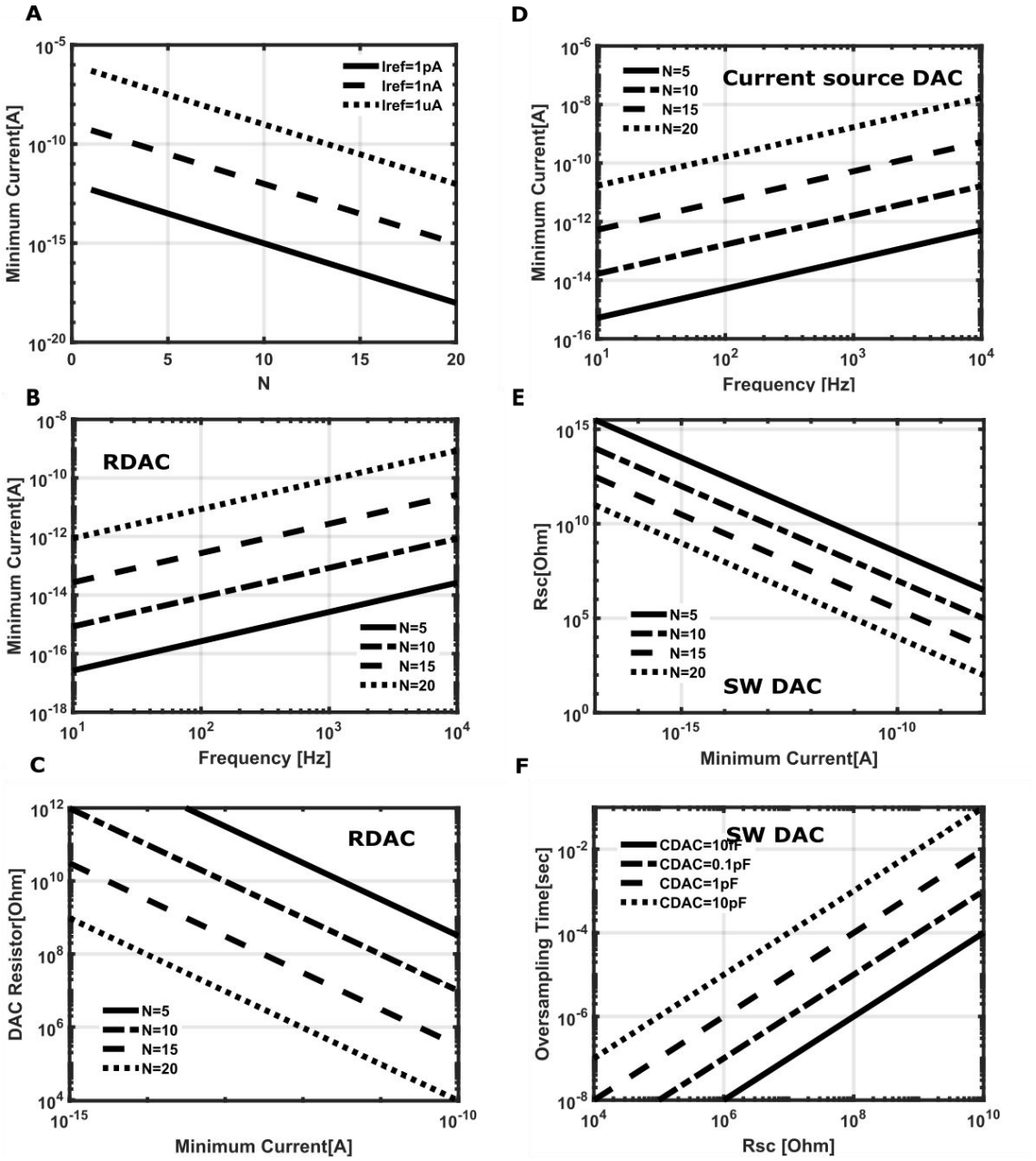

Figure 4.7: Delta Sigma ADC different DAC structures design plots, (a) Minimum detectable current versus number of bits dependency, (b) minimum current versus frequency dependency for resistive DACs , (c) DAC resistor vs. minimum current dependency for resistive DACs, (d) minimum current versus frequency dependency for current source based DACs, (e) R_{sc} vs. minimum detectable current dependency for switch capacitor DACs, (f) Sampling time vs. R_{sc} for switched capacitor DACs.

4.3.4 Design Methodology

In this section a methodology is introduced to easily select the appropriate DAC structure for a $\Delta\Sigma$ direct current-to-digital conversion based on the application. In this methodology, the reference voltage is assumed to be 1V for ease of calculations and is reasonable assumption given modern CMOS technology nodes. However, it can be scaled easily if needed.

This methodology uses the plots drawn in Fig. 4.7. Fig. 4.7A shows the relationship between minimum detectable current versus number of bits shown in equation (4.22) for different fixed reference currents. Selection of the feedback structure suitable for the design starts with the required minimum current based on the application. Using this value the number of bits needed for a fixed reference current selected based on process and power requirements can be determined.

Fig. 4.7D illustrates minimum current versus bandwidth for different number of bits for current source based DAC based on equation (4.24). The plot is drawn for a minimum SNR of 5 and minimum detectable current is defined as shown in equation (4.22). The required bandwidth is also dictated by the application. Therefore, for the minimum current and number of bits selected in Fig. 4.7A, the estimated bandwidth can be found from Fig. 4.7D. However, if the specifications are not met, changing the reference current and the number of bits can help to some extent.

Alternatively, a resistive DAC can be used and its performance is shown in Fig. 4.7B and C. Knowing the minimum current and number of bits from Fig. 4.7A, the bandwidth can be determined using the minimum current and bandwidth relationship plotted in Fig. 4.7B. The figure is based on equation (4.28) for a minimum SNR of 5. Here, the trade off seems to more relaxed compared to the current DAC but there is a third factor which has to be taken into account especially for chip level implementation namely

the feedback resistor value. The relationship between the DAC resistor and minimum detectable current is shown in Fig. 4.7C. Clearly from the plot, as minimum current decreases the value of resistor increases and as the resistor value increases it becomes impossible to implement on chip or even if possible, it consumes a large area making it unsuitable for compact large scale implementations. However, for some applications an optimum design value can be found.

Another alternative DAC structure is the switched capacitor DAC which has the benefit of replacing the feedback resistor with a capacitor, thereby removing the area issue faced by resistors. Fig. 4.7E shows R_{sc} values for minimum current and number of bits chosen from Fig. 4.7A. Once R_{sc} value is determined moving to Fig. 4.7F would give us choices for the DAC capacitor and oversampling frequency. For example, assuming we pick 1pA minimum current and 10 bits from Fig. 4.7A, moving to Fig. 4.7E, shows $R_{sc} \approx 1G\Omega$. Using this value, oversampling time and DAC capacitor values can be chosen from Fig. 4.7F, which is about $10\mu s$ for 10fF DAC capacitor. However, 10fF is a an unrealistic capacitor value due to process limitations. 100fF capacitor is more realistic which shows 100μs oversampling time. One can convert this to signal bandwidth by using the oversampling ratio.

Most sensor $\Delta\Sigma$ structures use either a first or second order architecture with a 1-bit quantizer. In this case there is a simple relationship, between the maximum achievable (Signal to Quantization Noise Ratio)SQNR and the OSR [61]. For the first-order it is given by:

$$SQNR_{max} = \frac{9(OSR)^3}{2\pi^2} \tag{4.33}$$

and for second-order, it is given by:

$$SQNR_{max} = \frac{15(OSR)^5}{2\pi^4} \tag{4.34}$$

Relating this to the design methodology requires a relationship between N and OSR which can be found through the relationship between N and SQNR, which is given by SQNR(dB) =6.02N-1.76. In our earlier example, N=10, yielding a required SQNR of ≈58dB or $10^{5.8}$. When substituted in the respective OSR relationship for first-order, we obtain an OSR of 111.4. Usually for practical reasons OSR is expressed in powers of 2, so the OSR for is 128 for this example. Thus, the signal bandwidth is approximately 40 Hz. If we use the second-order system, the OSR is 32 (nearest power of 2 for the actual value of 24), yielding a signal bandwidth of 156.25 Hz. Therefore, even though the switch-capacitor DAC saves area, there is a penalty to be paid in terms of the signal-bandwidth since the realized equivalent feedback resistor is dependent on the OSR.

4.3.5 Discrete-Time vs Continuous-Time ΔΣ modulators

Discrete-Time

Recently, an incremental ΔΣ modulators was reported [58]. This structure is shown in Fig. 4.8A. As illustrated, for feedback noise reduction, the current is scaled in the feedback using previous integrator-differentiator schemes. The discrete-time nature of this structure makes it suitable for large scale multiplexing schemes. However it suffers from switching noise. Another incremental approach was introduced in [62], which reduces the noise using a 12 bit SAR ADC and 11 bit DAC in the feedback at the price of adding more complexity to the structure.

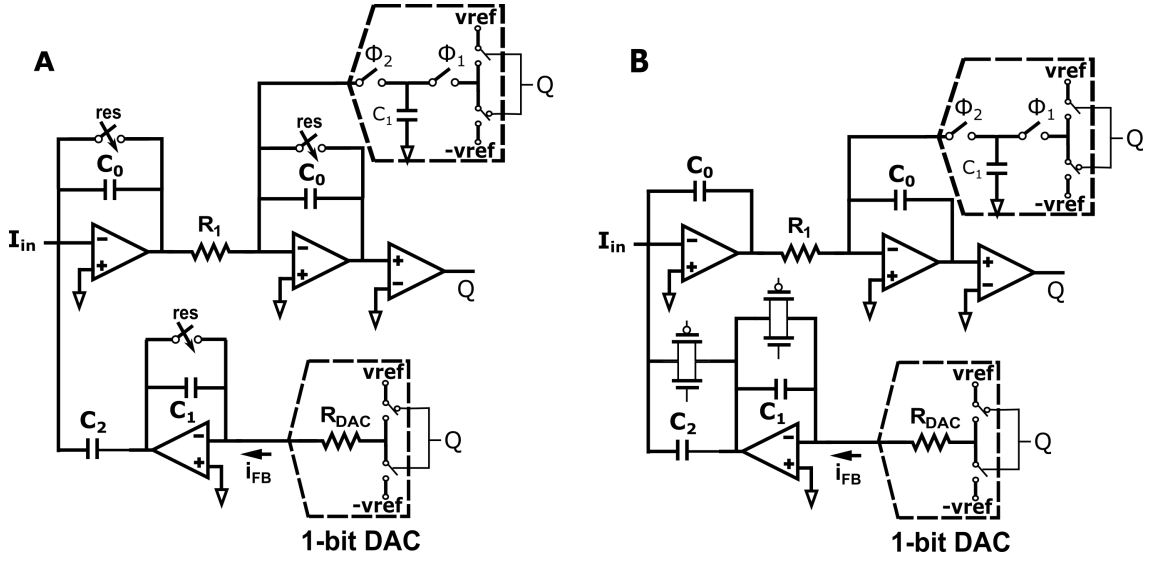

Figure 4.8: Direct current-to-digital conversion redrawn from [58], (a) is an incremental $\Delta\Sigma$ ADC with current scaling in the feedback, (b) continuous-time $\Delta\Sigma$ ADC with current scaling in the feedback with assisting transistors as feedback for bias set.

Continuous-Time

There are also continuous-time $\Delta\Sigma$ structures which convert current directly to voltage [63]. In this structure a 3^{rd} order modulator is designed to cover a wide range of input currents. Although a wide range has been achieved with this structure, the area and power consumption are still not suitable for arrays of biosensors. Moving towards more power and area efficient configurations, an opamp less first order $\Delta\Sigma$ ADC was proposed by [64]. However, the structure is only limited to first order modulators and relies on biosensor capacitance as the integrator. [65] proposed an hourglass asynchronous $\Delta\Sigma$ ADC which converts the current continuously to digital. Another continuous-time $\Delta\Sigma$ ADC shown in Fig. 4.8B uses also the current scaling technique in the feedback but instead of resetting the opamps, it provides an active element to set the bias [58].

We recently reported a continuous-time $\Delta\Sigma$ ADC [21], which also uses current scaling

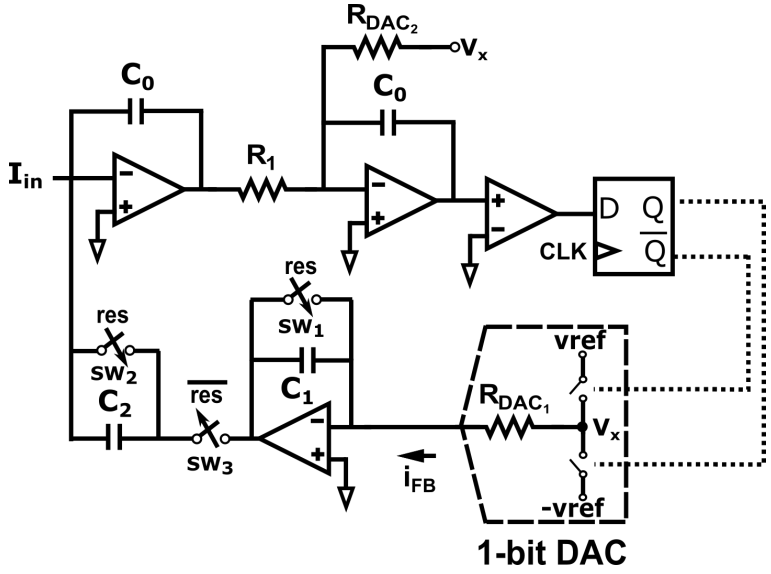

Figure 4.9: A continuous-time $\Delta\Sigma$ ADC with resetting current scaling in the feedback [21]

technique in the feedback with a different resetting approach to keep the structure operating as a CT-DSM and not as an incremental delta-sigma and is shown in Fig. 4.9. This structure further reduces the noise from feedback and enables recording smaller currents at a higher bandwidth. This technique can be applied to both first and second order $\Delta\Sigma$ structures.

4.4 Towards large scale implementation

As the push towards implementing massive arrays for multiplexing and high-throughput continues, power and area of the current-sensing circuits are drawing more attention In this section scalable architectures, along with power and area reduction techniques are reviewed.

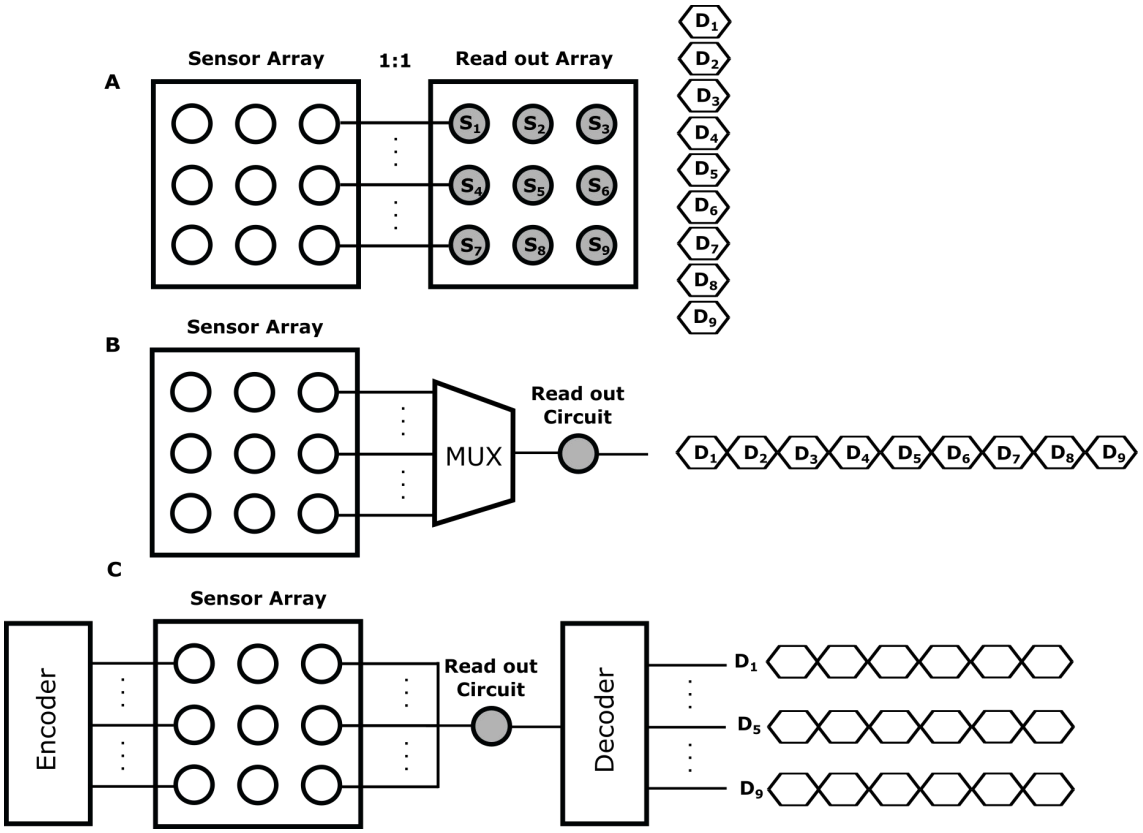

Figure 4.10: Arraying approaches, (a) Fully parallel sensing, (b) Time-division multiplexing, (c) Code-division multiplexing.

4.4.1 Scalable, parallel potentiostat architectures

Arraying nanopore biosensors is gaining more attention due to their portability and high throughput [66]. However, parallelizing nanopore biosensors introduces circuit design challenges due to limited chip area and increased power consumption. There are three popular methods to interface the read-out circuits and biosensor arrays, shown in Fig. 4.10 for a 3×3 biosensor array. Each approach is explained in detail in the next few sections.

Fully Parallel Sensing

Implementing a fully parallel read-out requires each sensor to have its own dedicated current sensing front-end. As shown in Fig. 4.10A there is a 1:1 mapping between biosensors and read out circuits. In this figure, S_i and D_i indicate the sensor and output data, where i represents the sensor number. Therefore, as illustrated in 4.10A, data rate would increase with the sample rate in discrete-time approaches. Also, with this configuration, simultaneous reading of continuous time data via dedicated parallel outputs would be feasible.

However, with the conventional read out circuits this would be very challenging due to the power and area constraints. There have been switching opamp structures [67] proposed which relaxes the opamp power and area limitations while maintaining the same performance as conventional opamps. However, separating the front-end and ADC, even with circuit optimization, still requires extra circuitry for further bandwidth and noise improvement before conversion by the ADC. Therefore, a structural improvement is needed to enable larger scale arrays. Direct current-to digital conversion are more suitable [21, 58, 63, 64] for this approach and are discussed in section 4.3.

Time-Division Multiplexing

Another common approach for reading arrayed biosensors, is time division multiplexing [68]. The principle of this approach is shown in Fig. 4.10B, where a fast multiplexer is shared between channels using a time-division approach. In this approach one channel is active and the others are idle. Therefore since only one read-out circuit is used and the multi-channel interface is done through multiplexing, the read-out circuit design is relaxed. As illustrated in Fig. 4.10B, the output data from each channel is arranged serially on the output channel. Therefore, the scan time is equal to the sum of each channel sampling time. This adversely affects the data sampling rate since the data in each sensor needs to be held for the duration of the scan time. For a $N \times N$ sensor array, the data rate is decreased by N^2.

In [69], an array of 3 $\times$ 3 sensors was implemented which can be addressed individually with a multiplexer interfaced to a DT capacitive feedback TIA followed by an ADC. In [55], an array of current-mirror based front-end ends were designed, which is then multiplexed to interface with one ADC. Using the same approach [70] implemented a scalable multiplexing architecture. A single external ADC/DAC, controls all channels using 1:64 time division multiplexing and 64:1 demultiplexing. Therefore, each channel can be selected individually.

Code-Division Multiplexing

Alternatively, code division multiplexing [71] can be used for arrayed sensors. This approach enables simultaneous measurement of multiple sensors on a single channel, as

shown in Fig. 4.10C. The basic principle of this approach is to mix each channel with a unique pseudo-random sequence and then combine all channels into one single channel before transmission. The key is usually generated by a pseudo-random bit generator, whose polynomial is known to both the sender and the receiver. Since the pseudo-random sequence is known to the receiver it can be decoded. Therefore, channels can be read simultaneously as illustrated in Fig. 4.10C. In this approach, the data update rate is equal to the channel sample rate. However, the circuit design for this approach can be fairly complex for low noise systems.

4.5 Conclusion

Depending on the type of nanopore sensor, the noise, bandwidth and minimum current requirements are different. In general, for nanopore devices, usually a few 100fA of rms noise is required with signal bandwidths in the 10s of kHz. In this chapter different current-sensing approaches were reviewed. A comparison table for all the approaches discussed is shown in Table 4.1. As discussed throughout the chapter, there is a trade-off between minimum detectable input signal and bandwidth and through years there has been a continued push to overcome these limitations. Recently there has been an increased focus on scalable structures, which enable large arrays of biosensors. Therefore, current designs tend to focus on low power and area efficient structures while satisfying the noise-bandwidth specifications. In keeping with this trend, direct current-to-digital conversion structures along with scalable architectures were also reviewed. We believe this work can serve as a useful reference to designers of the electronics behind the nanopore sensor.

Table 4.1: Comparison of different current sensing front-ends.

Paper	**Technology (nm)**	**Architecture**	**Noise** ($\frac{fA}{\sqrt{Hz}}$)	**BW (Hz)**	**Power (W)**	**Area** (mm^2)	**Input Range (A)**
[65]	180	ADSM	∼58	1.8	295μ	0.2	0.1p-10μ
[62]	55	Incremental DSM	∼342	512	1m	0.585	7p-200μ
[49]	350	DT-CTIA	5	1K	23m	0.5	0.15p-5n
[46]	500	RTIA	8	750K	-	∼0.18	1p-10μ
[72]	350	CT-CTIA	5	-	21m	0.11	-
[43]	500	RTIA	50	10K	0.3m	0.805	5p-20n
[58]	350	Incremental DSM	2.8	10K	4.6m	0.32	0.28p-1n
[58]	350	CT-DSM	2	10K	6.73m	0.63	0.2p-1n
[55]	180	Current-Mirror	10000	∼100	70μ	0.02	1n-1μ
[51]	130	Current-Conveyor	10000	-	4μ	0.01	8.6p-350n
[22]	**45**	**CT-DSM**	**∼10**	**15k**	**125μ**	**0.042**	**0.6p-1μ**

Chapter 5

Direct Current to Digital Conversion

5.1 Introduction

In this chapter, a new current sensing approach is introduced to minimize the effect of the input capacitance and reduce the complexity and area, thus enabling massively parallel arrays. We fold the integrating TIA into the $\Delta\Sigma$ while mitigating the noise from the 1-bit current DAC in the feedback. This chapter organized as follows. Section 5.2 introduces and compares different structures for direct current to digital conversion using $\Delta\Sigma$ ADCs. Section 5.3 describes the proposed architecture. Section 5.4 shows the noise analysis for the proposed structure. Section 5.5 includes experimental results and electrical characterization with a bilayer membrane model as the input. Section 5.6 summarizes the work.

5.2 System Level design

In direct current sensing with $\Delta\Sigma$ ADCs, as shown later, the feedback current DAC contributes to the input referred noise. The current DAC can be implemented using

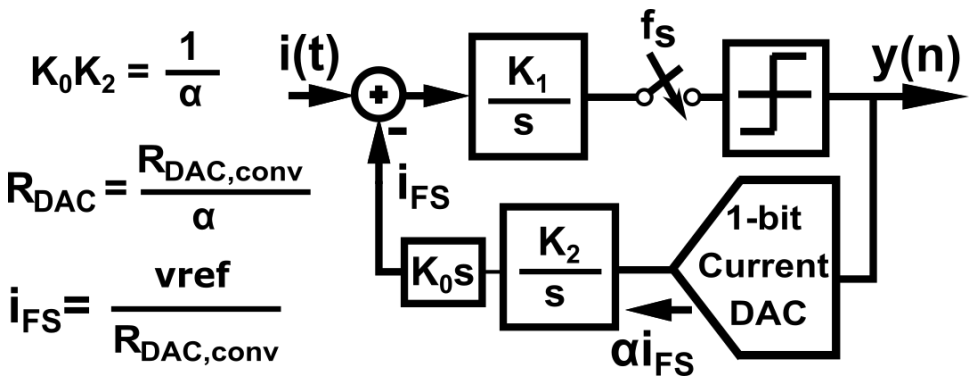

Figure 5.1: 1^{st} order $\Delta\Sigma$ modulator block diagram

current sources, resistors or switched capacitors. In Current Source-Based DAC Feedback there is the classical trade-off between the achievable bandwidth and minimum detectable signal [59]. As shown in Section 5.3 overcoming this fundamental trade-off is one of the key contributions of this work. An alternative to the current source, especially for discrete implementations, is the resistor. In a conventional $\Delta\Sigma$ the LSB current is limited by the resistor. In contrast, the LSB current of the proposed structure can be scaled which can relax the noise requirements to a certain extent. At the board level it is easy to use large resistors. So as a proof of concept, the proposed architecture is applied to this type of DAC and discussed in section 5.5. Alternatively, a switched capacitor can be used instead of a large resistor. According to noise analysis for switched capacitor DACs in CT-$\Delta\Sigma$ modulators in [60] noise reduction is limited by duty cycle and input resistance.

5.3 Proposed Architecture

Fig. 5.1 shows the proposed structure for a 1^{st} order Delta-Sigma Modulator (DSM). The idea is to use a noiseless capacitive element rather than a resistor as the feedback element. As shown in this section, unlike the switched-capacitor implementation, our architecture uses slope scaling via an integrator-differentiator pair, which does not trade-

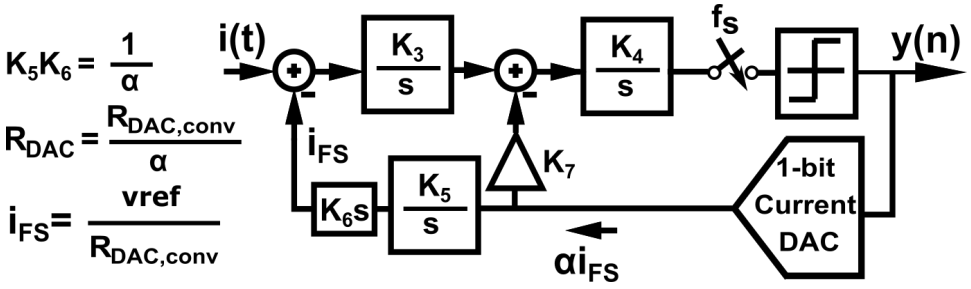

Figure 5.2: 2^{nd} order $\Delta\Sigma$ modulator block diagram

off bandwidth for sensitivity. Furthermore, slope scaling effectively scales the noise power by the square of the scale factor mitigating the noise from the integrator op-amp in the feedback. In Fig. 5.1 and Fig. 5.2 $R_{DAC,conv}$ is feedback resistor of the conventional $\Delta\Sigma$ modulator. Through this chapter R_{DAC} shows the scaled DAC resistor defined as $\frac{R_{DAC,conv}}{\alpha}$. As shown in Fig. 5.2, the α scale is compensated with slope scaling which keeps the loop gain the same as conventional $\Delta\Sigma$ modulator.

The new architecture has less noise contribution than a conventional resistive DAC feedback, without having to implement large on-chip resistors. When compared with the more practical current-source DAC based $\Delta\Sigma$ ADCs our proposed architecture has negligible feedback noise contribution to the input. Unlike the architectures proposed in [17,18], the same approach can be extended to 2^{nd} order $\Delta\Sigma$ ADC as shown in Fig. 5.2. Circuit implementation of the proposed architecture is shown in Fig. 5.3. In Fig. 5.3(a), DAC and switching structure are shown. Fig. 5.3(b) and Fig. 5.3(c) show the circuit realization and noise sources in res and $\overline{\text{res}}$ phases. In the next section we perform a comprehensive noise analysis of the slope-scaling approach.

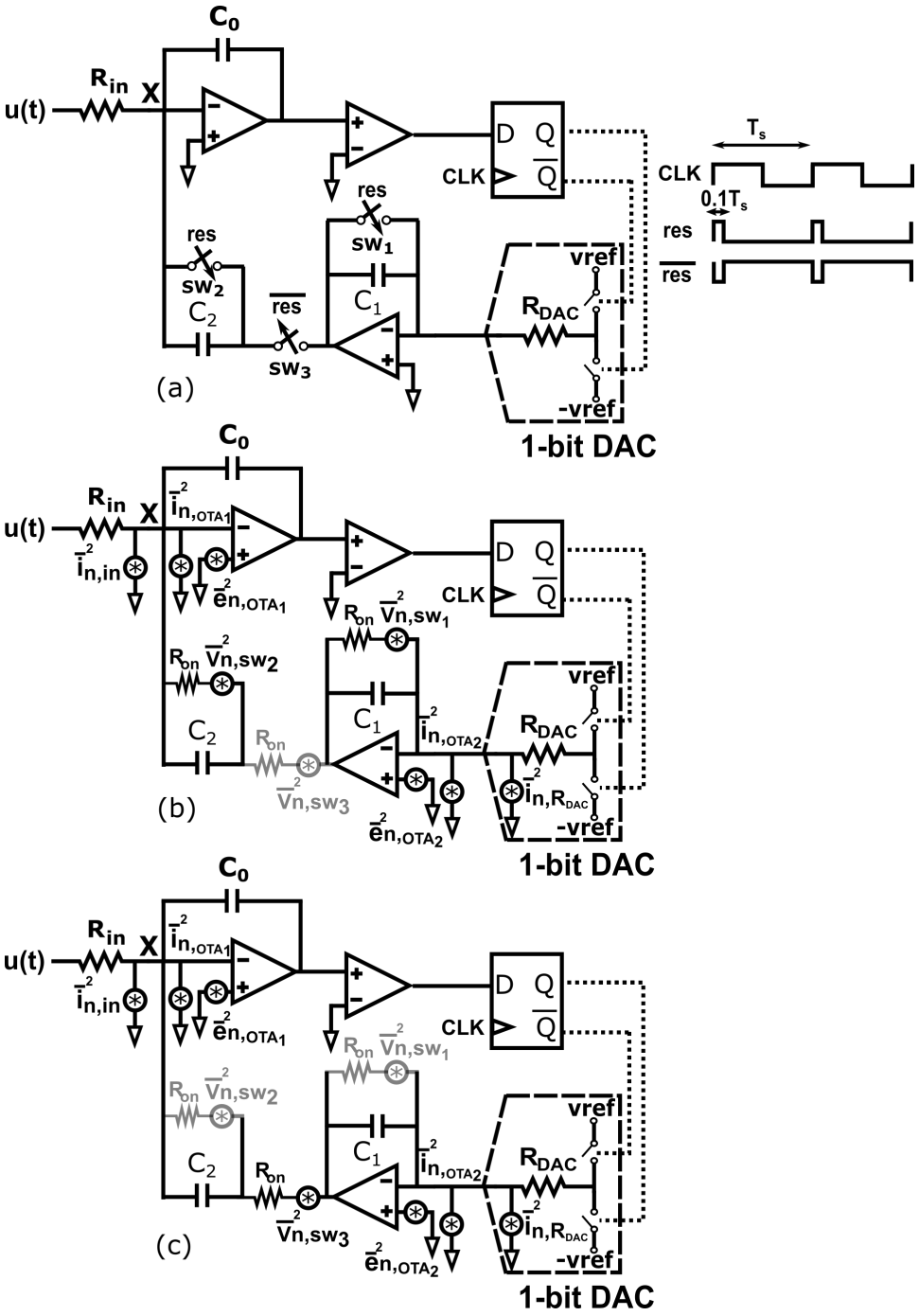

Figure 5.3: (a)1^{st} order DSM circuit implementation (b)1^{st} order DSM circuit noise model in res phase (c)1^{st} order DSM circuit noise model in $\overline{res}$ phase

5.4 Noise Analysis

As shown in this section the noise from the feedback DAC of the proposed 1^{st} order $\Delta\Sigma$ is negligible. Generally, noise sources contributing to the total input noise are white noise sources, including the feed-forward opamp current noise and the total current noise from the feedback DAC as shown in (5.1).

$$i_{n,in}^2 = i_{n,OTA_1}^2 + i_{n,fb}^2 \tag{5.1}$$

Noise sources contributing to the total feedback noise are the feedback opamp, feedback resistor and switch noise.

$$i_{n,fb}^2 = i_{n,sw}^2 + H_1(s)^2(i_{n,R_{DAC}}^2 + i_{n,OTA_2}^2) \tag{5.2}$$

$$H_1(s) \approx \frac{sC_2}{sC_1} = \frac{C_2}{C_1} \tag{5.3}$$

$$i_{n,sw}^2 = (sC)^2 v_{n,sw}^2 \tag{5.4}$$

$$v_{n,sw}^2 = 4kTR_{on}, i_{n,R_{DAC}}^2 = \frac{4kT}{R_{DAC}} \tag{5.5}$$

As it is shown in (5.2)-(5.5), input referred noise from noise sources in feedback, can be found by multiplying each source by squared of its transfer function and summing them up. The total in-band noise P_N, can be calculated by integrating this over the pass band:

$$P_N = 2\int_0^{f_B} \mid i_{n,in}^2 \mid df \tag{5.6}$$

$$P_{N_1} = 2\int_0^{f_B} \mid i^2_{n,OTA_1} \mid df \tag{5.7}$$

P_{N_1} is the feed-forward opamp input referred in-band noise. In Fig. 5.3(b), the resetting switches (SW_1 and SW_2) are turned on for 10% of clock period while SW_3 opens the loop. Therefore, the noise from SW_1 does not contribute to input and noise from SW_2 is negligible because of low parasitic capacitance connecting the switch to ground. Therefore, in this switch configuration the feedback noise does not contribute to input. When SW_3 is closed as it is shown in Fig. 5.3(c), SW_1 and SW_2 are open, the loop is closed and the in-band noise can be calculated as shown below:

$$P_{N_2} = 2\int_0^{f_B} \mid \frac{v^2_{n,sw}(4\pi^2 f^2 C_2^2)}{1 + 4\pi^2 f^2 C_2^2 R^2_{on}} \mid df \tag{5.8}$$

P_{N_2} is the feedback switch, input referred, in-band noise.

$$P_{N_2} = \frac{(4KTR_{on})(2\pi f_B C_2 R_{on} - \tan^{-1}(2\pi f_B C_2 R_{on}))}{(2\pi C_2)R^3_{on}} \tag{5.9}$$

As C_2 is in the order of picofarads, R_{on} a few ohms and f_B in order of tens of KHz, $2\pi f_B C R_{on}$ is small, so equation (5.9) can be rewritten as:

$$P_{N_2} \approx \frac{(4kTR_{on})(2\pi f_B C_2 R_{on} - 2\pi f_B C_2 R_{on})}{2\pi C_2 R^3_{on}} \approx 0 \tag{5.10}$$

As shown above the switch noise has a negligible contribution to input noise.

$$P_{N_3} = 2\int_0^{f_B} \mid (\frac{C_2}{C_1})^2(\frac{4kT}{R_{DAC}} + i^2_{n,OTA_2}) \mid df \tag{5.11}$$

$$P_{N_3} = \left(\frac{C_2}{C_1}\right)^2 \left(\frac{8kT}{R_{DAC}} + 2i^2_{n,OTA_2}\right) f_B \tag{5.12}$$

$$P_{N_4} = 2\int_0^{f_B} \mid (1 + \frac{1}{sR_{DAC}C_1} sC_2)^2 e_{n,OTA_2}^2 \mid df \tag{5.13}$$

P_{N_3} is the in-band integral of feedback resistor and opamp current noise sources multiplied by the squared of the transfer function from the output of the flip-flop to the input. P_{N_4} is the in-band integral of the opamp voltage noise.

$$P_{N_4} = \frac{C_2^2(2\pi C_1 f_B R_{DAC} + 1)^3}{6\pi C_1^3 R_{DAC}^3} e_{n,OTA_2}^2 \tag{5.14}$$

Since the integrator is reset every cycle, proper operation requires $\frac{V_{ref}T_S}{R_{DAC}C_1} \ll V_{sup}$, where V_{ref} is the DAC reference voltage, $\pm V_{sup}$ is the supply voltage rails and $T_S = 1/f_s = 1/(2 \times OSR \times f_B)$ is the sampling clock period. The above equation can be simplified by relating V_{ref} and V_{DD} by a scale factor i.e. $V_{ref}/V_{sup} = \gamma$, where $\gamma \leq 1$. $R_{DAC}C_1 \gg \gamma/f_s$ This can be rewritten as $R_{DAC}C_1 = \frac{\beta}{f_s} = \frac{\beta}{2\times OSR\times f_B}$, where $\beta = k \times \gamma \gg 1$, a reasonable design choice is $\beta \geq 10$. So we can recast (5.14) as follows:

$$P_{N_4} = \frac{C_2^2(\pi\frac{\beta}{OSR} + 1)^3}{6\pi C_1^3 R_{DAC}^3} e_{n,OTA_2}^2 \tag{5.15}$$

$$P_{N_4} = \left(\frac{C_2}{C_1}\right)^2 \frac{(\pi\frac{\beta}{OSR} + 1)^3}{6\pi C_1 R_{DAC}^3} e_{n,OTA_2}^2 \tag{5.16}$$

Insight can be gained into (5.16) by assuming $\frac{\beta}{OSR} = \frac{1}{\pi}$, which is valid provided $OSR \geq 32$ yielding $\beta \geq 10$. (5.16) can then be further simplified as:

$$P_{N_4} = \left(\frac{C_2}{C_1}\right)^2 \frac{8}{3} \frac{e_{n,OTA_2}^2 f_B}{R_{DAC}^2} \tag{5.17}$$

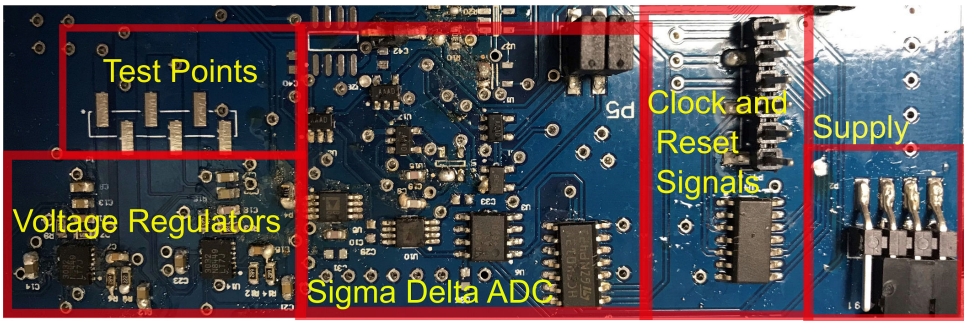

Figure 5.4: Proposed $\Delta\Sigma$ ADC PCB

If we want P_{N_4} to be minimal compared to the noise contributed by R_{DAC} then

$$\left(\frac{C_2}{C_1}\right)^2 \frac{8}{3}\frac{e_{n,OTA_2}^2 f_B}{R_{DAC}^2} \ll \left(\frac{C_2}{C_1}\right)^2 \frac{8kTf_B}{R_{DAC}} \tag{5.18}$$

$$e_{n,OTA_2}^2 \ll 3kTR_{DAC} \tag{5.19}$$

The α coefficient is implemented by choosing different values for C_1 and C_2 so that $C_1 = \alpha C_2$. Therefore, from (5.12) it can be seen that there is a $\frac{1}{\alpha^2}$ factor scaling both the opamp and resistor noise effectively reducing the noise contribution from the feedback path, assuming the input opamp noise is negligible compared to the resistor noise.

5.5 Experimental Results

In this section, measurement setup and results are shown. All the tests are done with a bilayer nanopore model.

5.5.1 Measurement Setup

The design was implemented on a 2-layer printed circuit board (PCB) with a dedicated ground plane. Fig. 5.4 shows the PCB setup. Coupling due to switching was avoided by ensuring separation of the analog and digital signals. Clock and reset signals

were applied to the PCB using an FPGA. ADC characterization was performed by applying a sine wave to the input via a signal generator. The output spectrum of the ADCs were recorded using a network analyzer and low-pass filtered. The proposed 1^{st} and 2^{nd} order $\Delta\Sigma$ ADCs were implemented with off-the-shelf components. The reference currents range between 1μA and 100 nA, corresponding to 10 nA and 100 pA LSB values, and can be adjusted via the feedback resistor value. A low pA input bias current opamp AD8610 was chosen for the integrators. The current noise density of these opamps is $5\frac{fA}{\sqrt{Hz}}$, low enough for pA resolution. The flip flop voltage is 5 V and using switches as a 1-bit DAC it is converted to $\pm$2.5V. In this implementation we chose α to be 10. The feedback resistor was then chosen utilizing the constraints of the voltage, scale factor and desired reference current, resulting in a 250 KΩ resistor. Considering the gain-bandwidth of the opamps, opamp feedback capacitor values of feed-forward and feedback opamps were chosen to be 10 pF and 40 pF ,respectively and the differentiator capacitor is designed to be $\frac{1}{10}$ of the resetting integrator feedback capacitor to yield the desired α.

5.5.2 Measurement Results

Both 1^{st} and 2^{nd} order $\Delta\Sigma$ ADCs were tested and Fig. 5.5-Fig. 5.7 show the dynamic range and output spectrum. According to (5.7)-(5.12), the total in-band noise for $1\mu A$ reference current with $R_{DAC} = 250K\Omega$, is equal to 200 fA_{rms}. As shown in Fig. 5.8, the measured noise floor, for the same reference current and R_{DAC}, is approximately $18\frac{fA}{\sqrt{Hz}}$. Therefore the measured in-band noise integrated over a 1 KHz bandwidth would be approximately 569 fA_{rms}, which is $369fA_{rms}$ larger than the theoretical value. This difference is due to lack of enough points in 1KHz bandwidth range according to Fig. 5.8 . Fig. 5.7 shows the in-band spectrum of the proposed $\Delta\Sigma$ ADC with a measured noise floor of about 70 dB and maximum noise value of about -62 dB. Table 5.1 compares prior

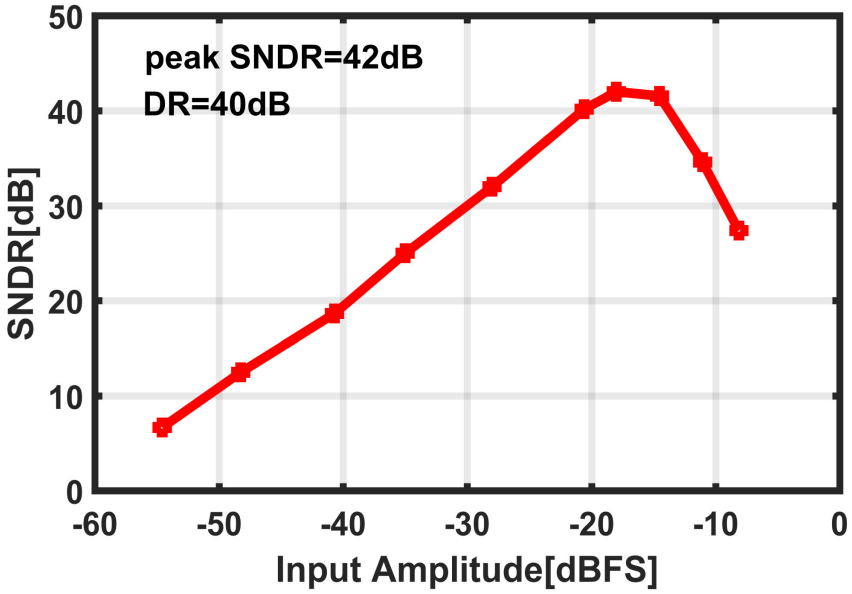

Figure 5.5: 1^{st} order DSM SNDR vs. input

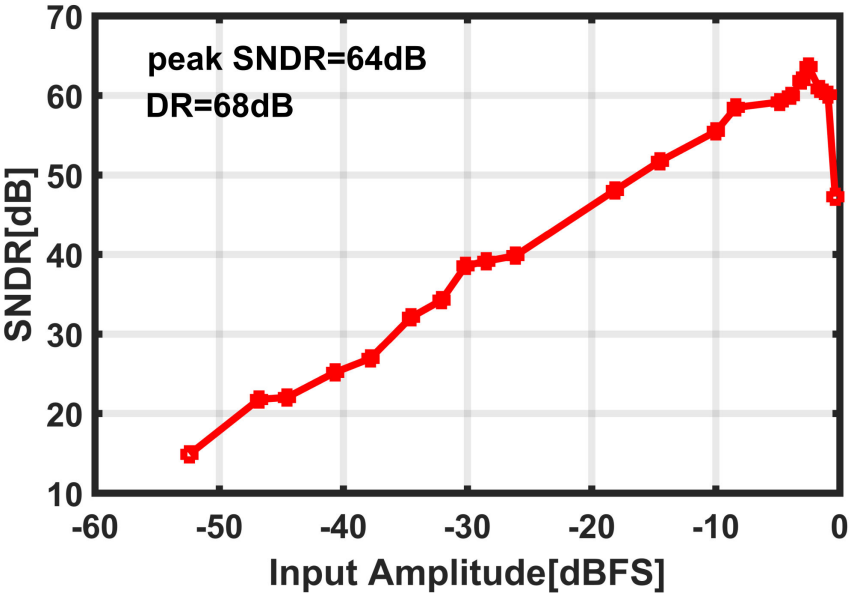

Figure 5.6: 2^{nd} order DSM SNDR vs. input

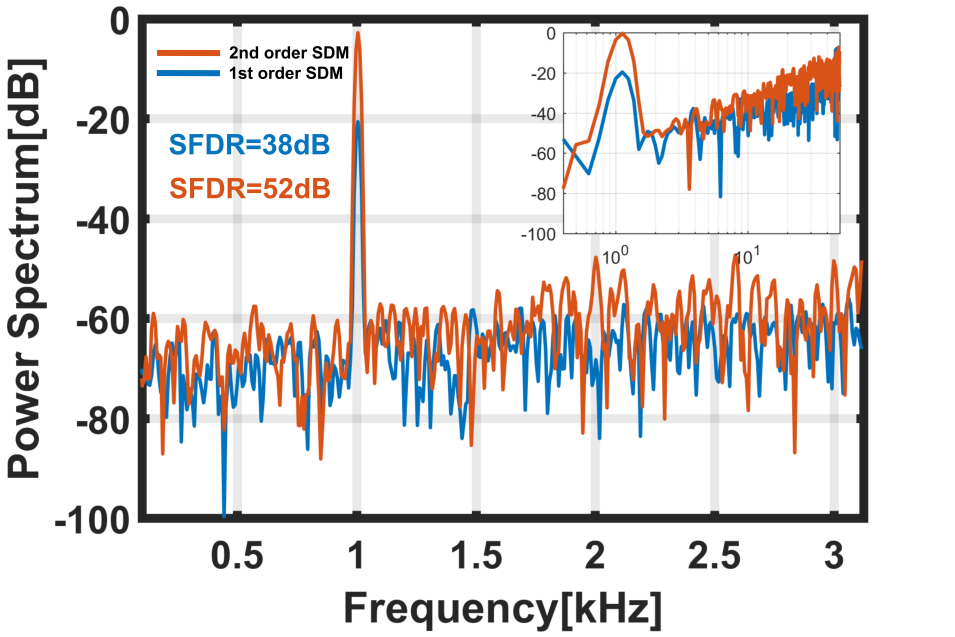

Figure 5.7: 1^{st} and 2^{nd} order DSM power spectrums for -20dB and full scale 1KHz input signal, respectively.

Table 5.1: Comparison with prior art

	[19]	*[73]*	*[18]*	***This work***
Technology[μm]	0.18	0.5	0.13	Discrete
Noise floor[A/$\sqrt{Hz}$]	10^{-14}	-	-	1.8×10^{-14}
Sensitivity[pA]	0.2	0.1	1	2.8[a]
(BW[Hz])	(400)	(0.1)	(-)	(1K)
max. BW[KHz]	1.8	4	5	6.25
f_s[MHz]	0.1	2	0.846, 8.46	0.2, 0.4

[a]Calculated.

arts to this work and shows the new architecture, even though is a PCB implementation rather than an integrated chip, performs competitively.

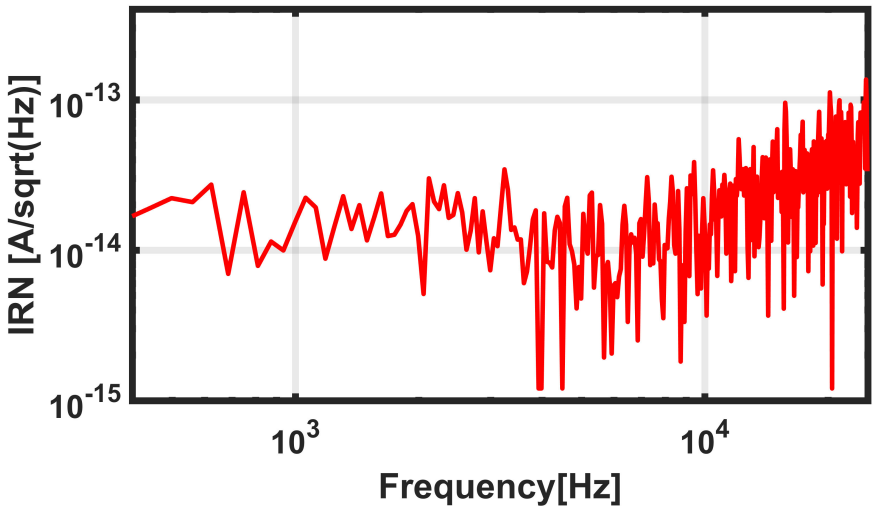

Figure 5.8: Measured data showing Input-Referred Noise (IRN)

5.6 Conclusion

We have presented a direct current-to-digital Delta-Sigma ADC and applied the proposed architecture to first and second order modulators. The idea behind this architecture is to reduce the noise contribution from the feedback so the dominant noise would be the feed-forward opamp noise. This architecture would be useful for sensitive low noise biosensing applications with pico-ampere current inputs. A comprehensive noise analysis was also included in this chapter. First and second order ADCs were implemented using off-the-shelf components on PCB to demonstrate the proof-of-concept. Measurement results are in excellent agreement with the theoretically calculated values.

Chapter 6

A Current Sensing ADC in 45 nm CMOS

6.1 Introduction

Single-molecule electronic biosensors require high-precision current sensing (∼1pA) with high bandwidth (∼1kHz) and dynamic range (∼10b). Higher data fidelity requires statistical averaging over a large number of sensors (10-100), placing severe constraints on the area per channel. Typical approaches require a TIA for each channel, with either capacitive [72, 74] or resistive feedback [75], followed by an ADC. Large TIA conversion gains (>140dbΩ) required for low current sensing limits the dynamic range of this approach. An alternative approach eliminates the need for the TIA and performs direct digital conversion using current-to-digital converters thereby overcoming this limitation. Direct analog to digital conversion using Continuous-Time Delta-Sigma modulators (CTDSM) have become increasingly popular replacements to the traditional analog sensor front ends in biosensing [76–78], neural recording [79, 80] and audio [81] applications. CTDSMs are gaining more attention due to their inherent anti-aliasing, thereby reducing complexity

compared to their discrete-time counterparts. Sensor interfaces typically use incremental DSMs due to their simple decimation filter, short latency, multiplexing feature and reduced idle tone power. Incremental CTDSMs combining the advantages of both techniques have become increasingly popular [76]. However, due to resetting of integrators and its nyquist-rate operation, using Incremental Analog to digital Converters (IADCs) has a noise penalty trade-off [82]. On the other hand, in CTDSMs, the input-referred noise and thus minimum input detectable is limited by the noise of its feedback Digital-to-Analog converter (DAC). Recently by using a 12-b SAR quantizer and a 11-b DAC a 140dB DR was achieved, since the noise of the DAC scales with the input signal [83]. However, this method comes at the expense of giving up the inherent linearity achievable in a 1-b quantizer and DAC increasing the area, complexity, and power of the converter. Also, slope-scaling techniques coupled with resistive feedback DAC can also reduce the noise from the feedback [76, 77]. This technique requires resetting to avoid saturation due to use of an integrator in the feedback. In [76], all integrators in DSM structure are reset and therefore resetting is employed in two configurations, one makes the structure act as an incremental CTDSM which is limited by the sampled reset noise and the other configuration is an CTDSM with an on demand reset which would contribute less noise but still because the resetting is done on all integrators in the structure, there would be noise contribution in reset times. This noise contribution from resetting is not a limitation with the structure proposed in [77]. In [77], only the integrator and differentiator are resetting and the loop is open in reset mode which makes the noise contribution from the reset switches be negligible. However, resistive feedback DAC has disadvantages when comes to chip level design.

Since, sensor interface designs are moving towards implementing massive parallel arrays which can be supplied with battery, it is important to consider low power and area efficient design along with high resolution and low noise.

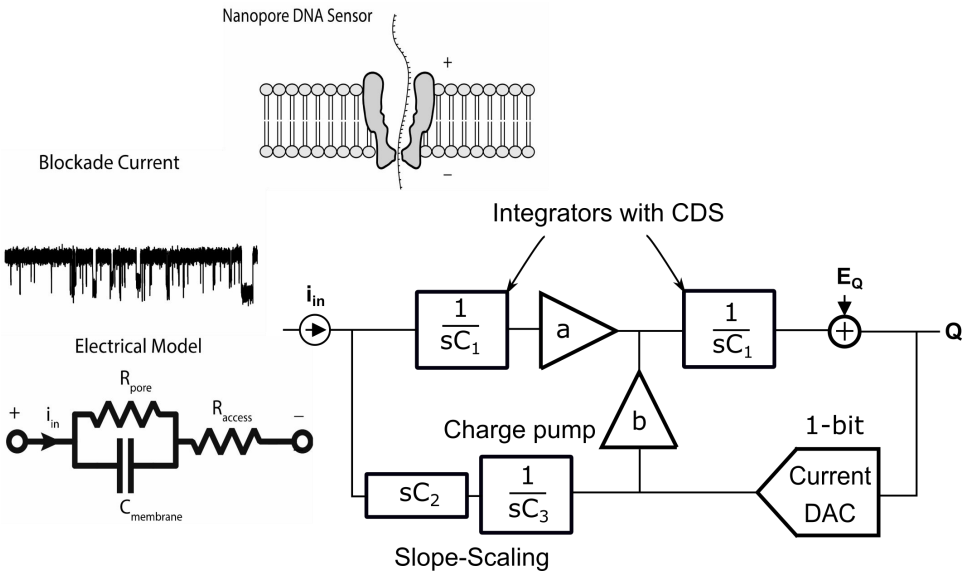

Figure 6.1: System block diagram

Our approach maintains the simplicity and linearity of the 1-b $\Delta\Sigma$ modulator while achieving 125dB cross-scale DR by using an advanced version of our current scaling method [77]. One major advantage of our $\Delta\Sigma$ approach is the ability to fold the TIA into the ADC via the first stage integrator.

Another is its insensitivity to process variations due to the feedback nature of the structure. Furthermore, it allows the use of lower gain amplifiers reducing area and power. We made the following modifications to a conventional second order $\Delta\Sigma$ modulator allowing us to directly sense sub-pA currents while using lower power and area: 1) A single stage common-source amplifier with a cascode load. 2) Feedback current scaling using capacitors (slope scaling, see Fig. 6.1) enabling low feedback DAC noise and thereby enabling sub-pA sensing. 3) Correlated double sampling (CDS) to lower amplifier noise and improve process variation tolerance while increasing amplifier gain [50]. Using these techniques, we achieved a sub-pA current sensing ADC.

The proposed CTDSM architecture is introduced in Section 6.2. The details of circuit

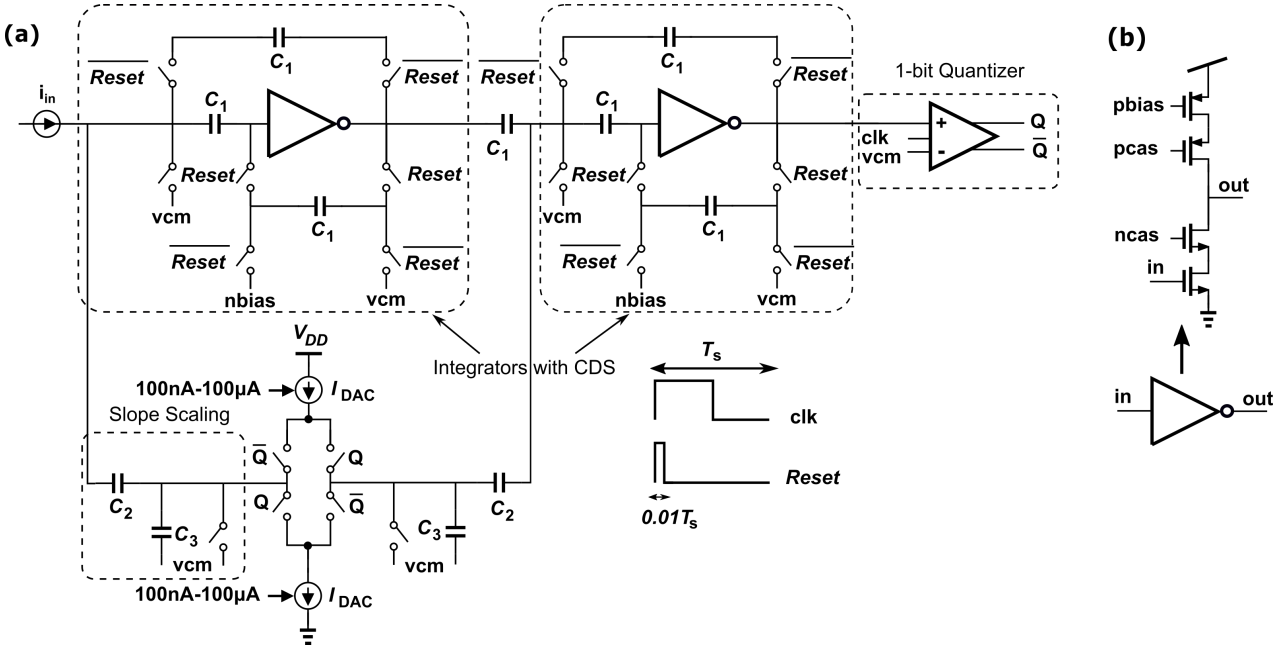

Figure 6.2: (a) CT-DSM current-sensing structure (b) Single-stage amplifier design

level implementation of each block in the system with a comprehensive noise analysis is given in Section 6.3. The total input-referred noise is analyzed in Section 6.4. In Section 6.5, the chip measurement results are discussed and in Section 6.6, the work is concluded.

6.2 Proposed CTDSM Architecture

This section introduces the system level design of the proposed CTDSM structure. Fig. 6.1 shows the block diagram of the proposed wide bandwidth high precision current sensing ADC front-end. As it is illustrated, the proposed structure is a 2^{nd} order continuous-time Delta Sigma ADC with 1 bit current-source based DAC in the feedback which uses slope scaling technique. Fig. 6.1 also shows the slope scaling technique implemented in the feedback path, which converts the output of the current DAC into a

voltage ramp via an integrator and then back into a current using a differentiator. This technique allows the scaling of the DAC current by the ratio of the integrator and differentiator capacitors. More importantly it eliminates the need for large-valued resistors normally required to lower the feedback current noise. Additionally, unlike switched capacitor feedback DACs it allows the use of small capacitors since the size does not set the integrator gain.

The coefficients of this CTDSM is designed from discrete time transfer function and conversion to continuous-time such that the modulator would be stable.

As shown, integrators with CDS structure are used in feed-forward path and a charge pump is used as the slope-scaling integrator in the feedback. Although, this is a fully continuous-time design, no resistor is used in the structure thanks to techniques used, therefore it is a fully capacitive design.

Fig. 6.1 also shows the electrical model for nanopore sensor.

6.3 Circuit Implementation

In this section, circuit design of each block in the proposed CTDSM is introduced. Fig. 6.2(a) shows the circuit level implementation of the proposed CTDSM. There are two main feed-forward integrators in CTDSM structure and one feedback integrator which in our case have different implementations. We will introduce the novel structures used for these integrators. We will describe our current-source based DAC with slope-scaling technique in the feedback. We will also show the comparator structure used in this work.

6.3.1 Main Integrators

One of the most critical circuits in DSM is the integrator specially for low power and area efficient applications. Usually, two to three stages of OTA is used for the first

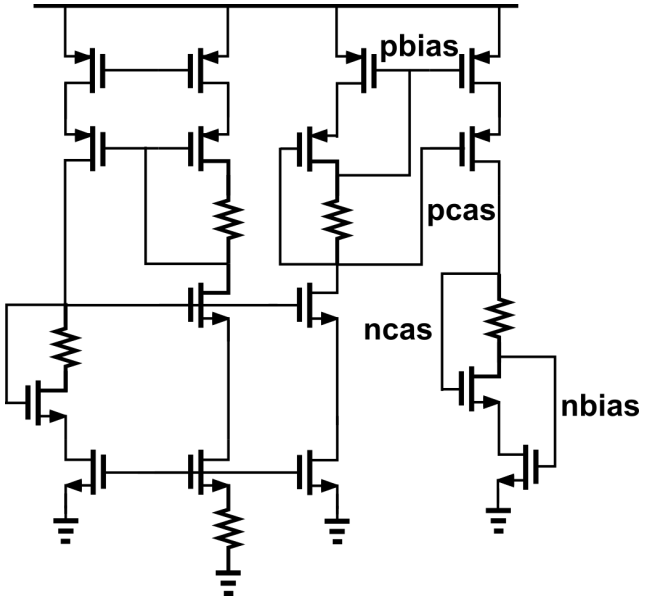

Figure 6.3: Circuit implementation of amplifier bias network

integrator in the DSM structure so that it would achieve a high DC gain (80 to 100dB) in order to reduce the non-linearities. However, such OTA would consume so much power that would not be suitable for massive arrays of DSM. To mitigate the issues with power hungry OTAs, and achieving a high DC gain at the same time, inverter-based opamps with correlated double sampling have been utilized before [50]. The CDS technique, samples slow varying (1/f) noise and amplifier offset, improving the gain and lowering the noise. These kind of structures consume much less power and area while achieving high DC gain and good linearity due to the CDS technique. A novel correlated double sampling single stage integrator is used as main integrators in our DSM structure. The simple single stage implementation allows for lower area and power. We will introduce our proposed CDS structure in this system next.

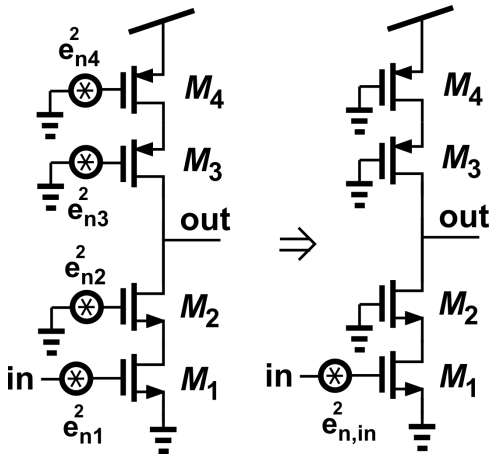

Figure 6.4: Circuit implementation of amplifier bias network

Amplifier

The single stage amplifiers are common-source amplifiers with cascode loads, as shown in Fig. 6.2(b). The bias network shown in Fig. 6.3 is designed such that it would bias the amplifier transistors at moderate inversion to achieve higher gain. Our current design is an amplifier with $\sim$ 40 dB gain effectively working as an amplifier with $\sim 80dB$ gain due to CDS enhancement. One of the dominant noise sources contributing to input-referred noise is amplifier noise. Fig. 6.4 shows the noise sources present in the amplifier. Therefore, the amplifier noise is calculated as below:

$$e_{out}^2 = (g_{m1}R_{out})^2 e_{n_1}^2 + (g_{m4}R_{out})^2 e_{n_4}^2 \tag{6.1}$$

In (6.1), the cascode transistors are not included due to their negligible noise. Gain of the amplifier is equal to $A_v = g_{m1}R_{out}$. Therefore, the input-referred noise is derived as:

$$e_{n,in}^2 = \frac{e_{out}^2}{A_v^2} = e_{n_1}^2 + (\frac{g_{m4}}{g_{m1}})^2 e_{n_4}^2 \tag{6.2}$$

$$e_{n,i}^2 = \frac{4kT\gamma}{g_m} \tag{6.3}$$

Where i represents transistor number. If $g_{m1} = g_{m4} = g_m$, then noise from each device contributes directly to the input-referred noise:

$$e_{n,in}^2 = e_{n,1}^2 + e_{n,4}^2 = \frac{8kT\gamma}{g_m} \tag{6.4}$$

Therefore, input-referred current noise would be:

$$P_{N1} = \int_0^{f_B} (1 + \frac{C_{in}}{C_1})^2 e_{n,in}^2 (2\pi f C_1)^2 \, df \tag{6.5}$$

Where C_{in} is the sensor input capacitance.

$$P_{N1} = \int_0^{f_B} (1 + \frac{C_{in}}{C_1})^2 \frac{8kT\gamma}{g_m} (2\pi f C_1)^2 \, df \tag{6.6}$$

$$P_{N1} = (1 + \frac{C_{in}}{C_1})^2 \frac{8kT\gamma}{g_m} \times 4\pi^2 C_1^2 \int_0^{f_B} f^2 \, df \tag{6.7}$$

$$P_{N1} \cong (1 + \frac{C_{in}}{C_1})^2 \frac{32\pi^2 (kT)\gamma}{g_m} C_1^2 (\frac{f_B^3}{3}) \tag{6.8}$$

Floating Correlated-Double-Sampling

Correlated double sampling is a popular technique in CTDSMs when decreasing noise and non-idealities are crucial [84]. A novel floating correlated double sampling single stage integrator is used as main integrators in the DSM structure shown in fig. 6.2(a). Fig. 6.5 shows the cds integrator in integrate and reset phases. As is shown in reset phase offset,

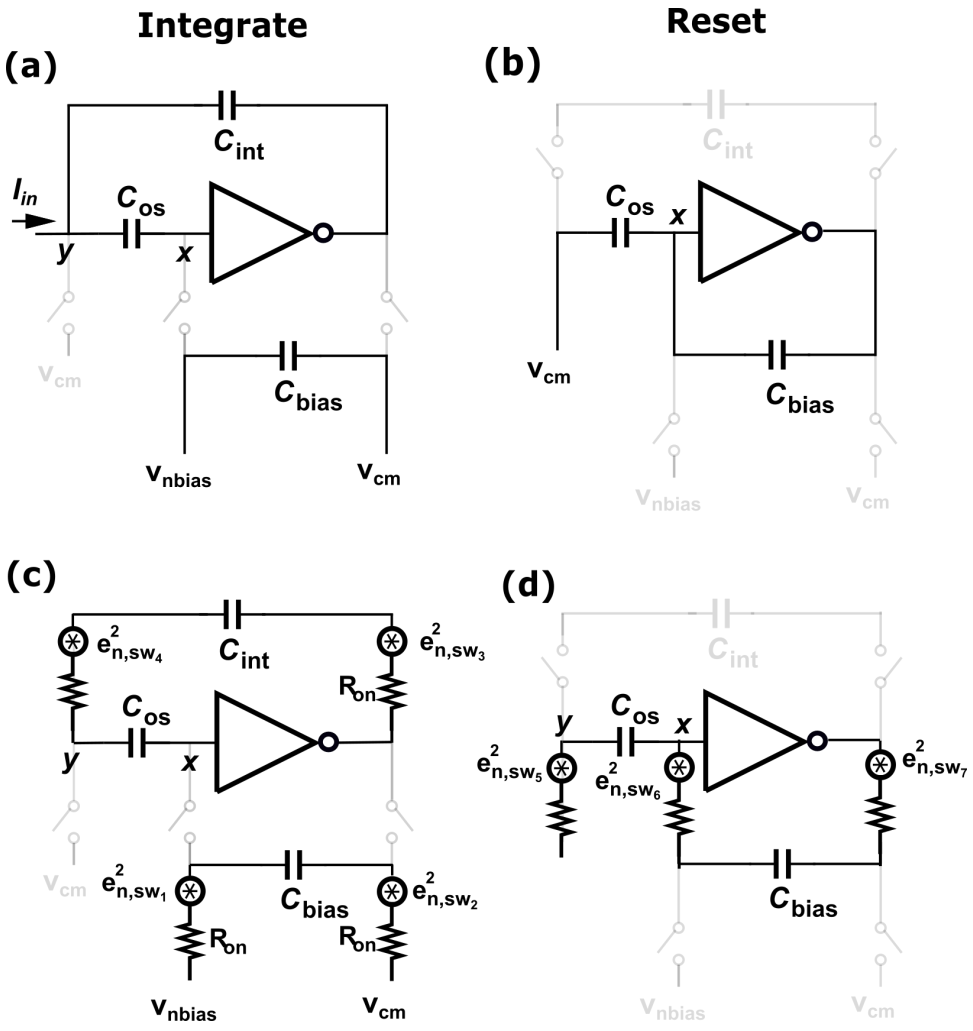

Figure 6.5: (a) CDS integrator in integration phase (b) CDS integrator in reset phase (c) Amplifier noise (d) Feedback noise in integrate and reset phases amplifier design

flicker noise and switch noises are getting sampled at x and y nodes and in integrate phase, offset is stored in the capacitor and gets cancelled out making y node act as a virtual ground.

One important element is the noise contribution of the cds circuit to the input. Fig. 6.5(c) and (d) show the noise sources present in integrate and reset phases, respectively. Since in integrate phase, C_{bias} is floating, the $\frac{kT}{C}$ noise that it picks up in reset and integrate phase, doesn't contribute to the input. In integrate phase since y becomes a virtual ground due to CDS offset cancellation, the noise from sw_4 will have negligible contribution to the input referred current noise and in reset phase the noise that C_{os} picks up from sw_5 in $0.01T_s$ gets averaged out in integrate phase and becomes negligible.

6.3.2 Feedback DAC

There are generally three different DAC structures used in a CTDSM, resistive DAC, current-source DAC and Switched-Capacitor (SC) DAC. SC DACs reduce the sensitivity to clock jitter at the price of putting a higher demand on main integrator linearity. Also, the inherent anti-aliasing filtering for these DACs is limited, requiring designing a filter which increases the complexity and power. Therefore, this kind of DAC would not be suitable for our structure specially because decreasing power and area are one of the main goals of our proposed CTDSM. As was discussed previously, since the noise from DAC in CTDSM is limiting the minimum detectable signal, slope-scaling technique is being used. Previously, this technique only has been implemented with resistive DACs [76, 77]. In this work, we implemented the technique with a current-source based DAC. In general, resistive DACs put a stricter demand on first main integrator linearity due to resistive loading at the virtual ground reducing the loop gain. Also, high resistivity polysilicon resistors are not available in all processes, and even if they are, generating small nA

reference currents require GΩ resistors which can be reduced to MΩ by using slope-scaling technique. However, it is still consuming much more area than a simple current-source based DAC. Although, resistive DACs are usually used for their intrinsic low flicker noise, designing a high PSRR and low flicker noise reference for resistive DAC would consume extra power and area. A current steering DAC (I-DAC) in opposite has intrinsic PSRR and with the slope scaling technique the flicker noise would be a non-dominant factor. The other benefit of current source based DAC is that its full scale can be tunable using the bias voltages. Thus, since area and power are key factors in our design we chose current source based DAC specially because its combination with the slope scaling technique would give us added benefit of further simplifying the feedback integrator circuit implementation which we will discuss next.

Feedback Integrator

The feedback integrator required for slope-scaling reduces to a charge pump while the associated differentiator is simply a capacitor since one end is held at virtual ground by the input integrator. A differential charge pump allows for robust performance while providing the feedback signal with opposite signs making it convenient to feedback to both the first and second stage of the 2^{nd} order DSM. Additionally, resetting the charge pump-based integrator is fast due to its feed-forward nature and only depends on the switch resistance. The fast reset times allows our design to use a relatively small fraction (1%) of the clock cycle for reset mitigating any deleterious effects posed by long reset times. Fig. 6.7 shows the noise sources in the feedback and the current scaling capacitors. Current scaling is achieved by the ratio (α) of capacitors C2 and C3, i.e.,

$$\alpha = \frac{C_3}{C_2} \tag{6.9}$$

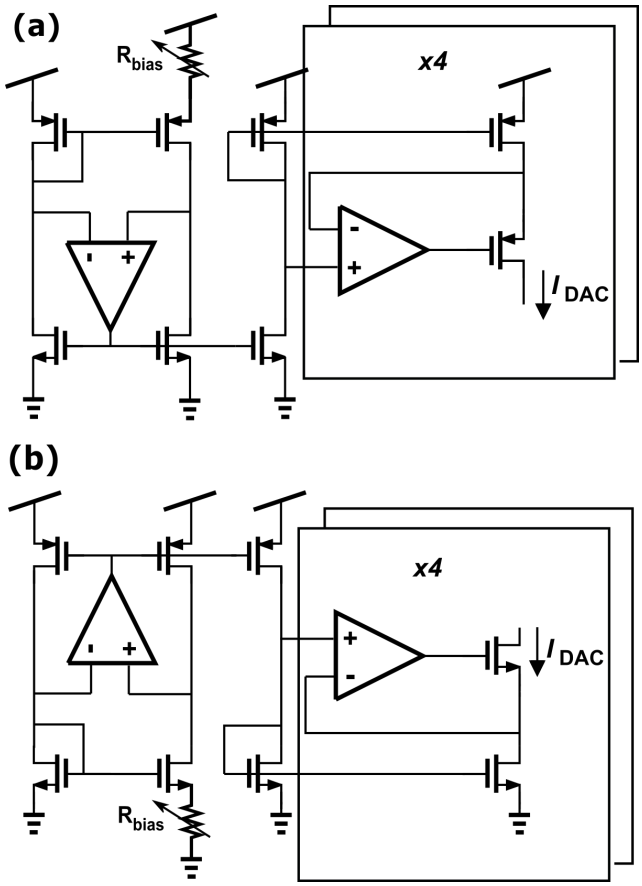

Figure 6.6: (a) positive current source (b) negative current source

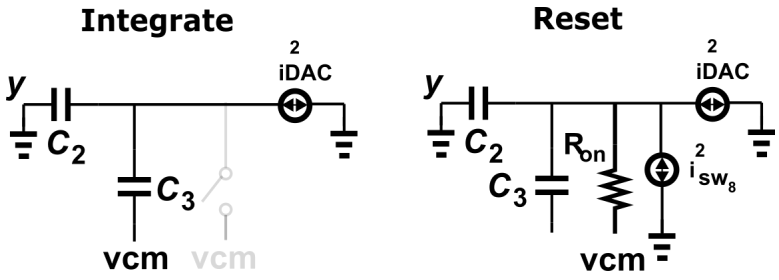

Figure 6.7: (a) positive current source (b) negative current source

The switch resetting the integrator has a current noise equal to:

$$i_{sw_8}^2 = \frac{4kT}{R_{on}},\ e_{sw_8}^2 = 4kTR_{on} \tag{6.10}$$

To find the charge pump reset noise contribution to the input-referred noise, we only assume switch noise is present in the model provided in Fig. 6.7, so it would simplify to a current noise source and C_2, C_3 and R_{on} in parallel. Since the reset time is $0.01T_s$, therefore the noise contribution from the switch noise to the input current noise is negligible [85].

The resetting nature of the design eliminates the need for using resistors and allows for the use of a completely capacitive CT-$\Delta\Sigma$ design.

Current source based DAC

Current DAC is designed such that it would be applicable to arrays of sensors. In this chip, a prototype for an array of 4 sensors is implemented. In this case, two tunable sub-threshold current sources are designed as illustrated in Fig. 6.6. Fig. 6.6(a) shows the positive current reference and Fig. 6.6(b) shows the negative current reference. At all times one is flowing into the feedback path to the input and one to the other path to the second feed-forward integrator. The voltage bias of the current source is routed out through the chip and 4 copies of the reference current is mirrored into each DSM. This DAC with increasing the number of sensors would not add much power to the system since it just adds up more current mirror branches. Fig. 6.7 shows the noise sources from feedback. In Section 6.3.2, switch noise is calculated, now we will calculate the feedback noise contribution to the input-referred noise assuming only current DAC is present. In integrating phase, as shown in Fig. 6.7 the current DAC noise is getting scaled by the

capacitor scaling factor of (6.9). Therefore:

$$P_{N3} = \int_0^{f_B} \frac{1}{\alpha^2} i^2_{n_{DAC}} \tag{6.11}$$

where $i^2_{n_{DAC}}$ is the noise of the 1-b current DAC. Since the reference current in the DAC is scaled up by a factor of α to maintain the right full-scale range and noise power scales linearly with the bias current, the net noise power is reduced by α compared to a conventional approach. This α scaling allows a larger bandwidth for the same noise level. Since the 1-bit current DAC is in sub-threshold due to its small current reference, the current noise source will be equal to:

$$i^2_{n_{DAC}} = 2qI_{DAC} \tag{6.12}$$

where I_{DAC} is the DAC reference current. Therefore P_{N2} calculates as:

$$P_{N3} = \frac{1}{\alpha^2}(2qI_{DAC}f_B) \tag{6.13}$$

As in Section 6.3.2, current DAC noise contribution to the input in reset phase would be negligible.

6.3.3 Comparator

The comparator designed is shown in Fig. 6.8. A strong arm latch with two pre-amplifier stages are designed to further reduce quantizer's possible errors for sub-pA current sensing. Comparator is consuming most of the power in this proposed CTDSM.

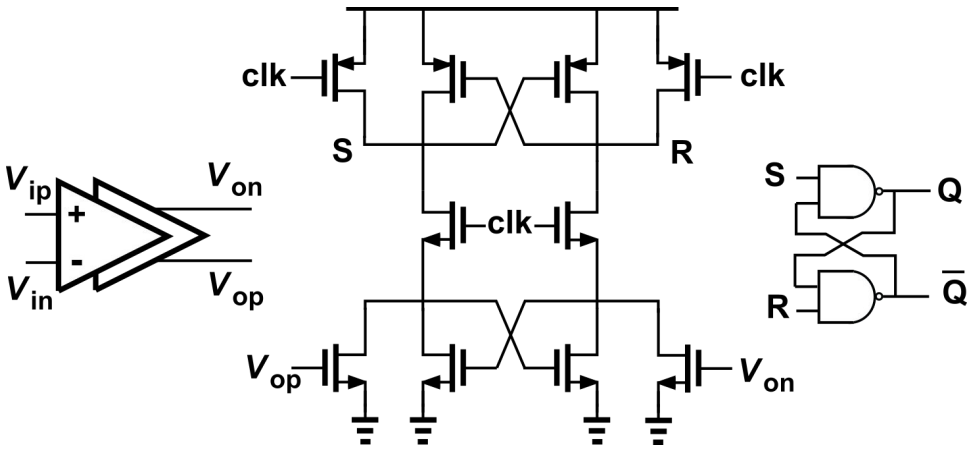

Figure 6.8: Circuit implementation of latched comparator

6.4 Noise Analysis

The input referred noise of the system consists of two parts, noise coming from the feedback and noise from the first main integrator. As discussed in 6.3.1, the only noise contributing to total noise from first main integrator, is amplifier noise and the feedback noise consists of the reset switch noise and current DAC noise sources. Therefore:

$$P_{N_t otal} = P_{ff} + P_{fb} \tag{6.14}$$

where P_{ff} is feed-forward noise spectral density and P_{fb} is feedback noise spectral density. From (6.8), the total feed forward noise is:

$$P_{ff} = P_{N2} = (1 + \frac{C_{in}}{C_1})^2 \frac{32\pi^2(kT)\gamma}{g_m} C_1^2 (\frac{f_B^3}{3}) \tag{6.15}$$

From (6.13), the total feedback noise is:

$$P_{fb} = P_{N3} = \frac{1}{\alpha^2}(2qI_{DAC}f_B) \tag{6.16}$$

Therefore, the total spectral noise density can be written as:

$$P_{N_{total}} = \frac{32\pi^2(kT)\gamma(1+\frac{C_{in}}{C_1})^2}{g_m}C_1^2(\frac{f_B^3}{3}) + \frac{1}{\alpha^2}(2qI_{DAC}f_B) \tag{6.17}$$

To further simplify (6.17), we substitute f_B with $\frac{f_s}{OSR}$:

$$P_{N_{total}} = \frac{32\pi^2(kT)\gamma(1+\frac{C_{in}}{C_1})^2}{g_m}C_1^2(\frac{f_s^3}{3OSR^3}) + \frac{1}{\alpha^2}(2qI_{DAC}\frac{f_s}{OSR}) \tag{6.18}$$

In (6.18), g_m has to be designed such that enough settling time is provided during reset. Assuming d to be duty cycle, and 5 times time constant needed for 99% settling, opamp bandwidth has to be larger than df_s, therefore:

$$\frac{g_m}{2\pi C} > \frac{df_s}{5} \tag{6.19}$$

Where C is the output capacitance of the opamp which is equal to C_1 in reset phase. Substituting g_m with (6.19), (6.18) simplifies to:

$$P_{N_{total}} = \frac{80(1+\frac{C_{in}}{C_1})^2\pi(kT)\gamma}{d}C_1(\frac{f_s^2}{3OSR^3}) + \frac{1}{\alpha^2}(2qI_{DAC}\frac{f_s}{OSR}) \tag{6.20}$$

From (6.20), there are several degrees of freedom to reduce the total noise, including sampling frequency, oversampling ratio, duty cycle, capacitor value and scaling factor to satisfy the equation. However there are limitations for the capacitor values which also limits the scaling factor. Also, since we want the circuit to be reset in a very short time so it is still operating as continuous-time ADC, there are limitations for duty cycle too. Now, due to slope scaling I_{DAC} is actually set α times larger than the reference current. If we set I_{DAC} less than 1μA translating to 10nA reference current for the modulator, current DAC would be in subthreshold region and (6.20) will hold. However, if I_{DAC} is

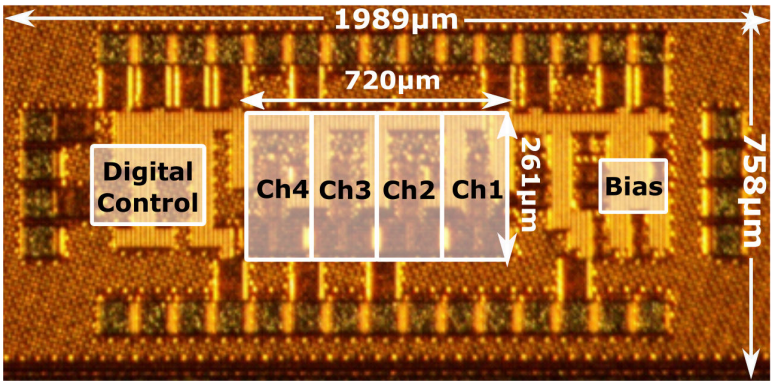

Figure 6.9: Chip micrograph

set for currents larger than 1μA, the 1-bit DAC would not be in subthreshold anymore and (6.12) would be changed to:

$$i^2_{n_{DAC}} = 4kT\gamma g_{m_{DAC}} \tag{6.21}$$

Therefore (6.18) will be changed to:

$$P_{N_{total}} = \frac{32\pi^2(kT)\gamma(1+\frac{C_{in}}{C_1})^2}{g_m} C_1^2(\frac{f_s^2}{3OSR^2}) + \frac{1}{\alpha^2}(4kT\gamma g_{m_{DAC}}) \tag{6.22}$$

Further simplifying to:

$$P_{N_{total}} = \frac{80\pi(kT)\gamma(1+\frac{C_{in}}{C_1})^2}{d} C_1(\frac{f_s^2}{3OSR^3}) + \frac{1}{\alpha^2}(4kT\gamma g_{m_{DAC}}) \tag{6.23}$$

6.5 Measurement Results

The current design was implemented in a 45nm RF SOI process. Chip micrograph is shown in fig. 6.9. As it is shown, the area occupied by 1 channel is (261μm $\times 161\mu$m). A variable reference current source (100nA- 100μA) is designed to serve as the 1-b cur-

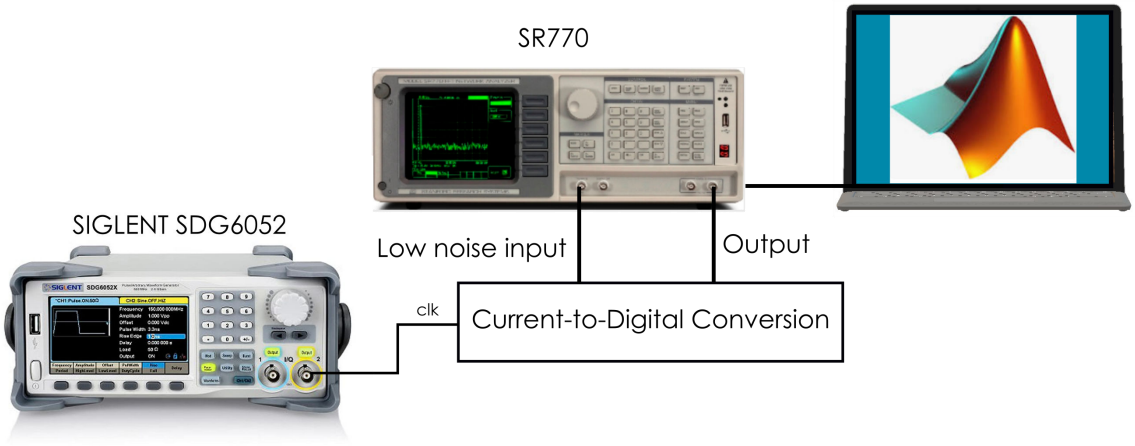

Figure 6.10: Measurement setup

rent DAC in the $\Delta\Sigma$ feedback. In the current design we chose α=100, with C_1=400fF, C_2=100fF and C_3=10pF, giving us a net reduction in current noise by a factor of 10, enabling sub-pA sensing at higher bandwidths. The measurement results reported here are for a reference current of 3nA which with α=100, translates to a DAC current of $0.3\mu A$. Therefore, the DAC operates at subthreshold. In the measurement results shown we chose the oversampling frequency of 1.024MHz, and Duty cycle d is also chosen to be 100. With these design values, the feed-forward input-referred noise from (6.20) is dominant.

Therefore with the proposed integrator structure, the noise from opamp is reduced. Moreover, the noise from feedback is reduced 10 times. Therefore, unlike conventional structures, in the proposed structure the feed-forward noise is dominant making feedback noise negligible.

In order to test the chip, a low noise test PCB with nanopore circuit model shown in Fig 6.1 is designed. To reduce the noise from the environment and external signals, an RF shield is used on top of the chip on PCB which is soldered and connected to

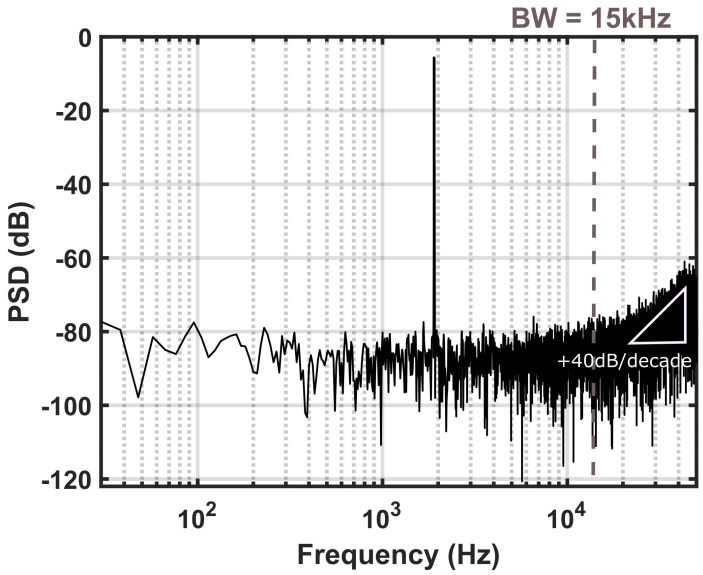

Figure 6.11: Measured 2_{nd} order DSM spectrum with -5 dBFS at 1.9kHz input

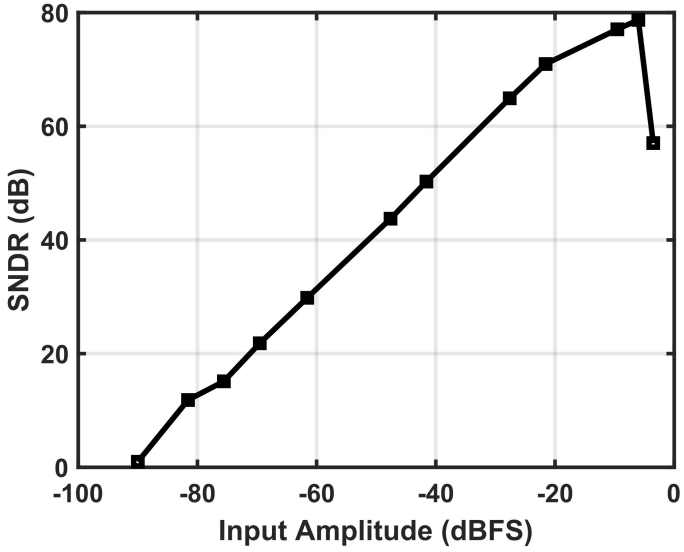

Figure 6.12: Measured SNDR versus input level

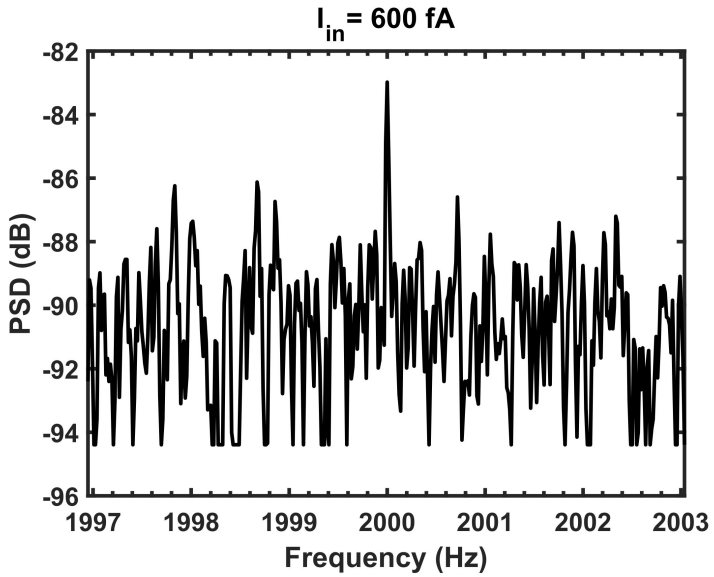

Figure 6.13: Measured minimum detectable signal at 2kHz input frequency

PCB ground plane. The input signal is applied as sine wave from a signal generator and the spectrum is measured in SR770 spectrum analyzer. For 0.6pA current measurement, the signal generators are too noisy. Therefore, low noise SR770 is also used as input for small current measurements as shown in Fig. 6.10. Combining all the enhancements yielded explained through the chapter, a current sensing ADC with an 80dB SNDR in a 4kHz signal bandwidth with an oversampling frequency 1.024MHz and an extended signal bandwidth of 15 kHz with 72dB SNDR, as shown in Fig. 6.11. The SNDR performance for the complete signal range is shown in Fig. 6.12. The sub-pA sensing capability is shown in Fig. 6.13, the result is for a 600fA signal at 2kHz. The performance of the current sensing ADC translates to an FoM of 153dB. The ADC achieves this performance while consuming only 125μW per channel, with a 1V supply. The breakdown of the power is shown in Fig. 6.14, with the comparator consuming the most power.

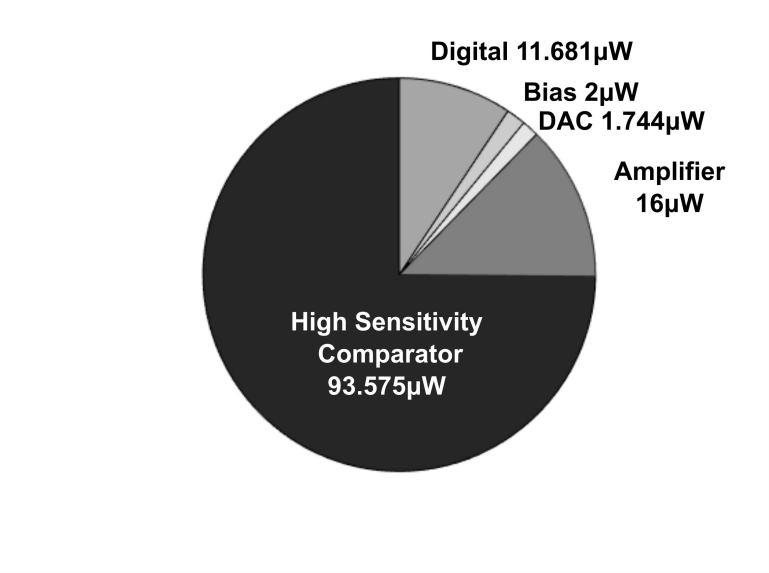

Figure 6.14: Power breakdown

6.6 Conclusion

To the knowledge of authors this is the first structure using current source based DAC with slope-scaling technique. Applying several techniques to the CTDSM including slope scaling, CDS and using charge pump as feedback integrator, lead to designing a sub-pA high bandwidth current-sensing ADC. Thanks to those techniques, implementing a power efficient and compact (261μm$\times161\mu$m) ADC was possible which makes it suitable for scalable designs. Our ADC is the smallest current sensing front-end reported (see Table 6.1) while achieving excellent current-bandwidth measurement results.
As shown in fig. 6.13 and fig. 6.15 and Table 6.1, our design achieves superior performance when area, power and signal bandwidth are critical.

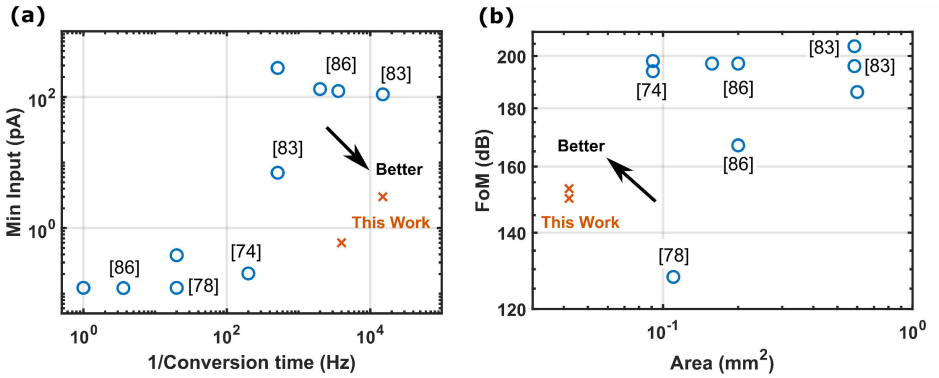

Figure 6.15: (a) Minimum input versus conversion frequency (b) Figure of Merit (FoM) vs area

Table 6.1: State-of-the-art

	[76]	[86]	[83]	[87]	**This Work**
Technology (nm)	350	180	55	180	**45nm CMOS**
Technique	Scaling	ADSM	Preset	$3^{rd} order$	**Scaling**
DAC type	Resitive	Current	Resistive	Switch-cap	**Current**
Bandwidth (Hz)	10K	3.6k	15K	10k	**15K**
Area (mm^2)/ch.	0.63/0.32	0.2	0.585	0.49	**0.042**
Power (mW)/ch.	6.73/4.6	0.295	1.011	1.7	**0.125**
Sensitivity (pA)@BW (Hz)	-	0.1@3.6	25@4k	0.314@100	**0.6@4k**

Chapter 7

Conclusion and Future Work

In this dissertation, our focus is on designing compact high performance CMOS VLSI circuits with low power consumption. This effort have been demonstrated for chip-to-chip electronic photonic transceivers in data centers and DNA sequencing as biological applications.

7.1 Electronic-Photonic Integration

In this dissertation, we proposed a transceiver system with circuit and system level novelties for electronic-photonic integration to be used in data center chip to chip interconnects. The system is demonstrated and implemented in 22nm FDX. The system is microring resonator based, therefore a scalable control loop is also implemented in TSMC 65nm to maintain stable locking of the rings.

7.1.1 High Speed Transceiver

Two different implementations of the transceiver is demonstrated for two different densities. The focus of the design is on achieving high performance as reducing power

and area consumption. First we proposed a system for the desired specifications. Since the data transmission is done at 26Gb/s data rate for 40 modulators (1Tb/s data totally), operation of the system at 26GHz is extremely power consuming mainly due to the clock distribution between 40 modulators. Therefore, 3GHz clocks are only used in the system to satisfy the power requirement and instead novel structures have been proposed so that the only power consuming parts of the system would be TIA and modulator driver which have to operate at 26GHz bandwidth.

As future extension of this work, since PRBS checker structure used in this dissertation has extra 32 flip flops it suffers from large area consumption, therefore, new designs for PRBS checker can be used to reduce power and area.

7.1.2 Control loop

As the system is micro ring modulator based, it is susceptible to temperature and process variations. In this dissertation, different structures for wavelength tuning and stable locking of the rings is proposed. First we discuss discrete implementation of an open loop heater driver for wavelength tuning of the rings and characterization. The implementation of an open loop heater driver results are demonstrated. Next, we proposed a closed loop heater driver for wavelength tuning and locking stabilization of the rings which is implemented in TSMC 65nm. Since 20 arrays of the loop was required on the chip, area consumption was of importance and one of the area consuming parts of the system is the TIA, therefore a current comparator is proposed for the front-end which is compact and power efficient.

Alternatively another novel $\Delta\Sigma$ assisted loop is proposed which utilizes a $\Delta\Sigma$ ADC to convert the photodiode current directly to digital and filters through a stochastic filter. These loops have been designed for both thermal tuning of the rings which is a current

driver and EO tuning of the rings which is a voltage driver. A new EO driver has also been proposed which enables 6v swing in low voltage process. Further power optimization of control loops can be conducted as future extension of the work.

7.2 Biological Applications

In this dissertation, one of the efforts was on designing compact, power efficient current sensing circuits for sub-pA detection in larger bandwidths (KHz range). First, we investigated different nanopore sensor requirements and review different current sensing structures which developed throughout years. We developed a design methodology which enables the designer to choose the proper design according to their application requirements. We further developed the design methodology to direct current to digital conversion using $\Delta\Sigma$ ADCs and choosing the proper configuration.

Further pushing the design limitations, we proposed a new $\Delta\Sigma$ direct current to digital conversion structure which we simulated in MATLAB and Altium. Implemented it on PCB and tested with off-the-shelf components and demonstrated the results which enabled sensing of pA currents in KHz bandwidth.

Next, we implemented the idea on chip in 45nm SOI process to miniaturize the structure and for showing its scalability 4 channels have been implemented. More novel ideas have also implemented in the integrated circuit to further reduce the area, power and sensitivity. The measurement results with a nanopore model are demonstrated.

Appendix A

Appendix

A.1 PRBS Checker Error Calculations

Fig. A.1 shows the topology of a (2^5-1) bit PRBS checker with solved error problems of the conventional ones [23]. Similar topology but with an extension to $(2^{31}-1)$ bit PRBS checker is used in this dissertation. The output of the checker of Fig. A.1 is calculated in following equations for the case that there is an error in the input to show only the error existed at the input appears at the output unlike conventional structures [23]. The same calculations can be extended to $(2^{31}-1)$ bit PRBS checker. In following equations, D, S and E represent data, signal and error, respectively. Based on the (2^5-1) bit PRBS polynomial:

$$D_0 = D_3 + D_5 \tag{A.1}$$

Therefore, signal at node A, C, E, F, G, H, J, L, M, N, and O are calculated to be:

$$S_A = D_1 + E_1 \tag{A.2}$$

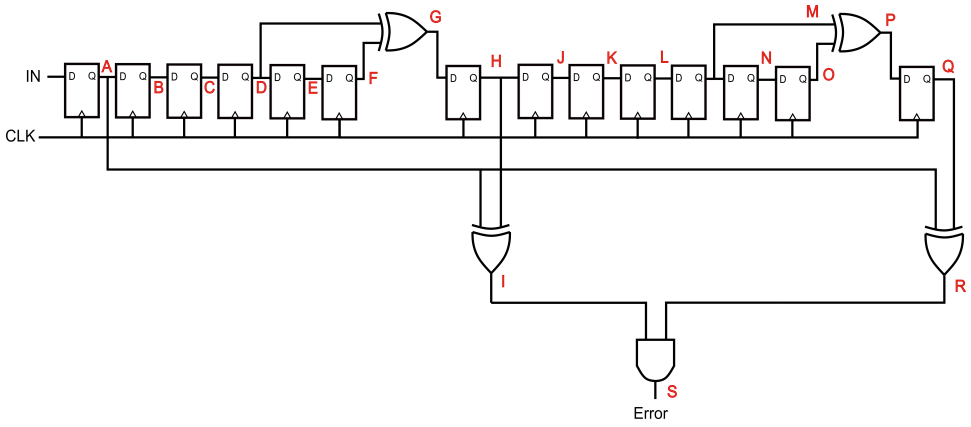

Figure A.1: $(2^5 - 1)$ bit PRBS checker

$$S_C = D_3 + E_3 \tag{A.3}$$

$$S_E = D_5 + E_5 \tag{A.4}$$

$$S_F = S_C + S_E = D_0 + E_3 + E_5 \tag{A.5}$$

$$S_G = D_1 + E_4 + E_6 \tag{A.6}$$

$$S_H = S_A + S_G = D_1 + E_1 + D_1 + E_4 + E_6 \tag{A.7}$$

$$S_J = D_3 + E_6 + E_8 \tag{A.8}$$

$$S_L = D_5 + E_8 + E_{10} \tag{A.9}$$

$$S_M = S_J + S_L = D_0 + E_6 + E_{10} \tag{A.10}$$

$$S_N = D_1 + E_7 + E_{11} \tag{A.11}$$

$$S_O = S_A + S_N = D_1 + E_1 + D_1 + E_7 + E_{11} \tag{A.12}$$

An AND operation is applied to the two signals at nodes I and R to output the error at S node which is:

$$S_S = S_I S_R = (E_1 + E_4 + E_6)(E_1 + E_7 + E_{11}) \tag{A.13}$$

$$S_S = E_1 \tag{A.14}$$

Therefore, only the error at the input shows up at the output unlike the conventional structure that 3 errors would have appeared [23].

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