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Architecture and Control of An Interleaved 6-Level Bidirectional Converter With an Active Energy Buffer for Level-II Electric Vehicle Charging

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***Abstract*—On-board electric vehicle (EV) chargers convert grid ac voltage to dc voltage to charge a high-voltage battery pack. High efficiency and high power density single-phase ac-dc converters are desirable in such applications to reduce the heat loss, volume and weight of these chargers. Moreover, the capability of bidirectional conversion is preferred for potential vehicle-to-grid applications. This paper presents the system architecture and embedded digital control implementation of a 7 kW, universal ac (120-240 V_{AC}) to 400 V_{DC} single-phase ac-dc bidirectional converter. The converter features an interleaved 6-level flying capacitor multilevel (FCML) ac-dc stage and a series-stacked buffer for buffering twice-line frequency pulsating power to achieve high efficiency and power density. Test results that demonstrate both ac-dc power factor correction (PFC) and inverter operation at kilowatt levels are provided.**

I. Introduction

Single-phase ac-dc converters are the main functioning blocks of level-II on-board electric vehicle chargers, which charge the high-voltage battery in the vehicle with single-phase ac-grid (120-240 V_{AC}) at kilowatt levels [1]. The operating condition of the on-board charger favors compact, lightweight, and high-efficiency designs due to the space and range constraints in electric vehicles. In this work, we seek to improve the overall power density and efficiency of the ac-dc stage of the level-II EV charger with a system-level design approach that considers converter topology, digital control and mechanical packaging simultaneously.

In terms of converter topology, conventional design of the ac-dc stage usually features a boost converter to regulate the input ac current with high power factor and low distortion, and a large electrolytic capacitor bank at the dc-bus to buffer the twice-line frequency pulsating power in single-phase conversion [2]. The boost inductor [3] and the large capacitor bank [4] are the two main barriers to achieve higher gravimetric and volumetric power density. To reduce the size of the passive components in the converter, a system architecture that features the flying-capacitor multilevel (FCML) converter as the power factor correction (PFC) stage, and a series-stacked buffer (SSB) as the twice-line frequency power buffer is selected. The high power density and high efficiency features of such an architecture have been demonstrated in 2 kW PV inverter applications [5]. Moreover, a high power density 7 kW inverter with two interleaved FCMLs (without active buffer) has also been investigated in [6].

For level-II bi-directional EV charger application, the required high power at 7 kW and the bidirectional operation bring extra challenges in the design of both hardware and control. In this paper, system operation and control challenges such as coupling PFC with SSB, interleaved FCML PFC current control and bi-directional operation are discussed. Numerous practical concerns related to signal sensing, sampling and actuation for this architecture are addressed and validated in a high performance hardware prototype. Test results that demonstrate ac-dc conversion with PFC for both 120 V_{AC} and 240 V_{AC} to 400 V_{DC}, and inverter operation from 400 V_{DC} to 240 V_{AC} at kilowatt levels are provided.

II. System Architecture and Operation

The overall system schematic drawing is shown in Fig. 1. From the ac side to the dc side, it consists of an active rectifier, an ac-dc (bi-directional) conversion stage with 2-phase interleaved FCML converters, and a series-stacked buffer (SSB) across the dc bus. The overall control diagram for both PFC and SSB is shown in Fig. 2, and the control for the inverter mode is shown in Fig. 3. For the analysis in this work, unity power factor is considered for both rectifier and inverter mode. The ac voltage and current are described as:

$$v_{\text{ac}} = V_{\text{ac}} \sin(\omega_L t), \tag{1}$$

and

$$i_{\text{ac}} = I_{\text{ac}} \sin(\omega_L t), \tag{2}$$

where V_{ac} and I_{ac} are the magnitudes, and ω_L is the line frequency (60 Hz U.S. line frequency is considered in this work).

A. Rectifier mode

1) FCML PFC stage: In the rectifier mode, the PFC stage regulates the input ac current to be in phase with the input voltage, which is implemented with two interleaved FCML boost converters. With the FCML, the inductor size is reduced by $(N-1)^2$ times from the conventional two-level boost converters (where N is the number of levels) [7], [8]. The smaller inductor brings challenges of input current phase leading caused by limited loop gain and bandwidth of the current compensator, which can be solved with additional feedforward term [9], [10]. The inductor current of each phase

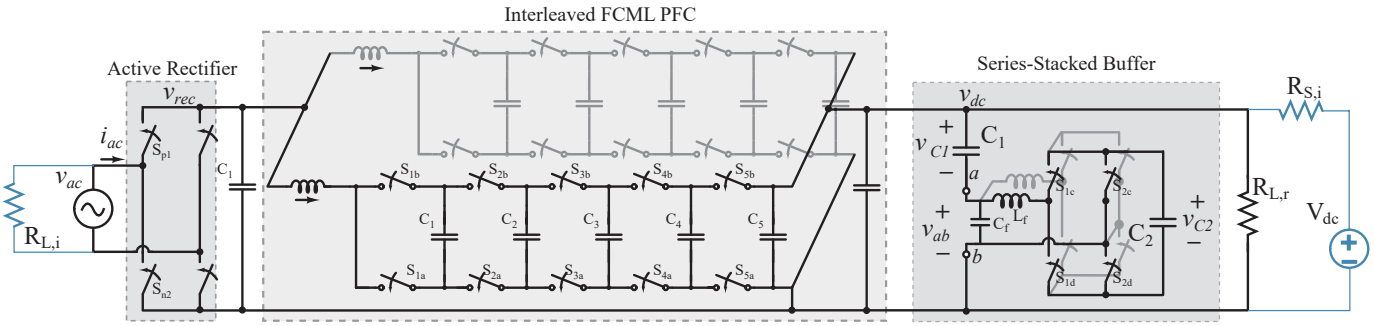

Fig. 1. Schematic of the overall system with active rectifier (unfolder), interleaved FCML, and series-stacked buffer. The dc source and load are shown in blue.

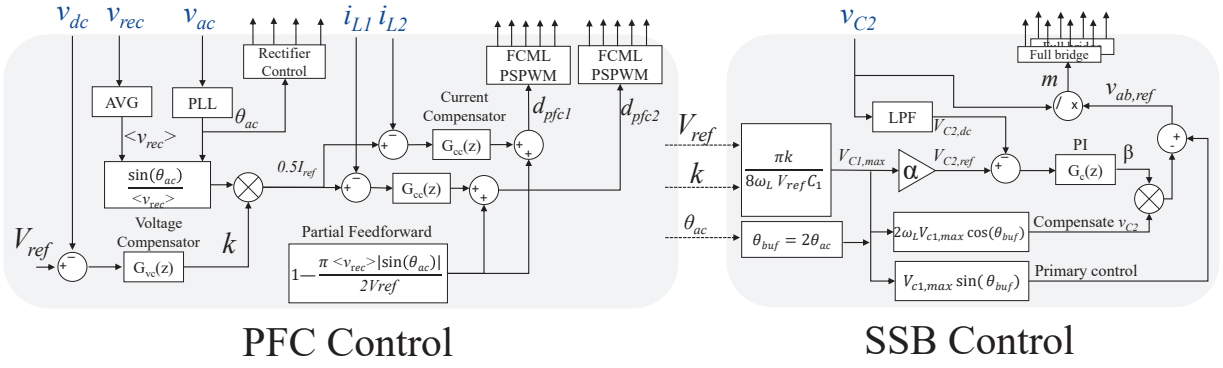

Fig. 2. Overall control system of the interleaved PFC and SSB in rectifier mode. The sensed parameters are in blue font.

is regulated independently as shown in Fig. 2 to ensure equal current sharing between the two phases.

2) Series-Stacked Buffer: The schematic of the SSB is shown in Fig. 1. The main buffering capacitor C_1 is connected in series with a full-bridge converter. As v_{C1} ripples with the pulsating power, the full-bridge converter actively cancels the ripple on v_{C1} with generated v_{ab} such that the dc-bus is ripple free. With the high voltage swing, the energy utilization of C_1 is increased to reduce the needed capacitance. Moreover, since the high dc-bus voltage is blocked by C_1 from the full-bridge converter, the full-bridge converter only processes a small fraction of the total system power, which results in high efficiency. The voltage of C_2 is regulated with a feedback loop that draws real power into the full-bridge converter to prevent the capacitor voltage from decaying, which will introduce a small amount of extra voltage ripple on the dc-bus. A detailed description of the operation and component sizing of the SSB architecture can be found in [11].

A control scheme [12], [13] that couples the SSB controller with the PFC control parameters is implemented to ensure the phase and power relation between the two stages. The voltage-loop factor k that scales the input current and the angle of the ac voltage are passed to the SSB controller to determine the magnitude and phase of the reference voltage for v_{ab}. If ac voltage is $V_{ac}\sin(\omega_L t)$, the ideal voltage v_{ab} is

$$v_{\text{ab}} = \frac{P_{\text{dc}}}{2\omega_L V_{\text{dc}} C_1}\sin(2\omega_L t) = \frac{\pi k}{8\omega_L V_{\text{dc}} C_1}\sin(2\omega_L t), \quad (3)$$

where P_{dc} is the dc load power, ω_L is the line angular frequency, V_{dc} is the average dc-bus voltage [13]. P_0 can then be calculated from the voltage-loop factor k such that the magnitude for v_{ab} is obtained.

B. Inverter Mode

In the inverter mode, the dc load is replaced with a dc-source, and the ac source is replaced with a resistor as shown in Fig. 1. For simplicity, the ac load considered in this work is resistive and the FCML inverter runs open-loop voltage control with the rectified sinusoidal duty ratio:

$$d_{\text{inv}} = m|\sin(\omega_L t)|, \quad (4)$$

where m is the modulation depth (0 to 1) determining the peak ac voltage $V_{\text{ac}} = mV_{\text{dc}}$. The angle $\theta_{ac} = \omega_L t$ is passed to the rectifier/unfolder control to create a full sine wave.

Instead of sensing the inverter current to generate a current reference for the SSB as in [14], the same inductor current sensors in the PFC mode are used to calculate the system power such that the voltage-based control scheme in [12], [13] can be applied. Note that the inductor current direction is reversed compared to the PFC mode, which means the current sensing circuitry should be able to measure bi-directional current. In the actual hardware implementation, the current amplifier LT1999 with 1.5-V dc bias at zero current is used.

The load ac current of the two FCML phases are measured and averaged with moving-average filter at 120 Hz. If the peak ac current is I_{ac}, the 120 Hz average value is $\frac{2I_{\text{ac}}}{\pi}$. As shown in (3), the magnitude of v_{ab} can be calculated with the dc power level. In this case, the averaged ac current is used to calculate

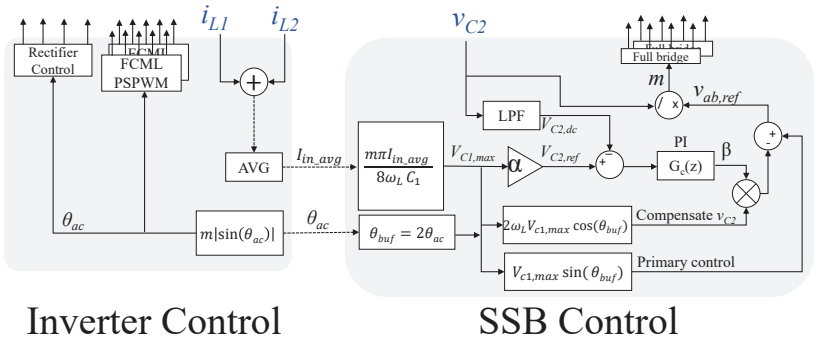

Fig. 3. Overall control system in inverter mode.

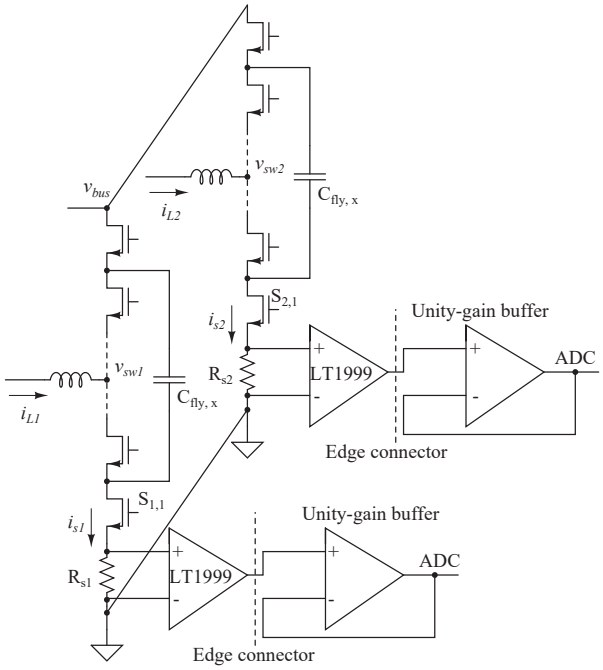

Fig. 4. Current sensing circuitry for two interleaved FCML phases.

the load dc power as

$$P_{\text{dc}} = V_{\text{dc}} I_{\text{dc}} = \frac{V_{\text{ac}} I_{\text{ac}}}{2} = \frac{m V_{\text{dc}} I_{\text{ac, avg}} \pi}{4}. \quad (5)$$

The new expression for the SSB controller to generate the correct v_{ab} can thus be simplified to:

$$v_{\text{ab, inv}} = \frac{P_{\text{dc}}}{2\omega_L V_{dc} C_1} \sin(2\omega_L t) = \frac{m\pi I_{\text{ac, avg}}}{8\omega_L C_1} \sin(2\omega_L t). \quad (6)$$

Once the magnitude of v_{ab} is determined, the remainder of the SSB control is identical to the PFC mode.

III. Interleaved FCML Average Inductor Current Sensing

This section discusses the method for capturing the average inductor current in the interleaved FCMLs. The required ADC timing and PWM signals are implemented with the internal ADC and ePWM modules in the Texas Instruments C2000 Delfino F28379D DSP.

A. Sensing average inductor current in FCML

In both PFC and inverter mode, the average inductor current in the FCMLs needs to be sampled accurately. Moreover, the inductor current of the two FCMLs need to be sampled separately such that they can be regulated independently to prevent unequal current sharing between the two phases.

In [9], [13], the inductor current is sensed with a shunt resistor in the ground return path to lower the common-mode voltage stress for the corresponding current amplifier. or an implementation employing a single FCML, the input inductor current does indeed equal the ground return current so that such placement of the shunt resistor is feasible. However, for two interleaved converters, while the total input inductor current equals the total return current, the individual inductor current of each phase cannot be obtained by sensing the individual ground return current. To sense the inductor current of each phase, the shunt resistors are placed between the source of the lowest switches and return ground, as in Fig. 4. In this configuration, the shunt resistors are directly sensing the current of the lowest switches $S_{1,1}$ and $S_{2,1}$, which will be equal to the inductor current only when $S_{1,1}$ and $S_{2,1}$ are on. Moreover, a unity-gain buffer is added between the current amplifier and ADC input to increase the driving strength and noise immunity of the signal as it is routed through multiple boards and connectors.

For a conventional 2-level converter, if an up-down count mode carrier counter (i.e., symmetrical triangular wave carrier) is used for digital PWM signal generation, the center of the PWM signal will align with the average inductor current [15], [16]. For the FCML, the same control can be applied to align PWM signals with the average inductor current. As can be seen in Fig. 5, the moment when the inductor current reaches the average value is when the carrier counter reaches either zero or peak value.

B. ADC triggering and windowing

The internal ADC channels and associated control modules in the Texas Instruments C2000 Delfino 28379D DSP are used to implement the required ADC timing.

When the ADC channel is triggered, the sample-and-hold (S/H) switch in the ADC is closed and a capacitor is charged during the programmed time window to sample the input voltage. However, at the moment when the S/H switch is closed, there will be a instantaneous voltage drop spike on

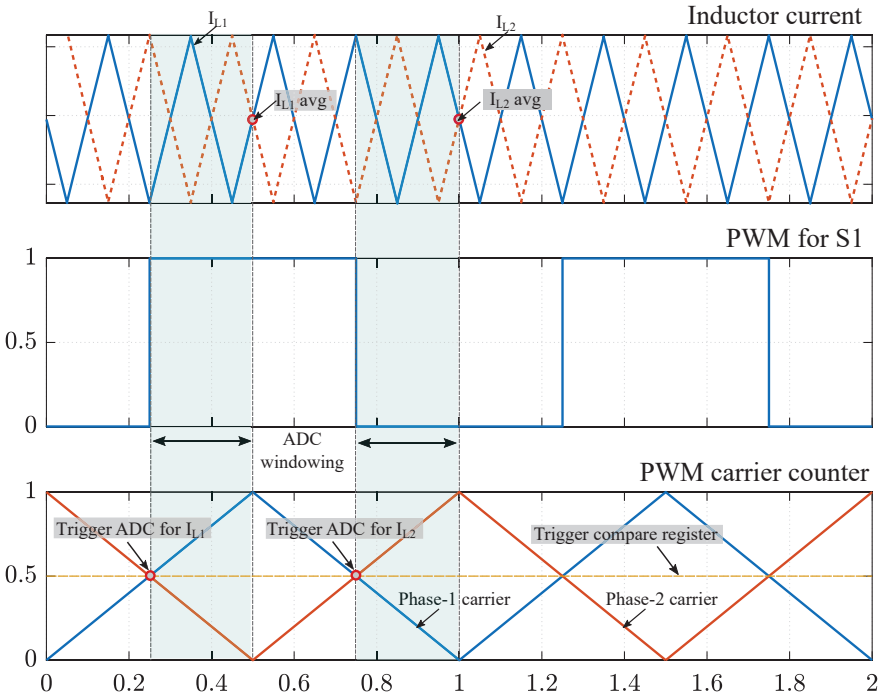

Fig. 5. Generalized key waveforms demonstrating the timing of ADC triggering to sample the average inductor current of the two phases. Duty ratio is 0.5 for PSPWM. Peak value of the carrier counter and the switching period are normalized.

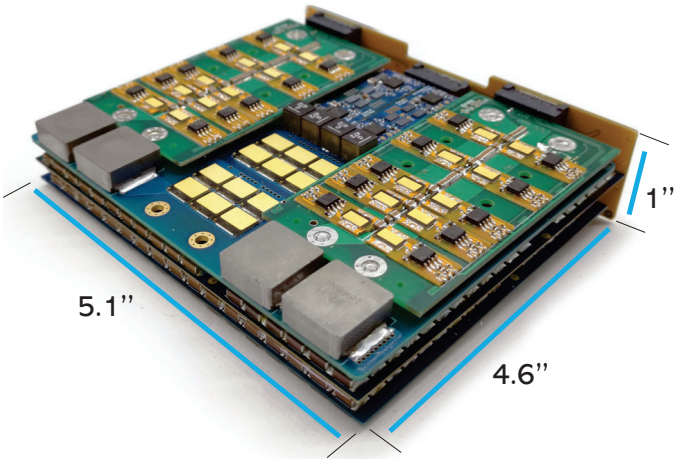

Fig. 6. The hardware assembly of the EV charger.

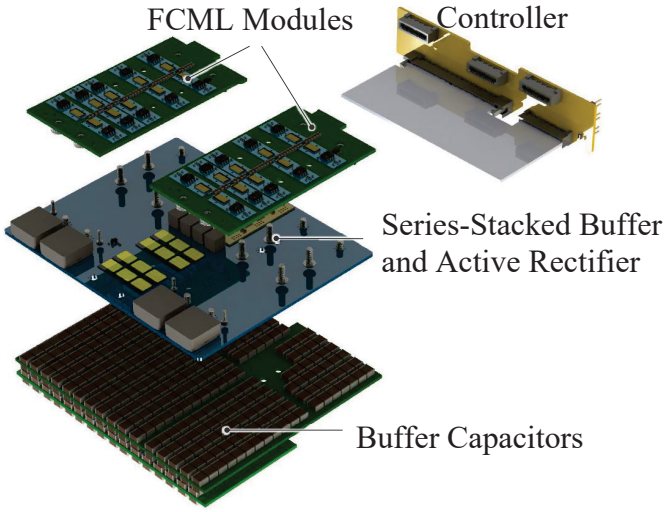

Fig. 7. Exploded view render of the hardware assembly.

the capacitor, which causes noise in the ADC reading [17]. Thus, the ADCs have to be triggered before the carrier counter reaches zero or peak value to obtain clean readings of the average inductor current.

For the S/H capacitor to obtain the average inductor current, the final reading of the S/H capacitor during the sample window has to be equal to the average inductor current. To ensure this, the ADCs are triggered by using the ePWM module in the TI Delfino DSP when the duty ratio is 0.5, referencing to the PWM carrier counter of $S_{1,1}$. With a duration of a quarter of the switching period, the sensing window ends right at the peak of the carrier counter. For interleaved current sensing, the ADC for i_{L1} is triggered at 0.5 duty ratio during the up-count region, and the ADC for i_{L2} is triggered during the down-count region. A detailed illustration of ADC triggering and windowing is shown in Fig. 5. Different ADC timing configurations can also be implemented to adapt to the overall system control as long as it ensures that the final reading of the S/H capacitor is correct. For example, the ADC window can be shortened to leave more headroom for system control computation, yet the end of the window has to be aligned with peak or zero of the carrier counter.

IV. Hardware Design and Assembly

A hardware prototype with the proposed architecture and control has been designed and constructed (Fig. 6). A render of the an exploded view of the assembly is shown in Fig. 7. The hardware prototype consists of an interleaved pair of FCML modules, a series-stacked buffer power stage, an

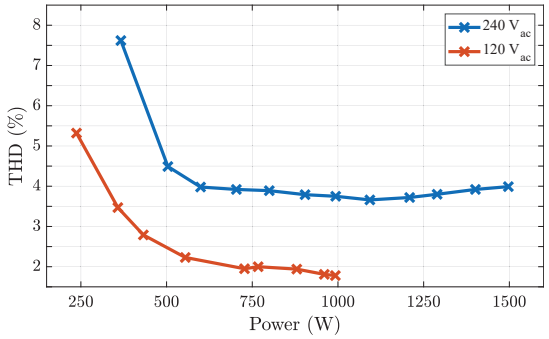

Fig. 8. The THD of the system, PFC mode from 120 and 240 V_{AC} to 400 V_{DC}.

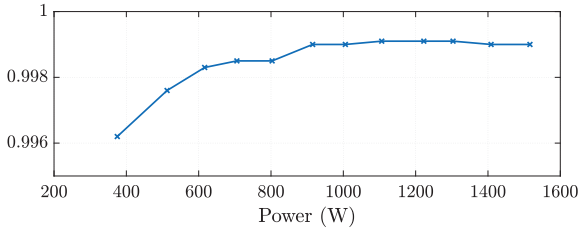

Fig. 9. The measured power factor of the system, PFC mode 240 V_{AC} to 400 V_{DC}.

unfolder/rectifier, and capacitors for energy buffering. Signal connectivity to the microcontroller board is provided through a connectors board, and power connectivity between the power stages is provided through bolt and power-tap element connections.

The prototype was designed with a philosophy of balancing a combination of electrical, mechanical, and thermal aspects. As such, the electrical design is relaxed from the absolute optimal layout in favor of mechanical mounting and capability for automated assembly. The mechanical design for the system focuses on a modular approach to assembly, with high utilization of 3D space. The thermal design for the system drove the mechanical and electrical designs such that all of the heat-generating surfaces were placed on a single side, to simplify fluid routing and thermal efficiency for a single-sided liquid- or air-cooling system.

For the 400 V_{DC} bus, each switch needs to block 80 V ($v_{dc}/5$), so 100 V rated GaN devices from GaN Systems are used in the FCML stage. The unfolder utilizes 650 V rated GaN devices from GaN Systems, as they are blocking the full 240 V_{AC} line voltage. For the series-stacked buffer, each switch must withstand about 110 V. Therefore, 150 V rated GaN devices from EPC are used.

V. Experimental Results

The converter was tested in the PFC mode with a 120 V_{AC} (low line) and a 240 V_{AC} (high line) input for a 400 V_{DC} output. The converter was also tested in the inverter mode with a 400 V_{DC} input and a 240 V_{AC} output up to 1 kW. The system was tested without a heatsink. Figure 8 shows the THD on the ac side of the system running in PFC mode, and Fig 9 shows the measured power factor for 240 V_{ac} to 400 V_{dc}. In

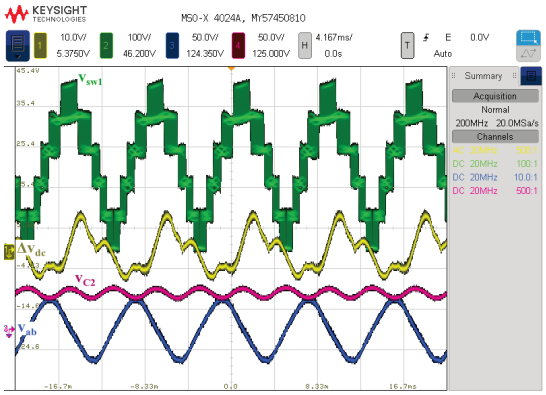

Fig. 10. Typical SSB voltage waveforms for v_{c2} and v_{ab}, dc bus voltage ripple (ac coupled), and FCML switch-node of the system, PFC mode from 240 V_{AC} to 400 V_{DC}, 1.5 kW.

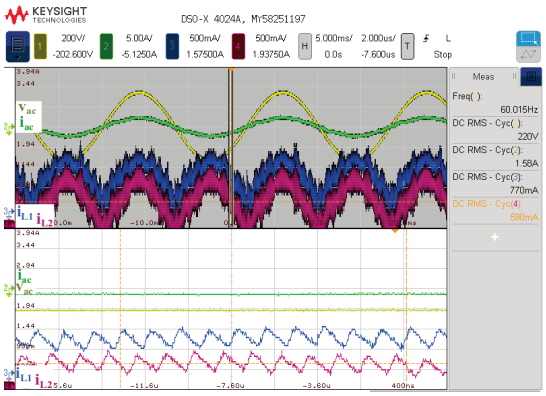

Fig. 11. Typical current waveforms of the interleaved FCML, PFC mode from 240 V_{AC} to 400 V_{DC}, 375 W.

all test conditions, the input voltage and current are well in-phase (PF $\geq$ 0.99), and the switching node voltage shows good balancing between the flying capacitor voltages (v_{sw1}, Fig. 10) and good current balancing between interleaved FCML modules (i_{L1}, i_{L2}, Fig. 11). For the SSB, film capacitors of smaller values than the full power specifications were used for C_1 (80 μF) and C_2 (68 μF) to simulate the voltage ripple effects at the full power level (7 kW). The dc bus ripple (Δv_{dc}) is about 10 V (2.5% of 400 V_{DC} – Fig. 10) at the 1.5 kW high-line PFC input case.

VI. Conclusions

This paper presents a system architecture that features the flying-capacitor multilevel converter (FCML) and the series-stacked buffer (SSB) topologies used in a single-phase Level II EV charger system. The design process is discussed including the overall system architecture, controller and hardware design. Test results demonstrating both ac-dc Power Factor Correction (PFC) and inverter operation at kilowatt levels are shown. The low THD, high power factor input current, balanced FCML flying capacitor voltage and the low dc-bus ripple all proved the effectiveness of the proposed system architecture and implmented digital control scheme.

VII. Acknowledgement

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