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Extremely Flexible (1mm bending radius) Biocompatible Heterogeneous Fan-Out Wafer-Level Platform with the Lowest Reported Die-Shift (<6 µm) and Reliable Flexible Cu-based Interconnects

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Extremely Flexible (1mm bending radius) Biocompatible Heterogeneous Fan-Out Wafer-Level Platform with the Lowest Reported Die-Shift (<6 µm) and Reliable Flexible Cu-based Interconnects

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Abstract—A flexible fan-out wafer-level packaging (FOWLP) process for heterogeneous integration of high performance dies in a flexible and biocompatible elastomeric package (FlexTrate™) was used to assemble >600 dies with co-planarity and tilt <1µm, average die-shift of 3.28 µm with σ < 2.23 µm. We have also engineered a novel corrugated topography of a stress buffer layer for metal interconnects on FlexTrate™ to mitigate the buckling phenomenon of metal films deposited on elastomeric substrates. Corrugated interconnects were then tested for their mechanical bending reliability and have shown less than 0.4% change in resistance after bending at 1 mm radius for 1,000 cycles. Finally, we demonstrate integration of an array of 25 dielets interconnected in a daisy chain configuration at 40 µm interconnect pitch.

Keywords-Flexible device integration, Biocompatible, FOWLP, Bendable interconnect, Metallization of PDMS

I. INTRODUCTION

Conventional flexible electronics have been mainly divided into two categories. One is the use of organic semiconductors that are deposited at low temperatures on flexible substrates at the sheet-level or using roll-to-roll processing [1-3]. The other category is what we coin "conventional" flexible hybrid electronics (FHE), which uses transfer techniques to integrate ultra-thin single-crystalline inorganic dies on flexible substrates. Although the performance of organic semiconductors has improved over the years [4, 5], the performance of inorganic semiconductors, represented by Si and III-V devices, is significantly superior compared to their organic counterparts [6, 7]. The FHE approach combines the best of both worlds, since it has both the flexibility of organic polymeric substrates, and the performance of inorganic single-crystalline semiconductor devices [8, 9].

In order to enhance the flexibility of conventional FHE, ultra-thin dies, typically less than 20 µm, are mounted on the FPC (flexible printed circuit) boards [9] because such thinned dies can follow curved surfaces. However, there are three major drawbacks of the "conventional" approach for realizing FHE. First, ultra-thin dies are sensitive to stress-induced device and circuit performance degradation. For example, Lee et al. have reported that the retention time of thinned DRAM having planar capacitors would be shortened when the die thickness is 50 µm or less by more than 50% [10]. Second, the potential manufacturability of products is dependent on achieving high yield after two processes: 1) wafer thinning from bulk inorganic substrates 2) handling of ultra-thin dies using flip chip techniques [6, 7]. Third and most important drawback, is that the printed interconnects on flexible substrates have coarse interconnect pitches, typically in the hundreds of µm range, which hinders integration of high performance logic/memory dies requiring high number of I/Os. In addition, either wire bonding/ball bumping is typically used to create connectors to communicate with other integrated chips, which does not allow for high number of I/Os needed for high performance logic and memory dies [11], and also limits the flexibility of the entire assembly [12], which is shown schematically in Fig. 1(a). This is why our FlexTrate™ approach was inspired by the current trend of fan-out-wafer-level-packaging (FOWLP), where Si processing techniques are adapted to packaging. In FOWLP heterogeneous dies are embedded in molding compound, which is used to "reconfigure" a wafer[13]. The reconfigured molded wafer is then interconnected at fine pitch using standard back end of the line (BEOL) processes to form redistribution layers (RDL). FOWLP has various benefits in terms of enabling heterogeneous integration, form factor reduction, and overall higher performance. However, current commercially available FOWLP are rigid and not flexible, and largely used in portable devices that benefit from form factor reduction.

In our approach, we integrate rigid inorganic dielets in a flexible polymeric molding compound, that we call

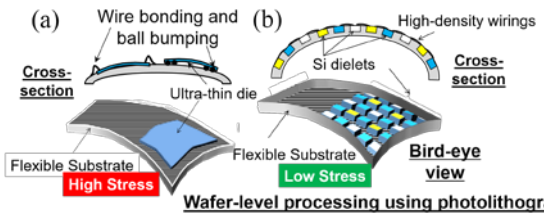

Fig. 1. Schematic comparison of die integration for FHE: ultra-thin/large die bonded on flexible substrate (left) and thin/small dielets embedded in flexible substrate "FlexTrate™" (right).

FlexTrate™, fabricated at the wafer-level using an advanced die-first FOWLP process[14]. Contrary to conventional rigid FOWLP process, the high flexibility of FlexTrate™ is given by the structure consisting of hard and soft segments similar to a bicycle chain, where the links themselves have sufficient flexibility as depicted schematically in Fig. 1(b), while inorganic dielets can be rigid. The integrated dielets are then electrically connected with high-density interconnects formed using a wafer-level process with a much finer interconnect pitch compared to conventional printed flexible electronics fabricated in sheet-level or roll-to-roll processing.

In this study, die shift and co-planarity between our molding compound, namely Polydimethylsiloxane (PDMS), and inorganic dielets are optimized in order to enable integration of interconnected dielets in a daisy chain at 40 μm wire interconnect pitch (20 μm wide lines, with 20 μm separation). Because of the thermomechanical material properties of FlexTrate™, we were able to demonstrate an array of 25 daisy chained connected dielets with 160 connections that are reliable under cyclic mechanical bending. We also evaluate the reliability of integrated dielets at fine pitch on FlexTrate™ through mechanical cyclic bending test down to 5 mm bending radius for than 1,000 cycles.

II. Overcomig FOWLP Process Challenges

Rigid FOWLP integration has four major process challenges: (1) the high glass transition temperature (T_g) of rigid molding compound used in wafer reconstruction, (2) the coefficient of thermal expansion (CTE) mismatch with respect to Si dielets, (3) high drag forces from the mold reflow during mold compression process, and (4) chemical shrinkage during the curing process [15]. These process challenges cause substrate warpage, poor die co-planarity with respect to the molding compound(die pop-up), and, most importantly, die shift from the original placement position [16, 17]. To minimize die shift, dies are "pre-shifted" to compensate for any shift during the molding and curing processes [15, 17]. Even so, state-of-the-art die-shifts are of the order of 10-20 μm [15]. These large die shifts result in large overlay tolerances for the interconnects that are used to connect the dies, which in turn limits the finest interconnect pitch to ~3x the worst-case die shift (*i.e.*, 40-80 μm). Rao et al. recently demonstrated 10 μm pitch lines for 1st layer RDL with 30 μm minimum pad size for rigid FOWLP based package-on-package (PoP), for package size of 15 mm×15 mm×0.2 mm, however, only 2 dies were used in their demonstration [18]. In this study we demonstrate an array of interconnected 25 dielets at 40 μm pitch using 20 μm pad size.

To overcome above mentioned FOWLP challenges, we have chosen a biocompatible molding compound, namely PDMS based "Silastic MDX4-4210 (Dow)", which has significantly improved thermo-mechanical properties compared to rigid epoxy-based molding compounds, as shown in Table 1. Although PDMS has significantly higher CTE mismatch with respect to both Si and Cu (300 vs. 3 and 17 ppm/K) when compared to rigid molding compounds (7.5 ppm/K), we are able to reduce die shift to less than 6 μm because of two reasons: (1) since the T_g of PDMS is -120ºC, we can cure the compound at room temperature, minimizing shrinkage after curing; (2) PDMS exhibits four orders of magnitude lower Young's modulus as compared to rigid molding compounds, the drag force during mold compression and flow is, therefore, not large enough to cause significant die shift.

TABLE I. Properties of a Biocompatible PDMS for FlexTrate™ and a non-biocompatible rigid epoxy used in typical FOWLP.

Properties	PDMS (MDX4-4210 DOW)	Epoxy Molding Compound
Elongation at break	~500%	<1%
CTE	~300 ppm/k	7.5 ppm/k
Young's Modulus	0.5 MPa	22 GPa
T_g	-120 ºC	165 ºC
Curing Temp.	25-80 ºC	125-150ºC
Biocompatibility	Implantable	None

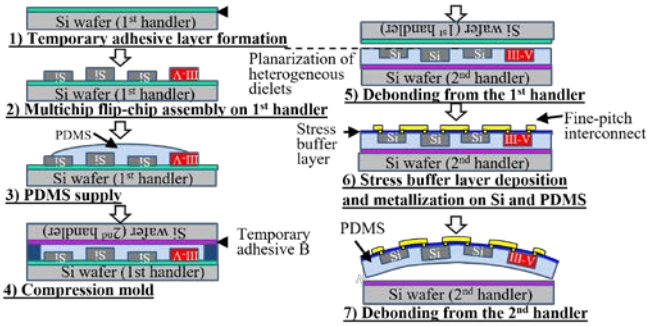

Fig. 2. A process flow for FlexTrate™ fabrication

III. Experimental Demostration

Fig. 2 shows the process of FlexTrate™ fabrication. First, a removable temporary adhesive layer was laminated on a handling Si substrate, 1st handler. Heterogeneous dielets, with possible thickness of 100-200 μm and 1-5 mm^2 sizes, were then precisely aligned in a face-down configuration on the adhesive formed on the 1st handler using a flip-chip bonder. A biomedical grade PDMS film was then applied on the die-on-wafer structure, and then sandwiched with a 2nd Si handling substrate, which has been already laminated with a different temporary adhesive. Both tapes are laminated at room temperature. This is followed by a compression molding step performed in a wafer bonder for various times and temperatures (24 hours for room temperature curing *vs.* 30 minutes for 80 ºC curing). The 1st handler was then thermally debonded at 130 ˚C for 5 min, and subsequently, several hundreds of dielets were transferred to the 2nd handler. Prior to the following metallization processes, a thin stress buffer layer of Parylene-C and a SU-8 planarization layer were sequentially formed with a Parylene-C coater and simple spin-coating on the PDMS/dielets, respectively. Then, using standard photolithography processes, fine-pitch wires were fabricated using vacuum-based evaporation or sputtering techniques for metal deposition, as well as, electroplating

using a semi-additive process depending on the intended application. Finally, FlexTrate™ was thermally debonded at 180 ˚C for 5 minutes from the 2nd handler.

IV. Die Coplanarity Evaluation

625 1mm×1mm 100 µm thick Si dielets were placed using a 5 N/chip placement force on first handler adhesive at 1.8 mm pitch, PDMS soft-molded and then transferred from the first handler to the second handler, as shown in Fig. 3(a). This corresponds to step 5 in Fig. 2. 3D surface profile of 625 Si dielets that were successfully transferred from the 1st handler to the 2nd handler measured using a surface metrology system equipped with confocal white light. Die tilt and height gap (pop-up) data were analyzed and summarized in Figs. 4 (a, b), respectively. The PDMS in this study was cured at room temperature. Fig. 4 (a) shows that intra-dielet tilt was within 1 µm for all 625 dielets. Co-planarity of all the dies and the PDMS surface are represented in the histogram in Fig. 4 (b). Die tilt was less than 1 µm, as can be seen from Fig. 4(a.) Fig. 4 (b) shows a maximum height gap (pop-up) of 6 µm. The modal value of the distribution is about 2-3 µm, which we were able to further reduce to less than 1 µm, with the deposition of planarizing stress buffer layers. This enables fine pitch lithographic patterning of metal redistribution layers (RDL).

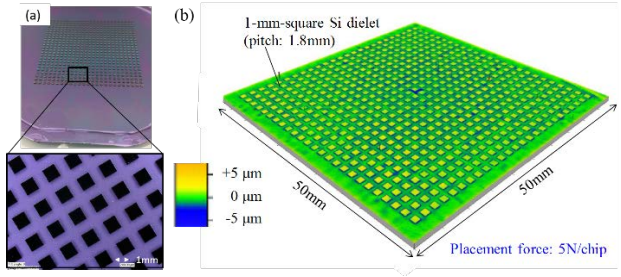

Fig. 3 (a) Photomicrographs of 625 dies transferred to 2nd Si handler (b) A cross-sectional schematic and the 3D surface profile of Si dielets embedded in molded PDMS after transfer to the handler.

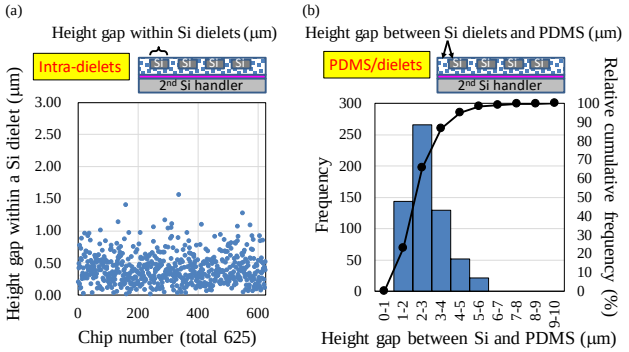

Fig. 4 Co-planarity evaluated for (a) intra-dielet tilt and (b) PDMS and dielets case evaluating the height gap (pop-up).

V. Die Shift Evaluation

We evaluated die shift before and after PDMS curing using Vernier scale patterns on the temporary adhesive laminated on the 1st handler. The dielets, having the corresponding Vernier patterns, are then aligned and placed using flip-chip pick and place tool on the adhesive tape. We used an alignment strategy that uses two alignment fiducials, as shown in Fig. 5 (a, b), on both the integrated dielets and the adhesive tape on the 1st handler. The flip chip assembled die on the adhesive is shown in Fig. 5(c). The placement accuracy of an array of 25 dies is shown in Fig. 6 (a, b) for alignment accuracy in both the x and y directions. The placement accuracy was measured to be ± 1 µm, as shown in Fig. 6 (a, b), where the average misplacement was measured to be < 1 µm. This ± 1 µm placement accuracy helps reducing the aggregate die shift measured after wafer reconstruction.

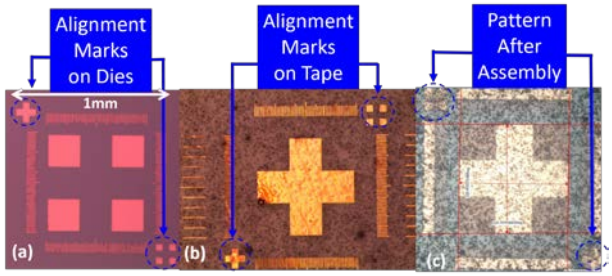

Fig. 5. Alignment fiducial marks on (a) die (b) tape, (c) the final assembly of die placed on the tape, which are imaged through the backside of a glass substrate.

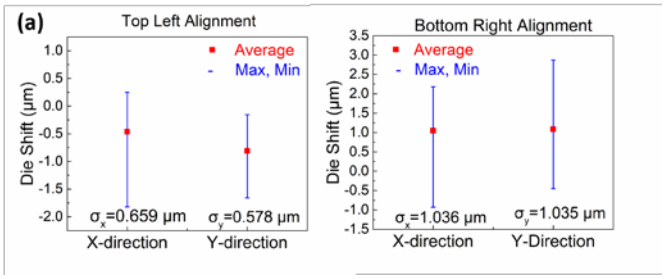

Fig. 6. Die placement accuracy measured mis-alignment average, standard deviation, and min-max values for (a) top left alignment fiducial, and (b) bottom right alignment fiducial marks.

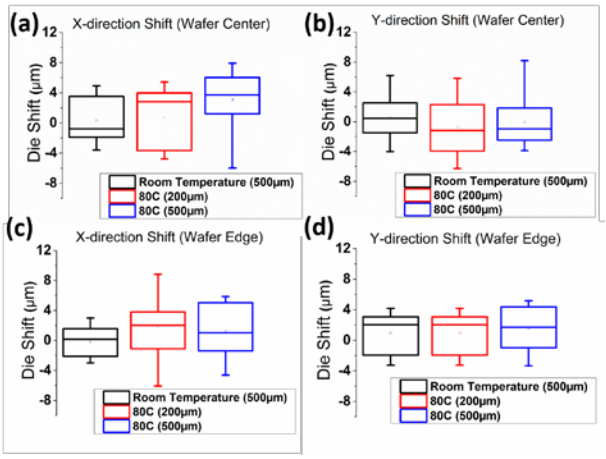

Fig. 7 Box and whisker representation showing effect of substrate thickness and curing temperature on x-direction shift and y-direction shift magnitude for (a,b) center and (c,d) edge dielets on 100 mm wafer.

After de-bonding from the first handler, automated die shift analysis was employed by processing 10x10mm images from an optical scanning microscope (500x lens) with ~2.39 pixels/μm resolution, which allowed us to image arrays of 25 dielets at both the center and edge of a 100 mm wafer, as shown in Fig. 7. Die shift was studied for two different curing conditions, namely room temperature cuing for 24 hours *vs.* curing at 80ºC for 30 minutes. Also, die shift was studied for two different substrate thicknesses: 200 and 500 μm. A support vector machine algorithm (SVM) and Förstner's corner detector algorithm were used to find the exact corners of each alignment mark and create a die map for calculating die shifts[19]. Data in Fig. 7 displays aggregate placement inaccuracies, accounting for both placement error and die shift effects due to curing and thermal shrinkage after first tape thermal release. Die shift and placement inaccuracy was noticeably lesser (±4-5μm) for the room temperature curing process compared to the higher temperature (80ºC) processes (± 6-8μm). Low processing temperature of PDMS FOWLP process reduces die shift effects by more than 10x compared to rigid epoxy molding compound of similar size, thus enabling fine pitch interconnects (FPI) on the FlexTrate™[18] without resorting to die pre-shift techniques.

VI. Flexible Interconnects Challenges

Forming of reliable fine pitch interconnects on elastomeric substrates is challenging because of the thermo-elastic wrinkling/buckling phenomenon arising due to compressive stress induced by shrinkage of a pre-strained substrate after release. This happens in the case of FlexTrate™ in the final thermal release step at 180ºC after the substrate is cooled down to room temperature (Step 7 in Fig. 2)[20]. This can potentially cause catastrophic failure due to buckle-induced delamination of deposited thin metal films [21, 22]. An image of released FlexTrate™ with 100 μm wide electroplated Cu interconnects is shown in Fig. 9(a) illustrating the buckling behavior**.** The Cu interconnects used in this study are 15 mm long, 2.4-5 μm in thickness, and 20-110 μm in width. The bendability of the FlexTrate™ having embedded dielets is then evaluated with an endurance testing system: tension-free U-shape folding tester. Lines were then mechanically bent at 10, 5 and 1 mm bending radii (R) consecutively for 1000 bending cycles for each radius, and average resistance values, measured from 4 lines/width, are shown in Fig. 9(b) along with the different interconnects' thicknesses. The thicknesses variation for the different line-widths is attributed to current crowding phenomenon arising from integration of various line thicknesses on the same die[23]. We extracted resistivity of the Cu interconnects to be between 2.3-2.7 μΩ-cm for four different interconnects width, where the Cu line width and thicknesses are noted in Fig. 9(b). Variations in measured resistance values due to bending cycling were less than 2.5 % indicative of the reliability of the fabricated electrical interconnects.

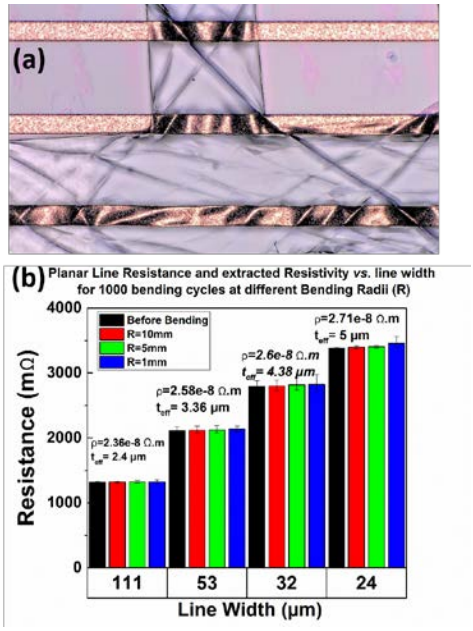

Fig. 9. (a) Planar 100 μm metal interconnect line micrographs after thermal release from 2nd handler. (b) 15 mm long interconnects resistance, and resistivity after bending at different bending radii for 1000 cycles.

While the thick electroplated lines have proven to be reliable when considering a single metallization layer; the effect of buckling/wrinkling behavior remains a concern for the mechanical integrity of subsequently deposited metal redistribution layers (RDL). Beam mechanics dictates that critical stress needed to induce buckling in a beam is inversely proportional to the square length of the beam[24]. Hence, linear reduction in the beam length can lead to a quadratic increase in the critical stress value needed for inducing buckling. This inspired the concept "corrugated" interconnects, where an intentional and controlled "segmentation" of the interconnects is used to counteract buckling due to the high compressive stress [20]. Planar and corrugated wires were thus fabricated side-by-side, as shown in Fig. 10(a,b). Images of the interconnects after thermal release show periodic buckle wavelength of 500 μm going through the planar structure for 100 μm lines, while it was not observed for the corrugated interconnects. Surface topography was measured by a laser-based optical profiler, and the amplitude of buckle waves of planar, and "corrugated" interconnects were measured to be 15 and 3 μm, respectively, showing more than 5x reduction as shown in Figs. 10 (c, d). Furthermore, resistance values for both planar and corrugated interconnects are reported after bending at different bending radii as shown in Figs. 11. Corrugated interconnects have shown less than 0.4% increase in average measured resistance per line width, which confirmed the reliability of the fabricated corrugated interconnects. The Von Mises stress profile was also studied in both planar and corrugated Cu interconnects in Figs. 12(a,b), respectively, under mechanical bending at 1 mm bending radius at the point of highest stress, for Cu interconnect length of 15 mm, width of 100 μm, and thickness of 4 μm. Results have shown that while the stresses

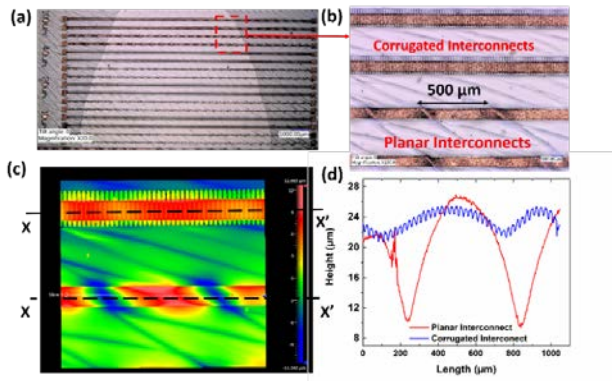

Fig. 10. (a) Image of fabricated sample after mechanical bending at R=1mm. (b) Image showing corrugated vs. planar 100 µm lines (c) Surface profile demonstrating buckling of planar lines with 15 µm peak-to-trough amplitude. (d) Plot of X-X' cross section in (c).

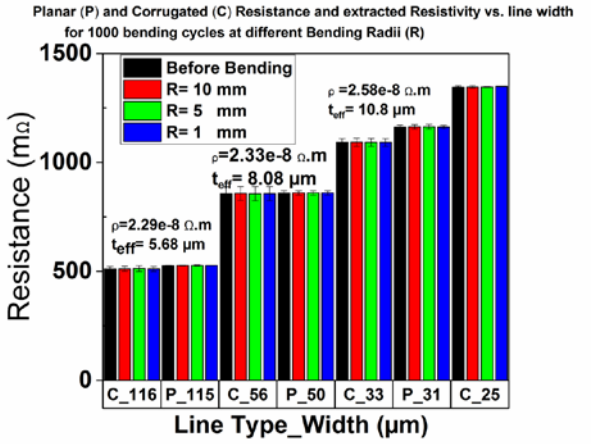

Fig. 11. (a) Metal line reliability and after bending for 1000 cycles at R=10, 5, and 1 mm for planar and corrugated interconnects.

depend on the exact location on the corrugation, the overall stress is shown to reduce on top of the corrugated structure, and show similar values to planar structure on the bottom of corrugations. In both cases, Cu did not undergo plastic deformation under bending at 1 mm bending radius.

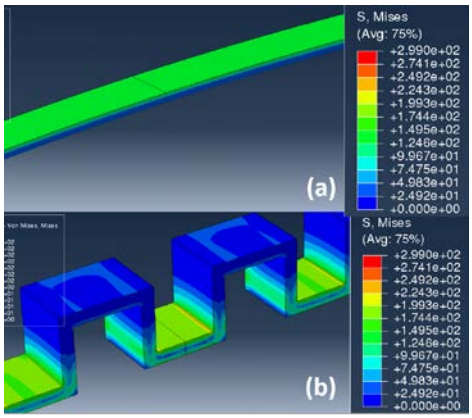

Fig. 12. Von Mises stress profile in (a) planar and (b) "corrugated" interconnect metal line bent at 1 mm bending radius at the point of highest stress.

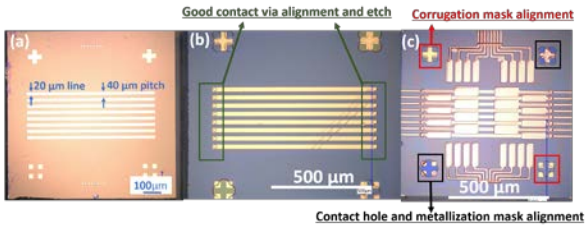

Fig. 13. (a) Fabricated 1 mm×1 mm×0.2 mm die after dicing Mask design for local alignment strategy to obtain fine alignment showing 8×20 µm Au interconnects with 40 µm interconnect pitch. (b) Contact vias etched through the buffer layers to contact the underlying 40 µm pitch lines on dies. (c) Design to obtain fine alignment using separate alignment marks for corrugations, via etching, and interconnect formation

VII. Daisy Chain Connected Dielets

Here, we connect a of 5×5 array of 1 mm^2 dielets at 1.8 mm dielet pitch with corrugated interconnects at 40 µm interconnect pitch on FlexTrate^{TM}. The 40 µm pitch interconnects form a daisy chain connection to the underlying dielets, which have 8×20 µm Au lines with corresponding 40 µm wire pitch and 20 µm pad size shown in Fig. 13(a). After dielets were transferred to the 2nd handler, deposited stress buffer layer acted as low-k dielectric, which we used for forming the first RDL. Vias were etched through the stress buffer layers, as shown in Fig. 13(b). The via diameter was measured to be ~18 µm over the 20 µm pad size. Masked lithography were used using alignment marks on the dielets for corrugations patterning, via etching, Cu interconnect plating and line passivation, as shown in Fig. 13(c).

The 40 µm fine pitch interconnects on 5×5 array of dies FlexTrate^{TM} are horizontally connected in daisy chain as shown in Fig. 14 (a) before thermal release. Figure 14(b) shows the 20 µm corrugated Cu interconnects with corrugation pitch of 27.5 µm. Fig. 14(c,d) shows staggered probe pads for performing 4-point probe measurement of 8 connections per dielet.

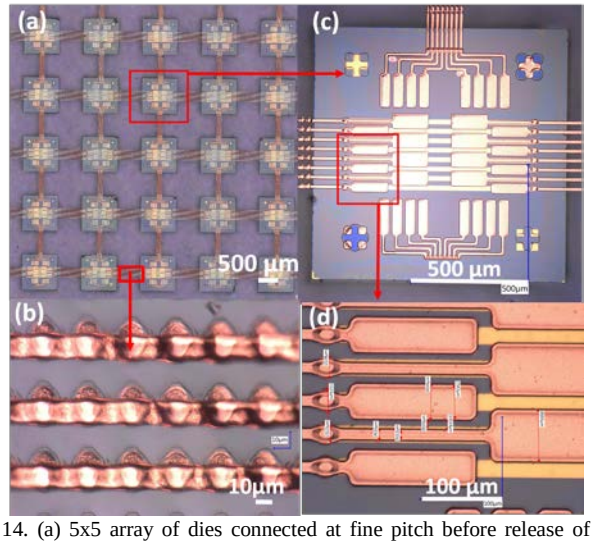

Fig. 14. (a) 5x5 array of dies connected at fine pitch before release of 2nd handler. (b) Zoomed in image corrugated interconnects. (c) Zoomed in image of a dielets with 16 staggered prove pads(d).

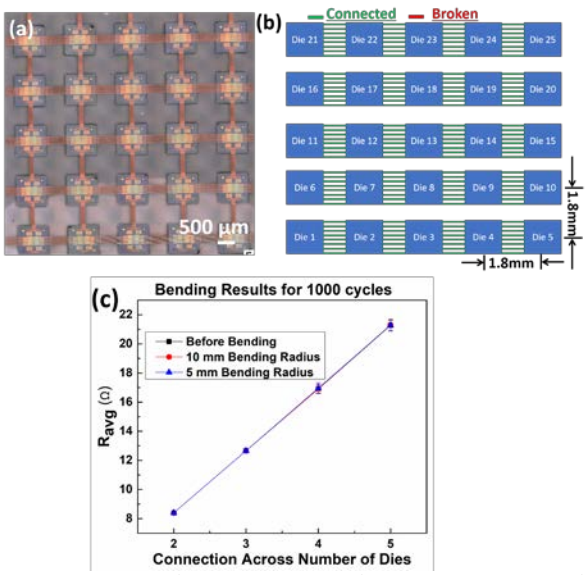

Fig. 15. (a) 5x5 array of dies connected at fine pitch post release of 2nd handler. (b) schematic of the electrical connections. (c) Measured DC resistance of Daisy chain connected dielets at 40 µm pitch before bending and after bending at 10 mm 5 mm bending radii.

The image of the array of 25 dielets after thermal release is shown in Fig. 15(a), where each of the 160 connections (5 rows×4interconnects per row× 8 connections per die) connections were checked and found to be functional schematically in Fig. 15(b). To test the flexibility of the FlexTrate™ with fine pitch interconnects, we measured the resistance of interconnects across the rows before bending, after bending at 10 mm, and after bending 5 mm bending radius for 1000 cycles each through 4-point probe measurement. The results are shown in Fig. 15(c). We first observe the linear increase in resistance as a function of the number of dies connected for the three conditions, which is expected. The measured average resistance shows identical values post bending at both 10, and 5 mm bending radius for 1000 cycles each showing the excellent reliability of the daisy chain connections. To the best of our knowledge, such a high-density integration (25 dies integrated across 8.2 mm×8.2 mm area at 40 µm die-die interconnect pitch, having total of 160 connections) has not been demonstrated on a flexible platform before.

VIII. Conclusion

We have described a flexible (FOWLP) process for heterogeneous integration of high performance dies in a flexible and biocompatible elastomeric package used to assemble >600 dies with a co-planarity and tilt (<1µm) die-shift (<6µm) and a corrugated-interconnect (ρ <2.3µΩ-cm) respectively with >1000 (R=1mm) bending cycles. We have also demonstrated an integrated FlexTrate™ with 40 µm die-die interconnect pitch which bendable down to 5 mm bending radius for 1000 cycles. If the second handler is not de-bonded, the resulting structure may be used for a rigid FOWLP assembly, as well. FlexTrate™ platform could potentially enable next generation of heterogeneous flexible/implantable systems that are high-performance, and potentially self-powered.

IX. Acknowledgment

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