Quench protection for high-temperature superconductor cables using active control of current distribution

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Abstract

Superconducting magnets of future fusion reactors are expected to rely on composite high-temperature superconductor (HTS) cable conductors. In presently used HTS cables, current sharing between components is limited due to poorly defined contact resistances between superconducting tapes or by design. The interplay between contact and termination resistances is the defining factor for power dissipation in these cables and ultimately defines their safe operational margins. However, the current distribution between components along the composite conductor and inside its terminations is *a priori* unknown, and presently, no means are available to actively tune current flow distribution in real-time to improve margins of quench protection. Also, the lack of ability to electrically probe individual components makes it impossible to identify conductor damage locations within the cable. In this work, we address both problems by introducing active current control of current distribution between components using cryogenically operated metal-oxide-semiconductor-field-effect transistors (MOSFETs). We demonstrate through simulation and experiments how real-time current controls can help to drastically reduce heat dissipation in a developing hot spot in a two-conductor model system and help identify critical current degradation of individual cable components. Prospects of other potential uses of MOSFET devices for improved voltage detection, AC loss-driven active quench protection, and remnant magnetization reduction in HTS magnets are also discussed.

Introduction

Superconducting magnet technology is essential for developing future fusion energy systems [1], [2]. HTS magnets built for plasma confinement and manipulation are expected to operate at elevated temperatures and fast ramping rates. These conditions dictate the use of composite cable conductors made upon multiple transposed components such as Roebel [3], CORC® [4], or Viper [5] to reduce magnetization effects and ensure operational stability through current sharing between components. Furthermore, using cables lowers magnet inductance, resulting in lower ramping voltage requirements and voltage on the coil during current extraction. Generally, the current flowing in the cable becomes shared through a normal stabilizer of individual HTS conductors whenever resistance appears due to a local conductor degradation, heating, or other factors reducing the superconducting conductor operational margin. Current sharing is a topic of active research due to its potential to improve HTS cable performance for magnet applications [6],[7],[8]. Yet, in many practical situations, current sharing is poorly defined, as contact resistance depends on factors such as normal stabilizer surface oxidation, stresses, bending deformations, etc. [9],[10],[11],[12],[13],[14]. Also, cable-in-conduit (CICC) CORC-based cable

conductors are being investigated for fusion magnet use [15],[16], where no current sharing exists between the components by design.

It is generally thought that limited current sharing translates into current distribution between components primarily determined by termination resistances. At sufficiently high current ramping rates, the distribution of component inductances and their mutual inductance matrix also plays a role in defining such distribution. The limited current sharing challenges quench protection when a hot spot appears in one of the components, and no current can bypass it locally through sharing with the neighboring component. At the same time, it also brings opportunities for implementing new quench detection approaches, such as those based on measuring the current imbalance between components at terminations [17],[18],[19], enabling access to intricate details of current re-distribution within the cable prior to the quench that is otherwise unavailable to other detection techniques that monitor the HTS cable as a single entity. As these novel detection techniques mature, it becomes increasingly evident that adding a capability of actively modifying current distribution in addition to passively measuring them can bring substantial advantages for cable diagnostics, improve quench protection, and broaden operational stability margins. Until recently, controlling high currents under cryogenic temperature as required for distributed control would have been a challenging technical task. Metal–oxide–semiconductor field-effect transistors (MOSFETs) have been earlier explored as current control elements for superconducting coils [20]. Today, steady progress in developing semiconductors based on new materials such as GaN, SiC, and SiGe brought a new class of MOSFET devices that are known to operate well at cryogenic temperatures [21],[22] are miniature (< 5 mm), fast (< 1 μs switching time), and capable of controlling currents at 100 A level while having an internal resistance below 1 mΩ in the closed state. This magnitude of internal resistance makes the associated heat load tolerable for HTS magnet systems and their associated cryogenics, while the effect of the magnetic field on MOSFET operation is not expected to be substantial [23]. The MOSFETs can also be binned together to achieve lower closed-state resistances and control higher currents. These devices are well-suited for on-off switching or AC modulation of component currents if built into cable terminations or de-mountable joints. Distributed detection and protection technology integrated with cable terminations may thus form a new paradigm for the quenching-free operation of HTS composite conductors at the peak of performance, making future fusion magnets cheaper and safer to run. This paper summarized the initial steps we took in simulation and experiment toward realizing this paradigm using in-house built MOSFET PC boards in combination with multi-conductor HTS assembly. The paper is structured as follows. First, we discuss current sharing in a “stack” of two HTS conductors separated by a normal metal base, derive the behavior of this system using an electrical network model, and discuss the benefits of implementing current distribution controls to drive individual conductors comprising the stack independently and to drastically decrease dissipation in a hot spot formed in one of the component conductors. Next, we review the MOSFET devices used for the cryogenic current control and present our experimental arrangement. Results of current re-distribution experiments demonstrating the diagnostic and protection capabilities are shown next, followed by a discussion on the broader implementation of active current controls for various critical HTS cable technology applications and preliminary conclusions.

Numerical modeling of current sharing

a. Current sharing in a tape stack

To investigate the problem of current sharing in an HTS cable, we implemented a 2D network model that calculates current and voltage distribution for a stack of ten HTS tape conductors current-shared through normal bulk metal in-between those conductors and having resistive current terminals interfaced to each of the conductors. Various public-domain and in-house developed circuit model realizations have been reported recently to provide current and voltage distributions for various HTS-related problems, such as a single HTS tape [24], HTS transformer [25], soldered stacked-twisted HTS wire [26], non-insulated coils [7], [27] and CORC® HTS cables [28]. Our model was implemented and solved using a freely available LTSpice® circuit simulator by Linear Technologies [29]. The circuit-defining input files for LTSPice® were generated using Python script, and calculation results were processed for visualization using an in-house developed Python-based interface. The network had 74 elements representing the tapes taken along the stack length and 10 elements along the thickness, one element per tape. Its equivalent electrical schematic is shown in Fig. 1. HTS conductors were represented as a serial chain of current-dependent voltage sources V_{00} … V_{oj} and V_{i0} … V_{ij}. An individual element $V_{ij}(I_{ij})$ was taken based on the commonly used power law representation of the current-voltage dependence of an HTS conductor [30], as:

$$V_{ij}(I_{ij}) = U_0 \left(\frac{I_{ij}}{I_{c\,ij}}\right)^n \quad (1)$$

where $I_{c\,ij}$ is the critical current of the single HTS conductor element, and I_{ij} is the current flowing in that element. We assigned $I_{c\,ij}$ values to be $I_{c0} \pm \Delta I_{ij}$ where $I_{c0} = 50$ A and $\Delta I_{ij}$was taken as a random number in the [0, 0.05*I_{c0}] interval, representing small variations of the critical current along the HTS conductor length. No temperature dependence of I_{c0} was assumed, nor were any thermal simulations performed in this work. The element voltage criterion U_0 was taken at 1 μV, assuming a physical length of a single element to be 10 mm and HTS conductor's voltage criterion of 1 μV/cm. The power-law

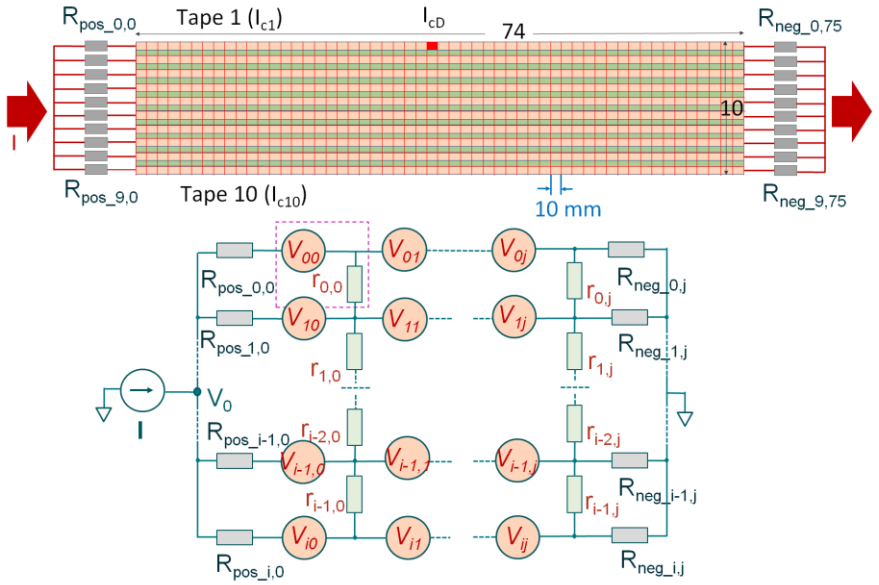

Fig. 1. A network model for a stack of 10 current-shared, individually-terminated HTS tapes. Each tape conductor is represented by 74 non-linear voltage source elements $V_{ij}(I_{ij})$ terminated with Ohmic termination resistances $R_{pos\_i,j}$, $R_{neg_i,j}$, and linked via current-sharing Ohmic resistances r_{ij}.

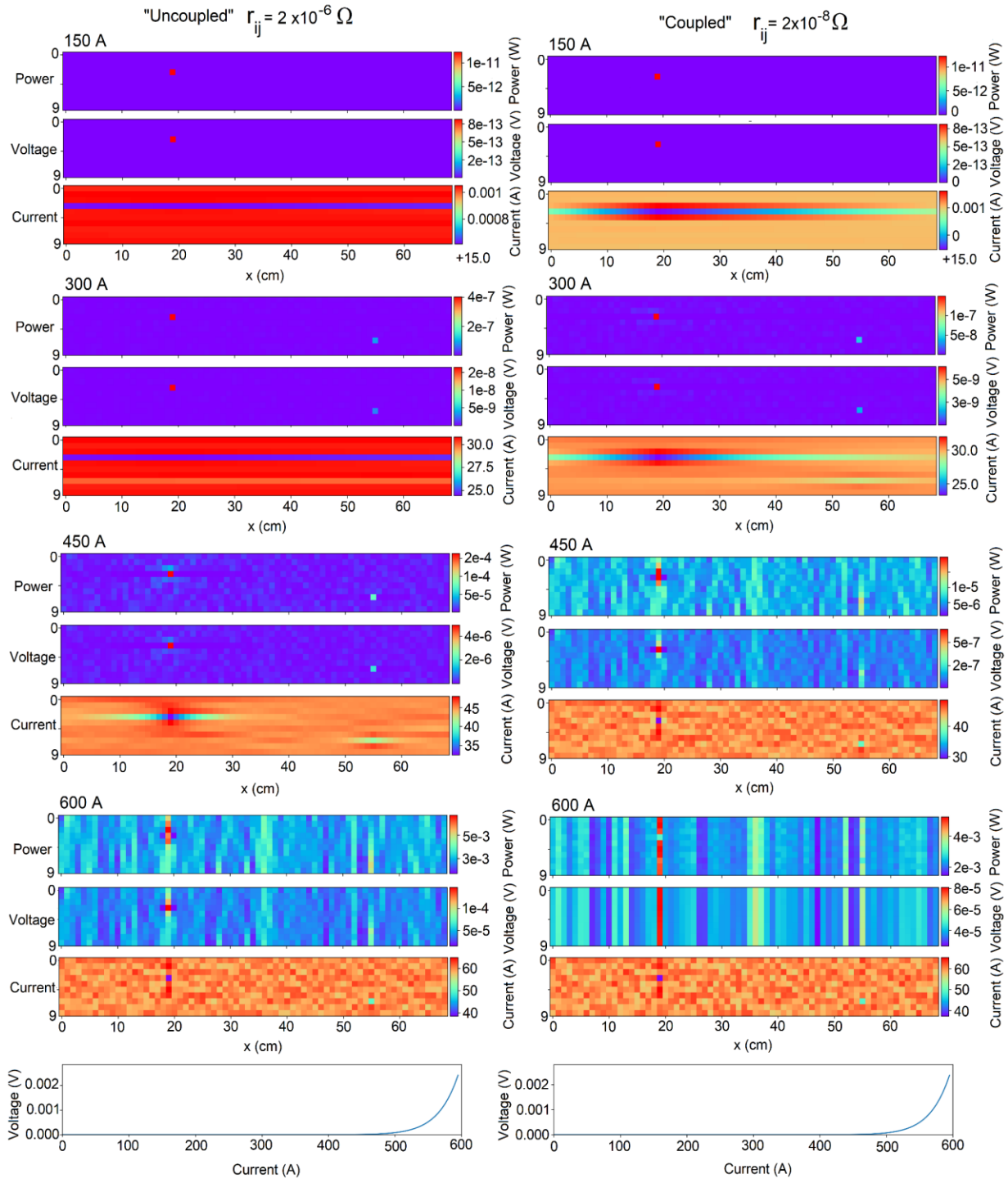

Fig. 2. Simulation results of the current re-distribution in the ten-tape stack. Colormaps show power, voltage, and current for each network element of the stack as a function of the applied current for 150 A, 300 A, 450 A, and 600 A (top to bottom). The bottom plots show the current-voltage characteristics of the stack. The left column shows simulation results for the "uncoupled" case of high current sharing resistance, while the right column shows the "coupled" case of low current sharing resistance.

exponent in (1) was taken as $n = 20$. The current sharing resistances were taken as $r_{ij0} + \Delta r_{ij}$, where $r_{ij0} = 2 \times 10^{-6}\ \Omega$ or $2 \times 10^{-8}\ \Omega$ and $\Delta I r_{ij}$ was taken as a random number in the [0, 0.05*r_{ij0}] interval, representing small resistance variations. The power dissipated in a single network element was calculated as a sum of powers dissipated in the voltage source and its adjacent current-sharing resistor (as outlined with a dashed line in Fig. 1). Termination resistances $R_{pos\_0\_0}$ … $R_{pos\_i\_0}$ and $R_{neg\_0\_j}$ … $R_{neg\_i\_j}$ were all taken equal to $10^{-9}\Omega$ (representing well-made solder joints). Two defects were assumed to be present in the stack, defined by a local drop in the critical current – one in Tape 3 at the location $i, j = (3,19)$ having $I_c\ (3,19) = 30$ A, and another one in Tape 7, at the location $I_c(7,55)$ = 40 A. In our simulation, the current source was ramped from 0 A to 600 A, with a step of 5 A, and voltage drop, current, and power dissipation were calculated for each node and plotted using color-map representation in Fig. 2, together with a simulated current-voltage characteristic of the entire stack (as measured between V_{pos} and the ground). The following observations could be made from this result. When current sharing resistance between the tapes is high ("uncoupled" case, left column), the initial current distribution is defined by the terminations, and it stays that way through a significant initial portion of the current ramp. Tapes containing defects with reduced current density carry less current over its entire length. As the net applied current increases, it increasingly flows around the simulated defects, and a more two-dimensional distribution emerges. Both simulated defects show up clearly in the distribution pattern. The current-shared length along the stack is also progressively shrinking around those defects. Finally, at 600 A, the current sharing occurs just at the defect vicinity, while a significant current fraction still flows through the defect itself, leading to very localized power dissipation. Voltage drop is still occurring in the very vicinity of the defect, and it is not "carried over" the thickness of the stack, thus making such cable prone to single-tape burnout. On the contrary, when current sharing resistance is low ("coupled" case, right column), the re-distribution around defects starts at a much lower applied current. The current-shared length along the stack shrinks earlier and more drastically, yielding a very localized voltage drop and power dissipation peak at the defect location already achieved at the intermediate (450 A) current. Interestingly, as the ramp progresses to 600 A, the current density around the defect becomes more significant than in the defect itself. This leads to the power being dissipated around the defect in a relatively larger volume. Voltage drop, on the other hand, becomes increasingly similar along the thickness of the stack at every longitudinal coordinate so that the defect-associated voltage drop is "carried over" the stack thickness. The simulated current-voltage characteristics appear very similar in both cases.

Our simulations clearly show that in the limit of poor current sharing (high r_{ij}) individual tape defects predominantly define the transverse current distribution across the stack thickness at low and intermediate net currents. The same transverse distribution may span longitudinally along the entire stack, provided resistances of terminations are small compared to tape resistances. It also implies that if tapes are uniform, but termination resistances vary from one tape to another, those termination resistances would define the current distribution across the stack. Thus, it is plausible to assume that varying termination resistances can drastically affect current dissipation distribution in the stack, including dissipation in and around defects localized in individual tape conductors. We will consider this problem next.

b. Dissipation and asymmetric current flow

To understand the effect of current sharing on dissipation in a composite conductor, let us first consider a trivial situation where the applied current I_0 should be split over two resistive paths R_1 and R_2 (Fig. 3a),

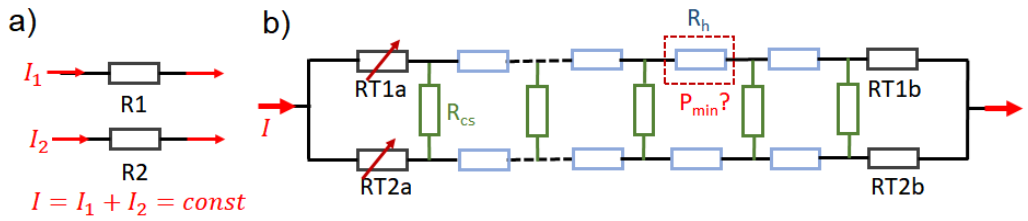

Fig. 3. Current distribution over two resistive paths. A) trivial case with no current sharing (b) a more realistic case for the current-shared conductor. A hot spot is denoted as R_h in the schematic.

and a question is asked for what distribution of currents I_1/I_2 the net power P_{net} dissipated in such system will be minimal. We get:

$$P_{net}(I_1) = I_1^2 R_1 + (I_0 - I_1)^2 R_2 \quad (2)$$

The minimum corresponding to $P'_{net}(I_1) = 0$ occurs when $I_1 = \frac{R_2}{(R_1+R_2)} I_0$, yielding voltage across the R_1 resistor of $V_1 = \frac{R_1 R_2}{(R_1+R_2)} I_0$, which is same as it would have been in case R_1 and R_2 are connected in parallel. Therefore, having the same voltage drop across both resistive branches minimizes the system net dissipation for a given net current, and this conclusion can be generalized to a case where the current is split over an arbitrary number n of the resistive branches. In application to composite HTS cables, however, minimizing net dissipation is far less important than minimizing dissipation in a developing local hot spot with a higher resistance than the rest of the cable. A schematic depicting the scenario of two conductors having current sharing resistances distributed between them and termination resistances is sketched in Fig. 3b, and the question may be asked if by varying values of termination resistors power dissipated in the hot spot R_h can be minimized for the applied net current I and stable distribution of the current sharing resistances.

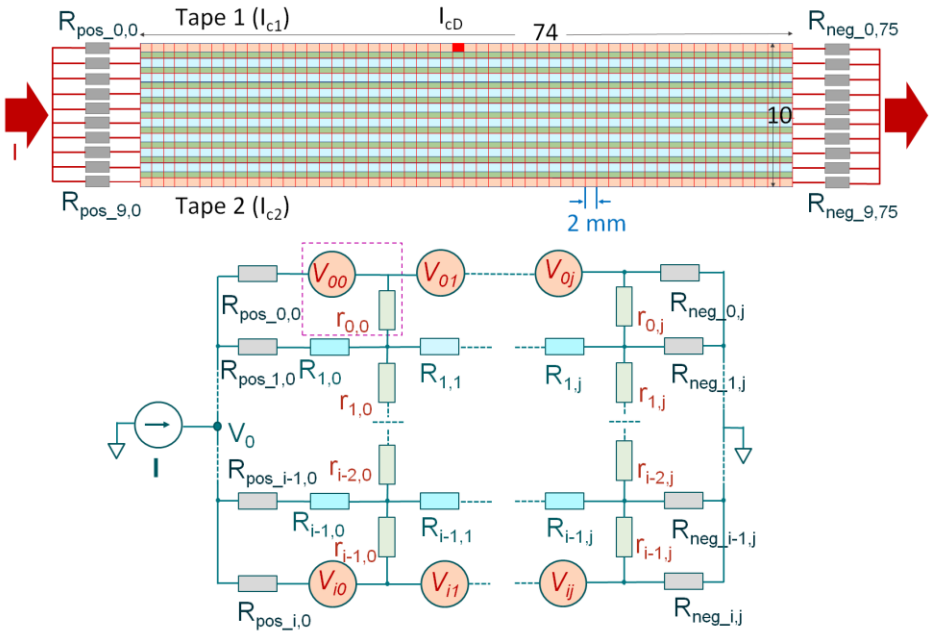

Fig. 4. A modified network model for the two HTS conductors current-shared through a bulk normal resistive material.

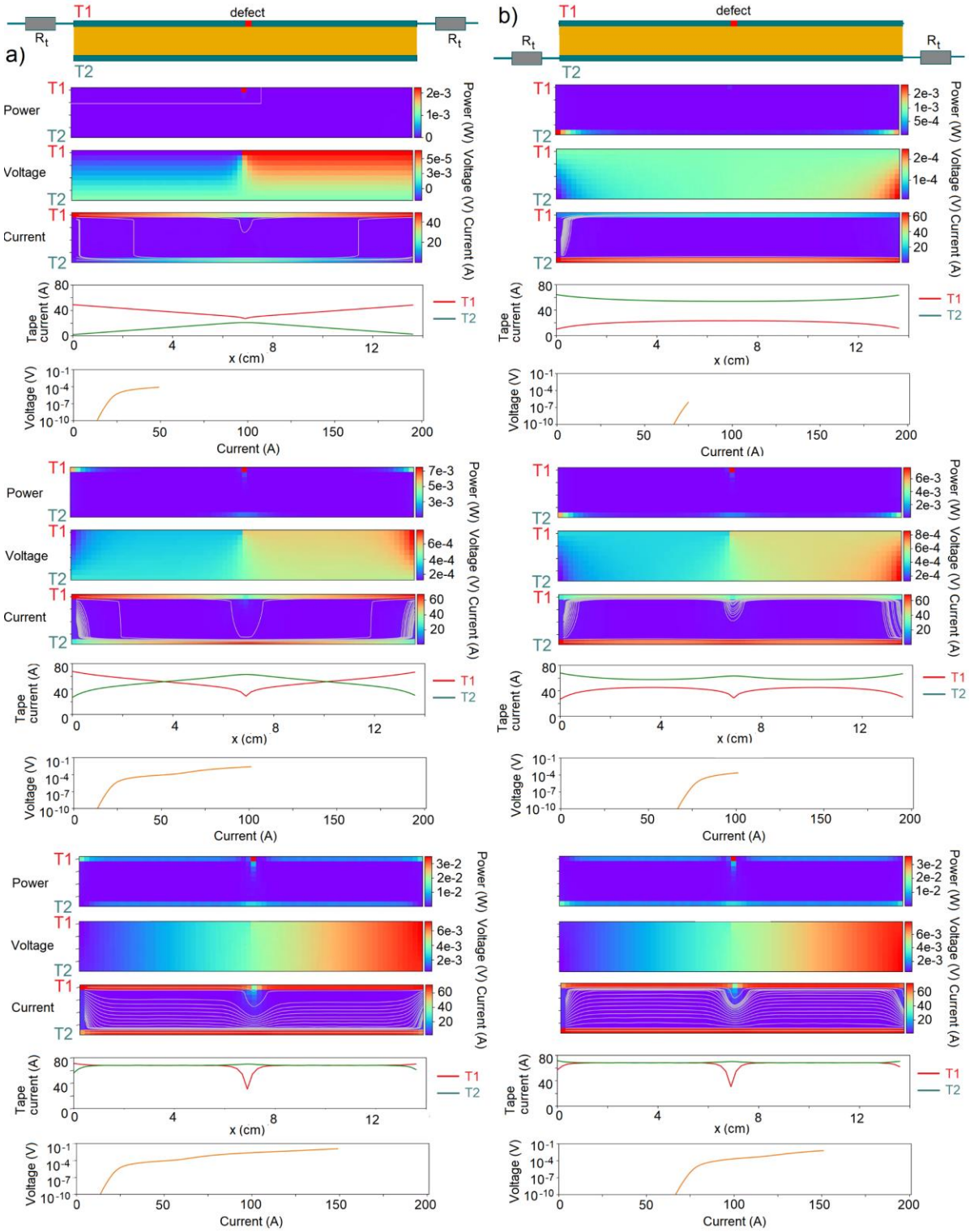

Fig. 5. Simulation results of the current re-distribution in a two-tape stack while ramping up the applied current. Colormaps show the power, voltage, and current distribution across the stack cross-section as a function of the applied current. The voltage of all elements is plotted as $(V_{ij} - V_0)$, where V_0 is the leftmost end of Tape 1. (a) Current is applied to Tape 1 having a defect. (b) Current is applied to Tape 2, which has no defect.

We have modified our network model to explore this problem further. The equivalent schematic of the modified model is shown in Fig. 4. The tape element voltage criterion U_0 was taken at 0.2 μV, assuming a physical length of a single element to be 2 mm and HTS conductor's voltage criterion of 1 μV/cm. The network portion representing bulk normal metal in-between the HTS conductors is a mesh of longitudinal resistances R_{ij} and transverse resistances r_{ij}, occupying j = [1, 8] space. We assumed bulk resistivity of the material similar to one the machinable "marine" yellow brass, which is $\sim 6 \times 10^{-8}\ \Omega\, m$ at room temperature and $\sim 3.2 \times 10^{-8}\ \Omega\, m$ at 77 K [31]. Then, using the 77 K resistivity value and assuming each resistive element being 2 mm long and 0.794 mm wide, we calculated $R_{ij} = 4.76\ x\ 10^{-5}\ \Omega$ and $r_{ij} = 7.8\ x\ 10^{-6}\ \Omega$. Like in the previously considered tape stack case, a small mutual variation of resistances, for this simulation in the narrower range of $0 - 0.5\ \%$, was assumed as it was found to improve the convergence speed of the network solver. A single defect was assumed to be present in one of the HTS conductors at the V_{9_37} position, represented by a local drop in the critical current. In the following simulation, we assumed the current was being injected and removed from just one of the tape conductors. In Fig. 5, results of the network modeling are shown for the two cases: (a) current is applied to and removed from the tape with a defect (Tape 1), and (b) current is applied to and removed from the tape without a defect (Tape 2). The first case was simulated by setting termination resistors $R_{pos\_7\_0}$, $R_{pos\_8\_0}$, $R_{neg\_7\_75}$ and $R_{neg\_8\_75}$ to 10^{-9} Ω, while keeping the rest of termination resistors at 1 Ω value. The second case was realized respectively by setting termination resistors $R_{pos\_0\_0}$, $R_{pos\_1\_0}$, $R_{neg\_0\_75}$ and $R_{neg\_1\_75}$ to 10^{-9} Ω, while keeping the rest of termination resistors at 1 Ω value.

The common features of the simulation result are as follows. Initially, the current is predominantly carried by Tape 1 it was applied to. However, as the current increases and approaches the critical current of the defective spot in Tape 1, a progressively larger fraction of the current becomes shared with the non-defective Tape 2 through the brass block. The voltage drop appears initially along the stack and is sharply localized at the defect location. As the current further increases, more current flows into the non-defective Tape 2, and its resistivity uniformly grows as its mean critical current is approached. Both tapes carry similar currents at high currents, except for the location near the defect, where local current re-distribution occurs. At the same time, voltage rises much more gradually along the length of the stack.

When current is applied to the non-defective Tape 2, it mostly stays in that tape until its mean critical current is reached, while voltage rises gradually along the stack length. Notably, since the defect is not within the current path, the voltage rise is substantially lower for the same applied current compared to the previous case. Then, as the applied current is ramped up, a redistribution across the brass block occurs, and increasingly more current flows into Tape 1. However, the presence of a defect limits the amount of current Tape 1 can carry, and a local current drop takes place around the defect at a higher applied net current, also leading to a more localized voltage drop across the defect region.

c. Heat dissipation in the hotspot

The difference in current flow evolution between the two cases considered above also yields a very different power dissipation at the defect at V_{9_37} position in the network. The latter has been calculated and plotted in Fig. 6 for the two cases described above and the case where the current was applied symmetrically to both tapes. Our calculation shows that if current sharing resistance is small, current distribution at terminations only plays a role for low applied currents. In contrast, local current sharing

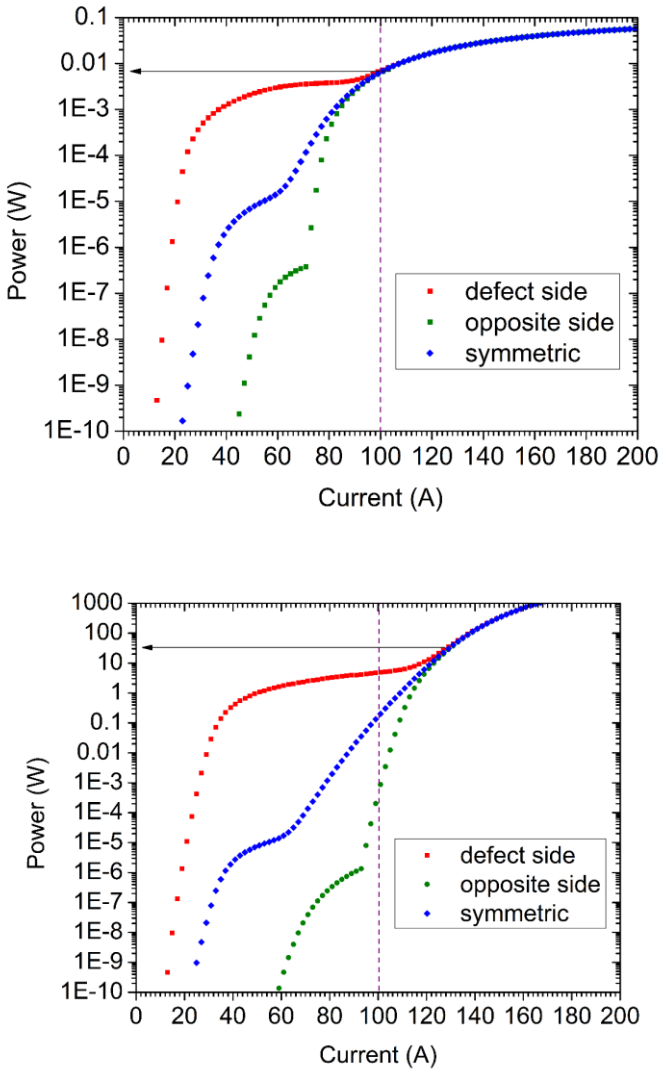

Fig. 6. (Top) Power dissipation at the defect in Tape 1 is calculated as a function of the applied current for three different current application points. When current is applied to the defective tape side, dissipated power at the defect location can be several orders of magnitude higher than if current is applied to the opposite, non-defective Tape 2. (Bottom) Same simulation, but assuming resistivity of the tape-separating block to be $10^5\rho_{brass}$. Lower degree of current sharing leads to a much larger difference in power dissipation between the considered cases.

defines power dissipation at the hot spot when the current approaches the critical value and beyond. On the other hand, as the degree of current sharing is reduced, the role of terminations increases and becomes dominant at a progressively lower fraction of the critical current. This indicates a practical opportunity to reduce hot spot power dissipation by re-distributing current flow at terminations and driving current away from the conductor component that experiences excess heat dissipation. To do so, two main conditions should be met. Firstly, practical devices for current flow control need to be implemented at the terminations of the multi-element conductor. Secondly, reliable monitoring of the current distribution between conductor components must be realized to provide real-time feedback for operating the controls.

Experimental

We conducted a series of experiments to demonstrate the active current control approach in practice and evaluate its efficiency in reducing power dissipation on the conductor components. First, we evaluated two MOSFET devices from different manufacturers and measured their operational parameters at cryogenic temperatures. An experimental setup was then built using two ReBCO tapes with limited current sharing between them, and MOSFET boards were installed at the tape terminals. Initially, we closed MOSFETs for one tape only while keeping them open for another tape, ramped up the current, and recorded individual tape current-voltage characteristics at 77 K. Next, we demonstrated an ability to balance currents equally between the tapes during the ramp by appropriately tuning the MOSFET gate voltages. Finally, we attempted to control the current distribution "on the fly" by actively varying MOSFET gate voltages during the ramp, and observing an increase in the apparent critical current of the tape assembly for the same voltage criterion, facilitated by the applied active control.

a. MOSFET devices for cryogenic current control

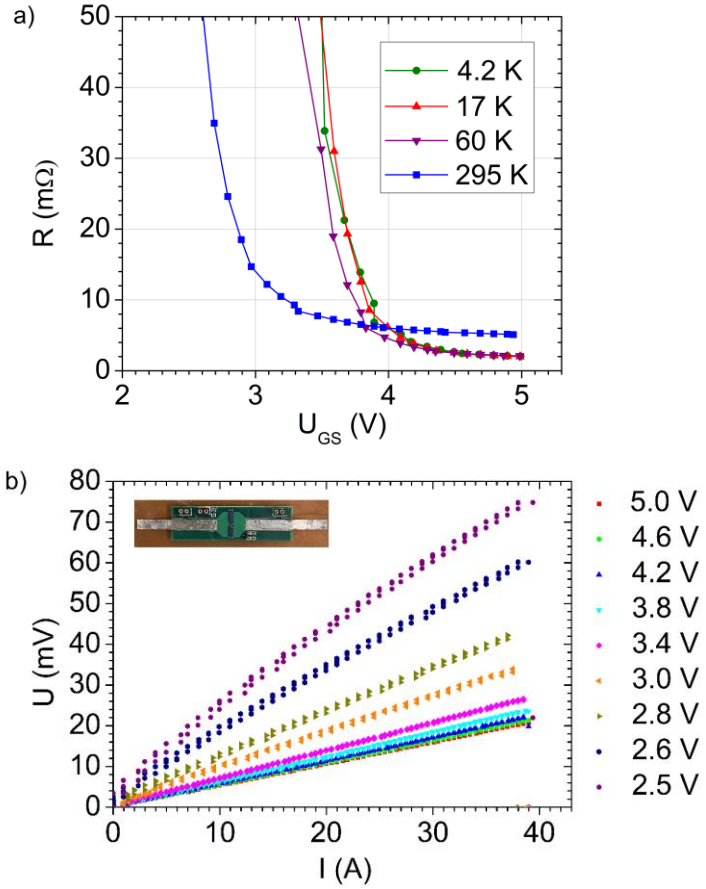

Fig. 7. (a) Resistance vs applied gate-source voltage traces for the GaN EPC2015C FET device measured at different background temperatures in helium gas atmosphere. The resistance of the device in the closed state saturates at ~2mΩ at an applied gate-source voltage of 5 V, and is practically independent of the temperature in the 4.2 – 60 K range. (b) Current-voltage characteristics of an assembly of four parallel-connected EPC2015C devices (shown in the inset) measured in liquid nitrogen at 77 K. Device resistance at a given gate voltage is only weakly dependent on the magnitude of the regulated current.

We have tested two MOSFET devices at cryogenic temperatures and assessed their suitability for proportional current control in superconducting circuits. Fig. 7a shows the resistance vs. gate voltage characteristics of the MOSFET device EPC2015C from Efficient Power Conversion Corporation [32], measured at several operating temperatures.

The characteristics of this device change from room temperature to cryogenic temperatures, exhibiting an increase in gate-source closing voltage U_{GS} for up to about 1 V. At the same time, the closed-state resistance of the device decreases from 5 mΩ at ambient temperature down to 2 mΩ at cryogenic conditions. The U_{GS} and the closed state resistance remain nearly temperature-independent in the 4.2 – 60 K range. When four MOSFET devices are connected in parallel, closed-state resistivity is reduced, and the operational current increases proportionally. We have assembled four EPC2015C devices on a single PCB and used superconducting 4 mm-wide HTS ReBCO tape for the board terminations. When operated in liquid nitrogen, it was possible to control and hold indefinitely currents up to 30 A per single device and ~100 A per four-device PCB assembly. The closed-state resistance of the assembly ($U_{GS} = 5\ V$) for the range of operational currents below 40 A was measured as 0.56 mΩ, and for the higher currents of 70-100 A, it decreased to 0.43 mΩ. Interestingly, the current-voltage characteristics of the device assembly (Fig. 7b) are nearly linear in the broad range of operational currents, especially for the fully closed state. This, in principle, allows for using voltage drop across the MOSFET to monitor the current flowing through it at any time provided U_{GS} is known.

We have also tested another device, an IAUC120N04S6L005 Si MOSFET from Infineon AG [33]. The device was found to control 100 A of current at 77 K and has a comparable closed-state resistance to the GaN device. A plot comparing the performance of both devices is shown in Fig. 8. However, tests at 4.2 K have shown a 5x increase of the closed-state resistances for this Si MOSFET compared to the 77 K value. This makes GaN FETs a more attractive option due to their broad-temperature operational capabilities.

b. Demonstration of the cryogenic MOSFET-based current control

To test the ability to control current distribution in multi-strand HTS conductors using MOSFETs proportionally, we have built an experimental setup shown in Fig 9a. Two 2 mm-wide HTS tape conductors

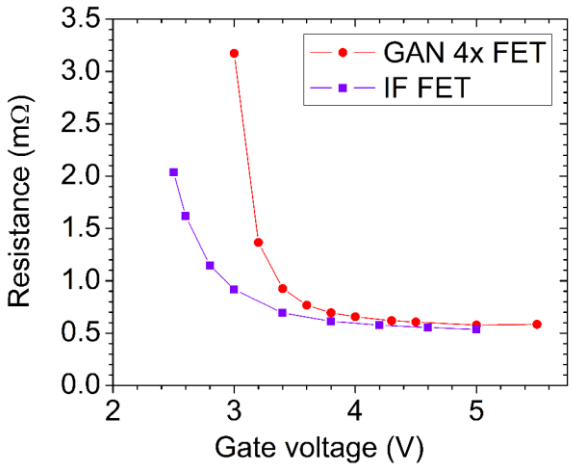

Fig. 8. Resistance versus gate-source voltage measured for the two devices (a 4x GaN EPC2015C assembly denoted "GAN 4xFET", and a single IAUC120N04S6L005 Si MOSFET denoted "IF FET") in liquid nitrogen at 77 K, for the constant current of 30 A flowing through the device. Both devices have a similar performance in the closed state, while the IF device exhibits a lower gate-source closing voltage U_{GS}.

were glued over 60 cm in length along their ReBCO sides to a brass block of 6.35 x 3.175 mm cross-section using silver epoxy and soldered to terminating PC boards using low-melt Field's alloy. Before affixing the tapes, a small point defect was introduced manually in the middle point of one of them (Tape 1) using a 0.8 mm diameter drill bit. The termination PC boards (Fig. 9b) were built with Infineon's IAUC120N04S6L005 Si devices and shunt resistors for the purpose of current control. An electrical schematic of the setup is shown in Fig. 9c. Also, voltage taps were added to each tape conductor. In the experiment, the setup was immersed in the liquid nitrogen bath. The current was supplied by TDK Lambda Genesys™ power supply, and tape voltages were monitored using Keysight 34420A 2-channel nanovoltmeter. Gate voltages for MOSFETs were supplied from the MC USB-3103 DAC, and shunt resistor voltages were monitored using NI USB-6225 ADC.

a. Individual tape characterization

Initially, we measured the current-voltage characteristics of each tape individually. For measuring just Tape 1, we supplied 5 V bias to gates G1 and G3, while Gates G2 and G4 were set to 0 V. Applying 5 V bias to the MOSFET gate brings it to the fully closed state of ~0.55 μΩ source-to-drain resistance as per data shown in Fig. 6. The power supply current was then ramped up linearly in 1 A steps, and tape voltages were monitored between V1 and V3 for Tape 1 and between V2 and V4 for Tape 2. In the second run, for measuring Tape 2, we set G2 and G4 bias at 5 V while keeping G1 and G3 at 0 V and repeated the current ramp. The results of both ramps are shown in the plots of Fig. 10a, showing currents flowing in and out of individual tapes (as derived from the voltages measured across 0.5 mΩ shunt resistors. In these tests, we assumed the power supply as our reference current source and made small (~1) scaling corrections to the measured individual currents, matching them with the power supply current in each case. The correction factors found with this procedure accounted for inevitable variation in shunt resistances and ADC channel calibration; these factors were then applied to all subsequent individual current measurements. Fig. 10b shows the current-voltage characteristics of individual tapes, normalized to the tape length. The tape critical current was determined using 0.1 μV/cm electric field criterion, yielding $I_{c(0.1)}$ =27.2 A for Tape 1 and $I_{c(0.1)}$ =30.7 A for Tape 2. When determined using 1 μV/cm electric field criterion, the critical currents were $I_{c(1)}$ = 37.9 A for Tape 1 and $I_{c(1)}$ = 35.9 A for Tape 2. Compared to the non-damaged Tape 2, the

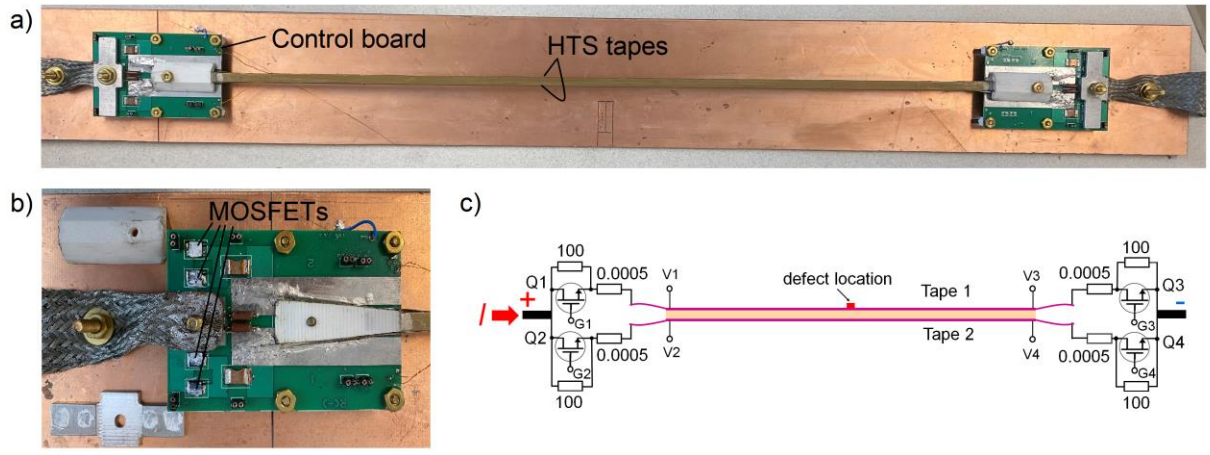

Fig. 9. (a) The test setup. (b) A MOSFET control board (protective covers removed). (c) Electrical schematics of the setup. Each MOSFET symbol in the schematic represents two IAUC120N04S6L005 devices connected in parallel.

artificial defect introduced in Tape 1 affected its critical current only slightly, while the n-value dropped by a factor of 2. In both ramps, voltages measured across the opposite (non-powered) tapes were negligibly small, indicating current flow was fully confined to the tape for which termination MOSFETs were set in the fully closed state. This test demonstrates a practical capability of performing *in-situ* I_c calibration and performance assessment for the individual conductors comprising an HTS cable for which MOSFET-based terminations have been implemented.

b. Balancing current distribution

In the next test, all four MOSFETs were initially fully closed by applying 5 V bias to gates G1-G4. This resulted in an unbalanced current flow distribution that, at low currents, was caused by the variation of resistances, and at high currents, also by the unevenly increasing resistance of the HTS tapes near their respective critical currents. Voltages across the tapes have been measured in this ramp. We then set the supply current to 20 A and tuned the MOSFET gate voltages V_{G1} and V_{G3} gradually down, increasing the net resistance in series with Tape 1, to uniformly balance the current between the tapes. The outcome of this tuning procedure resulted in gate voltages $V_{G1} = 3.06$ V, $V_{G2} = 5$ V, $V_{G3} = 3.32$ V, and $V_{G4} = 5$ V, balancing the currents with an accuracy better than 5% along the entire ramp. The current ramp was repeated, and the resulting tape voltages were measured again. In Fig. 11a, current ramps with unbalanced (left) and balanced (right) current distribution are shown. Once resistive transition starts in the tapes, current re-distributes across the brass spacer and a non-linear deviation of currents at the terminations from the mean value $I_{mean} = \frac{1}{4}(I_{T1\,in} + I_{T2\,in} + I_{T1\,out} + I_{T2\,out})$ occurs while the power supply current is being ramped up. In Fig 11b, these deviations are plotted for the balanced ramp, relative to I_{mean}. It can be seen that current re-distributes from Tape 1 into Tape 2 during the ramp, consistent with an earlier onset of the resistive transition in Tape 1. While deviations appear early in the ramp, at a supply current of ~ 20 A, they do not increase evenly, leading to a much larger deviation measured at the "out" end of the assembly. This suggests that net termination resistance that includes MOSFETs, shunts, and splices was somewhat higher at the "in" end of the assembly and, potentially, also indicates a presence of other defects in Tape 1 near its "out" end, in addition to the central artificial defect. The "in" and "out" traces for both tapes start diverging at ~ 100 s into the ramp, corresponding to the applied current of ~ 35 A. This current level corresponds to the very onset of resistance measured in the IV-curves for both tapes collected in both unbalanced and balanced ramps and shown together in Fig. 11c. In the unbalanced case, the resistive transition of Tape 1, when defined using the 0.1 μV/cm criterion, starts at $I_{c(0.1)} = 47.1$ A, and the transition in Tape 2 starts at $I_{c(0.1)} = 61.7$ A. Despite current sharing across the brass spacer, Tape 1 is still transitioning earlier than Tape 2, suggesting most heat dissipation would initially occur around the defect(s) in that tape. Balancing of the currents shifts the resistive transition in Tape 1 by $\Delta I_{c(0.1)} \approx 6$ A, and when the same current of 47.1 A is applied, the dissipation in Tape 1 decreases by ~ 50% (owing to a reduced Tape 1 current and voltage). Another positive consequence of current balancing was that the voltage drop implies that, on average, current flow through the brass spacer is also reduced, yielding reduced heat dissipation in the assembly. The shown in Fig. 11b current redistribution between individual HTS conductors can be readily used to detect an onset of tape resistance, analogously to the earlier proposed Hall sensor-based quench detection method [17], [18] also based on detecting the current imbalance. Furthermore, in the future, the current variation data, together with the *in-situ* measured current-voltage characteristics, may be fed into the real-time field-

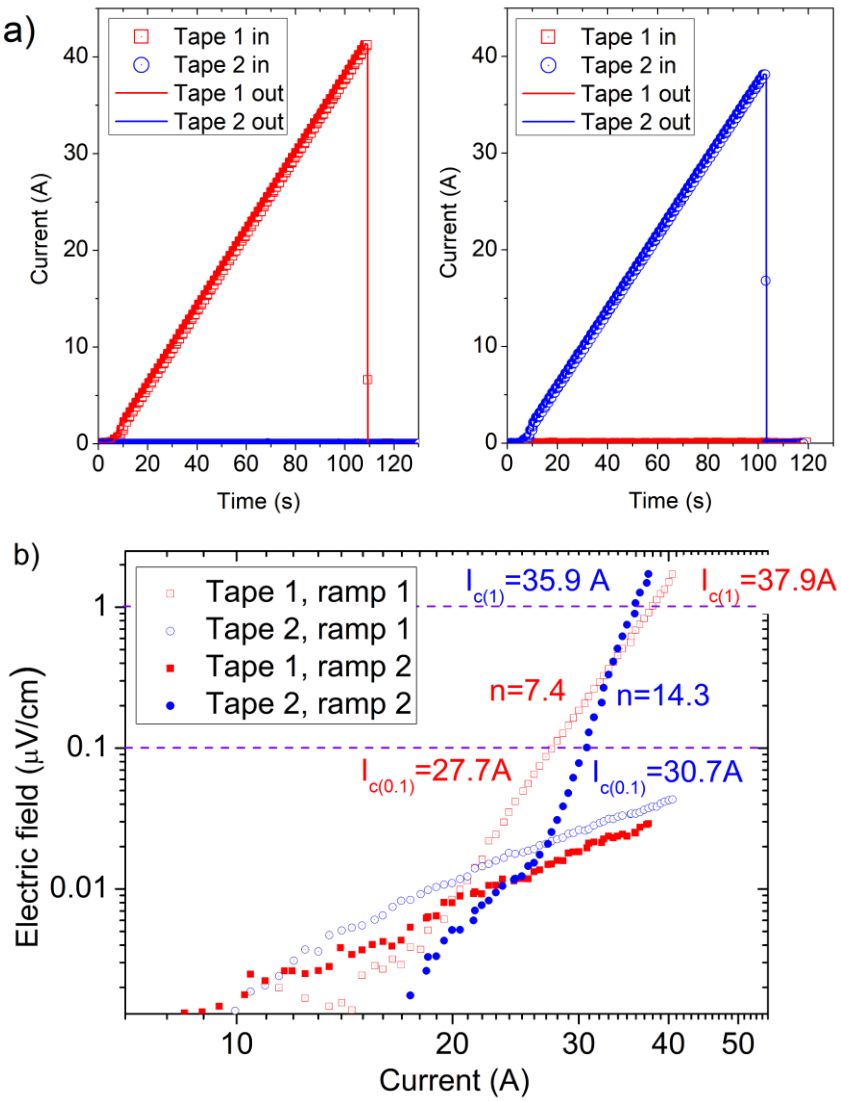

Fig. 10. (a) Currents flowing in and out of the individual tapes in the calibration ramps, as derived from shunt resistor voltages and corrected to match the power supply current. Supplying 0 V gate bias to the MOSFETs at both ends of an individual tape completely prevents the current from flowing into that tape. (b) Current-voltage characteristics of the tapes (normalized per 1 cm of the length) measured by individually powering the tapes using MOSFET termination boards.

programmable gate array (FPGA)-based hardware implementing the network model and providing continuous tape voltage estimates. This would eliminate the need for low-level monitoring of individual tape voltages. The voltage data, measured directly or network solver-derived, can then be used as input for controlling the MOSFET resistances, potentially enabling a closed-loop operation in future tests. It should be noted that once all MOSFETs have been calibrated for their source-to-drain resistance $R(U_{GS})$ as a function of gate voltage at the required operational temperature, one can use a voltage drop across the device to estimate current flowing through them accurately. This could be a viable alternative to using shunt resistors, as eliminating such resistors will simplify the control circuit and reduce its power dissipation. Another strategy for eliminating shunt resistors would be integrating an array of commercial

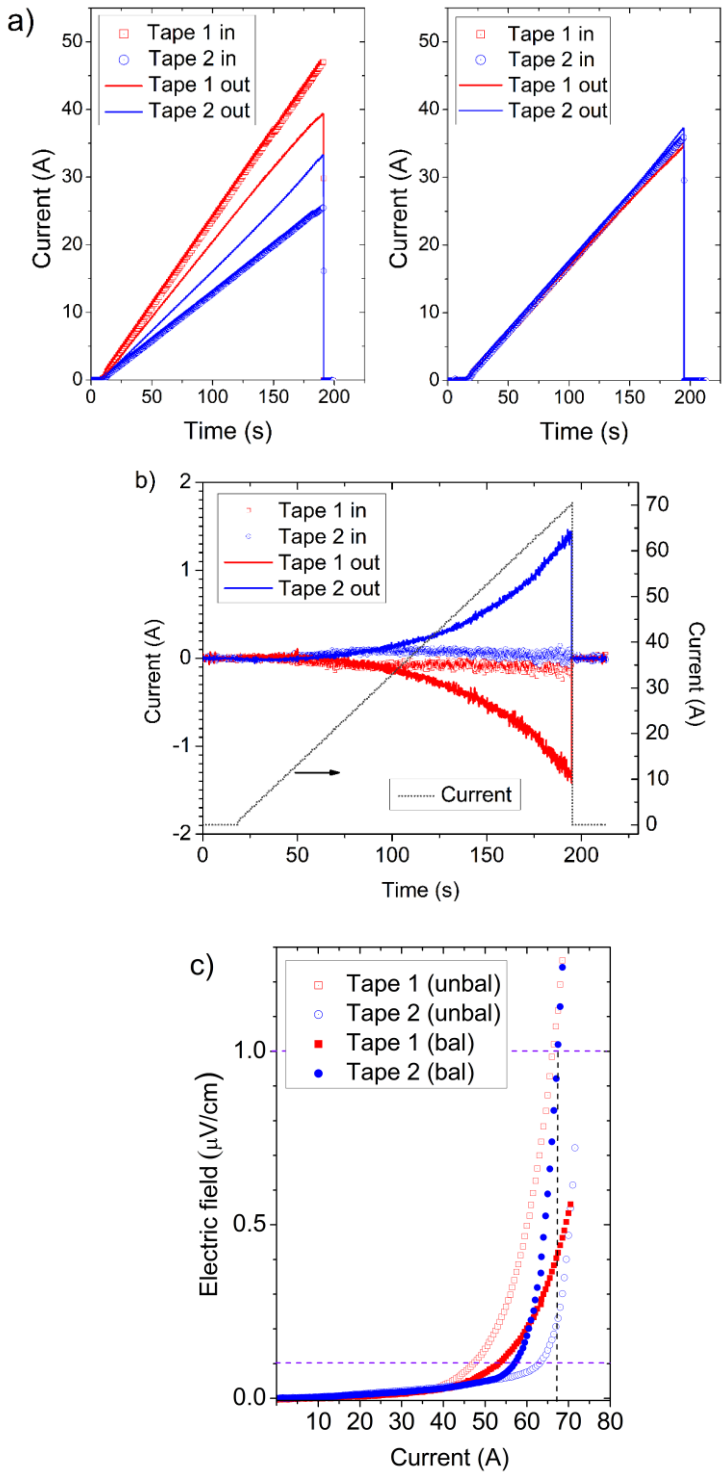

Fig. 11. (a) Plots of current flowing in and out of each tape as a function of time for the unbalanced (left) and balanced (right) cases. (b) Deviation of the current in each branch from the mean value, indicating an onset of non-linear resistance. The net current provided by the power supply is also shown in the same plot. (c) Current-voltage characteristics of individual tapes measured in both unbalanced and balanced ramps.

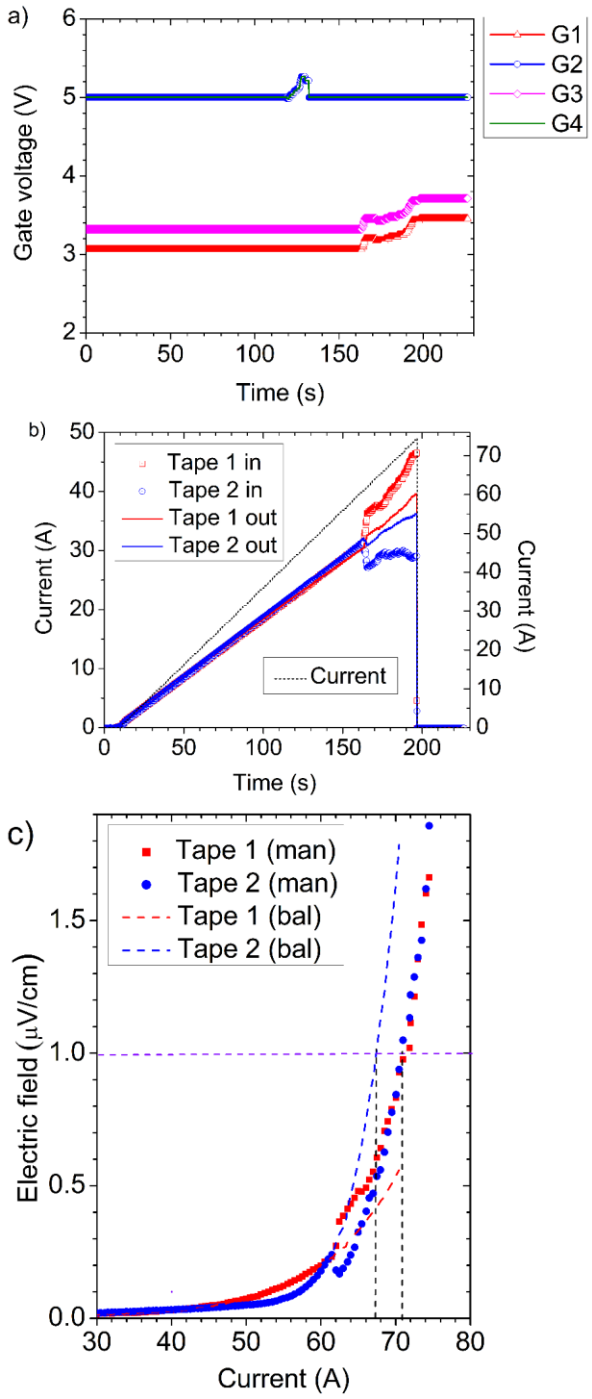

Fig. 12. (a) MOSFET gate voltages plotted as a function of time. V_{G1} and V_{G3} voltages were tuned manually to vary MOSFET resistances, aiming at equalizing voltages across the two HTS tapes for driving currents above 60 A. A small upwards excursion of V_{G2} and V_{G4} seen at ~120 s resulted from system testing and did not affect current distribution since MOSFETs Q2 and Q4 remained fully closed at this gate voltage level. (b) Currents flowing in and out of each tape during the ramp are plotted as a function of time. The initially balanced state was adjusted manually starting from ~ 160 s into the ramp (c) Current-voltage characteristics of the tapes in the manually-adjusted case (solid symbols) compared to those in the current-balanced state (dash lines).

low-cost GaAs Hall sensors into the terminals [19] and relying upon an inverse Biot-Savart solution to accurately determine absolute currents flowing in each component.

c. Balancing the voltage drop interactively

MOSFET gate voltages must be varied in real-time to minimize dissipation along the current ramp to benefit fully from active current controls. While we have not yet realized a closed-loop control system, the following simple experiment was conducted as proof of principle. The MOSFET gates were reconnected from the digital-to-analog converter (DAC) to a multi-channel regulated power supply, and an attempt was made to vary V_{G1} and V_{G3} voltages manually during the current ramp, aiming at keeping voltages across both tapes as similar as possible. In Fig. 12a, gate voltages and in Fig. 12b, currents through corresponding MOSFETs are plotted as a function of time for a linear current ramp from zero to 74 A. The circuit retained the balanced current flow up to ~60 A of the applied current, yielding the same tape voltages for the 0-60 A current range as those recorded in the previous test shown in Fig 11. In that previous test, above 60 A, Tape 2 voltage would grow faster than Tape 1 voltage. However, in the present test, we visually monitored Tape 1 and Tape 2 voltages in the real-time LabView plot, and aimed at keeping those voltages as similar as possible by manually tuning V_{G1} and V_{G3} with knobs of the regulated power supply during the rest of the current ramp. The resulting current-voltage plot for both tapes is shown in Fig 12c. A voltage drop of 1 μV/cm was reached nearly simultaneously in both tapes at ~70.9 A, which brought the apparent critical current of the assembly up from ~67.3 A ($I_{c(1)}$ of Tape 2 in the balanced case) and effectively reduced power dissipation in Tape 2 by nearly a factor of two, compared to dissipation in the "balanced" case at the same magnitude of the applied driving current.

Future developments

Our next step will be developing larger-scale control boards with ~20-30 individual MOSFET devices operating in parallel to control currents in the kA range while distributing heat dissipation over a larger surface area. We plan to use those boards to drive multi-component HTS cables and small HTS magnets wound with such cables. We aim to achieve a closed-loop control operation by implementing a real-time feedback system that would take the current distribution as input. At the same time, an algorithm solving for power dissipation in cable components will generate the output for the active controls aimed at reducing the dissipated power. The algorithm could be based on real-time solving of a network model for the multi-component cable system on a microprocessor or FPGA, as discussed in [18], and further speed-enhanced by a machine learning component that is pre-trained on a set of the network model solutions.

In a large magnet system built with a long HTS conductor with multiple local defects, measuring current distribution alone may be insufficient for adequate protection, and an addition of real-time distributed temperature sensing (fiberoptic [34],[35], ultrasonic [36], or RF-based [37]) could be required. Recently, a quench avoidance strategy has been put forward that relies on monitoring a slow temperature rise of the HTS conductor while still operating in a stable dissipative regime and evaluating conductor proximity to the thermal runaway using a pre-calibrated heat balance model [38]. Current distribution control comes naturally as a desired component of such a quench avoidance system. The closed-loop feedback would then compare real-time local temperatures measured along the conductor components to the pre-programmed runaway temperatures and actively vary the current distribution to increase the available thermal margin at the "worst" hot spot locations.

Notably, when the net current in a cable is not being varied, the time constant for current re-distribution between cable components is defined only by a relatively small mutual inductance. Since MOSFETs can operate at MHz frequencies, fast AC modulation of current distribution may bring additional benefits to HTS magnet operation and protection. For example, a small modulation could enable an AC-voltage-based quench detection with high noise rejection. A more significant AC modulation of the current distribution can generate hysteretic, inter-component, and eddy current losses in the conductor, potentially enabling a protection path similar to the CLIQ scheme [39]. AC modulation may also be explored to improve the HTS magnet field quality [40] by facilitating magnetization decay in tape-based HTS conductors [41], [42].

Conclusions

Using network modeling, we explored how current distribution in HTS tape stacks is affected by an interplay between current sharing and termination resistances. We calculated current, voltage, and power distribution in a current-driven HTS tape stack. In a high current sharing situation, for low driving current, we found that individual tape defects largely define current distribution across the stack thickness and maintain this distribution unchanged along the stack length. The dissipation is mainly localized within one tape at the defect location. However, at high driving current, current distribution varies significantly along the stack length, while the dissipation due to an individual tape defect spreads more evenly across the stack thickness at the defect location.

In a poor current sharing situation, a non-optimal distribution of termination resistances may cause excessive localized heating dissipation at the defect locations. Simulations were carried out for the assembly of two HTS tapes that are current-shared through a normal metal spacer. When a single defect with a lower critical current is present in one of the tapes, local power dissipation in such a defect was found to vary by orders of magnitude, depending on whether the driving current was applied to the defective tape side, the opposite (non-defective) tape side, or symmetrically to both sides. The dissipation in the defective tape can thus be drastically reduced by re-distributing current towards the non-defective one during current ramping.

We experimentally realized such a scheme for current distribution control using power MOSFET assemblies suitable for cryogenic operation. Two ReBCO tapes were current-shared through a brass block, and MOSFET assemblies were installed at their termination. We demonstrated the ability to vary dissipation in this two-tape system by balancing the current flow distribution using MOSFET-based control of termination resistances. An additional reduction in dissipation by a factor of two was achieved by implementing a rough control of the termination resistances “on the fly” to keep tape voltages in balance during the ramp.

We outlined our perspective on further developing the active control-based magnet protection methodology to control higher currents and realize closed-loop feedback. We also discussed the additional benefits of implementing AC modulation of current distribution for improved magnet quench protection and field quality.

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that they have no conflict of interest. The data supporting this study's findings are available from the corresponding author upon reasonable request.

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