Title

Structure Design, Process Development, and Integration of MIM Capacitor in Si-IF for Wafer-Scale System

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Publication Date

2024

Peer reviewed|Thesis/dissertation

UNIVERSITY OF CALIFORNIA

Los Angeles

Structure Design, Process Development, and Integration of MIM Capacitor in Si-IF for Wafer-Scale System

A thesis submitted in partial satisfaction of the requirements

for the degree Master of Science

in Materials Science and Engineering

by

Cheng-Ting Yang

2024

ABSTRACT OF THE THESIS

Structure Design, Process Development, and Integration
of MIM Capacitor in Si-IF for Wafer-Scale System

by

Cheng-Ting Yang

Master of Science in Materials Science and Engineering

University of California, Los Angeles, 2024

Professor Subramanian Srikantes Iyer, Chair

At the UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS), we are focused on advancing wafer-scale systems with fine-pitch, scalable interconnections to meet the growing demands of artificial intelligence (AI) and high-performance computing (HPC). One of the main challenges in our Silicon Interconnect Fabric (Si-IF) wafer-scale system is the integration of capacitors to ensure efficient power delivery and maintain signal integrity. While traditional printed circuit boards (PCBs) easily achieve desired capacitance with discrete components, integrating capacitors into the Si-IF presents significant challenges in both structure design and fabrication processes. This thesis explores the design, development,

and integration of Metal-Insulator-Metal (MIM) capacitors into the Si-IF platform. The work begins by selecting appropriate dielectric and electrode materials for the capacitors, considering their electrical performance and compatibility with the Si-IF process. A comprehensive process flow is developed, from initial structure design to fabrication, with a focus on optimizing the capacitor structure to improve process feasibility. The results demonstrate that the proposed MIM capacitor structure can be successfully integrated into the Si-IF platform. Electrical characterization of the test structures further validates the performance and effectiveness of the design. This research provides a viable path for incorporating capacitors into wafer-scale Si-IF systems, offering a solution to the power and performance challenges faced by AI and HPC applications.

The thesis of Cheng-Ting Yang is approved.

Mark S. Goorsky

Jenn-Ming Yang

Subramanian Srikanteswara Iyer, Committee Chair

University of California, Los Angeles

2024

Dedicated to my family

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ACKNOWLEDGEMENTS

First, I would like to express my deepest gratitude to my advisor, Prof. Subramanian S. Iyer, for his invaluable guidance and support throughout this journey. His mentorship has allowed me to grow as a researcher, while his encouragement to explore ideas independently has been truly inspiring.

I also extend my sincere thanks to Professors Jenn-Ming Yang and Mark Goorsky for serving on my thesis committee. I am grateful for their valuable time and insightful suggestions, which have greatly enriched my academic journey during these past two years in the Department of Materials Science and Engineering at UCLA.

A special thanks goes to Haoxiang Ren and Jui-Han Liu, who have been not only friends and colleagues but also mentors. Their assistance and advice have been invaluable. Our conversations about experiments and technology, even outside of work, have been a great learning experience for me.

I would like to extend my sincere appreciation to my colleagues and lab mates. Working alongside Haoxiang Ren, Jui-Han Liu, Vineeth Harish, Krutikesh Sahoo, Golam Sabbir, Randall Irwin, Henry Sun, Guangqi Ouyang, Siyun Qiao, Ziyi Guo, Xiaoya Chen, Mansi Sheth, and Tanmay Konnur has been an incredible experience. I have learned so much from each of you, and our discussions have been invaluable. I will never forget the times when we faced

challenges—you were always there with encouragement and advice.

I am deeply grateful to my girlfriend, Rou-Fang Pan, for standing by my side during the difficult times. Last but not least, I want to thank my parents, Jenn-Fa Yang and Yuan-Hong Lee, whose unconditional love and encouragement allowed me to pursue my dreams. I am forever grateful to have you as my parents. Finally, I would like to thank my sister, Yi-Ting Yang, who has always cared for me and provided valuable advice throughout this journey.

CHAPTER 1 INTRODUCTION

1.1 Silicon Interconnection Fabric (Si-IF) technology overview

Silicon Interconnection Fabric (Si-IF) technology represents a significant advancement in the field of heterogeneous integration, addressing the growing demands for high-performance, scalable, and efficient interconnects in modern electronic systems. The core motivation for developing Si-IF technology stems from the limitations of conventional packaging and interconnect methods. Traditional approaches often struggle to meet the performance requirements of advanced applications such as artificial intelligence (AI), high-performance computing (HPC), and data-intensive tasks[1]. Si-IF technology provides a scalable interconnection platform that can support fine-pitch bonding (sub-10 μm), and high-density interconnects, enabling the integration of chips, dies, chiplets, and other components into a cohesive system, Figure 1 shows how dielets are bonded and integrated on Si-IF.

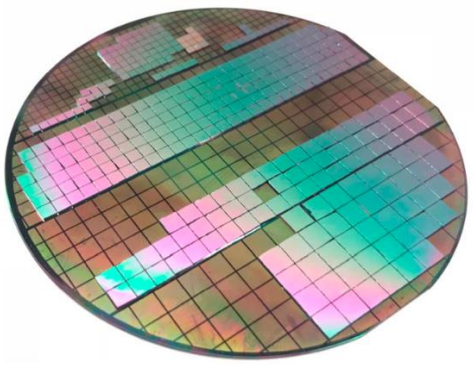


Figure 1. Fine-pitch integration of dielets on Si-IF using 10 μm pitch interconnection [2]

One of the key advantages of Si-IF technology is its ability to facilitate heterogeneous

integration, which allows the combination of different types of components—such as processors, memory, sensors, and specialized accelerators—onto a single substrate. Furthermore, the integration can accommodate dies with different BEOL processes such as Cu, Al, and Au pads bonding on Cu pillars on Si-IF, which is shown in Figure 2.

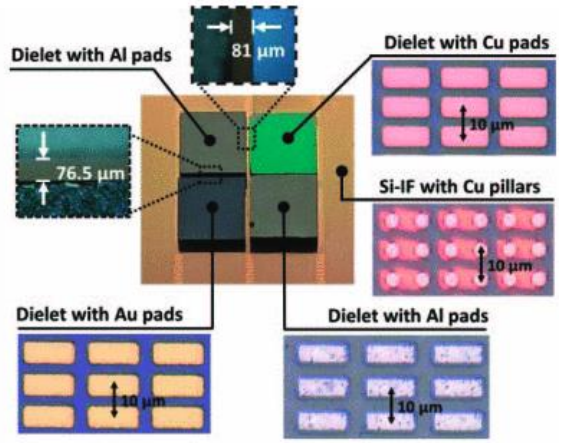


Figure 2. Heterogeneous integration of different BEOL dielets on Si-IF [3]

This integration capability is crucial for optimizing system performance, as it enables the co-location of components with diverse functionalities by reducing inter-dielet spacing[4], thereby reducing latency and improving data transfer rates while communicating between different dies. Moreover, by leveraging silicon-based substrates and decreasing communication links between dies, Si-IF can achieve lower power consumption and higher bandwidth compared to traditional interconnect solutions[2].

1.2 Motivation of the work

The objective of Si-IF technology is to replace traditional printed circuit boards (PCBs) by enabling the direct integration of dies onto a wafer-scale system, eliminating the need for interposers. This approach seeks to minimize interconnection distances, thus reducing latency and enhancing power efficiency. However, Si-IF technology is not yet capable of fully replicating all the functions of PCBs. PCBs can easily accommodate various circuit functions due to their larger pitch and bond pad sizes, which allow for the attachment of discrete components like resistors, inductors, and capacitors through surface-mount technology (SMT) or traditional soldering techniques. To further advance Si-IF as a cutting-edge technology platform, the integration of integrated passive devices (IPDs) into the BEOL process is essential. As power efficiency becomes increasingly crucial in advanced packaging, having built-in capacitors along the power delivery network (PDN) is necessary for efficient power delivery.

Therefore, investigating the process of integrating capacitors into current Si-IF technology is crucial for developing further applications and enhancing performance.

1.3 Capacitor integration in modern packages

The integration of capacitors in modern packaging technologies has become a critical factor in enhancing power delivery and signal integrity for high-performance applications. Recent approaches to integrate capacitors are shown in Figure 3, and the comparison is collected in Table 1.

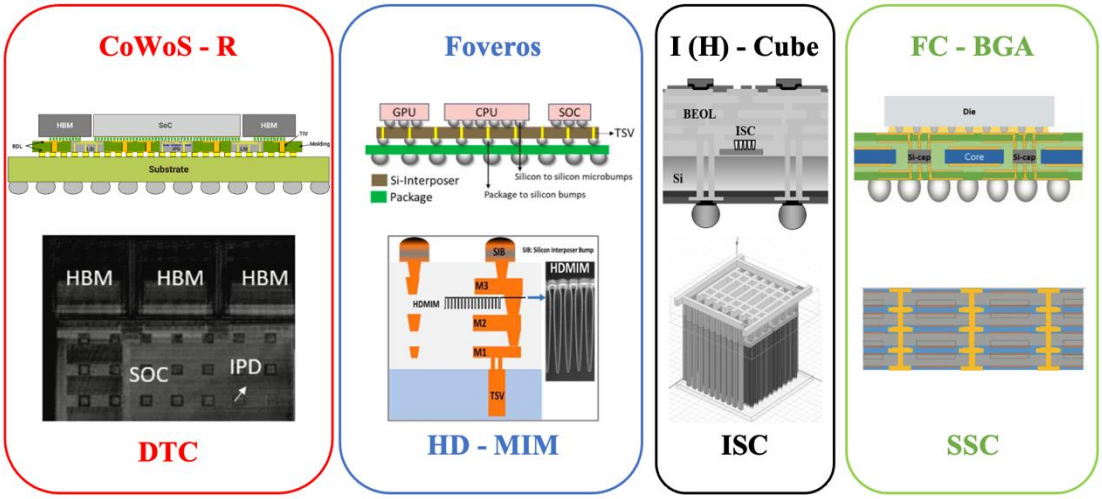


Figure 3. Different methods for integrating capacitors into packages with various architectures

Package	**CoWoS-R**	**Foveros**	**I (H)-Cube**	**FC-BGA**
Company	TSMC	Intel	Samsung	Samsung
Substrate	Silicon interposer	Silicon interposer	Silicon interposer	Organic thick core substrate (TCS)
Capacitor type	Deep trench capacitor **(DTC)**	High Density Metal-insulator-metal **(HD - MIM)**	Integrated stacked capacitor **(ISC)**	Stacked Silicon Capacitor **(SSC)**
Capacitor location	On the substrate of interposer	Wiring level of interposer	Wiring level of interposer	In the substrate
Capacitance density ($nf/\mu m^2$)	1.5×10^{-3} [5]	5×10^{-4}	$> 2.5 \times 10^{-4}$, $< 2.5 \times 10^{-3}$ [6]	1.5×10^{-3} [7]

Table 1. Comparison of advanced approaches to integrating capacitors into the package

While the deep trench capacitor (DTC) offers the highest capacitance density, its fabrication process is relatively complicated, time-consuming, and costly. Therefore, the MIM capacitor is chosen for this work due to its relatively simpler and more cost-effective fabrication process. Moreover, unlike DTC, MIM capacitors can be built at the wiring level, making the

substrate design more flexible. This flexibility allows MIM capacitors to be placed closer to each die or IC, improving their effectiveness in decoupling signals compared to DTC.

1.4 Organization of this thesis

In this thesis, Chapter 1 introduces the concepts of Si-IF and integrated passive devices (IPD). Chapter 2 focuses on the design, structure, and material selection for the MIM capacitor. Chapter 3 details the process of integrating the MIM capacitor into the Si-IF platform. In Chapter 4, the process development, structure optimization, and electrical characterization are explored. Finally, Chapter 5 provides a summary of the conclusions and outlines potential future work.

CHAPTER 2 STRUCTURE & DESIGN OF MIM CAP PROTOTYPE ON Si-IF

2.1 MIM capacitor structure

Several Cu BEOL-compatible MIM capacitor structures and processes have been collected and compared in the paper[8] and are illustrated in Figure 4. However, due to tool limitations and process feasibility, not all structures can be integrated into the Si-IF process flow. For example, structures (a)[9], (b)[10], and (f)[11] require more than two wiring levels to integrate MIM capacitors. This could induce unwanted stress and cause additional warpage, especially when manufacturing a wafer-scale substrate. Structures (d)[12] and (e) require excellent CMP control on the electrode, dielectric, and Cu; otherwise, dishing or defects might occur, impacting further processing. Structures (g)[13] and (h)[14] demand very precise etching recipes and technique control.

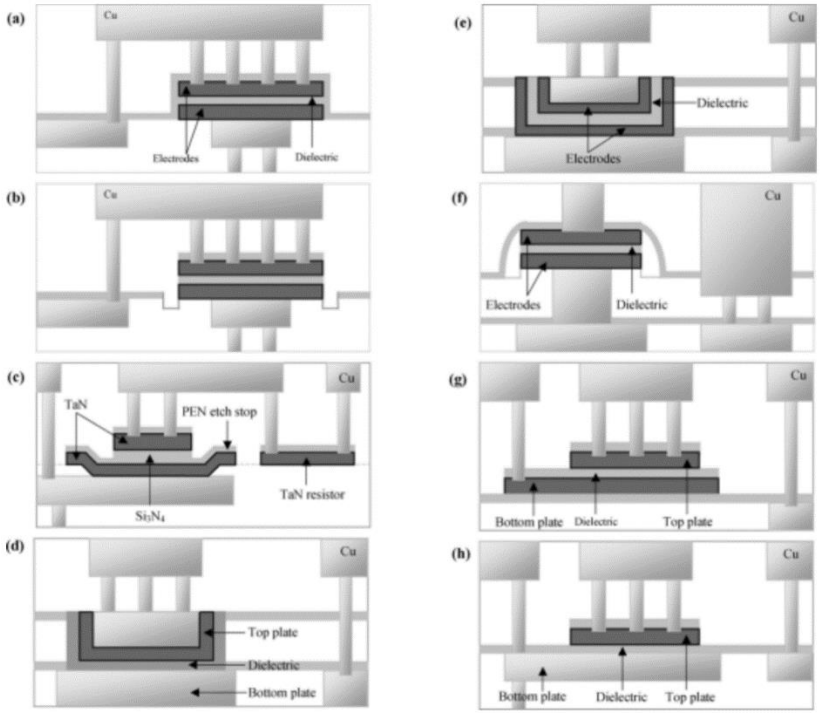


Figure 4. Schematic pictures of various MIM capacitors proposed for the Cu BEOL [8]

Given these considerations, two structures, shown in Figure 5, are proposed in this work to validate and test process feasibility on Si-IF. The material selection, processes, and comparisons will be discussed in the following chapters.

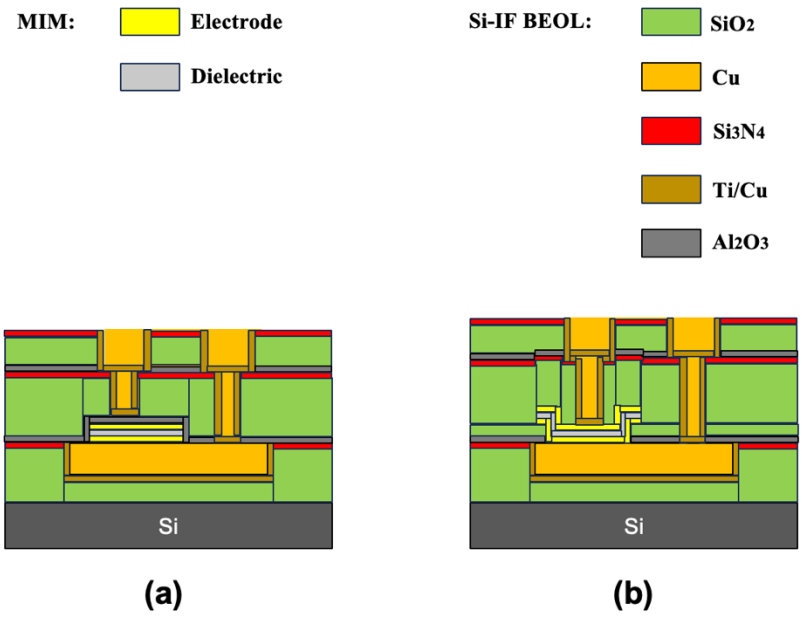


Figure 5. MIM capacitors integration in this work: (a) parallel capacitor (b) parallel capacitor with oxide passivation on Cu

2.2 Electrode and Dielectric material selection

2.2.1 Dielectric material selection

Hafnium Oxide (HfO_2) is widely utilized in CMOS technology as a high-κ gate dielectric material due to its relatively high dielectric constant, which directly influences the capacitance density of the device based on equation (1), in which C is the capacitance, κ is the dielectric constant of dielectric material, ε_0 is the permittivity of free space, A is the area of the capacitor and d is the distance between two parallel electrode plate. The higher the dielectric constant, the greater the capacitance density achievable, making HfO_2 an attractive choice for applications requiring high capacitance in a compact area[15].

$$C = \kappa\varepsilon_0 \frac{A}{d} \quad (1)$$

However, HfO_2 is not without its challenges. The material is known to suffer from defects within its thin films, leading to issues such as dielectric breakdown, elevated leakage current, and other reliability concerns. These issues stem from the presence of bulk-dielectric traps near the dielectric/metal interface, which can modulate the charges in the capacitor and adversely affect its performance.

To mitigate the reliability issues associated with HfO_2, dielectric stacking structures of Al_2O_3-HfO_2-Al_2O_3 (AHA), and Al_2O_3-HfO_2-Al_2O_3-HfO_2-Al_2O_3 (AHAHA) are also adopted in this work. The inclusion of Al_2O_3 layers in the stack helps address the deficiencies of HfO_2 by improving leakage current performance and enhancing the overall breakdown voltage of the dielectric structure.

The band diagram of TiN, Al_2O_3, and HfO_2 is shown in Figure 6, illustrating the impact of the bandgap of the electrode and dielectric layer on the performance of MIM capacitors and. The barrier heights at the interfaces (TiN/Al_2O_3 and TiN/HfO_2) are crucial in determining the leakage current through the capacitor. Higher barrier heights generally lead to lower leakage currents because they make it more difficult for charge carriers to tunnel through the dielectric layer. Al_2O_3, with its larger bandgap, adds an additional barrier, which effectively reduces leakage when combined with HfO_2. This combination enhances the breakdown voltage and provides better reliability under high electric fields.

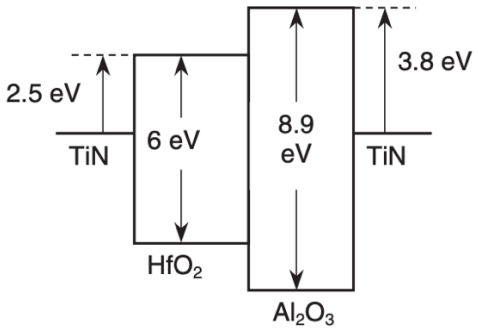


Figure 6. Band diagram for stacked Al_2O_3 - HfO_2 with TiN electrodes [15]

Al_2O_3, while having a lower dielectric constant compared to HfO_2, which is shown in Table 2, offers significant advantages such as a wide bandgap, high field strength, and excellent thermal stability. When combined with HfO_2 in a stacked configuration, these properties contribute to an improved balance between high capacitance density and low leakage current.

Dielectric Material	Dielectric Constant (κ)	Band Gap Energy (eV)
HfO_2	18 - 25	5.3 - 5.9
Al_2O_3	9 - 11	8.8 - 9.0
ZrO_2	18 - 25	5.2 - 7.8
SiO_2	3.9	8.9
Ta_2O_5	25	4.5
TiO_2	80 - 100	3.0 - 3.2
Si_3N_4	7 - 8	5.0 - 5.3

Table 2. Common materials used in MIM capacitors or other high-k application

2.2.2 Electrode material selection

The selection of electrode materials significantly affects the performance of MIM capacitors. The work function of an electrode material plays a pivotal role in determining the barrier height at the metal-dielectric interface, which in turn influences the breakdown voltage. The barrier height (Φ_B) is given by the difference between the work function of the electrode (Φ_M) and the electron affinity of the dielectric (χ), as shown in equation (2):

$$\Phi_B = \Phi_M - \chi \quad (2)$$

High work function electrodes are crucial in creating a larger barrier height at the interface, which significantly reduces the likelihood of electron tunneling through the dielectric layer. This reduction in electron tunneling effectively decreases leakage current, making these materials highly desirable for applications that require low leakage current and high reliability. On the other hand, low work function electrodes result in a smaller barrier height, which facilitates easier electron tunneling. This, in turn, increases leakage current, making low work function materials less ideal for Metal-Insulator-Metal (MIM) capacitors where low leakage current is a critical requirement.

Reactive metals that easily form interfacial compounds or diffuse into the dielectric, such as Al and Cu, tend to introduce defects in the dielectric layer. This alters electrical characteristics such as capacitance density. In contrast, non-reactive electrodes like Pt, Au, and TiN provide stable interfaces, thereby reducing defect formation and ensuring lower leakage currents[16]. Table 3 compares the work functions, reactivity, and compatibility of different electrode materials with dielectric materials.

Electrode material	**Work function (eV)**	**Reactivity**	**Compatibility**
TiN	4.7 – 4.9	Low	**High** compatibility, widely used due to good electrical conductivity and stability.

Al	4.06 – 4.26	High	**Low** compatibility, can introduce defects, leading to higher leakage currents.
Pt	5.65	Low	**High** compatibility, forms stable interfaces with dielectrics, reducing defect formation but cost
Au	5.1 - 5.47	Low	**High** compatibility, forms stable interfaces, minimizing leakage currents and defects but cost
Ta	4.12	High	**Low** compatibility, can introduce defects in the dielectric, increasing leakage currents.
Cu	4.65	High	**Low** compatibility, can diffuse into the dielectric, requiring barrier layers to prevent degradation

Table 3. Comparison of different electrode materials and compatibility with dielectric materials

Based on the information above, TiN is chosen for use in this work due to its low reactivity, high compatibility with dielectric materials, and excellent electrical conductivity and stability.

2.3 Si-IF BEOL compatible design

2.3.1 Design overview

There are a total of 10 different sets of MIM capacitors fabricated on a 4-inch wafer to test the process feasibility and electrical DOE (Design of Experiments). As illustrated in Figure 7, the MIM capacitor areas are designed in square shapes with side lengths of 10 μm × 10 μm, 20 μm × 20 μm, 40 μm × 40 μm, 60 μm × 60 μm, 80 μm × 80 μm, 100 μm × 100 μm, 300 μm × 300 μm, 500 μm × 500 μm, 1000 μm × 1000 μm, 2000 μm × 2000 μm.

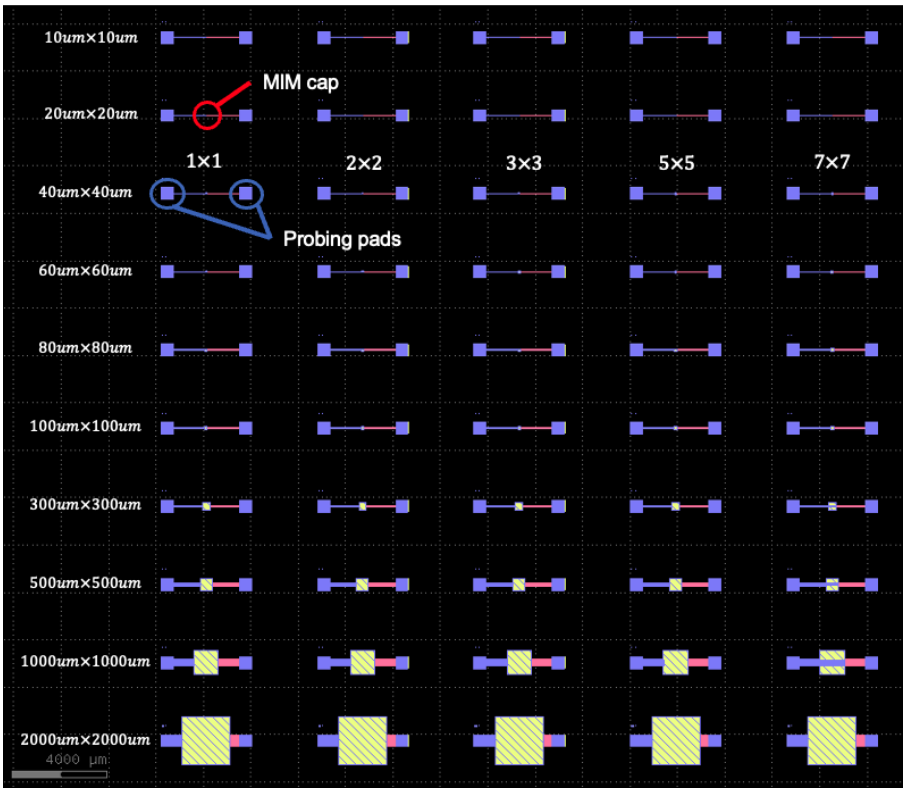


Figure 7. MIM capacitors DOE design

Furthermore, MIM capacitors larger than 40 µm×40 µm are divided into 1 × 1, 2 × 2, 3 × 3, 5 × 5, and 7 × 7 sets of parallel capacitors, with the combined area being equal to the original capacitor area. Figure 8 shows the 5 area combinations of the 300 µm × 300 µm capacitor sitting on the first wiring level and the copper connections between them.

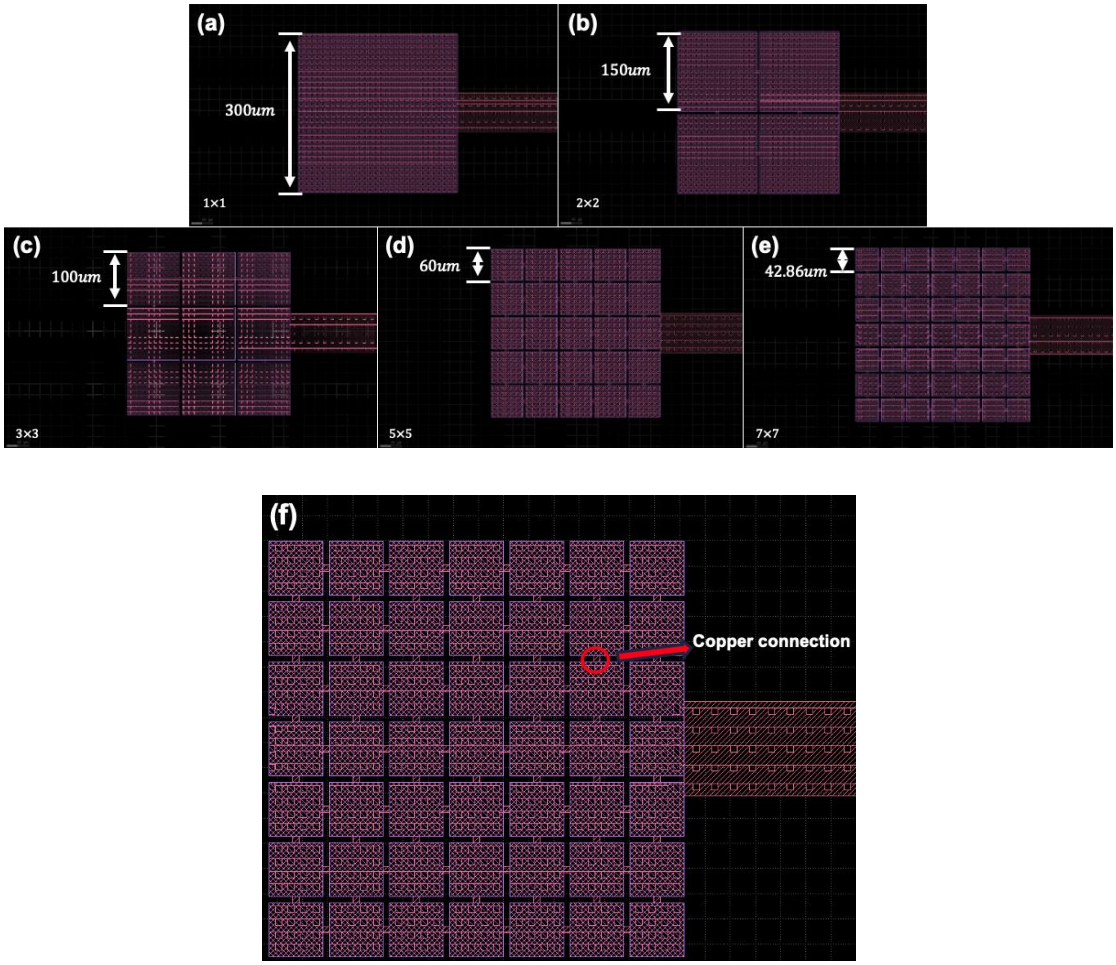


Figure 8. 300 µm × 300 µm capacitor area divided into(a) 1 × 1 (b) 2 × 2 (c) 3 × 3 (d) 5 × 5 (e) 7 × 7 arrays, (f) shows a clearer view of the interconnection on the bottom copper for paralleling capacitors

Vias with a diameter of 5 µm are used to connect the first wiring layer to the second wiring layer and connect the top electrode of the MIM capacitor to the second wiring layer. The whole device and the via are shown in Figure 9.

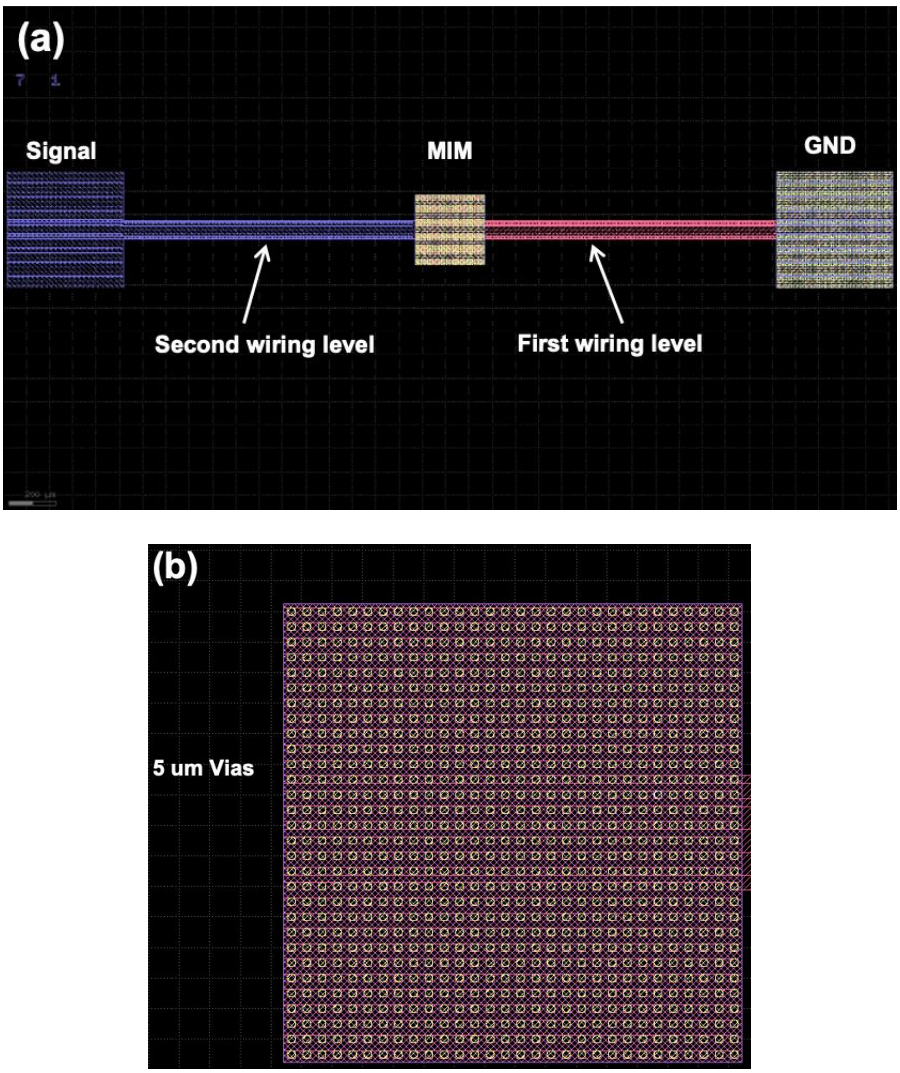


Figure 9. MIM device: (a) Whole device view with 2 wiring levels; (b) Vias connect MIM layer to the second wiring level

2.3.2 Process and reliability consideration in the design

To mitigate the dishing problem caused by CMP, the design across the entire wafer is divided into four quadrants with a symmetrical layout. This symmetrical arrangement helps balance the stress during the CMP process. Additionally, cheesing and metal fill patterns are incorporated into the mask used for BEOL processes to further optimize the CMP process, as

illustrated in Figure 10.

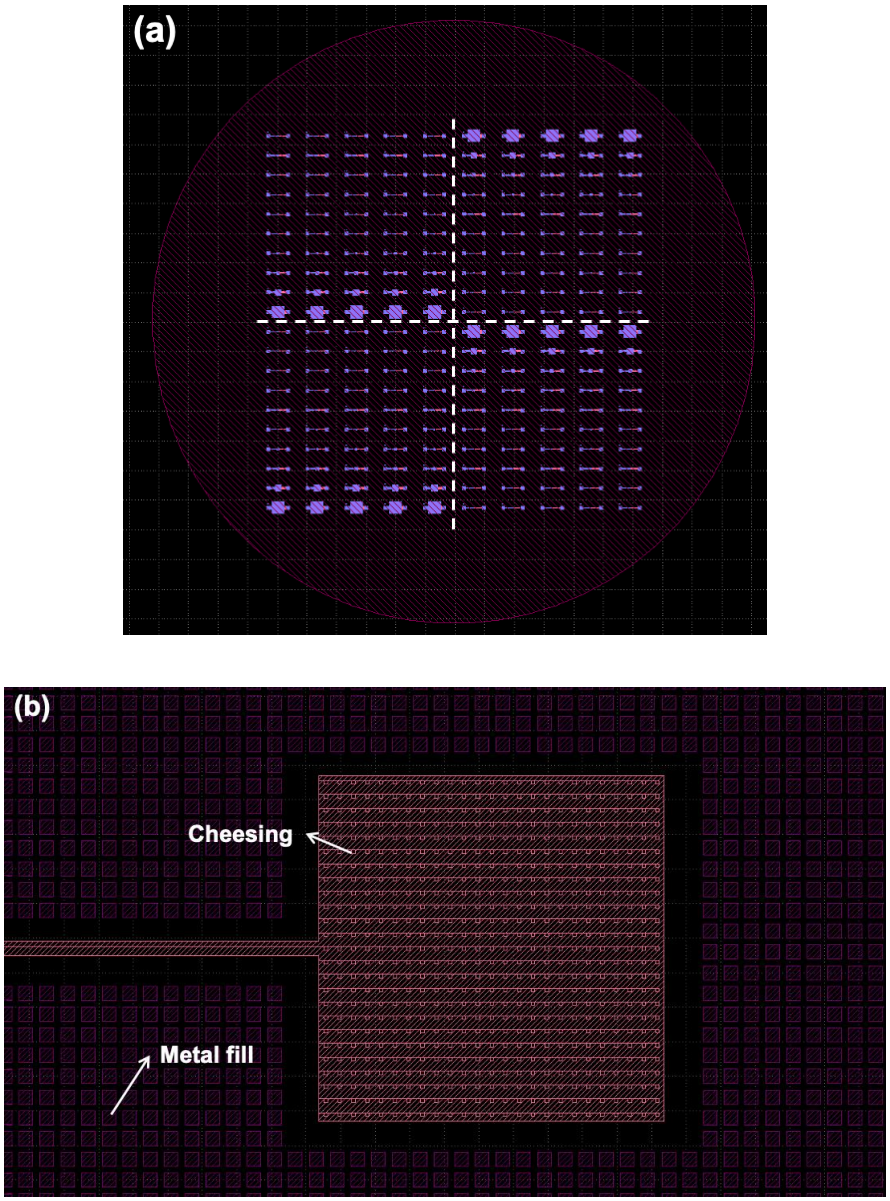


Figure 10. Process consideration in the design to prevent large dishing: (a) Symmetrical arrangement for 4 quadrants across the 4-inch wafer; (b) Cheesing on the copper pad and metal fill surrounding wiring level

As the area of the dielectric layer in MIM capacitors increases, the likelihood of encountering defects and early failures rises significantly. This area dependence is primarily due to the increased probability of defects being present in larger areas, which can act as sites

for leakage current initiation and eventual breakdown. Studies have shown that larger dielectric areas are more prone to reduce the reliability of the capacitors. The Weibull plot of time-to-breakdown distributions normalized to different areas, which is shown in Figure 11 indicates that the probability of early failures increases with larger dielectric areas. To avoid and validate the issue in Si-IF process flow, the devices are designed into single large capacitor and smaller parallel capacitors as mentioned in Chapter 2.3.1.

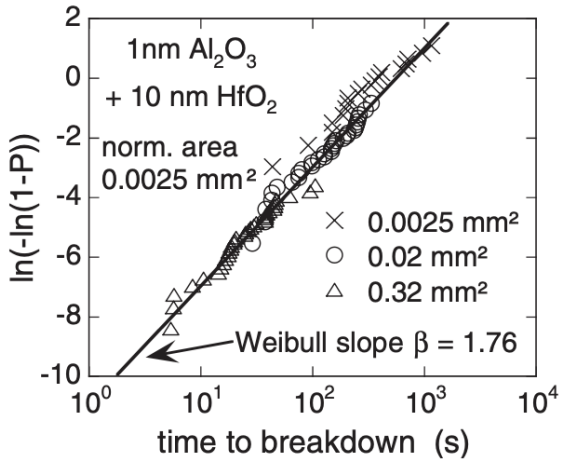


Figure 11. Weibull plot of time-to-breakdown distributions normalized to 0.0025 mm2 for 1 nm Al_2O_3 +10 nm HfO_2 samples of area ranging from 0.0025 to 0.32 mm2 (equivalent oxide field Eeq 1⁄4 13:5 MV/cm). [15]

CHAPTER 3. FABRICATION PROCESS FLOW OF MIM CAP INTEGRATED IN WAFER-SCALE SYSTEM

3.1 Silicon Interconnection Fabric (Si-IF) process overview

The Silicon Interconnection Fabric (Si-IF) processes leverage well-established CMOS Back-End-of-Line (BEOL) fabrication techniques. The wiring level is constructed within silicon dioxide (SiO_2), which is grown through thermal oxidation or deposited via plasma-enhanced chemical vapor deposition (PECVD). The initial copper layer, designated as the M1 layer, can be embedded within SiO_2 formed by thermal oxidation or an additional PECVD oxide layer deposited on a thin thermal oxide substrate. The patterning process involves lithography followed by fluorine-based etching. Subsequently, a titanium/copper (Ti/Cu) seed layer is sputtered, followed by electroplating and chemical mechanical planarization (CMP). These steps establish the first metal layer on the Si-IF, as illustrated in Figure 12.

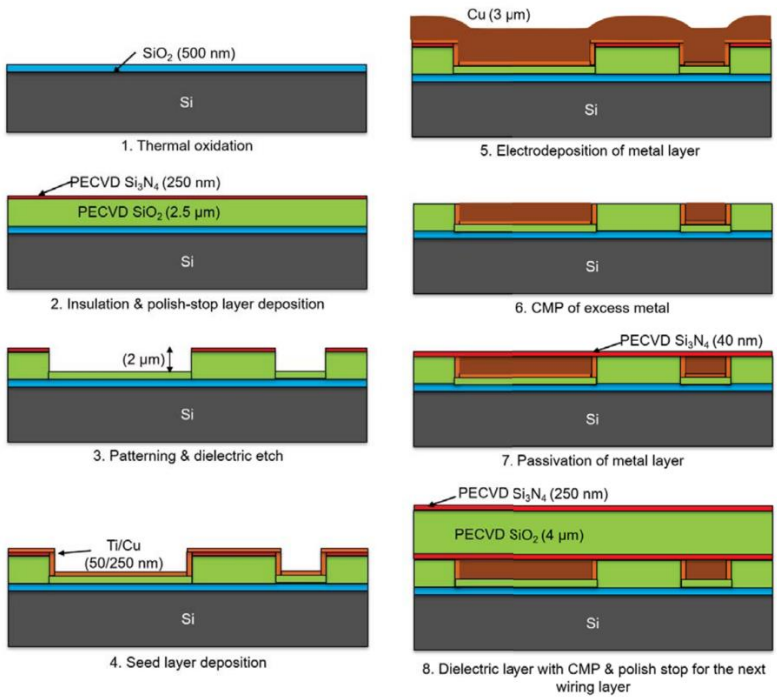


Figure 12. Process flow of Si-IF wiring level [17]

Previous studies have demonstrated the integration of a wiring level, specifically the M1 layer, combined with a pillar layer to facilitate further bonding. A similar process is applied to this layer. The initial photoresist application and patterning define the real pillars connected to the M1 layer, while a second photoresist application defines the pattern of dummy pillars to meet density requirements and ensure uniformity across the wafer during the subsequent CMP process. Fluorine-based reactive-ion etching (RIE) is then used to recess the oxide around the pillars, allowing the copper pillars to protrude for the bonding process. The detailed process is depicted in Figure 13.

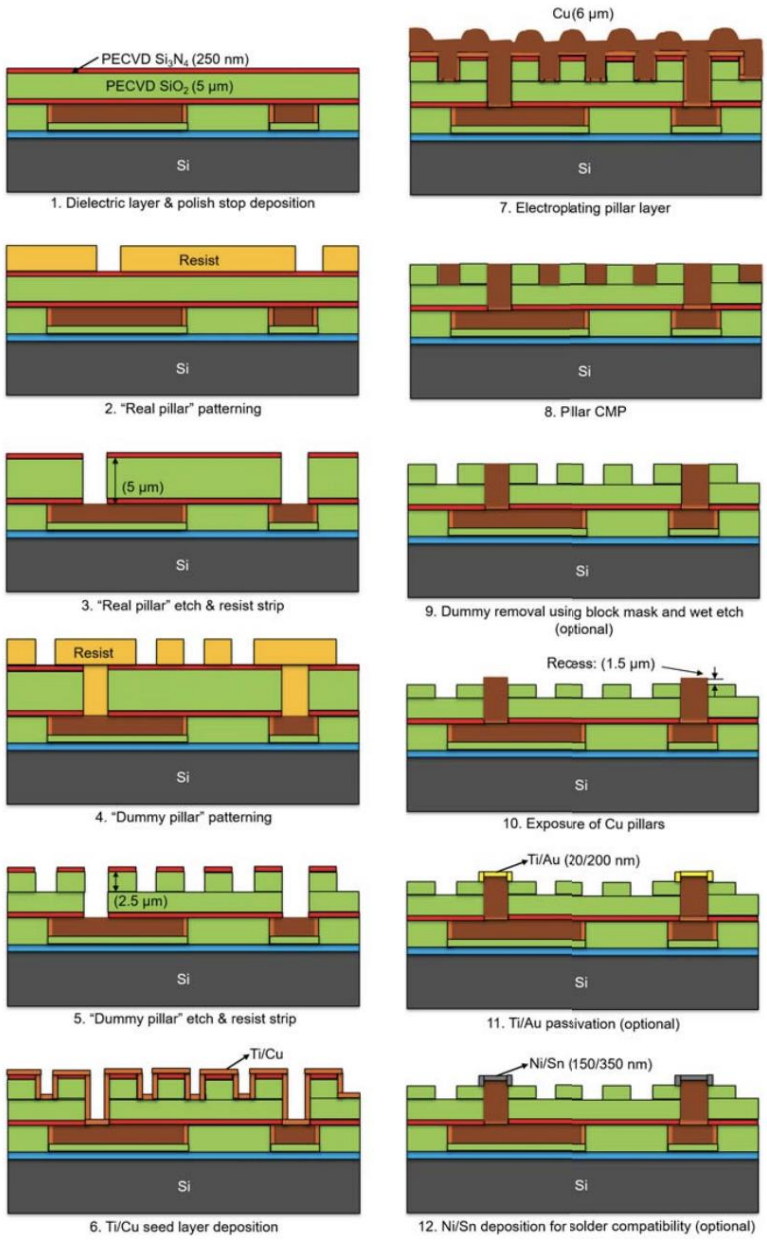


Figure 13. Cu pillars formation process on Si-IF [17]

Currently, there is no existing process flow for integrating passive devices, such as capacitors, within the Si-IF framework. Therefore, a novel process compatible with the original Si-IF process flow needs to be designed and implemented.

3.2 MIM capacitor integration in Si-IF

3.2.1 First wiring level

A single-side polished wafer with 2 μm of thermally grown oxide is utilized in this work. Cleaning steps, detailed in Table 4, are adopted before each deposition process to ensure the removal of any residuals or particles that could affect adhesion or unintentionally alter further patterning. Following the cleaning, a 250 nm low-stress PECVD Si_3N_4 layer is deposited using Plasma Therm Vision deposition tool, serving as a polish stop during the CMP process.

Cleaning Process	Time (s)
Acetone & ultrasonic vibration	60
Isopropyl alcohol wash	15
DI water wash	30

Table 4. Cleaning process before every deposition process

Subsequently, the photoresist is spin-coated onto the wafer, followed by the exposure process. Alignment and lithography are performed using a Karl Suss MA6 Mask Aligner. After developing the photoresist, the etching process is carried out using an STS Advanced Oxide Etcher (AOE), with etch rates for SiO_2 and Si_3N_4 being approximately 64 to 67 Å/s, defining a 1.5 μm deep pattern.

Following the etching, a Ti/Cu seed layer with a thickness of 20/200 nm is sputtered onto the wafer. The cavity is then overplated using electroplating with 3 μm of copper. The electroplating process is conducted in two stages of equal duration, with a 180-degree rotation

between the stages to achieve higher uniformity across the entire wafer. In each stage, 1.5 μm of copper is plated for 45 minutes, measured by a Keyence Profile Measurer, which is shown in Figure 14 and the result after plating is shown in Figure 15.

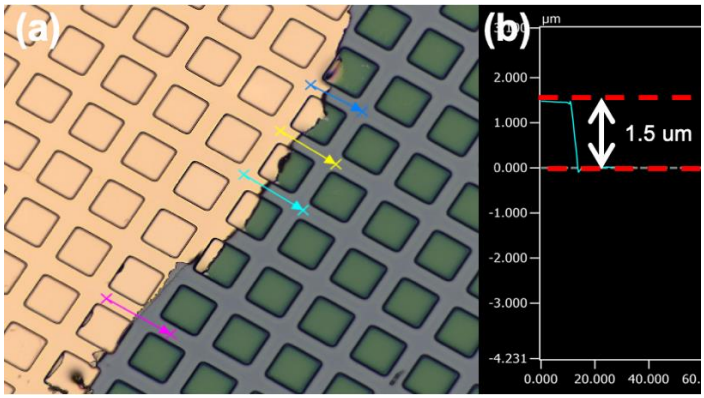


Figure 14. (a) The left side is electroplated for 45 minutes in one stage, and the right side is covered by Kapton tape so the area is not plated; (b) 1.5 μm plated Cu in one stage measured by the height difference between these two areas by Keyence profiler

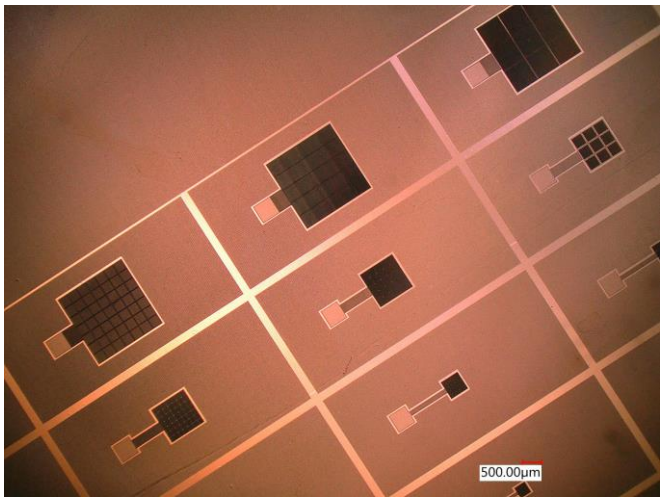


Figure 15. 3 μm of Cu electroplated for first wiring level

Finally, a CMP process is applied using a G&P Technology Poli 400L CMP machine to planarize the first layer of copper. The process flow for building the first wiring layer is

illustrated in Figure 16.

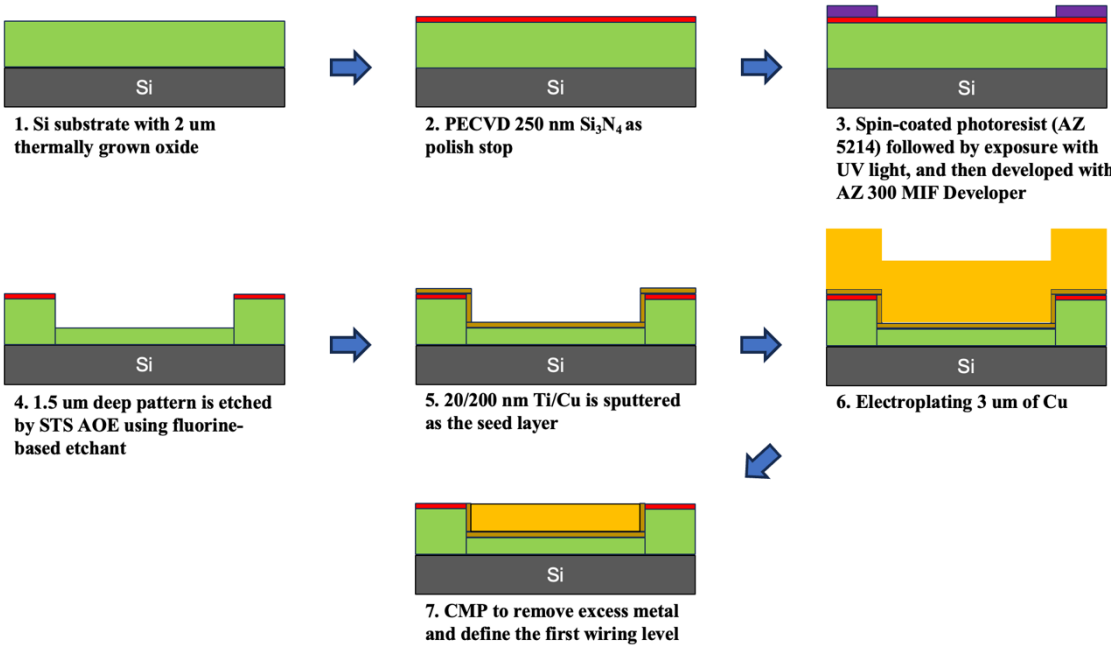


Figure 16. Process flow of the first wiring level

A clean pattern and the initial copper wiring level, surrounded by oxide, can be achieved after the CMP process. Figure 17 shows the 1000 µm × 1000 µm capacitor array, transitioning from a single capacitor array to being divided into 5 × 5 and 7 × 7 parallel capacitor arrays after CMP. The metal fill around the first wiring level helps balance the stress and maintain uniformity during the CMP process. The probing pad that will be connected to the second wiring level is also shown in Figure 17(a).

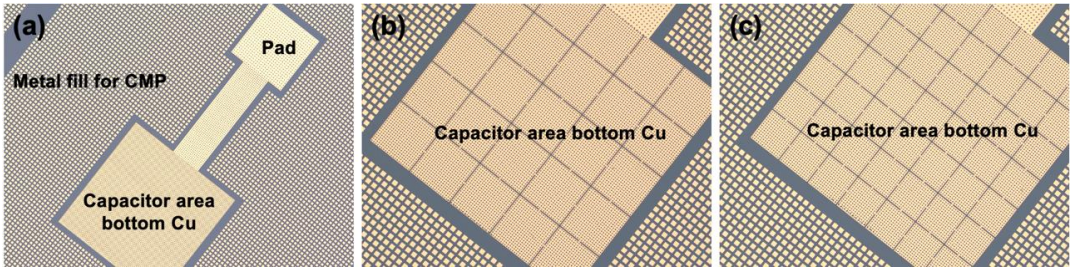


Figure 17. First wiring level with 1000 μm × 1000 μm capacitor area : (a) Single array capacitor (b) 5 × 5 parallel capacitor arrays (c) 7 × 7 parallel capacitor arrays

3.2.2 MIM cap fabrication

After the first wiring level is fabricated, the MIM cap will be constructed on the bottom copper electrode. As mentioned in Chapter 2, two different MIM cap structures with distinct process flows are fabricated, and each process is discussed separately in this chapter. However, the deposition rate of the electrode material, TiN, had not been characterized previously, necessitating a preliminary test.

3.2.2.1 Characterization of electrode deposition rate

Initially, the bottom electrode material, TiN, is sputtered using the ULVAC JSP 8000 Metal Deposition Sputter, as shown in Figure 18, with a 300W RF power setting.

Figure 18. ULVAC JSP 8000 Metal Deposition Sputter

The TiN sputtering rate is characterized by preparing a blanket substrate with Kapton tape applied to it, followed by sputtering TiN for 3000 seconds. The tape is then peeled off to perform a lift-off-like process, as shown in Figure 19. The sputter rate of 0.04 nm/s is determined and averaged from 13 points across the wafer using Veeco Dektak 8 Profilometers shown in Figure 20.

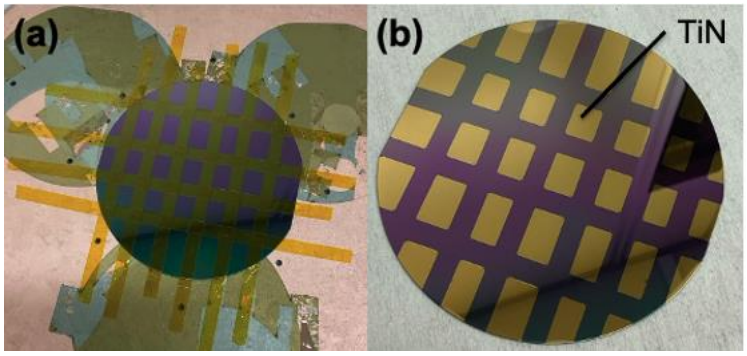
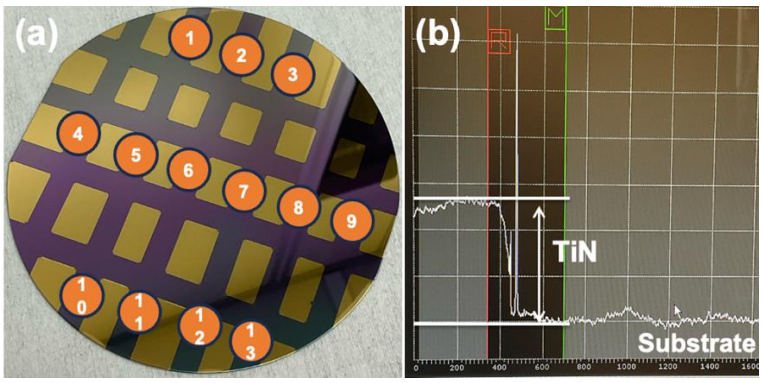


Figure 19. TiN sputtered dummy sample for characterization: (a) Taped sample before sputtering; (b) Lift-off process revealing the step height of TiN and the substrate



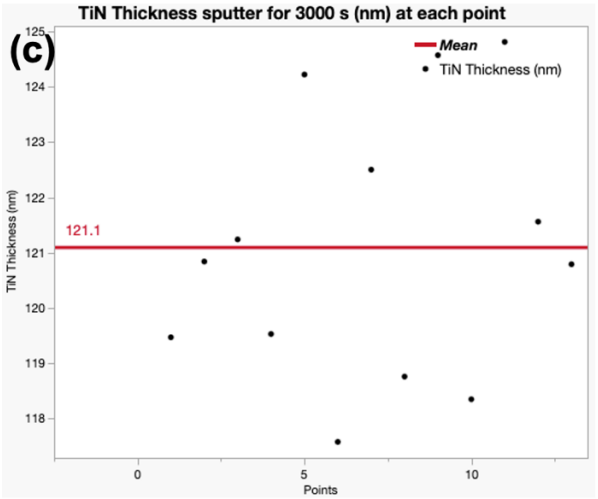


Figure 20. Sputter rate characterization: (a) Scanned point locations; (b) Step height measurement using Veeco Dektak 8 Profilometers; (c) The average thickness of TiN after 3000 s of sputtering is 121.1 nm, leading to the conclusion that the sputtering rate is approximately 0.04 nm/s.

3.2.2.2 Parallel plate capacitor

Once the electrode has been sputtered, the MIM capacitor can proceed with further manufacturing. In this phase, a parallel plate capacitor is constructed on the first wiring level. The detailed process flow is outlined in the following steps and depicted in Figure 22, with the top view after patterning shown in Figure 23.

Step 1: Acetic acid combined with ultrasonic vibration to remove copper oxide that affects electrical performance

Step 2: A 150 nm thick TiN is sputtered to act as the bottom electrode of the MIM capacitor

Step 3: The dielectric layer is deposited by Ultratech Fiji (Figure 21) by controlling the cycle and precursor to define the layer thickness and structure

Figure 21. Ultratech Fiji Plasma Enhanced ALD

Step 4: Another 150 nm thick TiN is sputtered to be the top electrode of the MIM capacitor

Step 5: Spin coat photoresist and develop the pattern

Step 6: MIM Patterning

Step 7: Strip the photoresist

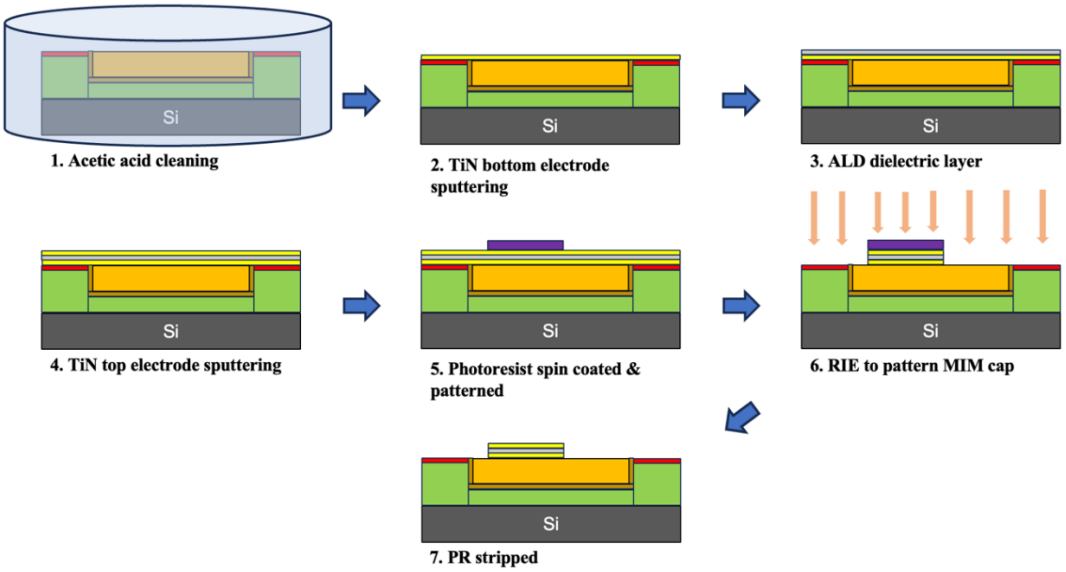


Figure 22. Process flow of parallel capacitor fabrication on first wiring level

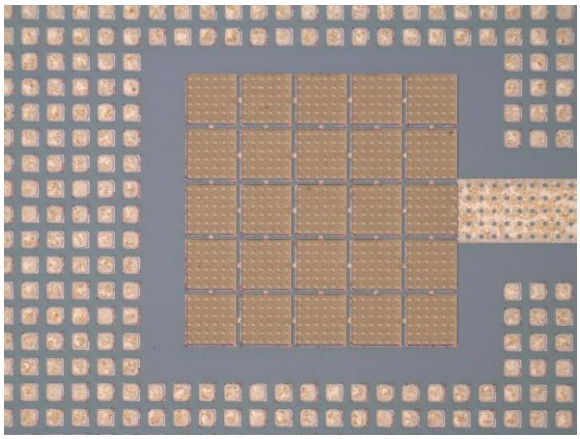


Figure 23. Planar MIM capacitor with 5 by 5 array after patterning

3.2.2.3 Parallel plate capacitor with oxide passivation

An alternative structure that can be integrated into the Si-IF is a parallel plate capacitor with an oxide passivation layer, offering a broader process window for MIM patterning. This process will be further discussed in Chapter 4. The process flow is outlined and illustrated in Figure 24, with the top view after patterning presented in Figure 25.

Step 1: Acetic acid combined with ultrasonic vibration to remove copper oxide

Step 2: A 20 nm of Al_2O_3 is deposited by ALD on the first wiring level under 200 ℃ to prevent copper from oxidation during the following step

Step 3: PECVD 200 nm of SiO_2 under 300 ℃ environment

Step 4: Spin coat photoresist and develop the pattern

Step 5: Etch the cavity with fluorine-based RIE that connected to the bottom copper wiring level

Step 6: Strip the photoresist

Step 7: Sputter 50 nm of TiN as the bottom electrode

Step 8: The dielectric layer is deposited by ALD under different cycles and precursors

Step 9: A 150 nm of TiN is sputtered as the top electrode

Step 10: Spin coat photoresist and pattern the MIM area whose side length is 2 μm more than the cavity created by Step 5

Step 11: MIM patterning

Step 12: Strip the photoresist

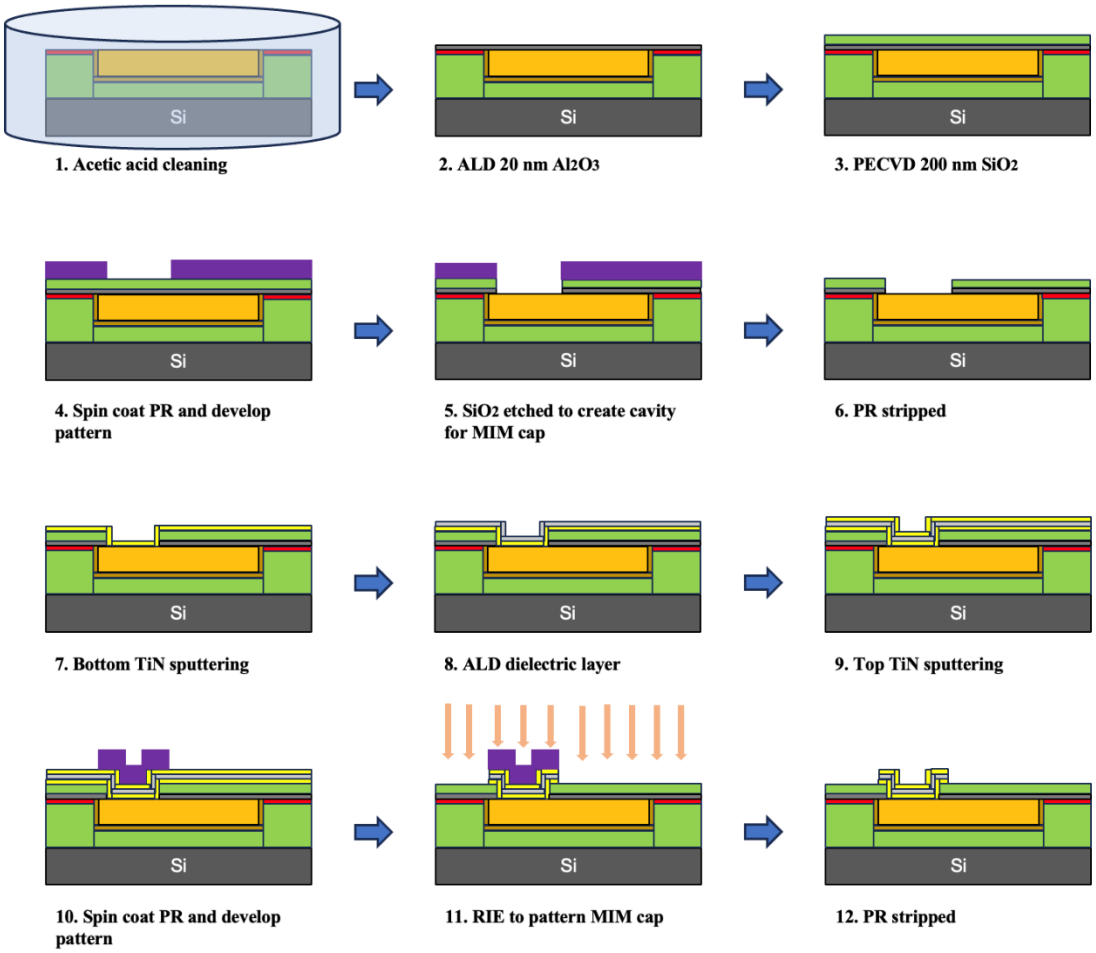


Figure 24. Process flow of parallel plate capacitor with oxide passivation integrated in Si-IF

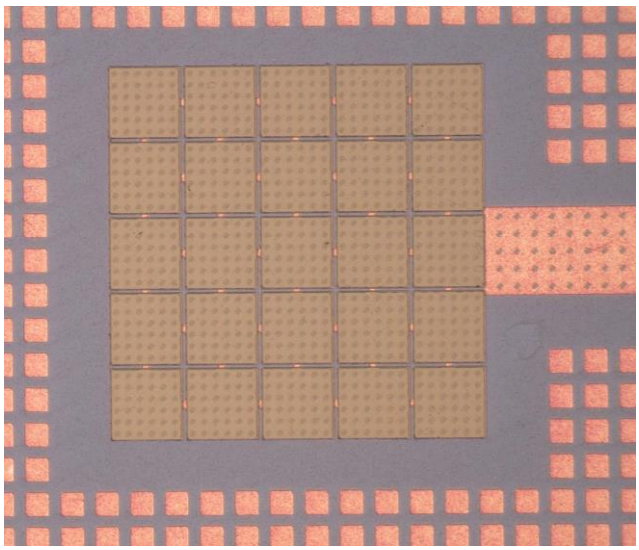


Figure 25. MIM capacitor with oxide passivation with 5 by 5 array after patterning

3.2.3 Via to top electrode and bottom electrode

Following the fabrication of the MIM cap, the via layer is fabricated to connect the first wiring level, the MIM cap, and the second wiring level. The process flow using the second structure mentioned in Chapter 3.2.2 is specified in Figure 26. These are typical Si-IF BEOL process flows, with the only difference being the MIM cap layer causing topography on the first wiring layer, which is compensated by further deposition and CMP.

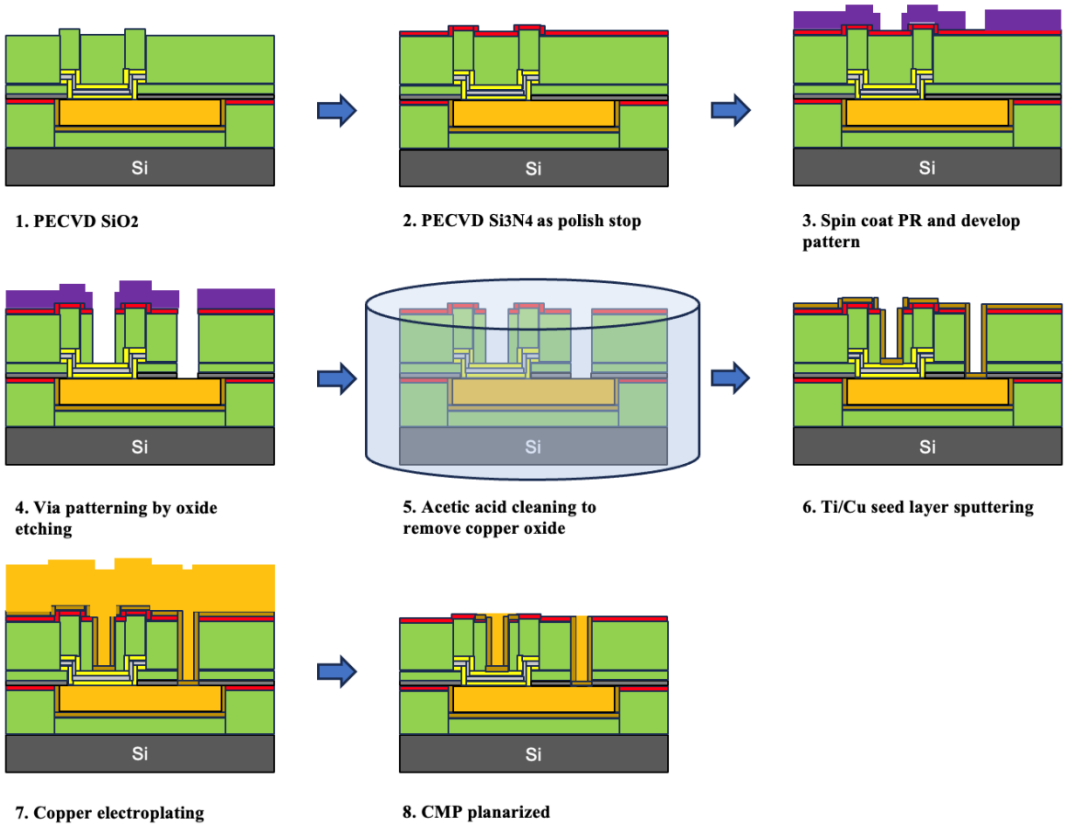


Figure 26. Process flow of via layer to connect top electrode, first wiring layer, and second wiring layer

3.2.4 Second wiring level

The second wiring level is followed via layer fabrication. This layer could be used for fan-

out and building copper pillars on it to do flip-chip fine-pitch bonding. The process flow and the final structure are shown in Figure 27.

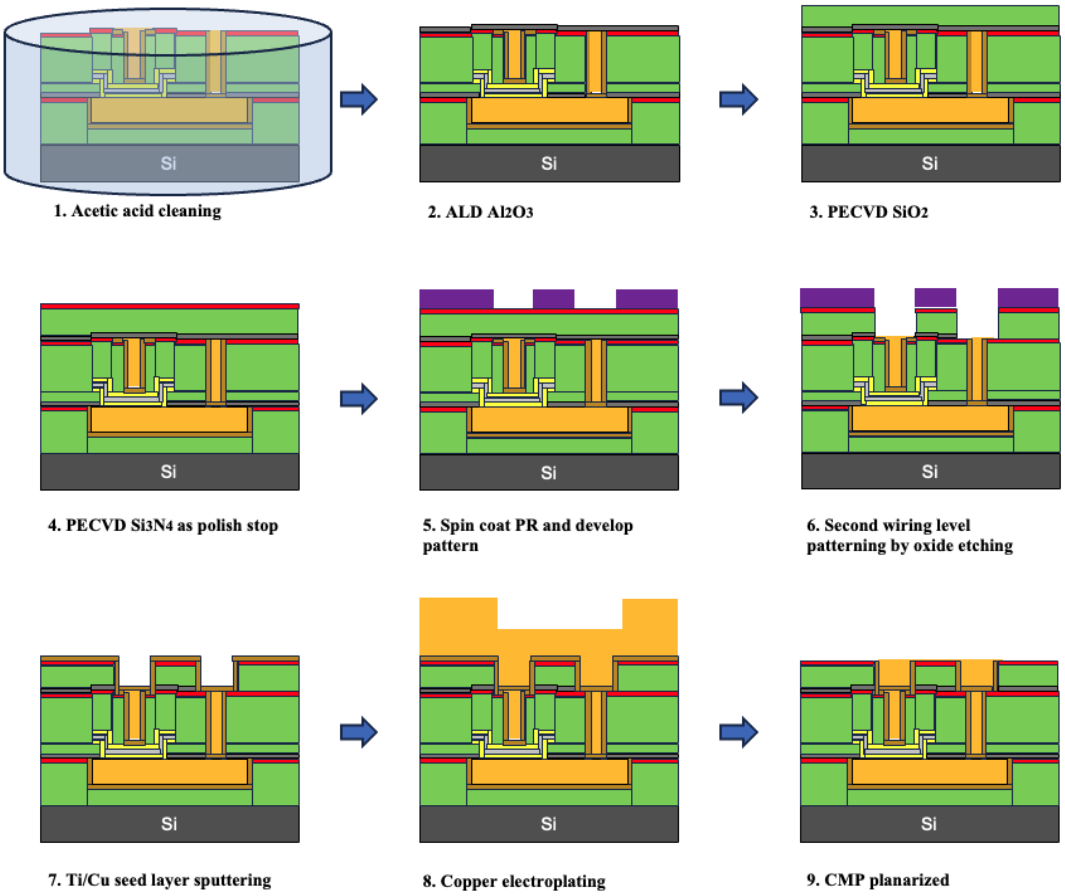


Figure 27. Process flow of building the second wiring layer with MIM cap integrated in Si-IF

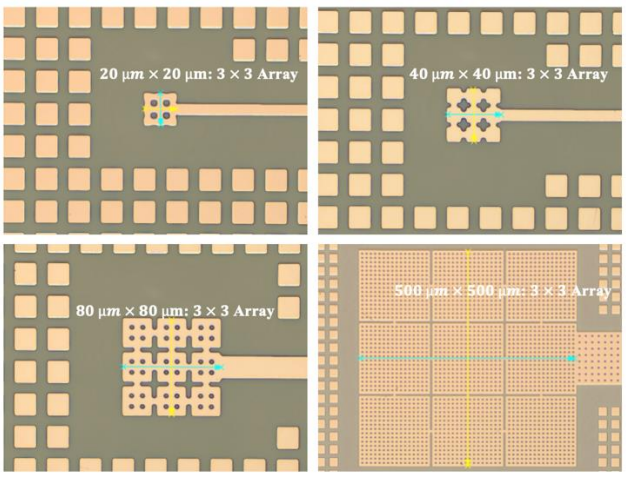
CHAPTER 4 PROCESS DEVELOPMENT AND ELECTRICAL RESULTS

4.1 MIM integration process development and characterization

4.1.1 First wiring level characterization

Various characterizations were performed on the first wiring level to assess the dishing effects influenced by the design discussed in Chapter 2. Figure 28 illustrates the comparison of dishing for different pad sizes—20 µm × 20 µm, 40 µm × 40 µm, 80 µm × 80 µm, and 500 µm × 500 µm—with a 3 × 3 array, as measured by the Keyence Profile Measurer. The measurement starts at the edge of the pad and extends to the opposite edge, with dishing data being derived by comparing the height differences between the edge and the center of the pad. The measurement lines also traverse the connection between each parallel bottom pad. The results indicate that larger pads exhibit greater height differences from the edge to the center.

(a)



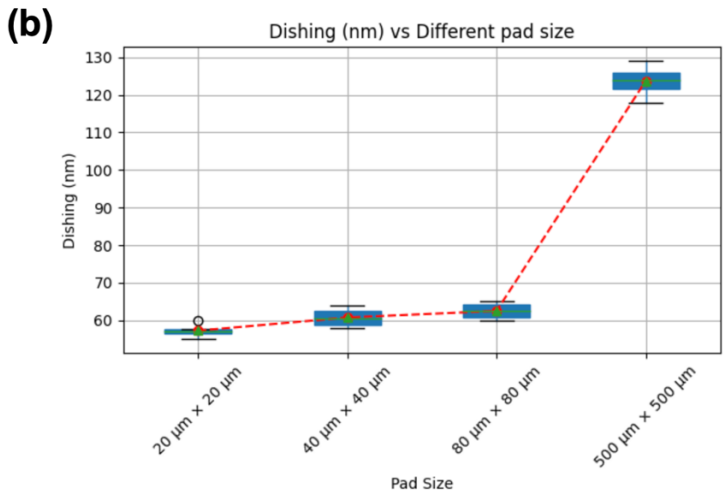
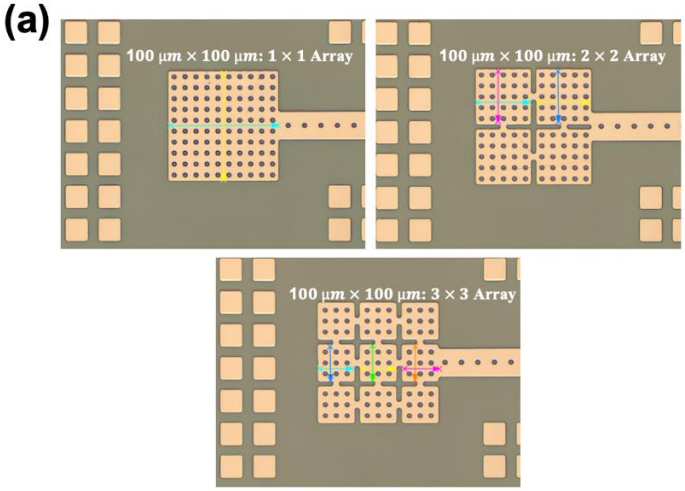


Figure 28. Dishing comparison on different pad sizes: (a) Measurement starts from the edge to another edge of the pad; (b) Dishing vs different pad sizes

To assess whether the parallel design mitigates dishing at the locations where the MIM capacitors are situated, dishing was also measured and is shown in Figure 29(a). The measurement extends from one edge of the unit pad to the opposite edge, with dishing determined by comparing the differences between the edge and the center of each unit pad. From Figure 29(b), a clear relationship between dishing and pad arrays is evident: dividing a large pad into more unit pads significantly reduces the dishing effect.



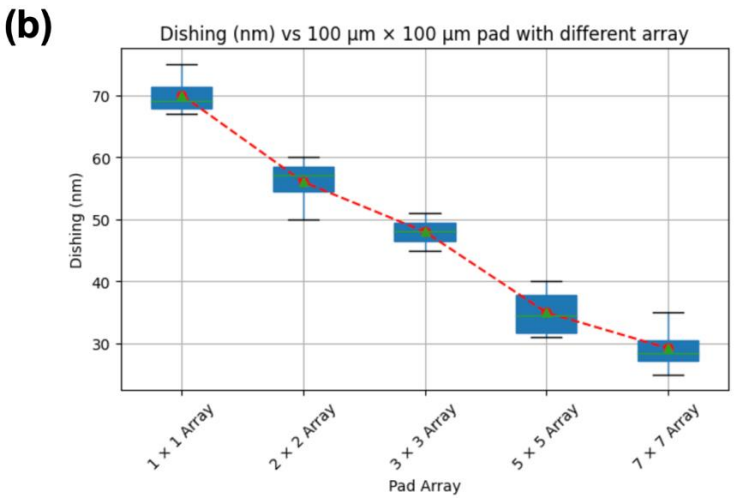
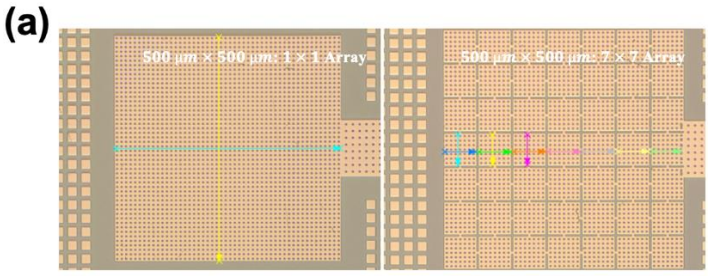


Figure 29. Dishing comparison on 100 µm × 100 µm pad arrays: (a) Measurement starts from the edge of each unit cells to their center; (b) Dishing vs 100 µm×100 µm pad with different arrays

A more pronounced result is observed in Figure 30 by comparing a 500 µm × 500 µm pad with a 1 × 1 array to one with a 7 × 7 array. The average dishing decreases from approximately 124 nm to 68 nm when the single large pad is divided into multiple smaller unit pads.



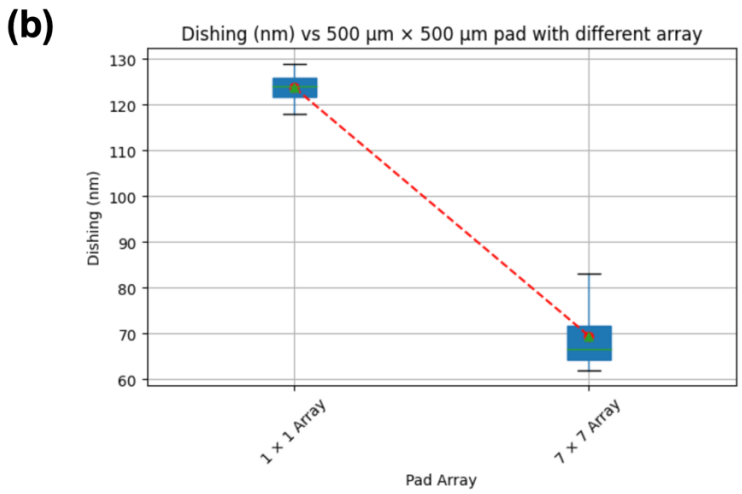


Figure 30. Dishing comparison on 500 µm × 500 µm pad arrays: (a) Measurement for unit pads; (b) Dishing comparison on 500 µm × 500 µm pad with 1 × 1 array and 7 × 7 array

4.1.2 MIM capacitor process development and structure optimization

4.1.2.1 MIM capacitor layer etching rate characterization

When patterning the MIM layer using RIE, there are two viable options for the etchants: fluorine-based[18] and chlorine-based[19]. Both are effective for etching TiN and the dielectric layer simultaneously. However, given the presence of SiO_2 around the first wiring level, the etching process for the MIM layer requires higher selectivity for SiO_2 to prevent uncontrolled topography changes and avoid over-etching the oxide. To determine the best etching process, a comparative test was conducted using a fluorine-based etchant with the STS AOE and a chlorine-based etchant with the ULVAC NE-550. The etch rates were measured using a Nanospec film thickness measurer, as illustrated in Figure 31.

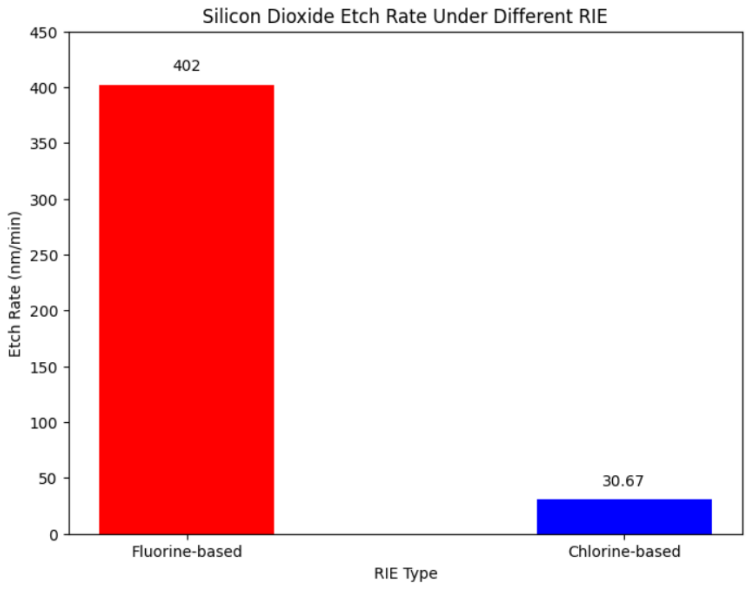


Figure 31. Silicon dioxide etch rate comparison under different RIE

The results indicated that the fluorine-based RIE etch rate on SiO_2 was excessively high, leading to difficulty in controlling the patterning process. Consequently, a chlorine-based etching process was selected for patterning the MIM layer using BCl_3/Cl_2 inductive coupled plasma[20]. To further evaluate the etching rate and selectivity of TiN and SiO_2 under chlorine-based RIE, a detailed characterization was performed, as shown in Figure 32(a). The measurement results are presented in Figure 32(b). The sample preparation involved applying Kapton tape to the wafer, sputtering TiN, and then performing a lift-off process by peeling the tape to create a step height corresponding to the thickness of the TiN layer.

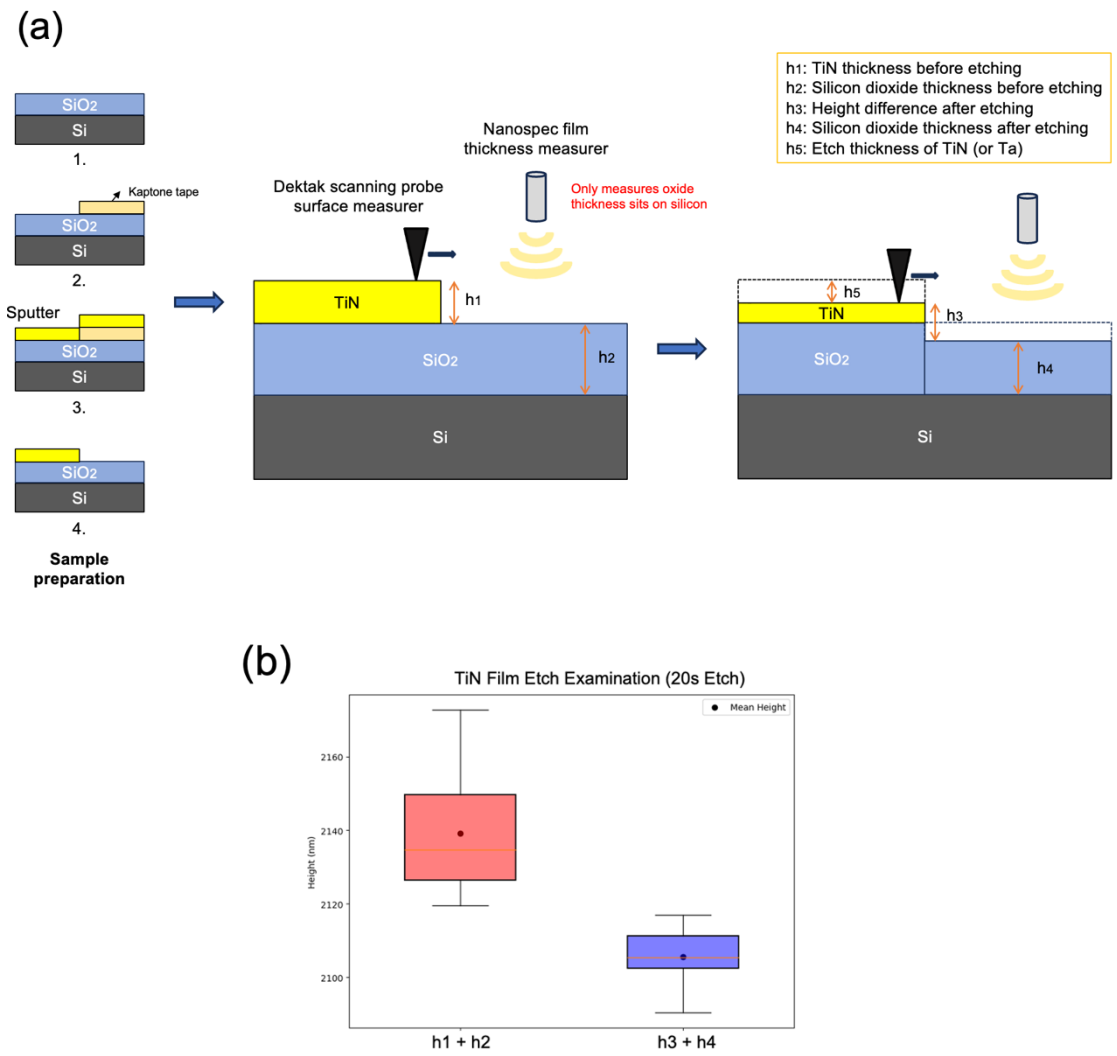


Figure 32. Etch rate and selectivity test on TiN and SiO_2: (a) Sample preparation and testing procedure; (b) Measurement results

Combining the Dektak scanning probe surface measurer and the Nanospec film thickness measurer, the etch rate and selectivity between TiN and SiO_2 under chlorine-based RIE were calculated using the equation (3), with the results displayed in Figure 33.

$$\textit{Etch Rate} = \textit{Etch thickness (h5)} / \textit{Etch Time} = [(h1 + h2) - (h3 + h4)] / \textit{Etch time} \quad (3)$$

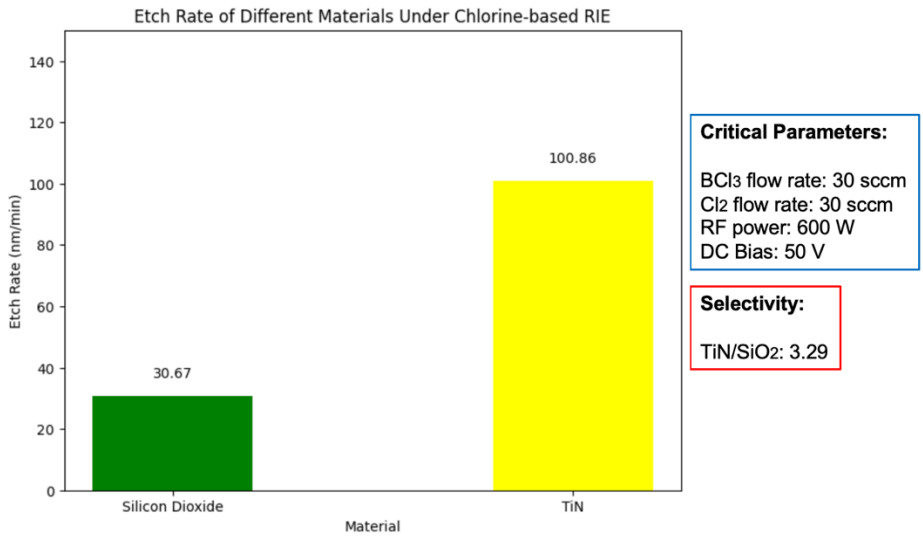


Figure 33. Etch rate and selectivity of silicon dioxide and TiN under chlorine-based RIE

4.1.2.2 Structure re-design and process development

While the patterning of some parallel MIM capacitors was successful, contamination from the chlorine etch was observed on the first wiring level in most samples, as shown in Figure 34. This contamination indicates that the initial process and structure are not robust or suitable for integration into Si-IF.

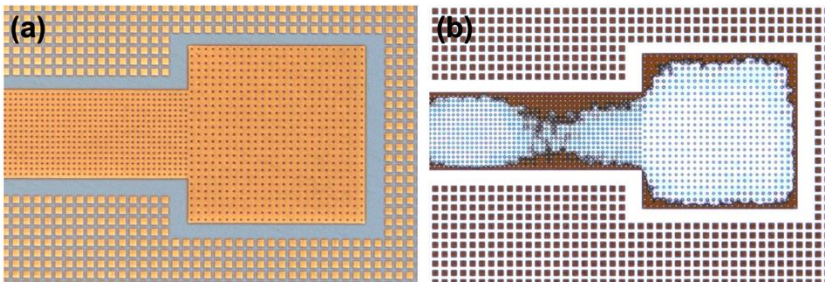


Figure 34. First wiring level after chlorine etch: (a) without contamination; (b) with contamination

To address this issue, a MIM capacitor with an oxide passivation structure was designed and tested for process feasibility by building a test structure. Figure 35(a) outlines the process

flow for preparing the test sample. Figure 35(b) demonstrates that the oxide layer effectively passivates the copper during chlorine etching, while Figure 35(c) shows that the copper layer maintains low resistance after the process. Furthermore, the sample was successfully electrically tested by probing the top electrode of MIM capacitors and the bottom copper electrode, indicating that this structure is feasible for integration into Si-IF.

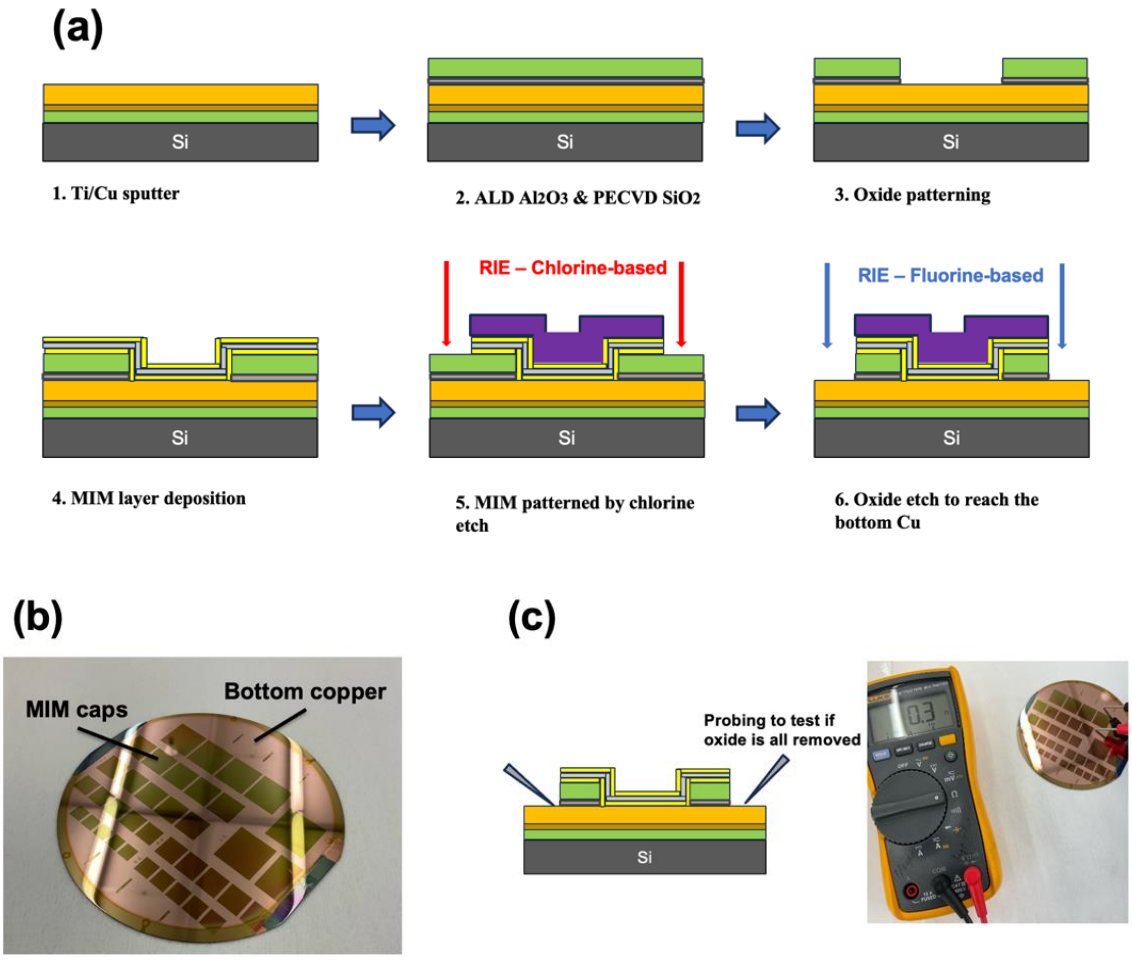


Figure 35. Sample to test the feasibility of integrating the re-designed structure into Si-IF: (a) Process for creating the sample; (b) Sample after patterning; (c) Resistance test on bottom Cu to assess the impact of etching

4.2 Electrical characterization on MIM capacitor

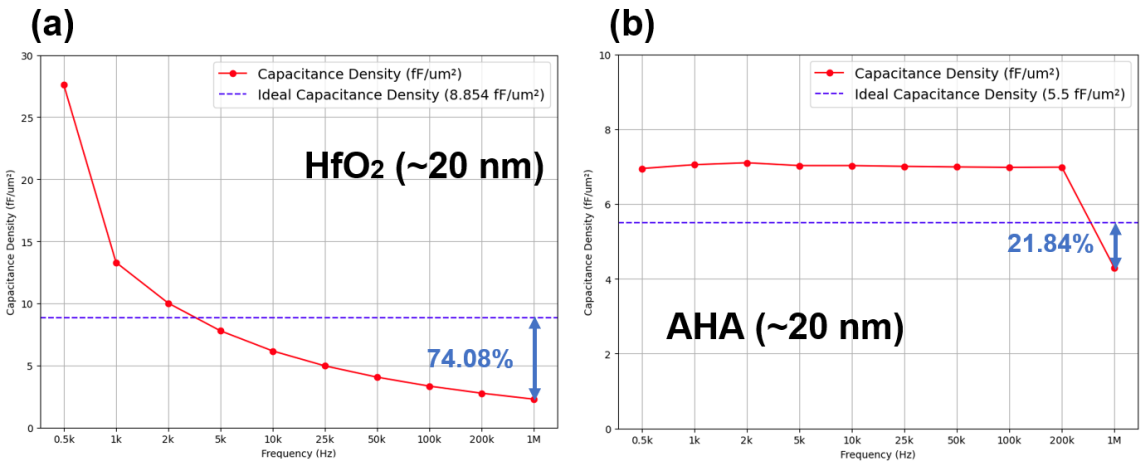
The electrical characterization was performed on the test structure to obtain preliminary results for the MIM capacitor and to evaluate the feasibility of integrating the proposed structure. To determine the optimal operating frequency range for the device, it is crucial to understand the relationship between capacitance and frequency. The ideal equivalent capacitance can be calculated using equation (4), treating the stacked dielectric layers as a series of single-layer capacitors:

$$\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \cdots + \frac{1}{C_n} \quad (4)$$

The capacitance density of various dielectric structures, including HfO_2 (20 nm), AHA (5 nm-10 nm-5 nm), and AHAHA (5 nm-10 nm-5 nm-10 nm-5 nm), was measured and compared to the ideal equivalent capacitance density. The results are shown in Figure 36.

From Figure 36(a), a significant deviation (~74.08%) between the measured and ideal capacitance densities for HfO_2 is observed. This large deviation is likely due to interfacial defects between the dielectric and metal, which act as charge-trapping sites, resulting in an apparent increase in capacitance at low frequencies. The polarization mechanism at low frequencies is dominated by space charge polarization. As illustrated in Figure 37, interfacial traps and defects accumulate charges at the interface, leading to an increase in the real permittivity and, consequently, a higher dielectric constant. Figure 36(b) shows that, at 1 MHz, the capacitance density of the AHA structure is more stable compared to the HfO_2-only

structure, with a smaller deviation from the ideal capacitance density (~21.84%). This demonstrates that the addition of Al_2O_3 effectively reduces the impact of defects and charge traps at the dielectric/electrode interface. Further validation is provided by Figure 36(c), which shows the capacitance density for the AHAHA structure. By adding an additional Al_2O_3 layer, the deviation from the ideal capacitance density is reduced to 15.96%, and the frequency stability is further improved. This improvement is directly reflected in the dielectric constant throughout the frequency range. The equivalent dielectric constant for the three structures was reverse-calculated using Equation (1) with the measured thickness and capacitance density. Notably, only the AHAHA structure maintained a dielectric constant within the ideal range for HfO_2 and Al_2O_3, as depicted in Figure 38.



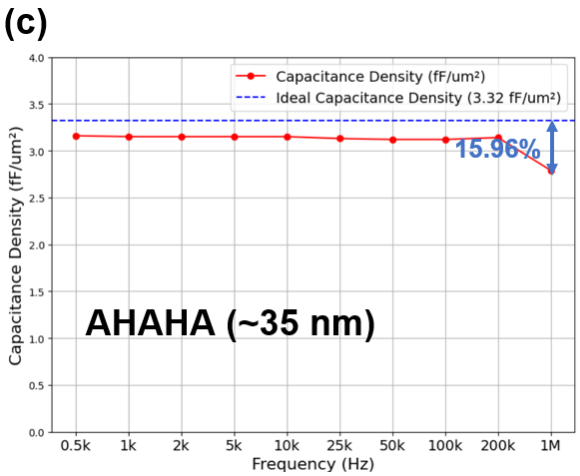


Figure 36. Capacitance density of MIM caps with different structure vs frequency: (a) HfO_2; (b) AHA; (c) AHAHA

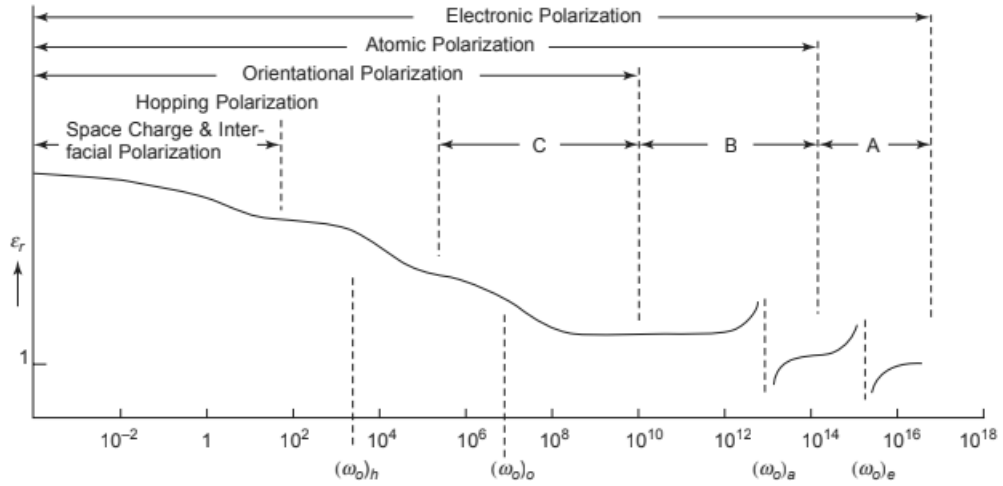


Figure 37. Relative permittivity as a function of frequency [21]

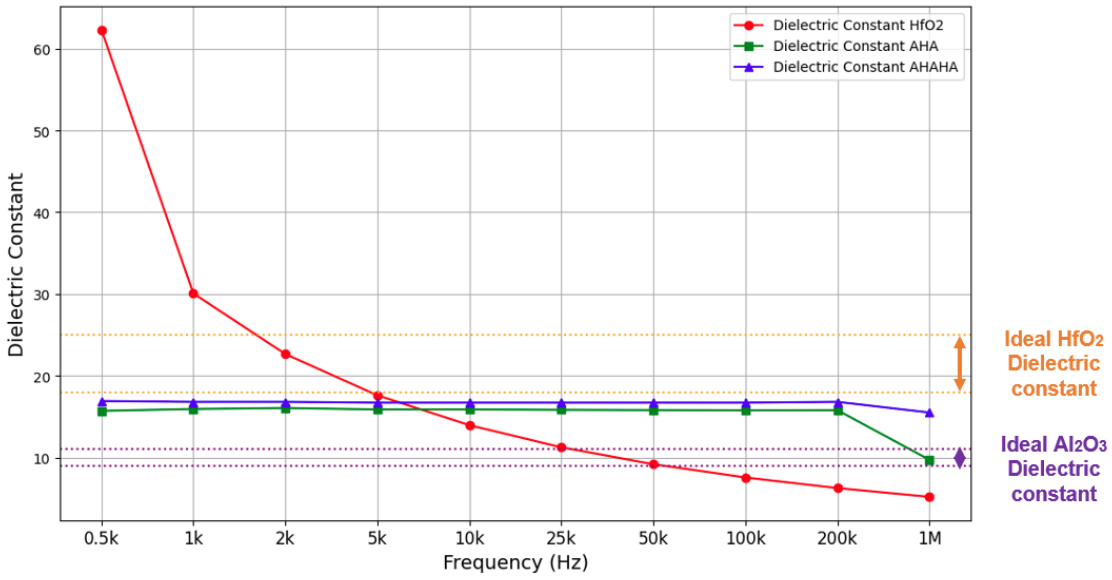


Figure 38. Dielectric constant of MIM caps with different structures vs frequency

Additionally, an area scalability test was conducted on the AHAHA MIM capacitor, with measurements taken at 200 kHz. The results indicate that, as the area increases, the capacitance density decreases. This trend aligns with predictions that larger areas are more prone to containing defects, which, in turn, increase parasitic capacitance and degrade the overall capacitance as shown in Figure 39.

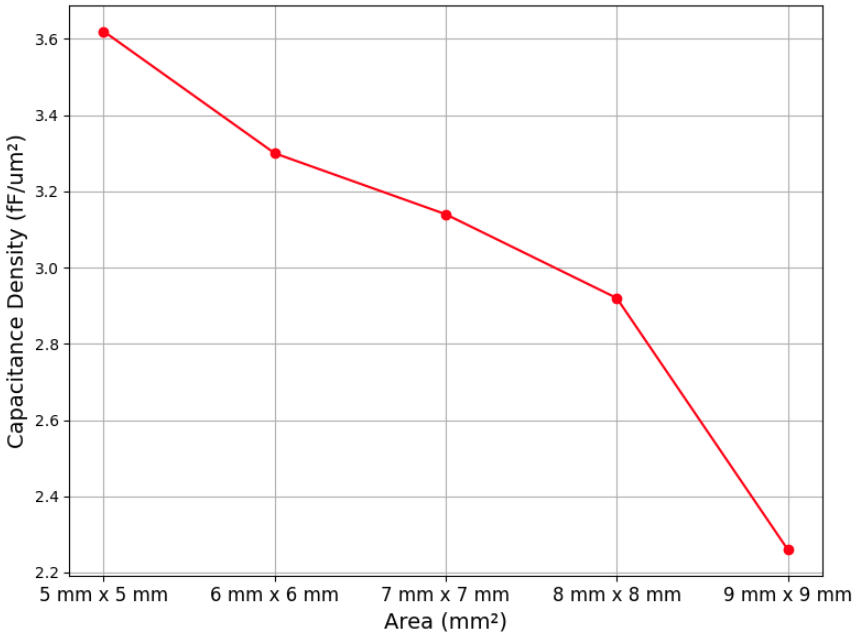


Figure 39. Capacitance density of AHAHA MIM cap with different areas measured under 200 kHz

CHAPTER 5 CONCLUSIONS AND FUTURE WORK

In this thesis, the successful development of a MIM capacitor structure suitable for integration into the Si-IF platform has been demonstrated through meticulous design, careful material selection, and process optimization. By overcoming critical challenges such as dishing, material compatibility, and process refinement, this work contributes valuable insights into the feasibility of incorporating MIM capacitors in wafer-scale systems. The electrical characterization of the proposed structures, which utilized different dielectric configurations—HfO_2 (20 nm), AHA (5 nm-10 nm-5 nm), and AHAHA (5 nm-10 nm-5 nm-10 nm-5 nm)—resulted in capacitance densities of 2.29 fF/μm², 4.29 fF/μm², and 2.79 fF/μm², respectively. Among these, the AHAHA structure has emerged as the most stable and feasible option for Si-IF integration. Furthermore, additional testing at 200 kHz confirmed that as the area of the AHAHA structure increases, the capacitance density decreases, underscoring the need for careful consideration of area scaling in future implementations.

The most significant challenge in integrating HfO_2 as a dielectric layer is mitigating defects and interfacial charge traps, which hinder the full realization of its high dielectric constant. To enhance capacitance density, it is essential to explore rapid thermal processes (RTP) or other annealing techniques to crystallize the amorphous dielectric and reduce intrinsic defects. However, these thermal treatments must remain compatible with BEOL processes to

avoid issues such as thermal stress or delamination. Another approach to increasing capacitance density is to investigate structures that allow for greater surface area while maintaining the same base area, such as introducing shallow trenches in the oxide to expand the overall surface area of the MIM capacitor.

Future research will delve deeper into the dielectric mechanisms and explore new processes and structures to further improve MIM capacitors for integration into the Si-IF platform. These developments will be crucial for addressing the challenges faced by modern AI, HPC, and power delivery systems.

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