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Authors

Abramson, Rose A
Krishnan, Sahana
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et al.

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An Active Split-Phase Control Technique for Hybrid Switched-Capacitor Converters Using Capacitor Voltage Discontinuity Detection

R. A. Abramson
S. Krishnan
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R. C. N. Pilawa-Podgurski

An Active Split-Phase Control Technique for Hybrid Switched-Capacitor Converters Using Capacitor Voltage Discontinuity Detection

Rose A. Abramson, Sahana Krishnan, Margaret E. Blackwell, and Robert C. N. Pilawa-Podgurski
Department of Electrical Engineering and Computer Sciences, University of California, Berkeley
Email: {rose_abramson, sahana_krishnan, blackwell, pilawa}@berkeley.edu

***Abstract*—Hybrid switched-capacitor (SC) converters have gained popularity due to their efficient switch utilization and use of energy-dense capacitors, which allows them to achieve high efficiency and power density even at large conversion ratios. The Dickson converter is one such popular hybrid SC converter, as it can achieve the theoretical minimum switch stress rating for a given operating condition. However, unlike other hybrid SC topologies that can automatically achieve full soft-charging through the addition of one or more augmenting inductors, certain Dickson variants also require the use of special switching schemes to fully soft-charge all flying capacitors. This technique, denoted as split-phase switching, inserts extra sub-phases into the control scheme so that flying capacitors are disconnected or connected at staggered times. Traditionally, split-phase timing has been calculated analytically, sometimes using imprecise models. This paper instead proposes an active control technique for detecting hard-charging events on the flying capacitors, such that the split-phase timing automatically converges on soft-charging operation. The technique is validated on an 8-to-1 resonant single-inductor Dickson hardware prototype. While this method is demonstrated on a resonant fixed-ratio converter in this work, the technique can also be applied to regulating split-phase applications, as well as used to detect hard-charging events in general.**

I. Introduction

Hybrid switched-capacitor (SC) converters have become increasingly popular in applications where both high efficiency and high power density are required. Their combined use of energy-dense capacitors for power conversion and augmenting inductors for capacitor soft-charging allows for high performance designs without the inrush current losses of pure SC converters. Therefore, they are gaining popularity in high performance applications such as data center power delivery and automotive drivetrains. For example, high efficiency high step-down converters can be used as first-stage intermediate bus converters, to step the 48 V bus in data centers down to the low voltage used at the point-of-load (PoL) by the CPUs and GPUs. By increasing the conversion ratio of this first-stage, the overall performance of the power delivery network can be increased, as this allows the second stage buck converters to operate more efficiently at a lower input voltage [1]–[3]. Previous work has demonstrated several high performance large step-down hybrid SC converters used in this application [4], [5]. In addition, hybrid SC converters have also been applied to electric drivetrains, both for use with the high voltage battery bus as well as lower voltage 48 V peripheral buses [6]–[10].

One popular SC topology is the Dickson converter, which can be implemented both as a pure SC converter [11], [12] or a hybrid SC converter [13], [14]. The Dickson converter can achieve very efficient switch utilization [15] and exhibits the theoretical minimum switch stress compared to other SC converters [16]. However, while other hybrid SC topologies can softly charge all flying capacitors through the proper placement of one or more inductors [17], [18] – thereby avoiding the large impulse currents and corresponding losses associated with hard capacitor charge redistribution – soft-charging in the Dickson converter is not as straightforward. To obtain full soft-charging, the Dickson converter requires either specific capacitor sizing (applicable to only odd-conversion ratios), such as that presented in [19] for a 7-to-1 converter, or the use of a split-phase control technique, as presented in [13]. Split-phase operation introduces two sub-phases in addition to the main two operating phases, wherein certain capacitors are independently connected or disconnected from the main network at optimal points in their discharge and charge cycle to ensure no discontinuous capacitor voltage transitions.

Previous work has presented different analytical approaches for calculating the required split-phase timings under various assumptions, such as negligible or linear inductor current ripple [13], [20]. While [21] presents a full-ripple second-order LC analysis, all of these above methods assume constant capacitance and inductance values. In practice, these assumptions may break down if operating under large-ripple conditions or if using Class II multi-layer ceramic capacitors (MLCCs) and soft-saturating magnetics, whose values derate as a function of operating conditions. As a result of these real-world impacts, the necessary timings required for full-soft charging can deviate substantially from the calculated values found using analytical methods. Furthermore, while the higher fidelity calculation methods may be able to produce more accurate results, they can become quite complex to implement in hardware as they require the use of extensive lookup tables collected across the full range of operating conditions.

This paper therefore presents an active split-phase control technique that detects hard-charging events on the flying capacitors and continuously tunes the switch gating signals to achieve soft-charging. This control technique is demonstrated on an 8-to-1 resonant Dickson converter implemented with

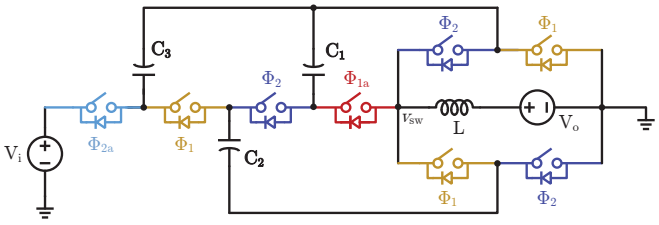

Fig. 1: Schematic drawing of a 4-to-1 single-inductor resonant Dickson converter, with operating phases labeled. Φ_1 and Φ_2 are the main operating control signals, while Φ_{1a} and Φ_{2a} are the split-phase control signals.

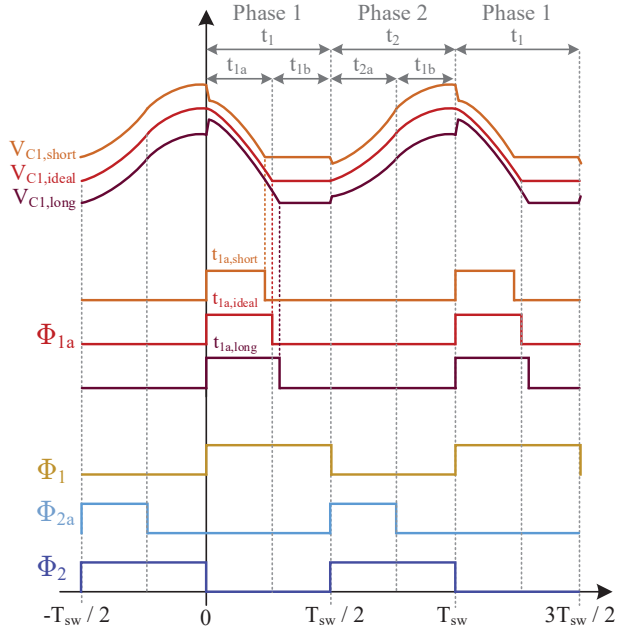

Fig. 2: Gating signals for the converter in Fig. 1. The capacitor voltage across C_1 is also shown for soft-charging operation (correct timing) and hard-charging operation (too long or too short timing).

Class II MLCCs and a soft-saturating composite inductor, and is shown to converge on soft-charging split-phase timings. A similar active control method has been recently proposed specifically for regulating Dickson converters [22], wherein the capacitor voltages are sensed during the "quiet" regulating phases where the capacitor network is left open-circuited, such that no charge flows. While this allows for simplified circuitry and low-bandwidth sensing, these phases do not exist in resonant fixed-ratio converters, necessitating other detection methods such as the one presented in this work. Moreover, while this hard-charging detection technique is validated here with resonant capacitor voltage waveforms, it is general in approach and can be tuned to detect hard-charging events in a wide variety of circuit topologies and operating modes.

II. Theory of Operation

For the sake of demonstration, the control method is described for a 4-to-1 resonant Dickson topology, but can easily be extended to N-to-1 Dickson converters. Fig. 1 shows a schematic drawing of the 4-to-1 topology, with gating signals as labeled. The converter is operated with two main phases, Phase 1 and Phase 2, with durations of t_1 and t_2 and gating signals ϕ_1 and ϕ_2. Both phases operate with 50% duty cycle. To achieve soft-charging, two additional sub-phases, Phase 1a and Phase 2a, can be introduced with durations $t_{1\mathrm{a}}$ and $t_{2\mathrm{a}}$ and gating signals ϕ_{1a} and ϕ_{2a}, as shown in Fig. 2. For the 4-to-1 topology shown in Fig. 1, these sub-phases ensure that C_1 and C_3 are disconnected once their voltages have reached the values that satisfy the KVL loop defined by the next phase equivalent circuit, as described in [13]. If the capacitor voltages deviate from these values at the start of the next phase, hard charge redistribution will occur, resulting in increased losses. For a general N-to-1 Dickson converter with $N-1$ flying capacitors, only capacitors $C_{\mathrm{N}-1}$ and C_1 will require split-phase switching, making the analysis easily extendable to higher-order conversion ratios.

In an ideal Dickson converter, Phase 1 and Phase 2 (and their corresponding sub-phases) are equivalent, such that the phase time durations satisfy $t_{1\mathrm{a}} = t_{2\mathrm{a}} = t_{\mathrm{a}}$ and $t_{1\mathrm{b}} = t_{2\mathrm{b}} = t_{\mathrm{b}}$. This work therefore only senses the voltage of the low-side split-phase capacitor, C_1, and then modifies both $t_{1\mathrm{a}}$ and $t_{2\mathrm{a}}$ simultaneously. However, both split-phase capacitor (C_1 and C_3) voltages could be sensed to allow for independent modulation of the split-phase times, though this is not explored in this work. Finally, the converter is assumed to operate with a fixed frequency, such that only $t_{1\mathrm{a}}$ and $t_{2\mathrm{a}}$ are changed by the feedback loop, while t_1 and t_2 remain constant.

Fig. 2 shows characteristic capacitor voltage waveforms for C_1 for both soft-charging and hard-charging operation. When the split-phase time duration $t_{1\mathrm{a}}$ is correctly tuned, the capacitor voltage will exhibit a smooth continuous waveform throughout the switching period, as demonstrated by $V_{\mathrm{C_1,ideal}}$. However, if t_a is off in either direction, the capacitor voltage will experience sharp discontinuities as hard charge redistribution occurs when the converter enters the next operating phase. The polarity of these discontinuities corresponds to whether the previous timing was too short or too long. A steep negative slope – as demonstrated by $V_{\mathrm{C_1,short}}$ – corresponds to split-phase time durations $t_{1\mathrm{a}}$ and $t_{2\mathrm{a}}$ that are too short, while a steep positive slope – as demonstrated by $V_{\mathrm{C_1,long}}$ – corresponds to split-phase time durations that are too long. The proposed control method is designed to detect these discontinuities, and based on the polarity, appropriately increase or decrease the split-phase times.

This technique is similar to the zero-voltage-switching (ZVS) detection methods presented in [23], [24]. The methods are somewhat analogous, as here the control detects a resonant soft-charged capacitor voltage versus a discontinuous hard-charged capacitor voltage, while the ZVS control in the referenced works detects a resonant drain-to-source voltage versus a discontinuous hard-switching drain-to-source voltage. However, these ZVS detection methods are only designed for ground-referenced switches, while the proposed method can handle the floating voltages characteristic of flying capacitors in hybrid SC converters.

A. Analog Circuitry

The control architecture is presented in Fig. 3. The analog circuitry is powered by a single supply of $V_{\mathrm{cc}} = 5$ V. The first stage consists of a subtractor circuit, which converts the differ-

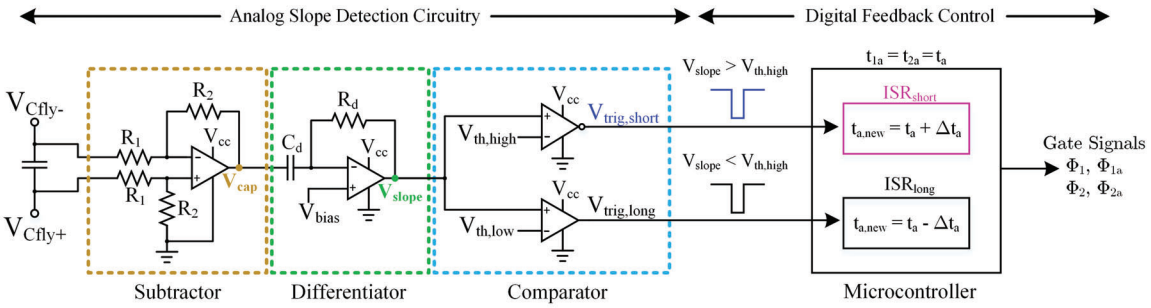

Fig. 3: Schematic of the active split-phase control circuitry, including the analog slope detect circuitry and the controller logic. The "short" timing path is color-coded to match the experimental waveforms shown in Fig. 8.

ential flying capacitor voltage to a single-ended voltage, given by $V_{\text{cap}} = \frac{R_2}{R_1} \cdot (V_{\text{Cfly}+} - V_{\text{Cfly}-})$. This voltage is then fed into an active differentiator circuit, whose output is proportional to the slope of the input, given by $V_{\text{slope}} = -R_d C_d \frac{dV_{\text{cap}}}{dt} + V_{\text{bias}}$. The signal is biased around $V_{\text{bias}} = 2.5$ V so that it is centered between the comparator supply rails, where V_{bias} is created using a simple resistor divider powered from the V_{cc} rail.

When a hard-charging event occurs at the Phase 2-to-Phase 1 transition (as labeled in Fig. 2), the steep slope present in V_{Cfly} and V_{cap} generates a large pulse on V_{slope}. This signal is then compared to two different threshold voltages, $V_{\text{th,high}}$ and $V_{\text{th,low}}$, to determine whether the hard-charging event is caused by too short or too long of split-phase timing. These thresholds are also set using simple resistor dividers supplied by the V_{cc} rail, and are only tuned during initial circuit design. The threshold levels should be set so that the detection circuit triggers the comparators correctly at low current, as the magnitude of the pulse will be at its lowest at light load.

As an example, if the split-phase timing is too short, the upward pulse on V_{slope} will go above $V_{\text{th,high}}$, generating a falling edge on $V_{\text{trig,short}}$. This then triggers an external interrupt in the microcontroller, so that the phase timing can be updated. Fig. 4 illustrates the output of each stage of the control circuitry for the case where the split-phase time duration, t_a, is too short. Similarly, if the split-phase timing is too long, V_{slope} will exhibit a downward pulse that will go below $V_{\text{th,low}}$, generating a falling edge on $V_{\text{trig,long}}$ and triggering the corresponding external interrupt.

Note that while V_{slope} is fed into the positive terminal of both comparator channels, the inverted comparator output is used to generate $V_{\text{trig,short}}$, while the non-inverted comparator output is used to generate $V_{\text{trig,long}}$. This is done to simplify the hysteresis resistor network used to prevent oscillations around the trigger level (not shown in Fig. 3).

In practice, the capacitor voltage discontinuities can be larger at the Phase 2-to-Phase 1 transition compared to the Phase 1-to-Phase 2 transition (as shown in Fig. 2), in part due to parasitic effects. This results in a larger corresponding pulse in V_{slope}, which is easier to sense. However, the control could be adjusted to monitor both phase transitions to detect hard-charging events at twice the frequency, though a more conservative control approach may be to only adjust duty cycle timings once per switching cycle, such that Phase 1 and Phase 2 remain symmetrical within one switching period.

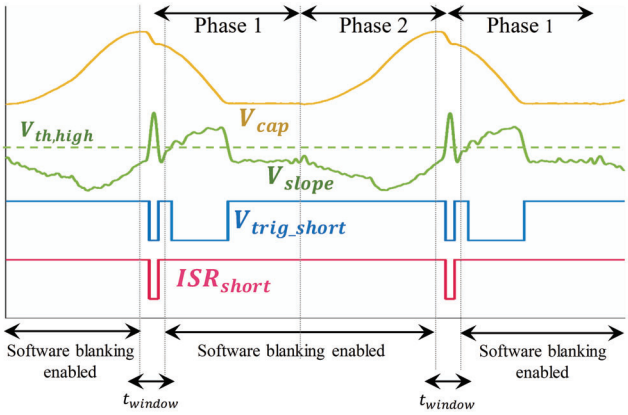

Fig. 4: Simplified control circuit waveforms, corresponding to the case where t_a is too short. The output of each control stage is plotted. A blanking window is implemented in code to isolate only the V_{slope} pulses at the Phase 2-to-Phase 1 transition.

B. Microcontroller Feedback

Depending on which comparator channel triggers the controller, the duration of t_a will be increased or decreased. For example, a falling edge on $V_{\text{trig,short}}$ will trigger the interrupt service routine, ISR_{short}, which will increase the split-phase time t_a by a step-size Δt_a. Similarly, ISR_{long} will decrease t_a by Δt_a, as shown in Fig. 3. This step-size can be tuned to achieve the desired trade-off between the control convergence speed and overshoot behavior.

As mentioned previously, the amplitude of the pulse on V_{slope} will increase with load current. Therefore, to increase the sensitivity of the hard-charging detection circuitry at light load, the trigger thresholds should be set as close to the level of the soft-charged V_{slope} waveform as possible. However, as can be seen in Fig. 4, at other times in the switching period V_{slope} can exceed this threshold level even when not in the presence of a hard-charging event, due to the sinusoidal shape of the capacitor voltage waveform. To account for this, the V_{slope} signal is only monitored by the controller during a time t_{window}, centered around the peak of V_{cap} at the Phase 2-to-Phase 1 transition. A software-enabled blanking window ignores any other comparator triggers, so that the controller will only modify t_a in this window, regardless of whether $V_{\text{slope}} > V_{\text{th,high}}$ at other times during the switching

TABLE I: Power Stage and Control Components

8-to-1 Dickson Power Stage Components

Component	Part Number	Description
Switches	IQE006NE2LM5	Si MOSFET, 25 V, 0.65 mΩ
Gate Driver	LT4440-5	80 V, high-side
Inductor	IHLP5050EZERR68M01	680 nH, 54 A I_{sat}, 1.7 mΩ
Fly Capacitors		4 μF derated
C_1	C2012X7R1V225K085AC	2 × 2.2 μF ± 10%, 35 V X7R 0805
C_2	CGA5l3X7R1V225K160AB	2 × 2.2μF ± 10%, 35 V, X7R 1206
C_3	CGA5l3X7R1V225K160AB	1 × 2.2 μF ± 10%. 35 V, X7R 1206
	C3216X5R1V475K085AB	1 × 4.7 μF ± 10%, 35 V, X5R 1206
C_4	CGA5l3X7R1V225K160AB	3 × 2.2 μF ± 10%, 35 V, X7R 1206
C_5	C3216X5R1H106K160AB	2 × 10 μF ± 10%, 50 V, X5R 1206
C_6	C3216X5R1H106K160AB	2 × 10 μF ± 10%, 50 V, X5R 1206
	CGJ4J3X7R1E105K125AB	1 × 0.68 μF ± 10%, 50 V, X5R 1206
C_7	C3216X5R1H106K160AB	3 × 10 μF ± 10%, 50 V, X5R 1206

Control Board Components

Component	Part Number	Description
Subtractor op-amp	AD8091	145 V/μs, 110 MHz
Differentiator op-amp	AD8091	145 V/μs, 110 MHz
Comparator	AD8611	Ultrafast 4 ns Single-Supply
Controller	F28379D	Delfino Experimenter Kit

Control Biasing Components

Component	Value
Voltage divider resistor, R_1	49.9 kΩ, 0.1%
Voltage divider resistor, R_2	4.99 kΩ, 0.1%
Filter resistor, R_d	4.99 kΩ, 0.1%
Filter capacitor, C_d	3 × 220 pF

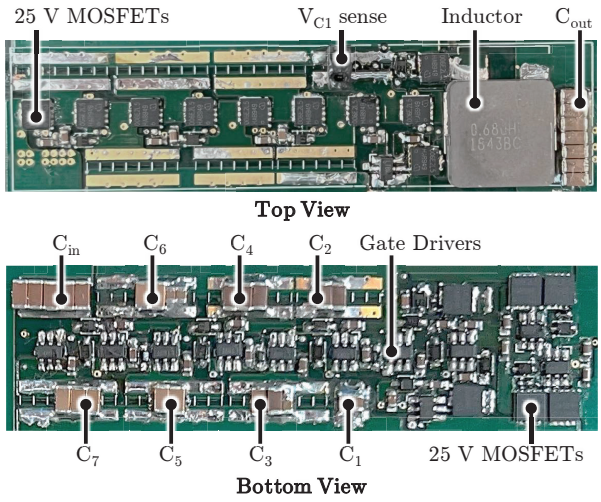

Fig. 5: Annotated photograph of the 8-to-1 Dickson power stage, with main components labeled. Dimensions: 2.8 in (7.0 cm) x 0.7 in (1.8 cm).

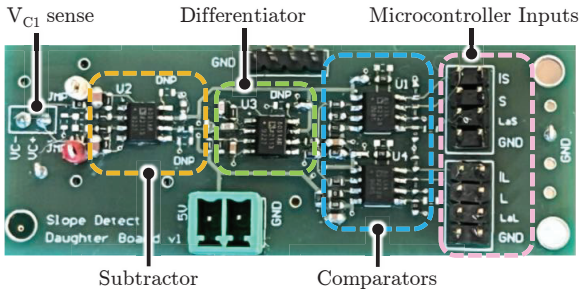

Fig. 6: Annotated photograph of the single-sided control daughterboard. Dimensions: 2.8 in (7.0 cm) x 1.1 in (2.8 cm).

period. Fig. 4 illustrates this software blanking window for the case where the split-phase timing is too short. The threshold $V_{\text{th,high}}$ is set near the base of the upward pulse on V_{slope}, allowing for the circuitry to detect hard-charging events across a wide load range. Extra filtering, such as additional high-pass filters, can be added to push down the noise floor of V_{slope} to allow for easier detection of hard-charging events. However, this can further attenuate the amplitude of the pulse and also requires more circuit stages, presenting a trade-off for the designer.

The control uses a hysteretic approach to converge onto the split-phase timing that results in soft-charging. Because $V_{\text{th,high}} \neq V_{\text{th,low}}$, when converging on split-phase timing from a hard-charging condition, the converter will enter a hysteresis band defined by these thresholds, preventing oscillatory behavior and allowing the control to more easily maintain a steady state timing.

III. Experimental Results

The hard-charging detection circuitry was validated on an 8-to-1 resonant Dickson converter, as shown in Fig. 5. The converter was designed with a derated flying capacitance of 4 μF and an inductance of 680 μH, while the switches were implemented with 25 V Si MOSFETs. The hard-charging detection circuitry was implemented as a daughterboard mounted on top of the 8-to-1 Dickson converter. Fig. 6 shows an annotated photograph of the daughterboard, highlighting the individual stages of the control circuitry. Table I gives a full list of the main components for the 8-to-1 Dickson power stage and the control daughterboard, as labeled in Fig. 5 and Fig. 6. The experimental setup was tested at an input voltage of 48 V and an unregulated output voltage of 6 V, up to an output current of 10 A (60 W), as summarized in Table II. The total power draw of the control circuitry from the V_{cc} rail was 90 mW across the load range. The threshold levels $V_{\text{th,high}}$ and $V_{\text{th,low}}$ were tuned during initial circuit design, and were implemented using 0.1 V hysteresis to prevent comparator oscillation.

A. Control Circuit Tradeoffs

The daughterboard was designed for control validation, and therefore used separate ICs for each stage. However, total board area could be significantly reduced by combining both the subtractor and differentiator stages as well as the comparator stages into single ICs, reducing the total number of discrete ICs from four to two.

TABLE II: Operating Parameters

Parameter	Description	Value
Power Stage		
V_{in}	Input Voltage	48 V
V_{out}	Output voltage	6 V
$I_{\text{load,max}}$	Full load current	10 A
f_{sw}	Switching frequency	67.5 kHz
Control Biasing		
V_{bias}	Bias voltage	2.5 V
$V_{\text{th,high}}$*	High threshold	2.58 V
$V_{\text{th,low}}$*	Low threshold	2.43 V
P_{ctrl}	Control power	90 mW

*with 0.1 V hysteresis

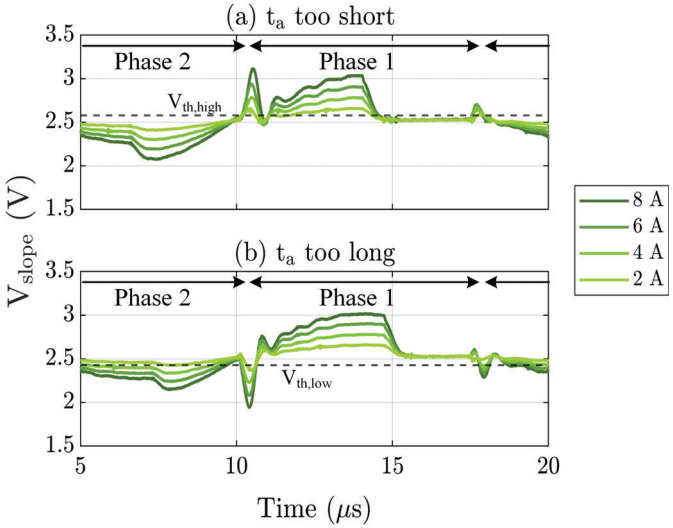

Fig. 7: Experimental V_{slope} waveforms across several values of I_{load}, for (a) "too short" t_a and (b) "too long" t_a. At the Phase 2-to-Phase 1 transition, a short t_a results in an upwards pulse on V_{slope}, while a long t_a results in a downwards pulse. The comparator trigger thresholds $V_{\text{th,high}}$ and $V_{\text{th,low}}$ are also plotted.

While the subtractor op-amp should have a high enough slew rate to faithfully replicate the steep discontinuities on the capacitor voltage waveform, the slew rate requirement on the differentiator may not be as stringent depending on the converter operating parameters. Therefore, the designer could choose to use different op-amp ICs for the subtractor and differentiator stages to reduce the total power draw of the control circuitry. These specifications can be set to achieve the desired trade off between power consumption and filter performance.

B. Experimental Validation

Experimental V_{slope} waveforms are plotted in Fig. 7 for a range of load currents, I_{load}. Fig. 7 (a) shows the case where the split-phase time t_a is too short, and V_{slope} sees an upwards pulse at the phase transitions. The magnitude of the pulse increases with load current. Fig. 7 (b) shows the case where the split-phase time t_a is too long, and V_{slope} sees a downwards pulse at the phase transitions. As mentioned previously, the pulse at the Phase 1-to-Phase 2 transition can have a lower magnitude compared to the pulse at the Phase 2-to-Phase 1 transition, due to deadtime dynamics. The comparator threshold levels, $V_{\text{th,high}}$ and $V_{\text{th,low}}$, are also plotted, and are set as close to the base of the pulse as possible to allow the control to trigger at low current. Spurious triggering at other points in the switching period is prevented by the control windowing described in Section II. B.

Fig. 8 shows experimental waveforms for the converter before, during, and after convergence to a soft-charging state when operating at 48 V input, 6 V output, and 5 A load current. The converter is initialized with too short of a t_a value, resulting in downward step discontinuities on the capacitor voltage, V_{cap}. Once the control is enabled, the circuitry detects the resulting large upward pulse on V_{slope}, causing $V_{\text{trig,short}}$ to be pulled low and ISR_{short} to be triggered. The ISR increases the split-phase times $t_{1\text{a}}$ and $t_{2\text{a}}$ by a step size Δt_a until the converter reaches a timing that results in smooth, soft-charged capacitor voltage waveforms. The software blanking window ignores any comparator triggering outside of the phase transition window, t_{window}. After convergence, the controller continues to ignore comparator falling edges outside of t_{window}, and will remain in this steady-state condition unless perturbed.

Similarly, Fig. 9 shows experimental waveforms before, during, and after convergence when the converter is initialized with too long of a t_a timing, again at 48 V input, 6 V output, and 5 A load current. This improper timing results in an upward step discontinuity on V_{cap}, which triggers ISR_{long} once the control is enabled. The converter is similarly able to converge on the correct split-phase timing, resulting in smooth capacitor voltages.

The converter was also tested with various load steps while operating under closed-loop control, to test the ability of the control loop to re-converge on soft-charging timing when perturbed. Fig. 10 shows a load step from 25% to 75% of full load (i.e. 2.5 A to 7.5 A). As I_{load} ramps up, the split-phase timing becomes too long for the new load condition, resulting in ISR_{long} triggering for a time $t_{\text{control}} = 85.5$ μs after the load step. At this point, V_{cap} no longer exhibits hard-charging, and the converter takes an additional 126.5 μs to reach a new steady state, resulting in a total settling time $t_{\text{settle}} = 212$ μs (approximately 14 switching cycles).

Fig. 11 shows a similar load step from 75% to 25% of full load (i.e. 7.5 A to 2.5 A). As I_{load} ramps down, the split-phase timing is initially too short, triggering ISR_{short}. The control slightly overshoots, resulting in ISR_{long} triggering briefly. After 128 μs, the capacitor voltage converges to smooth waveforms, and the converter then takes an additional 44 μs to reach its new steady state condition, for a total settling time of $t_{\text{settle}} = 172\mu s$ (approximately 12 switching cycles).

The above hardware waveforms demonstrate that the control loop can converge on the correct split-phase timing required for soft-charging in the case of 1) incorrect timing initialization, and 2) load perturbations, thereby allowing the converter to achieve soft-charging across a wide range of operating conditions.

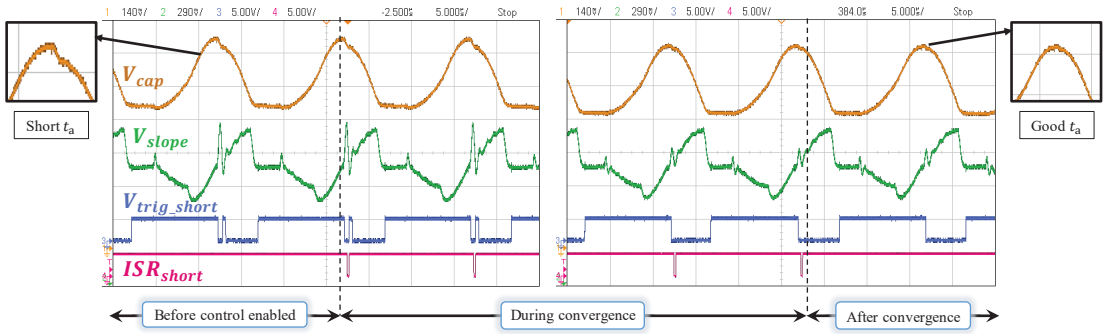

Fig. 8: Experimental waveforms for the converter operating at 48 V input, 6 V output, and 5 A load current. The converter is initialized with a split-phase time t_a, which is shorter than that required for soft-charging. After control is enabled, the converter converges on smooth capacitor voltage waveforms.

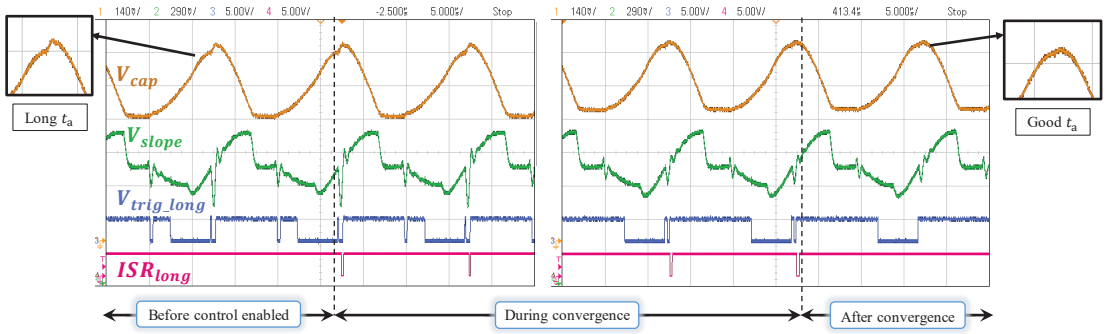

Fig. 9: Experimental waveforms for the converter operating at 48 V input, 6 V output, and 5 A load current. The converter is initialized with a split-phase time t_a, which is longer than that required for soft-charging. After control is enabled, the converter converges on smooth capacitor voltage waveforms.

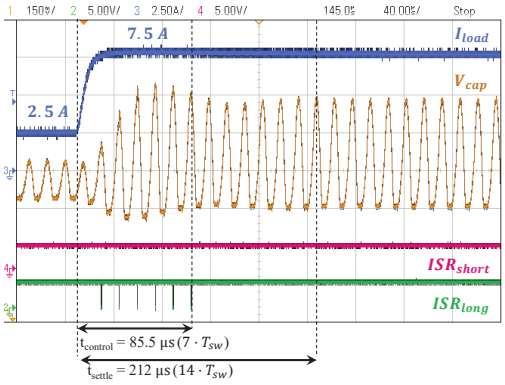

Fig. 10: System waveforms for a load step of 2.5 A to 7.5 A. The control takes 85.5 μs to converge on soft-charged split-phase timing. The converter takes a total of 212 μs (approximately 14 switching periods, T_{sw}) to settle to its new steady state condition.

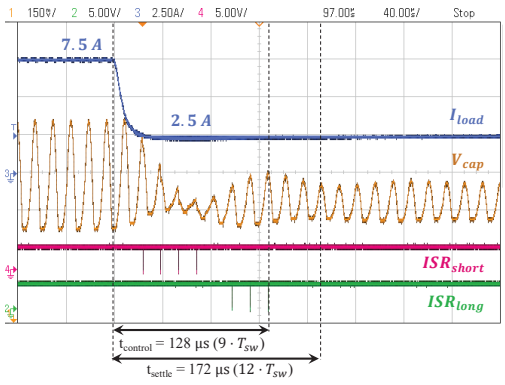

Fig. 11: System waveforms for a load step of 7.5 A to 2.5 A. The control actively takes 128 μs to converge on soft-charged split-phase timing. The converter takes a total of 172 μs (approximately 12 switching periods, T_{sw}) to settle to its new steady state condition.

IV. Conclusion

Certain Dickson converter variants require the use of split-phase switching to soft-charge all flying capacitors. While the split-phase timing can be calculated analytically, in practice this can be complex or inaccurate due to component tolerances and variable operating conditions. This paper discusses the design and validation of an active control circuitry which detects hard-charging events in the capacitor voltage waveforms and tunes the split-phase timing accordingly to achieve soft-charging. The control was validated on an 8-to-1 resonant Dickson converter prototype, and was able to correctly detect improper split-phase timing and converge on soft-charging operating conditions. Furthermore, when operating under closed-loop control, the converter was able to maintain soft-charging timing even under changing load conditions. This method can account for component value deviations in Class II capacitors or soft-saturation magnetics, and enables operation over a wider range of conditions. In addition, the technique can also be applied to a variety of converter topologies and operating modes, wherever hard-charging may occur.

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