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A Six-level Flying Capacitor Multi-level Converter for Single Phase Buck-type Power Factor Correction

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***Abstract*—This work investigates behavior of flying capacitor multi-level (FCML) converters in single phase buck-type power factor correction (PFC) applications. Recent developments in FCML converters using GaN transistors are leveraged to improve power density of a single-phase 240 V_{RMS} ac to direct 48 V dc conversion stage in data center power delivery applications. Here, we experimentally demonstrate this concept in a digitally controlled six-level FCML converter hardware prototype. The experimental prototype can deliver 4.5 A average output current at 48 V, resulting in 216 W output power. A key contribution of this work is experimental demonstration of an FCML buck converter in a single-phase PFC application where the flying capacitor voltages follow fractions of the rectified input voltage by swinging at twice-line frequency.**

***Index Terms*—Flying Capacitor Multilevel Converters, Buck-type Power Factor Correction, Server Power Delivery**

I. INTRODUCTION

Due to the low dc supply voltage need of computing and storage circuits, data centers employ many cascaded power converters that convert grid voltage to low voltage dc. During this conversion process, the power converters step up and down the voltage several times, and must achieve power factor correction (PFC) and twice-line frequency energy buffering.

An example of a conventional data center power delivery architecture is shown in Fig. 1. Here, utility scale 50/60 Hz transformers and power distribution units provide single phase ac power (e.g., 240 V_{RMS}) to the server racks. The single phase ac voltage is rectified at the rack level by a diode bridge or active rectifier, then boosted up to a higher dc voltage (e.g., 400 V) for power factor correction (PFC) and twice-line frequency energy buffering. Following this, the high dc voltage is stepped back down to 48 V to be delivered to server blades through a dc bus. A recent trend in data center power delivery applications is to place the uninterruptible power supply (UPS) at the dc bus in the rack, as shown in Fig. 1. A dc-dc converter (commonly known as an intermediate bus converter) is employed to step down the bus voltage (to typically 9-12 V), followed by multiple point-of-load (PoL) converters to provide low-voltage (e.g., 1 V, 1.8 V, 3.3 V) to various digital loads such as central processing unit and memory. Alternatively, PoL converters can be directly connected to the 48 V to provide a single stage solution. As can be seen in Fig. 1, numerous power converters are employed to ultimately regulate a few volts for computing and storage elements. Electrical isolation has been an essential part of data center power delivery architectures, and may be implemented at various points depending on the preferred data center power delivery architecture. Although typically the step-down dc-dc converter between high voltage dc bus and 48 V [1] or between 48 V dc bus and 12 V [2] provides isolation, recently unity transformation ratio dc-dc converters that provide only electrical isolation (without voltage conversion) have also been demonstrated at 400 V [3] and 48 V [4] for data center applications. This work investigates a single phase ac to non-isolated 48 V dc power conversion stage for data center applications. A unity transformation ratio converter can be attached to the output of the proposed converter, if so desired.

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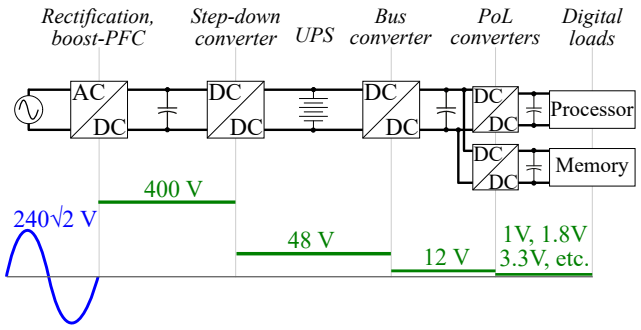


Fig. 1. An example of conventional power delivery in data centers illustrating main power conversion stages with annotated voltage levels.

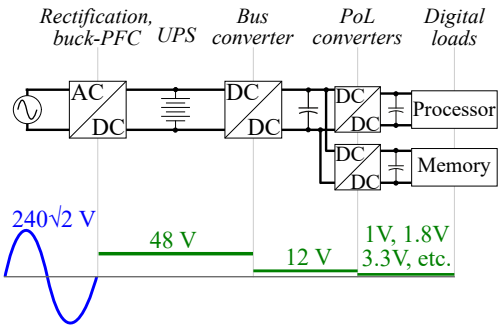


Fig. 2. A single-stage power conversion from single phase ac source to 48 V dc.

Conventionally, power conversion between single phase ac and 48 V dc in data center applications involve a two-stage solution: i.e., a boost-type PFC and a high voltage step down dc-dc converter, as illustrated in Fig. 1. Seeking a single-stage solution in this application, as illustrated in Fig. 2, could have various advantages. First, stepping up the voltage for the PFC and twice-line frequency energy buffering, and then stepping down the voltage for power distribution on the motherboard is a counter-productive approach since the final loads are at various low dc voltage levels that are much below the high dc voltage created to achieve PFC. In addition, a two-stage solution requires both power stages to be optimized, implemented, controlled and tested separately. Furthermore, the power is being processed twice, limiting the system level efficiency, and increasing total power converter footprint. Thus, recently many research efforts have focused on the efficiency and power density improvements of boost-type PFC, and high voltage step-down converters. For instance, in recent literature a carefully optimized boost-type PFC converter has an efficiency curve ranging from 97.7% to 98.8% and a power density of 220 W/in^3 [5], and a carefully optimized 400 V to 48 V dc-dc converter has a peak efficiency of 94.5% and a power density of 164 W/in^3 [1]. Combining these two stages would yield a best-case 93.4% efficiency and 94 W/in^3 power density. On the other hand, commercial products achieve 92% typical efficiency and 140 W/in^3 power density [6] for boost PFC, and 93.6% peak efficiency and 258 W/in^3 power density [7] for 400 V to 48 V dc-dc conversion. Combining these two stages would yield a best-case 86.1% efficiency and 90.8 W/in^3 power density. Note that these above mentioned converter efficiencies and power densities do not include twice-line frequency energy buffering solutions; however, they provide isolated 48 V dc output.

In this work, we seek to leverage the 48 V UPS to provide the twice-line frequency energy buffering, and to investigate a single stage 240 V_{RMS} to 48 V buck-type converter for PFC to target the efficiency and power density improvements between the single-phase ac input and the dc bus. This work is based on our previously published conference paper [8], and includes additional details on hardware prototype design, extended explanation of the control algorithm, and refined experimental results. An added contribution of this manuscript is the mathematical details of input current displacement compensation which takes into account effective input capacitance in a FCML converter. Furthermore, the additional details on hardware prototype include an extended component list and annotated pictures of the prototype. Different from the experimental results in the conference submission, the experimental results in this manuscript focus on the impact of the input current displacement compensation algorithm in power conversion efficiency and power factor at 240 V_{RMS}. In addition, key experimental results that investigate the value of passives and switching frequency in the hardware prototype and how they impact the flying capacitor voltage behavior are provided. The remainder of this paper is organized as follows: Section II provides background information on buck-type PFC conversion and flying capacitor multi-level converters, and states the key contributions of this work. The proposed PFC control algorithm is explained in detail in Section III. Section IV presents the six-level FCML buck converter hardware prototype and the experimental results; and Section V concludes the paper. Appendix A summarizes key experimental results when determining the value of passives and switching frequency in the hardware prototype.

II. Buck-type PFC with FCML converter

The buck converter can perform power factor correction in single phase ac to dc applications [9]–[12], though achieving unity power factor is theoretically not possible. This is due to the nature of the converter, i.e., when the input voltage is less than the output voltage, the buck converter cannot draw current from its input terminal, as depicted in Fig. 3. Power factor of

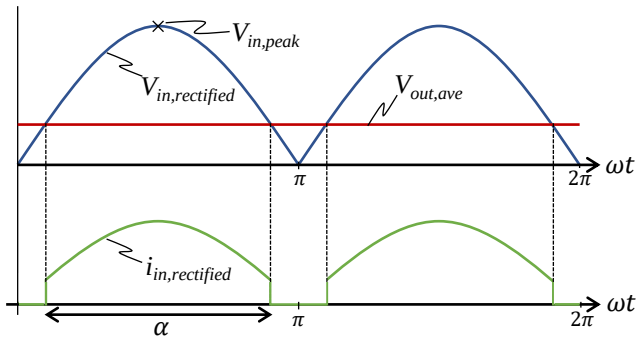


Fig. 3. Theoretical rectified input voltage, output voltage and rectified input current in a buck-type PFC.

a distorted but not displaced current waveform, similar to the one shown in Fig. 3, is equal to $i_{in,1,RMS}/i_{in,RMS}$. Using Fourier coefficient analysis, the theoretical limit of achievable power factor of the distorted input current in Fig. 3 can be calculated as

$$PF = \sqrt{\frac{\alpha}{\pi} + \frac{\sin(\alpha)}{\pi}} \tag{1}$$

where $\alpha = \pi - 2\sin^{-1}(V_{out,ave}/V_{in,peak})$. In this work, the target input voltage is 240 V_{RMS} and the target output voltage is 48 V, which reduces the theoretical achievable power factor to 0.999. It should be further noted that lower ac input voltage, as may be desired to accommodate universal input voltage range, would reduce α and result in lower power factor by (1). For example, the lower end of the universal voltage range, 85 V_{RMS}, reduces the theoretical achievable power factor to 0.986. In practice, because of PFC control limitations, output voltage ripple and input filtering, power factor is expected to be lower than the theoretical limit. Also, the rectified input current cannot suddenly change as depicted in the theoretical waveforms in Fig. 3, owing to non-negligible inductance. Typically, a secondary boost stage (activated only when the input voltage is below the low output dc voltage) is employed to achieve theoretical unity power factor [13]. Here, we explore non-unity power factor operation, where the step-down PFC turns-off when the line voltage is below 48 V.

To improve the power density, the buck converter can be replaced with a flying capacitor multi-level (FCML) converter [14]. In recent literature, FCML converters have been explored in high voltage step up [15] and down [16]–[18] dc-dc, dc-ac [19]–[22] and ac-dc [23], [24] power conversion applications employing low voltage wide band-gap semiconductor (GaN) switches to increase the power density of the conventional 2-level buck and boost topologies. Similar performance improvements can theoretically be realized in a multi-level buck-type PFC. However, employing an FCML buck converter in an ac-dc conversion application presents a unique operation case in which the flying capacitor voltages must follow the 50/60 Hz input voltage, which has significant practical challenges, which are explored in this work.

Shown in Fig. 4 is a schematic drawing of an N-level FCML step-down converter, which is used to briefly explain the operation and key theoretical advantages of the FCML converters. The ideal operation of the FCML converter can be summarized as follows: In Fig. 4, the switch pairs S_{iA} and S_{iB} where $i = 1, 2, ..., (N-1)$, are driven by complementary PWM signals at an equal switching frequency f_{sw}, with each high-side switch at a duty cycle of $D = V_{out}/V_{in}$, as in the conventional 2-level synchronous buck converter. Assuming the floating capacitors (also called flying capacitors) $C_{fly,j}$, where $j = 1, 2, ..., (N-2)$, are sufficiently large such that their voltage can be assumed constant during a switching period ($T_{sw} = 1/f_{sw}$), phase shifting the PWM signals that drive two consecutive switch pairs by $(N-1)/360°$ enforces equal charge and discharge times on the flying capacitors. In steady-state, when operated with properly phase-shifted PWM signals, $C_{fly,j}$ are charged to $j \times V_{in}/(N-1)$, which is commonly known as the natural flying capacitor voltage balancing property of FCML converters [25], [26]. By controlling the D of individual switch pairs, N different voltage levels ($k \times v_{in}/(N-1)$, where $k = 0...(N-1)$) can be achieved at the switching node at an effective frequency of $(N-1) \times f_{sw}$. The switching node voltage (V_{sw}) is then filtered by the filter inductor (L) and output capacitor (C_{out}) to achieve the desired output voltage. The key theoretical advantages of the FCML converters include: reduced switch voltage amplitude (each switch must only be rated for $V_{in}/(N-1)$), reduced voltage ripple on the inductor, and increased frequency at the switching node (the effective switching frequency ($f_{sw,eff}$) observed at the switching node is $(N-1) \times f_{sw}$). Theoretically, the FCML converter can achieve superior power density because of the reduced inductance requirement due to the reduced voltage magnitude at the switching node and the increased effective switching frequency.

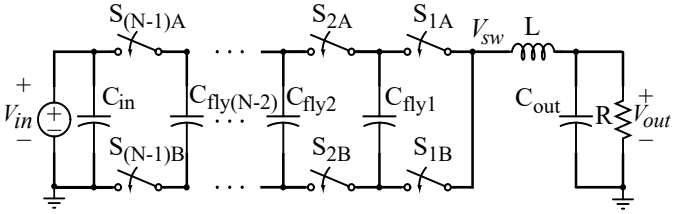


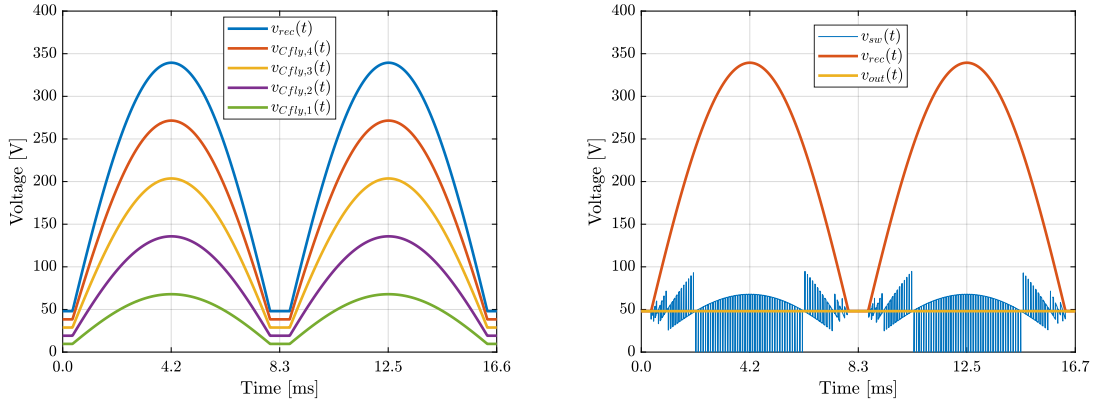
Fig. 4. N-level FCML buck converter.

The buck-type FCML converter shown in Fig. 4 is a well-known topology. However, its use in a PFC application where the flying capacitor voltages must follow the fractions of the rectified ac line voltage at 50/60 Hz in an ac-dc converter has not been previously demonstrated, and is a key contribution of this work. Past work where the flying capacitor voltages are subject to a voltage swing at the twice-line frequency include [27]–[29]. In [27], a four-level FCML buck converter is employed in an ac-ac application to step down the ac input voltage by using a fixed duty cycle during the entire line cycle. In [28] and [29], three-level FCML buck converters are modified with an auxiliary switch to utilize the flying capacitor as a twice-line frequency energy buffer in a single phase ac-dc application. Here, in contrast to [27], the FCML converter is used to achieve PFC in an ac-dc application which results in a unique operating scheme as the duty cycle changes at ac line frequency; and, in contrast to [28] and [29], the flying capacitors participate in energy conversion at the switching frequency rather than at the twice-line frequency to maintain the well-known advantages of FCML converters mentioned above. The nominal waveforms of the buck-type FCML converter during PFC operation are shown in Fig. 5.

III. PFC Control Algorithm

Although an FCML buck converter offers increased power density, it presents challenges in PFC control. In this section, a PFC control methodology that is applicable to the FCML buck topology is proposed.

PFC control of the buck converter has been thoroughly analyzed in the literature and several different control methods have been proposed. Most of the existing work in the literature



(a) Averaged flying capacitor voltage waveforms

(b) Switching node, input, and output voltage waveforms

Fig. 5. Ideal buck PFC system waveforms at V_{in} = 240 V_{RMS} and V_{out} = 48 V.

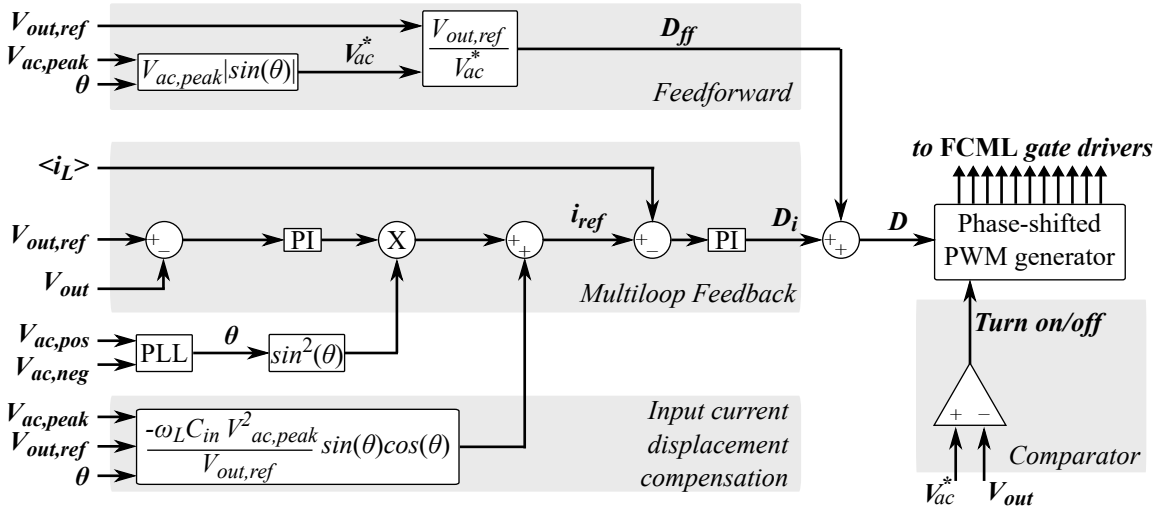


Fig. 6. High-level control diagram.

uses a full bridge rectifier followed by an asynchronous buck converter, in order to simply turn-off the converter by opening the high side switch when the input voltage is lower than the output voltage, and by controlling the on time of the high side switch to control the inductor current, similar to [12]. Such PFC control methodologies for buck converter are not directly applicable to an FCML buck topology because it employs synchronous switch pairs that are controlled with complementary phase shifted PWM signals. In phase-shifted PWM control, natural balancing of flying capacitor voltages relies on all flying capacitors charging and discharging for the same duration in each switching period. This makes cycle by cycle duty ratio adjustments to limit inductor current within a band at the switching frequency challenging. Moreover, flying capacitor voltages in a FCML topology for PFC in this work are expected to follow the input voltage at 50/60 Hz; therefore, they are not intended for twice line frequency energy buffering. In this work, feedforward control, combined with a high bandwidth inner current loop and a slower bandwidth outer voltage loop are used to generate the duty ratio, which is kept constant during each switching period to achieve natural balancing of flying capacitors with phase shifted PWM signals.

In order to focus on the PFC task in the development of the proposed control algorithm, twice-line frequency energy buffering is assumed to be handled by a capacitor bank at the converter output, and the FCML buck converter is assumed to achieve natural balancing of the flying capacitor voltages. Active voltage balancing of the flying capacitors such as [30] and advanced twice-line frequency energy buffering techniques such as [31] can be incorporated later if needed. The proposed control algorithm is applicable to any number of levels, including conventional (i.e., two-level) buck converter.

A. Overview of the proposed control algorithm

A high-level control diagram of the proposed PFC algorithm for the FCML buck converter is illustrated in Fig. 6. The algorithm is implemented on a 32-bit floating-point microcontroller with a 200 MHz system clock. The 12-bit ADC submodules of the microcontroller are used to sample the input voltage, output voltage, and output (or, average) inductor current, shown as $V_{ac,pos}$, $V_{ac,neg}$, V_{out}, and $< i_L >$ in Fig. 6, respectively. The control signal (i.e., duty ratio), shown as D in Fig. 6, is sent

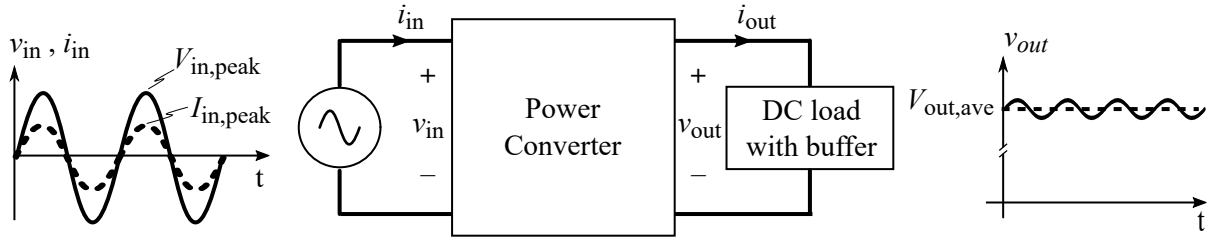


Fig. 7. A generic ac-dc power converter connected between a single-phase ac input source and a dc load that includes a twice-line frequency energy buffering element.

to the FCML gate drives through the PWM peripherals of the microcontroller. The ADC and control signal calculation are executed at a sampling frequency matched to the switching frequency. The microcontroller has a trigonometric math unit (TMU) which is used to construct signal equivalents of the input voltage and reference current. A similar control approach applied to boost PFC FCML converter can also be found in [24]. Note that by excluding the phase shifted PWM block in Fig. 6, the proposed algorithm can also be applied to a conventional two-level buck converter.

The proposed control algorithm comprises a feedforward term, D_{ff}, which provides the ideal duty ratio given the converter operating point, and a multiloop control term, D_i, which compensates the nonidealities which are not governed within the feedforward control. The multiloop control consists of a higher bandwidth inner current loop which tracks a desired reference current to achieve PFC and a slower bandwidth voltage loop which provides an amplitude for the reference current to regulate the output voltage. Other supporting functions of the proposed control algorithm include a phase-locked loop to synchronize the converter with the ac input voltage, a comparator to determine when the PFC algorithm and the converter should be turned on or off, and compensation for the line frequency displacement current drawn by the input capacitance, C_{in}.

B. PLL

A phase-locked loop (PLL) based adaptive notch filter is used to synchronize the converter with the ac input voltage. As shown in Fig. 6, the PLL control block uses $V_{ac,pos}$ and $V_{ac,neg}$ to extract the phase angle of the input ac voltage (denoted as θ in Fig. 6). Once the converter is locked to the ac input voltage, the peak value of the input voltage and the phase angle are used to construct a distortion- and noise-free replica of the input voltage (denoted as V_{ac}^* in Fig. 6) with the help of the TMU of the microcontroller.

C. Comparator

As stated in Section II, an FCML buck converter is unable to perform PFC and deliver power when the input voltage is less than the output voltage. Therefore, a comparator block is needed to compare the replica of the input voltage (V_{ac}^*) to the measured output voltage (V_{out}) at every sampling period. The output of the comparator is a logic high or low, indicating whether the converter must be turned on or off. The logic high is used to pass the sum of multiloop feedback and feedforward terms, D, to phase-shifted PWM generator to drive the transistors, while the logic low signal is used to open all transistors in the converter. Here, using the replica of the input voltage (V_{ac}^*) instead of the actual input voltage measurement prevents the converter from having a turn-on/off oscillation after it is enabled at every ac half-cycle.

D. Reference current

A reference signal is needed as an input to the current loop portion of the PFC controller so that the input current is in phase and sinusoidal when the input voltage is higher than the output voltage. As mentioned before, in this work, the high bandwidth inner current loop tracks the average inductor current which, unlike boost-type PFC converters, is at the converter output. Since the input current must be as sinusoidal as possible to achieve good power factor, power flow analysis is needed to identify a reference current for the average inductor current.

Figure 7 shows an ac-dc power converter that is connected between a single-phase ac power source and a dc load that includes a twice-line frequency buffering element. In single-phase ac-dc power conversion, unity power factor occurs when the input voltage, v_{in}, and current, i_{in}, are both sinusoidal and in phase (i.e., $v_{in}(t) = V_{in,peak}\sin(\omega t)$ and $i_{in}(t) = I_{in,peak}\sin(\omega t)$). The instantaneous input power is given by

$$P_{in}(t) = v_{in}(t)i_{in}(t) = V_{in,peak}\sin(\omega t)I_{in,peak}\sin(\omega t). \tag{2}$$

In this analysis, it is assumed that the power converter also provides twice-line frequency power buffering, through active or passive means. Under this assumption, although some voltage ripple still exists at the output, its amplitude will be much smaller than the average value of the output voltage. Thus, the output voltage is assumed to be constant in this analysis and $v_{out}(t) \approx V_{out,ave}$. The instantaneous output power is given by

$$P_{out}(t) = v_{out}(t)i_{out}(t) \approx V_{out,ave}i_{out}(t). \tag{3}$$

Further assume that the generic ac-dc power converter in Fig. 7 is ideal. By equating (2) and (3), a mathematical relationship for the instantaneous output current can be obtained as

$$i_{out}(t) = \frac{v_{in}(t)i_{in}(t)}{v_{out}(t)} = \frac{V_{in,peak}I_{in,peak}}{V_{out,ave}}\sin^2(\omega t). \tag{4}$$

Equation (4) means that sinusoidal and in-phase input current requires the output current to be proportional to a sine squared

waveform that is in phase with the input voltage. In order to compensate for losses that are ignored by equating (2) and (3), and also to achieve output voltage regulation, a proportionality constant K can be determined by the outer voltage loop. In conclusion, in order to achieve high power factor by tracking the output current (i.e., the average inductor current in a buck converter), the inner current loop reference is given by

$$i_{ref}(t) = \begin{cases} Ksin^2(\omega t), & \text{if } |v_{in}(t)| > v_{out}(t) \\ 0, & \text{otherwise.} \end{cases} \quad (5)$$

Once the PLL provides the angle of the input voltage, the TMU of the microcontroller can calculate the sine squared term in (5). A similar conclusion can also be found in [32]. In (5), $i_{ref}(t) = 0$ when the input voltage is not greater than the output voltage since the buck-type PFC can not draw current from its input terminal as shown in Fig. 3.

E. Feedforward control

Feedforward control is an effective method to improve control performance by reducing the effects of disturbances in PFC applications, and is often preferred in boost-type PFC converters [24], [33]. Here, feedforward is used to estimate the ideal duty ratio by using circuit equations that govern converter behavior. As mentioned before, the control algorithm is developed by approximating FCML buck converter dynamics with conventional buck converter dynamics. Thus, in order for the inductor current to follow the reference current derived above, the following first-order equation must be satisfied:

$$L\frac{\mathrm{d}i_L}{\mathrm{d}t} = v_{in}D - v_{out}. \quad (6)$$

Given the reference current i_{ref} and target output voltage $V_{out,ref}$, (6) can be rewritten as

$$L\frac{\mathrm{d}i_{ref}}{\mathrm{d}t} = v_{in}D - V_{out,ref}. \quad (7)$$

In order to obtain a feedforward term, (7) can be reorganized as

$$D = \frac{L}{v_{in}}\frac{\mathrm{d}i_{ref}}{\mathrm{d}t} + \frac{V_{out,ref}}{v_{in}}. \quad (8)$$

Considering the buck-FCML PFC application investigated in this work, the first term in (8) is very small relative to the second term since L is expected to be in micro-Henrys and i_{ref} changes at the line frequency. To simplify the discrete implementation of (8) in this work, the feedforward term can be approximated as:

$$D_{ff} = \frac{V_{out,ref}}{v_{in}}. \quad (9)$$

A similar approximation can also be found in [24] and [33] where a feedforward term that is similar to (9) is also derived for boost PFC converters and called "partial feedforward".

This work uses (9) to calculate the feedforward term, and relies on multiloop feedback control to track the reference current and voltage. Note that in Fig. 6 the actual implementation of (9) uses the signal replica of the input voltage (V_{ac}^*).

F. Multiloop feedback control

Multiloop control [34], which consists of a fast inner current loop and a slower voltage loop, is employed in this work. Both the inner loop and the outer loop employ proportional and integral (also known as PI, lag, or type 1) compensation, and are tuned by using a linearized small-signal converter model. The dynamic behavior of the FCML buck converter is approximated with the dynamic behavior of a conventional buck converter. (Interested readers can refer to [35] for an experimental validation of this approximation.) Since the proposed control algorithm is implemented using digital control, discrete time modeling of the buck converter and design of the PI compensator are preferred in this work. Although the small signal model is not completely appropriate for large signal (i.e., PFC) operation, in this work the feedforward term (i.e., (9)) brings the converter near an ideal operating point by providing the expected conversion ratio between input and output. Multiloop feedback control then compensates for nonidealities and uncertainties around the operating point provided by the feedforward term. The control loops are tuned using a discrete small-signal model. Interested readers can refer to [34] for complete details of discrete time modeling of a synchronous buck converter (Section 3.2.1 in [34]), and multiloop feedback control compensator design of a synchronous buck converter (Section 4.2.3 in [34]), and to [35] for the multiloop PI controller tuning details of the hardware prototype used in this work.

G. Input current displacement compensation

The dc-dc buck converter is well known to have discontinuous current at its input as a result of the high frequency switching action. Consequently, the input capacitance of the converter must be large enough to filter these harmonics and achieve an adequate dc input. Similarly, in PFC operation, a large input capacitance better filters switching harmonics; however, it also induces displacement current at the line frequency and degrades power factor. Appropriately sizing the input capacitance produces competing constraints when reducing the distortion versus displacement of the input current wave shape.

This work proposes to predictably adjust the reference current regulated at the converter output to achieve unity displacement power factor at the input in real-time for any value of input capacitance. Stated another way, the buck converter input impedance can be made to appear inductive and precisely counteract the capacitive impedance of the input capacitor. This compensated reference current can be derived with instantaneous power flow analysis

$$P_{in}(t) = P_{out}(t) + P_c(t) \quad (10)$$

where the instantaneous input and output power are defined in (2) and (3), respectively, and the instantaneous power contribution from all capacitors within the circuit is denoted by $P_c(t)$. For the traditional 2-level buck PFC converter, the

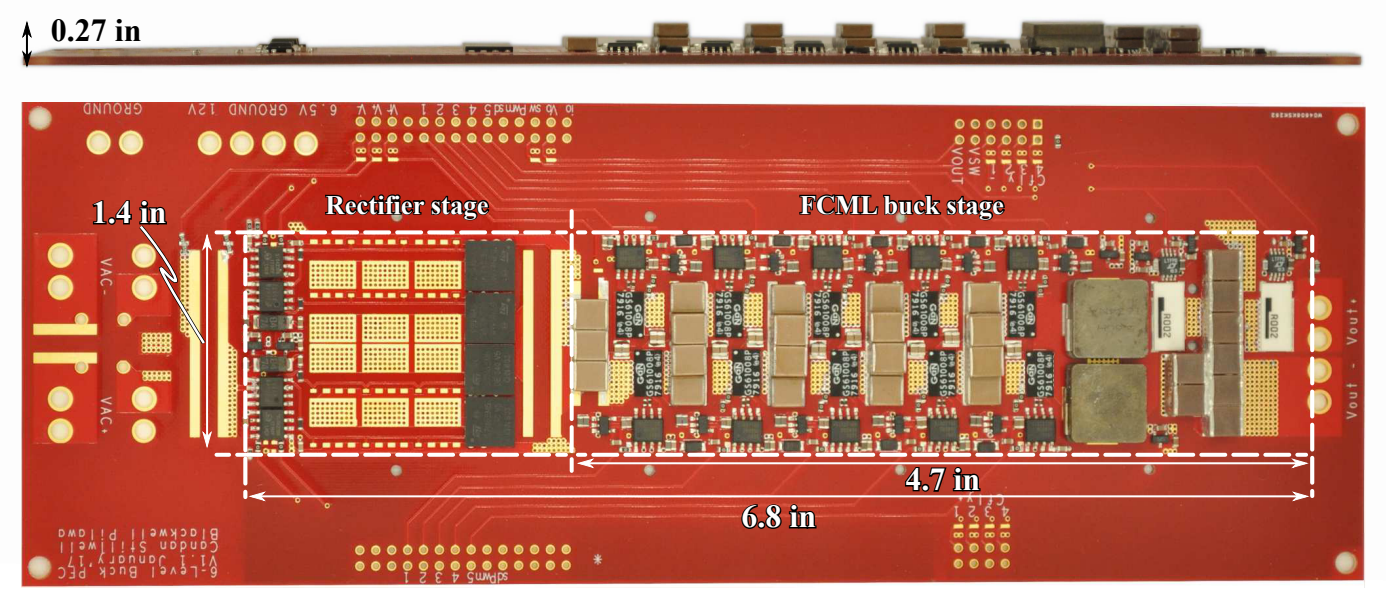


Fig. 8. The top and side view of the hardware prototype.

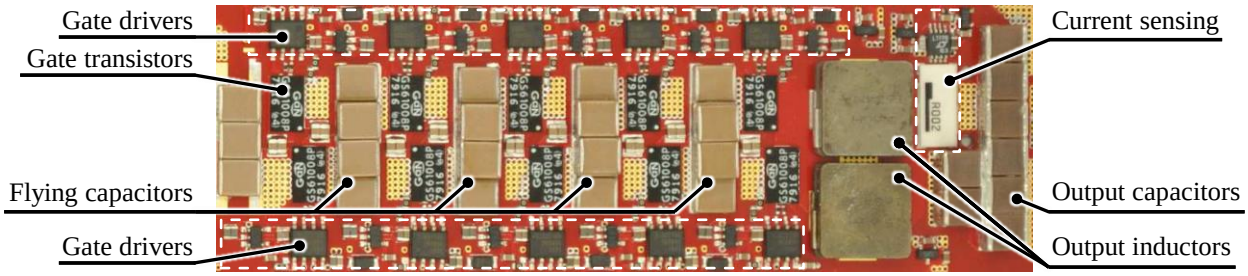


Fig. 9. A picture of the six-level FCML buck stage with annotated key components. (actual size)

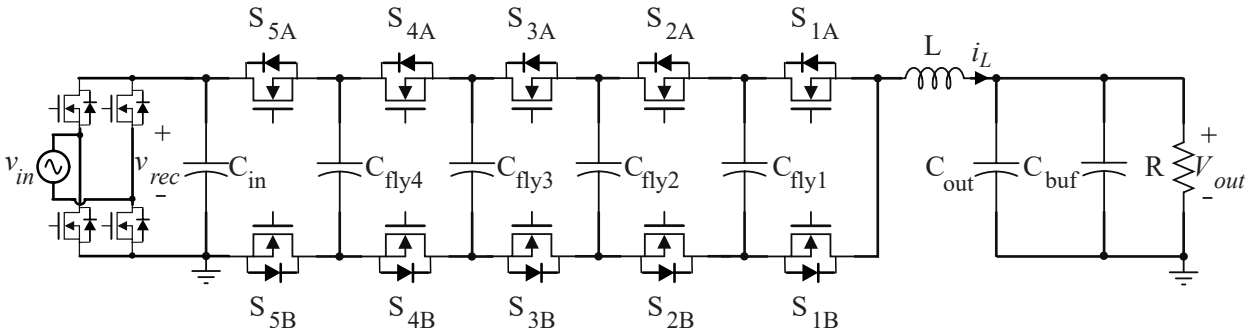


Fig. 10. Six-level FCML buck converter in single phase ac to dc power conversion

power through the input capacitor C_{in} can be expressed as [36]

$$\begin{aligned} P_c(t) &= v_c(t) \cdot i_c(t) = v_c(t) \cdot C \frac{d}{dt} v_c(t) \\ &= \omega C_{in} V_{in,peak}^2 \sin(\omega t) \cos(\omega t) \end{aligned} \tag{11}$$

since the voltage across the input capacitor, C_{in}, is $v_c(t) = v_{in}(t) = V_{in,peak} \sin(\omega t)$. Substituting (2), (3), and (11) into the power equation (10) and solving for the preferred reference output current yields

$$i_{ref}(t) = \begin{cases} \left(K \sin^2(\omega t) \right. \\ \left. - \frac{\omega C_{in} V_{in}^2}{V_{out}} \sin(\omega t) \cos(\omega t) \right), & \text{if } |v_{in}(t)| > v_{out}(t) \\ 0, & \text{otherwise.} \end{cases} \tag{12}$$

The displacement current has a more pronounced effect for larger input voltages and dominates for lighter loads when K is relatively small.

In an FCML converter, the flying capacitors also contribute to the reactive power flow, which is introduces an additional control challenge in buck FCML PFC converters. Moreover, as each capacitor is connected to the input for only brief moments, the effective input capacitance is a function of the number of levels. Here, we derive this for the case of balanced phase-shifted PWM operation (as shown in Fig. 5a). Each averaged flying capacitor voltage can be explicitly described as a proportional scaling of the time-varying rectified ac input voltage v_{rec}(t) or

$$v_{C_{fly,j}}(t) = \frac{j}{N-1} \cdot v_{rec}(t) \qquad \text{for } j = 1, 2, ..., (N-2) \tag{13}$$

The instantaneous power through each flying capacitor, $C_{fly,j}$, can thus be derived as

$$\begin{aligned} P_{C_{fly,j}}(t) &= v_{C_{fly,j}}(t) \cdot i_{C_{fly,j}}(t) \\ &= v_{C_{fly,j}}(t) \cdot C \frac{d}{dt} v_{C_{fly,j}}(t) \\ &= \left(\frac{j}{N-1}\right)^2 \omega C_{fly,j} V_{in,peak}^2 \sin(\omega t)\cos(\omega t) \end{aligned} \tag{14}$$

and the overall capacitive power including the input capacitance is defined as

$$P_c(t) = P_{C_{in}}(t) + \sum_{j=1}^{N-2} P_{C_{fly,j}}(t) \tag{15}$$

For the general N-level FCML case, assuming all flying capacitances are equivalent; substituting (2), (3), and (15) into the power equation (10); and solving for the preferred reference output current yields

$$i_{ref}(t) = \begin{cases} \left(K \sin^2(\omega t) - \frac{\omega C_{in,eff} V_{in}^2}{V_{out}} \right. \\ \left. \sin(\omega t)\cos(\omega t)\right), & \text{if } |v_{in}(t) > v_{out}(t)| \\ 0, & \text{otherwise.} \end{cases} \tag{16}$$

where the effective capacitance $C_{in,eff}$ at the input is

$$C_{in,eff} = C_{in} + C_{fly} \frac{(N-2)(2N-3)}{6(N-1)} \tag{17}$$

If the input current displacement compensation is enabled in the proposed algorithm, (16) is used to calculate the reference current for the current control loop.

IV. Hardware Prototype and Experimental Results

This section provides implementation details of the hardware prototype that is used to validate the proposed control techniques and presents the experimental results.

A. Hardware prototype

The prototype converter, shown in Fig. 8 and Fig. 9, is designed for 240 V_{RMS} input voltage. The number of levels in the FCML buck converter is chosen as six, not only because of prior work [37] which demonstrated that an even number of levels has better natural balancing of the flying capacitor voltages, but also because a six-level design yields 68 V maximum voltage stress at the ac line peak, enabling the use of 100 V semiconductor switches with adequate margin. It should be noted that higher ac input voltage, such as 264 V_{RMS} which may be desired to accommodate universal input voltage range, would reduce this margin. Considering the high output current requirements of buck-type PFC converters, GaN transistors are preferred to achieve high power density and low conduction loss despite the dynamic on-state resistance phenomena present in power GaN transistors [38]. Gate drive circuitry for the floating transistors in the FCML buck converter is energized using a cascaded bootstrap scheme [39]. Additionally, if $C_{in} = C_{fly}$, then $C_{in,eff} = 2.2\ C_{in}$ for a 6-level converter using (17). In this case, the flying capacitors account for more than half of all line frequency displacement current seen at the input if left uncompensated according to (5).

The choice of inductor, flying capacitor, and the switching frequency values are essential for proper operation of the buck FCML converter in an ac-dc application, since they impact the effective time constant of flying capacitor voltage balancing dynamics. As mentioned before, the flying capacitor voltages in ac-dc operation of the FCML buck converter must

TABLE I
KEY COMPONENTS OF THE SIX-LEVEL FCML BUCK STAGE

Component	Manufacturer & Part Number
Transistors	GaN Systems GS61008P
Gate driver	Silicon Labs SI8271GB-IS
C_{fly}	TDK C5750X6S 2.2 μF, 6 in parallel per level
$C_{fly,decoupling}$	TDK C2012X7T 47 nF, 4 in parallel per level
L	Vishay ILHP5050EZER 5.6 μH, 2 in parallel
C_{out}	TDK CGA9N3X7S 10 μF, 16 in parallel
C_{in}	TDK C5750X6S 2.2 μF, 9 in parallel
Microcontroller	Texas Instruments F28377D
Current sensor	Linear Technology LT1999, 50 V/V
Sense resistor	Ohmite FC4L, 2 mΩ

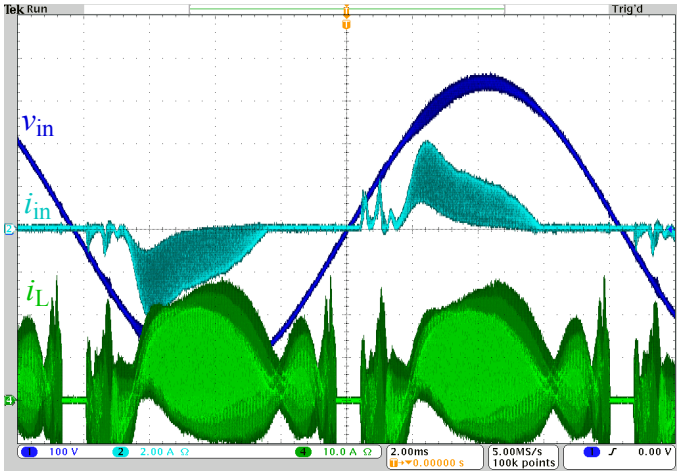
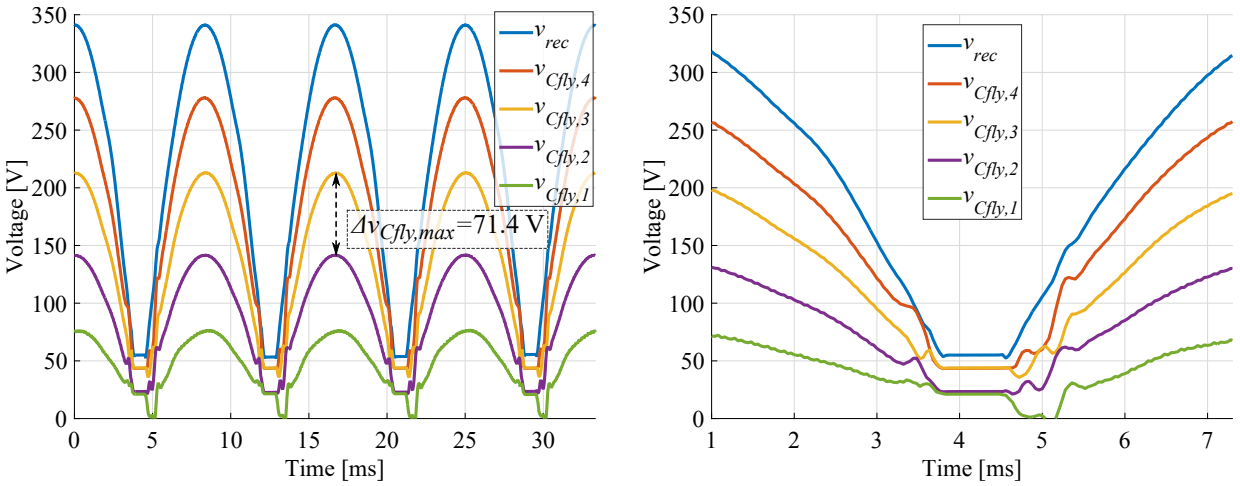


Fig. 11. Input and output voltage, current, and power of the six-level buck converter in PFC operation at 240 V_{RMS} input voltage and 4.5 A output current. Power factor = 0.77



(a) For two ac line cycle

(b) During turn on and off

Fig. 12. Experimentally measured flying capacitor voltages at V_{in} = 240 V_{RMS}.

reasonably follow appropriate fractions of the rectified input voltage which varies at twice-line frequency. Also, since this work pursues natural balancing of the flying capacitor voltages during PFC operation, the flying capacitor voltage dynamics must be much faster than the variation of the rectified input voltage at twice-line frequency. Thus, determination of inductor, flying capacitor and switching frequency values requires careful consideration of natural voltage balancing dynamics. Reference [35] experimentally investigates various L and C_{fly} values at various f_{sw} values for ac-dc PFC application using the six-level hardware prototype, and concludes that L = 2.8 μH, C_{fly} = 13.2 μF (per stage), and f_{sw} = 40 kHz result in sufficiently fast natural balancing dynamics when the rectified input voltage varies at 120 Hz. Select results of this experimental investigation are given in the Appendix. (Interested readers can refer to [35] for complete results). The switching frequency and flying capacitor value (i.e., C_{fly} = 13.2 μF (per stage), and f_{sw} = 40 kHz) limit average output current of the hardware prototype to 4.5 A. Thus, the hardware prototype is rated for 216 W at 48 V output voltage.

A schematic of the hardware prototype is given in Fig. 10. Key components of the FCML buck stage are listed in Table I. Since this work focuses on the PFC front end converter and aims to leverage a 48 V UPS to provide twice-line frequency energy buffering, a large electrolytic capacitor bank (annotated as C_{buf} in Fig. 10) is added to the converter output to mimic 48 V UPS behavior for the experimental work. Impedance looking into the AC power source is 30 uH and 1 ohm.

B. Experimental Results

The experimental setup consists of a programmable ac power supply, a programmable dc electronic load, and a Keysight PA2201A power analyzer. The input voltage and flying capacitor voltages were measured with an NI PXIe-1078 data acquisition unit to record the flying capacitor voltage behavior in PFC operation. The proposed PFC control algorithm is first applied to the six-level FCML buck converter prototype without enabling the input current displacement compensator.

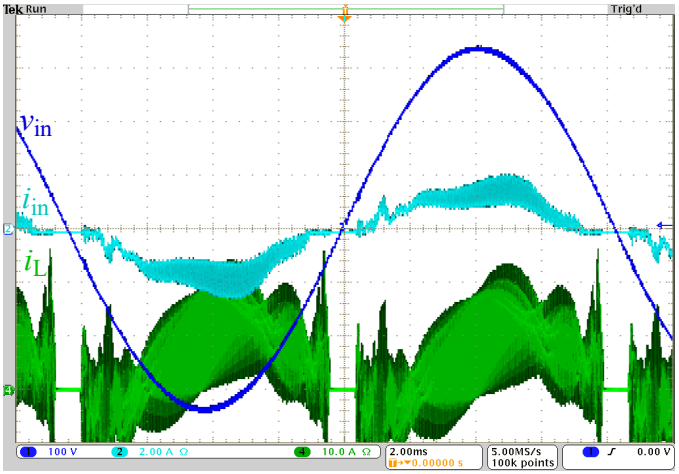
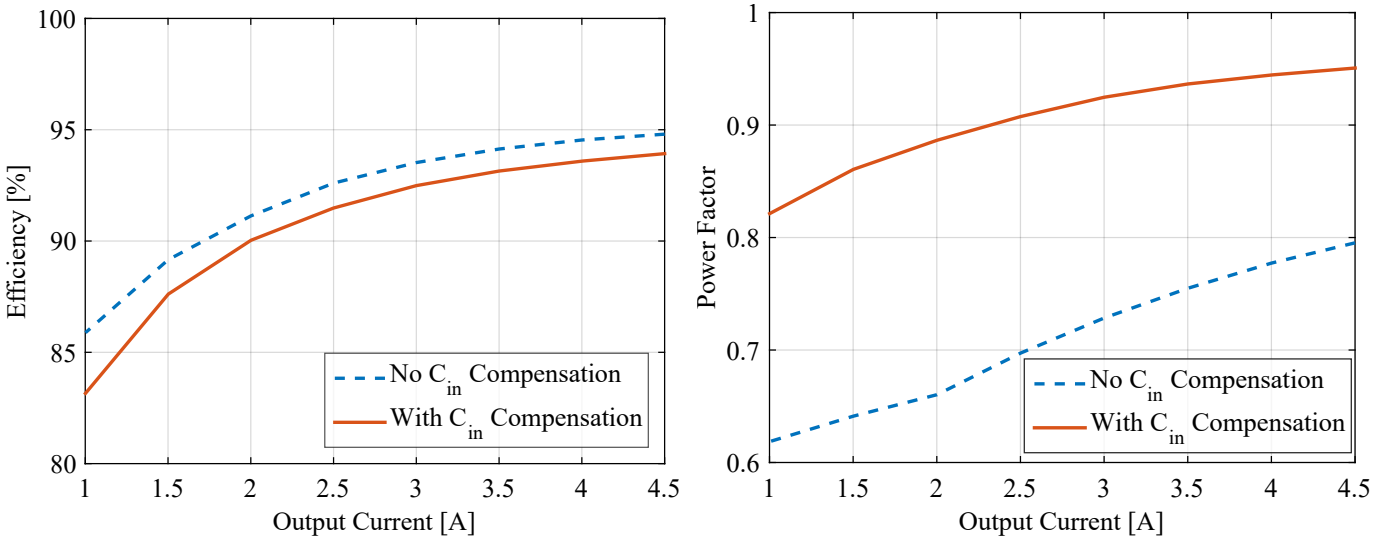


Fig. 13. Input and output voltage, current, and power of the six-level buck converter in PFC operation at 240 V_{RMS} input voltage with C_{in} compensation. Power factor = 0.95.

The input voltage and current, as well as the inductor current, are given in Fig. 11 for 240 V_{RMS} input voltage and rated output current. Flying capacitor voltages at this operating point are given in Fig. 12 for two full ac line cycles and during converter turn on and off.

As shown in Fig. 11, the converter exhibits high inductor and input current ripple which results in weak current shaping performance. As shown in Fig. 12a, where the flying capacitor voltages are given for two full ac line cycles, they are close to their expected values which are specific fractions of the rectified input voltage.

At the converter turn on and off, where the rectified input voltage has the highest $\frac{dv}{dt}$ and the duty ratio change is the fastest across the ac line cycle, flying capacitor voltage balance is not maintained, as can be seen in Fig. 12b. In addition, the poor balance around the converter turn-off results in flying capacitor voltages at uncontrolled levels just before the converter is disabled. This results in a non-ideal initial condition for the flying capacitor voltages at the converter turn-on in the next



(a) AC to dc conversion efficiency vs. output current.

(b) Power factor vs. output current.

Fig. 14. Power factor and efficiency, with and without C_{in} compensation at 240 V_{RMS}.

ac line cycle. Thus, the flying capacitor voltages oscillate after the converter is enabled. Nevertheless, voltage imbalances on flying capacitor voltages around the converter turn-on and turn-off instants do not violate the switch voltage ratings even at rated input voltage. For safe circuit operation (i.e., in order not to violate the voltage rating of the transistors), the flying capacitor voltages must be well-balanced at the input voltage peak, as is the case demonstrated in Fig. 12a. The maximum voltage that a transistor withstands (i.e., the maximum voltage between any two consecutive flying capacitor when the input voltage peaks) is 71.4 V, sufficiently below the rated transistor voltage. For 240 V_{RMS} input voltage, the six-level FCML buck converter and the proposed PFC control without input current displacement compensation achieves 0.77 power factor and 94.80% power conversion efficiency at rated current.

The excessive input current ripple, as shown in Fig. 11, is a major reason for the reduced power factor. As mentioned in Section III-G, to improve the power factor and reduce the input current switching ripple amplitude, C_{in} can be increased and input current displacement compensator can be enabled. Fig. 13 shows input voltage and current as well as the inductor current for 240 V_{RMS} input voltage where C_{in} is 19.8 μF and i_{ref} is phase shifted using the compensation term, given in (16). As can be seen in Fig. 13, the input current is in phase with the input voltage, and input current ripple amplitude is attenuated. Using C_{in} compensation, power factor increases from 0.77 to 0.95 at the rated current. However, the high inductor current ripple due to low switching frequency and the small inductor is still present, as shown in Fig. 11 and Fig. 13. In addition, due to imperfections in flying capacitor voltage balancing, the inductor current ripple is still distorted. These restrain current shaping performance of the proposed PFC control which aims to control the input current through shaping the inductor current as explained in Section III-D. Therefore, although the input current displacement is reduced by using proposed C_{in} compensation method, the input current still exhibits distortion.

According to IEC 61000-3-2 standard, the harmonic current content limits for Class D equipment are defined as a function of active input power with an absolute maximum permissible value [40]. Fig. 15 and Table II show the harmonic current limits defined in IEC 61000-3-2 and the measured harmonic content of the hardware prototype with input current displacement compensation activated. The harmonic content of the theoretical buck-PFC input current, (i.e., the un-rectified version of the input current in Fig. 3) is also shown in Fig. 15 for reference. The experimental results using the six-level flying capacitor buck converter prototype and the proposed PFC control with input current displacement compensation show that all except the 11th harmonic content of the input current meet the IEC 61000-3-2 standard with at least 43.6% margin. The 11th harmonic meets the IEC 61000-3-2 standard with 7% margin.

Fig. 14a and 14b show output current versus measured ac to dc conversion efficiency and power factor, respectively, with and without C_{in} compensation at 240 V_{RMS} input voltage. As shown in Fig. 14a and 14b, C_{in} compensation successfully improves the power factor throughout the load range; although the power factor still decreases as the load decreases due to more pronounced deviation from ideal characteristics of the input and flying capacitors. Also, the efficiency is slightly reduced due to additional reactive power processed by the converter while delivering the same active power to the load.

V. Conclusion

In data center power delivery applications, the ultimate goal is regulating low dc voltage for digital loads; therefore, in this work a six-level FCML buck converter that can provide 48 V directly from 240 V_{RMS} in a single power stage has been introduced. Well-known performance benefits of FCML topology such as leveraging capacitors along with inductors in the energy conversion process and reducing the overall

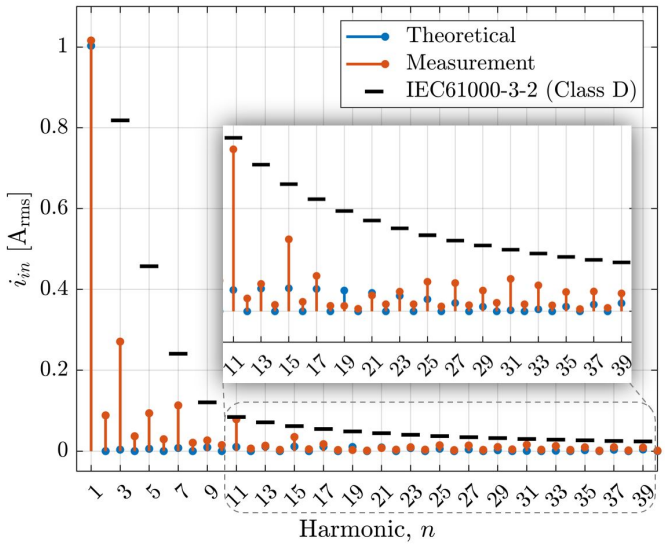


Fig. 15. The theoretical input current harmonic content of an ideal buck-type PFC converter, the measured input current harmonic content of the hardware prototype, and per watt harmonic current limits as defined in IEC 61000-3-2 Standard.

TABLE II
THE MEASURED INPUT CURRENT HARMONIC CONTENT OF THE HARDWARE PROTOTYPE, PER WATT HARMONIC CURRENT LIMITS AS DEFINED IN IEC 61000-3-2 STANDARD, AND MARGIN.

Harmonic	Value [mA/W]	Limits [mA/W]	Margin [%]
3	1.12	3.4	67
5	0.39	1.9	79.6
7	0.47	1	53.2
9	0.11	0.5	78
11	0.33	0.35	7
13	0.06	0.2962	81.4
15	0.14	0.2567	43.6
17	0.07	0.2265	68.5
19	0.01	0.2026	94.5
21	0.03	0.1833	82.5
23	0.04	0.1674	76.4
25	0.06	0.1540	61.4
27	0.06	0.1426	60.1
29	0.04	0.1328	68.5
31	0.07	0.1242	47.4
33	0.05	0.1167	55.2
35	0.04	0.1100	64.6
37	0.04	0.1041	61.6
39	0.04	0.0987	63.5

required inductor size to improve power density are explored in a single phase buck-type PFC application. However, such an implementation of an FCML buck converter in a PFC application introduces a unique operation scenario in which the flying capacitor voltages must follow the input voltage at line frequency proportionally to ensure proper converter operation. A key contribution of this paper is demonstrating the key features of the topology and concept with experimental results. Here, we also provided the design aspects of a six-level FCML buck converter with GaN transistors and the details of a digital control algorithm with an input current displacement compensator to experimentally demonstrate single phase buck-type PFC.

APPENDIX

A. Impact of Flying Capacitor, Inductor and Switching Frequency Values on Natural Balancing of Flying Capacitor Voltages at Twice-Line Frequency

Natural voltage balancing dynamics are analyzed in time domain for a six-level converter in [26]. The analysis and exact results are mathematically complicated. Here, the relationships between component values and operating parameters are provided. A flying capacitor voltage can be summarized by:

$$v_C(t) = v_{C,nom} + g(t)e^{(-t/\tau)}, \tag{18}$$

where $v_{C,nom}$ is the nominal voltage of each flying capacitor (i.e., a fraction of the input voltage), τ is the damping time constant of the flying capacitor voltage dynamics, and $g(t)$ is a function of coupled flying capacitor voltages and oscillatory charge transfers between unbalanced flying capacitors, and is in units of volts [26]. The time constant τ has the following parameter dependencies:

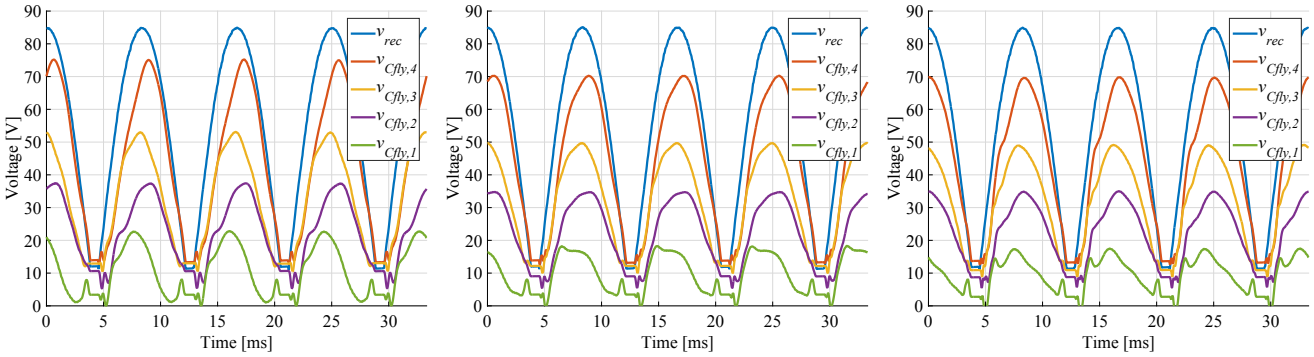
$$\tau \propto L^2, f_{sw}^2, C_{fly}, \frac{1}{R}, h(D), \tag{19}$$

where, L is the inductor value, f_{sw} is the transistor switching frequency, C_{fly} is the flying capacitor value per level, R is the load, and $h(D)$ is a nonlinear function that depends on the duty ratio D [26]. According to (18) the dynamic behavior of the flying capacitor voltages decays with a time constant τ, which is related to circuit parameters by (19). From (18) and (19), the natural balancing is linearly related to C_{fly}, and is quadratically related to L and f_{sw}; additionally, to accelerate the natural balancing, L, C_{fly} and f_{sw} should be reduced. It is acknowledged that (18) and (19) govern flying capacitor voltage dynamics when the input voltage is constant, which is not the case in the ac-dc applications.

In order to experimentally investigate the natural balancing of flying capacitor voltages at a 60 Hz ac input without violating the transistor ratings of the hardware prototype, the input and output voltage are scaled down by four times, to preserve the current conduction angle for PFC operation.

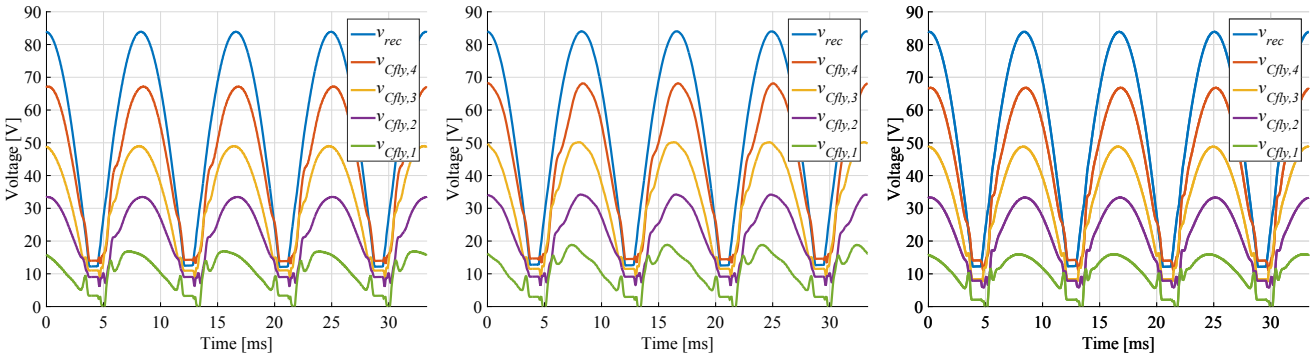
The six-level FCML converter in PFC operation was first tested by keeping L and f_{sw} values constant at 5.6 μH and 80 kHz, respectively, and by changing the flying capacitor values between 4×2.2 μF and 8×2.2 μF. The flying capacitor voltages for selected C_{fly} values are given in Fig. 16. As is apparent in Fig. 16, C_{fly} changes the balancing behavior of flying capacitors as they charge and discharge at twice-line frequency. According to (19), τ should reduce (or the natural balancing should accelerate) as C_{fly} is reduced from 8×2.2 μF to 4×2.2 μF. A visual comparison of Fig. 16 shows that the peak voltages of $C_{fly,1}$ through $C_{fly,4}$ better align with the peak voltage of V_{rec} as C_{fly} reduces.

As mentioned before, C_{fly} is linearly related to τ, while L and f_{sw} are quadratically related. Therefore, further acceleration of natural balancing was investigated by reducing f_{sw} to 40 kHz (i.e., half of the previous switching frequency which should accelerate natural balancing by 4 times) while keeping C_{fly} constant at 6×2.2 μF. The flying capacitor voltages for this test are given in Fig. 17a. As can be seen in



(a) $C_{fly} = 8 \times 2.2\ \mu$F (b) $C_{fly} = 6 \times 2.2\ \mu$F (c) $C_{fly} = 4 \times 2.2\ \mu$F

Fig. 16. Flying capacitor voltages of six-level buck converter in PFC operation for different C_{fly} values. $V_{in} = 60$ V_{RMS}, $V_{out} = 12\ V$, $L = 5.6\ \mu$H, and f_{sw}=80 kHz.



(a) $L = 5.6\ \mu$H, f_{sw} = 40 kHz (b) $L = 2.8\ \mu$H, f_{sw} = 80 kHz (c) $L = 2.8\ \mu$H, f_{sw} = 40 kHz

Fig. 17. Flying capacitor voltages of six-level buck converter in PFC operation for different L and f_{sw} values. $V_{in} = 60$ V_{RMS}, $V_{out} = 12\ V$, and $C_{fly} = 6 \times 2.2\ \mu$F.

Fig. 17a, natural balancing of the flying capacitor voltages was accelerated, yielding better alignment around the input voltage peak compared to the flying capacitor voltages in Fig. 16.

According to (19), natural balancing can also be accelerated by reducing L. The hardware prototype was tested by reducing L to 2.8 μH at a switching frequency of 80 kHz. The flying capacitor voltages for this test are given in Fig. 17b. Following (19), this test should result in flying capacitor voltage behavior similar to the results in Fig. 17a, since the effective τ is the same in both tests. Close examination of Fig. 17a and Fig. 17b shows that this is indeed the case; however, flying capacitor voltages do not follow the rectified input voltage sufficiently close. Therefore, τ was even further reduced by updating the hardware prototype with L = 2.6 μH and f_{sw} = 40 kHz, which represents a factor of 16 reduction compared to Fig. 16b where $C_{fly} = 6 \times 2.2\ \mu$F, L = 5.8 μH and f_{sw} = 80 kHz. The flying capacitor voltages for this test are given in Fig. 17c.

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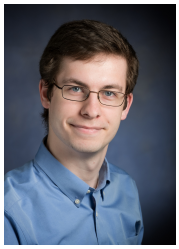

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