UNIVERSITY OF CALIFORNIA SAN DIEGO

# Digital Enhancement Techniques for Digital Fractional-*N* Phase-Locked Loops

A dissertation submitted in partial satisfaction of the requirements for the degree

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in

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by

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The dissertation of Cristián Enrique Álvarez Fontecilla is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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DEDICATION

*To Castor Barracuda.*

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ABSTRACT OF THE DISSERTATION

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by

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Phase-locked loops (PLLs) are critical components in modern electronics communication systems, where they are used to synthesize local oscillator signals for modulation and demodulation in wireless transceivers. They are also used to clock digital-to-analog converters (DACs), analog-to-digital converters (ADCs), and digital processors.

Most PLLs incorporate either analog filters and voltage-controlled oscillators (VCOs) or digital filters and digitally-controlled oscillators (DCOs). The former are called analog PLLs

and the latter are called digital PLLs. To date, analog PLLs have the best phase error performance, but digital PLLs have the lowest circuit area and are more compatible with highly-scaled CMOS integrated circuit (IC) technology. Thus, improving the performance of digital PLLs has been the subject of intensive research for many years.

The first chapter of this dissertation presents a multi-rate dynamic element matching (MR-DEM) technique and an adaptive mismatch-noise cancellation (MNC) technique that work together to mitigate spectral breathing in digital PLLs, a problem caused by mismatches among the frequency control elements (FCEs) within the DCO. It presents a theoretical analysis of the techniques, as well as behavioral simulation results that support the analysis.

The second chapter of this dissertation presents delta-sigma ($\Delta\Sigma$) frequency-to-digital converter (FDC) all-digital enhancements for FDC-based digital fractional-*N* PLLs. It describes an enhanced $\Delta\Sigma$ FDC architecture that has relaxed timing constraints and reduced phase-frequency detector (PFD) output pulse-span compared to prior-art $\Delta\Sigma$ FDCs. It also describes and analyses a $\Delta\Sigma$ FDC forward gain calibration technique that reduces the complexity associated with the system's implementation and improves the phase noise performance of PLLs with high loop bandwidths.

The third chapter of this dissertation presents an integrated circuit high-performance PLL which implements the MR-DEM and MNC techniques presented in the first chapter. It demonstrates the detrimental effects of the spectral breathing phenomenon, as well as the effectiveness of the MR-DEM and MNC techniques to mitigate this problem.

# CHAPTER 1

# MULTI-RATE DEM WITH MISMATCH-NOISE CANCELLATION FOR DCOS IN DIGITAL PLLS

**Abstract**—Mismatches among frequency control elements in digitally-controlled oscillators can be a significant source of phase error in digital phase-locked loops (PLLs). This paper presents a multi-rate dynamic element matching technique and an adaptive mismatch-noise cancellation (MNC) technique that work together to address this problem. The two techniques operate in back-ground during normal PLL operation, and the MNC technique has typical cold start convergence times of a few seconds.

## I. INTRODUCTION

High-performance phase-locked loops (PLLs) are critical components in modern electronic communication systems. For example, in wireless transceivers they generate radio

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frequency local oscillator signals for up-conversion and down-conversion of transmitted and received signals, the phase error of which often limits overall transceiver performance.

Most PLLs incorporate either analog filters and voltage-controlled oscillators (VCOs) or digital filters and digitally-controlled oscillators (DCOs). The former are often called *analog PLLs* and the latter are often called *digital PLLs*. To date, analog PLLs have the best phase error performance, but digital PLLs have the lowest circuit area and are more compatible with highly-scaled CMOS IC technology. Thus, reducing phase error in digital PLLs has been the subject of intensive research and development for over a decade [1-49].

Nevertheless, frequency control element (FCE) mismatches in DCOs remain a significant source of phase error in high-performance digital PLLs [39]. This problem has only been addressed in prior work via an offline calibration technique that requires several minutes to complete [16, 18]. This paper presents a multi-rate dynamic element matching (DEM) technique and an adaptive mismatch-noise cancellation (MNC) technique that work together to address the problem. Both techniques run in background during normal PLL operation, and the MNC technique typically converges in a few seconds from a cold start.

The paper describes the proposed multi-rate DEM and MNC techniques in detail. Section II provides DCO background information. Section III discusses the effects of FCE mismatches on the DCO frequency. Section IV presents an error model for FCE mismatches. Section V presents the multi-rate DEM technique. Section VI presents the MNC technique. Section VII presents behavioral simulation results that support the analysis of the paper. The proposed techniques are described in the context of an example to simplify the explanations.

## II. BACKGROUND INFORMATION

A DCO is an oscillator whose frequency is controlled by one or more FCEs, each of which is controlled by a 1-bit digital sequence. For instance, each FCE in an LC-based DCO contributes to the DCO's tank a capacitance that takes on one of two values depending on the state of the FCE's input bit. Changing the FCE's input bit increases or decreases the DCO frequency by a fixed frequency step.

The instantaneous frequency of a DCO is given by a fixed offset frequency plus $f_{\text{tune}}(t)$, where

$$f_{\text{tune}}(t) = \sum_{i=1}^{N_{\text{FCE}}} f_i(t), \tag{1}$$

$N_{\text{FCE}}$ is the number of FCEs in the DCO, and $f_i(t)$ is the contribution of the $i$th FCE to the DCO frequency. Ideally,

$$f_i(t) = \left(b_i[m_t] - ½\right)\Delta_i, \tag{2}$$

where $b_i[m]$ is the FCE's input bit value (either 0 or 1) over the $m$th clock interval, $m_t = \lfloor f_{\text{FCE}} t \rfloor$, $f_{\text{FCE}}$ is the clock-rate of the input bit, and $\Delta_i$ is the FCE's frequency step size.[2]

The DCO's input sequence, $d[n]$, represents the ideal value of $f_{\text{tune}}(t)$ over the $n$th clock interval. For example, suppose $d[n]$ is represented as a 16-bit two's complement code where the least significant bit (LSB) represents a DCO frequency step of $\Delta$ (e.g., $\Delta$ = 100 Hz). Then

$$d[n] = \left( -2^{15} d_{15}[n] + \sum_{i=0}^{14} 2^i d_i[n] \right) \Delta, \tag{3}$$

[2] By definition, $m_t$ is the largest integer less than or equal to $f_{\text{FCE}}t$ at time $t$, so it is a continuous-time waveform. Hence, $b_i[m_t]$ is a continuous-time waveform even though $b_i[m]$ is a discrete-time sequence.

where $d_i[n]$, for each $i = 0, 1, \ldots, 15$, is the value of the $i$th bit of the code (either 0 or 1) over the $n$th clock interval.

Ideally, $f_{\text{tune}}(t) = d[n_t]$, where $n_t = \lfloor f_{\text{in}} t \rfloor$ and $f_{\text{in}}$ is the clock-rate of the DCO input. Equations (1)-(3) with $f_{\text{FCE}} = f_{\text{in}}$ imply that this can be achieved with a bank of 16 FCEs, where the $i$th FCE's frequency step size is $\Delta_i = 2^{i-1}\Delta$, $b_i[n] = d_{i-1}[n]$ for $i = 1, 2, \ldots, 15$, and $b_{16}[n] = 1 - d_{15}[n]$.

Unfortunately, in PLL applications that require low phase noise, such as local oscillator synthesis for cellular telephone transceivers, DCOs with minimum frequency steps of tens of Hz are required, but most existing FCEs have minimum frequency steps of tens of kHz or more [50, 51]. A common solution to this problem is described below for an example case in which $f_{\text{tune}}(t)$ needs to be controlled in steps of $\Delta$, yet the smallest realizable FCE frequency step size is $\Delta_{\min} = 2^8\Delta$. In this case, the 8 LSBs of $d[n]$ are said to represent the *fractional part* of $d[n]$ because they cause DCO frequency steps that are fractions of $\Delta_{\min}$, and the 8 most significant bits (MSBs) of $d[n]$ are said to represent the *integer part* of $d[n]$ because they cause DCO frequency steps that are multiples of $\Delta_{\min}$.

The idea is to have two FCE banks: an *integer FCE bank* controlled by the integer part of $d[n]$, and a *fractional FCE bank* controlled by the output of an oversampling digital $\Delta\Sigma$ modulator driven by the fractional part of $d[n]$ [2]. The $\Delta\Sigma$ modulator's highpass-shaped quantization noise is lowpass filtered by the DCO, so provided the oversampling rate is sufficiently high, it negligibly contributes to the DCO's phase error.

Fig. 1 shows a specific example in the context of an LC-based DCO, where $p_t = \lfloor f_{\text{fast}} t \rfloor$, $f_{\text{fast}} \gg f_{\text{in}}$, and $d_I[n_t]$ and $d_F[n_t]$ are the integer and fractional parts of $d[n_t]$, respectively. The $f_{\text{fast}}$-

clk signal is such that $p_t$ changes synchronously with $n_t$, so that $n_t$ can be written as a function of $p_t$, i.e.,

$$n_t = g(p_t). \tag{4}$$

In this example $g(p_t) = \lfloor (f_{in}/f_{fast})p_t \rfloor$, where $f_{fast}/f_{in}$ is an integer much greater than 1.

It follows from (3) that $d[n_t] = d_I[n_t] + d_F[n_t]$, where

$$d_I[n_t] = \left( -2^{15} d_{15}[n_t] + \sum_{i=8}^{14} 2^i d_i[n_t] \right) \Delta \tag{5}$$

and

$$d_F[n_t] = \Delta \sum_{i=0}^{7} 2^i d_i[n_t]. \tag{6}$$

As shown in Fig. 1, $d_F[n_t]$ is sampled at a rate of $f_{fast}$ by a second-order digital $\Delta\Sigma$ modulator. The $\Delta\Sigma$ modulator's output is a four-level sequence quantized to multiples of $\Delta_{min}$ and can be written as

$$y_{\Delta\Sigma}[p_t] = d_F[n_t] + e_{\Delta\Sigma}[p_t], \tag{7}$$

where $e_{\Delta\Sigma}[p_t]$ is second-order highpass-shaped quantization noise plus any dither used within the $\Delta\Sigma$ modulator. A thermometer encoder maps $y_{\Delta\Sigma}[p_t]$ to a 4-bit thermometer code which drives a bank of four FCEs, each with a frequency step of $\Delta_{min}$. It follows from (1), (2) and (7) that the contribution of the fractional FCE bank to the DCO frequency, $f_F(t)$, is

$$f_F(t) = \sum_{i=1}^{4} f_i(t) = d_F[n_t] + e_{\Delta\Sigma}[p_t]. \tag{8}$$

The integer FCE bank is directly driven by $d_I[n_t]$. Specifically, the $i$th FCE, for $i = 5, 6, \ldots, 11$, has input $b_i[n_t] = d_{i+3}[n_t]$ and frequency step size $\Delta_i = 2^{i+3}\Delta$, and the 12th FCE has input

$b_{12}[n_t] = 1 - d_{15}[n_t]$ and frequency step size $\Delta_{12} = 2^{15}\Delta$. It follows from (1), (2) and (5) that the contribution of the integer FCE bank to the DCO frequency, $f_I(t)$, is

$$f_I(t) = \sum_{i=5}^{12} f_i(t) = d_I[n_t], \tag{9}$$

where a constant additive term has been omitted.

The contribution of the two FCE banks to the DCO frequency is $f_{\text{tune}}(t) = f_I(t) + f_F(t)$, so (8) and (9) imply that

$$f_{\text{tune}}(t) = d[n_t] + e_{\Delta\Sigma}[p_t]. \tag{10}$$

Accordingly, $e_{\Delta\Sigma}[p_t]$ causes DCO frequency error. The DCO's phase error is the integral of its frequency error, so as mentioned above, a lowpass-filtered version of $e_{\Delta\Sigma}[p_t]$ appears as a component of the DCO's phase error. Given that $e_{\Delta\Sigma}[p_t]$ has a highpass-shaped spectrum that peaks at $f_{\text{fast}}/2$, its contribution to the DCO's phase error can be made negligible relative to other sources of phase error if $f_{\text{fast}}$ is large enough [2, 11, 50].

## III. EFFECTS OF FCE MISMATCHES

The FCEs in the previous example are ideal. Unfortunately, non-ideal circuit behavior causes $f_i(t)$ to deviate from (2). For example, suppose for now that $f_i(t)$ is modeled as ideal except for a static gain error given by $\alpha_i$, i.e.,

$$f_i(t) = \left(b_i[m_t] - ½\right)\alpha_i\Delta_i. \tag{11}$$

Ideally, $\alpha_i = 1$ for $i = 1, 2, ..., N_{\text{FCE}}$, but inevitable component mismatches introduced during fabrication cause $\alpha_i$ to deviate from 1.

Repeating the analysis for the example in Fig. 1 with (11) in place of (2) gives

$$f_{\text{tune}}(t) = \alpha_F \, f_{\text{tune-ideal}}(t) + e_F(t) + e_I(t) + \left(\alpha_I - \alpha_F\right) d_I[n_t], \tag{12}$$

where $f_{\text{tune-ideal}}(t)$ is given by the right side of (10), $\alpha_F$ and $\alpha_I$ are the averages of $\alpha_i$ for $i = 1, 2, 3, 4$ and $i = 5, 6, \ldots, 12$, respectively,

$$e_F(t) = \sum_{i=1}^{4} (\alpha_i - \alpha_F)\left(b_i[p_t] - ½\right)\Delta_{\min} \tag{13}$$

and

$$e_I(t) = \sum_{i=5}^{12} (\alpha_i - \alpha_I)\left(b_i[n_t] - ½\right)\Delta_i. \tag{14}$$

Hence, the FCE static gain errors introduce a gain factor, $\alpha_F$, and three additive error terms to $f_{\text{tune}}(t)$. The $\alpha_F$ gain factor does not significantly degrade performance in typical PLLs. In contrast, as explained next, the three additive error terms in (12) tend to cause spurious tones and increase phase error in PLLs because they are nonlinear functions of $d[n_t]$.

The individual bits of $d[n]$, i.e., $d_i[n]$, for each $i = 0, 1, \ldots, 15$, each depend on $d[n]$ but are restricted to values of 0 and 1. Hence, each $d_i[n]$ is a nonlinear function of $d[n]$. Nevertheless, they can be combined as in (3) to yield $d[n]$, which implies that multiplying $d_0[n]$, $d_1[n]$, …, $d_{14}[n]$, and $d_{15}[n]$ by $2^0$, $2^1$, …, $2^{14}$, and $-2^{15}$, respectively, and adding the results causes the nonlinear components from the individual bits to cancel each other. Any deviation from a set of scale factors proportional to those mentioned above prevents full cancellation of the nonlinear components. It can be verified from (5), (13) and (14) that $e_F(t)$, $e_I(t)$, and $(\alpha_I - \alpha_F)d_I[n_t]$ are each a function of a subset of the individual bits of $d[n_t]$, so they are nonlinear functions of $d[n_t]$.

A partial solution to this problem is to replace the thermometer encoder in Fig. 1 with a mismatch-shaping DEM encoder [52]. Doing so would cause $e_F(t)$ to be replaced by highpass-

shaped noise that is free of nonlinear distortion and is uncorrelated with $d[n_t]$, so it would be suppressed by the DCO like the $\Delta\Sigma$ quantization noise. Similarly, the integer FCE bank could be modified to accommodate a mismatch-shaping DEM encoder clocked at a rate of $f_{\text{in}}$, which would cause $e_I(t)$ to be replaced by shaped noise that is free of nonlinear distortion and is uncorrelated with $d[n_t]$. However, $f_{\text{in}} \ll f_{\text{fast}}$, so less of the shaped noise would be suppressed by the DCO. Unfortunately, DEM as described above would not help prevent the last term in (12) from introducing nonlinear distortion because $d_I[n_t]$ is a non-linear function of $d[n_t]$.

As demonstrated in [39], the last two terms in (12) increase the phase error in a PLL unless $d_I[n_t]$ remains constant once the PLL is locked. In most published digital PLLs $d[n]$ varies by much less than $\Delta_{\text{min}}$ when the PLL is locked, and measured results are usually presented for PLL frequencies at which $d_I[n_t]$ does not change during the measurement interval. This renders the last two terms in (12) constant, so they do not contribute phase error. Unfortunately, this is not a viable option in practice because DCO center frequency drift caused by flicker noise, voltage and temperature variations, and pulling from external interference cause $d[n_t]$ to vary by far more than $\Delta_{\text{min}}$ over time. For instance, measurement results indicate that the frequency of the DCO presented in [39] varies by about −200 kHz/°C, which corresponds to ~$7\Delta_{\text{min}}$ per degree Celsius. In practice, this causes the digital PLL's phase noise to increase drastically from time to time as $d[n_t]$ slowly drifts past integer multiples of $\Delta_{\text{min}}$. This issue is sometimes called "spectral breathing" because the phase noise spectrum, as viewed on laboratory measurement equipment, appears to swell up every now and then as if it is taking deep breaths. During these "breaths" the PLL's performance is extremely degraded. Furthermore, when the PLL is used to generate phase or frequency modulated signals, such as

a GFSK signal for a Bluetooth transmitter, $d[n_t]$ typically varies by more than $\Delta_{\min}$, so there are no periods between "breaths" during which the phase noise performance is good.

To address this problem, a single bank of FCEs driven by a $\Delta\Sigma$ modulator and a mismatch-shaping DEM encoder could be used, where the $\Delta\Sigma$ modulator oversamples $d[n_t]$ instead of just $d_F[n_t]$. The DEM encoder would cause any mismatches among the FCEs to contribute shaped noise instead of nonlinear distortion, and the oversampling would ensure that most of the noise is suppressed by the DCO. Unfortunately, high oversampling ratios would be required in practice, which makes this solution impractical because of the associated high power consumption.

In the remainder of the paper, a new multi-rate DEM technique and an MNC technique that work together within a PLL to solve the problems that arise from FCE mismatches are presented. As in Fig. 1, two FCE banks are used. Both FCE banks are driven by a multi-rate DEM encoder, which ensures that the error arising from FCE mismatches is free of nonlinear distortion. In addition, the multi-rate DEM encoder avoids high power consumption because most of its digital logic is clocked at a rate of $f_{\text{in}}$ instead of $f_{\text{fast}}$.[3] Much of the additive error is not oversampled, so instead of relying on the DCO to suppress it, the MNC technique adaptively measures the error and cancels it in real time.

[3] Although the hardware of the proposed techniques is different from that of the solution in which $d[n_t]$ is oversampled and a DEM encoder clocked at a high rate is used to control the FCEs, a pessimistic power consumption analysis suggests that the proposed techniques are at least five times more power-efficient.

## IV. FCE MISMATCH MODEL

FCEs with $\Delta_i > \Delta_{\min}$ are usually built by connecting nominally identical minimum-weight FCEs in parallel. Static mismatches among these FCEs are sources of error, but other non-idealities such as the non-instantaneous frequency transitions of realizable FCEs are also sources of error. Hence, a more comprehensive model than (11) for $f_i(t)$ is

$$f_i(t) = \left(b_i[m_t] - ½\right)\Delta_i + e_i(t), \tag{15}$$

where $e_i(t)$ is error that models both the static mismatch and the non-ideal frequency transitions of the $i$th FCE. FCEs are designed such that frequency transitions caused by input bit changes settle within a clock period, so $e_i(t)$ only depends on $b_i[m_t - 1]$ and $b_i[m_t]$. This can be modeled as

$$e_i(t) = \begin{cases} e_{11i}, & \text{if } b_i[m_t - 1] = 1,\ b_i[m_t] = 1, \\ e_{01i}(t), & \text{if } b_i[m_t - 1] = 0,\ b_i[m_t] = 1, \\ e_{00i}, & \text{if } b_i[m_t - 1] = 0,\ b_i[m_t] = 0, \\ e_{10i}(t), & \text{if } b_i[m_t - 1] = 1,\ b_i[m_t] = 0, \end{cases} \tag{16}$$

where $e_{11i}$, $e_{01i}(t)$, $e_{00i}$, and $e_{10i}(t)$ represent the error over each clock interval corresponding to the four different possibilities of the FCE's current and prior input bit values [53].[4]

Fig. 2 shows example waveforms associated with (15) and (16). A consequence of the frequency transitions settling within a clock period is that when an FCE's input bit does not change between clock periods, neither does its contribution to the DCO frequency, so $e_{00i}$ and $e_{11i}$ are constant. In contrast, $e_{01i}(t)$ and $e_{10i}(t)$ are not constant because they represent deviations

[4] The FCE model given by (15) and (16) is analogous to that of a non-return-to-zero (NRZ) 1-bit DAC. To prevent $e_i(t)$ from depending on $b_i[m_t - 1]$, return-to-zero (RZ) FCEs could be implemented by setting the FCEs to a signal-independent state for a fraction of each clock period, but this is not practical for PLLs because it would periodically slew the DCO frequency and thereby introduce excessive phase noise.

from the FCE's ideal instantaneous frequency transitions when its input bit changes. As shown in Fig. 2, the shape of each of these frequency transitions depends only on whether the corresponding FCE input changed from 0 to 1 or 1 to 0, and both $e_{01i}(t)$ and $e_{10i}(t)$ are $1/f_{\mathrm{FCE}}$-periodic.

Experimental results suggest, at least for the LC-based DCOs presented in [36] and [39], that the frequency transition introduced by each FCE when its input bit changes from 0 to 1 and that when the input bit changes from 1 to 0 are antisymmetric to a high degree of accuracy, i.e., $e_{11i} - e_{01i}(t) = -[e_{00i} - e_{10i}(t)]$. Therefore, substituting (16) into (15), applying this observation, collecting terms and omitting constant additive terms yields

$$f_i(t) = \left(b_i[m_t] - \tfrac{1}{2}\right)\alpha_i(t)\Delta_i + \left(b_i[m_t - 1] - \tfrac{1}{2}\right)\gamma_i(t), \tag{17}$$

where

$$\alpha_i(t) = 1 + (e_{01i}(t) - e_{00i})/\Delta_i \quad \text{and} \quad \gamma_i(t) = e_{11i} - e_{01i}(t). \tag{18}$$

Given that $\alpha_i(t)$ and $\gamma_i(t)$ are functions of $e_{01i}(t)$ and $e_{10i}(t)$, which are $1/f_{\mathrm{FCE}}$-periodic, they are also $1/f_{\mathrm{FCE}}$-periodic.

## V. MULTI-RATE DEM

### A. Starting Point: Single-Rate Segmented DEM

Suppose the DCO's input sequence is given by (3), and for now suppose that ΔΣ quantization is not necessary because FCEs with small-enough step sizes are available, i.e., $\Delta_{\min} = \Delta$. Even in this case, FCE mismatches are a problem because they cause nonlinear distortion. A conventional single-rate segmented DEM encoder can be used to prevent this problem. For

example, the mismatch-shaping segmented DEM encoder shown in Fig. 3 can be used with 34 FCEs [54]. The $i$th FCE has input $b_i[n_t] = c_i[n_t]$ and frequency step size $\Delta_i = K_i\Delta$, where

$$\begin{aligned} K_{2i-1} &= K_{2i} = 2^{i-1} \quad \text{for } i = 1, 2, \ldots, 13, \text{ and} \\ K_i &= 2^{13} \qquad\qquad\quad \text{for } i = 27, 28, \ldots, 34. \end{aligned} \tag{19}$$

The DEM encoder's input sequence, $c[n_t]$, is obtained from the DCO input sequence as

$$c[n_t] = d[n_t]/\Delta + 2^{15} + 2^{13} - 1 \tag{20}$$

for reasons explained in [54].

As shown in Fig. 3, the DEM encoder consists of 33 digital switching blocks (SBs), labeled $S_{k,r}$ for $k = 1, 2, \ldots, 16$, and $r = 1, 2, \ldots, 17$, configured in a tree structure. The 13 shaded SBs are called segmenting SBs, whereas the other 20 SBs are called non-segmenting SBs. The functional details of the SBs are shown in Fig. 4. The top and bottom outputs of each segmenting SB are $\frac{1}{2}(c_{k,1}[n_t] - 1 - s_{k,1}[n_t])$ and $1 + s_{k,1}[n_t]$, respectively, where $c_{k,1}[n_t]$ is the SB input sequence, and $s_{k,1}[n_t]$, called a switching sequence, is 0 when $c_{k,1}[n_t]$ is odd and ±1 otherwise. Similarly, the top and bottom outputs of each non-segmenting SB are $\frac{1}{2}(c_{k,r}[n_t] - s_{k,r}[n_t])$ and $\frac{1}{2}(c_{k,r}[n_t] + s_{k,r}[n_t])$, respectively, where $c_{k,r}[n_t]$ is the SB input sequence and $s_{k,r}[n_t]$ is 0 when $c_{k,r}[n_t]$ is even and ±1 otherwise.

Regardless of the SB type, each switching sequence is zero-mean and has a first-order highpass-shaped power spectral density (PSD) that peaks at $f_{in}/2$. It is generated in two's complement format by the logic shown in Fig. 4(c), wherein $d_{k,r}[n_t]$ is generated within each SB and is well-modeled as a two-level white random sequence that takes on values of 0 and 1 with equal probability and is independent of the $d_{k,r}[n_t]$ sequences in the other SBs.

B. Extension to Multi-Rate Segmented DEM

Now suppose that the smallest practical FCE frequency step size is $\Delta_{\min} = 2^8\Delta$. As the lower 16 FCEs in the example above all have frequency step sizes smaller than $\Delta_{\min}$, the bottom 16 outputs of the DEM encoder can no longer drive FCEs directly. The multi-rate DEM architecture shown in Fig. 5 addresses this situation, where the bottom 4 FCEs make up the fractional FCE bank, the top 18 FCEs make up the integer FCE bank, and $w_t = p_t - 1$ is a $T_{\text{fast}}$-delayed version of $p_t$, where $T_{\text{fast}} = 1/f_{\text{fast}}$. As in Fig. 1, $n_t = g(p_t)$ changes synchronously with $p_t$.

The block labeled slow DEM encoder in Fig. 5 is a modified version of the DEM encoder in Fig. 3. Its outputs $c_{17}[n_t]$, $c_{18}[n_t]$, …, $c_{34}[n_t]$ are identical to those in Fig. 3, and instead of outputs $c_1[n_t]$, $c_2[n_t]$, …, $c_{16}[n_t]$ it has an output, $x_f[n_t]$, given by

$$x_f[n_t] = \Delta \sum_{i=1}^{16} K_i \left( c_i[n_t] - ½ \right). \tag{21}$$

Each $c_i[n_t]$ takes on values of 0 and 1, so (19) and (21) imply that $|x_f[n_t]| \le 255\Delta$ and $x_f[n_t]$ is restricted to multiples of $\Delta$.

The slow DEM encoder could be implemented from the DEM encoder of Fig. 3 directly by combining $c_1[n_t]$, $c_2[n_t]$, …, $c_{16}[n_t]$ as in (21), but the structure of Fig. 6 is used instead because is simpler. As implied by Fig. 4(b), the sum of the outputs of each non-segmenting SB is equal to the SB's input, so it follows from (21), Fig. 3 and Fig. 4(a) that $x_f[n_t]$ can be computed directly from the bottom outputs of $S_{16,1}$, $S_{15,1}$, …, $S_{9,1}$ as

$$x_f[n_t] = \Delta \sum_{k=9}^{16} 2^{16-k} s_{k,1}[n_t]. \tag{22}$$

Hence, as shown in Fig. 6, $S_{1,1}$, $S_{1,2}$, …, $S_{1,8}$ are not necessary in the slow DEM encoder.

The $\Delta$ scale factor shown in Fig. 6 is not an actual multiplier; it just denotes that the subsequent digital logic should interpret the LSB of $x_f[n_t]$ to represent a DCO frequency step size of $\Delta$.

As shown in Fig. 5, $x_f[n_t]$ is sampled at a rate of $f_{\text{fast}}$ by a second-order digital $\Delta\Sigma$ modulator whose functional diagram is shown in Fig. 7. The dither sequence, $d_{\Delta\Sigma}[p_t]$, is generated such that it can be well-modeled as a two-level white random sequence that is independent of $d[n_t]$ and $x_f[n_t]$ and takes on values of 0 and $\Delta$ with equal probability. It ensures that the $\Delta\Sigma$ modulator's quantization noise is asymptotically independent of $x_f[n_t]$ and $d_{\Delta\Sigma}[p_t]$, and has a PSD equal to that of the output of a filter with transfer function $(1 - z^{-1})^2$ driven by white noise with a variance of $\Delta_{\text{min}}^2/12$ [55]. The $\Delta\Sigma$ modulator output is quantized to values in the set $\{-2\Delta_{\text{min}}, -\Delta_{\text{min}}, 0, \Delta_{\text{min}}, 2\Delta_{\text{min}}\}$ and is given by

$$y_{\Delta\Sigma}[p_t] = x_f[n_t] + e_{\Delta\Sigma}[p_t], \tag{23}$$

where $e_{\Delta\Sigma}[p_t]$ is second-order highpass-shaped quantization noise plus $d_{\Delta\Sigma}[p_t]$.

The block in Fig. 5 labeled fast DEM encoder is a conventional mismatch-shaping non-segmented DEM encoder with a clock rate of $f_{\text{fast}}$. It is implemented as a tree of non-segmenting SBs, and it maps $y_{\Delta\Sigma}[p_t]$ to four 1-bit sequences, each of which drives an FCE with a frequency step size of $\Delta_{\text{min}}$ [56, 57].

Each $b_i[w_t]$ in Fig. 5, for $i = 1, 2, 3, 4$, is clocked at a rate of $f_{\text{fast}}$ and toggles rapidly enough such that the FCE frequency transitions from the fractional FCE bank introduce high-frequency error components to the DCO's phase error. Such components are lowpass filtered by the DCO, so they are not a problem in practice provided $f_{\text{fast}}$ is large enough. Consequently,

the frequency transitions of the FCEs from the fractional FCE bank are modeled as ideal, so that $f_i(t)$ is given by (11) for $i = 1, 2, 3, 4$.

It follows from the results presented in [53] and (11) that

$$f_F(t) = \alpha_F y_{\Delta\Sigma}[w_t] + e_F(t), \tag{24}$$

where $\alpha_F$ is the average of $\alpha_i$ for $i = 1, 2, 3, 4$ and $e_F(t)$ is a function of the errors introduced by the fractional FCE bank and the switching sequences from the fast DEM encoder. The fast DEM encoder ensures that $e_F(t)$ is free of nonlinear distortion, uncorrelated with $y_{\Delta\Sigma}[w_t]$, and has a first-order highpass-shaped PSD that peaks at $f_{\text{fast}}/2$, so this term is not a problem in practice provided $f_{\text{fast}}$ is large enough. Thus, substituting (23) into (24) and neglecting $e_F(t)$ gives

$$f_F(t) = \alpha_F x_f[g(w_t)] + \alpha_F e_{\Delta\Sigma}[w_t]. \tag{25}$$

As shown in Fig. 5, the $c_{17}[n_t]$, $c_{18}[n_t]$, …, $c_{34}[n_t]$ outputs of the slow DEM encoder drive the same FCEs as those of the DEM encoder of Fig. 3. As shown in Appendix A, this implies that $f_I(t)$ is given by

$$f_I(t) = \alpha_I(t) d[g(w_t)] + \gamma_I(t) d[g(w_t - 1)] + e_I(t), \tag{26}$$

where

$$e_I(t) = \Delta \sum_{k,r} \left\{ \alpha_{k,r}(t) s_{k,r}[g(w_t)] + \gamma_{k,r}(t) s_{k,r}[g(w_t - 1)] \right\}, \tag{27}$$

$\alpha_I(t)$, $\gamma_I(t)$, $\alpha_{k,r}(t)$ and $\gamma_{k,r}(t)$ are $T_{\text{fast}}$-periodic waveforms that depend on the errors introduced by the integer FCE bank, and the summation indices indicate the summation over all $k$ and $r$ values corresponding to the SBs within the slow DEM encoder.

The contribution to the DCO frequency from both FCE banks is $f_{\text{tune}}(t) = f_I(t) + f_F(t)$, so (25) and (26) imply that

$$f_{\text{tune}}(t) = \alpha_I(t) d[g(w_t)] + \gamma_I(t) d[g(w_t - 1)] + \alpha_F e_{\Delta\Sigma}[w_t] + e_M(t), \tag{28}$$

where

$$e_M(t) = e_I(t) + \alpha_F x_f[g(w_t)] \tag{29}$$

is called *FCE mismatch error*. As shown below, $e_M(t)$ is a linear combination of the switching sequences from the slow DEM encoder whose coefficients depend on the errors introduced by both FCE banks.

The $\gamma_I(t) d[g(w_t - 1)]$ term in (28) is proportional to a $T_{\text{fast}}$-delayed version of $d[g(w_t)]$, so it represents a linear filtering operation. It follows from the expressions for $\alpha_I(t)$ and $\gamma_I(t)$ in Appendix A that this term tends to be much smaller than the desired signal component, $\alpha_I(t) d[g(w_t)]$, so it is not a problem in practice. The $\alpha_F e_{\Delta\Sigma}[w_t]$ term is proportional to $\Delta\Sigma$ quantization noise plus dither so it is free of nonlinear distortion, is uncorrelated with the other terms in (28), and has a highpass-shaped PSD. The $e_M(t)$ term also has these properties because it is a linear combination of the switching sequences from the slow DEM encoder. The PSD of $\alpha_F e_{\Delta\Sigma}[w_t]$ peaks at $f_{\text{fast}}/2$, whereas the PSD of $e_M(t)$ peaks at $f_{\text{in}}/2$. Hence, $f_{\text{fast}}$ can be increased to make the DCO phase error introduced by $\alpha_F e_{\Delta\Sigma}[w_t]$ negligible, but this would not reduce the DCO phase error contribution from $e_M(t)$. Therefore, $e_M(t)$ is the only problematic term in (28).

Substituting (22) and (27) into (29) yields

$$e_M(t) = \Delta \sum_{k,r} \left\{ \delta_{k,r} s_{k,r}[g(w_t)] + \gamma_{k,r}(t) \left( s_{k,r}[g(w_t - 1)] - s_{k,r}[g(w_t)] \right) \right\}, \tag{30}$$

where

$$\delta_{k,r} = \begin{cases} \alpha_{k,r}(t) + \gamma_{k,r}(t) + \alpha_F 2^{16-k}, & \text{if } k \geq 9, r = 1, \\ \alpha_{k,r}(t) + \gamma_{k,r}(t), & \text{otherwise,} \end{cases} \tag{31}$$

is constant for each $k$ and $r$, even though neither $\alpha_{k,r}(t)$ nor $\gamma_{k,r}(t)$ are constant. As can be verified by substituting (18) into the expressions for $\alpha_{k,r}(t)$ and $\gamma_{k,r}(t)$ in Appendix A, the non-constant terms in each $\alpha_{k,r}(t)$ are equal in magnitude but opposite in sign to the corresponding terms in $\gamma_{k,r}(t)$, so $\alpha_{k,r}(t) + \gamma_{k,r}(t)$, and hence $\delta_{k,r}$, are constant. Therefore, the terms proportional to $\delta_{k,r}$ in (30) represent the DCO frequency error contribution from FCE static gain errors, whereas the terms proportional to $\gamma_{k,r}(t)$ in (30) represent the DCO frequency error contribution from non-ideal FCE frequency transitions.

## VI. ADAPTIVE FCE MISMATCH NOISE CANCELLATION

The purpose of the MNC technique is to cancel most of the DCO phase error that would otherwise be caused by $e_M(t)$. To do this, the sequence

$$e_{\mathrm{MNC}}[p_t] = \Delta \sum_{k,r} \left\{ a_{k,r} s_{k,r}[n_t] + b_{k,r} \left( s_{k,r}[g(w_t)] - s_{k,r}[n_t] \right) \right\}, \tag{32}$$

where $a_{k,r}$ and $b_{k,r}$ are called the MNC coefficients, is injected into the fractional path of the multi-rate DEM encoder. The ideal MNC coefficient values, i.e., the values of $a_{k,r}$ and $b_{k,r}$ for which the DCO phase error contribution of $e_M(t)$ is minimized, are estimated with a least-mean-square (LMS)-like algorithm.

In the following, it is explained how $e_{\mathrm{MNC}}[p_t]$ affects the DCO's phase error, how the FCE mismatch error is measured, and how the MNC coefficients are adaptively computed from the FCE mismatch error measurement.

### A. MNC Sequence Application

Fig. 8 shows the fractional path of the multi-rate DEM encoder shown in Fig. 5 modified

to accommodate MNC. The $e_{\text{MNC}}[p_t]$ sequence is subtracted from $x_f[n_t]$ prior to the ΔΣ modulator, and the output range of the ΔΣ modulator, the range of the fast DEM encoder, and the number of FCEs driven by the fast DEM encoder are all four times those of the original system to accommodate the resulting dynamic range increase. Thus, $f_F(t)$ is still given by (24), but now $y_{\Delta\Sigma}[p_t]$ is given by the right side of (23) minus $e_{\text{MNC}}[p_t]$. Despite having the same qualitative properties as before, $\alpha_F$ and $e_F(t)$ in (24) are slightly different in the modified system because of the additional FCEs.

An analysis almost identical to that presented in Section V shows that $f_{\text{tune}}(t)$ is now given by

$$f_{\text{tune}}(t) = \alpha_I(t)d[g(w_t)] + \gamma_I(t)d[g(w_t - 1)] + \alpha_F e_{\Delta\Sigma}[w_t] + e_R(t), \tag{33}$$

where

$$e_R(t) = e_M(t) - \alpha_F e_{\text{MNC}}[w_t] \tag{34}$$

is the *residual* FCE mismatch error, i.e., what is left of $e_M(t)$ when $e_{\text{MNC}}[p_t]$ is applied. It follows from (30), (32) and (34) that

$$e_R(t) = \Delta\sum_{k,r}\left\{\delta_{k,r\text{-res}}s_{k,r}[g(w_t)] + \gamma_{k,r\text{-res}}(t)\left(s_{k,r}[g(w_t - 1)] - s_{k,r}[g(w_t)]\right)\right\}, \tag{35}$$

where $\delta_{k,r\text{-res}}$ and $\gamma_{k,r\text{-res}}(t)$ are defined as

$$\delta_{k,r\text{-res}} = \delta_{k,r} - \alpha_F a_{k,r} \text{ and } \gamma_{k,r\text{-res}}(t) = \gamma_{k,r}(t) - \alpha_F b_{k,r}, \tag{36}$$

respectively.

Given that $\delta_{k,r}$ is constant, there exists an $a_{k,r}$ that causes $\delta_{k,r\text{-res}} = 0$. In contrast, there is no $b_{k,r}$ that causes $\gamma_{k,r\text{-res}}(t)$ to vanish completely, because $\gamma_{k,r}(t)$ is not constant. However, $\gamma_{k,r}(t)$ is $T_{\text{fast}}$-

periodic so there exists a $b_{k,r}$ that makes the DC component of $\gamma_{k,r\text{-res}}(t)$ zero, such that $\gamma_{k,r\text{-res}}(t)$ is a linear combination of sinusoids with frequencies that are non-zero multiples of $f_{\text{fast}}$ [58]. Therefore, it follows from (36) that if

$$a_{k,r} = \frac{\delta_{k,r}}{\alpha_F} \text{ and } b_{k,r} = \frac{1}{\alpha_F T_{\text{fast}}} \int_0^{T_{\text{fast}}} \gamma_{k,r}(\tau) d\tau, \tag{37}$$

for each $k$ and $r$, then

$$\delta_{k,r\text{-res}} = 0 \text{ and } \int_0^{T_{\text{fast}}} \gamma_{k,r\text{-res}}(\tau) d\tau = 0. \tag{38}$$

In the absence of FCE static mismatches, $a_{k,r} = 0$, and if the FCE frequency transitions are ideal, $b_{k,r} = 0$.

Phase error is the integral of frequency error, so the DCO phase error introduced by $e_R(t)$ is given by

$$\theta_R(t) = \int_0^t e_R(\tau) d\tau. \tag{39}$$

If (38) is satisfied, then (35) and (39) imply that

$$\theta_R(t) = \Delta \sum_{k,r} \left( s_{k,r}[g(w_t - 1)] - s_{k,r}[g(w_t)] \right) \int_0^{t - p_t T_{\text{fast}}} \gamma_{k,r\text{-res}}(u) du, \tag{40}$$

where $t - p_t T_{\text{fast}} = t - \lfloor f_{\text{fast}} t \rfloor T_{\text{fast}} < T_{\text{fast}}$. The term within the parenthesis in (40) equals zero when $g(w_t) - g(w_t - 1) = 0$ and $s_{k,r}[g(w_t) - 1] - s_{k,r}[g(w_t)]$ otherwise. Given that $g(w_t) - g(w_t - 1)$ can only take on values from the set $\{0, 1\}$, then

$$\begin{aligned} &s_{k,r}[g(w_t - 1)] - s_{k,r}[g(w_t)] = \\ &\qquad \left( g(w_t) - g(w_t - 1) \right) \left( s_{k,r}[g(w_t) - 1] - s_{k,r}[g(w_t)] \right). \end{aligned} \tag{41}$$

Furthermore, $g(w_t)$ is a $T_{\text{fast}}$-delayed version of $n_t$, which increases by one unit every $T_{\text{in}} = 1/f_{\text{in}}$, so

$g(w_t) - g(w_t - 1)$ is $T_{\text{in}}$-periodic and is given by

$$g(w_t) - g(w_t - 1) = \sum_{k=-\infty}^{\infty} r\left(t - kT_{\text{in}}\right), \tag{42}$$

where $r(t) = 1$ for $t \in [T_{\text{fast}}, 2T_{\text{fast}})$ and 0 otherwise. It follows from (42) that the Fourier expansion of $g(w_t) - g(w_t - 1)$ is

$$\frac{f_{\text{in}}}{f_{\text{fast}}} + \sum_{m=1}^{\infty} \frac{2}{m\pi} \sin\left(m\pi \frac{f_{\text{in}}}{f_{\text{fast}}}\right) \cos\left(2\pi m f_{\text{in}} \left[t - \frac{3}{2} T_{\text{fast}}\right]\right). \tag{43}$$

Thus, if the conditions shown in (38) are satisfied, (40), (41) and (43) imply that $\theta_R(t)$ would be given by second-order shaped noise multiplied by a $T_{\text{in}}$-periodic waveform and a DC-free $T_{\text{fast}}$-periodic waveform. Consequently, $e_R(t)$ would introduce components with frequencies around $f_{n,m} = nf_{\text{fast}} \pm mf_{\text{in}}$ to the DCO's phase error, where $n = 1, 2, 3, \ldots$ and $m = 0, 1, 2, \ldots$. It follows from (43) that the power of the components around frequencies $f_{n,m}$ with $m$ near multiples of $f_{\text{fast}}/f_{\text{in}}$ is very low. Therefore, $\theta_R(t)$ would not be a problem if $f_{\text{fast}}$ is large enough because $e_R(t)$ would only introduce high-frequency components to the DCO's phase error that would be lowpass filtered by the DCO. Simulation results also suggest that $\theta_R(t)$ is not a problem provided the conditions shown in (38) are satisfied and $f_{\text{fast}}$ is large enough.

B. FCE Mismatch Error Measurement

The ideal MNC coefficient values are estimated as part of the feedback loop in a digital fractional-$N$ PLL that incorporates the DCO. This is done during the PLL's normal operation by adaptively adjusting $a_{k,r}$ and $b_{k,r}$ such that the conditions shown in (38) are satisfied for each $k$ and $r$, thereby minimizing $e_R(t)$.

The purpose of a fractional-$N$ PLL is to generate a periodic output signal, $v_{\text{PLL}}(t)$, with

frequency $f_{\text{PLL}} = (N + \alpha)f_{\text{ref}}$, where $N$ is a positive integer, $\alpha$ is a fractional value and $f_{\text{ref}}$ is the frequency of a reference oscillator waveform, $v_{\text{ref}}(t)$. The general form of a digital fractional-$N$ PLL without MNC is shown in Fig. 9. It consists of a phase-error-to-digital converter (PEDC), a lowpass digital loop filter (DLF), and a DCO. The PEDC's output is an $f_{\text{ref}}$-rate digital sequence of the form

$$p[n] = -\theta_{\text{PLL}}[n] + e_p[n], \tag{44}$$

where $\theta_{\text{PLL}}[n]$ is an estimate of the PLL's phase error and $e_p[n]$ is additive error that includes quantization error from the PEDC's digitization process as well as error from circuit noise and other non-ideal circuit behavior in both the PEDC and reference oscillator.

Suppose the DCO contains the multi-rate DEM structure shown in Fig. 5 modified as shown in Fig. 8 with $f_{\text{in}} = f_{\text{ref}}$. Typically, $f_{\text{fast}}$-clk is a divided-down version of $v_{\text{PLL}}(t)$. Given that $f_{\text{PLL}} = (N + \alpha)f_{\text{ref}}$, $f_{\text{ref}}$ and $f_{\text{fast}}$ are incommensurate frequencies when $\alpha \neq 0$, so it is not possible for $n_t$ to change synchronously with $p_t = \lfloor f_{\text{fast}} t \rfloor$ if $n_t = \lfloor f_{\text{ref}} t \rfloor$. Therefore, as shown in Fig. 10, in practice the DCO input is synchronized to $f_{\text{fast}}$-clk so (4) is satisfied, i.e., so $n_t$ only changes at times $\mu_n$, which are multiples of $T_{\text{fast}}$, instead of times $nT_{\text{ref}}$, where $T_{\text{ref}} = 1/f_{\text{ref}}$ is the reference period. It is common practice in digital PLLs to synchronize the DLF output to the clock signal of the fractional path, so this is not a special requirement of the proposed system. A circuit to avoid metastability issues is also needed as part of the synchronization circuit shown in Fig. 10(a), but it has been omitted for simplicity [59].

A key requirement of a PLL is to suppress low-frequency DCO error, which is achieved by subjecting additive frequency error introduced by the DCO to a highpass filter that has at least one zero at DC. In the following, the impulse response of this filter is denoted as $h[n]$, and its

running sum, i.e., $h[0] + h[1] + \ldots + h[n]$, is denoted as $l[n]$.

As shown in Appendix B, $p[n]$ can be written as

$$p[n] = p_{\text{ideal}}[n] + p_R[n], \tag{45}$$

where $p_{\text{ideal}}[n]$ represents the contribution to $p[n]$ of all noise sources except FCE mismatches and $p_R[n]$ is the contribution to $p[n]$ from $e_R(t)$. Specifically, $p_R[n]$ is given by

$$p_R[n] = \Delta\alpha_F T_{\text{fast}} \sum_{i=0}^{n-1} \sum_{k,r} \left\{ y_{k,r\text{-}a}[i] + y_{k,r\text{-}b}[i] \right\} l[n-1-i], \tag{46}$$

where $y_{k,r\text{-}a}[i] + y_{k,r\text{-}b}[i]$ is proportional to the PLL's frequency error introduced by the $s_{k,r}[n]$ sequences. As explained in Appendix B, if $a_{k,r}$ and $b_{k,r}$ in (32) are replaced by $a_{k,r}[n_t]$ and $b_{k,r}[n_t]$, respectively, then

$$y_{k,r\text{-}a}[i] = \left(q_{i-1} - 3\right) s_{k,r}[i-1] a_{k,r\text{-error}}[i-1] + 3 s_{k,r}[i] a_{k,r\text{-error}}[i] \tag{47}$$

and

$$y_{k,r\text{-}b}[i] = \left(s_{k,r}[i-1] - s_{k,r}[i]\right) b_{k,r\text{-error}}[i], \tag{48}$$

where $q_{i-1}$ is the number of $T_{\text{fast}}$ periods between times $\mu_{i-1}$ and $\mu_i$, and

$$a_{k,r\text{-error}}[n] = a_{k,r}[n] - a_{k,r} \text{ and } b_{k,r\text{-error}}[n] = b_{k,r}[n] - b_{k,r} \tag{49}$$

are the MNC coefficient errors at sample time $n$.

The term proportional to $s_{k,r}[i]$ in (47) arises because the time at which the PEDC samples the PLL's phase error, which is given by $\mu_n + 4T_{\text{fast}}$ in the design example, is not equal to the time at which the integer FCE bank's inputs are updated, i.e., $\mu_n + T_{\text{fast}}$. Accordingly, the integer FCE bank's inputs are updated three $T_{\text{fast}}$ before the PLL's phase error is sampled, which causes $y_{k,r\text{-}}$

$_a[i]$ to depend on $s_{k,r}[i-1]$ and also on $s_{k,r}[i]$.

As implied by (45)-(48), the PEDC's output has information regarding the MNC coefficient errors. The MNC coefficient estimation process described next is based on this result and on the properties of the switching sequences.

C. MNC Coefficients Estimation

A digital fractional-*N* PLL with the multi-rate DEM encoder and MNC technique is shown in Fig. 11(a). The details of the MNC logic are shown in Fig. 11(b) and Fig. 11(c), wherein

$$t_{k,r}[n] = \sum_{i=0}^{n} s_{k,r}[i] \tag{50}$$

is the running sum of $s_{k,r}[n]$, and $K_a$ and $K_b$ are called the MNC gains. The MNC logic block consists of an adder and 25 $s_{k,r}[n_t]$ residue estimators.

It follows from Fig. 4 that each $s_{k,r}[n]$ sequence is a concatenation of sequences of the form $1, 0, \ldots, 0, -1, 0, \ldots, 0$ or $-1, 0, \ldots, 0, 1, 0, \ldots, 0$, where each 0 is present only when the input of the $s_{k,r}[n]$ generator is zero [52]. Thus, $|s_{k,r}[n]| \le 1$, $|t_{k,r}[n]| \le 1$ and $|s_{k,r}[n] - s_{k,r}[n-1]| \le 2$ for all *n*, so the multipliers in Fig. 11(c) are simple in terms of hardware.

The $s_{k,r}[n_t]$ residue estimators are responsible for the computation of the MNC coefficients. At each sample time, the MNC coefficient errors are measured and $a_{k,r}[n_t]$ and $b_{k,r}[n_t]$ are updated such that they approach the values shown in (37). The measurement of the MNC coefficient errors is based on the statistical properties of the switching sequences [60].

As explained in [57] and can be verified from Fig. 4, although each $s_{k,r}[n]$ sequence depends on the input of its corresponding SB, when it is non-zero, its sign depends on $d_{k,r}[n]$. Given that the $d_{k,r}[n]$ sequences are independent of the $d_{k,r}[n]$ sequences in the other SBs, this

provides enough randomization for the $s_{k,r}[n]$ sequences to be uncorrelated with each other. Furthermore, as the $d_{k,r}[n]$ sequences are also independent of all electronic device noise sources in the PLL, each $s_{k,r}[n]$ sequence is uncorrelated with all such sources as well, and it is also uncorrelated with the PEDC's quantization noise in PLLs where such noise source is uncorrelated with the PLL's phase error [29, 39]. Hence, in such cases, the $s_{k,r}[n]$ sequences are uncorrelated with all PLL noise except the terms in $p[n]$ arising from $e_R(t)$, i.e., $p_R[n]$.

As explained above, the $y_{k,r\text{-}a}[i]$ and $y_{k,r\text{-}b}[i]$ terms in $p[n]$ depend on the MNC coefficient errors, and such terms are proportional to functions of the $s_{k,r}[n]$ sequences. Specifically, it can be seen from (45)-(48) that $p[n]$ has information about an accumulated version of

$$\left(q_{n-2}-3\right)s_{k,r}[n-2]a_{k,r\text{-error}}[n-2], \tag{51}$$

and that $p[n]-p[n-1]$ has information about

$$\left(s_{k,r}[n-2]-s_{k,r}[n-1]\right)b_{k,r\text{-error}}[n-1]. \tag{52}$$

Therefore, it follows that the accumulator inputs in Fig. 11(c), i.e., $-p[n]t_{k,r}[n-2]$ and $(p[n-1]-p[n])(s_{k,r}[n-2]-s_{k,r}[n-1])$, when non-zero, are noisy estimates of $a_{k,r\text{-error}}[n]$ and $b_{k,r\text{-error}}[n]$, respectively, so they can be used to adaptively compute the ideal MNC coefficients. In practice, the top and bottom branches within each $s_{k,r}[n_t]$ residue estimator interfere with each other in a way that makes the accumulator inputs have information about both MNC coefficient errors. However, extensive simulations run by the authors suggest that the MNC coefficient values converge to their ideal values regardless of such interferences provided the MNC gains are set properly.

It would also be possible to correlate $p[n-1]-p[n]$ by $s_{k,r}[n-2]$ to get an estimate of $a_{k,r\text{-error}}[n]$. However, as $a_{k,r}[n]$ is only updated when the accumulator input is non-zero, correlating

$p[n-1]-p[n]$ against $s_{k,r}[n-2]$ instead of $-p[n]$ against $t_{k,r}[n-2]$ would significantly decrease the convergence speed of $a_{k,r}[n]$ because normally $s_{k,r}[n-2]$ is zero more often than $t_{k,r}[n-2]$. Although correlating $-p[n]$ against $t_{k,r}[n-2]$ effectively increases the error variance of $a_{k,r}[n]$, as explained next, this problem can be mitigated by reducing $K_a$.

As is common in most LMS-like algorithms, the choice of $K_a$ and $K_b$ represents a tradeoff. The larger the MNC gains, the faster the convergence, but the larger the error variance of $a_{k,r}[n]$ and $b_{k,r}[n]$. Also, as the $s_{k,r}[n_t]$ residue estimators comprise two LMS-like loops in parallel that interfere with each other, $K_a$ and $K_b$ each affect the convergence time and error variance of both $a_{k,r}[n]$ and $b_{k,r}[n]$. Although it might be possible to develop closed-form expressions that quantify these tradeoffs, the authors currently use simulations to assist the design process and to choose the values of $K_a$ and $K_b$.

## VII. SIMULATION RESULTS

The multi-rate DEM and the MNC techniques were tested in an event-driven behavioral simulation of a modified version of the ΔΣ frequency-to-digital converter based fractional-$N$ PLL presented in [39, 40]. As explained in [38], $p[n]$ is given by (44) where $e_p[n]$ is first-order shaped quantization noise that is uncorrelated with the PLL's phase error plus error from both the PEDC and reference oscillator.

The DLF consists of two single-pole IIR stages and a proportional-integral stage. Its transfer function is

$$L(z)=K_M\left(K_P+\frac{K_I}{1-z^{-1}}\right)\prod_{i=0}^{1}\frac{\lambda_i}{1-\left(1-\lambda_i\right)z^{-1}}, \tag{53}$$

where $K_M$, $K_P$, $K_I$, $\lambda_0$ and $\lambda_1$ are constant loop filter parameters. The DCO consists of an LC oscillator core with a power-of-two-weighted coarse capacitor bank, an integer FCE bank and a fractional FCE bank. The latter two are driven by the multi-rate DEM encoder shown in Fig. 5 and modified as shown in Fig. 8 with $f_{fast} = f_{PLL}/8$ and $\Delta_{min} = 40$ kHz (i.e., $\Delta = 156.25$ Hz).

The static gain error of the $i$th FCE was modeled as an additive zero-mean Gaussian random variable with a standard deviation of 5% of $\Delta_i$ divided by the square root of $\Delta_i/\Delta_{min}$, which is consistent with measurement results obtained by the authors from the PLL IC presented in [36]. The FCE frequency transitions were modeled as second-order transients that settle within one $T_{fast}$ period. The parameters of these transients, such as the damping factor and the natural frequency, are modelled as random variables with means and standard deviations determined from transistor-level simulation results. Fig. 12 shows example frequency transients used in the simulation.

The simulated noise parameters of the DCO and the reference oscillator, as well as the PEDC internal parameters, are the same as those used in [38]. Specifically, $f_{ref} = 26$ MHz, $N = 134$ and $\alpha = 0.0003846153$, so that $f_{PLL} = 3.484$ GHz and $f_{fast} = 435.5$ MHz. The DLF parameters used were $K_M = 1.25$, $K_P = 2^4$, $K_I = 2^{-4}$, $\lambda_0 = 2^{-3}$ and $\lambda_1 = 2^{-2}$, and the MNC gains were set to $K_a = 2^{-3}$ and $K_b = 2^{-5}$. The simulated PLL has a bandwidth of 206 kHz and a phase margin of 63 degrees.

Fig. 13(a) shows the simulated PLL phase noise PSD with the multi-rate DEM technique disabled, i.e., with the flip-flops in both the slow and fast DEM encoders frozen. The two curves in Fig. 13(a) were obtained from two different simulations: one in which $d_I[n_t]$ is constant and another one in which $d_I[n_t]$ changes frequently. As mentioned in Section III, although the DCO

input sequence does not vary significantly in the short term once the PLL is locked, its moving average drifts over time such that $d_l[n_t]$ eventually begins to change frequently, at which point it degrades the PLL's phase noise as shown in Fig. 13(a). Once the multi-rate DEM technique is enabled, whether or not $d_l[n_t]$ changes has no significant effect on the DCO's frequency, so spectral breathing no longer occurs.

Fig. 13(b) shows the simulated PLL phase noise PSD with the multi-rate DEM technique enabled for two cases: one case with just static gain errors, and the other case with just non-ideal frequency transitions. Fig. 13(c) shows the simulated PLL phase noise PSD considering both sources of error with the multi-rate DEM technique enabled and with the MNC technique disabled and enabled. The theoretical PLL phase noise PSD for ideal FCEs, which was computed using the linearized model presented in [38], is also plotted as the dashed curves in Fig. 13 to provide a comparison baseline.

As shown in Fig. 13(c), when the MNC technique is enabled the resulting phase noise PSD matches the theoretically-predicted phase noise PSD for ideal FCEs after $13 \cdot 10^7$ reference periods (5 seconds) from a cold start. This implies a phase noise improvement of more than 20 dB at an offset frequency around 10 MHz. As the FCE mismatches are mostly determined by circuit component mismatches, they are not expected to change significantly over time. Hence, once obtained, the MNC coefficients can be stored in memory and used subsequently by the PLL, thereby avoiding future convergence time delays.

Fig. 14 shows the evolution of the MNC coefficient errors over time from the simulation used to generate the curves in Fig. 13(c). As shown in Fig. 14, some $b_{k,r}[n]$ coefficients initially move away from their ideal values. As explained above, this happens because the top and

bottom branches of each $s_{k,r}[n_t]$ residue estimator interfere with each other so that the error estimate at the input of each accumulator is biased by the MNC coefficient error of the opposite branch. As suggested by Fig. 14, if the MNC gains are set properly, this is not a problem in practice because this effect becomes less significant as either one or both MNC coefficients approach their ideal values.[5]

It follows from (47) and (48) that the terms proportional to $a_{k,r\text{-error}}[n]$ in $p[n]$ are $q_n - 3$ times larger than those proportional to $b_{k,r\text{-error}}[n]$ (e.g., $q_n \cong 16$ in the design example), so for $K_a = K_b$, the error variance of each $b_{k,r}[n]$ is expected to be larger than that of $a_{k,r}[n]$. Therefore, in order to make the error variance of the $b_{k,r}[n]$ coefficients comparable to that of the $a_{k,r}[n]$ coefficients, $K_b$ has to be smaller than $K_a$. As shown in Fig. 14, this causes the $b_{k,r}[n]$ coefficients to converge to their ideal values at a slower rate than the $a_{k,r}[n]$ coefficients, so the convergence speed of the MNC technique is limited by $K_b$. Nonetheless, it follows from Fig. 14 that the $a_{k,r}[n]$ coefficients get close to their ideal values in less than $10^7$ reference periods (~0.4 seconds). Hence, as the most significant sources of phase noise are the FCE static gain errors, the MNC technique allows for a considerable phase noise improvement in less than half a second.

To reduce the cold-start convergence time of the MNC technique, large MNC gains can be used initially and decreased over time [61]. Fig. 15 shows the evolution of the MNC coefficient errors over time for $7.8 \cdot 10^7$ reference periods (3 seconds) for an example case in which $K_a$ and $K_b$ are initially set to $2^{-1}$ and $2^{-2}$, respectively, and then divided by two at the

[5] Furthermore, extensive simulations run by the authors in which $p[n]$ was subjected to pessimistic nonlinearities suggest that the convergence of the MNC coefficients is barely affected by nonlinearities in the PEDC.

times indicated by the vertical dashed lines. In this case, the MNC coefficients reach the final values shown in Fig. 14 in roughly 3 seconds, and the $a_{k,r}[n]$ coefficients get close to their ideal values in less than $2 \cdot 10^6$ reference periods (~0.08 seconds), which is five times faster than in Fig. 14.

## APPENDIX A

It follows from Fig. 5 and (17) that

$$f_I(t) = \sum_{i=5}^{22} \Big[ \big( b_i[w_t] - ½ \big) \alpha_i(t) \Delta_i + \big( b_i[w_t - 1] - ½ \big) \gamma_i(t) \Big]. \tag{54}$$

Expressions for each $b_i[w_t] = c_{i+12}[g(w_t)]$ in terms of $d[g(w_t)]$ and the switching sequences can be found by tracing through the tree of Fig. 6 and applying (20) and the expressions shown in Fig. 4(a) and Fig. 4(b). This leads to

$$c_i[g(w_t)] - ½ = m_i d[g(w_t)]/\Delta + \sum_{k,r} \kappa_{k,r,i} s_{k,r}[g(w_t)], \tag{55}$$

where

$$m_i = 0 \text{ for } 17 \le i \le 26 \text{ and } m_i = 2^{-16} \text{ for } 27 \le i \le 34, \tag{56}$$

and each $\kappa_{k,r,i}$ is one of 0, $-½$, ½, $-2^{-k}$ or $2^{-k}$. Combining (4), (19) and (54)-(56) yields (26) and (27), where $\alpha_I(t)$ and $\gamma_I(t)$ are the averages of $\alpha_i(t)$ and $(2^{-13}/\Delta)\gamma_i(t)$ for $i$ = 15, 16, …, 22, respectively,

$$\alpha_{k,r}(t) = \sum_{i=5}^{22} \alpha_i(t) K_{i+12} \kappa_{k,r,i+12} \text{ and } \gamma_{k,r}(t) = \sum_{i=5}^{22} \frac{\gamma_i(t)}{\Delta} \kappa_{k,r,i+12}. \tag{57}$$

Each $\alpha_I(t)$, $\gamma_I(t)$, $\alpha_{k,r}(t)$ and $\gamma_{k,r}(t)$ is $T_{\text{fast}}$-periodic, because it is a linear combination of $\alpha_i(t)$ and $\gamma_i(t)$, which are $T_{\text{fast}}$-periodic.

## APPENDIX B

The phase error of the digital PLL shown in Fig. 9 is given by

$$\theta_{\mathrm{PLL}}(t) = \int_0^t \psi_{\mathrm{PLL}}(u)du, \tag{58}$$

where $\psi_{\mathrm{PLL}}(t)$ is the PLL's frequency error at time $t$. The $\theta_{\mathrm{PLL}}[n]$ term in (44) is a sampled version of $\theta_{\mathrm{PLL}}(t)$ given by

$$\theta_{\mathrm{PLL}}[n] = \theta_{\mathrm{PLL}}(\tau_n), \tag{59}$$

where $\tau_n = nT_{\mathrm{ref}} + \lambda_n$ and $\lambda_n$ is a small implementation-dependent deviation of $\tau_n$ from its ideal value. It follows from (44), (58) and (59) that

$$p[n] = p[0] - T_{\mathrm{ref}} \sum_{i=1}^{n} \psi_{\mathrm{PLL}}[i] + e_p[n], \tag{60}$$

where

$$\psi_{\mathrm{PLL}}[i] = \frac{1}{T_{\mathrm{ref}}} \int_{\tau_{i-1}}^{\tau_i} \psi_{\mathrm{PLL}}(u)du \tag{61}$$

is the PLL's average frequency error over the time interval $[\tau_{i-1}, \tau_i]$ and $p[0]$ is the initial value of $p[n]$. Fig. 9 and (61) imply that $e_R(t)$ causes a term in $\psi_{\mathrm{PLL}}[i]$ given by

$$\{e_R * h\}[i] = \sum_{j=0}^{\infty} h[j]e_R[i-j], \tag{62}$$

where

$$e_R[i] = \frac{1}{T_{\mathrm{ref}}} \int_{\tau_{i-1}}^{\tau_i} e_R(u)du \tag{63}$$

and $h[j]$ is the impulse response of the highpass filtering operation imposed by the PLL on the DCO's additive frequency error as described in Section VI-B.

In the design example of this paper $\lambda_n = 4.2T_{\text{fast}} + \frac{1}{8}T_{\text{fast}}v[n]$, where $v[n]$ is an integer-valued sequence restricted to the set $\{-6, -5, \ldots, 5, 6\}$, so $\tau_n = nT_{\text{ref}} + 4.2T_{\text{fast}} + \frac{1}{8}T_{\text{fast}}v[n]$. As the magnitude of $\frac{1}{8}T_{\text{fast}}v[n]$ is at most $\frac{3}{4}T_{\text{fast}}$, its effect is negligible. Furthermore, for the sake of simplicity, $\tau_n$ is assumed to be given by

$$\tau_n = \mu_n + 4T_{\text{fast}}, \tag{64}$$

where $\mu_n$, as shown in Fig. 10(b), is a multiple of $T_{\text{fast}}$. Given that $0 < \mu_n - nT_{\text{ref}} \leq T_{\text{fast}}$ for all $n$ and that $T_{\text{fast}}$ is a small fraction of $T_{\text{ref}}$, this approximation does not significantly affect the following results. Substituting (36) with $a_{k,r}$ and $b_{k,r}$ replaced by $a_{k,r}[g(w_t)]$ and $b_{k,r}[g(w_t)]$, respectively, into (35), and the result of this operation and (64) into (63) yields

$$\begin{aligned} e_R[i] = \frac{\Delta}{T_{\text{ref}}} \sum_{k,r} \int_{\mu_{i-1}+4T_{\text{fast}}}^{\mu_i+4T_{\text{fast}}} \Big\{ \Big(\delta_{k,r} - \alpha_F a_{k,r}[g(w_t)]\Big) s_{k,r}[g(w_t)] \\ + \Big(\gamma_{k,r}(t) - \alpha_F b_{k,r}[g(w_t)]\Big)\Big(s_{k,r}[g(w_t - 1)] - s_{k,r}[g(w_t)]\Big)\Big\} dt. \end{aligned} \tag{65}$$

Given that $t \in [\mu_n, \mu_{n+1})$ implies $g(p_t) = n - 1$, it follows that $g(w_t) = i - 2$ for $t \in [\mu_{i-1} + 4T_{\text{fast}}, \mu_i + T_{\text{fast}})$ and $g(w_t) = i - 1$ for $t \in [\mu_i + T_{\text{fast}}, \mu_i + 4T_{\text{fast}})$, so (65) can be written as

$$e_R[i] = -\Delta \frac{\alpha_F T_{\text{fast}}}{T_{\text{ref}}} \sum_{k,r} \Big\{ y_{k,r\text{-}a}[i-1] + y_{k,r\text{-}b}[i-1] \Big\}, \tag{66}$$

where $y_{k,r\text{-}a}[i]$ and $y_{k,r\text{-}b}[i]$ are given by (47) and (48), respectively, and it has been assumed that $q_i = (\mu_{i+1} - \mu_i)/T_{\text{fast}}$ is greater than 3 for all $i$ (e.g., $q_i \cong 16$ in the design example). Substituting (66) into (62) and the result into (60), rearranging terms and considering that $s_{k,r}[n] = 0$ for $n < 0$ gives (45) and (46).

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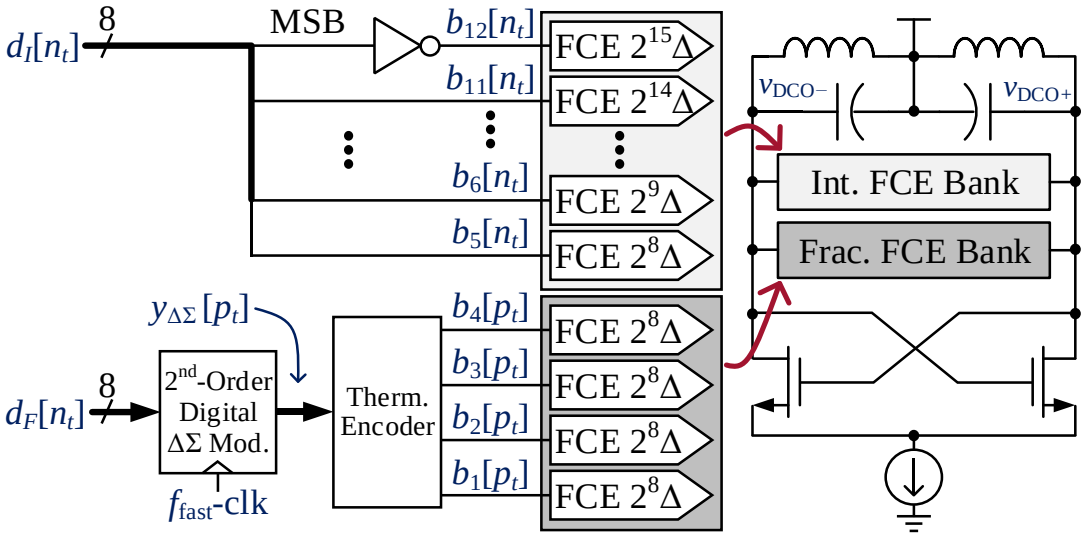


Figure 1: Conventional frequency control technique for an LC-based DCO.

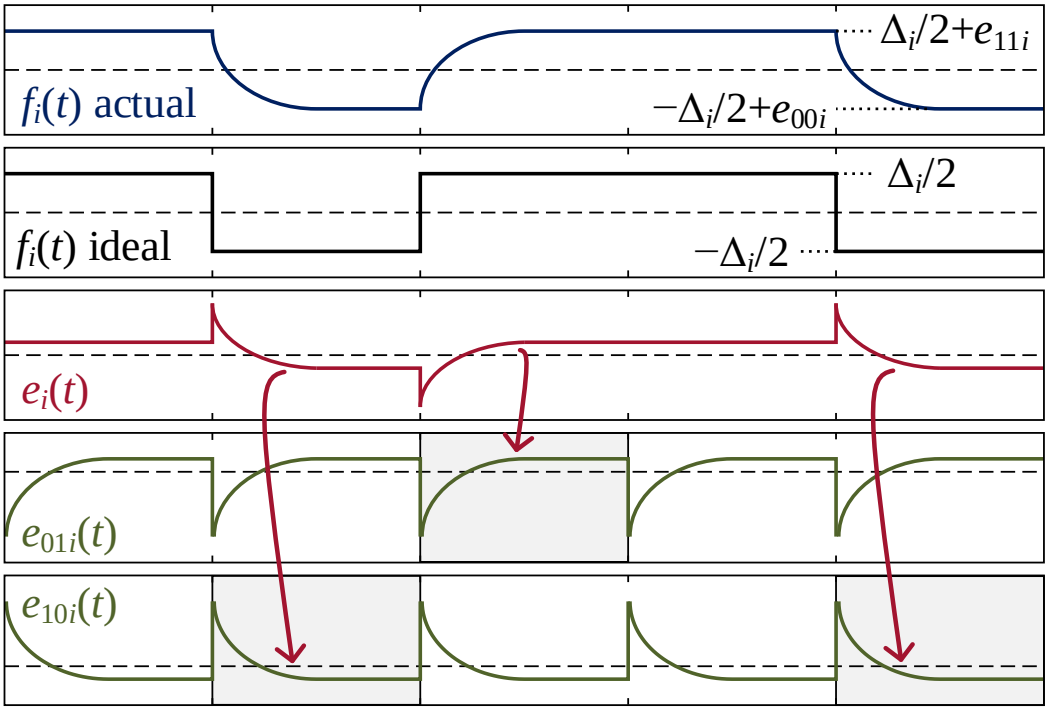


Figure 2: Example waveforms related to (15) and (16) for an FCE input bit sequence of 1, 0, 1, 1, 0.

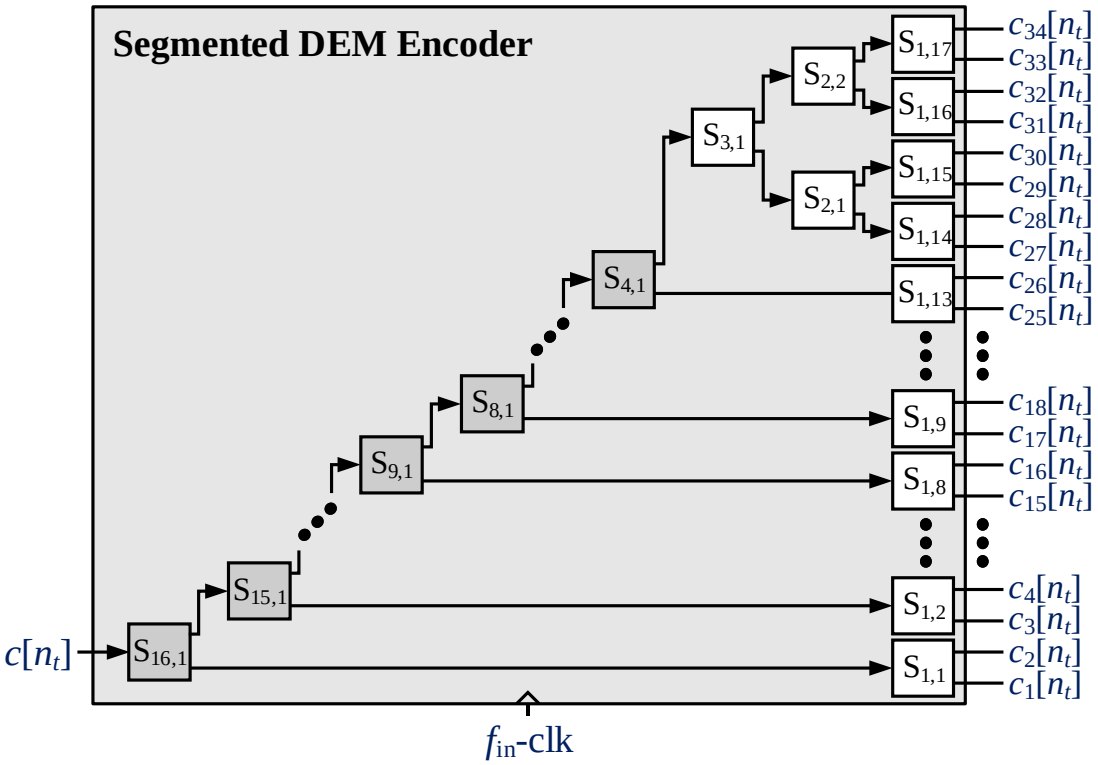


Figure 3: Segmented DEM encoder example.

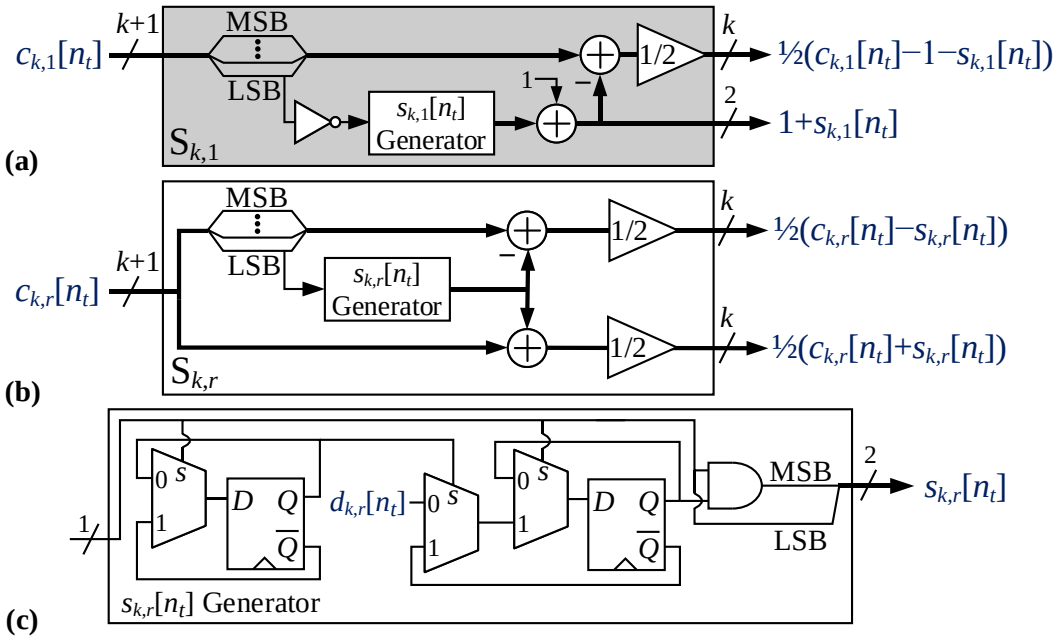


Figure 4: (a) Segmenting switching block, (b) non-segmenting switching block, and (c) switching sequence generator.

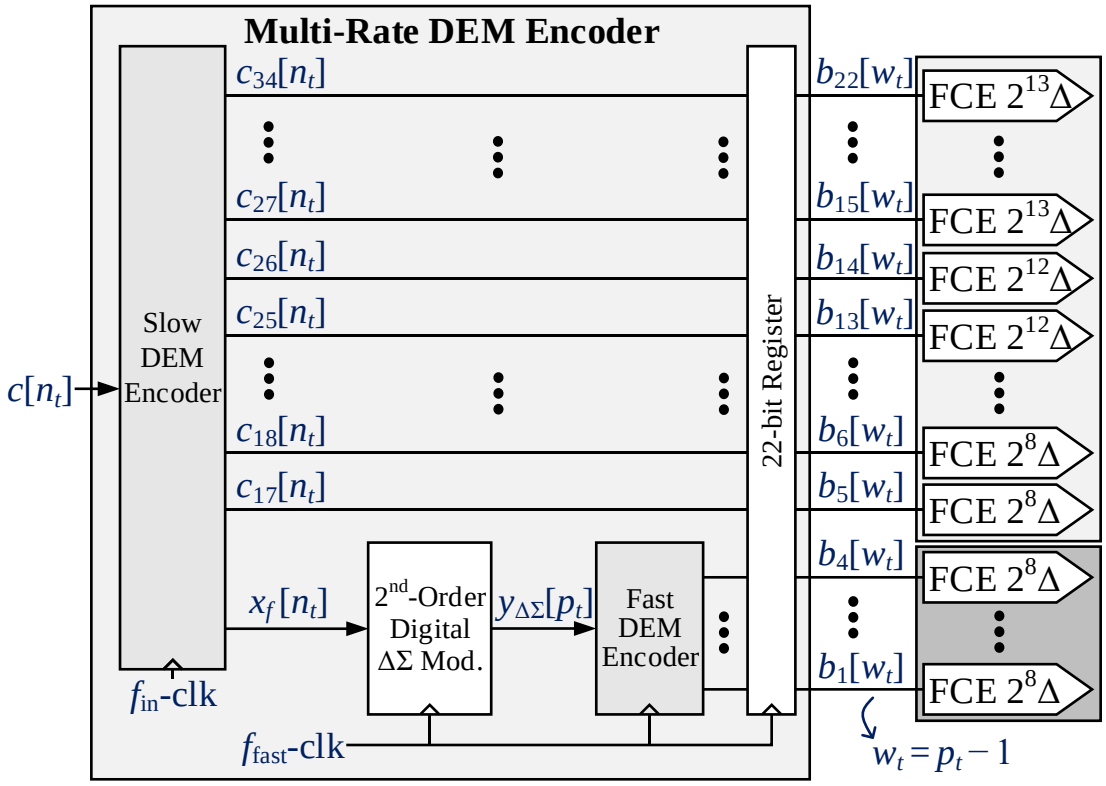


Figure 5: Multi-rate DEM encoder example.

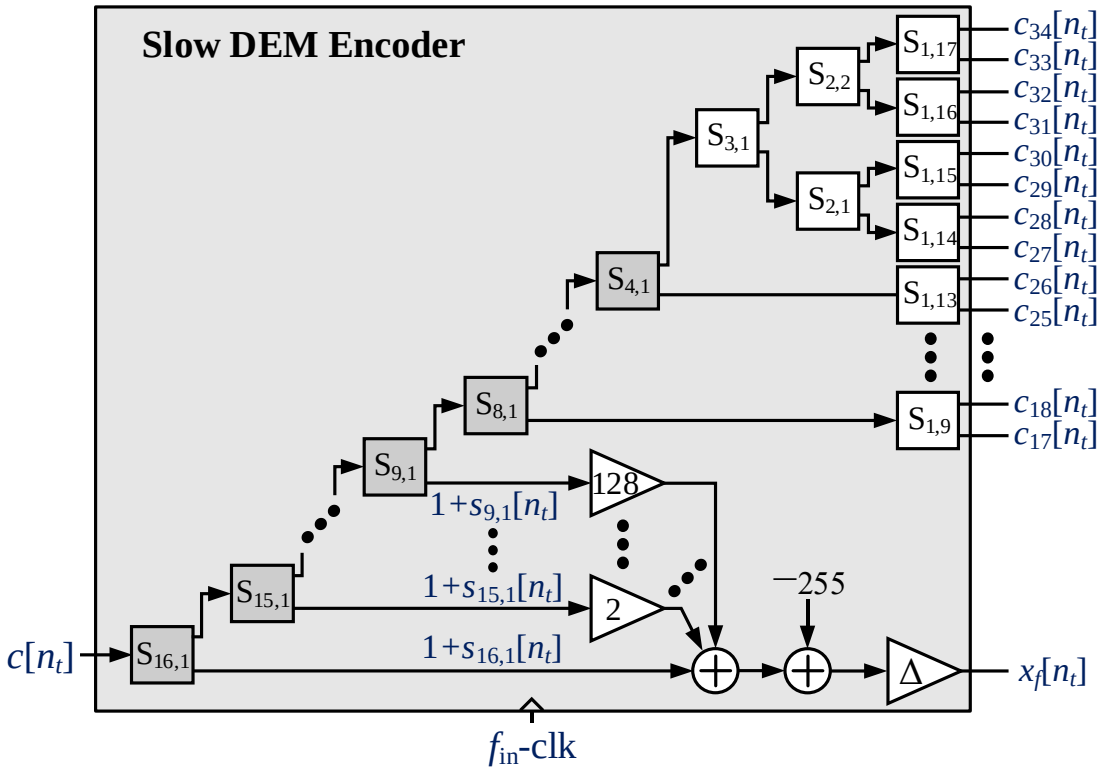


Figure 6: Slow DEM encoder example.

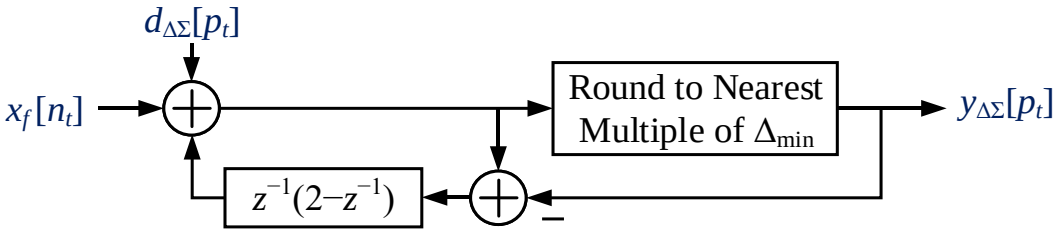


Figure 7: Details of the second-order digital ΔΣ modulator.

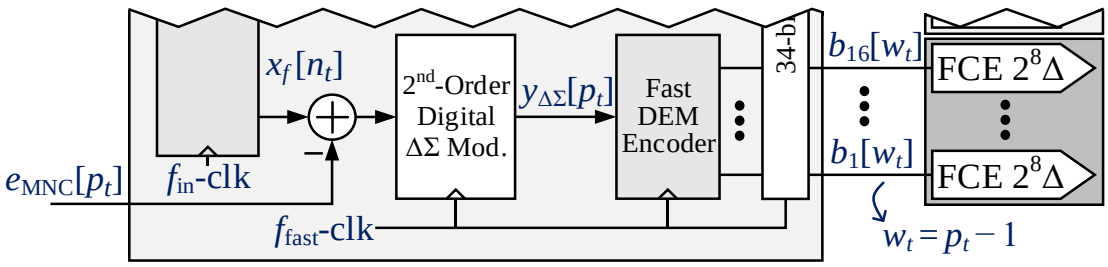


Figure 8: Fractional path of the example multi-rate DEM encoder shown in Fig. 5 modified to accommodate $e_{MNC}[p_t]$.

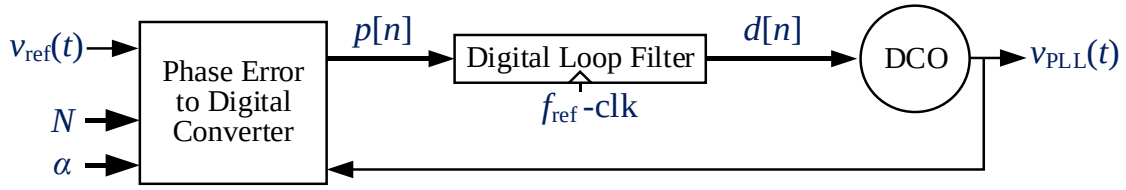


Figure 9: General form of a digital fractional-*N* PLL.

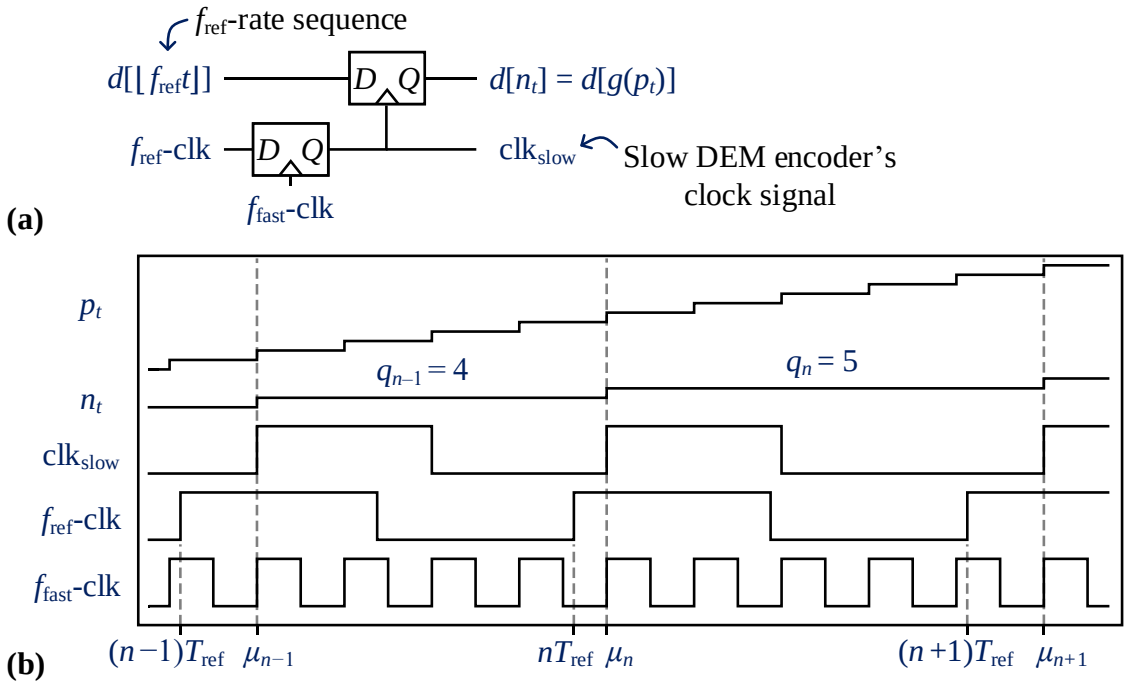


Figure 10: (a) Synchronization circuit used at DCO input, and (b) illustration of the clock signals within the DCO, $p_t$, and $n_t = g(p_t)$ for $f_{fast} = 4.5f_{ref}$.

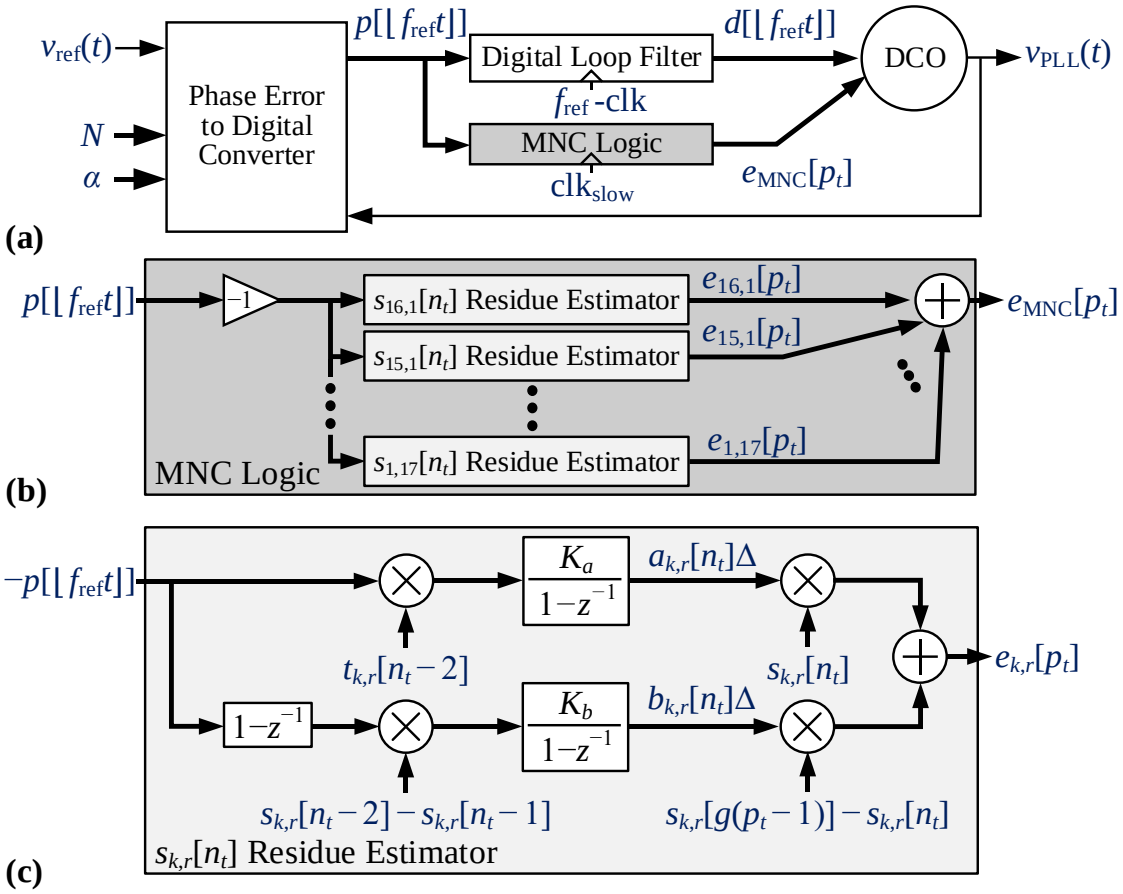


Figure 11: (a) Digital fractional-N PLL with multi-rate DEM and MNC, (b) details of the MNC logic, and (c) details of each switching sequence residue estimator.

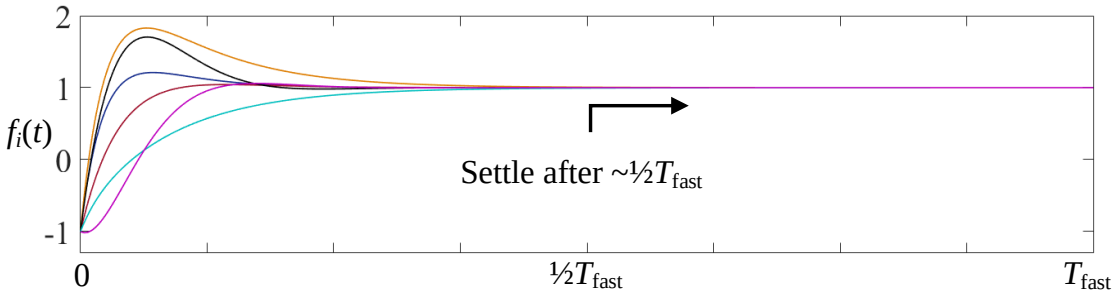


Figure 12: Example frequency transitions normalized to $\Delta_i/2$ versus time over $T_{fast} = 8T_{PLL}$ for six different FCEs.

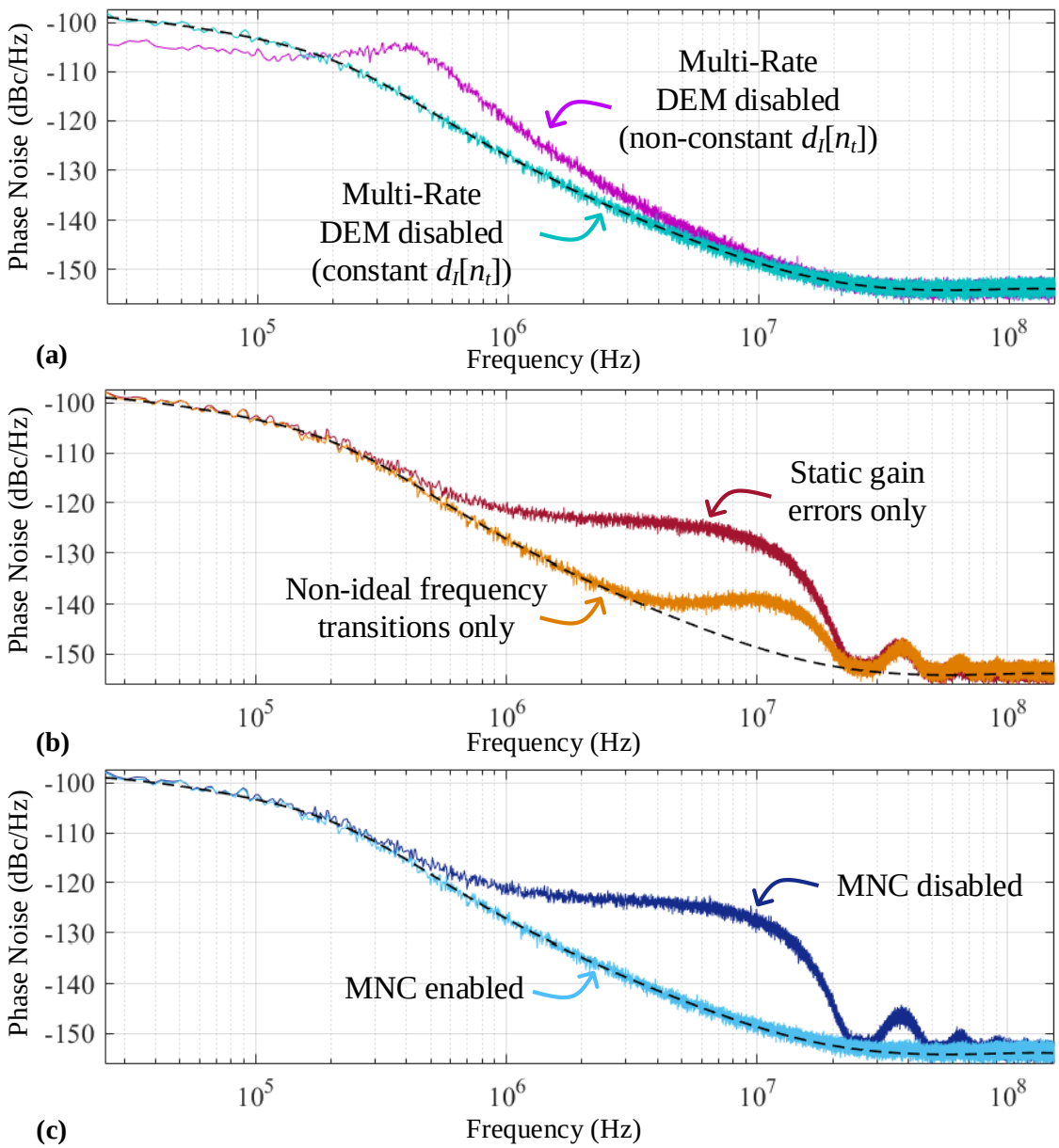


Figure 13: Simulated PLL phase noise PSD versus frequency with (a) static gain errors and non-ideal frequency transitions enabled and the multi-rate DEM technique disabled, (b) static gain errors and non-ideal frequency transitions enabled separately and the multi-rate DEM technique enabled, and (c) both sources of error enabled, the multi-rate DEM technique enabled and the MNC technique disabled and enabled.

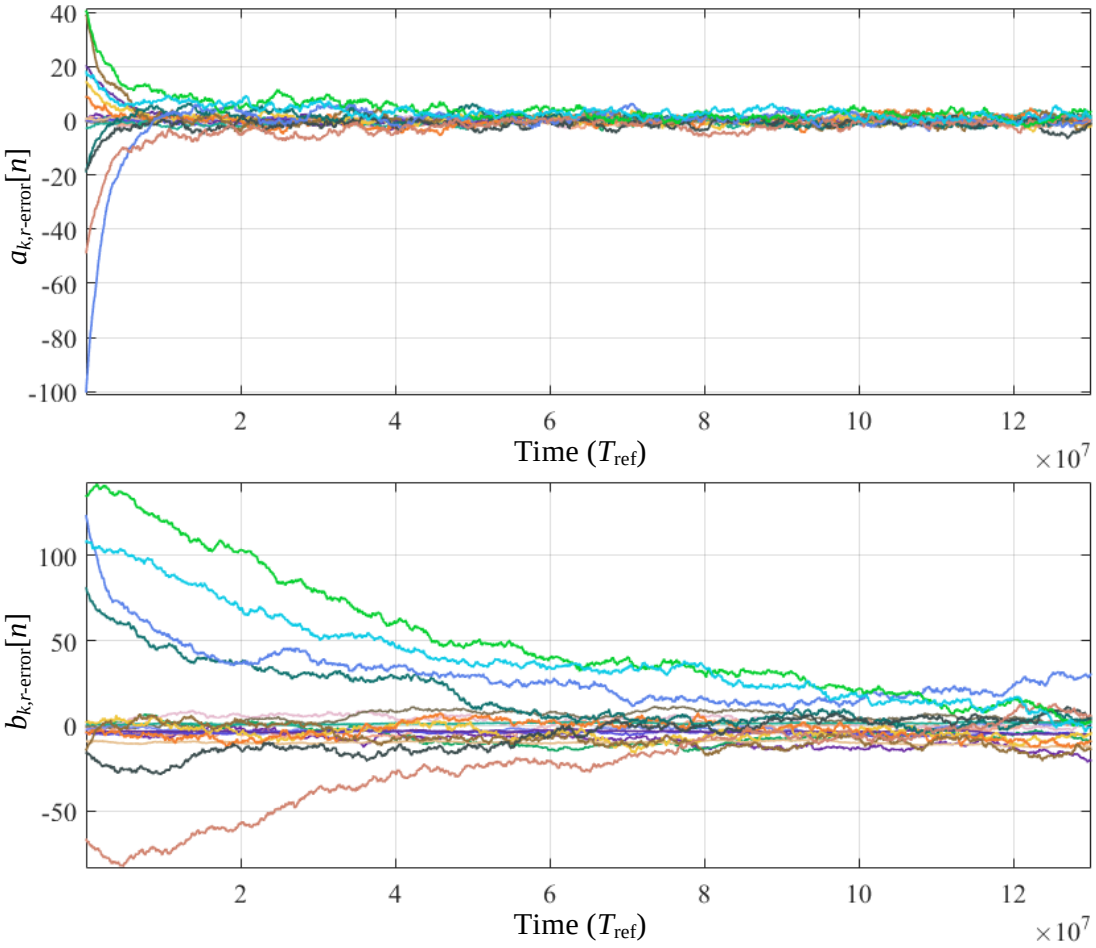


Figure 14: MNC coefficient error evolution over time for $K_a = 2^{-3}$ and $K_b = 2^{-5}$.

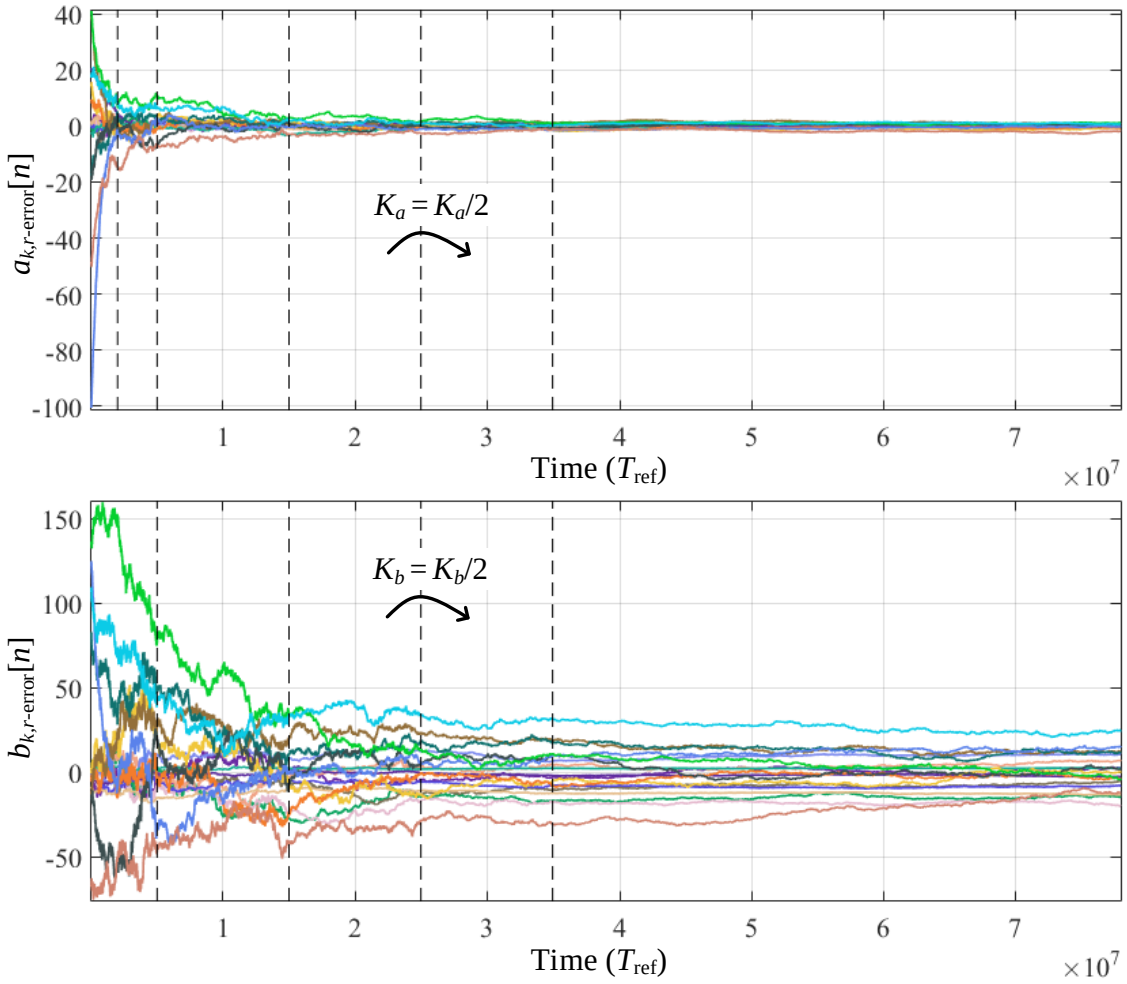


Figure 15: MNC coefficient error evolution over time for MNC gains that change over time. Initially $K_a = 2^{-1}$ and $K_b = 2^{-2}$, and after 3.5·107 reference periods $K_a = 2^{-6}$ and $K_b = 2^{-6}$.

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# CHAPTER 2

# DELTA-SIGMA FDC ENHANCEMENTS FOR FDC-BASED DIGITAL FRACTIONAL-*N* PLLS

**Abstract**— This paper describes all-digital enhancements for digital fractional-*N* phase-locked loops (PLLs) based on delta-sigma (ΔΣ) frequency-to-digital converters (FDCs). The enhancements include an improved dual-mode ring oscillator (DMRO)-based ΔΣ FDC architecture and a digital background calibration technique that compensates for the ΔΣ FDC's forward path gain error. The improved ΔΣ FDC has significantly relaxed timing constraints and a 3× smaller phase-frequency detector output pulse-width span relative to the prior art, which make it simpler to implement and amenable to higher-frequency reference signals. The calibration technique compensates for non-ideal DMRO frequencies in the digital domain. It eliminates the need to tune the DMRO instantaneous frequencies as a function of the PLL output frequency, thereby simplifying the DMRO implementation, and it also improves the phase noise performance of PLLs with high loop bandwidths.

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# I. INTRODUCTION

Digital fractional-*N* phase-locked loops (PLLs) based on second-order delta-sigma (ΔΣ) frequency-to-digital converters (FDCs) offer advantages of both analog and digital PLLs [1]–[12]. They have the same quantization error behavior as analog PLLs based on second-order ΔΣ modulators, but they do not require large-area analog loop filters.

This paper presents all-digital enhancements for ΔΣ FDCs that reduce implementation complexity and improve performance. The enhancements include a modified dual-mode ring oscillator (DMRO)-based ΔΣ FDC architecture and a digital background calibration technique that compensates for ΔΣ FDC forward path gain error caused by non-ideal DMRO frequencies.

The modified ΔΣ FDC architecture has relaxed timing constraints and a 3× smaller phase-frequency detector (PFD) output pulse-width span compared to prior-art ΔΣ FDCs [8]–[12]. These benefits make the new ΔΣ FDC simpler to implement [13]. They also make it amenable to higher-frequency reference signals for any given PLL output frequency, which is useful because increasing the reference frequency reduces the contributions of the reference signal phase noise, ΔΣ FDC quantization error, and DMRO phase noise to the PLL's output phase noise [11].

The DMRO in a DMRO-based ΔΣ FDC is designed to oscillate at one of two frequencies at any given time. These frequencies, denoted as $f_{high}$ and $f_{low}$ in this paper, ideally have a specific relationship to the PLL output frequency, $f_{PLL}$. In prior art DMRO-based ΔΣ FDCs, $f_{high}$ and $f_{low}$ are adjusted each time $f_{PLL}$ is changed to approximate this ideal relationship, which adds complexity to the DMRO design. Furthermore, while the PLL's performance is

relatively insensitive to deviations of $f_{high}$ and $f_{low}$ from their ideal values for low-to-moderate PLL bandwidths, this is not the case for high PLL bandwidths.

The proposed digital background calibration technique addresses these issues. Rather than dynamically adjusting $f_{high}$ and $f_{low}$ by controlling the DMRO's analog circuitry as a function of $f_{PLL}$, it dynamically adjusts digital circuitry to compensate for error that would otherwise be caused by non-ideal values of $f_{high}$ and $f_{low}$. Moreover, it does so with much finer resolution than prior art ΔΣ FDCs are able to adjust the DMRO to tune $f_{high}$ and $f_{low}$. These benefits greatly simplify the DMRO, which can now be designed to have fixed values of $f_{high}$ and $f_{low}$, and significantly reduce phase noise for high PLL bandwidths.

The remainder of the paper consists of four main sections. Section II provides an overview of prior-art fractional-*N* PLLs that incorporate ΔΣ FDCs based on DMROs. Sections III and IV present the proposed ΔΣ FDC enhancements described above, and Section V presents simulation results that demonstrate their performance.

## II. ΔΣ FDC DIGITAL FRACTIONAL-*N* PLL OVERVIEW

### A. ΔΣ FDC-Based PLL

A high-level block diagram of a second-order ΔΣ FDC-based fractional-*N* PLL is shown in Fig. 16. It consists of a ΔΣ FDC, a digital loop controller (DLC) with quantization noise cancellation (QNC), and a digitally-controlled oscillator (DCO) [8]–[12]. The signal $v_{ref}(t)$ is t he output of a reference oscillator with frequency $f_{ref}$ and $v_{PLL}(t)$ is the PLL output waveform. Ideally, $v_{PLL}(t)$ is periodic with frequency $f_{PLL} = (N + \alpha)f_{ref}$, where $N$ is a positive integer and $\alpha$ has a fractional value that can range from –½ to ½.

The ΔΣ FDC generates two $f_{ref}$-rate digital sequences, $y[n]$ and $-\hat{e}_q[n]$. Specifically,

$$y[n] = -\alpha - e_{PLL}[n] + \underbrace{e_q[n] - 2e_q[n-1] + e_q[n-2]}_{2^{nd}\text{-order shaped version of } e_q[n]}, \tag{67}$$

where $e_q[n]$ is the quantization error introduced by the ΔΣ FDC and $e_{PLL}[n]$ is a measure of the average frequency error of $v_{PLL}(t)$ over the $n$th reference period. The $\hat{e}_q[n]$ sequence is an estimate of $e_q[n]$. It is used to partially cancel the contribution of $e_q[n]$ at the input of the digital loop filter (DLF) within the DLC [12]–[15]. By cancelling the quantization error prior to the loop filter, QNC allows the PLL's bandwidth to be increased without significantly degrading the PLL's phase noise.

B. Original ΔΣ FDC Architecture

A simplified block diagram of the ΔΣ FDC presented in [11], hereafter referred to as the original ΔΣ FDC, is shown in Fig. 17(a). It consists of a PFD with top output $u(t)$, a multi-modulus divider with output $v_{div}(t)$, a DMRO, a digital ring phase calculator (RPC), and a $2 - z^{-1}$ digital feedback block with output $v[n]$ that controls the divider. Although not shown in Fig. 2 for simplicity, the RPC's accumulator clips to keep its output in the range $-2 \leq r[n] < 3$. As explained in [10], this reduces the PLL's worst-case locking time, but has no effect on the PLL's locked behavior. The PFD and divider are identical to those in analog PLLs.

Each reference period, the signal encoded in the width of the $u(t)$ pulse is accumulated by the DMRO. Then, the outputs of the DMRO, which represent a quantized version of its phase, are sampled and processed by the RPC to generate $y[n]$ and $-\hat{e}_q[n]$.

The DMRO is implemented as a ring of $N_R$ nominally identical delay cells. Ideally, its instantaneous frequency is $f_{high}$ when $u(t)$ is high and $f_{low}$ when $u(t)$ is low, where

$$A\frac{\left(f_{\text{high}}-f_{\text{low}}\right)}{f_{\text{PLL}}}=1, \tag{68}$$

and $A$ is a design parameter [11].[7]

Each reference period, the quantized DMRO phase, $p_R[n]$, is computed from the DMRO output lines. As indicated in Fig. 2(a), $p_R[n]$ is passed through a $1-z^{-1}$ block, and a positive constant, $M$, is subtracted from the result prior to the multiplication by $A$ and accumulation. These operations yield $r[n]$, which is a fixed-point measure of $-\alpha - e_{\text{PLL}}[n]$ in units of cycles per reference period. The three most significant bits (MSBs) of $r[n]$ correspond to the integer part of $r[n]$, whereas the remaining least significant bits (LSBs) correspond to the fractional part of $r[n]$[11].

The operation of the divider is such that adjacent rising edges of $v_{\text{div}}(t)$ are separated by $N-v[n]$ PLL output periods. Ideally, $v[n]$ would be set to $2r[n]-r[n-1]$, but dividers can only count integer numbers of PLL output periods and $r[n]$ contains both integer and fractional parts. Therefore, it is necessary to instead use just the integer part of $r[n]$, i.e., $y[n]$, so that $v[n] = 2y[n]-y[n-1]$ is integer-valued. Given that $y[n]$ is a quantized version of $r[n]$, the fractional part of $r[n]$, i.e., $-\hat{e}_q[n]$, is the negative of the corresponding quantization error. The DLC uses $-\hat{e}_q[n]$ to perform QNC.

As proven in [11], the behavior of the system shown in Fig. 2(a) is identical to that of the second-order ΔΣ modulator shown in Fig. 3(a). The phase quantization operation performed by the DMRO is denoted by $Q_r$ and modeled as a fine quantizer of step-size $\Delta_r = (2N_R)^{-1}$. Its

[7] In [11], $2^{-J}$, where $J$ is an integer, is used instead of $A^{-1}$, but the structures shown in Fig. 2 do not restrict $A$ to be a power of 2.

quantization error, $e_{qr}[n]$, corresponds to the *residual* quantization error that is left after QNC. The quantization operation that occurs at the output of the RPC is denoted as $Q_c$ and modeled as a *coarse* quantizer with step-size $\Delta_c = 1$. If $2N_R/A$ is integer-valued, then the blocks contained in the dashed contour in Fig. 3(a) are equivalent to an accumulator followed by a quantizer, $Q$, with unity step-size and associated error given by

$$e_q[n] = Ae_{qr}[n] + \hat{e}_q[n]. \tag{69}$$

In this case, $y[n]$ is given by (67) and the system's self-dithering property causes $e_q[n]$ to have a power spectral density (PSD) equivalent to that of a zero-mean white noise sequence with variance 1/12 [16], [17].

### C. Original ΔΣ FDC Issues

The original ΔΣ FDC suffers from two issues. One issue is tight timing constraints on both the digital part of the ΔΣ FDC and the divider. The other issue is high sensitivity to non-ideal DMRO frequencies for high PLL bandwidths.

Once the ΔΣ FDC locks, the rising edges of $v_{\text{div}}(t)$ succeed and precede rising and falling edges of $v_{\text{ref}}(t)$, respectively [10], [11]. Therefore, as implied by Fig. 17(a), after the $n$th rising edge of $v_{\text{div}}(t)$, the ΔΣ FDC must compute $y[n]$ and use it along with $y[n-1]$ to form $v[n]$, which the divider then uses to determine the $(n + 1)$th rising edge of $v_{\text{div}}(t)$. This limits the time available for the ΔΣ FDC to process the $u(t)$ pulse and compute $y[n]$ to approximately one reference period, and requires a divider that is capable of loading the divider modulus in the middle or toward the end of the divider count [10]. These features tend to increase the power consumption, circuit area, and complexity of the divider.

As explained in [11], ΔΣ FDC-based PLLs are not highly sensitive to non-ideal values of $f_{high}$ and $f_{low}$, i.e., values of $f_{high}$ and $f_{low}$ that do not exactly satisfy (68), in much the same way that a second-order ΔΣ modulator is not sensitive to deviations in the gain of its second accumulator [16]. Nevertheless, the need to adjust the DMRO in the original ΔΣ FDC each time $f_{PLL}$ changes so that $f_{high}$ and $f_{low}$ at least approximately satisfy (68) complicates the DMRO design. Moreover, as shown in Section IV, the accuracy with which (68) must be satisfied increases significantly with PLL bandwidth to the point that process, voltage, and temperature variations cause $f_{high}$ and $f_{low}$ to deviate from their ideal values enough to significantly degrade the PLL's phase noise.

## III. IMPROVED ΔΣ FDC

### A. Proposed ΔΣ FDC Architecture

The proposed ΔΣ FDC is shown in Fig. 17(b).[8] It is similar to that shown in Fig. 17(a) except for the feedback digital block and the details of the RPC. Instead of feeding back $2y[n] - y[n-1]$ through the divider, $2y[n-1]$ is fed back directly to the input of the accumulator within the RPC, and only $y[n-1]$ is fed back through the divider.

An argument similar to that presented in [11] shows that the resulting system's behavior is identical to that of the second-order ΔΣ modulator shown in Fig. 18(b), whose behavior is identical to that of the system shown in Fig. 18(a) provided $2N_R/A$ is integer-valued.

[8] The sequences $v[n]$, $p_R[n]$ and $d_R[n]$ and the signals $u(t)$ and $v_{div}(t)$ in Fig. 17(b) are not identical to those in Fig. 17(a), but they play the same roles in both ΔΣ FDCs, which is why they share the same names.

A feature of the original ΔΣ FDC is that once it locks, the DMRO locks to an average frequency of $Mf_{\text{ref}}$, which minimizes the potential for fractional spurs if $M$ is integer-valued [10]. Specifically, given that $r[n]$ is bounded when the ΔΣ FDC is locked, the input to the accumulator within the RPC, and, hence, the $M$-adder output, must be zero-mean, which can only happen if the DMRO phase advances, on average, $M$ cycles per reference period.

In the proposed ΔΣ FDC, the average of the $M$-adder output is forced to zero by subtracting $2\alpha$ from the accumulator's input, so that the average DMRO frequency is given by $Mf_{\text{ref}}$. Reasoning similar to that presented above and (67) imply that without the $2\alpha$ subtraction the local feedback around the accumulator would cause the output of the $M$-adder to have an average of $-2A^{-1}\alpha$. In this case, the DMRO would lock to $(M - 2A^{-1}\alpha)f_{\text{ref}}$, which would increase the potential for fractional spurs.

The $2\alpha$ subtraction slightly increases the PLL's digital complexity relative to a comparable PLL based on the original ΔΣ FDC. For instance, in the PLL implementation described in Section V, the cycle counter and phase decoder's output, $p_R[n]$, has 10 fractional bits, $\alpha$ has 20 fractional bits, and $A = 1$, so the $2\alpha$ subtraction nearly doubles the number of fractional bits required to represent the RPC accumulator's input. Nonetheless, the number of fractional bits in the DLF input is determined by $\alpha$ regardless of which ΔΣ FDC is used, so the proposed ΔΣ FDC's $2\alpha$ subtraction only affects the RPC's accumulator. Hence, it represents only a minor increase in the PLLs overall digital complexity. Moreover, this increase in complexity is offset by the proposed ΔΣ FDC's features described below.

It follows from Fig. 18(b) that for the proposed ΔΣ FDC the discrete-time transfer function from the input to the second accumulator output has a pole at DC, which suggests that

the system is unstable. Although the $2\alpha$ term injected within the RPC causes the DC component at the output of the second accumulator to be zero, noise present at this node can cause the magnitude of the accumulator output to grow without bound. However, the second accumulation shown in Fig. 18(b) is performed by the DMRO, so this is not an issue in practice because the DMRO behaves as an accumulator with infinite output range [10]. Specifically, provided the cycle counter within the RPC does not roll-over more than once per reference period, which can be ensured by design, then the $1 - z^{-1}$ block within the RPC can unwrap the sampled DMRO phase and retrieve the information encoded in it, thereby allowing the magnitude of the second accumulator's output in Fig. 18(b) to be arbitrarily large.

While the DC pole issue is not a problem in the modified ΔΣ FDC as explained above, it would present practical issues if corresponding modifications were applied to the charge pump (CP)-based ΔΣ FDC described in [8], [9], and [12]. In CP-based ΔΣ FDCs, the CP performs integration in place of the DMRO, yet charge pumps do not offer the convenient roll-over feature inherent to DMROs.

## B. Proposed ΔΣ FDC Features

*Relaxed Timing Constraints:* Fig. 19 shows example timing diagrams for the original and proposed ΔΣ FDCs, where the time sequences $t_n$ and $\tau_n$, for $n = 0, 1, 2, \ldots$, are the times of the $n$th rising edges of $v_{\text{ref}}(t)$ and $v_{\text{div}}(t)$, respectively, and the $n$th divider modulus is the number of PLL output periods between $\tau_{n-1}$ and $\tau_n$. In this example, the DMRO phase is sampled at times $\gamma_n = t_n + T_{\text{ref}}/2$, where $T_{\text{ref}} = 1/f_{\text{ref}}$ is the reference period, and the $n$th divider modulus can be loaded at time $t_n$ at the latest.

In the original ΔΣ FDC, the $n$th divider modulus is given by $N-(2y[n-1]-y[n-2])$, but as illustrated in Fig. 19(a), $y[n-1]$ cannot be computed before the DMRO phase is sampled at $\gamma_{n-1} > \tau_{n-1}$. It follows that the $n$th divider modulus can only be loaded once $y[n-1]$ is ready *around the middle or near the end* of the count, which increases the divider's complexity. For example, the divider in [10] required significant additional logic to meet this requirement compared to the original version of the divider presented in [18]. Furthermore, as the divider modulus must be updated before $t_n$, the amount of time available for the ΔΣ FDC to compute $y[n-1]$ is limited to $T_{\text{ref}}/2$.

As illustrated in Fig. 19(b), the proposed ΔΣ FDC has much more relaxed timing constraints. In this case, the $n$th divider modulus is given by $N-y[n-2]$. By the time of the ($n$ – 1)th rising edge of $v_{\text{div}}(t)$, the ΔΣ FDC has already had a duration of more than $T_{\text{ref}}/2$ to compute $y[n-2]$, so the next count can start with a known divider modulus. Alternatively, the computation of $y[n-2]$ can take up to $T_{\text{ref}}$, and the divider modulus can be updated *near the beginning* of the current count. In either case, compared to the original ΔΣ FDC, the proposed ΔΣ FDC allows for simpler divider topologies to be used and imposes looser digital timing constraints on the ΔΣ FDC.

*Reduced PFD Output Span:* As shown in [11], for the original ΔΣ FDC, $e_{\text{PLL}}[n]$ in (67) is given by

$$e_{\text{PLL}}[n]=\psi_{\text{PLL}}[n]-\left(N+\alpha\right)\psi_{\text{ref}}[n]-A\left(\psi_{\text{DMRO}}[n]-\psi_{\text{DMRO}}[n-1]\right), \tag{70}$$

the $e_q[n]$ sequence is bounded by

$$-1<e_q[n]\leq 0, \tag{71}$$

and the width of $u(t)$ is given by

$$\begin{aligned}\tau_n - t_n = T_{\bar{u}} + \Big( & -y[n-1] - \psi_{\mathrm{PLL}}[n] + \big(N+\alpha\big)\psi_{\mathrm{ref}}[n] \\ & - A\psi_{\mathrm{DMRO}}[n-1] - e_q[n-1] + e_q[n-2] - \alpha\Big) T_{\mathrm{PLL}},\end{aligned} \tag{72}$$

where $\psi_{\mathrm{PLL}}[n]$, $\psi_{\mathrm{ref}}[n]$ and $\psi_{\mathrm{DMRO}}[n]$ are the phase noise changes per reference period of $v_{\mathrm{PLL}}(t)$, $v_{\mathrm{ref}}(t)$ and the DMRO, respectively, and

$$T_{\bar{u}} = \frac{M - T_{\mathrm{ref}} f_{\mathrm{low}}}{f_{\mathrm{high}} - f_{\mathrm{low}}} \tag{73}$$

is the average width of the $u(t)$ pulse.

Suppose $b_{\mathrm{PLL}}$ and $b_{\mathrm{DMRO}}$ are the maximum magnitudes of $e_{\mathrm{PLL}}[n]$ and $\psi_{\mathrm{DMRO}}[n]$, respectively, so

$$\left|e_{\mathrm{PLL}}[n]\right| < b_{\mathrm{PLL}} \quad \text{and} \quad \left|\psi_{\mathrm{DMRO}}[n]\right| < b_{\mathrm{DMRO}} \tag{74}$$

for all $n$. Then, it follows from (67), (70)-(72) and (74) that the maximum span of $u(t)$, $\Delta T_u$, which is defined as

$$\Delta T_u = 2 \max_n \left|\tau_n - t_n - T_{\bar{u}}\right|, \tag{75}$$

satisfies

$$\Delta T_u < 2\Big(3 + 2b_{\mathrm{PLL}} + Ab_{\mathrm{DMRO}}\Big) T_{\mathrm{PLL}}. \tag{76}$$

An analysis similar to that presented in [11] for the proposed ΔΣ FDC yields (70), (71) , and the following expression for the width of the $u(t)$ pulse during the $n$th reference period:

$$\begin{aligned}\tau_n - t_n = T_{\bar{u}} + \Big( & y[n-1] - \psi_{\mathrm{PLL}}[n] + \big(N+\alpha\big)\psi_{\mathrm{ref}}[n] \\ & - A\psi_{\mathrm{DMRO}}[n-1] - e_q[n-1] + e_q[n-2] + \alpha\Big) T_{\mathrm{PLL}},\end{aligned} \tag{77}$$

where $T_{\bar{u}}$ is also given by (73). Hence, (67), (70), (71), (74), (75) and (77) imply that, for the proposed ΔΣ FDC, $\Delta T_u$ satisfies

$$\Delta T_u < 2\left(1+2b_{\mathrm{PLL}}+Ab_{\mathrm{DMRO}}\right)T_{\mathrm{PLL}}. \tag{78}$$

In practice, $b_{\mathrm{PLL}}$, $b_{\mathrm{DMRO}} << 1$, so (76) and (78) imply that $\Delta T_u$ for the proposed ΔΣ FDC is approximately a third of that of the original ΔΣ FDC.

A smaller $\Delta T_u$ allows for a larger minimum difference between the phases of $v_{\mathrm{ref}}(t)$ and $v_{\mathrm{div}}(t)$, so it is beneficial as it mitigates spurs generated as a consequence of variations in the PFD supply voltage when $v_{\mathrm{ref}}(t)$ and $v_{\mathrm{div}}(t)$ are close in phase [19]. Additionally, reducing $\Delta T_u$ mitigates spurs from non-ideal DMRO behavior by increasing the time available for the DMRO's frequency transients to die out each reference period [10].

*Higher-Frequency Reference Signal:* The relaxed timing constraints and smaller $\Delta T_u$ of the proposed ΔΣ FDC allows for the use of higher-frequency reference signals, which lowers the contribution to the PLL's phase noise from all noise sources within the ΔΣ FDC. As in conventional fractional-$N$ PLLs, the contribution of the reference signal to the PLL output phase noise PSD, $S_{\mathrm{PLL}}(f)$, is proportional to $(N+\alpha)^2$ [8], [11]. Equations (67), (70) and Fig. 1 imply that the ΔΣ FDC quantization error and the DMRO phase noise appear first-order shaped at the DLF input, so their contribution to $S_{\mathrm{PLL}}(f)$ is proportional to $\sin^2(\pi T_{\mathrm{ref}} f)$. Additionally, the PSD of the quantization error is proportional to $T_{\mathrm{ref}}$ [11]. Therefore, increasing $f_{\mathrm{ref}}$ by a factor of $x$ for a given $f_{\mathrm{PLL}}$ with all other things being the same reduces the contributions to the PLL's phase noise from the reference signal, ΔΣ FDC quantization error, and DMRO by $20\log(x)$, $30\log(x)$ and $20\log(x)$, respectively.

## IV. DIGITAL GAIN CALIBRATION TECHNIQUE

### A. Effects of ΔΣ FDC Forward Path Gain Error

As explained in Section III, the behavior of the system shown in Fig. 17(b) is identical to that of a second-order ΔΣ modulator provided (68) holds and $2N_R/A$ is integer-valued. However, in practice

$$A\frac{f_{\text{high}}-f_{\text{low}}}{f_{\text{PLL}}}=\delta^{-1}, \tag{79}$$

where the deviation of the factor $\delta$ from its ideal value of 1 is the ΔΣ FDC's forward path gain error. This error degrades the system's self-dithering property [16], [17], and, as shown below, it reduces the extent to which QNC cancels the error introduced by the ΔΣ FDC's coarse quantization operation.

The analysis presented in [11] can be modified with (79) instead of (68) for the proposed ΔΣ FDC, which yields the behavioral model of the ΔΣ FDC shown in Fig. 20(a). The model is similar to that shown in Fig. 18(b), except that $e_{\text{PLL}}[n]$ is given by (70) with $\delta A$ instead of $A$, and the gain of the second accumulator is $(\delta A)^{-1}$ instead of $A^{-1}$. An analysis similar to that in [11] can also be performed to obtain a linearized model of the ΔΣ FDC PLL shown in Fig. 16 with the proposed ΔΣ FDC and (79) instead of (68). The resulting model is shown in Fig. 20(b), where $\theta_{\text{ref}}(t)$, $\theta_{\text{DMRO}}(t)$, $\theta_{\text{DCO}}(t)$ and $\theta_{\text{PLL}}(t)$ are the phase error waveforms of the reference signal, DMRO, DCO and PLL output, respectively,[9] $L(z)$ is the DLF's transfer function, $K_{\text{DCO}}$ is the

[9] Reasoning similar to that presented in [8] can be applied to the linearized model shown in Fig. 20(b) to obtain expressions for the PLL output's phase noise components that depend on $\theta_{\text{ref}}(t)$, $\theta_{\text{DMRO}}(t)$, $\theta_{\text{DCO}}(t)$, $e_{qr}[n]$ and $\hat{e}_q[n]$.

DCO gain (i.e., the amount in Hz by which the DCO frequency changes when the DCO input changes by unity) and

$$H(z) = 1 - \left(1 - \delta^{-1}\right) z^{-2}. \tag{80}$$

It follows from Fig. 5(b) that the discrete-time transfer functions from $e_{qr}[n]$ and $\hat{e}_q[n]$ to the input of the DLF, $p[n]$, are given by

$$A\frac{\left(1 - z^{-1}\right)}{H(z)}\frac{1}{1 + T(z)} \quad \text{and} \quad \left(1 - \delta^{-1}\right) z^{-2}\frac{\left(1 - z^{-1}\right)}{H(z)}\frac{1}{1 + T(z)}, \tag{81}$$

respectively, where

$$T(z) = \delta^{-1} K_{\text{DCO}} T_{\text{ref}} \frac{z^{-2} L(z)}{\left(1 - z^{-1}\right) H(z)} \tag{82}$$

is the discrete-time loop gain of the PLL. The right-most expression in (81) implies that if $\delta = 1$, then $p[n]$ does not depend on $\hat{e}_q[n]$, but if $\delta \neq 1$, then $\hat{e}_q[n]$ leaks into the DLF input. As the power of $\hat{e}_q[n]$ is much larger than that of $e_{qr}[n]$ in practice, this can be problematic, particularly for high PLL bandwidths. For instance, in the DMRO-based PLL presented in [10], $A = 1$ and $N_R = 13$, so $\Delta_r = 1/26$ and the power of $\hat{e}_q[n]$ is approximately 28 dB larger than that of $e_{qr}[n]$ (recall that $\Delta_c = 1$). In this case, (81) with $A = 1$ implies that a ΔΣ FDC forward path gain error corresponding to $\delta^{-1} = 1 \pm 0.08$ would introduce an additional error component that depends on $\hat{e}_q[n]$ with approximately double the power of the component that depends on $e_{qr}[n]$. This would significantly increase the PLL output phase noise PSD at offset frequencies where the ΔΣ FDC quantization error contribution dominates those of the other noise sources.

B. Proposed Digital Gain Calibration Technique

The proposed digital gain calibration technique is a modification of the ΔΣ FDC's RPC, the details of which are shown in Fig. 6, where $\mathrm{sgn}(x) = 1$ if $x \geq 0$ and –1 otherwise. To minimize clutter, Fig. 21 only shows a portion of the RPC. The modifications that implement the gain calibration technique are contained entirely within the dashed contour shown in the figure, and except for these modifications the ΔΣ FDC is identical to that shown in Fig. 17(b).

The gain calibration technique consists of a signed least-mean square (LMS)-like loop with gain $K$ and output $g_n$, which digitally compensates for forward path gain error caused by $\delta \neq 1$. It is based on the following two results that can be derived from an analysis similar to that presented in [11]. The first result is that $d_R[n]$ in Fig. 17(b) can be multiplied by a constant factor $g_n$ to compensate for non-ideal DMRO frequencies. In the presence of this factor, the transfer function from $\hat{e}_q[n]$ to $p[n]$ is given by

$$\left(1-g_n\delta^{-1}\right)z^{-2}\frac{\left(1-z^{-1}\right)}{H_g(z)}\frac{1}{1+T_g(z)}, \tag{83}$$

where $H_g(z)$ is given by (80) with $\delta^{-1}$ replaced by $g_n\delta^{-1}$ and $T_g(z)$ is given by (82) with $H_g(z)$ and $g_n\delta^{-1}$ instead of $H(z)$ and $\delta^{-1}$, respectively. It follows from (83) that $g_n = \delta$ makes the contribution to $p[n]$ from $\hat{e}_q[n]$ equal to zero. The second result is that $g_n(d_R[n] - d_R[n-1])$ equals $-v[n-1] - \alpha$ plus zero-mean error when $g_n$ is equal to its ideal value of $\delta$, i.e., $\delta(d_R[n] - d_R[n-1]) = -v[n-1] - \alpha$ plus zero-mean error.

These observations suggest that, provided it is stable, the gain calibration feedback loop ramps $g_n$ up or down until it reaches the point where the input to the accumulator with gain $K$ is zero-mean noise. Fig. 21 implies that this happens when $g_n(d_R[n] - d_R[n-1]) + v[n-1] + \alpha$ is

uncorrelated with $v[n-1]+\alpha$. Therefore, to the extent that the error component in $\delta(d_R[n]-d_R[n-1])$ is uncorrelated with $v[n-1]+\alpha$, the system converges to the ideal value of $g_n = \delta$.

In addition to preventing $\hat{e}_q[n]$ from leaking into the PLL loop, the proposed calibration technique also allows for the use of DMRO topologies with coarse frequency tuning or no tuning at all. This not only simplifies the design and implementation of the DMRO, but also simplifies the system as it renders feedback loops that tune $f_{\text{high}}$ and $f_{\text{low}}$ as a function of $f_{\text{PLL}}$ unnecessary.

The proposed calibration technique somewhat increases the digital complexity of the ΔΣ FDC, but typically does not add significantly to the PLL's overall power or area consumption. For example, in the PLL implementation described in Section V, both $d_R[n]$ and $g_n$ have 10 fractional bits, so 20 fractional bits are required to represent $g_n d_R[n]$. Given that $\alpha$ also has 20 fractional bits, the gain calibration technique negligibly increases the number of fractional bits required to represent the RPC accumulator's input. Therefore, as the calibration technique's digital LMS loop is relatively simple, the $f_{\text{ref}}$-rate digital multiplier prior to the RPC's accumulator represents most of the calibration technique's added complexity.

### C. Convergence Analysis

Fig. 22 shows the block diagram of Fig. 5(a) modified to include the gain calibration technique, where $\varepsilon_n$ is the error in $g_n$ at sample time $n$, which is defined as

$$\varepsilon_n = \delta^{-1} g_n - 1. \tag{84}$$

For any fixed value of $g_n$ and neglecting $e_{qr}[n]$, Fig. 22 implies that $a[n]$ is equal to $(1+\varepsilon_n)e[n]$, because the two $1-z^{-1}$ blocks cancel the two accumulators in the path between $e[n]$ and $a[n]$. The gain calibration loop adds $v[n-1]+\alpha$, which is an estimate of $-e[n]$, to $a[n]$, and

multiplies the result by the sign of $v[n-1]+\alpha$ to obtain a measure of $\varepsilon_n$, $b[n]$, which is approximately equal to $-\varepsilon_n|e[n]|$.

More precisely, Fig. 22 and (84) imply that $e[n]$ is given by

$$e[n]=-v[n-1]-\alpha-e_{\mathrm{PLL}}[n], \tag{85}$$

and that $a[n]$ can be written as

$$a[n]=\left(1+\varepsilon_n\right)e[n]+\left(\varepsilon_n-\varepsilon_{n-1}\right)\sum_{i=0}^{n-1}e[i]+a_e[n], \tag{86}$$

where $a_e[n]$ is the contribution of $e_{qr}[n]$ to $a[n]$. Substituting (85) into (86), adding $v[n-1]+\alpha$ to the result, and then multiplying the resulting expression by $\mathrm{sgn}(v[n-1]+\alpha)$ yields

$$b[n]=-\varepsilon_n\left|v[n-1]+\alpha\right|+b_e[n], \tag{87}$$

where $b_e[n]$ is error that arises from the error in the estimate of $e[n]$, the contribution of $e_{qr}[n]$, and $g_n$ not being constant.

Fig. 22 together with (84) and (87) further imply that

$$\varepsilon_{n+1}=\left(1-\delta^{-1}K\left|v[n-1]+\alpha\right|\right)\varepsilon_n+\delta^{-1}Kb_e[n], \tag{88}$$

from which it follows that

$$\bar{\varepsilon}_{n+1}=\left(1-\delta^{-1}K\left|v[n-1]+\alpha\right|\right)\bar{\varepsilon}_n+\delta^{-1}K\bar{b}_e[n], \tag{89}$$

where $\bar{\varepsilon}_n$ and $\bar{b}_e[n]$ are the expected values of $\varepsilon_n$ and $b_e[n]$, respectively, conditioned to the sequence $v[n-1]$.

When $\delta\neq 1$, the self-dithering property of the ΔΣ FDC is not perfect, so $e_{qr}[n]$ can be correlated with $\mathrm{sgn}(v[n-1]+\alpha)$. Furthermore, it follows from Fig. 16 that

$$p[n] = -e_q[n] + e_q[n-1] + \sum_{i=0}^{n} y[i] + \alpha \tag{90}$$

so Fig. 20(b) and $v[n-1] = y[n-2]$ imply that the term $\psi_{\mathrm{PLL}}[n] = \theta_{\mathrm{PLL}}(\tau_n) - \theta_{\mathrm{PLL}}(\tau_{n-1})$ in $e_{\mathrm{PLL}}[n]$, which depends on a low-pass filtered version of $p[n]$, can also be correlated with $\mathrm{sgn}(v[n-1] + \alpha)$. As $b_e[n]$ depends on both $e_{qr}[n]$ and $e_{\mathrm{PLL}}[n]$, it follows from these observations that $\bar{b}_e[n]$ in (89) is not zero, so $b_e[n]$ biases the LMS loop and causes $g_n$ to converge to a value that is slightly different than $\delta$. However, numerous simulations run by the authors suggest that the magnitude of this bias is sufficiently small that $\bar{b}_e[n]$ can be neglected in the remainder of the analysis. Hence, (89) reduces to

$$\bar{\varepsilon}_{n+1} = \left(1 - \delta^{-1} K \left| v[n-1] + \alpha \right|\right) \bar{\varepsilon}_n. \tag{91}$$

The recursive application of (91) to itself yields

$$\bar{\varepsilon}_{n+1} = \prod_{i=0}^{n} \left(1 - \delta^{-1} K \left| v[i-1] + \alpha \right|\right) \bar{\varepsilon}_0, \tag{92}$$

which implies that, on average, $\varepsilon_{n+1}$ tends to zero provided $K$ is chosen such that

$$\lim_{n \to \infty} \prod_{i=0}^{n} \left(1 - \delta^{-1} K \left| v[i-1] + \alpha \right|\right) = 0. \tag{93}$$

As $|v[n-1] + \alpha|$ is bounded and is regularly non-zero, (93) is easy to satisfy in practice.

D. Gain Calibration Technique for CP-Based ΔΣ FDCs

The digital gain calibration technique shown in Fig. 21 can be modified to apply to the CP-based ΔΣ FDC shown in Fig. 23(a) [8], [9], [12]. The modified version of the digital gain calibration technique is shown in Fig. 23(b). Its implementation details are almost identical to those in Fig. 21, except for an extra $1 - z^{-1}$ block. In the CP-based ΔΣ FDC, the CP and

subsequent analog-to-digital converter (ADC) play the same role as the DMRO in the DMRO-based ΔΣ FDC. The DMRO-based ΔΣ FDC already has a $1-z^{-1}$ block following the DMRO, which is needed as part of the circuitry that makes it possible to read out the DMRO's phase error [10], but this block is not necessary in the CP-based ΔΣ FDC. The additional $1-z^{-1}$ block in Fig. 23(b) compensates for the absence of a $1-z^{-1}$ block at the output of the ADC in the CP-based ΔΣ FDC architecture.

## V. SIMULATION RESULTS

This section presents results from bit-exact, event-driven, behavioral C code simulations of the fractional-*N* PLL of Fig. 16 with the proposed ΔΣ FDC and digital gain calibration technique. All digital operations were simulated with fixed-point arithmetic. The PLL's DLF consists of a loop gain multiplier with gain $K_M$, two single-pole IIR stages with poles at $\lambda_0$ and $\lambda_1$, and a proportional-integral stage with proportional path gain $K_P$ and integral path gain $K_I$. Its transfer function is given by

$$L(z) = K_M \left( K_P + \frac{K_I}{1-z^{-1}} \right) \prod_{i=0}^{1} \frac{\lambda_i}{1-(1-\lambda_i)z^{-1}}. \tag{94}$$

The parameters used for the simulations are listed in Table 1.

Fig. 24 shows the simulated PLL phase noise PSD with and without gain calibration enabled for four different combinations of PLL bandwidth and ΔΣ FDC forward path gain. For each case it also shows the theoretical PLL phase noise PSD with $g_n = \delta$ as a black dashed curve, and the theoretical combined contribution to the PLL phase noise from $e_{qr}[n]$ and $\hat{e}_q[n]$

as colored dashed curves.[10] As demonstrated in the figure, the higher the PLL bandwidth, the more sensitive the PLL's phase noise is to the ΔΣ FDC quantization error, which becomes more dominant when less filtering is applied to $p[n]$. Consequently, deviations of $\delta^{-1}$ from its ideal value of 1 cause a significant degradation of the PLL phase noise PSD for high PLL bandwidth settings.

Given that $N_R = 31$, the power of $\hat{e}_q[n]$ is approximately 36 dB larger than that of $e_{qr}[n]$. Therefore, in the absence of gain correction, it follows from (81) with $A = 1$ that the power of the additional quantization error component seen by the PLL loop is approximately 22 dB and 16 dB higher than that of the $e_{qr}[n]$ component for $\delta^{-1} = 0.8$ and $\delta^{-1} = 1.1$, respectively. This is supported by the simulation results shown in Fig. 24(a) and Fig. 24(c), where the spot phase noise degradation at a 3 MHz offset frequency is approximately 20 dB and 15 dB, respectively.

Fig. 25 shows $\varepsilon_n$ versus time for several values of $K$ with a PLL bandwidth of 1 MHz and $\delta = 0.8$.[11] Equation (92) with $\varepsilon_0$ in place of $\overline{\varepsilon_0}$, i.e.,

$$\prod_{i=0}^{n}\left(1-\delta^{-1}K\left|v[i-1]+\alpha\right|\right)\varepsilon_0, \tag{95}$$

is also plotted (as a dashed curve) for each value of $K$ to provide a comparison baseline and show that the evolution of $g_n$ follows the trend predicted by the analysis in Section IV-C. The simulated PLL phase noise PSD after $g_n$ converged was nearly identical to that shown in Fig. 24(a) with gain calibration enabled. In the $K = 2^{-2}$ case, however, the total integrated jitter increased slightly to 688 $\text{fs}_{\text{rms}}$ because of the relatively large variance of $\varepsilon_n$. As shown in the

[10] The curves corresponding $e_{qr}[n]$ and $\hat{e}_q[n]$ were generated under the assumption that both sequences are white. However, the sequences are not necessarily white if $\delta \neq 1$, which is why the simulated curves in Fig. 24 deviate somewhat from their respective theoretical predictions, particularly in the $\delta^{-1} = 0.8$ case.

[11] The resolution of the gain calibration technique's accumulator was limited to 1 integer bit and 36 fractional bits, but its output, $g_n$, was truncated to have only 10 fractional bits to reduce hardware complexity.

figure's inset, $\varepsilon_n$ crosses the −0.01 mark for the first time in about 50 reference periods (1.9 $\mu$s) and 400 reference periods (15.4 $\mu$s) for $K = 2^{-2}$ and $K = 2^{-6}$, respectively, and the absolute value of the mean error after convergence is lower than 0.043% of $\delta$ in all cases.

As in most LMS-like algorithms, the choice of $K$ represents a tradeoff between convergence speed and the error variance of $g_n$ [20], [21]. Although it might be possible to derive a closed-form expression that quantifies this tradeoff for the proposed calibration technique, the authors currently choose the value of $K$ based on simulation results.

Fig. 26 shows normalized histograms of $\tau_n - t_n - T_{\bar{u}}$, where $T_{\bar{u}}$ was calculated using (73) , for both the original ΔΣ FDC and the proposed ΔΣ FDC. The $u(t)$ pulse widths were measured for over one million reference periods after the gain calibration had converged with $K = 2^{-9}$. The 1 MHz-bandwidth set of parameters with $\delta = 0.8$ was used for the simulations in Fig. 26(a) and Fig. 26(b), whereas the same parameters except for $\alpha$, which was set to 0.401008987426758, were used for the simulations in Fig. 26(c) and Fig. 26(d).

Although (76) and (78) do not show an explicit dependence of the $u(t)$ pulse-width span on $\alpha$ in either ΔΣ FDC version, it follows from (67) and Fig. 17 that different ΔΣ FDC output levels are exercised for different values of $\alpha$. Accordingly, different values of $\alpha$ cause $e_q[n]$ to take different values with higher probability than others, which affects the histogram shapes shown in Fig. 26 but not the maximum $u(t)$ pulse-width.

As explained in Section III-B, the span of the $u(t)$ pulse-width in the proposed ΔΣ FDC is approximately three times smaller than that of the $u(t)$ pulse-width in the original ΔΣ FDC, which is supported by the simulation results shown in Fig. 26. As shown in Fig. 26(a), the span of $u(t)$ in the original ΔΣ FDC goes from $-3T_{\mathrm{PLL}}$ to $3T_{\mathrm{PLL}}$, although it reaches the extremes

values only rarely. As demonstrated by the results in Fig. 26(c), the span is about $5T_{PLL}$ for a larger value of $\alpha$, and the extreme values in this case (i.e., around $-2.4T_{PLL}$ and $2.6T_{PLL}$) are reached with higher probability compared to Fig. 26(a). Conversely, as shown in Fig. 26(b) and Fig. 26(d), the proposed architecture's $u(t)$ pulse-width span does not vary significantly with $\alpha$, and as suggested by (78), it is approximately limited to $2T_{PLL}$.

## VI. CONCLUSION

This paper presents all-digital enhancements of digital fractional-$N$ PLLs based on ΔΣ FDCs. The enhancements comprise an improved DMRO-based ΔΣ FDC architecture and a digital background gain calibration technique. The former reduces the span of the PFD output pulse-width and significantly relaxes the timing constraints imposed on the ΔΣ FDC's digital portion and divider, which makes the system amenable to simpler divider topologies and higher-frequency reference signals. The latter compensates for non-ideal DMRO frequencies in the digital domain, thereby facilitating the use of simple DMRO topologies with fixed values of $f_{high}$ and $f_{low}$, and improving the phase noise performance of high-bandwidth PLLs.

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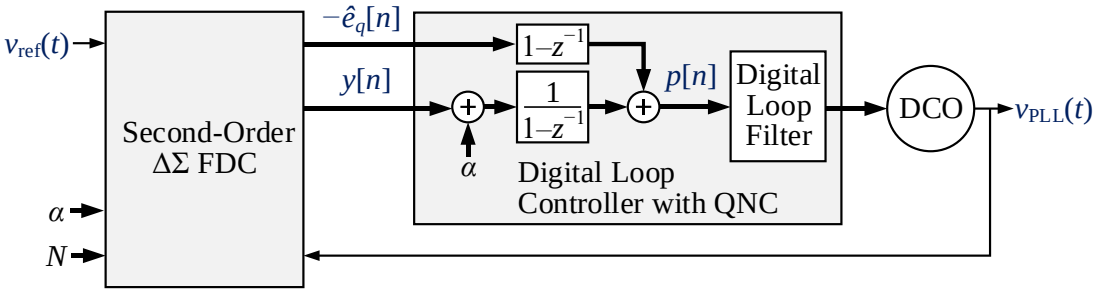


Figure 16: High-level block diagram of a second-order ΔΣ FDC-based digital fractional-*N* PLL with quantization noise cancellation (QNC).

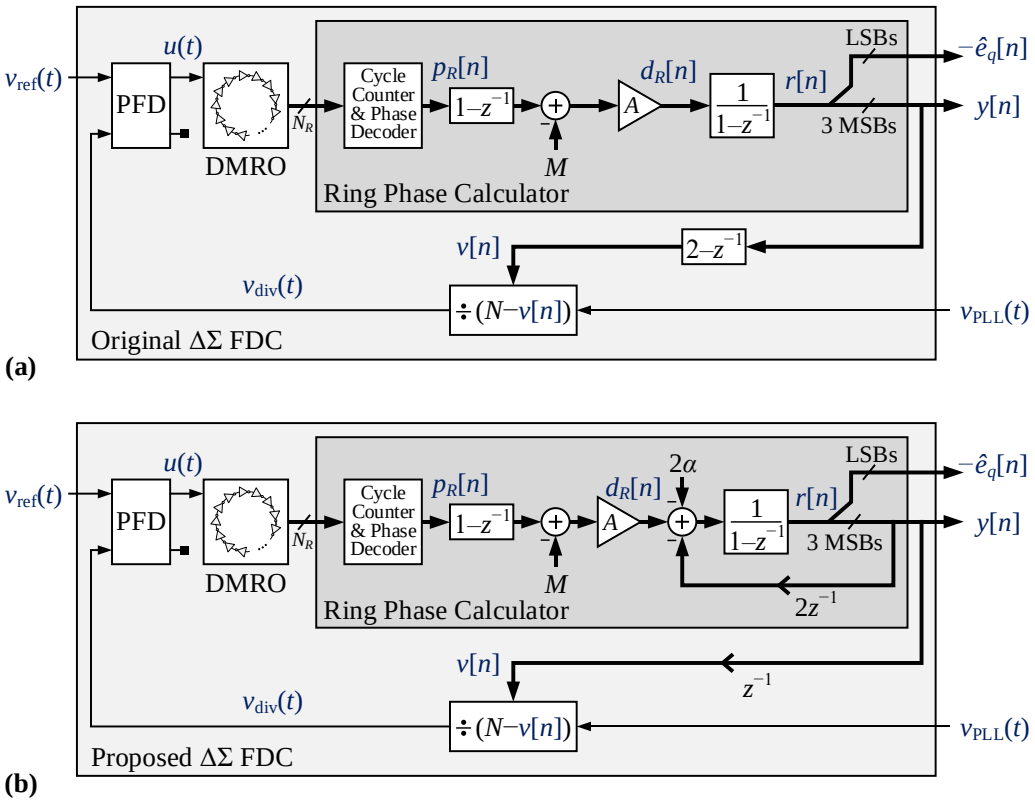


Figure 17: (a) Simplified block diagram of the DMRO-based ΔΣ FDC described in [11], and (b) simplified block diagram of the proposed ΔΣ FDC.

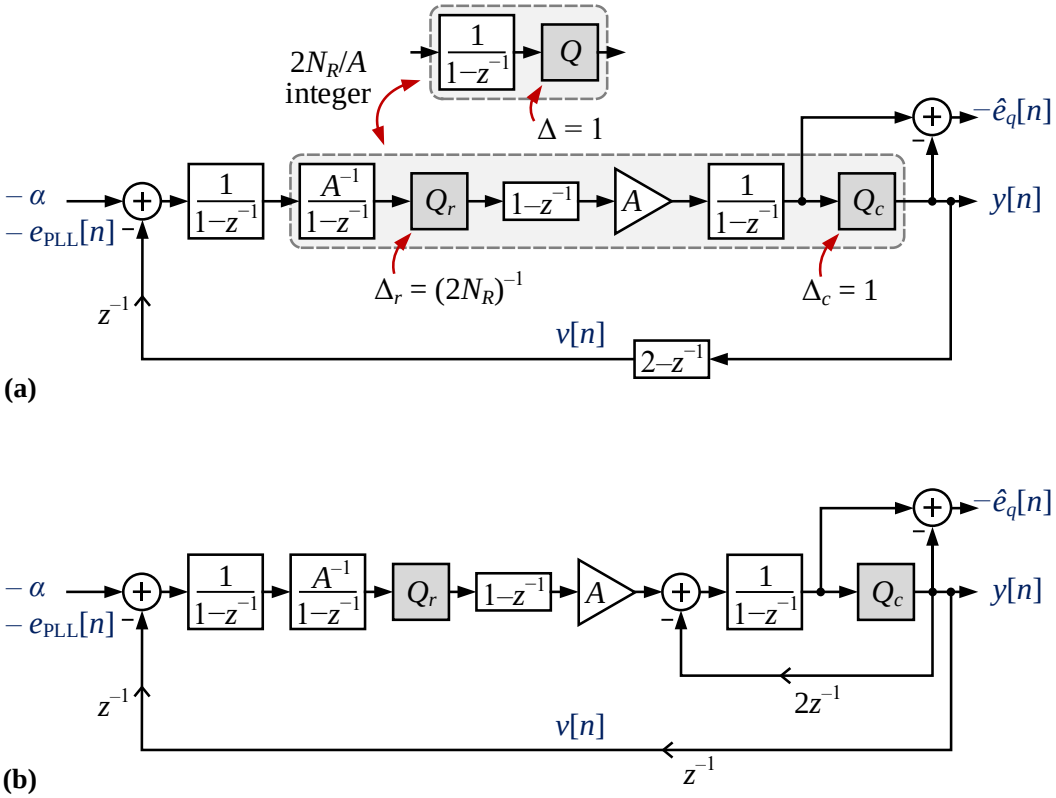


Figure 18: Signal processing equivalents of the ΔΣ FDCs shown in Fig. 17(a) and Fig. 17(b) when they are locked.

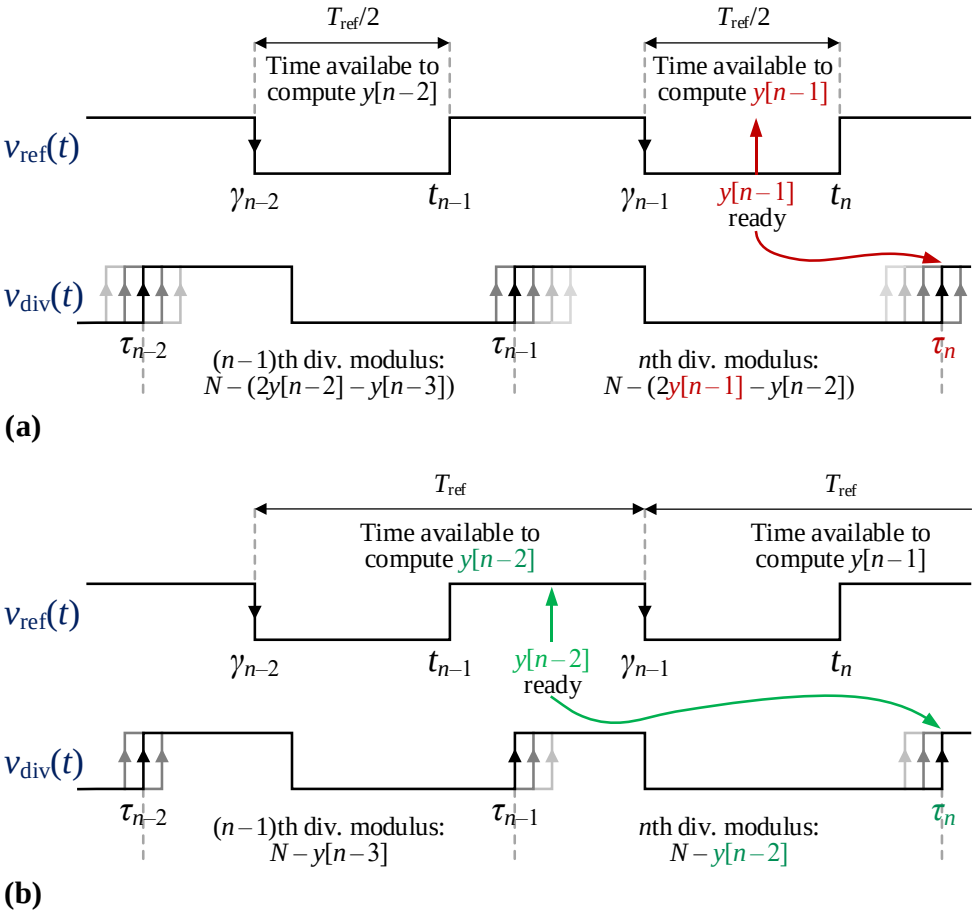


Figure 19: Example timing diagram of (a) the original ΔΣ FDC and (b) the proposed ΔΣ FDC.

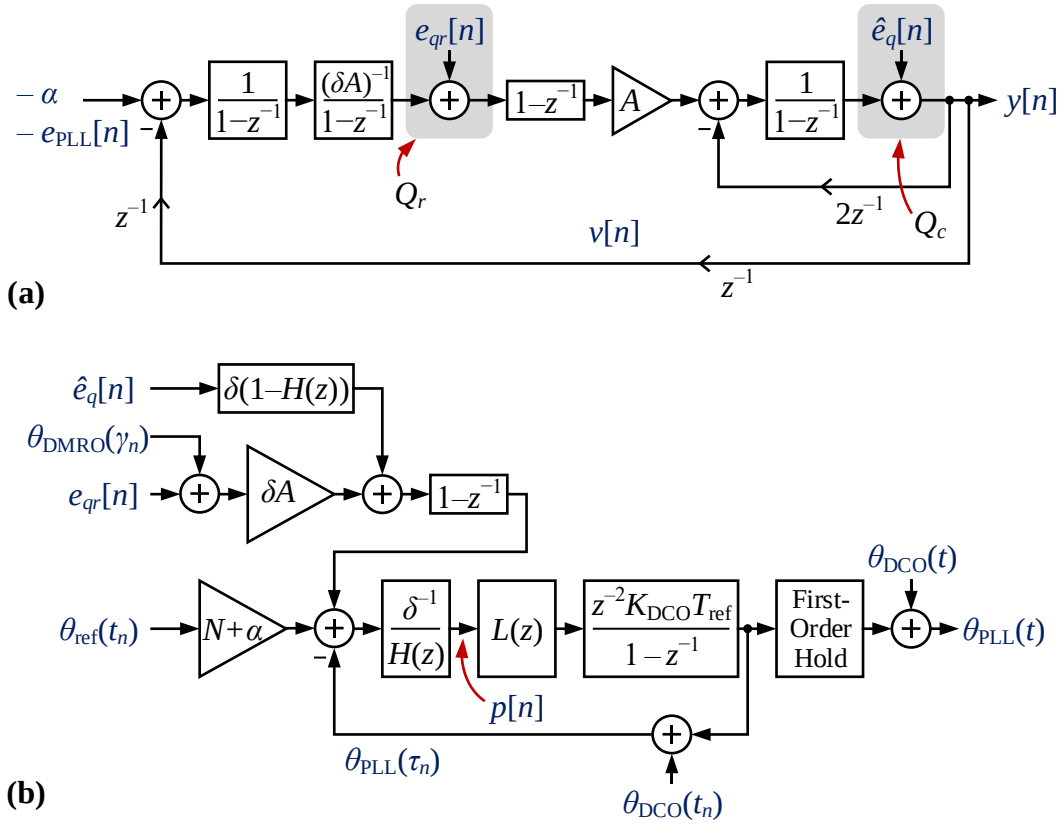


Figure 20: (a) Behavioral model of the proposed ΔΣ FDC with (79), where $Q_r$ and $Q_c$ are replaced by the additive error sources $e_{qr}[n]$ and $\hat{e}_q[n]$, respectively, and (b) linearized model of the ΔΣ FDC-based PLL shown in Fig. 16 with the proposed ΔΣ FDC and (79).

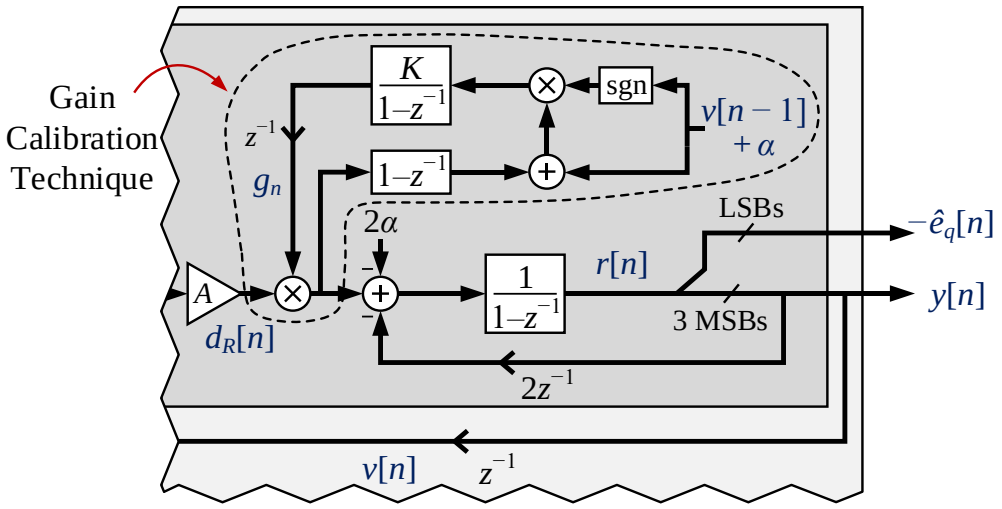


Figure 21: Digital gain calibration technique shown in the context of the proposed DMRO-based ΔΣ FDC architecture.

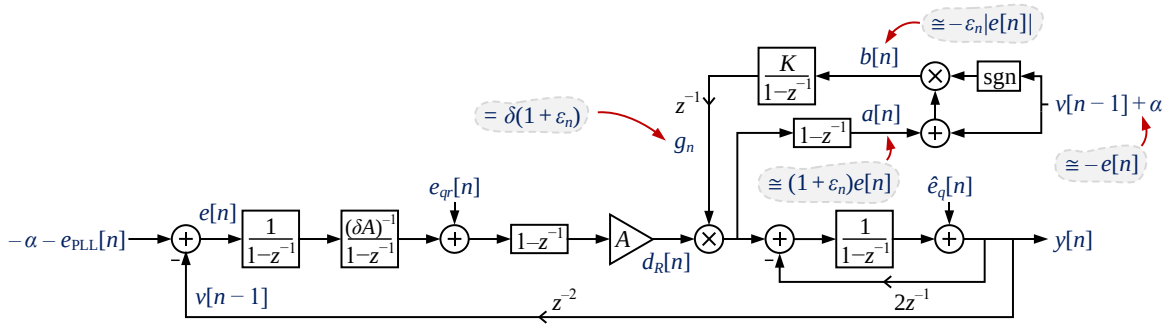


Figure 22: Rearranged version of the behavioral model shown in Fig. 20(a) modified to accommodate the proposed gain calibration technique.

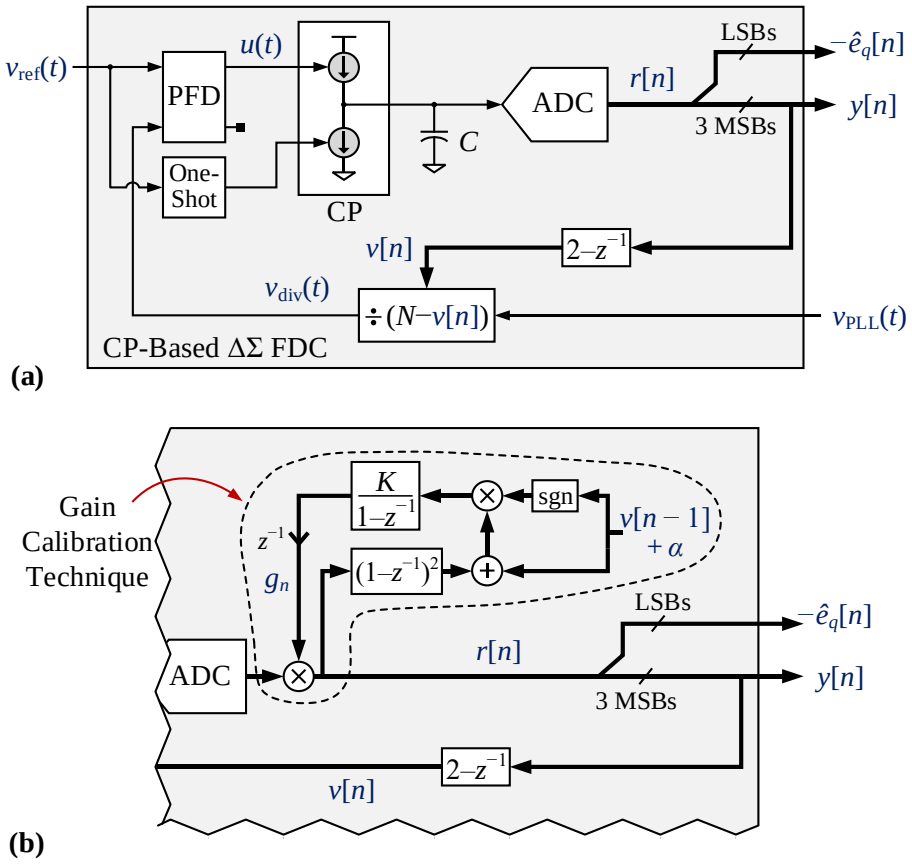


Figure 23: (a) Simplified block diagram of CP-based ΔΣ FDC, and (b) digital gain calibration technique shown in the context of the CP-based ΔΣ FDC architecture.

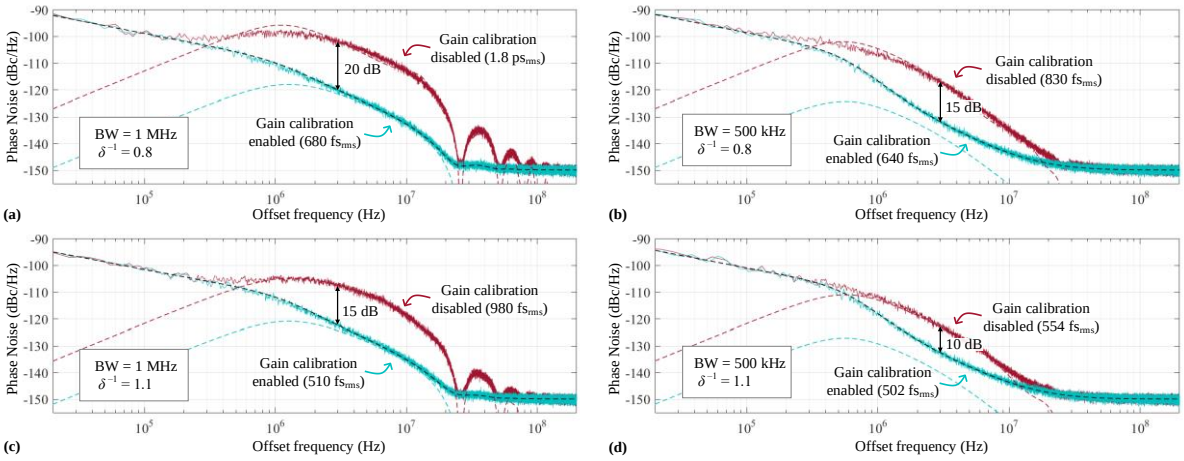


Figure 24: Simulated PLL phase noise PSD with and without gain calibration enabled for four combinations of PLL bandwidth (BW) and $\delta^{-1}$. The black and colored dashed curves correspond to the theoretical phase noise PSD for $g_n = \delta$ and the combined contribution to the PLL phase noise from $e_{qr}[n]$ and $\hat{e}_q[n]$, respectively.

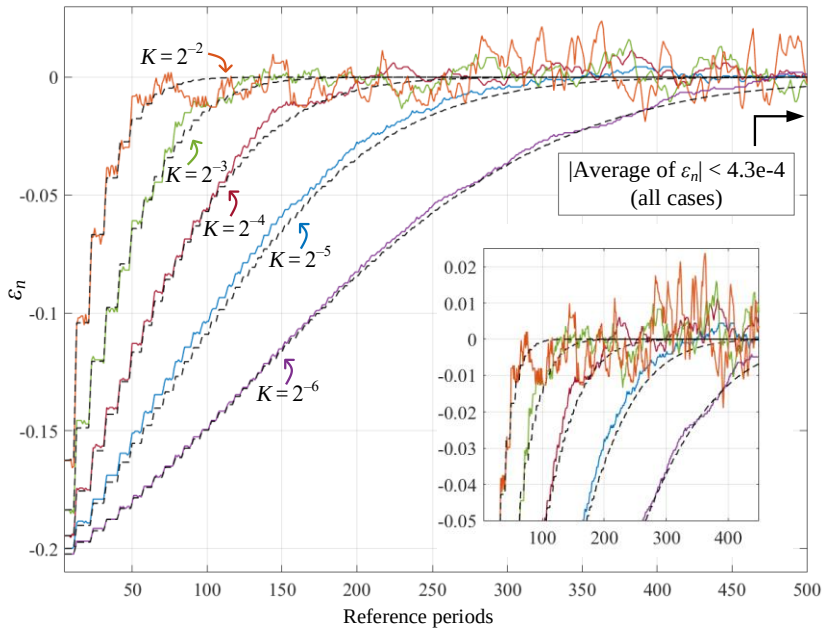


Figure 25: Sequence $\varepsilon_n$ as a function of $n$ for several values of $K$, where $\varepsilon_n$ calculated via (95) is plotted as a dashed curve for each case.

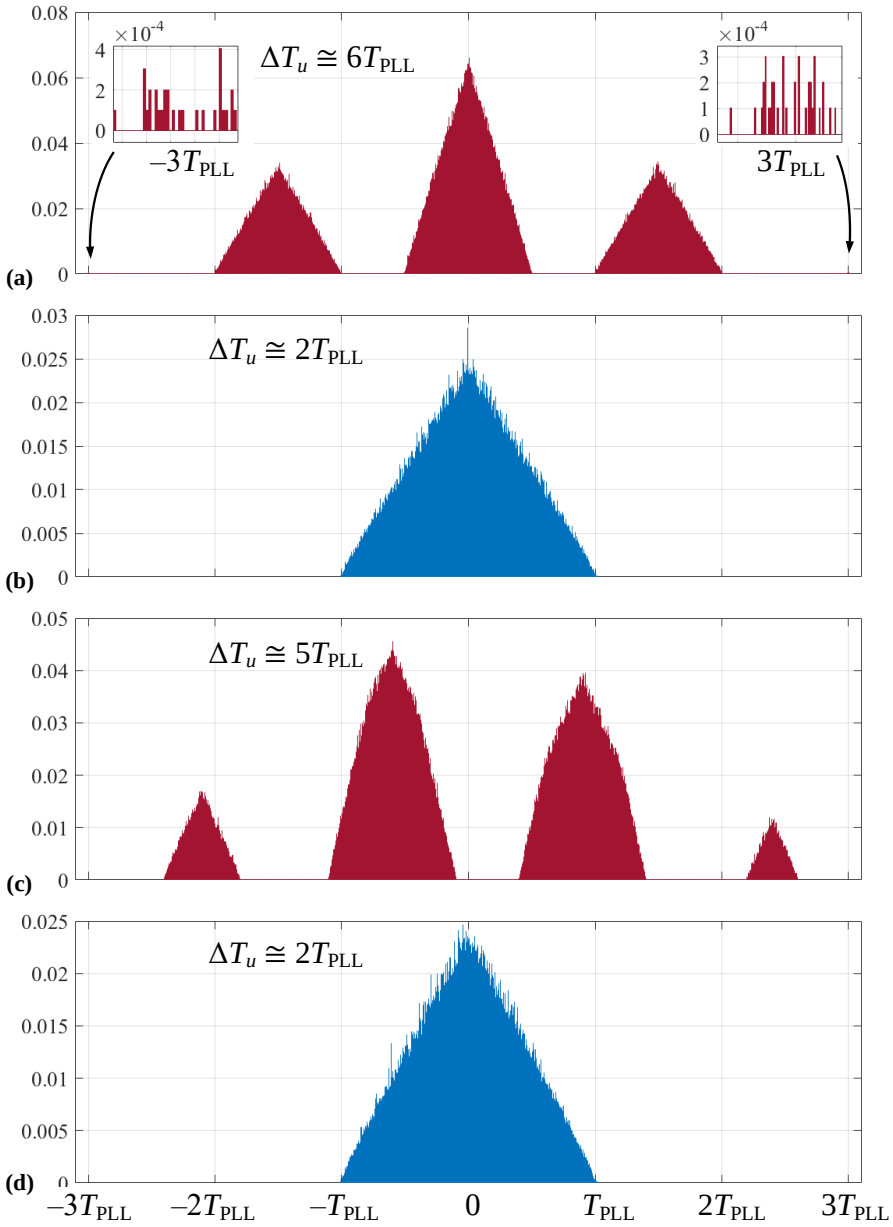


Figure 26: Normalized histogram of $u(t)$ pulse width minus $T_{\bar{u}}$ calculated via (73) for the original FDC [(a) and (c)] and the proposed FDC [(b) and (d)], where $\alpha$ = 0.001008987426758 for (a) and (b) and $\alpha$ = 0.401008987426758 for (c) and (d).

TABLES

Table 1: Parameters used for the simulation.

| Design Parameters | | Value | |
|---|---|---|---|
| Reference Source | Frequency, $f_{ref}$ | 26 MHz | |
| | Phase noise (white) | −155 dBc/Hz | |
| DCO | DCO gain, $K_{DCO}$ | 40 kHz | |
| | Phase noise [(1)] | −130, −125 and −150 dBc/Hz | |
| DMRO | Number of stages, $N_R$ | 31 | |
| | Frequencies, $f_{low}$, $f_{high}$ | 150 MHz, 3.0 GHz (nominal) | |
| | | 225 MHz, 2.5 GHz ($\delta^{-1} = 0.8$) | |
| | | 142 MHz, 3.3 GHz ($\delta^{-1} = 1.1$) | |
| | Phase noise [(1)] | −99, −109 and −150 dBc/Hz | |
| FDC | Fixed count, $M$ | 40 | |
| | $A$ | 1 | |
| DLF | Loop gain multiplier, $K_M$ | 1.5 | |
| | Proportional gain, $K_P$ | $2^6$ | $2^5$ |
| | Integral gain, $K_I$ | $2^{-2}$ | $2^{-4}$ |
| | IIR poles, $\lambda_0$, $\lambda_1$ | $2^{-1}$, $2^0$ | $2^{-2}$, $2^{-1}$ |
| PLL Settings | Integer multiplier, $N$ | 110 | |
| | Fractional multiplier, $\alpha$ | 0.001008987426758 | |
| | Output frequency, $f_{PLL}$ | 2.86 GHz | |
| | Loop bandwidth | 1 MHz | 500 kHz |

[1] $1/f^3$, $1/f^2$ and white phase noise components at 1 MHz offset.

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# CHAPTER 3

# SPECTRAL BREATHING AND ITS MITIGATION IN DIGITAL FRACTIONAL-*N* PLLS

**Abstract**— Although digital phase-locked loops (PLLs) offer several advantages over their analog counterparts, they suffer from a major disadvantage that is rarely mentioned in published papers. The disadvantage, known as spectral breathing, is caused by component mismatches among the frequency control elements within a PLL's digitally-controlled oscillator (DCO). The mismatches introduce DCO frequency modulation nonlinearity which fluctuates and, therefore, causes erratic variations in the PLL's measured phase noise spectrum as the DCO's center frequency drifts. The phenomenon is called spectral breathing because the measured phase noise spectrum tends to slowly swell and contract over time as if taking breaths of air. During these breaths, the PLL's phase noise often becomes severely degraded. This paper presents an experimental demonstration of the spectral breathing phenomenon and its solution in a digital fractional-*N* PLL. The demonstrated solution is a multi-rate dynamic element matching technique and a mismatch-noise cancellation technique that together eliminate spectral breathing.

## I. INTRODUCTION

Digital fractional-*N* phase-locked loops (PLLs) offer several advantages over analog PLLs such as lower loop filter circuit area and compatibility with highly-scaled CMOS IC

technology [1]–[14]. However, unlike their analog counterparts, digital PLLs suffer from a problem called *spectral breathing* which can significantly degrade phase noise performance.

Spectral breathing is the result of nonlinear frequency modulation caused by inevitable mismatches among the frequency control elements (FCEs) in a PLL's digitally-controlled oscillator (DCO) [15]. Flicker noise inevitably causes the DCO's center frequency to drift over time, so different FCEs are exercised as the PLL adjusts the DCO's input sequence to compensate for the drift. This causes the DCO's frequency modulation nonlinearity and, therefore, the PLL's measured phase noise spectrum to swell up from time to time as if taking breaths of air.

The effect is particularly significant in the large percentage of digital PLLs that use a digital delta-sigma (ΔΣ) modulator to oversample the fractional part of the DCO input. In such PLLs, the ΔΣ modulator drives a bank of FCEs called the *fractional FCE bank* and the integer part of the DCO input drives a separate bank of FCEs called the *integer FCE bank*. The fractional FCE bank's FCEs are exercised many times per reference period because they are driven by the oversampling ΔΣ modulator. In contrast, the integer FCE bank's FCEs are exercised at most once per reference period because they are driven directly by the integer part of the DCO's input sequence. Accordingly, mismatches within the integer FCE bank are the main problem; error from FCE mismatches within the fractional FCE bank is spread over a much larger frequency range and, thus, contributes much less to the DCO's phase noise than error from FCE mismatches within the integer FCE bank.

Perhaps because the problem is not visible when measurements are restricted to time periods during which the integer FCE bank input bits do not change, it is seldom mentioned in

the published literature. Nevertheless, in practice the integer FCE bank input bits do change, at least over time periods of several seconds because of the DCO's center frequency drift, so the problem is significant in applications.

To the knowledge of the authors, the phenomenon was first reported and explained, although not yet named, in [2]. As the PLL presented in [2] uses the DCO frequency control method described above which was already well-known and widely-used at the time, the authors of [2] were surprised to find that FCE mismatches caused the PLL's measured phase noise spectrum to significantly vary over time.

Apart from applying dynamic element matching (DEM) clocked at the ΔΣ modulator output rate to all the FCEs, which would be prohibitively power-hungry among other issues, only three solutions have been proposed to date that mitigate spectral breathing [15]. An offline calibration technique is proposed in [16] and [17] to compensate for FCE mismatches, but the technique requires several minutes to complete. A digital integer-boundary avoider circuit prior to the DCO is proposed in [3], yet the technique is only effective in cases where the integer FCE bank input bits change relatively infrequently. To the authors' knowledge, the only published comprehensive solution is the combination of a multi-rate DEM (MR-DEM) technique and a mismatch-noise cancelation (MNC) technique [15].

This paper presents a fractional-*N* digital PLL IC that incorporates the MR-DEM and MNC techniques to avoid spectral breathing. In addition to providing the first experimental demonstration of the techniques proposed in [15], it presents implementation details, refinements, and practical observations that are not presented in [15].

# II. BACKGROUND INFORMATION

## A. Conventional DCO Frequency Control Technique

Most fractional-$N$ digital PLLs have the general structure shown in Fig. 27(a), which consists of a phase-error-to-digital converter (PEDC), a digital loop filter (DLF), and a DCO. The PLL's input, $v_{\text{ref}}(t)$, is generated by a reference oscillator not shown in the figure and the PLL's output, $v_{\text{PLL}}(t)$, ideally is periodic with frequency $f_{\text{PLL}} = (N + \alpha)f_{\text{ref}}$, where $f_{\text{ref}}$ is the reference oscillator frequency, $N$ is a positive integer, and $\alpha$ is a fractional value. The PEDC generates an $f_{\text{ref}}$-rate sequence of the form $-\theta_{\text{PLL}}[n] + e_p[n]$, where $\theta_{\text{PLL}}[n]$ is the PLL's phase error and $e_p[n]$ represents the combined effect of all other errors. The PEDC output is filtered by the DLF, and the DLF output, $d[n]$, controls the DCO frequency.

The DCO's instantaneous frequency, $f_{\text{DCO}}(t)$, can be written as a fixed offset frequency plus $f_{\text{tune}}(t)$, where $f_{\text{tune}}(t)$ depends on the states of the DCO's FCEs. Ideally, $f_{\text{tune}}(t) = d[n_t]$, where $n_t = n$ over the $n$th period of the $f_{\text{ref}}$-rate clock that updates $d[n]$, so $n_t$ is a continuous function of time that takes on values $n = 0, 1, 2, 3, \ldots$ as $t$ increases. If $d[n]$ is represented as a $b$-bit two's complement code sequence and its least-significant bit (LSB) represents a frequency step of $\Delta$, then, $d[n_t] = (-2^{b-1}d_{b-1}[n_t] + 2^{b-2}d_{b-2}[n_t] + \ldots + 2^0 d_0[n_t])\Delta$, where $d_i[n_t]$ is the $i$th bit of the $d[n_t]$ code for $i = 0, 1, \ldots, b-1$. In principle, the DCO could be implemented with $b$ FCEs, where the $i$th FCE increases or decreases $f_{\text{DCO}}(t)$ by $2^i\Delta$ whenever the FCE's input bit changes from 0 to 1 or 1 to 0, respectively. In this case, the input to the $i$th FCE would be $d_i[n_t]$ for $i = 0, 1, \ldots, b-2$, and $1 - d_i[n_t]$ for $i = b-1$. Unfortunately, in most PLLs this would require FCEs with impractically small frequency steps.

Fig. 27(b) shows an example configuration of a DCO control technique that is widely used to circumvent this problem [1]. In this example, the minimum practical FCE frequency step is $\Delta_{min} = 2^8\Delta$, and $d[n]$ is decomposed into an integer part, $d_I[n]$, that takes on values that are multiples of $\Delta_{min}$, and a fractional part, $d_F[n]$, that takes on values in the range $\{0, \Delta, 2\Delta, \ldots, \Delta_{min} - \Delta\}$. The $d_I[n]$ sequence drives an *integer FCE bank* directly. The $d_F[n]$ sequence is oversampled at a rate of $f_{fast} > f_{ref}$ and re-quantized by a digital $\Delta\Sigma$ modulator. The $\Delta\Sigma$ modulator output is converted to a thermometer code that drives a *fractional FCE bank* which consists of four FCEs, each with a frequency step of $\Delta_{min}$. Thus, $f_{tune}(t)$ is equal to $d[n_t]$ plus $f_{fast}$-rate highpass-shaped $\Delta\Sigma$ modulator quantization error that is lowpass filtered by the DCO.

Ideally, the contribution to $f_{DCO}(t)$ from the $i$th FCE instantaneously increases or decreases by $\Delta_i$ when the FCE's input bit changes from 0 to 1 or 1 to 0, respectively, where $\Delta_i$ is the FCE's nominal frequency step. In practice, non-ideal circuit behavior causes the FCE's frequency transitions to be non-instantaneous, and component mismatches cause its frequency step to deviate somewhat from $\Delta_i$ as illustrated in Fig. 27(c). These nonidealities introduce input-code-dependent DCO frequency modulation nonlinearity. As illustrated in Fig. 27(c), this causes the PLL's phase noise spectrum to vary over time as the DCO's center frequency, and, hence, $d_I[n]$, drift [15].

## B. MR-DEM and MNC Techniques

Fig. 28(a) shows a high-level diagram of a digital fractional-*N* PLL that includes the MR-DEM and MNC techniques. The system is similar to that shown in Fig. 27(a), except for the addition of two digital blocks: an MR-DEM encoder that is built into the DCO and an MNC logic block.

The MR-DEM encoder is based on the same principle as mismatch-shaping DEM encoders [18]. The idea is to shuffle the error introduced by FCE mismatches, so that $f_{tune}(t)$ equals a scaled version of $d[n_t]$ plus additive highpass-shaped error that depends on pseudo-random digital sequences that are known to the system because they are generated within the MR-DEM encoder. This additive error has both $f_{ref}$-rate and $f_{fast}$-rate components. Most of the $f_{ref}$-rate error component in $f_{tune}(t)$ is canceled by the MNC technique, which applies a least-mean-square (LMS)-like algorithm to compute digital coefficients with which it forms a correction sequence, $e_{MNC}[p]$, that is injected into the MR-DEM encoder. The $f_{fast}$-rate error component is not canceled by the MNC technique, but its high sample-rate in conjunction with its highpass spectral shape ensures that most of its contribution to the DCO's phase noise gets suppressed by the DCO's first-order lowpass frequency-modulation-to-phase-noise transfer function.

Fig. 28(b) shows the details of the MR-DEM technique for an example case where $d[n]$ has 16 bits. It consists of an MR-DEM encoder that comprises a slow DEM encoder, a second-order digital ΔΣ modulator, and a fast DEM encoder. The slow DEM encoder is a modified version of a conventional segmented DEM encoder, the details of which are described shortly, and the fast DEM encoder is a conventional non-segmented DEM encoder. The slow DEM encoder is clocked by the $f_{ref}$-rate clock signal, $clk_{ref}(t)$, whereas the MR-DEM encoder's fractional path, which consists of the digital ΔΣ modulator and the fast DEM encoder, is clocked by the $f_{fast}$-rate clock signal, $clk_{fast}(t)$.

The signal processing details of the slow DEM encoder are shown in Fig. 29, where the Δ multiplication prior to the $x_f[n]$ output denotes that the LSB of $x_f[n]$ represents a frequency

step of Δ. The slow DEM encoder consists of 25 digital switching blocks (SBs), labeled $S_{k,r}$ for $k = 1, 2, \ldots, 16$ and $r = 1, 2, \ldots, 17$. The shaded SBs are called segmenting SBs, whereas the remaining SBs are called non-segmenting SBs. The functional details of each SB type are also shown in Fig. 29, where $c_{k,r}[n]$ is the input sequence of $S_{k,r}$. The outputs of each segmenting SB are $\frac{1}{2}(c_{k,1}[n] - 1 - s_{k,1}[n])$ and $1 + s_{k,1}[n]$, where $s_{k,1}[n]$, called a switching sequence, is 0 when $c_{k,1}[n]$ is odd and ±1 otherwise. The outputs of each non-segmenting SB are $\frac{1}{2}(c_{k,r}[n] - s_{k,r}[n])$ and $\frac{1}{2}(c_{k,r}[n] + s_{k,r}[n])$, where $s_{k,r}[n]$ is 0 when $c_{k,r}[n]$ is even and ±1 otherwise. Each switching sequence is zero-mean and has a highpass-shaped power spectral density that peaks at $f_{\text{ref}}/2$.

As explained in [15], in the absence of the MNC technique the MR-DEM encoder would cause

$$f_{\text{tune}}(t) \cong d[n_t] + \Delta \sum_{k,r} \delta_{k,r} s_{k,r}[n_t] + p_{\text{fast}}(t) \Delta \sum_{k,r} \gamma_{k,r}(t) \left( s_{k,r}[n_t - 1] - s_{k,r}[n_t] \right), \qquad (96)$$

where $\delta_{k,r}$ and $\gamma_{k,r}(t)$ are constant and $1/f_{\text{fast}}$-periodic waveforms, respectively, that depend only on FCE errors, and $p_{\text{fast}}(t)$ is a series of unit-amplitude, $1/f_{\text{fast}}$-width pulses that go high whenever $n_t$ changes.[12] As implied by (96), the MR-DEM technique causes $f_{\text{tune}}(t)$ to be a linear function of $d[n_t]$ at the expense of introducing two additive error terms. One of the error terms is caused by FCE static gain errors, i.e., mismatch-induced errors in the FCEs' frequency step-sizes. The other error term is inter-symbol interference (ISI) that results from non-instantaneous rise and fall frequency transients of individual FCEs [15].

The details of the MNC logic are shown in Fig. 30(a). It consists of 25 $s_{k,r}[n]$ residue estimators that each compute a correction sequence corresponding to one of the slow DEM

[12] The summation indices in (96) indicate the summation over all $k$ and $r$ values corresponding to the SBs within the slow DEM encoder.

encoder's switching sequences, and an adder that combines these sequences to form $e_{\mathrm{MNC}}[p]$. As shown in Fig. 30(b), each $s_{k,r}[n]$ residue estimator comprises two branches, one to compute the correction sequence associated with FCE static gain error, and another to compute the correction sequence associated with ISI error, hereafter referred to as the static-error and ISI-error correction branches, respectively.

As indicated in Fig. 30, the MNC logic block's output is

$$e_{\mathrm{MNC}}[p] = \Delta\sum_{k,r} a_{k,r}[n]s_{k,r}[n] + p_{\mathrm{fast}}(t)\Delta\sum_{k,r} b_{k,r}[n]\Big(s_{k,r}[n-1] - s_{k,r}[n]\Big), \tag{97}$$

where $a_{k,r}[n]$ and $b_{k,r}[n]$ are measures called MNC coefficients that correspond to $\delta_{k,r}$ and $\gamma_{k,r}(t)$, respectively. As explained in [15], the MNC coefficients converge such that $e_{\mathrm{MNC}}[p]$ is a sampled measure of the additive error terms in (96). As illustrated conceptually in Fig. 30(c), when injected into the DCO as shown in Fig. 28(b), $e_{\mathrm{MNC}}[p]$ largely prevents these terms from contributing to the DCO's phase noise.

## III. IMPLEMENTATION DETAILS

The MR-DEM and MNC techniques were implemented as modifications to the 6.5 GHz digital fractional-*N* PLL presented in [4]. As the underlying PLL is explained in detail in [4], only the additional implementation details relevant to the MR-DEM and MNC techniques are presented here.

### A. MR-DEM Encoder

The high-level details of the implemented MR-DEM encoder are identical to those shown in Fig. 28(b). The second-order digital ΔΣ modulator is implemented as an error

feedback structure to reduce its hardware complexity [19]. The fast DEM encoder is implemented as a 4-layer tree of non-segmenting SBs with first-order highpass-shaped switching sequences [20], [21]. The slow DEM encoder is implemented as shown in Fig. 31. The SBs within the slow and fast DEM encoders are identical to the adder-free SBs described in [22], except for a modification made in the slow DEM encoder's SBs for them to accommodate both white and first-order highpass-shaped switching sequences.

It follows from Fig. 29 that the slow DEM encoder bottom output, $x_f[n]$, is given by

$$\Delta\sum_{k=9}^{16} 2^{16-k}\, s_{k,1}[n], \tag{98}$$

which can be computed by combining the bottom outputs of $S_{16,1}$, $S_{15,1}$, … and $S_{9,1}$ as indicated in Fig. 29. However, in this work $x_f[n]$ is instead computed without using adders to reduce the block's hardware complexity. As explained shortly, the LSB, $c_{8,1\text{-LSB}}[n]$, of the input to $S_{8,1}$, $c_{8,1}[n]$, corresponds to a quantized version of $d_F[n]$, and its quantization error is proportional to (98). The proposed slow DEM encoder architecture takes advantage of this property to generate $x_f[n]$ by simply combining the bits of the $d_F[n]$ and $c_{8,1\text{-LSB}}[n]$ sequences as indicated in Fig. 31.

Fig. 31 implies that

$$x_f[n] = -2^8\left(1 - c_{8,1\text{-LSB}}[n]\right)\Delta + d_F[n], \tag{99}$$

and the SB signal processing operations shown in Fig. 29 imply that

$$c_{8,1}[n] = \frac{1}{2^8}\left(c[n] + 1 - 2^8 - \sum_{k=9}^{16} 2^{16-k}\, s_{k,1}[n]\right)\Delta. \tag{100}$$

As explained in [22], the segmenting SBs use negative-extra-LSB encoding, so $c_{8,1\text{-LSB}}[n]$ has a negative weight. This with the segmenting SB details presented in [22] implies that $c_{8,1\text{-LSB}}[n]$ is given by minus the right side of (100) with $c[n]$ replaced by $d_F[n]/\Delta$, i.e.,

$$c_{8,1\text{-LSB}}[n] = -\frac{1}{2^8}\left(\frac{d_F[n]}{\Delta} + 1 - 2^8 - \sum_{k=9}^{16} 2^{16-k} s_{k,1}[n]\right)\Delta. \tag{101}$$

Substituting (101) into (99) yields (98) plus a –1 offset. This offset is not a problem in practice because it is suppressed by a zero-frequency zero in the PLL's transfer function.

B. MNC Logic

The MNC logic implementation details are shown in Fig. 32. Each variable is represented in fixed-point, two's complement format, and its number of bits is specified via the notation $\{b_I, b_F\}$, where $b_I$ and $b_F$ are the numbers of integer and fractional bits, respectively. The braces and $b_F$ are omitted in cases where $b_F = 0$.

Each $s_{k,r}[n]$ residue estimator computes two sequences, $e_{k,r\text{-stat}}[n]$ and $e_{k,r\text{-ISI}}[n]$. The $e_{k,r\text{-stat}}[n]$ sequences are combined to form $e_{\text{MNC-stat}}[n]$, which corresponds to the first summation in (97), i.e., the part of $e_{\text{MNC}}[p]$ associated with FCE static gain errors. The $e_{k,r\text{-ISI}}[n]$ sequences are combined and then multiplied by the unit-amplitude pulse sequence, $p_{\text{fast}}(t)$, to form $e_{\text{MNC-ISI}}[p]$, which corresponds to the second summation in (97), i.e., the part of $e_{\text{MNC}}[p]$ associated with FCE ISI errors. Although not shown in Fig. 32, $e_{\text{MNC-stat}}[n]$ and $e_{\text{MNC-ISI}}[p]$ are combined at the ΔΣ modulator's input in Fig. 2(b) to form $e_{\text{MNC}}[p]$.

As explained in [21], each $s_{k,r}[n]$ is a concatenation of sequences of the form 1, 0, …, 0, –1, 0, …, 0 or –1, 0, …, 0, 1, 0, …, 0. Thus, $|s_{k,r}[n]| \le 1$ and $|s_{k,r}[n] - s_{k,r}[n-1]| \le 2$ for all $n$, and the running sum of $s_{k,r}[n]$ never exceeds 1 nor –1. However, after startup, the finite state

machines that generate the switching sequences do not necessarily start at the beginning of their respective cycles, which could cause the magnitudes of the running sums of some switching sequences to exceed 1. This issue is avoided by the inclusion of a ±1 clipper within each $s_{k,r}[n]$ accumulator as shown in Fig. 32.

Each MNC coefficient within each $s_{k,r}[n]$ residue estimator is the output of a 29-bit clipping accumulator. The 20 LSBs of the coefficients are dropped prior to their respective multiplication by $s_{k,r}[n]$ and $s_{k,r}[n-1] - s_{k,r}[n]$, which reduces power consumption at the expense of reducing the accuracy with which $e_{\mathrm{MNC}}[p]$ cancels the additive error terms in (96). The number of bits to drop was determined with the aid of simulations performed by the authors using a bit-accurate, event-driven, C-language, custom PLL simulator such that the contribution to the PLL's phase noise from the residual error that is left after MNC is applied is negligible.

The $K_a$ and $K_b$ gains are restricted to powers of 2 so the implementation of their respective multipliers only involves bus-shifting. Consequently, as shown in Fig. 32, the MNC logic requires no actual digital multipliers.

### C. DCO FCE Banks

The DCO consists of a single-turn center-tapped inductor, a cross-coupled NMOS pair, a tail resonant tank [23], a triode-MOS tail source, and integer and fractional FCE banks. The implemented FCEs are of the type presented in [2], and the minimum-size FCE has an equivalent frequency step of $\Delta_{\mathrm{min}} = 160$ kHz at 6.5 GHz. The integer FCE bank comprises eight $32\times\Delta_{\mathrm{min}}$ FCEs and five pairs of 16×, 8×, 4×, 2× and $1\times\ \Delta_{\mathrm{min}}$ FCEs, whereas the fractional FCE bank comprises sixteen $\Delta_{\mathrm{min}}$ FCEs. All FCEs are implemented by connecting one or more $\Delta_{\mathrm{min}}$ FCEs in parallel.

Both FCE banks are laid out as illustrated in Fig. 33, where the FCEs are indexed according to their respective control bits. Each FCE is driven by a flip-flop clocked by $\mathrm{clk}_{\mathrm{fast}}(t)$, followed by a buffer. The size of each buffer is scaled according to the number of parallel $\Delta_{\mathrm{min}}$ FCEs it drives.

As shown in Fig. 33, the ten largest FCEs of the integer FCE bank, FCEs 25 to 34, are split into two halves each, which are laid out in a common-centroid fashion to avoid the FCE mismatches from being exacerbated. As explained in Section II-B, the MNC technique cancels much of the error that arises from FCE mismatches, but the larger the FCE mismatches, the larger the required dynamic range of $e_{\mathrm{MNC}}[p]$ and the larger the resulting output dynamic range of the MR-DEM encoder's fractional path. A larger fractional path output dynamic range is undesirable in practice as it increases the MR-DEM encoder's power consumption, as well as the number of control lines that need to be routed from the DCO control to the FCE banks' drivers. Therefore, care was taken with the layout to minimize FCE mismatches.

## IV. MEASUREMENT RESULTS

The prototype IC consists of the digital fractional-*N* PLL as well as a serial peripheral interface (SPI) and additional circuitry used for testing. The IC was fabricated in the Global-Foundries 22 nm CMOS 22FDX technology.

The IC's place-and-route (PNR) digital block has a 0.8 V power supply and is clocked by an $f_{\mathrm{fast}}$-rate clock, where $f_{\mathrm{fast}} = f_{\mathrm{PLL}}/8$. However, most of the PNR digital block's sub-blocks are clocked by $f_{\mathrm{ref}} = 80$ MHz clocks that are derived from the $f_{\mathrm{fast}}$-rate clock. The maximum value of $f_{\mathrm{fast}}$ is 830 MHz, although the PNR digital block was designed to run at a clock-rate as

high as 1 GHz to provide design margin. The PNR digital block's area is 0.0482 $mm^2$, half of which corresponds to the circuitry associated with the MR-DEM and MNC techniques.

Fig. 34 shows the measured PLL phase noise at $f_{PLL}$ = 6.56 GHz for a PLL bandwidth of 900 kHz under various conditions. The signal source analyzer's averaging option was set to 32 when taking each measurement result shown in the figure. In Fig. 34(a), the MR-DEM technique is disabled, i.e., it is configured to operate as a conventional DCO control technique,[13] the MNC technique is disabled, and the measurement was taken over a time period wherein $d_I[n]$ did not vary. Thus, the phase noise profile shown in Fig. 34(a) corresponds to a standard phase noise profile, as reported in most published papers that report digital PLL results. Fig. 34(b) shows the measured PLL phase noise for the same conditions of Fig. 34(a), except that the measurement time duration was increased and the instrument's persistence option was enabled. The PLL was left running for 2 hours for the measurement, and $d[n]$ was regularly monitored through the SPI to check for integer-boundary crossings. As shown in Fig. 34(b), the PLL phase noise varies significantly over time, such that the spot phase noises at 20 kHz and 1 MHz offset frequencies vary by 9 dB and 11 dB, respectively. The $d[n]$ sequence crossed three integer boundaries several times during the measurement. Additional measurements performed by the authors indicate that phase noise profiles almost identical to that shown in Fig. 34(b) can be easily obtained in a few minutes, or even in a few seconds if less averaging is used.

Fig. 34(c) shows the measured PLL phase noise for the same conditions of Fig. 34(b), except with the MR-DEM and MNC techniques both enabled. In this case, $d[n]$ crossed two

[13] Specifically, the slow DEM encoder's randomization is disabled, in which case the slow DEM encoder behaves as a conventional encoder. The digital ΔΣ modulator and fast DEM encoder were enabled for all the measurements reported in this paper.

integer boundaries several times during the measurement. As demonstrated in Fig. 34(c), the PLL phase noise varies much less with the proposed techniques enabled. Even at offset frequencies lower than 100 kHz, where the phase noise profile is expected to vary somewhat because of the algorithm used by the instrument to compute the spectrum, the variations in Fig. 34(c) are considerably less significant than those in Fig. 34(b) (e.g., less than 2 dB versus more than 9 dB at a 20 kHz offset frequency). As explained below, the ISI-error correction branch of the MNC technique does not perfectly cancel the ISI component of the error at the PLL output. This is reflected in Fig. 34(c) as a slight phase noise increase at offset frequencies above 10 MHz.

Fig. 34(d) shows the measured PLL phase noise for the same conditions of Fig. 34(c), except that the MR-DEM technique was disabled and the MNC technique's coefficients were frozen after convergence but prior to the measurement. In this case, $d[n]$ crossed two integer boundaries several times during the measurement. The phase noise profile shown in Fig. 8(d) is similar to that shown in Fig. 34(c), except for slightly larger variations at offset frequencies below 200 kHz and at a 1 MHz offset frequency, and the phase noise at offset frequencies above 10 MHz which does not exhibit the excess noise shown in Fig. 34(c). The increase in phase noise variation at low offset frequencies in Fig. 34(d) compared to Fig. 34(c) happens because MNC coefficient noise gets sampled, and, hence, locked in when the MNC coefficients are frozen. Hence, in this configuration, the PLL's performance is expected to be similar to that of the PLL without the MR-DEM and MNC techniques enabled but with considerably smaller FCE mismatches.

Fig. 35 shows the measured PLL phase noise at $f_{PLL}$ = 6.56 GHz with the signal source analyzer's averaging option set to 32 and different combinations of the proposed techniques enabled and disabled. The PLL bandwidth was set to 900 kHz in each case. Fig. 35(a) shows the effect on the PLL phase noise of the MR-DEM technique in the absence of MNC compared to the baseline case of Fig. 34(a). As shown in the figure, the spot phase noise increases by up to 11.5 dB compared to the case of Fig. 34(a), whereas the total integrated jitter from 10 kHz to 80 MHz, $\sigma_{TJ}$, increases from 176 $fs_{rms}$ to 190 $fs_{rms}$. Fig. 35(b) shows the measured PLL phase noise with the MR-DEM technique and only the static-error correction branch of the MNC technique enabled. The spot phase noise around a 20 MHz offset frequency decreases by 8 dB, which corresponds to most of the noise introduced by the MR-DEM technique. Fig. 35(c) shows the measured PLL phase noise with the MR-DEM technique and both branches of the MNC technique enabled. As shown in Fig. 35(c), the improvement after applying ISI error correction results in a 1.2 dB spot phase noise reduction around a 20 MHz offset frequency, and the resulting phase noise profile still shows some residual error, although its effect on $\sigma_{TJ}$ is almost negligible.

As explained in [15], each $b_{k,r}[n]$ coefficient in (97) converges to a value proportional to the average over $1/f_{fast}$ of its respective $\gamma_{k,r}(t)$ coefficient in (96). Consequently, the ISI-error correction branch of the MNC technique does not perfectly cancel the third term from the right side of (96). Nonetheless, as demonstrated in Fig. 35, this is not a problem in practice because the power of the ISI-error component introduced by the MR-DEM technique is much smaller than that of the static-error component. Additional measurements taken by the authors for the same conditions used to generate Fig. 34(d), except with the MNC technique's ISI-error

correction branch disabled, yielded phase noise profiles virtually identical to that shown in Fig. 34(d). This suggests that, at least in the case of the presented prototype IC, the ISI-error correction branch of the MNC technique could be omitted to save both power and area without significantly affecting the effectiveness of the MR-DEM and MNC techniques to mitigate spectral breathing.

Although originally intended to work with highpass-shaped switching sequences, the MNC technique also works with white switching sequences. Fig. 36 shows measured PLL phase noise profiles similar to those shown in Fig. 35(a) and Fig. 35(c) but for white switching sequences within the slow DEM encoder. As shown in Fig. 36(a), the PLL phase noise is severely degraded when enabling MR-DEM in this case. The spot phase noise increases by up to 12.6 dB, and $\sigma_{TJ}$ increases from 176 to 425 $fs_{rms}$. Nonetheless, as shown in Fig 36(b), the MNC technique cancels most of the noise introduced by the MR-DEM technique, except for a small portion for the reasons explained above. As in the case with highpass-shaped switching sequences, most of the noise in Fig. 36(a) gets cancelled when enabling the MNC technique's static-error correction branch; the ISI-error correction branch accounts for less than a 1 dB reduction.

Table 2 summarizes the increase of the PNR digital block's power consumption for different combinations of the MR-DEM and MNC techniques enabled and disabled. As shown in the table, the proposed techniques increase the power consumption by up to 1.64 mW and 1.4 mW when using highpass-shaped and white switching sequences, respectively. In both cases, the most significant contributor is the ISI-error correction branch of the MNC technique.

The proposed techniques can be used without significantly increasing the PLL's power consumption by freezing the MNC coefficients after convergence and disabling the MR-DEM technique, in which case the PLL's power consumption only increases by 250 $\mu$W. However, as demonstrated in Fig. 34(c) and Fig. 34(d), the effectiveness of the techniques to mitigate spectral breathing is slightly reduced is in this case.

Additional measurements taken by the authors suggest that the proposed techniques have no effect on the PLL's fractional spur performance. In contrast, the reference spur power increases by 10 dB (from –80 dBc to –70 dBc) as a result of enabling MR-DEM, but it does not increase when MNC is enabled with its coefficients frozen and MR-DEM is disabled.

Although the reference spur is expected to increase when enabling MR-DEM due to coupling from the DCO control lines to the DCO outputs, the authors believe that the reported increase of 10 dB is exacerbated by a layout issue in the DCO, which was not caught prior to fabrication because of a post-layout extraction tool flaw. As explained in [4], this issue caused the DCO's quality factor to be significantly lower than expected even after FIB surgery. Consequently, the DCO outputs swing is extremely low, even when raising the DCO tank's supply voltage to 0.9 V, and the DCO is highly sensitive to interference from other circuit blocks.

## V. CONCLUSION

This paper presents the first experimental demonstration of the MR-DEM and MNC techniques described in [15], which mitigate the spectral breathing problem in digital PLLs that

results from non-ideal FCE behavior. Additionally, implementation details as well as practical observations that complement the techniques' descriptions in [15] are presented.

The MR-DEM technique linearizes the DCO input-output characteristics at the expense of additive highpass-shaped error which depends on known digital sequences. This error has a component that arises from FCE static gain errors, and another component that arises from ISI, both of which are cancelled by the MNC technique. By freezing the MNC coefficients after convergence and disabling MR-DEM, the presented techniques significantly mitigate the spectral breathing problem while only negligibly increasing the PLL's total power consumption.

Measurement results suggest that for this particular DCO design, the power of the ISI component of the DCO error is much less significant than that of the component that arises from FCE static gain errors. Furthermore, the results suggest that white switching sequences can be used in the MR-DEM technique's slow DEM encoder to reduce digital logic complexity, thereby reducing both power and area consumption.

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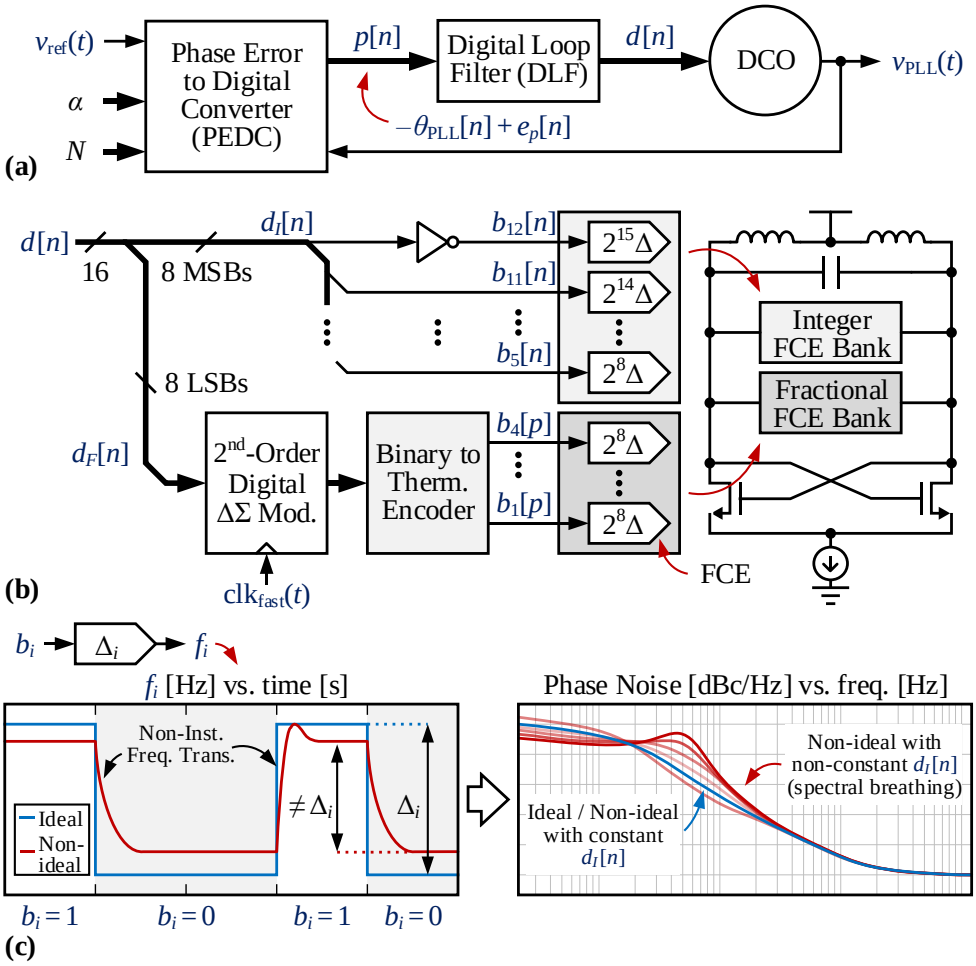


Figure 27: (a) General form of a digital fractional-*N* PLL (b) conventional DCO control technique, and (c) illustration of the effects of non-ideal FCE behavior on the PLL's phase noise spectrum.

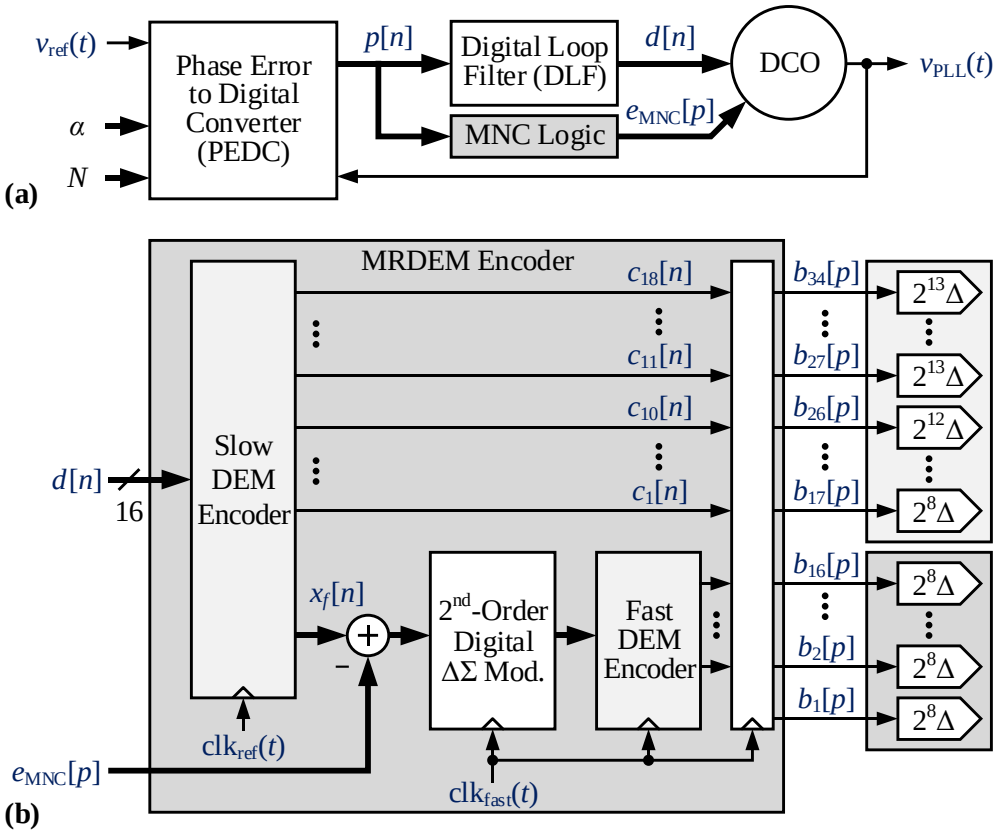


Figure 28: (a) Block diagram of a digital fractional-*N* PLL with the MR-DEM and MNC techniques, and (b) MR-DEM technique details.

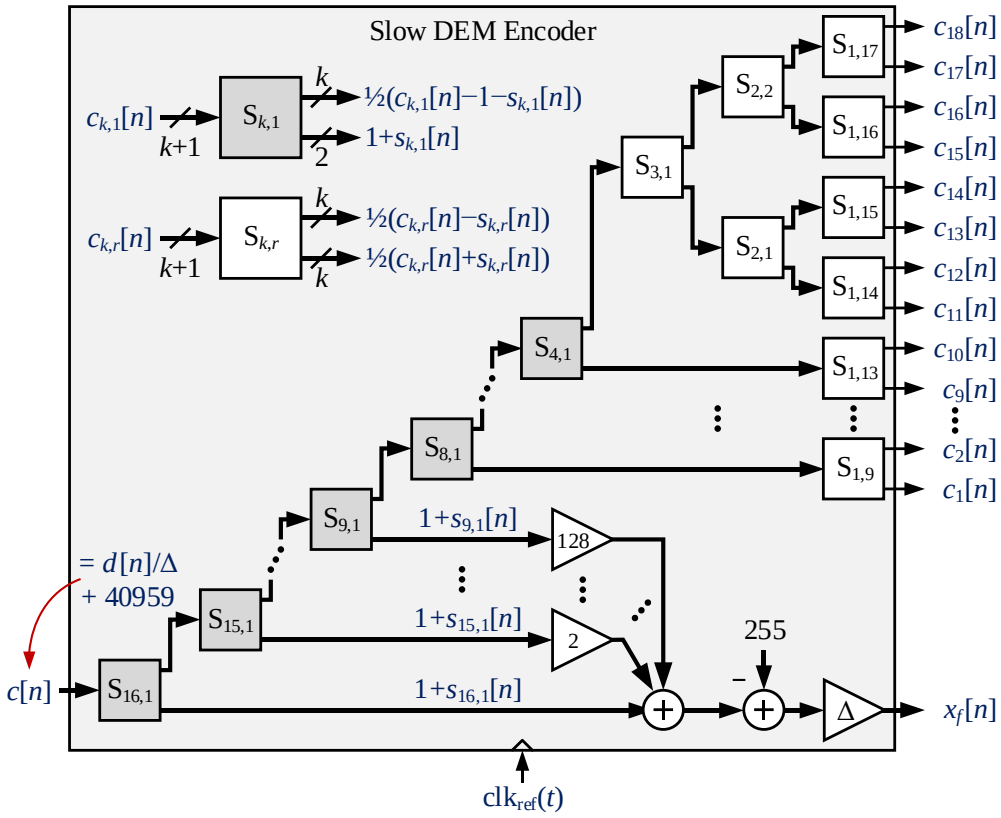


Figure 29: Slow DEM encoder signal processing.

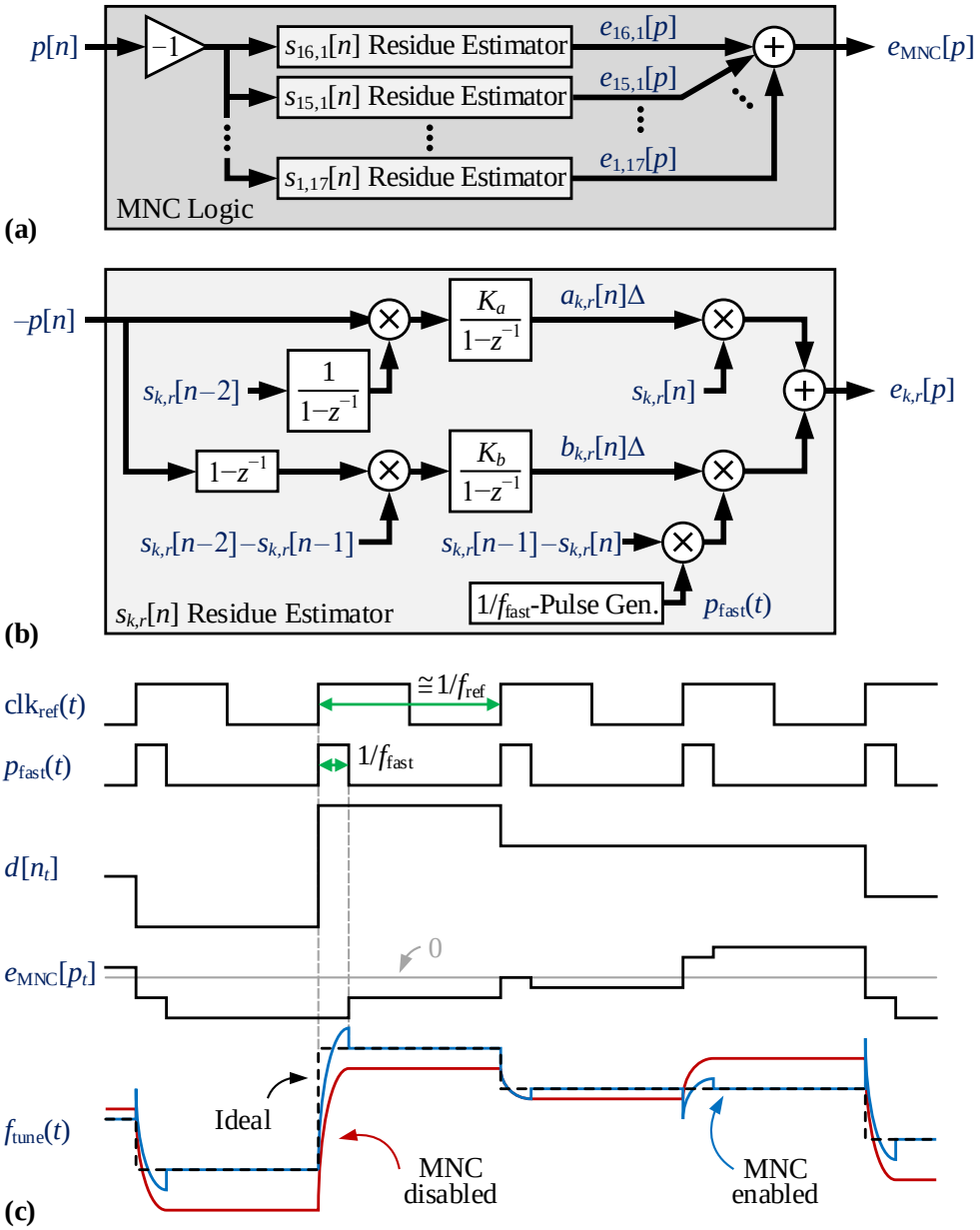


Figure 30: (a) MNC logic signal processing, (b) $s_{k,r}[n]$ residue estimator signal processing, and (c) illustration of the MNC technique operation where $p_t = p$ over the $p$th period of $\text{clk}_{\text{fast}}(t)$.

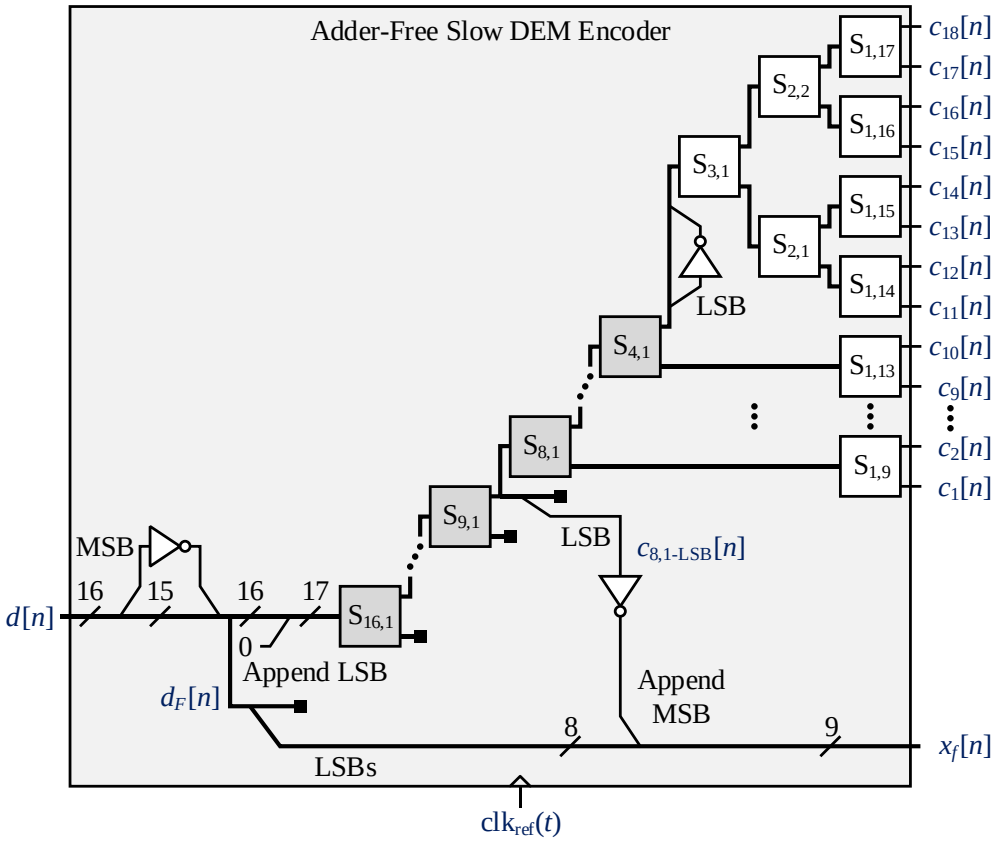


Figure 31: Adder-free slow DEM encoder implementation.

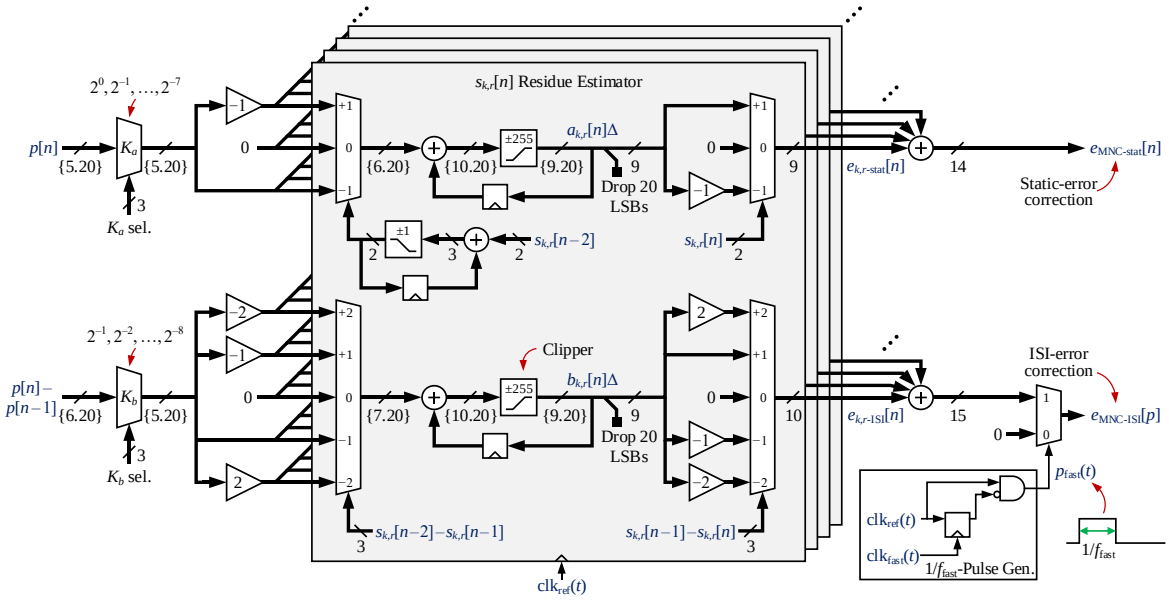


Figure 32: MNC logic bit-level implementation.

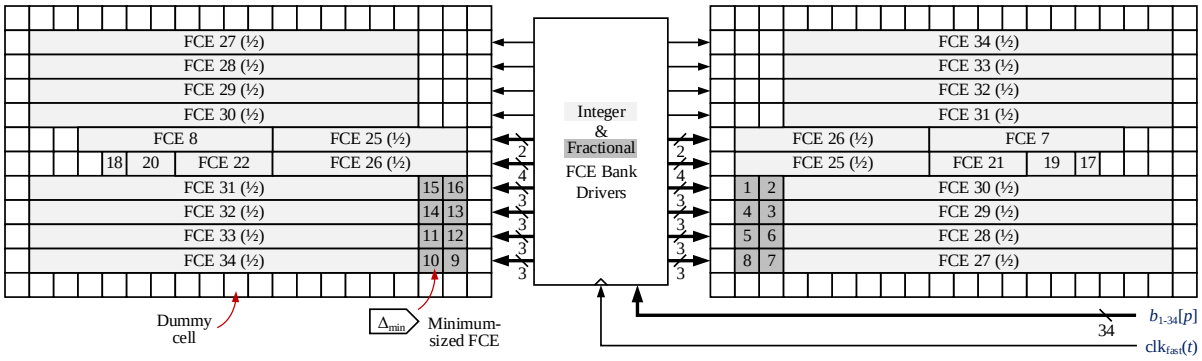


Figure 33: Integer and fractional FCE banks layout.

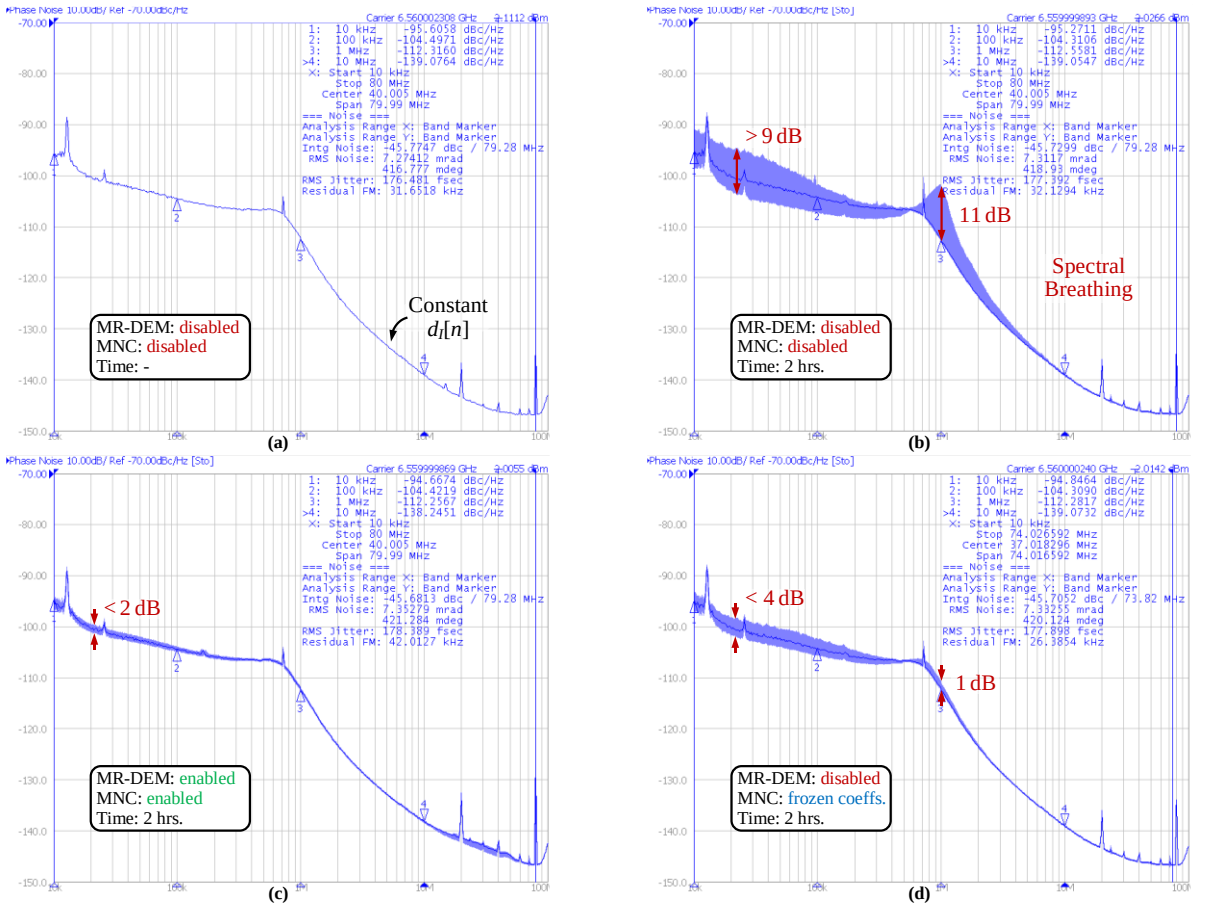


Figure 34: Measured PLL phase noise at $f_{PLL}$ = 6.56 GHz for (a) conventional DCO control technique with constant $d_l[n]$, (b) conventional DCO control technique and persistence enabled for 2 hrs. (c) MR-DEM and MNC enabled and persistence enabled for 2 hrs., and (d) MR-DEM disabled, MNC enabled with coefficients frozen after convergence, and persistence enabled for 2 hrs.

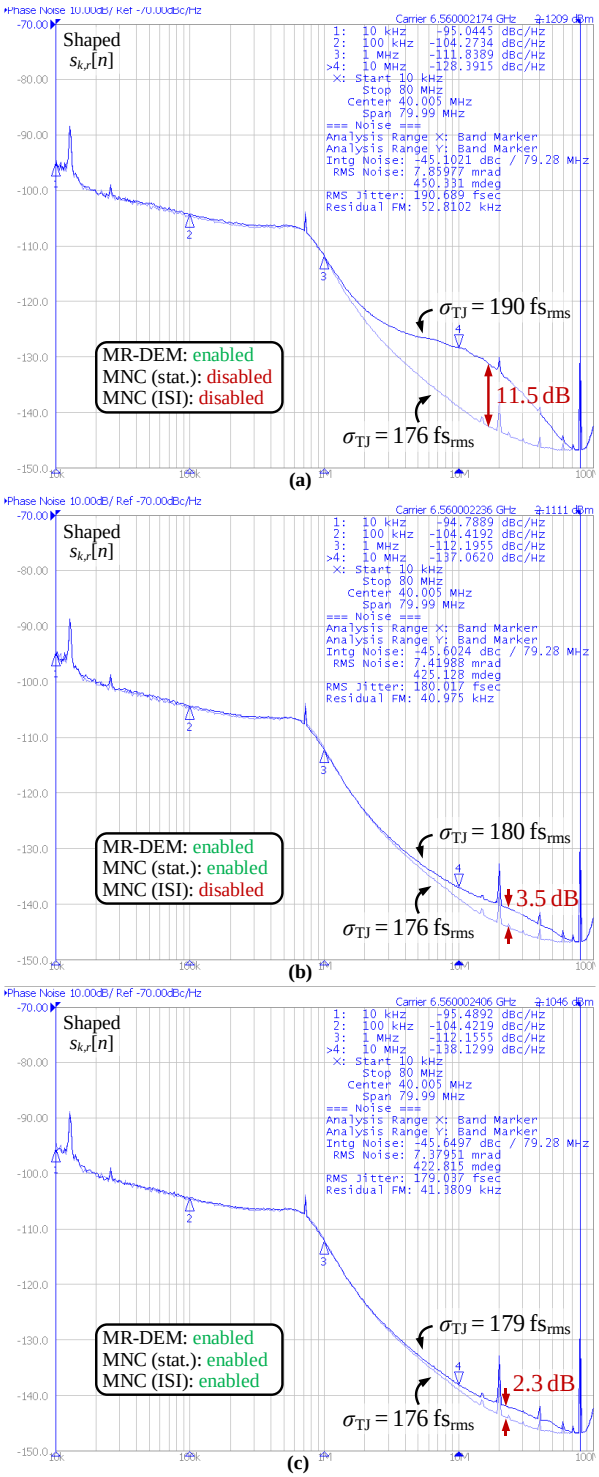


Figure 35: Measured PLL phase noise at $f_{PLL}$ = 6.56 GHz for (a) MR-DEM enabled and MNC disabled, (b) MR-DEM and MNC (stat. branch only) enabled, and (c) MR-DEM and MNC (both stat. and ISI branches) enabled

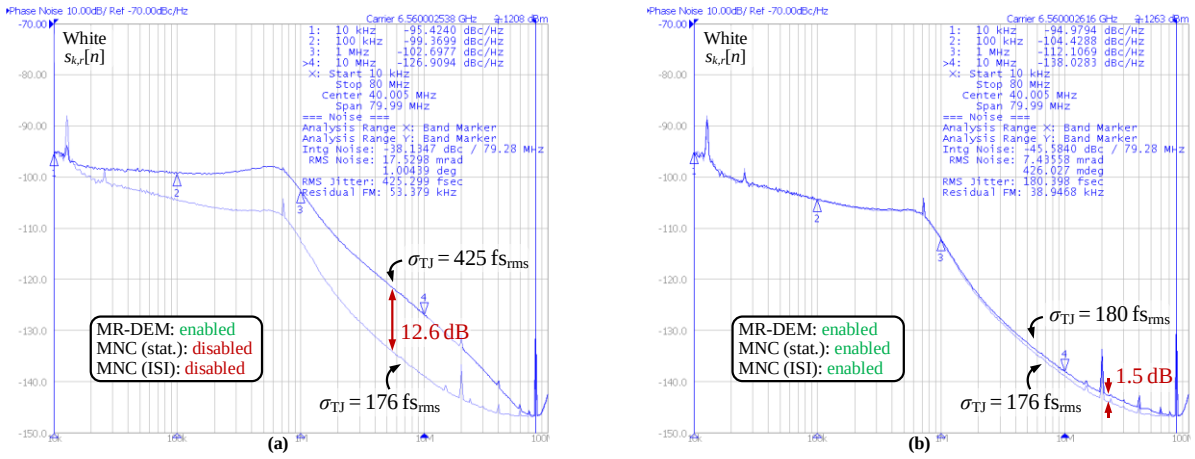


Figure 36: Measured PLL phase noise at $f_{PLL}$ = 6.56 GHz with MR-DEM enabled for (a) MNC disabled, and (b) MNC (both stat. and ISI branches) enabled.

TABLES

Table 2: PNR digital block power consumption.

| MR-DEM | MNC | | Power increase (mW) [1] | |
|---|---|---|---|---|
| | Stat.-error branch | ISI-error branch | MNC coeffs. update active | MNC coeffs. frozen |
| Disabled | Enabled | Enabled | - | 0.25 |
| First-Order Highpass-Shaped $s_{k,r}[n]$ | | | | |
| Enabled | Disabled | Disabled | 0.52 | 0.52 |
| | Enabled | Disabled | 0.92 | 0.57 |
| | Enabled | Enabled | 1.64 | 0.86 |
| White $s_{k,r}[n]$ | | | | |
| Enabled | Disabled | Disabled | 0.43 | 0.43 |
| | Enabled | Disabled | 0.83 | 0.47 |
| | Enabled | Enabled | 1.40 | 0.70 |

[1] With respect to the case where MR-DEM and MNC are disabled.

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