Title
Switched Capacitor DC-DC Converter: Superior where the Buck Converter has Dominated

Author
Ng, Vincent Wai-Shan

Publication Date
2011

Peer reviewed|Thesis/dissertation

Switched Capacitor DC-DC Converter: Superior where the Buck Converter has Dominated

By

Vincent Wai-Shan Ng

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering – Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Seth Sanders, Chair
Professor Elad Alon
Professor Roberto Horowitz

Fall 2011

Abstract

Switched Capacitor DC-DC Converter: Superior where the Buck Converter has Dominated

By

Vincent Wai-Shan Ng

Doctor of Philosophy in Engineering - Electrical Engineering and Computer Science

University of California, Berkeley

Professor Seth R. Sanders, Chair

The traditional inductor-based buck converter has been the default design for switched-mode voltage regulators for decades. Switched capacitor (SC) dc-dc converters, on the other hand, have traditionally been used in low power (<10mW) and low conversion ratio (<4:1) applications where neither regulation nor efficiency is critical. This work encompasses the complete successful design, fabrication, and test of a CMOS based switched capacitor dc-dc converter, addressing the ubiquitous 12 V to 1.5 V board-mounted point-of-load application, which the buck converter has dominated. In particular, the circuit developed in this work attains higher efficiency (92% peak, and >80% over a load range of 5 mA to 1 A) than surveyed competitive buck converters, while requiring less board area and less costly passive components. The topology and controller enable a wide input range of 7.5 V to 13.5 V. Controls based on feedback and feedforward provide tight regulation under worst case line and load step conditions. This work shows that the SC converter can outperform the buck converter, and thus the scope of SC converter application can and should be expanded.

Contents

List of Figures

Acknowledgment

I would like to thank my adviser, Professor Seth Sanders, for his guidance and support throughout my years of graduate studies. I would also like to thank my committee members, Professor Elad Alon, and Professor Roberto Horowitz for their advice on my thesis and research. I must also thank my fellow colleagues, Jason Stauth, Hanh-Phuc Le, Mervin John and Michael Seeman for their help throughout my studies. Last but not least, I must thank my parents, my family and my dear friends. Doing a PhD here and going through all the exams and hurdles are definitely not easy, and I am sincerely thankful to have all of you by my side. I devote this thesis to all of you, and wish you good luck in all your endeavors.

Chapter 0

Executive Summary

The traditional inductor-based buck converter has been the default design for most switched-mode voltage regulators for decades. In its simplest form, the buck converter contains only two switches, one inductor, and the input capacitor[1]. Due to its relatively simple structure and control methodology, it is the dominant design for applications that require tight regulation (<10mV), high efficiency (>90%) and high output power (>100mW). Switched capacitor (SC) dc-dc converters, on the other hand, have traditionally been used in low power (<10mW) and low conversion ratio (<4:1) applications where neither regulation nor efficiency is critical. This work encompasses the complete successful design, fabrication, and test of a CMOS based switched capacitor dc-dc converter, addressing the ubiquitous 12V to 1.5V board-mounted point-of-load application. In particular, the circuit developed in this work attains higher efficiency (92% peak, and >80% over a load range of 5mA to 1A) than surveyed competitive buck converters, while requiring less board area and less costly passive components. The topology and controller enable a wide input range of 7.5V to 13.5V. Controls based on feedback and feedforward provide tight regulation under worst case line and load step conditions. This work shows that the SC converter can outperform the buck converter, and thus the scope of SC converter application can and should be expanded.

As discussed in references [3, 4] and later in Introduction section 1.2, a number of SC converter topologies are very effective in their utilization of switches and passive elements, especially in relation to the ever popular buck converter. In terms of switches, the power switches in the buck converter each block the full input voltage and support the full output current. For a large or even moderate conversion ratio, this leads to a high switch total Volt-Ampere product, and causes the buck converter to suffer from poor power device utilization. In contrast, the switches in a ladder or Dickson SC converter only block a fraction of the input voltage, while supporting a fraction of the output current. This not only enables utilization of native low-voltage CMOS transistors in a modern low-cost CMOS process, but also leads to a low total switch Volt-Ampere product, allowing these SC converters to sustain high efficiency with a high conversion ratio. In terms of passive elements, SC converters benefit from the significantly higher energy density of capacitors over inductors. As shown in Table 1 [5], surveyed surface mount scale capacitors have a volumetric energy density that is over 1000 times higher than that of surveyed inductors. This can lead to a considerable reduction in Printed Circuit Board (PCB) area and in cost by replacing one bulky inductor with several smaller capacitors. This work builds a moderate conversion ratio

Table 1: Energy density of common capacitors and inductors

Type	Manufacturer	Capacitance	Dimensions $[mm^3]$	Energy density
Ceramic Cap	Taiyo-Yuden	$22\mu F@4V$	$1.6 * 0.8 * 0.8$	$344\mu J/mm^3$
Ceramic Cap	Taiyo-Yuden	$1\mu F@35V$	$1.6 * 0.8 * 0.8$	$1196\mu J/mm^3$
Tantalum Cap	Vishay	$10\mu F@4V$	$1.0 * 0.5 * 0.6$	$533\mu J/mm^3$
Tantalum Cap	Vishay	$100\mu F@6.3V$	$2.4 * 1.45 * 1.1$	$1037\mu J/mm^3$
Electrolytic Cap	Kemet	$22\mu F@16V$	$7.3 * 4.3 * 1.9$	$94\mu J/mm^3$
Electrolytic Cap	C.D.E	$210mF@50V$	$76\phi * 219$	$172\mu J/mm^3$
Shielded SMT Ind	Coilcraft	$10\mu H@0.2A$	$2.6 * 2.1 * 1.8$	$0.045\mu J/mm^3$
Shielded SMT Ind	Coilcraft	$100\mu H@0.1A$	$3.4 * 3.0 * 2.0$	$0.049\mu J/mm^3$
Shielded Inductor	Coilcraft	$170\mu H@1.0A$	$11 * 11 * 9.5$	$0.148\mu J/mm^3$
Shielded Inductor	Murata	$1mH@2.4A$	$29.8\phi * 21.8$	$0.189\mu J/mm^3$

(12 V-to-1.5 V) SC converter in a 0.18μm/0.6μm process to realize these advantages of the SC converter.

Figure 1 shows the schematic of the Dickson SC converter implemented in this work. The input voltage may range from 7.5V to 13.5V, while the converter outputs a nominal voltage of 1.5V, defined by an on-chip bandgap reference. Capacitors $C_1 - C_9$ are the power-train capacitors, and they are implemented with off-chip ceramic capacitors. The Dickson converter operates in two phases, and achieves voltage conversion through charge transfers among capacitors $C_1 - C_9$ [6]. Switches $S_1 - S_{12}$ are the power switches, and the phase in which they are turned on is indicated by the number in bracket next to the switch label in the figure; the switch is turned off in the other phase. As further discussed in section 2.4, switches $S_{13} - S_{18}$ are also power switches, but they may turn on in either clock phase depending on the conversion ratio of the converter. These switches allow the converter to attain seven different conversion ratios, ranging from 5-to-1 to 8-to-1 with half integer steps. As further discussed in section 2.2, the integrated circuit implementation, in a 0.18 micron triple-well CMOS process, is sub-divided into various voltage domains to allow the usage of low voltage transistors (blocking a maximum of 4V) to accommodate a moderate voltage input, as high as 13.5V [34]. As further explained in chapter 3, this converter achieves regulation by first adjusting its nominal conversion ratio, and then by modulating the switch conductance of switches $S_{1,4,5}$. Switch conductance modulation allows tight regulation for line and load variation whereas changing conversion ratio allows the converter to attain a high efficiency throughout the operating space. Further, the converter modulates switching frequency to attain high efficiency at light load conditions. Auxiliary functions such as self-startup, over-current protection and safe shutdown are also implemented. Further details of the controller are discussed in chapter 3.

Figure 2 shows the expected efficiency and measured efficiency of the converter versus load current (I_{OUT}) at around $V_{IN} = 8.7V$. As shown in the figure, this converter attains a peak efficiency of 93% and maintains efficiency higher than 80% over an output current range from 5mA to 1A. Figure 3 shows the expected efficiency and measured efficiency of the converter versus input voltage with load current at two different values, namely 50mA and 220mA. As shown in the figure, this converter maintains efficiency higher than 85% from 7.5V

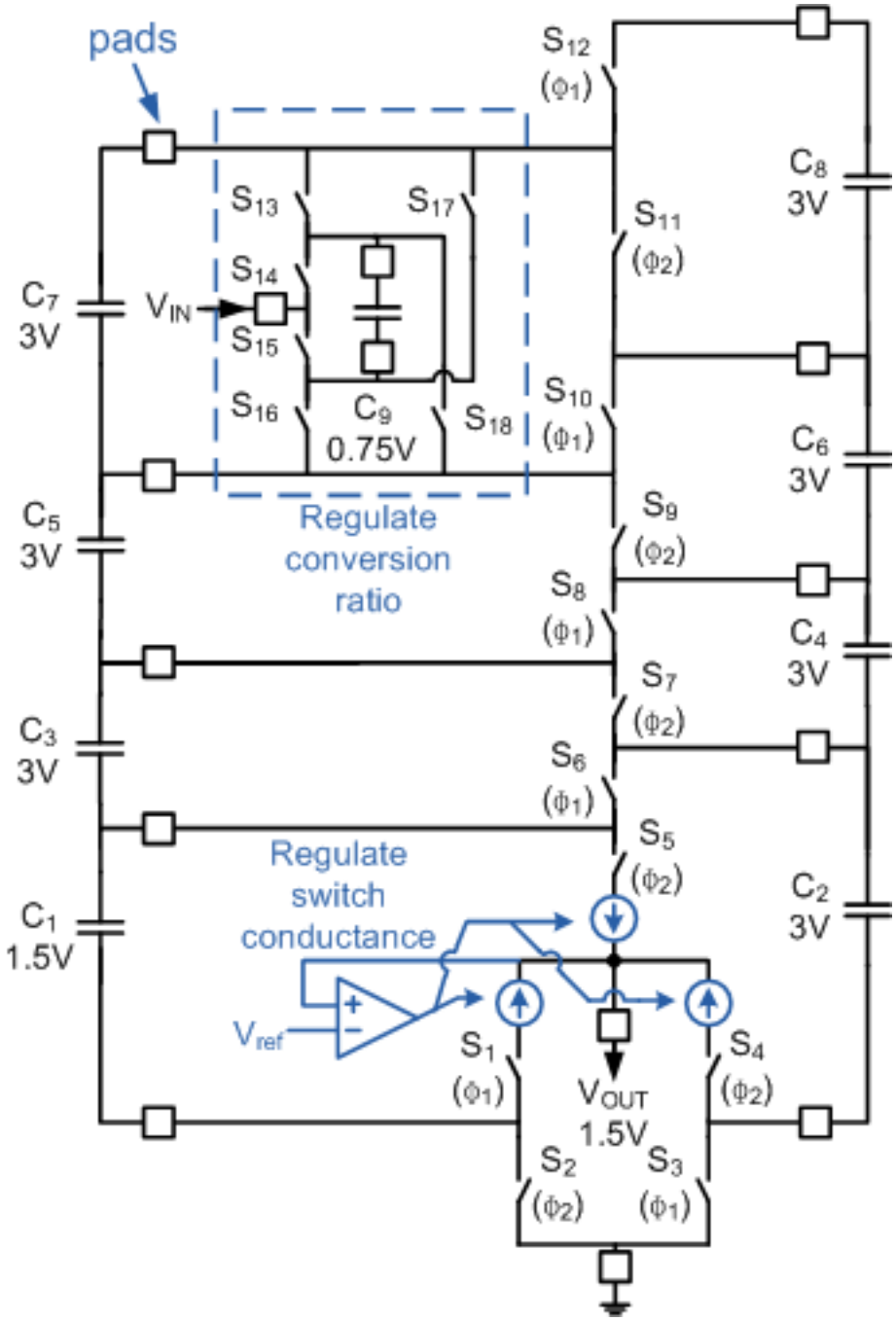


Figure 1: Circuit schematic of implemented converter

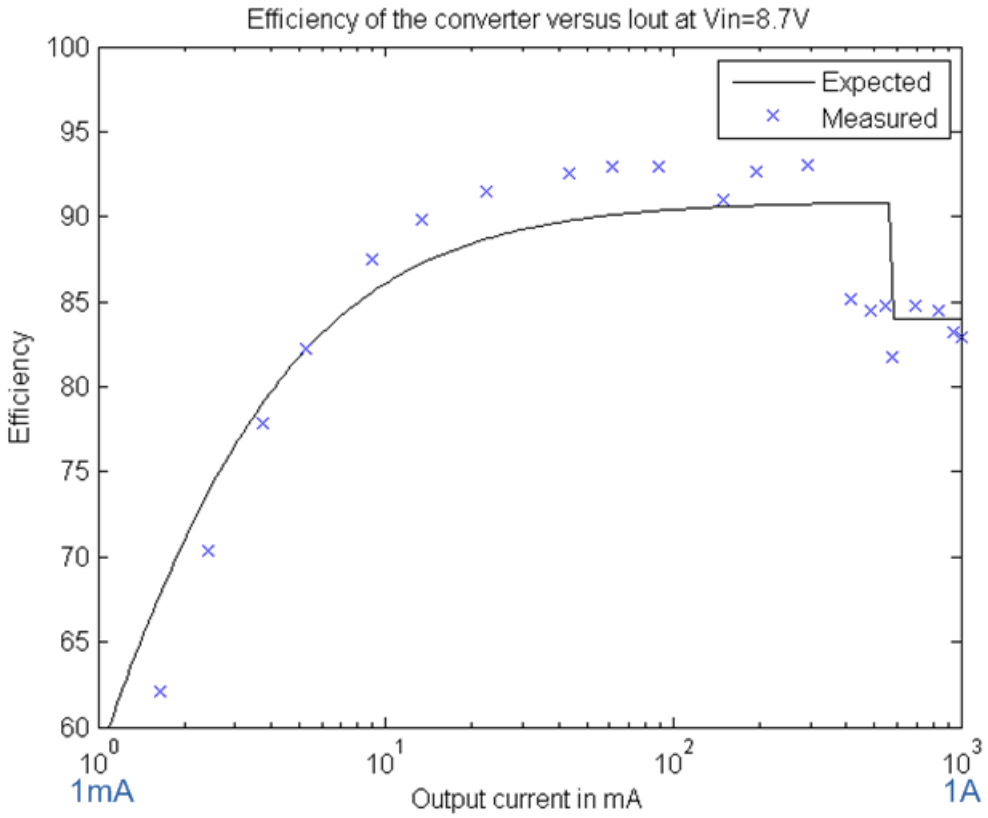


Figure 2: Efficiency versus I_{OUT} at around $V_{IN} = 8.7$V

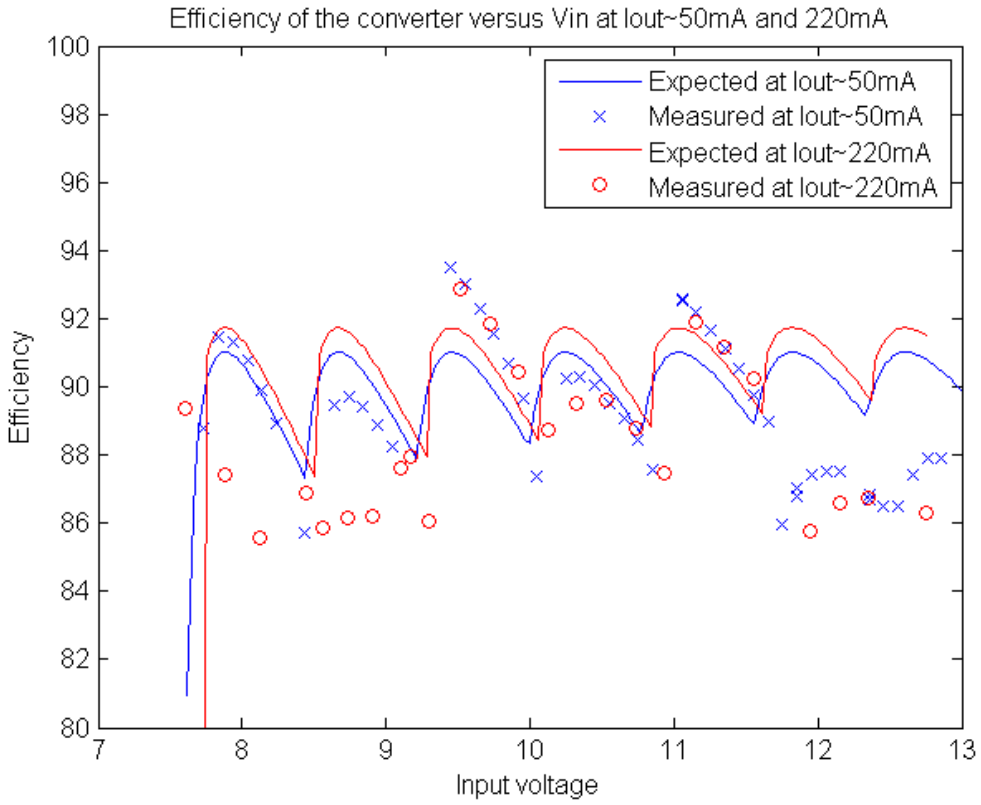


Figure 3: Efficiency versus V_{IN} at I_{OUT} ~ 50mA and 220mA

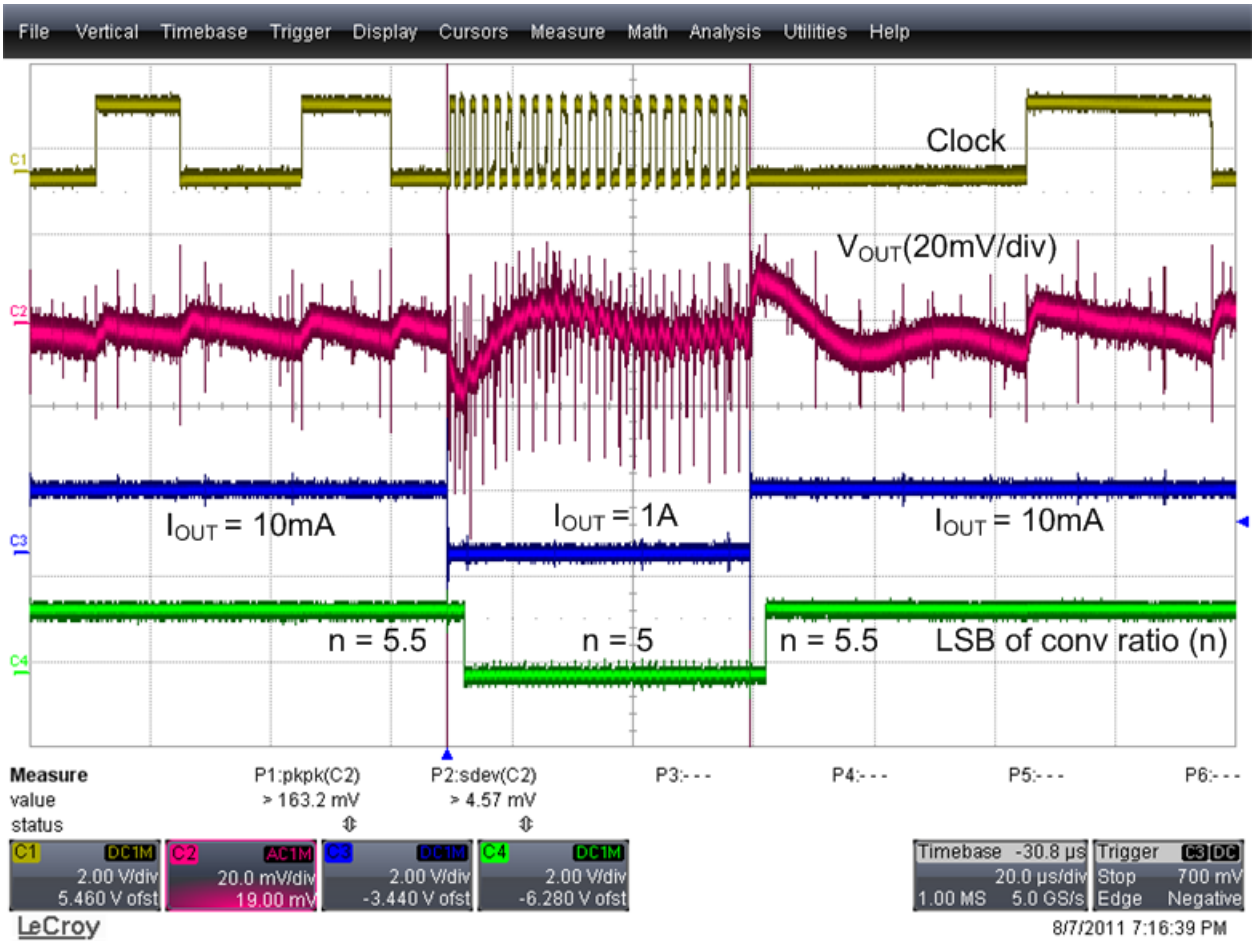


Figure 4: Oscilloscope plot of loading and unloading I_{OUT} step of 1A at $V_{IN} = 9V$. The top waveform is the switching clock of the converter. The second waveform is an AC coupled signal of the output voltage in 20mV/div. The third waveform shows the drain of a MOSFET that switches in three 4Ω resistors in parallel to the output. The fourth waveform shows the least significant bit of the conversion ratio, indicating that the converter changes conversion ratio back and forth by one step during the measurement. The timescale is $20\mu s/div$.

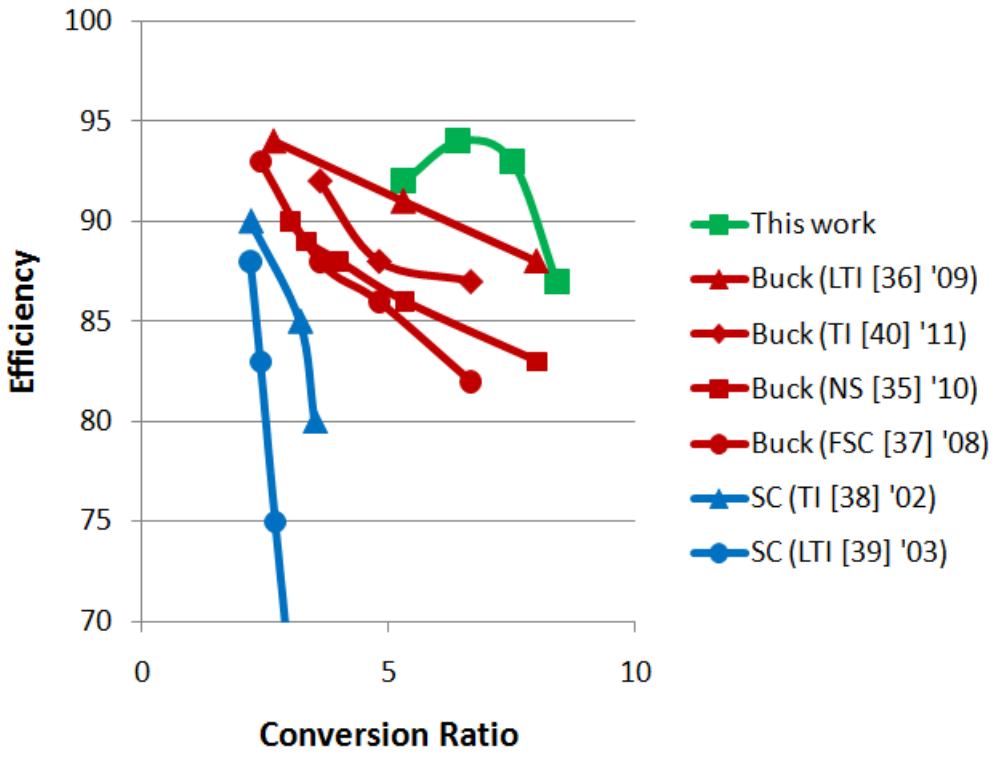


Figure 5: Comparison of peak efficiency between this work and similar works.

to 13V with a nominal output voltage of 1.5V. Figure 4 shows the load transient response of the converter during loading and unloading steps of 1A. The output voltage is regulated to within 30mV during the transient. The behavior of the converter and the controller during this transient are discussed in chapter 3 and in chapter 5, section 5.4. Figure 5 shows a comparison of the peak efficiency of this converter with that of similarly rated converters. All the surveyed buck and SC converters achieve respectable efficiency, but show a general trend of reduced efficiency as conversion ratio increases. The present work shows a significant increase in efficiency when compared to similarly rated SC and buck converters. As further discussed in section 5.5, this work also achieves an overall reduction in PCB area and passive component cost when compared to dc-dc converters with similar ratings. This work shows that the SC converter, implemented in standard CMOS technology, provides a new direction for performance and cost advantages with respect to the conventional buck converter. This work shows that the SC converter can outperform the buck converter in areas where the latter currently dominates, and its scope can be greatly expanded.

Chapter 1

Introduction

The traditional inductor-based buck converter has been the default design for most switched-mode voltage regulators for decades. In its simplest form, the buck converter contains only two switches, one inductor, and the input capacitor[1]. Ideally, it can attain any voltage step-down conversion ratio with 100% efficiency by varying duty ratio. Due to its relatively simple structure and control methodology, it is the dominant design for applications that require tight regulation (<10mV), high efficiency (>90%) and high output power (>100mW). The Switched Capacitor (SC) dc-dc converter, on the other hand, has its nominal conversion ratio defined by its topology. When an SC converter operates away from its unloaded conversion ratio, its efficiency suffers. Its maximum possible efficiency, Eff_{MAX}, is given by:

$$Eff_{MAX} = \frac{V_{OUT}}{V_{IN}/n} \tag{1.1}$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, and n is the unloaded conversion ratio of the converter [3]. In order to attain high efficiency across V_{IN} and/or V_{OUT} variations, an SC converter needs to support several conversion ratios, which increases its complexity and the required number of switches and capacitors. Depending on conversion ratio and topology, an SC converter can have more than a dozen switches and capacitors. Further, as explained in chapter 3, there are numerous ways to control an SC converter. The large number of active components (switches) and passive components (capacitors), together with non-trivial control, has prevented SC converters from becoming the most popular design in voltage regulators. Traditionally, SC converters are used in low power (<10mW) applications where regulation and efficiency is non-critical. For example, SC converters are used to boost voltage for the erase function in flash memories. This application uses SC converters because erase voltage need not be precise, and low efficiency is tolerable since the erase operation is infrequent compared with reading. Applications that require high performance voltage regulators almost all use the buck converter.

However, as explained later in section 1.2, the SC converter can be superior to the buck converter in terms of both cost and efficiency. This allows the SC converter to be very competitive in dc-dc converter markets, where the buck converter currently dominates. This work aims to address the challenges in designing and controlling the SC converter, and to unleash the full potential of the Switched Capacitor dc-dc converter.

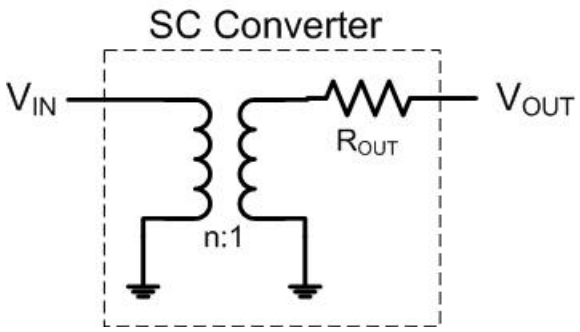


Figure 1.1: Basic model for an SC converter

1.1 The model used for SC converter

Before a discussion of the benefits of using an SC converter, a review of the SC converter model and operation is provided in this section. This model has been discussed in references [2, 3, 5, 4], so only a brief summary will be included here. Figure 1.2(a) shows a simple 3:1 SC converter using the Dickson topology[6]. This SC converter is a two phase circuit with nominally 50% duty cycle. By connecting the power-train capacitors differently in the two clock phases, the SC converter attains the nominally 3:1 voltage conversion ratio by charge sharing among the capacitors. As a beginning step [3], an SC converter can be modeled as an ideal transformer in series with an output referred resistance, R_{OUT}, as shown in figure 1.1. The turns ratio in the ideal transformer represents the unloaded conversion ratio of the converter. When the converter is loaded, this necessitates a voltage drop across the converter due to charge transfer and conduction loss, and this is represented by a voltage drop across R_{OUT}. There are two asymptotic limits to R_{OUT}, the slow switching limit (SSL), and the fast switching limit (FSL). In the SSL, capacitors are allowed to fully equilibriate within each clock phase, and charge transfer can be modeled as impulsive. In this limit, R_{OUT} is determined only by the switching frequency of the converter and the capacitors in the circuit, as explained in subsection 1.1.1. In the FSL, capacitor voltages remain constant, and current flow is modeled as being constant within each clock phase. In this limit, R_{OUT} is determined only by switches and other resistances in the converter, as explained in subsection 1.1.2. A combined result will be discussed in subsection 1.1.3.

This simplified model captures the series conduction loss of an SC converter. Other major losses, namely switching loss due to gate switching, can be modeled as parallel losses. This can be modeled as a resistor in parallel with the output terminal in figure 1.1. For simplicity this resistor is not included in the model but switching loss will be discussed separately in subsection 1.2.3.

1.1.1 SSL model of SC Converter

In the asymptotic slow switching limit (SSL), the output referred resistance R_{OUT}, denoted as R_{SSL}, is given by:

$$R_{SSL} = \sum_{i \epsilon caps} \frac{(a_{c,i})^2}{f_{SW} C_i} \tag{1.2}$$

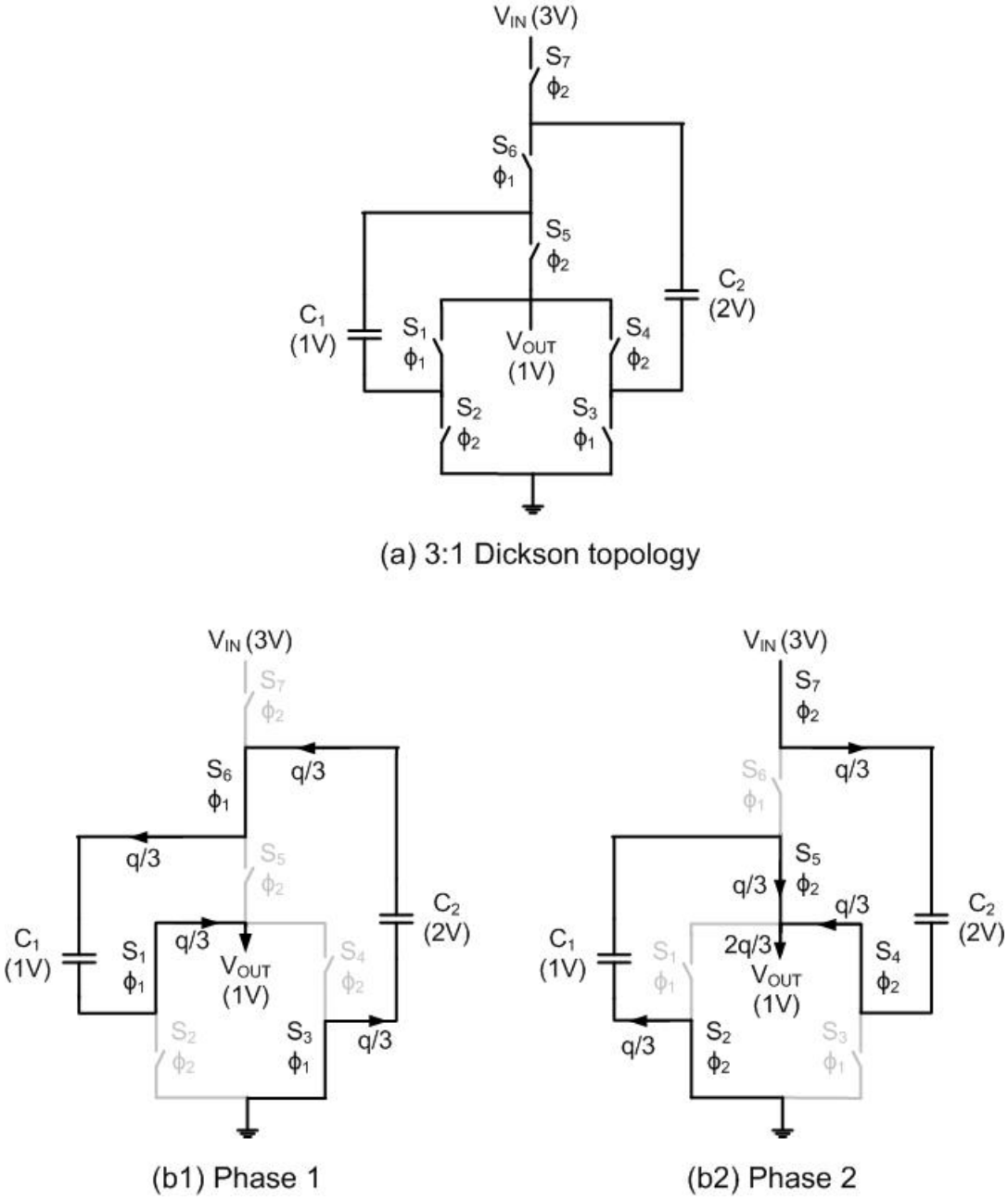


Figure 1.2: (a) Schematic and (b) charge flow of the 3V-to-1V Dickson Converter in the two clock phases.

where f_{SW} is the switching frequency of the converter, and C_i stands for the capacitance of capacitor C_i. Coefficient $a_{c,i}$ is called the charge multiplier coefficient; it is the ratio between the charge flow per period in C_i and the total output charge flow per period in steady state. Using the charge flow diagram of a 3:1 Dickson Converter [6] in figure 1.2 as an example, one can see that the total charge flow to the output is q, and the charge flow in both capacitors C_1 and C_2 are $q/3$. Thus $a_{c,1} = a_{c,2} = 1/3$. If $C_1 = C_2 = 1\mu F$ and $f_{SW} = 1MHz$, R_{SSL} is calculated to be $2/9\Omega$.

For a given R_{SSL} and frequency, one can optimally size C_i to give the lowest total capacitor energy storage requirement. This energy, denoted as E_{TOT}, is given by:

$$E_{TOT} = \sum_{i \epsilon caps} \frac{1}{2} C_i \left(v_{c,i(rated)}\right)^2 \tag{1.3}$$

where $v_{c,i(rated)}$ is the rated voltage of the capacitor. The rated voltage of the capacitor needs to be at least its blocking voltage, and is subjected to the constraint of available technology. In figure 1.2, the blocking voltage of capacitor C_2 is $2V$, and thus $v_{c,2(rated)} \geqslant 2V$. The optimally sized C_i is given by:

$$C_i = \left| \frac{a_{c,i}}{v_{c,i(rated)}} \right| \frac{2E_{TOT}}{\sum_{k \epsilon caps} \left| a_{c,k} v_{c,k(rated)} \right|} \tag{1.4}$$

and the resulting R_{SSL} is given by:

$$R_{SSL} = \frac{1}{2E_{TOT} f_{SW}} \left(\sum_{i \epsilon caps} \left| a_{c,i} v_{c,i(rated)} \right| \right)^2 \tag{1.5}$$

For the circuit in figure 1.2, using a target $R_{SSL}$of $2/9\Omega$, $f_{SW} = 1MHz$ and $v_{c,i(rated)}$ equals to the respective blocking voltage, equation 1.5 shows that $E_{TOT} = (9/4)\,\mu J$. Using equation 1.4, one can show that the optimal sizing is $C_1 = 1.5\mu F$ and $C_2 = 0.75\mu F$. Since E_{TOT} is roughly proportional to the printed circuit board (PCB) area of discrete capacitors or silicon area of integrated capacitors, this optimization methodology can help to attain the smallest PCB footprint or silicon area of an SC converter for a given R_{SSL}.

1.1.2 FSL model of SC Converter

In the asymptotic fast switching limit (FSL), the output referred resistance R_{OUT}, denoted as R_{FSL}, is given by:

$$R_{FSL} = \sum_{i \epsilon switches} \sum_{j \epsilon phases} \frac{R_i}{D_j} \left(a_{r,i}^j\right)^2 \tag{1.6}$$

where R_i is the resistance of switch S_i or other parasitic resistances, and D_j is the duty ratio of the jth phase. Coefficient $a_{r,i}^j$ is the charge multiplier coefficient, defined similarly to $a_{c,i}$ in SSL. It is the ratio between the charge flow per period in S_i in phase j and the total output charge flow per period in steady state. In figure 1.2, switch S_1 conducts charge $q/3$ in phase 1, but is off in phase 2. Thus $a_{r,1}^1 = 1/3$ and $a_{r,1}^2 = 0$. For the circuit in figure 1.2,

if each of the switches has a resistance of 1Ω and both clock phases have 50% duty ratio ($D_j = 0.5$), one can show that $R_{FSL} = 14/9\Omega$.

Similar to capacitors in SSL, there exists an optimal set of switch sizes that will give a required R_{FSL} while minimizing the total switch size, referred to as A_{TOT}. In an integrated circuit, this quantity is roughly proportional to area. This cost function, A_{TOT}, is given by:

$$A_{TOT} = \sum_{i \epsilon switches} G_i \left(v_{r,i(rated)}\right)^2 \tag{1.7}$$

where $G_i = 1/R_i$ is the conductance of switch S_i, and $v_{r,i(rated)}$ is its rated voltage. Analogously to capacitors, the rated voltage of the switch needs to be at least its blocking voltage, and is subjected to the constraint of available technologies. For the circuit in figure 1.2, switch S_6 blocks $2V$, whereas all other switches block $1V$. The cost function, represented by equation 1.7, reflects typical technology behavior in both CMOS (complimentary metal oxide semiconductor) and LDMOS (laterally diffused metal oxide semiconductor) switches. When practical devices deviate from this assumption, one can account for this by using a method similar to the one outlined in section 2.3. If only switch resistances are being considered and duty ratio $D_1 = D_2 = D$, the optimal switch conductance G_i is given by:

$$G_i = \left|\frac{a_{r,i}}{v_{r,i(rated)}}\right| \frac{A_{TOT}}{\sum_{k \epsilon switched} \left|a_{r,k} v_{r,k(rated)}\right|} \tag{1.8}$$

and the resulting R_{FSL} is given by:

$$R_{FSL} = \frac{1}{D * A_{TOT}} \left(\sum_{i \epsilon switches} \left|a_{r,i} v_{r,i(rated)}\right| \right)^2 \tag{1.9}$$

For the circuit in figure 1.2, using a target R_{FSL} of $14/9\Omega$, $D_1 = D_2 = 0.5$ and $v_{r,i(rated)}$ equal to the respective switch blocking voltage, equation 1.9 shows that $A_{TOT} = 64/7$. Using equation 1.8, one can show that the optimal sizing is $G_6 = 4/7$, and $G_i = 8/7$ for all other switches. Since A_{TOT} roughly corresponds to the die area of integrated switches, this optimization methodology can help to attain the smallest die area of an SC converter for a given R_{FSL}.

1.1.3 Combined model of SC Converter

While subsections 1.1.1 and 1.1.2 discuss output referred resistances (R_{OUT}) in the SSL and the FSL, a real design usually lies somewhere between these two asymptotic limits. In the intermediate region, charge flow between capacitors in each clock phase will be neither impulsive nor constant, but will decay with a settling time constant. Deriving an algebraic expression for R_{OUT} in this region is inconvenient [5], but it can be approximated by combining R_{SSL} and R_{FSL} as follows:

$$R_{OUT} \approx \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{1.10}$$

When the cost of both capacitors and switches are important, the optimal design strategy will be to set $R_{SSL} \approx R_{FSL}$, and then to independently optimize capacitors and switches

using the methodology outlined in subsections 1.1.1 and 1.1.2, respectively. If the design is capacitor constrained, one may want to pick $R_{SSL} > R_{FSL}$ and vice versa if the design is switch constrained. The analysis and optimization methodology outlined in this section are very useful in evaluating and designing an SC converter, and they will be the basis for discussions in the following sections and chapters. Further background information can be found in reference [5] for the interested reader.

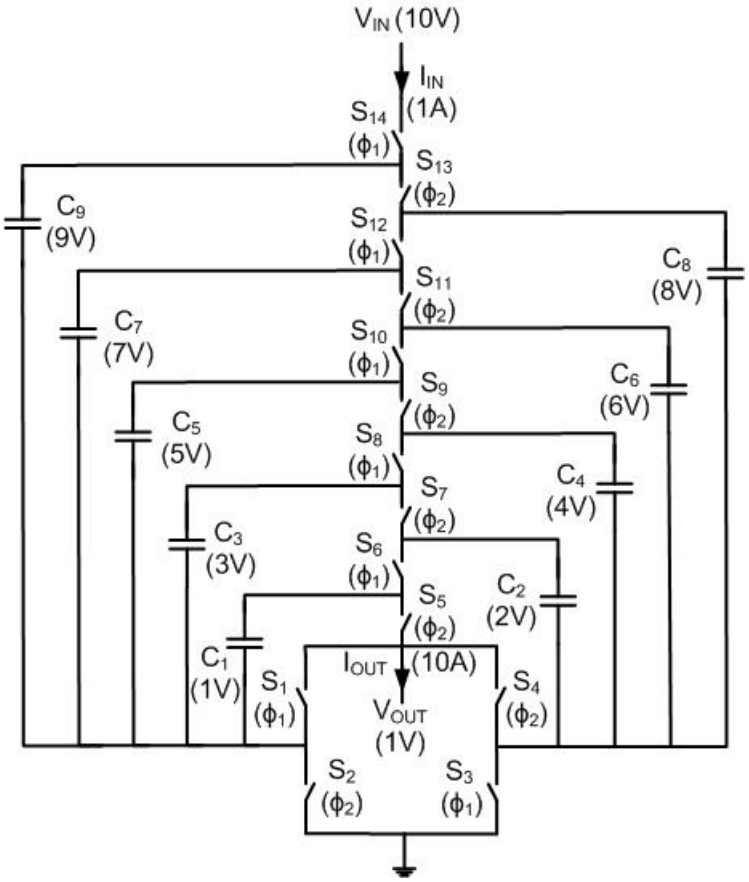
1.2 Advantages of SC converters

The main criteria for evaluating voltage regulators are: component costs, power efficiency, and regulation performance. This section will show that the SC converter is advantageous in both costs and efficiency when compared to the inductor-based buck converter - the dominant architecture for dc-dc converters. Regulation, however, can be a concern, and it will be discussed in detail in chapter 3. The component costs of a dc-dc converter can be divided into two main categories, active elements (switches) or passive elements (capacitors or inductors), and can be measured in terms of manufacturing cost, PCB area, and die area. Subsections 1.2.1 and 1.2.2 will use these metrics to discuss active and passive elements respectively. The power loss of a dc-dc converter can also be divided into two main categories, conduction loss and switching loss. Conduction loss of a dc-dc converter is a series loss component and is dominated by its active elements and passive elements. Switching loss, on the other hand, is a parallel loss and will be discussed separately in subsection 1.2.3. While there are many different SC converter topologies, this section will focus on the Dickson topology [6] since it is the topology chosen in this work. The reason for choosing the Dickson topology will be discussed in section 2.1.

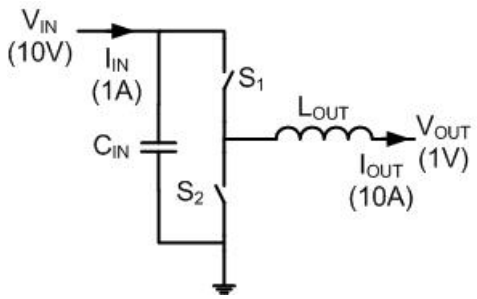
1.2.1 Active element analysis

To compare active element (switches) utilization among power converters, one can use the switch stress parameter $G-V^2$ product [31]. A higher $G-V^2$ product means higher switch stress, and it usually entails more costly or larger PCB area for discrete switches or a larger die area for integrated switches with a target power loss. The $G-V^2$ switch stress of an SC converter is compared to the buck converter using an example given in figure 1.3. Figure 1.3a shows an SC converter using the Dickson topology, whereas figure 1.3b shows a buck converter. Both converters are stepping down from 10V to 1V and with an output current of 1A. A comparison between these two converters is done by comparing the effective output resistance, R_{OUT}, of both converters for a given cost function, A_{TOT}, as shown in equation 1.7. For simplicity, A_{TOT} is set to be 1 in the comparison.

In terms of the SC converter, as discussed in section 1.1, switches only matter in the FSL calculations but not in the SSL calculations, and thus this subsection will focus on an SC converter operating in the FSL. Although peak current through a switch is infinite in SSL, the switches can be reduced in size to lower this peak current without deteriorating R_{OUT}. Thus the real switch stress of an SC converter can be evaluated when it is operating in the FSL, and can no longer reduce peak current without affecting R_{OUT}. For the example in figure 1.3a, the charge multiplier coefficients, $a_{r,5-14}$, $= 1/10$ for switches $S_5 - S_{14}$, whereas



(a) A 10V-to-1V Dickson SC converter



(b) A 10V-to-1V buck converter

Figure 1.3: 10V-to-1V SC converter and buck converter

$a_{r,1,2} = 5/10$ and $a_{r,3,4} = 4/10$ for switches 1,2 and 3,4 respectively. In terms of blocking voltage, switches $S_1 - S_5$ block $1V$ whereas switches $S_6 - S_{13}$ block $2V$. Thus using equation 1.9, the output impedance $R_{OUT}(\sim R_{FSL})$ of the SC converter equals is 26Ω for $D = 0.5$ and when $A_{TOT} = 1$. In terms of the buck converter, since the duty factor is 0.1, $R_{OUT} = 0.1/G_1 + 0.9/G_2$, where G_1 and G_2 are the switch conductance of switches S_1 and S_2 respectively. The optimal sizing of switches S_1 and S_2 is such that $G_2 = 3G_1$. Since both switches block 10V, $A_{TOT} = \sum GV^2 = 400G_1$. Setting $A_{TOT} = 1$, $G_1 = 1/400$. Thus $R_{OUT} = 0.1/G_1 + 0.9/G_2 = 160$ for the buck converter.

In this simple example, the buck converter has an output impedance, R_{OUT}, that is more than seven times as high as that of the SC converter, and thus the SC converter is much superior in terms of switch utilization. As shown in references [3, 5], this advantage increases further as conversion ratio increases, and this makes the SC converter even more favorable. References [5, 4] further show that the Dickson SC converter is at the switch utilization fundamental limit of dc-dc converters derived in [7], meaning that no other dc-dc converter, whether inductor-based or capacitor-based, can have a better switch utilization than the Dickson SC converter.

Further, the Dickson SC converter only requires low voltage transistors, making it possible to only use native transistors in a CMOS process. The buck converter, on the other hand, requires high voltage transistors, and thus may require LDMOS transistors when switches are integrated. This can increase the complexity of the process and increase manufacturing cost. However, if discrete transistors are used, it may be possible to manufacture the high voltage transistors with a low cost legacy technology. As a conclusion for switches, due to its low $G - V^2$ product and low switch blocking voltage, the Dickson SC converter will likely have lower manufacturing cost, smaller die area, and thus lower overall cost for switches.

1.2.2 Passive element analysis

The Dickson topology chosen in this work is superior in switch utilization, but not in capacitors when compared to other SC topologies [3]. However, its passive component utilization and that of other SC topologies are still superior to the buck converter when one takes into account the comparative energy density of capacitors and inductors. Table 1.1 shows the dimension and energy density of representative discrete capacitors and inductors [5]. By inspection, surveyed capacitors have a volumetric energy density that is over 1000 times higher than that of surveyed inductors. This more than compensates for the weaker reactive element utilization of the Dickson topology when compared with the buck converter and other SC topologies [4]. Moreover, as will be shown in section 5.5, discrete capacitors used in SC converters are usually an order of magnitude cheaper than the discrete inductors used in buck converters. When integrated passives are used, references [8, 4] further shows that an SC converter can achieve a power density that is orders of magnitude higher than that of the buck converter [9, 10]. With a superior passive component utilization, SC converters can potentially have lower passive component cost and PCB/die area for a given amount of power loss, or equivalently attain a higher efficiency with the same amount of resources, when compared to the buck converter.

Table 1.1: Energy density of common capacitors and inductors

Type	Manufacturer	Capacitance	Dimensions $[mm^3]$	Energy density
Ceramic Cap	Taiyo-Yuden	$22\mu F@4V$	$1.6 * 0.8 * 0.8$	$344\mu J/mm^3$
Ceramic Cap	Taiyo-Yuden	$1\mu F@35V$	$1.6 * 0.8 * 0.8$	$1196\mu J/mm^3$
Tantalum Cap	Vishay	$10\mu F@4V$	$1.0 * 0.5 * 0.6$	$533\mu J/mm^3$
Tantalum Cap	Vishay	$100\mu F@6.3V$	$2.4 * 1.45 * 1.1$	$1037\mu J/mm^3$
Electrolytic Cap	Kemet	$22\mu F@16V$	$7.3 * 4.3 * 1.9$	$94\mu J/mm^3$
Electrolytic Cap	C.D.E	$210mF@50V$	$76\phi * 219$	$172\mu J/mm^3$
Shielded SMT Ind	Coilcraft	$10\mu H@0.2A$	$2.6 * 2.1 * 1.8$	$0.045\mu J/mm^3$
Shielded SMT Ind	Coilcraft	$100\mu H@0.1A$	$3.4 * 3.0 * 2.0$	$0.049\mu J/mm^3$
Shielded Inductor	Coilcraft	$170\mu H@1.0A$	$11 * 11 * 9.5$	$0.148\mu J/mm^3$
Shielded Inductor	Murata	$1mH@2.4A$	$29.8\phi * 21.8$	$0.189\mu J/mm^3$

1.2.3 Switching loss analysis

While the SC converter is superior to the buck converter in terms of both active and passive components, this only represent series loss. A complete analysis of power loss requires the consideration of parallel loss, which is dominated by switching loss. The main switching loss in an SC converter is due to the voltage fluctuations in the power-train capacitors, but this has already been accounted for in the SSL calculation of conduction loss. The other switching losses, gate drive and parasitic capacitance, are common to both the SC converter and buck converter. However, the buck converter has an additional switching loss component due to inductive commutation of current from one switch to another. This leads to power loss when both current and voltage appear across a switch during phase transition. While resonant methods like zero-current switching (ZCS) and zero-voltage switching (ZVS) can reduce this loss[11, 12, 13], this loss still remains a significant portion of the total switching loss of a buck converter in most cases. The SC converter is in a clear advantage in this aspect as current goes to zero right after a switch turns off unless there is significant parasitic inductance. A parasitic inductance can lead to a dissipation of its stored energy at the end of a conduction period, but with values in the orders of nH for the converters built in this work, this loss is negligible. While parasitic inductances do not lead to significant power loss, they can lead to over voltage stress for some circuits, and this necessitates the inclusion of protection circuits to be discussed in chapter 4, section 4.11.

In terms of the switching losses that are common to both the SC converter and the buck converter, the SC converter benefits from having a lower voltage swing in all of its switching nodes. Using figure 1.3 as an example, no nodes in the SC converter need to swing more than 2V, whereas the internal node in the buck converter needs to swing 10V. Since capacitive loss is proportional to the square of the voltage swing, this will likely lead to a much higher loss for the buck converter. In the case of an SC converter using integrated capacitors, there is capacitor bottom plate parasitic capacitance that is absent in the buck converter [8]. However, this capacitance is negligible for discrete passives. All of these factors add up to allow the SC converter to have much lower switching loss than a buck converter. With an advantage in both conduction loss and switching loss, the SC converter has a total power loss that is lower than that of the buck converter in an optimized design.

1.3 Target applications of this work

After discussing the advantages of the SC converter in section 1.2, the following chapters will discuss the methods to realize them in a real design. The point-of-load application is chosen as the target application because it is an important one dominated by the buck converter. By showing the superiority of the SC converter in this area, this work will show that the applications for SC converters can be greatly expanded. The specification of this work is a dc-dc converter stepping down to 1.5V with an input voltage range of 7.5V-13V, and with an output current of 1A.

This moderate conversion ratio is chosen because it is common for many applications. For example, the laptop computer power converter may need to step down from 10-16V down to 1-2V. Further, most telecommunication and network switching systems include on-board power supplies that step down from 12V to 1-2V. This market is currently dominated by the buck converter and constitutes a significant proportion of the overall dc-dc converter market. This market section requires a conversion ratio that has not been attempted by any SC converters to the best of the author's knowledge. Most SC converters operate with a conversion ratio of less than 4-to-1, and thus a successful 8-to-1 SC converter expands the scope of SC converters into this vast market. Coincidentally, the benefits of using an SC converter increase with higher conversion ratio, and thus this choice of conversion ratio is also a strategic opportunity to showcase the superiority of the SC converter. A higher conversion ratio is not chosen because the number of components and complexity of the converter increases with conversion ratio. A moderate conversion ratio represents a trade-off between the potential relative benefit and the complexity of the circuit.

The moderate output current of 1A is chosen because this current level is significantly higher than the typical values for SC converters in the market. Most SC converters not only have a low conversion ratio, but also have current levels below 100mA. However, many applications dictate load current well above 1A, for example a microprocessor can draw up to 100A of current. Being able to supply high current is an important market segment as electronics become more power hungry. These applications are exclusively dominated by the buck converter, and thus it will be groundbreaking to show that the SC converter not only can achieve similar results but can do even better. A load current level exceeding 1A is not chosen because those converters are usually multi-phase and built with many smaller converters bundled together. Although one can apply multi-phase technique to SC converters as well, this nonetheless adds another layer of complexity to the design. Since the purpose of this work is path-finding, it is strategic to limit the complexity and not try to reach the end goal in one step. An output current level of 1A is a typical current level for a single phase buck converter in the market, and thus using a single phase SC converter for this work will be a fair comparison.

In terms of integration, most buck converters with similar conversion ratio and output current use integrated switches and off-chip inductors. Thus this work utilizes integrated switches and off-chip passives, namely capacitors, as well. The chips fabricated in this work utilize the $0.18\mu m/0.6\mu m$ (CMOS + LDMOS) process from National Semiconductor. This technology node is popular among power converters for this application. Chapters 2 and 3 discuss the architecture and control algorithm of this work, and chapter 4 discusses the circuit designs. Chapter 5 discusses the test results of the test chips, and compares them

with other works from industry and literature. The culminating test chip obtains a peak efficiency of 92%, and maintains an efficiency higher than 80% from 5mA to 1A of output current. This performance not only far exceeds that of the surveyed SC converters, but also exceeds that of surveyed buck converters. Further, the PCB footprint of the capacitors in this work is only a fraction of the PCB footprint area of the inductors in the surveyed buck converters. These results show that the SC converter can be more than competitive in an area where the buck converter has dominated for decades. Chapter 6 concludes this work and discusses future opportunities to further expand the potential of the SC converter.

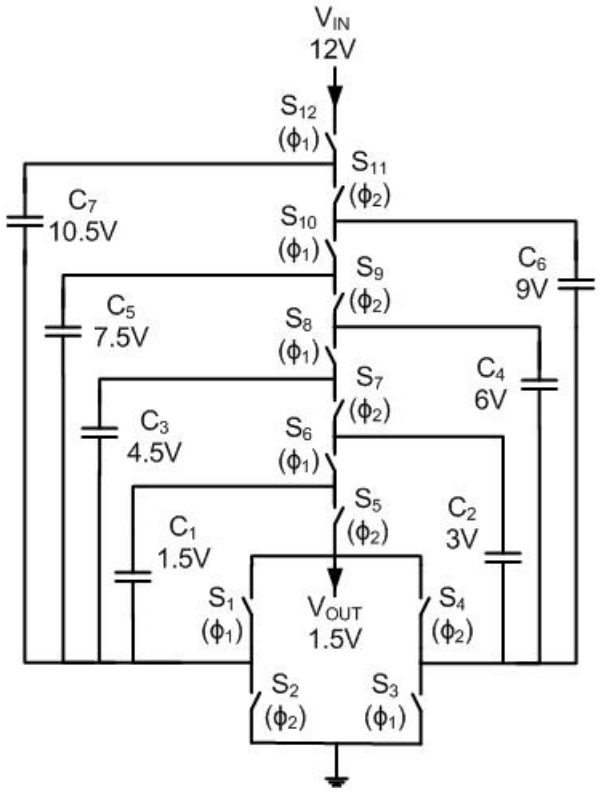
Chapter 2

Architecture

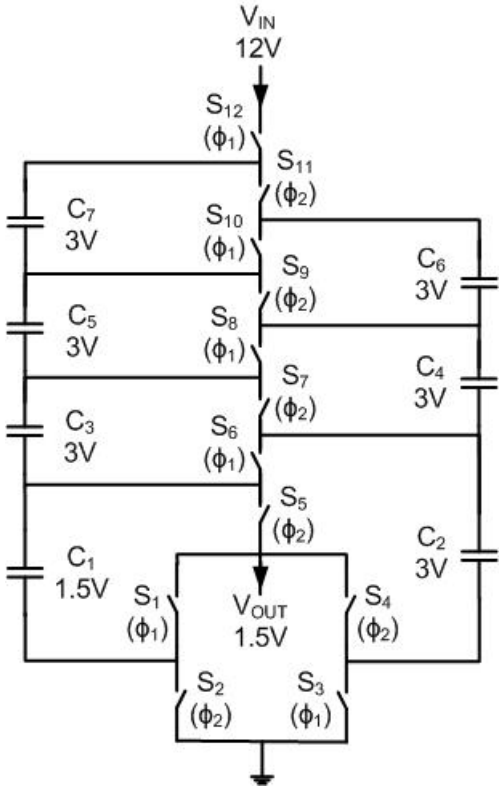
After discussing the motivation and specification of this work in Chapter 1, this chapter discusses the architecture of the converter. A 12V-to-1.5V dc-dc converter is implemented using off-chip ceramic capacitors and integrated switches in a $0.18\mu m/0.6\mu m$ process. Ceramic capacitors are chosen due to their high energy density and low R_{ESR}(equivalent series resistance). These attributes allow a low R_{OUT} while having a small PCB footprint. The switching frequency of the converter can be varied, and is designed to go up to $5MHz$. Varying switching frequency can be used to optimize power loss [19] as explained in subsection 2.3.3, or to achieve regulation [21] as explained in section 3.1. The frequency is limited at $5MHz$ because the ESR corner frequency of the ceramic capacitors is around this frequency and going beyond this point has little benefit in either efficiency or regulation. The following sections will discuss in detail the architecture of the converter, and the ways to achieve the best performance.

2.1 Topology choice

The topology chosen is the 12V-to-1.5V (8:1) Dickson converter. It is shown in figure 2.1 with two different capacitor configurations: (a) star and (b) ladder. In terms of switches, these two configurations are identical, with the same blocking voltage and current flow for each switch. In terms of capacitors, by using equation 1.5, one can show that they both require the same total capacitor energy storage capacity (E_{TOT}, eq. 1.3) to achieve a given output referred resistance in the slow switching limit (R_{SSL}). These two configurations are basically equivalent but have subtle differences in practice. Although both configurations give the same E_{TOT} requirement, ceramic capacitors have a higher energy density per volume for a part with a higher rated voltage. Since the star configuration uses higher voltage capacitors, it will benefit from a higher E_{TOT} and thus have a lower R_{SSL} for a given volume of ceramic capacitors. However, the ladder configuration has a more favorable transient response than the star configuration. For example, when the input voltage increases, all the capacitor voltages will have to increase since the conversion ratio is fixed at 8-to-1. The ladder configuration will allow this to occur more uniformly since the capacitors are connected in series. On the other hand, the star configuration would require several switching periods before the equilibrium voltage levels are reached. Thus the ladder configuration should be



(a) Capacitors in "star" configuration



(b) Capacitors in "ladder" configuration

Figure 2.1: 12V-to-1.5V Dickson SC converter

used when line regulation is taken into account.

There are many SC converter topologies, and for those compared and contrasted in [3], some are better in terms of switch utilization while others are better in terms of capacitor utilization. The Dickson topology chosen in this work has good switch utilization but is not as good in terms of capacitor utilization. This work made this choice because capacitance is in abundance due to the usage of off-chip capacitors but switches are integrated and a larger die area leads to a higher cost. When compared to the other topologies that have similar switch utilization, for example the ladder topology, the Dickson converter is chosen because it has fewer capacitors. This gives a minimum number of I/O pins and off-chip components. These translate to a lower pad overhead on the die, and a smaller PCB footprint and thus a lower cost for the converter.

Considering the implementation of the switches, the process used in this work has two choices of CMOS transistors: the $0.18\mu m$ transistor with a rated voltage of 1.8V and the $0.6\mu m$ transistor with a rated voltage of 5V. Switches $S_1 - S_5$ block 1.5V and are implemented with 1.8V transistors; whereas switches $S_6 - S_{11}$ need to block 3V and are implemented with 5V transistors. Switch S_{12} only needs to block 1.5V, but due to the way in which switches are driven, as explained in section 2.2, it is also implemented with a 5V transistor. Since these voltage blocking levels match well with these devices, this process is a very appropriate choice. All of these switches are driven in a two phase manner as indicated in figure 2.1. The configuration in each phase can be obtained by using a diagram similar to figure 1.2. The two phase clocks are non-overlapping to prevent direct current flow that can short out a power-train capacitor and cause significant power loss.

2.2 Multiple voltage domains

The converter is subjected to an input voltage of 12V, and yet it is made up of transistors with a rated voltage of 5V or less. In order to prevent over-voltage stress of any of these devices, the silicon chip is divided into numerous voltage domains isolated from the substrate by deep n-well structures. Communication across voltage domains is achieved by using the levelshifter circuit discussed in section 4.1. Figure 2.2 shows the 9 different voltage domains in the converter, and the arrows next to the switches indicate which voltage domain the switch resides in. This figure uses the ladder-type capacitor configuration, but a similar design can also be obtained by using the star-type capacitor configuration. When compared with figure 2.1b, figure 2.2 has 1 more capacitor, C_8, and 1 more switch, S_{13}. These two components are added to create voltage domain 9 that drives switches S_{11} and S_{12}. This is a 3V voltage domain, and thus switch S_{12} is implemented with 5V transistor even though it only needs to block 1.5V. When compared to figure 2.1b, switch S_{12} is connected to the top plate of C_8 instead of C_7. These two implementations of S_{12} are equivalent since when S_{12} turns on in clock phase 1, the top plate of C_7 and C_8 are connected. Switch S_{12} is implemented this way so that it can be a PMOS transistor driven easily by voltage domain 9. Although capacitor C_8 can be implemented with much reduced capacitance, it is nonetheless implemented with off-chip ceramic capacitors for the sake of uniformity. There may be benefits in moving it on-chip and reducing the required PCB area.

By separating the die into different voltage domains, no switch sees a voltage stress higher

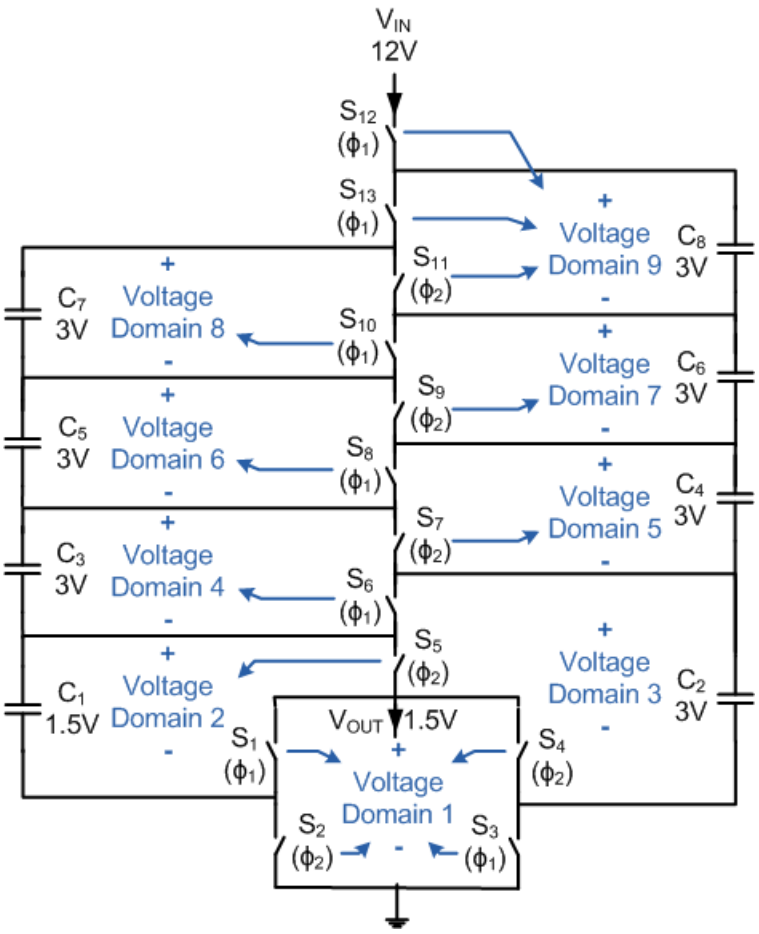


Figure 2.2: Various voltage domains of the 12V-to-1.5V Dickson converter. The arrows indicate which voltage domains the switches reside in.

than 3V even though some nodes may be more than 12V above the substrate voltage level. The only junctions that need to withstand a voltage level higher than 3V are the n-well to p-substrate p-n junction. These junctions can withstand a higher voltage level, exceeding 15V, due to the low dopant level in the substrate of the CMOS process. For example, switch S_{10} is implemented using a 5V NMOS transistor residing in voltage domain 8. This voltage domain is across capacitor C_7, which has a nearly constant voltage level in both clock phases. The body of the NMOS switch is connected to the lower rail of the voltage domain, whereas its deep n-well is connected to the upper rail of the voltage domain. Its gate is driven by a driver also implemented in the same voltage domain. Thus both switch S_{10} and its driver operate with a safe voltage of 3V even though the top plate of capacitor C_7 is at 12V in clock phase 1.

This biasing scheme results in numerous p and n layers at various voltage levels and this leads to a concern of latch-up. However, reference [14] shows that the triple well structure using deep n-well is latch-up free because the parasitic thyristor structure is absent. One can show that the biasing scheme in this converter preserves this immunity to latchup by also having no parasitic thyristors. However, a parasitic thyristor can exist if within any

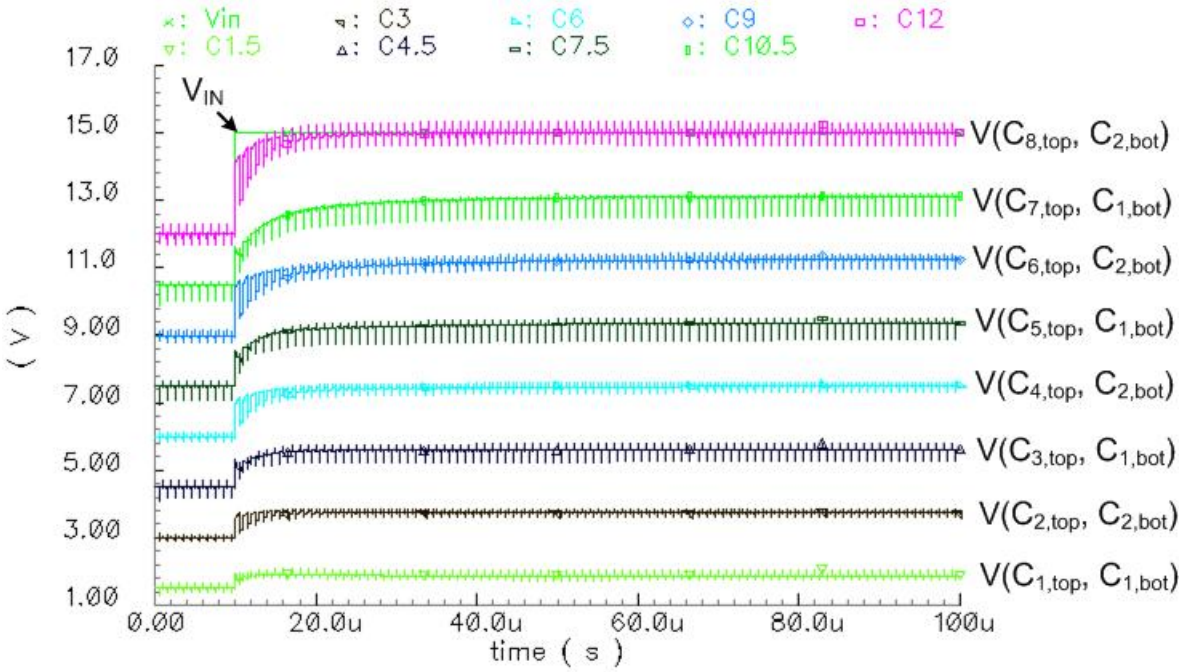
voltage domain, the n-well of a PMOS device is merged with the deep n-well of an NMOS device [15]. This creates a parasitic thyristor similar to the familiar case in a non-triple-well CMOS process [16]. However, this threat of latch-up is no greater than that in the familiar CMOS case, and should already have been considered when the design rules were written. Nonetheless, by the virtue of conservative layout, this layout merger is avoided in this work, and the two types of transistors are always placed in separate wells. Latch-up has not been observed during testing of any version of the fabricated devices.

One consideration of using voltage domains defined by power train capacitors is that it also favors the usage of the ladder type capacitor configuration over the star type capacitor configuration. When there is a rapid change in the input voltage, all power-train capacitor voltages will change in the same direction if the capacitor configuration is ladder-type. This spreads out the change in input voltage by capacitive division. On the other hand, if a star configuration is being used, only the voltage of capacitor C_7 in figure 2.1a will change initially, and it will take many clock cycles before the other capacitors reach the new equilibrium voltage levels. This is illustrated by simulation results shown in figure 2.3. The simulations show how the power-train capacitor voltage levels change when the input voltage steps from 12V to 15V. Figure 2.3a shows the case when a ladder configuration is used, whereas figure 2.3b shows the case when a star configuration is used. The converter is switching at a constant frequency of 1MHz in both cases. In both cases, the top plate of C_8 is pulled up immediately since the body diode of PMOS transistor S_{12} is turned on. As shown in the simulations, the star configuration takes significantly longer time to attain symmetric division among the voltage levels. More significantly, in the simulation of the star configuration in figure 2.3b, the voltage level of voltage domain 9 is increased substantially with respect to the other voltage domains in the beginning of the transient. This can cause the levelshifter circuit discussed in section 4.1 to fail. This is a major consideration that motivates the use of the ladder configuration. It can be shown that a similar effect occurs when the conversion ratio of the converter changes. Design for multiple conversion ratios is discussed in section 2.4.

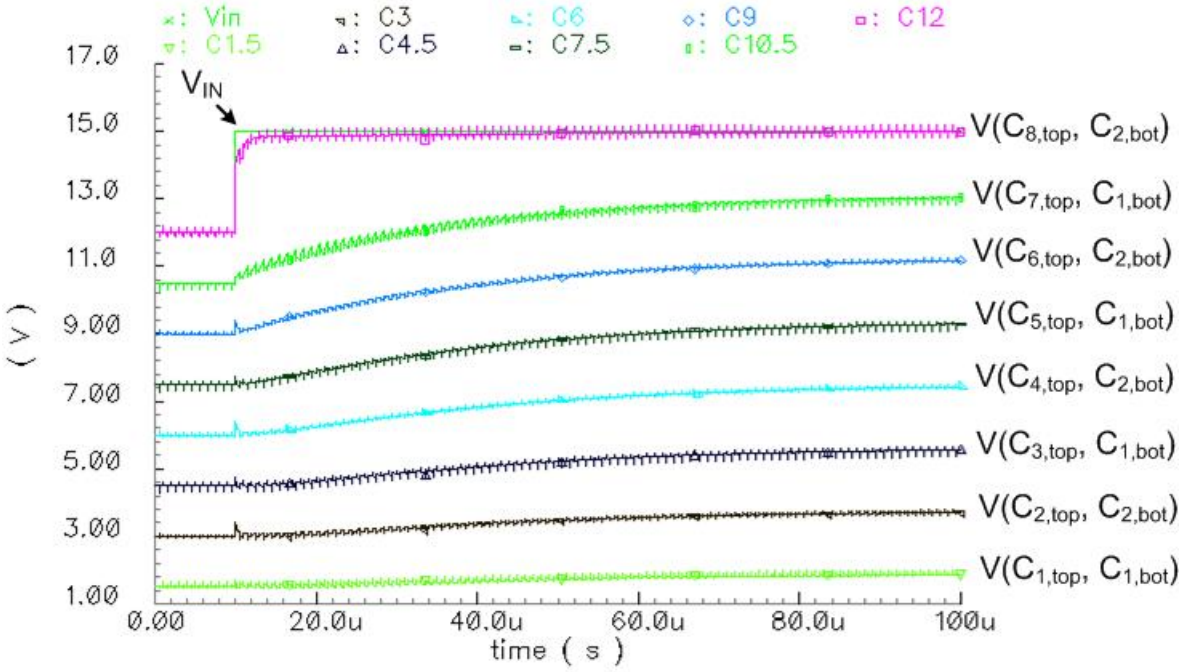
2.3 Device sizing and optimization

2.3.1 Capacitor Sizing

After determining the topology of the converter, one needs to choose the individual sizes of each capacitor and switch to minimize PCB area and die area. For all the off-chip capacitors, the high value multilayer ceramic capacitors with size 0603 (16mm*8mm) from Taiyo-Yuden with code X5R are chosen. Size 0603 capacitors are chosen for their high capacitance, which reduces R_{SSL} to a fraction of R_{FSL} at a switching frequency of $1MHz$, as discussed in chapter 5. There may be a strategic choice in using smaller size capacitors to reduce PCB area, but this route is not taken because 0402 capacitors have significantly reduced energy density. The capacitance of each capacitor is then picked by choosing the part with the maximum capacitance that has an ESR corner frequency exceeding $5MHz$ and with a rated voltage exceeding the blocking voltage requirement. The optimization scheme outlined in subsection 1.1.1 is not used because the major cost, PCB area, is fixed and does not scale with E_{TOT} as defined by equation 1.3. However, the optimization scheme can be useful if capacitor sizes



(a) When the capacitors are in a ladder configuration



(b) When the capacitors are in a star configuration

Figure 2.3: Changes in power-train capacitor voltage levels for a step change in input voltage

are more granular in a different design setting.

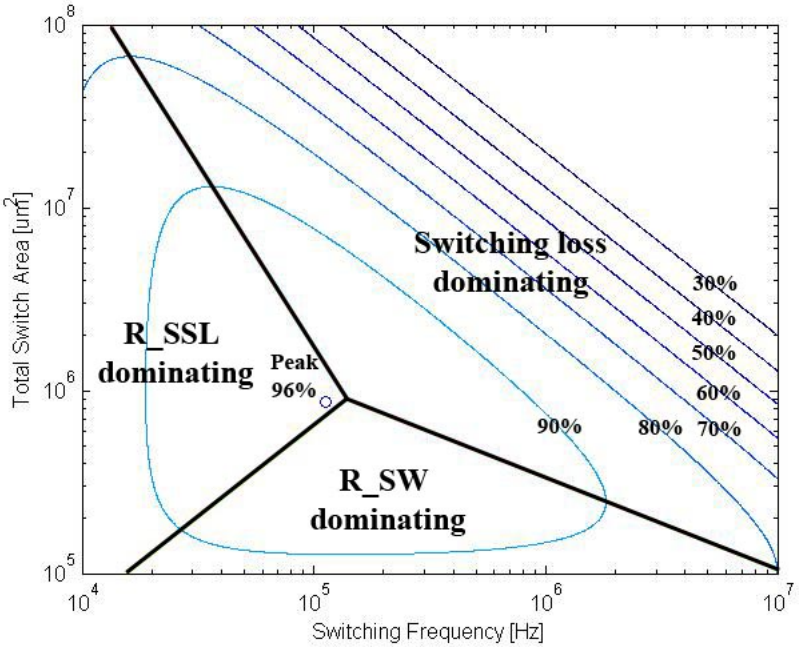
2.3.2 Switch sizing

The switches in this design are integrated and their sizes can vary smoothly. Thus, unlike the capacitors, the optimization scheme outlined in subsection 1.1.2 becomes useful. Instead of using the scheme directly, this work modifies it slightly to reflect the actual data from the process. The cost function being optimized, as defined in equation 1.7, assumes that switch area is proportional to GV_{rated}^2, where G is the conductance of the switch and V_{rated} is its rated voltage. While this assumption is roughly true for the active area of a CMOS transistor, a real transistor layout deviates from this due to many factors, including carrier mobility, gate drive, contact layout overhead etc. However, one can capture most of these factors by assigning a number to V_{rated}^2 that need not be the rated voltage of the switch. Parameter V_{rated}^2 is a weight in the optimization to capture the relative cost of the different types of switches, and it can be used to capture any factor that the designer considers. In this work, it is used to capture the real layout area of switches. First, V_{rated}^2 is set to 1 for the 1.8V NMOS transistor. Then V_{rated}^2 for another transistor type is defined as the area it occupies in mm^2 in order to have the same conductance as $1mm^2$ of 1.8V NMOS transistor. After V_{rated}^2 is determined for each of the switch types, equations 1.8 and 1.9 can be used to determine the optimal size of each switch in the converter for a target R_{FSL} or total switch area.

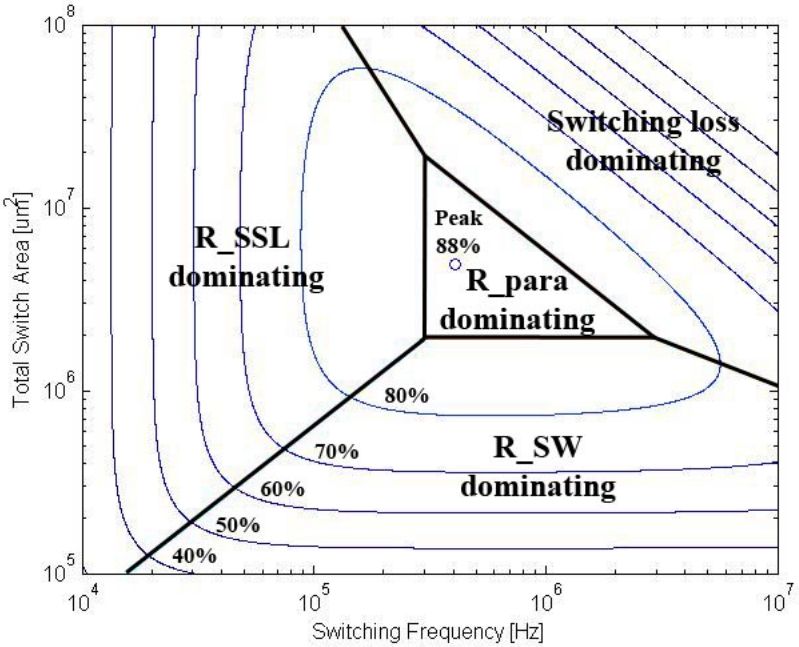
2.3.3 Overall optimization

After the sizes of the capacitors and the relative sizes of the switches are determined, the next step is to determine the optimal switching frequency and total switch area for the converter. This can be done by numerical optimization using contour plots [5]. Figure 2.4 shows the efficiency contours of an SC converter for various total switch areas and switching frequencies. At small total switch areas, the power loss is dominated by conduction loss due to switch resistances, R_{SW}. This is given by R_{FSL} defined in equation 1.6 by only considering switch resistances. At low switching frequencies, the power loss is dominated by the conduction loss due to R_{SSL}, which is defined by equation 1.2. At large switch areas and high switching frequencies, the power loss is dominated by gate drive loss of the switches. Bottom plate capacitance is negligible in this design due to the use of off-chip capacitors, otherwise bottom-plate loss will be the dominant power loss at high frequencies and small switch area. The optimal total switch area and switching frequency is where the R_{SW} loss, the R_{SSL} loss, and the switching loss are all equal. This is indicated by the circle in figure 2.4.

At high output current levels, the conduction loss due to parasitic resistances may start to dominate. This is represented by the central region in figure 2.4b. The dominant power loss in this region is given by R_{FSL} defined in equation 1.6, but by only considering parasitic resistances. This parasitic resistance can be the equivalent series resistance of the capacitors (R_{ESR}), the interconnect bond-wire resistances, or other resistances that do not scale with switch area. As shown in figure 2.4, this central region only exists in figure 2.4b where output current is high, but not in figure 2.4a where output current is lower.



(a) Efficiency of the converter at 100mA output current.



(b) Efficiency of the converter at 1A output current.

Figure 2.4: Efficiency contours of an example SC converter for 2 different output current levels.

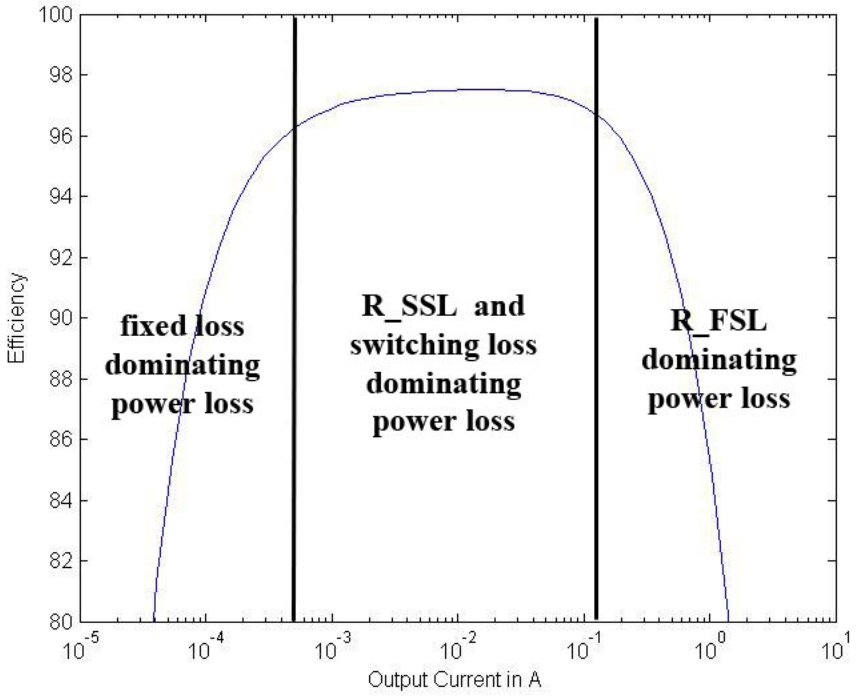


Figure 2.5: Efficiency versus output current for the example converter in figure 2.4 using a total switch area of $2mm^2$ and when switching frequency is optimized.

As shown in figures 2.4a and 2.4b, the optimal total switch area and switching frequency depend upon the output current level. While one can dynamically change switch area, it is not done here due to the complexity of such a design. This work chooses the total switch area based on the contour plot of the nominally full rated current level, then varies switching frequency when the converter operates at light load. The switching frequency can then be set such that the R_{SSL} loss, given by $I_{OUT}^2 R_{SSL}$, equals the gate drive switching loss, SW_{LOSS}. This is given by the following equation:

$$Freq = I_{OUT} * \sqrt{\frac{R_{SSL@1Hz}}{SW_{LOSS@1Hz}}} \tag{2.1}$$

where $R_{SSL@1Hz} = R_{SSL} * Freq$, $SW_{LOSS@1Hz} = SW_{LOSS}/Freq$. Figure 2.5 shows the resulting efficiency for this example converter at various output current levels if a total switch area of $2mm^2$ is chosen. At high current levels, the power loss is dominated by R_{FSL} loss of both power switches and parasitic resistances. At medium current levels, the power loss is dominated by both the R_{SSL} loss and the switching loss. At low current levels, the power loss is dominated by fixed losses, which includes power consumed by auxiliary control circuits.

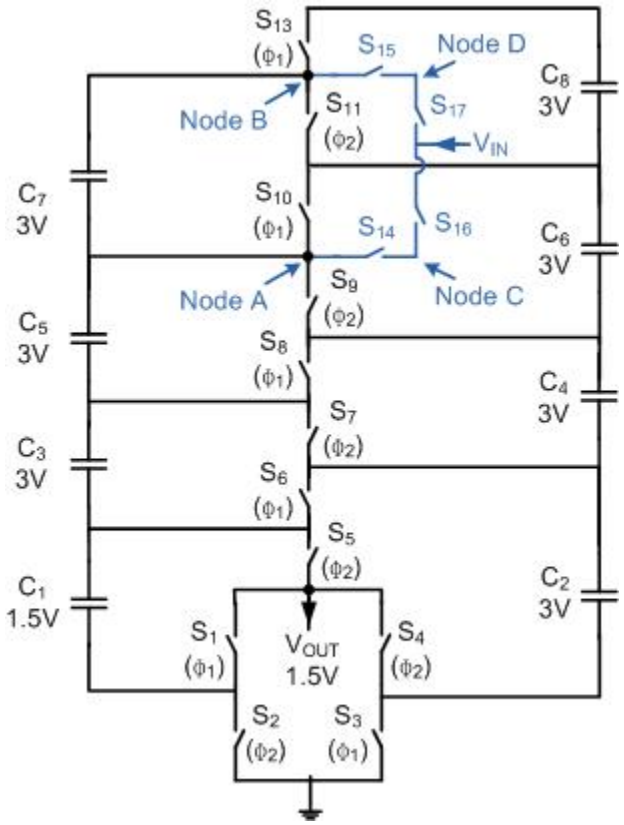


Figure 2.6: Dickson converter with multiple conversion ratio in integer step. Possible conversion ratios are 5:1, 6:1, 7:1 and 8:1

2.4 Multi-conversion-ratio design

The converter architecture described so far in sections 2.1 to 2.3 has a fixed conversion ratio of 8:1, but it can be extended to support multiple conversion ratios with small adjustments. Being able to support multiple conversion ratios is important when regulation is considered, as in chapter 3.

2.4.1 Integer step topology

By comparing the 10:1 converter in figure 1.3a with the 8:1 converter in figure 2.1a, one can see that the Dickson converter has a very regular structure. One can increase the conversion ratio simply by adding in more capacitors and extending the "ladder" structure in the center. Conversely, one can reduce the conversion ratio by connecting the input to one of the internal nodes within the ladder structure. One can also obtain a different conversion ratio by making a connection at the same node but at the opposite clock phase. Figure 2.6 shows a modification of the converter in figure 2.2 that will allow 4 different conversion ratios, namely 5:1, 6:1, 7:1 and 8:1. The converter in figure 2.6 replaces switch S_{12} in figure 2.2 with switches $S_{14} - S_{17}$. These switches are used to connect the input to the converter at either node A or B during during either clock phase 1 or clock phase 2. Table 2.1 shows

Table 2.1: Switch action table for the converter shown in figure 2.6

		Phase 1 ($\phi 1$)				Phase 2 ($\phi 2$)			
Conv ratio	V_{IN}	S_{14}	S_{15}	S_{16}	S_{17}	S_{14}	S_{15}	S_{16}	S_{17}
8:1	12V	*On*	*On*	Off	*On*	Off	Off	Off	*On*
7:1	10.5V	Off	Off	Off	*On*	*On*	*On*	Off	*On*
6:1	9V	*On*	*On*	*On*	Off	Off	Off	*On*	Off
5:1	7.5V	Off	Off	*On*	Off	*On*	*On*	*On*	Off

the actions of the switches to achieve the 4 different conversion ratios. The table also shows the corresponding input voltages that will give an unloaded output voltage of 1.5V.

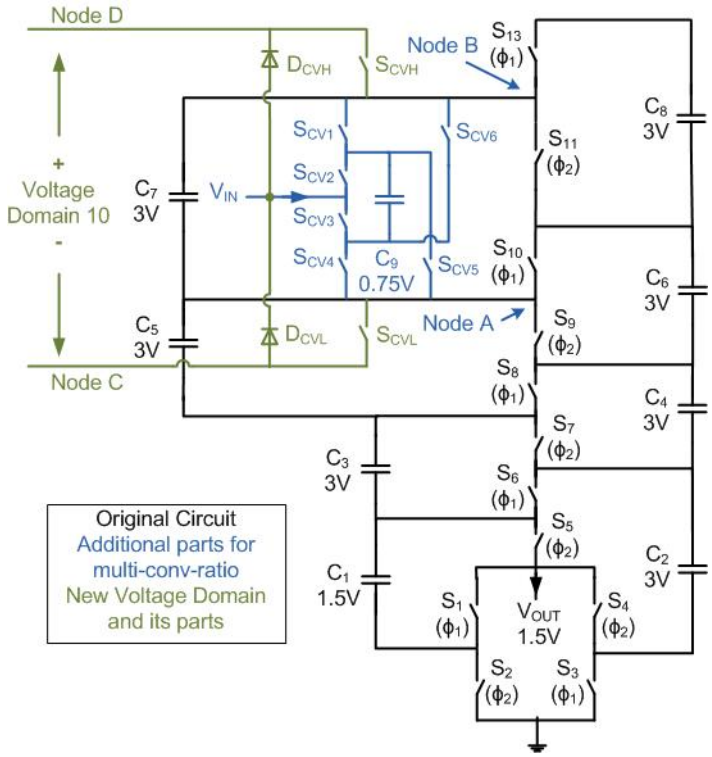
Switches S_{14} and S_{15} are not directly connected to V_{IN}, but through switches S_{16} and S_{17} due to convenience in gate drive voltage domains. By adding switches S_{16} and S_{17}, switches S_{14} and S_{15} can be driven by the voltage domains defined by capacitors C_6 and C_8 respectively, and switches S_{16} and S_{17} can be driven by a new voltage domain between nodes C and D. This new voltage domain is maintained at roughly 3V by clocking S_{14} and S_{15} together. In order to minimize switching loss, switches S_{16} and S_{17} are only switched when the conversion ratio changes. The benefit of using this circuit is that it allows multiple conversion ratios without increasing PCB area or I/O pin count since it does not require any additional capacitors. However, this converter may require a slightly larger integrated switch area to account for the increase in resistive loss by replacing one switch, S_{12}, with four switches, pairwise in series.

2.4.2 Half step topology

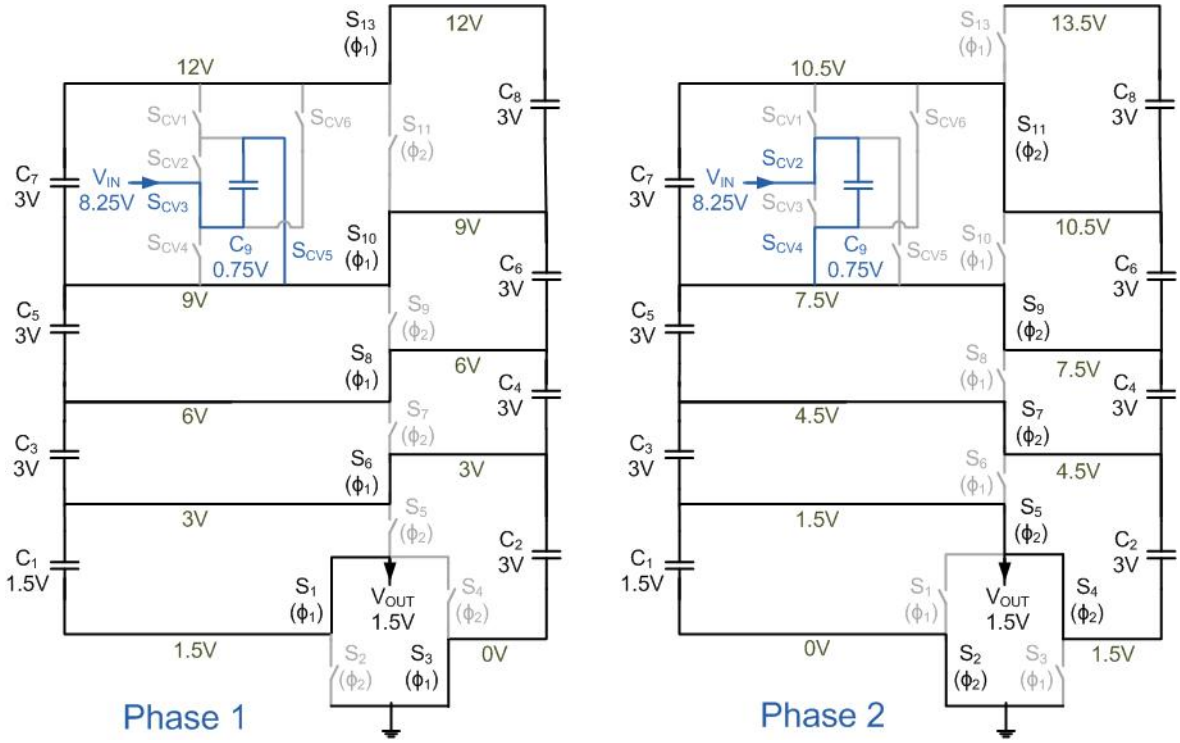
The circuit discussed in subsection 2.4.1 allows multiple conversion ratios in integer steps, but if a finer conversion ratio step is needed, one can add one capacitor and achieve half-integer-step conversion ratios. However, unlike the integer-step version, this half-integer-step version will increase the PCB area and I/O pin count. This is because the additional capacitor is part of the power-train and will require the high capacitance of an off-chip capacitor. Figure 2.7a shows the modified Dickson converter that can achieve 7 conversion ratios in half-integer steps, namely 5:1, 5.5:1, 6:1, 6.5:1, 7:1, 7.5:1 and 8:1. The actions of the switches for each conversion ratio are shown in table 2.2. Table 2.2 also shows the corresponding V_{IN} that will give an unloaded V_{OUT} of 1.5V.

When the circuit in figure 2.7a is compared with the original circuit in figure 2.2, switch S_{12} is eliminated while 6 switches, $S_{CV1} - S_{CV6}$, and 1 capacitor, C_9, are added. The other additional switches and diodes are for gate drive purposes, and are not part of the power-train. This circuit can be considered as an expansion to the integer-step version in figure 2.6. Both circuits achieve the 4 integer-step conversion ratios by connecting the input to either nodes A or B during one of the two clock phases. This latter circuit achieves the additional intermediate half-steps by using capacitor C_9. As an example, figure 2.7b shows the circuit configuration for the conversion ratio of 5.5:1. The circuit configurations for the other 6 conversion ratios can be obtained in a similar fashion.

Similar to the integer-step version, this half-step version also requires a new voltage



(a) Converter topology and the voltage domain to drive the additional switches



(b) An example when the conversion ratio is 5.5:1

Figure 2.7: Dickson converter with multiple conversion ratio in half-integer steps.

Table 2.2: Switch action table for the circuit in figure 2.7 . Parameter n stands for conversion ratio.

		Phase 1 ($\phi 1$)									
n	V_{IN}	S_{CV1}	S_{CV2}	S_{CV3}	S_{CV4}	S_{CV5}	S_{CV6}	S_{CVH}	D_{CVH}	S_{CVL}	D_{CVL}
8:1	12V	*On*	*On*	Off	Off	Off	Off	*On*	Off	*On*	Off
7.5:1	11.25V	*On*	Off	*On*	Off	Off	Off	*On*	Off	*On*	Off
7:1	10.5V	Off	Off	Off	Off	Off	Off	*On*	Off	*On*	Off
6.5:1	9.75V	Off	*On*	Off	*On*	Off	Off	*On*	Off	*On*	Off
6:1	9V	Off	Off	*On*	*On*	Off	Off	*On*	Off	*On*	Off
5.5:1	8.25V	Off	Off	*On*	Off	*On*	Off	*On*	Off	Off	*On*
5:1	7.5V	Off	Off	Off	Off	Off	Off	*On*	Off	Off	*On*

		Phase 2 ($\phi 2$)									
n	V_{IN}	S_{CV1}	S_{CV2}	S_{CV3}	S_{CV4}	S_{CV5}	S_{CV6}	S_{CVH}	D_{CVH}	S_{CVL}	D_{CVL}
8:1	12V	Off	Off	Off	Off	Off	Off	Off	*On*	*On*	Off
7.5:1	11.25V	Off	*On*	Off	Off	Off	*On*	Off	*On*	*On*	Off
7:1	10.5V	*On*	*On*	Off	Off	Off	Off	*On*	Off	*On*	Off
6.5:1	9.75V	*On*	Off	*On*	Off	Off	Off	*On*	Off	*On*	Off
6:1	9V	Off	Off	Off	Off	Off	Off	*On*	Off	*On*	Off
5.5:1	8.25V	Off	*On*	Off	*On*	Off	Off	*On*	Off	*On*	Off
5:1	7.5V	Off	Off	*On*	*On*	Off	Off	*On*	Off	*On*	Off

domain to drive the additional switches. The rails that define this new voltage domain are named nodes C and D in figure 2.7a as in the integer-step version in figure 2.6. However, this new voltage domain is more complicated than any of the other voltage domains discussed so far. This voltage domain does not have a fixed voltage level, but changes with clock phase and conversion ratio. The voltage level varies from 3V to 4.5V, but it is within the 5V rated voltage of the $0.6\mu m$ transistor available in this process. Switches S_{CVH} and S_{CVL}, and diodes D_{CVH} and D_{CVL} are used to control this voltage domain, and their actions are also shown in table 2.2. Switch S_{CVL} and diode D_{CVL} are used to connect node C to either V_{IN} or node A, whichever has a lower voltage level. Similarly, switch S_{CVH} and diode D_{CVH} are used to connect node D to either V_{IN} or node B, whichever has a higher voltage level.

2.5 Shutdown and Startup

As discussed in section 2.2, dividing the converter into multiple voltage domains allows the usage of 1.8V and 5V transistors in this 12V converter. These voltage domains are defined by the power-train capacitors, which during normal operation, have near constant voltage levels due to the switching action of the converter. However, these voltage levels are not well defined during the transients of shutdown and startup, and a protection scheme and a startup plan is needed.

2.5.1 Shutdown protection

After a converter stops switching during shutdown, the power-train capacitor voltages may drift in an unanticipated manner and cause over-voltage levels in some voltage domains. To prevent this from happening and over-stressing any device, active clamp circuits are implemented in each voltage domain to limit the peak voltage level. Figure 2.8 shows the conceptual idea of this clamp; the circuit details are discussed in section 4.2. The voltage level of the voltage domain is divided down by a resistive divider, and then compared to a reference voltage. If the voltage level is too high, the comparator will turn on an NMOS transistor, drain current across the voltage domain and reduce the voltage back to a safe level. Since capacitor voltage drift is a slow process, this clamp circuit has a low bandwidth and consumes little power. This clamp circuit is designed to drain 5mA when on, and about 200nA when off. The power consumed by these clamps is less than the power loss due to sub-threshold leakage current through the power-train switches.

2.5.2 Startup scheme

The objective of the startup scheme is to charge up the power-train capacitors and build up the various voltage domains while protecting the low-voltage transistors from the high voltage input source during this transient. Figure 2.9 shows the concept of the startup scheme implemented in this work. Initially, the converter is isolated from the input source with a high voltage blocking switch while a precharging regulator charges up the output rail. The converter then operates in charge-pump (boost) mode to charge up all the capacitors and internal nodes to pre-determined values. The high voltage blocking switch is then

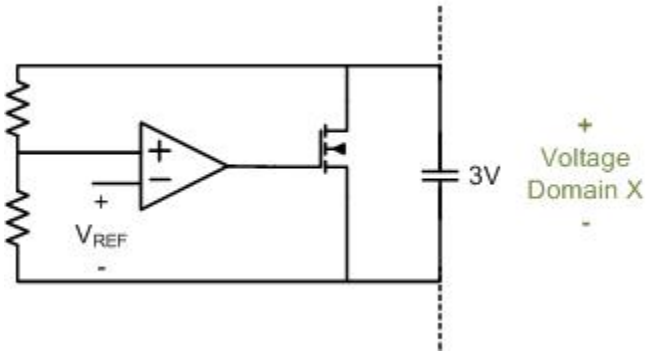


Figure 2.8: Shutdown protection clamp

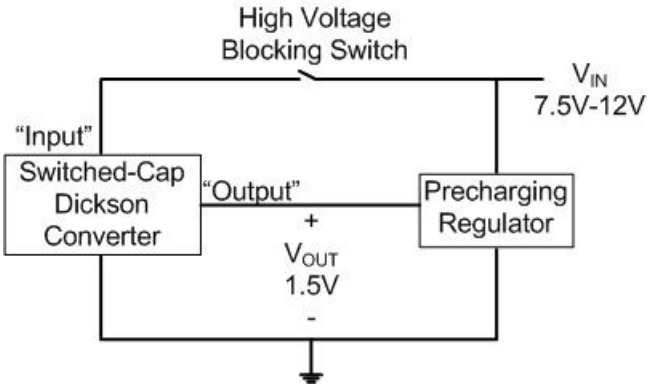


Figure 2.9: Startup scheme

activated, followed by turn-off of the precharging regulator. The converter then operates in the normal mode as discussed in the previous sections. Running the converter in boost mode guarantees that the capacitors are charged up gradually and sequentially, and thus no low-voltage transistor is stressed during the transient. The Dickson topology was originally designed as a charge-pump, and its operation in boost mode is well-documented in the literature [6, 17, 18]. Section 4.3 discusses the circuits to enable charge-pump mode of the converter, and section 4.5 discusses the design of the precharging regulator. The state machine that implements this startup sequence is discussed in subsection 3.3.6.

This startup scheme requires a high voltage switch, which may contradict the benefit that this converter handles high voltage with only low voltage transistors. While this switch and the power switches in the buck converter both block the input voltage, they are different in many aspects. First of all, this high voltage switch only supports the input current while the power switches in the buck converter supports the output current. Since the input current is only a fraction of the output current, the SC converter has a lower V-A product than the buck converter even when this switch is included in the analysis in subsection 1.2.1. Secondly, this switch does not switch during normal operation and thus, unlike the switches in the buck converter, there is no switching loss associated with this switch. This high voltage switch is implemented with 12V LDMOS transistor which is also available in this process. The circuit level design of this high voltage switch is discussed in section 4.4.

Chapter 3

Regulation

The inductor based buck converter has two switches and two reactive elements, and regulation is already not a trivial task. An SC converter can easily have more than a dozen switches and capacitors, and its configuration can vary widely depending on topology, conversion ratio and application. With so many components and variables, there exist numerous ways to achieve regulation. While this gives the designer lots of choices, this can become daunting when one has to decide which knob to turn. This chapter discusses and contrasts some possible ways to control an SC converter, and explains the method chosen in this work.

3.1 Possible control methods

Referring to the static model in figure 1.1, the conversion ratio of an SC converter is determined by the unloaded conversion ratio, n, and the output resistance, R_{OUT}. Resistance R_{OUT} can be further broken down into R_{SSL} and R_{FSL}, as given by equation 1.10. The numerous control methodologies proposed in the literature [25, 24, 21, 22, 23, 41] can all be considered as modifying one or more of the three parameters: R_{SSL}, R_{FSL}, and n. Modifying conversion ratio, n, is required to control the voltage drop across the equivalent series output resistance of the SC converter, and thus allows the converter to attain optimal efficiency. However, changing n requires changing the topology of the converter, and may significantly increase the complexity of the converter [25]. Thus modulating R_{FSL} and/or R_{SSL} are desirable for tight regulation in a SC converter with practical complexity. Subsections 3.1.1 to 3.1.3 will discuss in detail the pros and cons of utilizing each of these three control parameters. Depending on the application, the designer may decide to change more than one control parameter to obtain optimal regulation. A discussion of this "hybrid" control where a combination of several parameters is manipulated will be given in subsection 3.1.4.

3.1.1 Control through R_{SSL}

As discussed in subsection 1.1.1, the slow switching limit output referred resistance, R_{SSL}, is determined by the switching frequency of the converter and the capacitance of the power-train capacitors. While it may be inconvenient to dynamically vary the sizes of the capacitors, varying the switching frequency is a popular method in many designs. Some designs

skip clock pulses [21], and some designs control the clock hysteretically [22]. While these methods differ in implementations, they all achieve regulation through effectively varying the switching frequency of a converter.

The main advantage of using switching frequency to achieve regulation is high efficiency at light load conditions. As load current reduces, switching frequency is reduced to maintain regulation. This in turns reduces switching loss, which is usually the dominant loss factor at light load conditions. Further, many frequency regulators consume low standby power as they are made up of only comparators and digital logic. As discussed in subsection 2.3.3, this allows high efficiency at very light loads when the converter is barely switching and standby power dominates power loss. The main disadvantages of controlling through switching frequency is potentially high output voltage ripple as charge transfer is impulsive in the SSL. In order to compensate for this, a large output capacitor C_L may be required or interleaving has to be introduced [26]. This will, however, increase component cost or the complexity of the controller, in the case of off-chip capacitors.

3.1.2 Control through R_{FSL}

Instead of varying R_{SSL}, one can control R_{OUT} by varying the R_{FSL} term in equation 1.10. This either involves changing the duty ratio of the switches [24], or the resistances of the switches by controlling gate-drive voltage [23], or switch size. If the control methodology involves changing the resistances of the switches connected to the output terminal, current to the output can be held at near constant values, and the output voltage ripple can be minimized [41]. With this control method, the SC converter will behave very similarly to a linear regulator, and the compensation techniques developed for the linear regulators [20] are excellent references. However, there are additional dynamics associated with the SC converter that are absent in the linear regulator, and these dynamics have to be well understood if aggressive compensation schemes such as canceling of poles and zeros are used.

The main drawback of varying R_{FSL} to control V_{OUT} is reduced efficiency at light load if switching frequency is constant at all times. Efficiency is also reduced in heavy load as operating in the FSL requires high switching frequency, which increases switching loss. If switch resistance control is being used, further losses from high standby power may be incurred. This is because controlling switch gate-drive voltage requires analog buffers, which are more power hungry than their digital counterparts. Duty ratio control eliminates the analog buffer but may not support regulation for a wide load range. To maintain regulation, duty ratio is proportional to load current. While load current may vary by orders of magnitude, varying duty ratio by orders of magnitude is impractical, or at least difficult or costly. All of these disadvantages can be mitigated by dynamically reducing the switch sizes at low current levels. This will, however, increase the complexity of the controller and the control algorithm.

3.1.3 Control through conversion ratio, n

While regulation can be achieved through varying the output resistance of the converter, this requires a voltage drop across a resistive element and thus limits the maximum efficiency

achievable by an SC converter. This is similar to the case of a linear regulator. Equation 1.1 shows that the only way to achieve maximum efficiency for a given V_{IN} and V_{OUT} is to be able to choose any conversion ratio, n. However, changing n requires changing the topology, and may significantly increase the complexity of the converter [25]. A large number of switches and capacitors may have to be added, which not only increase power loss but also the cost of the converter. The number of components and component stress increase with the number of possible conversion ratios, and thus most practical SC converters only support a few conversion ratios. Without a fine resolution of n, the resolution of regulation is also limited and tight regulation is not possible. Being able to support a large number of conversion ratios without significantly increasing the number of components is an area of great interest. The half-integer step Dickson topology discussed in subsection 2.4.2 was designed to achieve this goal.

3.1.4 Hybrid control

The three control categories discussed in subsections 3.1.1 to 3.1.3 each has its own merits and problems. While many designs make use of only one of them [25, 24, 21, 23], many applications may require more than one to achieve optimal efficiency and regulation. Conversion ratio change is indispensable if high efficiency is desired in applications where wide variations in V_{IN} and/or V_{OUT} is anticipated. If tight regulation is also required, then the controller must also be able to vary R_{SSL}, R_{FSL}, or both. An effective control strategy may be to first set n based on the ratio between V_{IN} and V_{OUT}, and then change either R_{SSL} or $R_{FSL}$to maintain tight regulation. Varying R_{SSL} allows high efficiency at light load conditions, whereas varying R_{FSL} allows low ripple. Since R_{OUT} can be approximated by a quadratic sum of R_{SSL} and R_{FSL}, as given by equation 1.10, it is not strategic to operate deep in either R_{SSL} or R_{FSL}. Thus the best operating condition is to set R_{SSL} and R_{FSL} roughly equal to or within a factor of two or so from each other for all load and line conditions.

3.2 Proposed control algorithm - Two loop control

In order to attain high overall performance, this work utilizes all three control methodologies discussed in section 3.1. Conversion ratio change is used to attain coarse regulation and to allow high efficiency, while switch conductance modulation of all the "output" switches is used to minimize voltage ripple and achieve tight regulation. Switching frequency is also modulated to achieve high efficiency, but the frequency is designed to be high enough such that R_{OUT} is dominated by R_{FSL}, and thus R_{SSL} has little effect on regulation. This is achieved by slaving the clock to a proxy of R_{FSL}, as will be discussed in subsection 3.3.2. This work uses the half-step multi-conversion-ratio Dickson converter discussed in subsection 2.4.2 for its fine conversion ratio step and few additional components. Switches S_1, S_4 and S_5 of figure 2.7 are the three "output" switches, and their resistances are modulated by changing their gate-drive voltages. The controller is made up of a fast inner loop that controls both R_{FSL} and R_{SSL}, and a slow outer loop that controls n. Figure 3.1 shows a conceptual diagram of this two-loop control. Subsections 3.2.1 to 3.2.3 will discuss the algorithm of

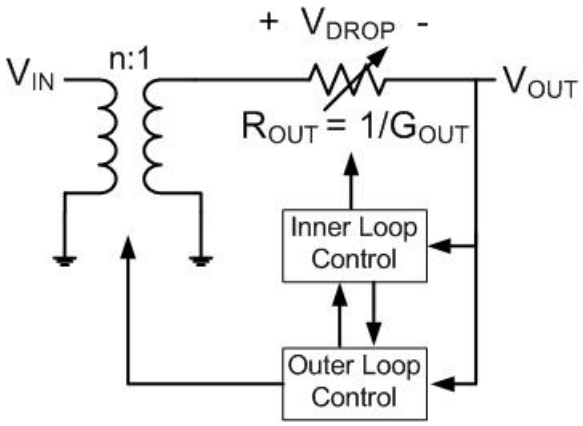


Figure 3.1: Conceptual diagram of the two loop control method

the outer loop to choose conversion ratio, n. The analysis is first simplified in subsections 3.2.1 and 3.2.2 by assuming that the voltage drop across R_{OUT} is the only power loss in the converter. This assumption is removed in subsection 3.2.3 where a more complete analysis is given. Section 3.3 discusses the detailed architecture to implement this two-loop control algorithm. The circuit details are discussed in chapter 4.

3.2.1 Conversion ratio selection algorithm

In order to fully benefit from the fine conversion-ratio resolution of the half-step topology, this converter chooses n not only based on V_{IN}/V_{OUT}, but also based on I_{OUT}. This allows the converter to increase n, resulting in a lower V_{DROP}, and thus attain higher efficiency as I_{OUT} reduces. For optimal efficiency and regulation, the converter only needs to switch to a lower conversion ratio if the converter output referred conductance, $G_{OUT} = 1/R_{OUT}$, required to maintain regulation exceeds its maximum value, G_{MAX}. Parameter G_{MAX} is entirely determined by the power-train design. In this situation, the converter requires a larger V_{DROP}, which is the voltage drop across R_{OUT} as indicated in figure 3.1, in order to supply the needed load current. This condition causes the inner loop to saturate, which can be detected by comparing the gate-drive voltage of the "output" switches to a pre-defined maximum value. On the contrary, in the case of lighter load, the converter should switch to a higher conversion ratio to increase efficiency if after doing so the required converter conductance is less than G_{MAX}. The exact equation governing this transition is derived below.

Before increasing conversion ratio, the converter should be in regulation, and the converter conductance, G, is given by:

$$G = I_{OUT} / \left(\frac{V_{IN}}{n_{cur}} - V_{OUT} \right) \tag{3.1}$$

where n_{cur} is the current conversion ratio. After increasing conversion ratio, the new converter conductance, G_{NEW} is given by:

$$G_{NEW} = I_{OUT} / \left(\frac{V_{IN}}{n_{cur} + S} - V_{OUT} \right) \tag{3.2}$$

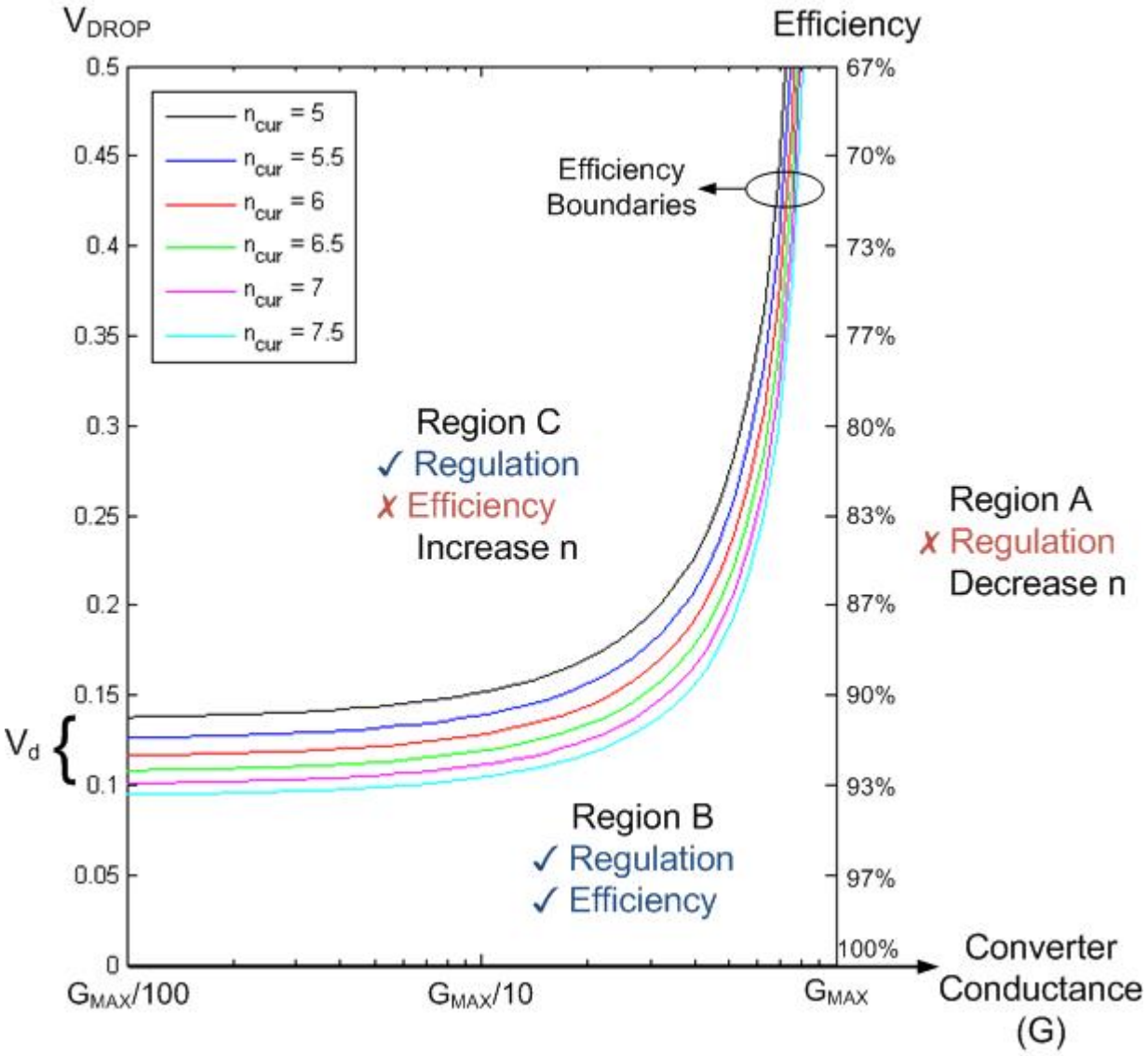


Figure 3.2: A $G - V_{DROP}$ plot showing the efficiency boundaries for the various n_{cur}

where $n_{cur} + S$ is the new conversion ratio, and S is the step size in n. Parameter S equals 0.5 for the half-step converter in subsection 2.4.2, and equals 1 for the integer-step converter in subsection 2.4.1. If $G_{NEW} < G_{MAX}$, then the converter should increase conversion ratio. By combining equations 3.1 and 3.2, and the inequality $G_{NEW} < G_{MAX}$, this condition is given by:

$$G < G_{MAX} \frac{\left(\frac{V_{IN}}{n_{cur}+S} - V_{OUT}\right)}{\left(\frac{V_{IN}}{n_{cur}} - V_{OUT}\right)} \tag{3.3}$$

which can also be rewritten as:

$$G < G_{MAX} \frac{V_{DROP} - V_d}{V_{DROP}} \tag{3.4}$$

$$V_{DROP} = \frac{V_{IN}}{n_{cur}} - V_{OUT} \tag{3.5}$$

$$V_d = \frac{V_{IN}}{n_{cur}} - \frac{V_{IN}}{n_{cur} + S} = \frac{S\left(V_{DROP} + V_{OUT}\right)}{n_{cur} + S} \tag{3.6}$$

where V_d is the value of V_{DROP} under open circuit condition, $G = 0$, and it represents the minimum V_{DROP} before an increase in conversion ratio should be considered. Plugging in the values for this converter, $V_{OUT} = 1.5V$, $S = 0.5$, $5 < n_{cur} < 7.5$, and assuming $V_{OUT} \gg V_{DROP}$, V_d ranges from 0.094V to 0.136V. Conversion ratio $n_{cur} = 8$ is not considered because it is the highest conversion ratio possible, and thus the converter cannot switch to yet a higher one.

Figure 3.2 shows equation 3.4 on the $G - V_{DROP}$ plane. Equation 3.4, together with $G = G_{MAX}$, divides the $G - V_{DROP}$ plane into three regions, characterized by whether regulation is satisfied and whether maximum efficiency is obtained. In region A, regulation is not satisfied since it requires a conduction, G, beyond its maximum value, G_{MAX} . In region C, regulation is satisfied but efficiency is not maximized since inequality 3.4 holds here. It is only in region B that both regulation and maximum efficiency are satisfied. Since inequality 3.4 separates region B from region C where the difference is achieving maximum efficiency, it is labeled as an efficiency boundary. In figure 3.2, efficiency boundaries are shown for the seven different values of current conversion ratio, n_{cur}.

Figure 3.2 represents the control algorithm developed in this work, and it governs when conversion ratio should be changed. If the controller were to command the converter to operate in region A, where $G > G_{MAX}$, the converter would go out of regulation, and it needs to decrease conversion ratio. If the converter is operating in region C, G is on the left of the efficiency boundary, and inequality 3.4 is satisfied. The converter is under regulation, but can and should maximize efficiency by increasing conversion ratio. In region B, the converter is both under regulation and at the maximum efficiency achievable by the converter. With this scheme, there is one and only one conversion ratio that lies within region B for any V_{IN} and I_{OUT} pair.

As shown in figure 3.2, the efficiency boundary depends on n_{cur}. In order to simplify the control algorithm, this work uses the efficiency boundary corresponding to $n_{cur} = 5$ regardless of the actual n_{cur}. This leads to more than one possible conversion ratio that lies within region

B for some V_{IN} and I_{OUT} pair when $n_{cur} \neq 5$. Since the control algorithm changes conversion ratio unless the converter is operating in region B, this leads to more than one possible solution and thus effectively introduces hysteresis. When $n_{cur} \neq 5$, region B is expanded by the area between its real efficiency boundary and the one corresponding to $n_{cur} = 5$. This region defines the hysteresis in the $G - V_{DROP}$ plane and can be used to determine the resulting reduction in efficiency. Note that if an efficiency boundary corresponding to $n_{cur} \neq 5$ is used instead, at $n_{cur} = 5$, region B will be reduced instead of increased. This will lead to no possible conversion ratio that lies within region B for some V_{IN} and I_{OUT} pairs. In these cases, the controller will continuously hop between two different conversion ratios.

3.2.2 Control through $G - V_{DROP}$ state space

As indicated in subsection 3.2.1, the control algorithm in this work uses the $G - V_{DROP}$ parameter space instead of the more familiar $V_{IN} - I_{OUT}$ space. The $G - V_{DROP}$ space is used because it is more natural and results in simpler relations both for increasing conversion ratio and decreasing conversion ratio. Conductance G is the natural parameter for regulation because the converter is under regulation as long as G is less than G_{MAX}. On the other hand, V_{DROP} reflects the efficiency of the converter since $V_{OUT}/\left(V_{DROP} + V_{OUT}\right)$ defines the maximum possible efficiency of the converter as given by equation 1.1. Figures 3.3 and 3.4 show the transformation from the $V_{IN} - I_{OUT}$ space to the $G - V_{DROP}$ space by fixing V_{IN} and I_{OUT}, respectively. The figures also show the effect of the regulation law on the movement of the operating point. As shown in the diagram, there is a one-to-one mapping between the two spaces when conversion ratio n is specified. It can be shown that the two spaces are equivalent, and there is no loss of information in the transformation once n and V_{OUT} are specified.

In terms of measurement, as shown by equation 3.5, V_{DROP} can also be measured by dividing V_{IN} by n_{cur} and comparing it with V_{OUT}. Output voltage V_{OUT} is not a constant, like a reference voltage, but it is regulated closely to one by the inner loop. Thus, in implementation, V_{IN}/n_{cur} is compared with a reference voltage instead of V_{OUT} for simplicity. Since V_{DROP} is only used to detect whether the converter is operating in region C or region B in figure 3.2, the converter is always in regulation when the detection is carried out. Thus high accuracy in measuring V_{DROP} is not required, and this simplification yields minimal degradation to performance. Similarly, the measurement of converter output referred conductance G need not be accurate, and it is approximated by digitizing the switch gate drive voltage in the inner loop by using a simple analog-to-digital converter.

3.2.3 Refined analysis of the outer loop algorithm

The control algorithm discussed in subsection 3.2.1 assumes that power loss is dominated by voltage drop across R_{OUT}, and ignores all other loss factors for simplicity. This section refines the control algorithm by taking into account the switching loss of the converter and the fixed loss. The efficiency of an SC converter is given by:

$$Eff = 1 - \frac{I_{OUT}V_{DROP} + SW_{LOSS@1Hz} * f_{SW} + Fixed_{LOSS}}{I_{OUT}\left(V_{DROP} + V_{OUT}\right)} \tag{3.7}$$

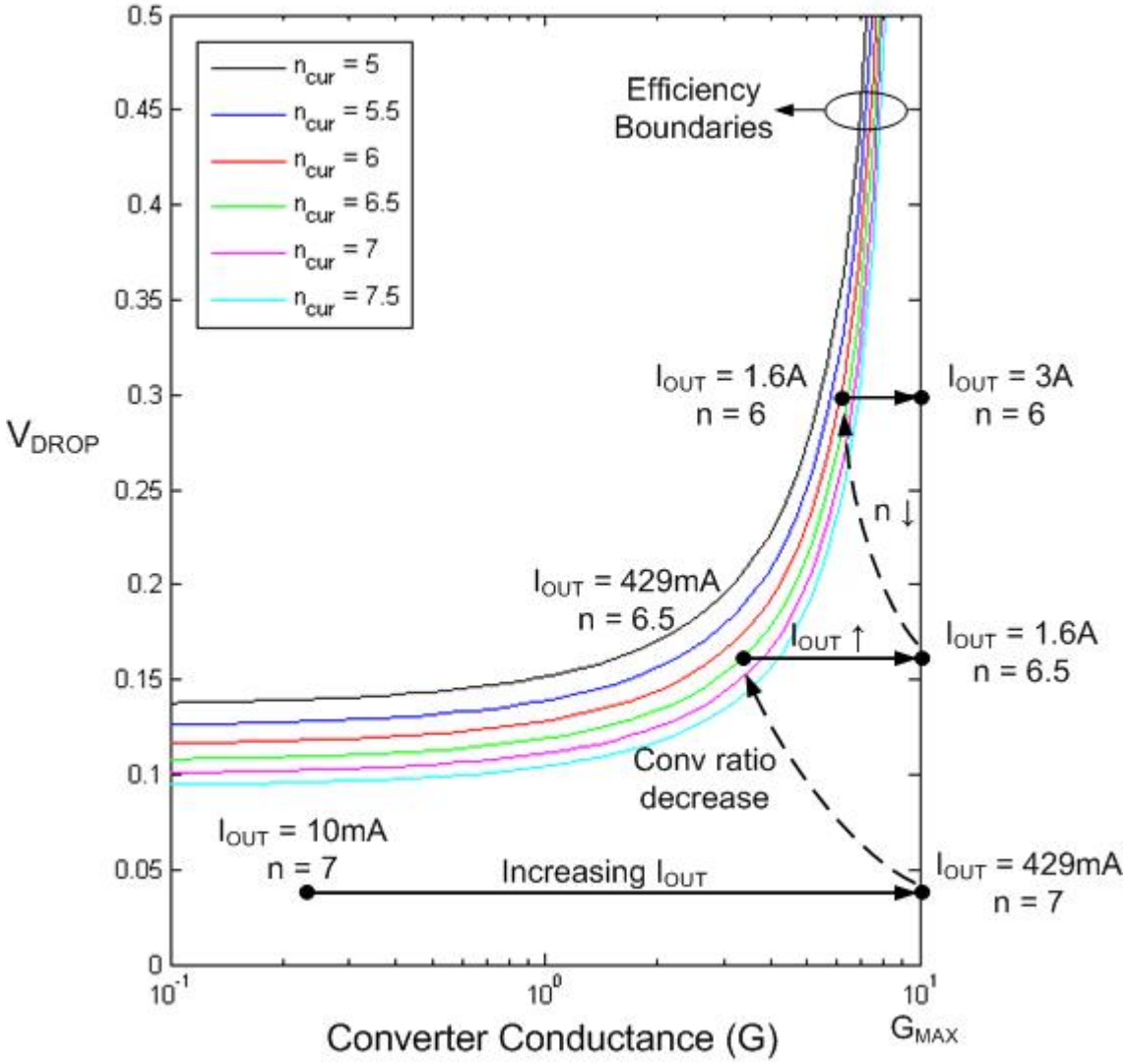


Figure 3.3: The locus of operating point on the $G - V_{DROP}$ state space as I_{OUT} increases with V_{IN} fixed at 10.8V. Changing of conversion ratio occurs at the exact curve rather than at the one corresponding to n=5, as in the simplified algorithm.

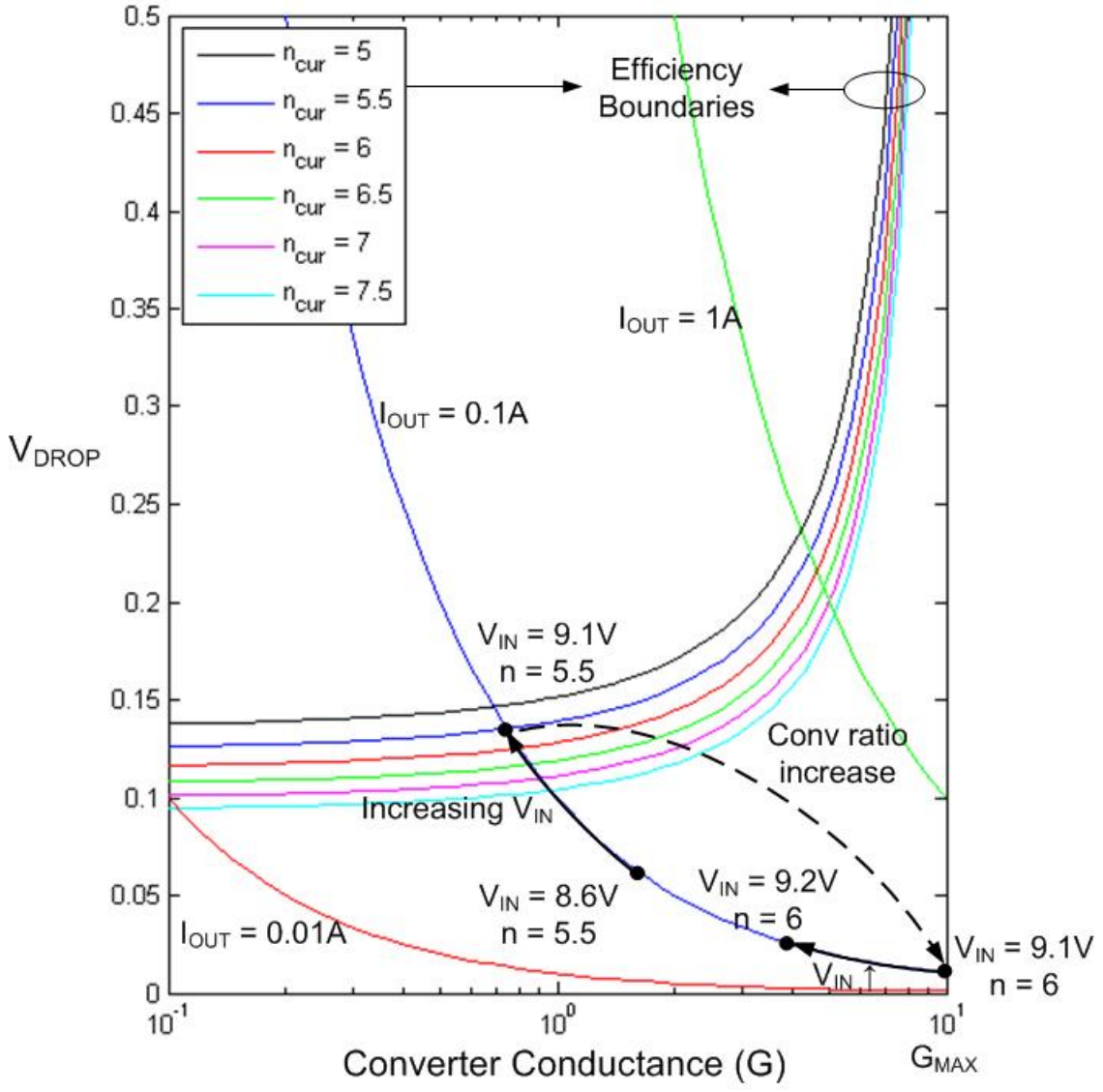


Figure 3.4: The locus of operating point on the $G - V_{DROP}$ state space as V_{IN} increases with I_{OUT} fixed at 0.1A.

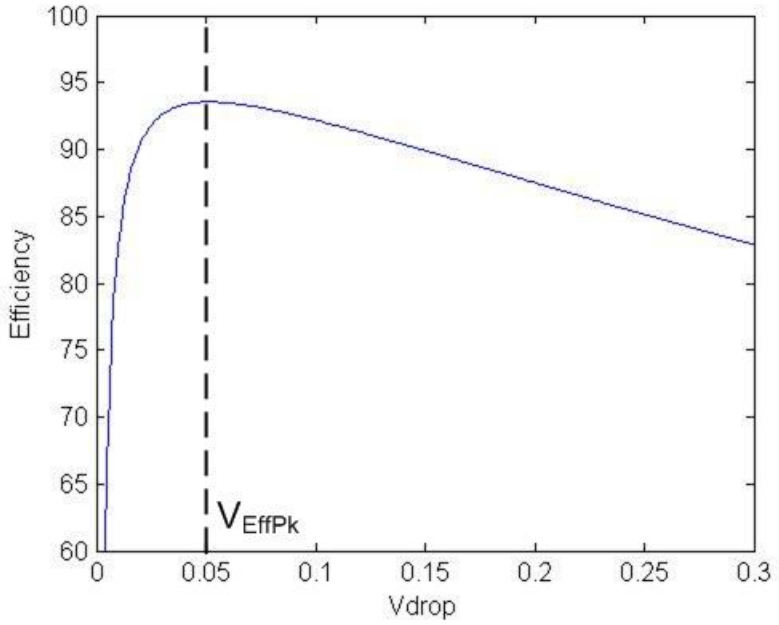


Figure 3.5: Efficiency versus V_{DROP} for $G > G_{BOD}$

where $SW_{LOSS@1Hz} * f_{SW}$ is the switching loss of the converter, f_{SW} is the switching frequency, and $Fixed_{LOSS}$ is the fixed loss of the converter. Equation 3.7 can be converted to the $G - V_{DROP}$ state space by substituting $I_{OUT} = G * V_{DROP}$, and by setting

$$f_{SW} = K * G * R_{SSL@1Hz} \tag{3.8}$$

where K is the proportional constant between R_{SSL} and R_{OUT}, and $R_{SSL@1Hz} = R_{SSL} * f_{SW}$. Equation 3.8 is a control objective of the inner loop controller to be discussed in section 3.3. By setting f_{SW} proportional to G, the switching loss will be roughly proportional to I_{OUT}, whereas R_{SSL} will be roughly inversely proportional to I_{OUT}. This will roughly give the optimal switching frequency for maximum efficiency, as given by equation 2.1. Setting R_{SSL} to be a fixed proportion of R_{OUT} will prevent the converter from operating deep in the SSL or the FSL, which can lead to low efficiency or high ripple respectively, as discussed in section 3.1. With these two substitutions, equation 3.7 can then be rewritten as:

$$Eff = 1 - \frac{V_{DROP} + \frac{K(SW_{LOSS}@1Hz)(R_{SSL}@1Hz)}{V_{DROP}} + \frac{Fixed_{LOSS}}{G * V_{DROP}}}{V_{DROP} + V_{OUT}} \tag{3.9}$$

In order to further simplify equation 3.9, the $G - V_{DROP}$ space can be divided into 2 regimes, determined by whether the second term or the third term in the numerator in equation 3.9 is larger. The value of G in which the second term equals the third term is defined as G_{BOD}, and this G boundary is given by:

$$G_{BOD} = \frac{Fixed_{LOSS}}{K\,(SW_{LOSS}@1Hz)\,(R_{SSL}@1Hz)} \tag{3.10}$$

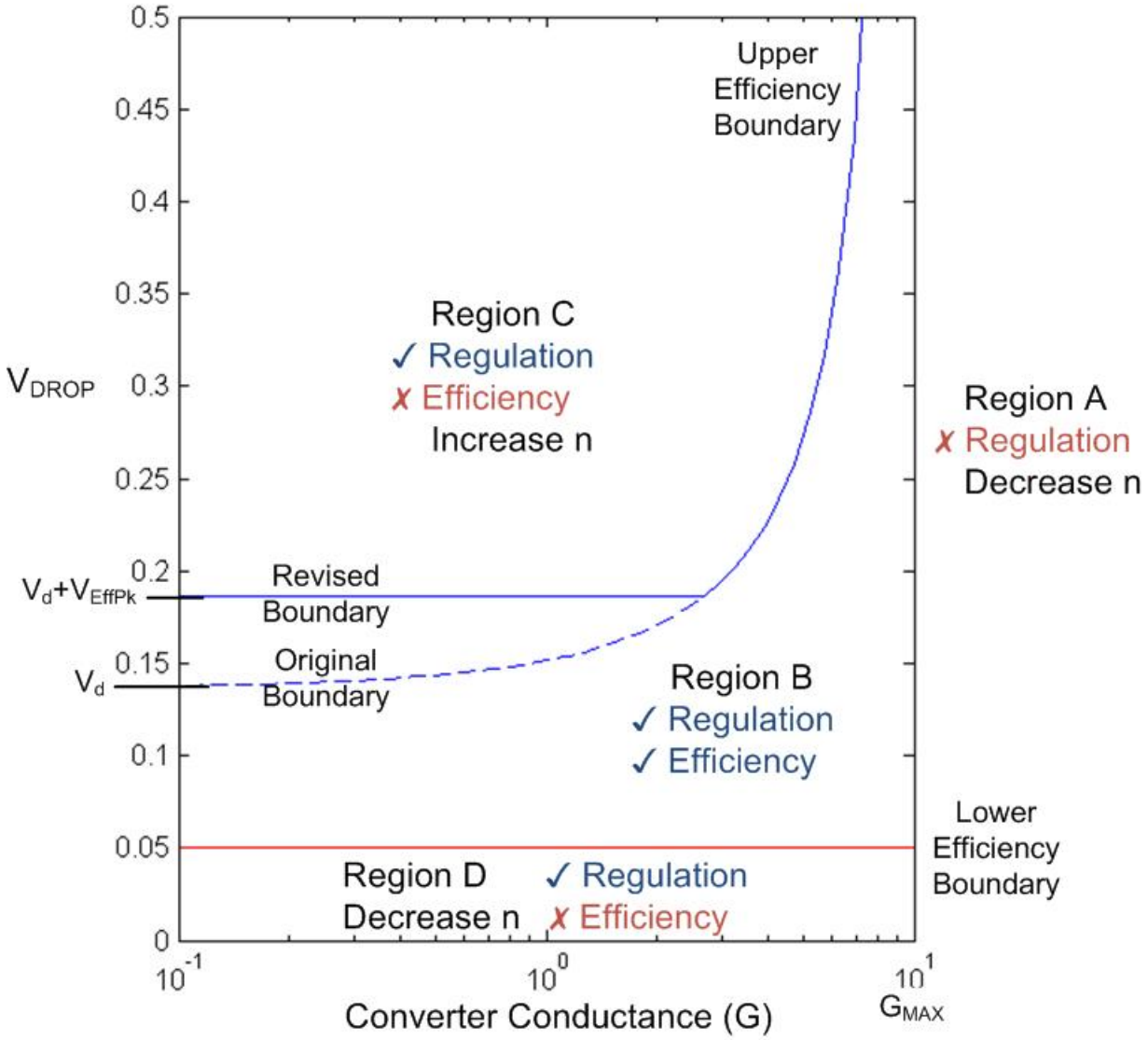


Figure 3.6: Refined control law after taking into account other loss factors.

When the second term of the numerator in equation 3.9 is larger than the third term, that is $G < G_{BOD}$, the power loss of the converter is dominated by leakage power and the constant power drawn by the control circuitry. During this situation, load current is very low and the converter is basically sitting idle. As discussed in chapter 2 subsection 2.3.3 and shown by figure 2.5, efficiency in this operating region drops very quickly with falling load regardless of control action. In this region, the controller has little leeway to increase efficiency besides turning itself off. To avoid the additional complexity of powering on and off the controller, this work focuses on situations where control action can make a difference. While there is little benefit in doing optimal control when $G < G_{BOD}$, the controller can potentially increase peak efficiency significantly when $G > G_{BOD}$. The controller can make an impact by choosing the optimal conversion ratio to trade-off the first term and second term of the numerator in equation 3.9. Thus this discussion focuses on the case when $G > G_{BOD}$, and the third term in equation 3.9 will be ignored.

With this simplification of equation 3.9, it can be shown that efficiency peaks at $V_{DROP} = V_{EffPk}$ where V_{EffPk} is given by:

$$V_{EffPk} = \sqrt{K\left(SW_{LOSS}@1Hz\right)\left(R_{SSL}@1Hz\right)} \tag{3.11}$$

Figure 3.5 shows efficiency versus V_{DROP} as predicted by equation 3.9 when $G \gg G_{BOD}$. As shown in the figure, efficiency peaks at $V_{DROP} = V_{EffPk}$, but reduces sharply as V_{DROP} approaches zero. Thus in order to obtain maximum efficiency, the converter should reduce conversion ratio and increase V_{DROP} at low V_{DROP} values. This defines an efficiency boundary in addition to the one defined by inequality 3.4. When V_{DROP} falls below this additional efficiency boundary, the converter should reduce conversion ratio. This additional efficiency boundary will be denoted as the lower efficiency boundary since it occurs at low V_{DROP} values, whereas the one defined by equation 3.4 will be called the upper efficiency boundary.

Finding an algebraic expression for this lower efficiency boundary can be tricky and difficult to implement. In order to simplify the control low, this work picks the lower efficiency boundary to be a fixed V_{DROP} value, and this value is chosen to be the V_{EffPk} at $G = G_{MAX}$. This choice sets the lower efficiency boundary to be closer to $V_{DROP} > V_{EffPk}$, and due to the asymmetrical steepness from the two side of the peak in figure 3.5, this will reduce the impact on efficiency of such a simplification. This lower efficiency boundary is implemented by adding one more control constraint to the control law discussed in subsection 3.2.1. This refined control law is shown in figure 3.6. Instead of decreasing conversion ratio only when $G > G_{MAX}$, the control law now decreases conversion ratio when either $G > G_{MAX}$ or $V_{DROP} < V_{EffPk}@\left(G = G_{MAX}\right)$ is satisfied. For increasing conversion ratio, the controller needs to check both the condition defined by inequality 3.4 and $V_{DROP} > V_d + V_{EffPk}@\left(G = G_{MAX}\right)$. This additional condition prevents the converter from falling into region D when conversion ratio is increased. If this were to occur, the converter would keep hopping between two conversion ratios.

3.3 Controller implementation

Figure 3.7 shows the block diagram of the controller implemented in this work. As discussed in section 3.2, the controller is divided into two loops; the inner loop modulates the switch

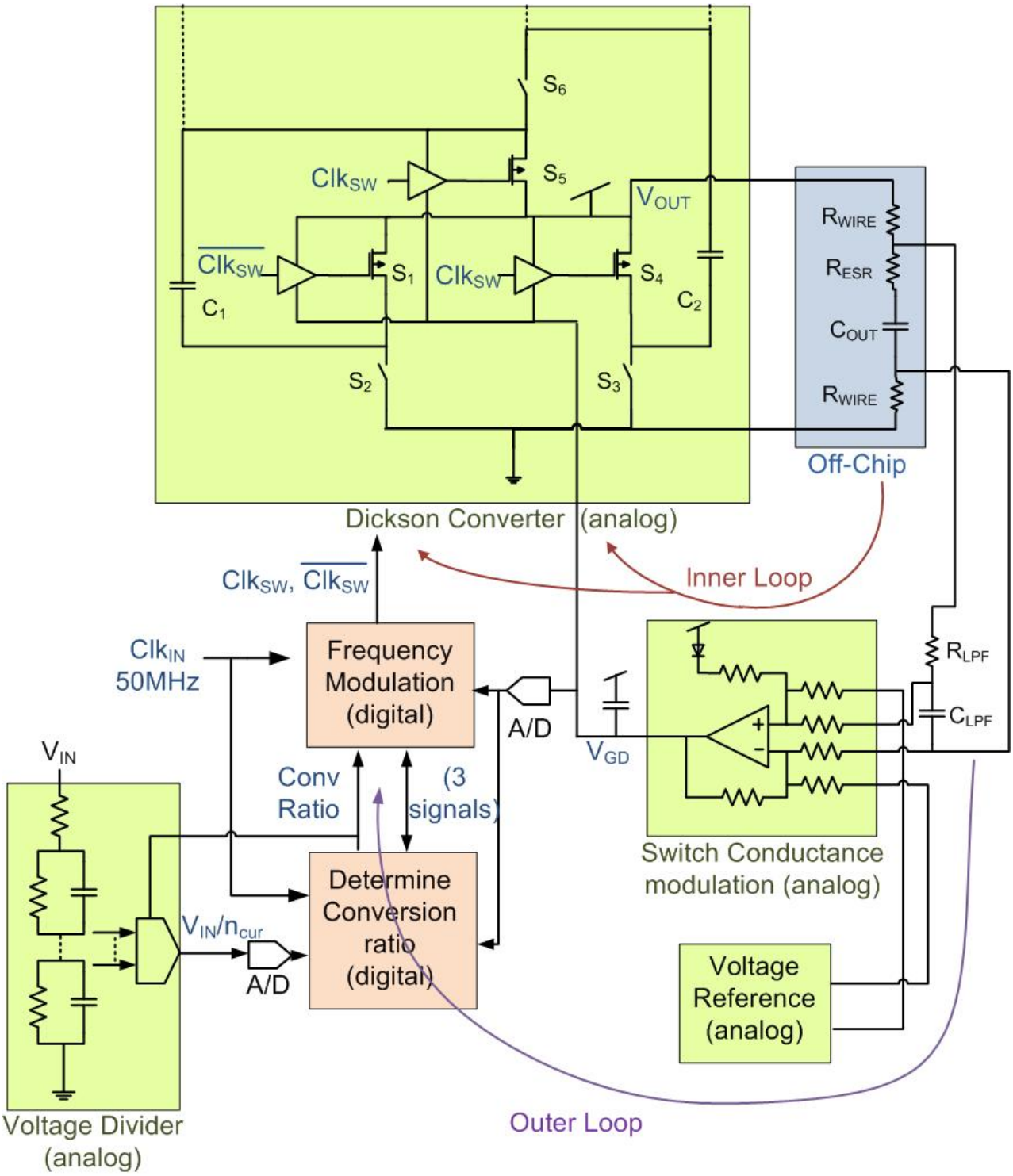


Figure 3.7: Overall block diagram of the controller

conductance and switching frequency, and the outer loop modulates the conversion ratio, n. Switch conductance modulation is achieved through modulating the gate drive voltages of the three output switches, S_1, S_4 and S_5. These three switches all block 1.5V and are implemented using $0.18\mu m$ PMOS transistors. This choice of device allows the three switches to be in the same voltage domain when they are on, and thus only one controlled supply rail, with voltage V_{GD}, is needed to provide their gate drive voltages. Voltage V_{GD} is maintained by an error amplifier that compares the output voltage with a reference voltage generated on-chip. On-chip decoupling capacitors are also added to reduce the fluctuations on this controlled supply rail. The output voltage is sensed differentially with a pair of Kelvin sense wires to eliminate the effects of voltage drops on the bondwire resistances, R_{WIRE}. A low pass filter composed of R_{LPF} and C_{LPF} is inserted to reduce the noise associated with remote sensing. The pole frequency of this low pass filter is chosen to be approximately the ESR corner frequency of the output capacitor so as to roughly cancel the zero associated with it.

With the exception of the switch modulation error amplifier, all the other control functions are implemented in the digital domain. This is because these other control functions are implemented using finite state machines, and thus are easier to implement using logic in the digital domain. These digital control blocks necessitate the use of Analog-to-Digital Converters (ADCs) to convert V_{GD} and V_{IN}/n_{cur} into the digital domain. Voltage V_{GD} is used as a proxy for G, and V_{IN}/n_{cur} is used to calculate V_{DROP}. Voltage V_{IN}/n_{cur} is obtained by using a voltage divider that divides V_{IN} by the existing current conversion ratio, n_{cur}. The frequency controller uses V_{GD} to estimate $R_{OUT} = 1/G$, and to adjust frequency such that R_{SSL} roughly equals to half of R_{FSL}. The outer loop controller uses both G and V_{DROP} to determine the optimal conversion ratio. Both of these digital controller blocks shown in figure 3.7, together with the ADCs, run at a 50MHz clock rate, with clock supplied from an on-chip signal generator. The details of the two loops and their interaction are discussed in subsections 3.3.1 to 3.3.4. The design of the inner loop involves designing the loop dynamics and the frequency controller, which are discussed in subsections 3.3.1 and 3.3.2 respectively. Subsection 3.3.3 discusses the algorithm of the outer loop controller, and subsection 3.3.4 discusses the state machine that implements the algorithm. The simulation results of the controller are discussed in subsection 3.3.5. The startup algorithm discussed in subsection 2.5.2 is also implemented by the controller, and it is discussed in subsection 3.3.6.

3.3.1 Inner loop dynamics design

The inner loop controller involves controlling V_{DROP}, and operates very similarly to a linear regulator, as shown in figure 3.8. For simplicity, only proportional feedback is used in the inner loop, and thus loop dynamics design only involves making sure the non-dominant poles of the system are beyond the maximum gain bandwidth product of the loop. The lowest frequency non-dominant pole of the system is the pole of the error amplifier. Due to the use of ceramic capacitors, the zero associated with the capacitor ESR is beyond the gain bandwidth product of the loop and can be ignored. However, if this zero is within the bandwidth of the loop, then the effect of this zero, together with the low pass filter pole represented by R_{LPF} and C_{LPF} in figure 3.7, has to be considered. With these simplifications, this regulator can be approximated by figure 3.8. This regulator has its dominant pole given by $1/C_{OUT}R_L$, and thus the gain-bandwidth product is given by:

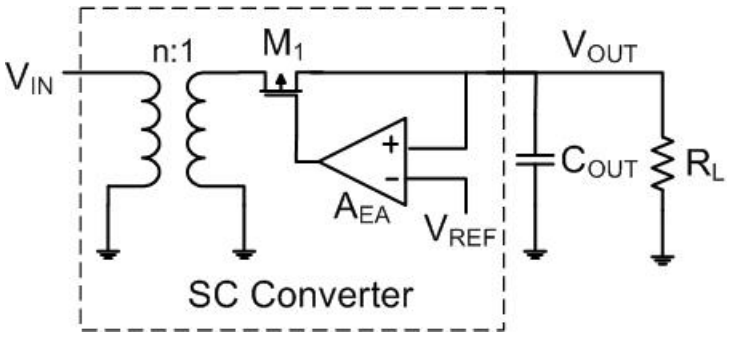


Figure 3.8: Dynamic model of the inner loop of the converter

$$G * BW = A_{EA}\frac{G_m}{C_{OUT}} \tag{3.12}$$

where A_{EA} is the gain of the error amplifier, C_{OUT} is the output capacitor, and G_m is the transconductance of transistor M_1. The value of all three terms can be determined or estimated by other specifications of the converter. Capacitor C_{OUT} is chosen based on the target ripple voltage of the converter, while error amplifier gain A_{EA} is picked based on the target tightness of regulation. In order to maintain gain stability, gain A_{EA} is implemented using resistive feedback around an opamp. Transconductance G_m can be approximated by the transconductance of the output switches, S_1, S_4 and S_5. Since these switches conduct during non-overlapping clock phases, G_m can be approximated by the average of g_{m1} and $(g_{m4} + g_{m5})$, where g_{m1}, g_{m4} and g_{m5} are the transconductance of switches S_1, S_4 and S_5 respectively. This G_m is, however, still dependent on operating point, as also is the case in linear regulators [20]. The maximum value of G_m has to be determined to obtain the maximum gain-bandwidth product which in turns dictates the minimum frequency of secondary poles required for stability. Estimating this maximum value can be tricky because at high $|V_{GS}|$ values of switches $S_{1,4,5}$, the transistors are operating in triode region. In a conservative design for stability, the designer can assume switches $S_{1,4,5}$ to be always in saturation and use the resulting maximum g_m.

While this subsection provides a methodology to analyze the loop dynamics of an SC converter, it is based on numerous approximations. In order to avoid instability in the loop, this work depends on ample simulation at various operating conditions to approximate the maximum gain-bandwidth product of the converter. The reader is advised to use this methodology with caution and to run ample simulations as well. The maximum gain-bandwidth product is estimated to be about $300kHz$ by simulation. The worst case output voltage ripple is when charge transfer is impulsive, and in this worst case scenario, output capacitor, C_{OUT}, can be chosen using equation $I_{OUT} = C_{OUT} * \Delta v/\Delta t$. An output capacitance of $C_{OUT} = 50\mu F$ is chosen to give a ripple voltage, Δv, of $6mV$ at maximum $I_{OUT} = 1.5A$ and maximum switching frequency of 2.5MHz. Note that since the converter is a two-phase circuit, the ripple frequency is at 5MHz and $\Delta t = 0.2\mu s$. This ripple analysis ignores the effect of equivalent series resistance, R_{ESR}, of the output capacitor. The R_{ESR} of the output capacitor is about $3m\Omega$, and it adds about $1.5A * 3m\Omega * 2 = 9mV$ of output ripple voltage. Thus the total ripple voltage of the converter is designed to be about $15mV$

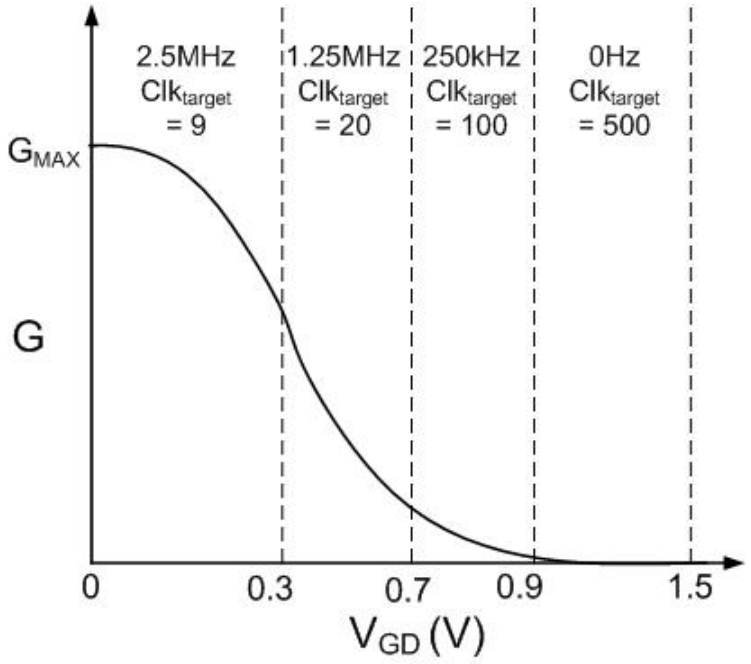


Figure 3.9: Relationship between V_{GD} and G, and the assignment of switching frequency. The labeling on the x-axis is not drawn to scale.

at maximum switching frequency and output current. For error amplifier gain, A_{EA}, a target regulation of $20mV$ over load is chosen, and thus $A_{EA} = 1.5V/20mV = 75$ is used.

3.3.2 Inner loop frequency controller

The frequency controller aims to maintain high efficiency for the converter at each output load condition. With the converter conductance, G, mainly set by the switch conductance modulation loop, the switching frequency is set high enough such that R_{FSL} dominates R_{SSL}, but not so high that switching loss significantly impact efficiency. The frequency controller aims to set $R_{SSL} \sim R_{FSL}/2$, but this ratio is not maintained zealously for simplicity. The frequency controller uses voltage V_{GD} to estimate G, and their relationship is shown in figure 3.9. Any discrepancy in the estimation of G for the purpose of controlling frequency can be considered as an offset, and has minimal effect on the inner feedback loop. Figure 3.9 also shows how switching frequency is quantized into different bands depending on V_{GD}. With the availability of the 50MHz input clock, Clk_{IN}, the various switching frequencies are obtained by counting Clk_{IN}, and comparing the count value, Clk_{count}, to predetermined values, Clk_{target}. If $Clk_{count} > Clk_{target}$, then the converter will switch to the next clock phase and Clk_{count} is reset. This operation will result in the switching clock period being $(1/50MHz) * (Clk_{target} + 1) * 2$ where the factor of two is due to the two-phase operation of the SC converter, and the additional clock count due to the deadtime between the two phases. The decision flow diagram of this controller is shown in figure 3.10, and the state machine is shown in figure 3.11. In order to avoid overlapping of the two phase clock signals, the controller gives a deadtime period equal to one Clk_{IN} period. The signal $Count_{reset}$ in

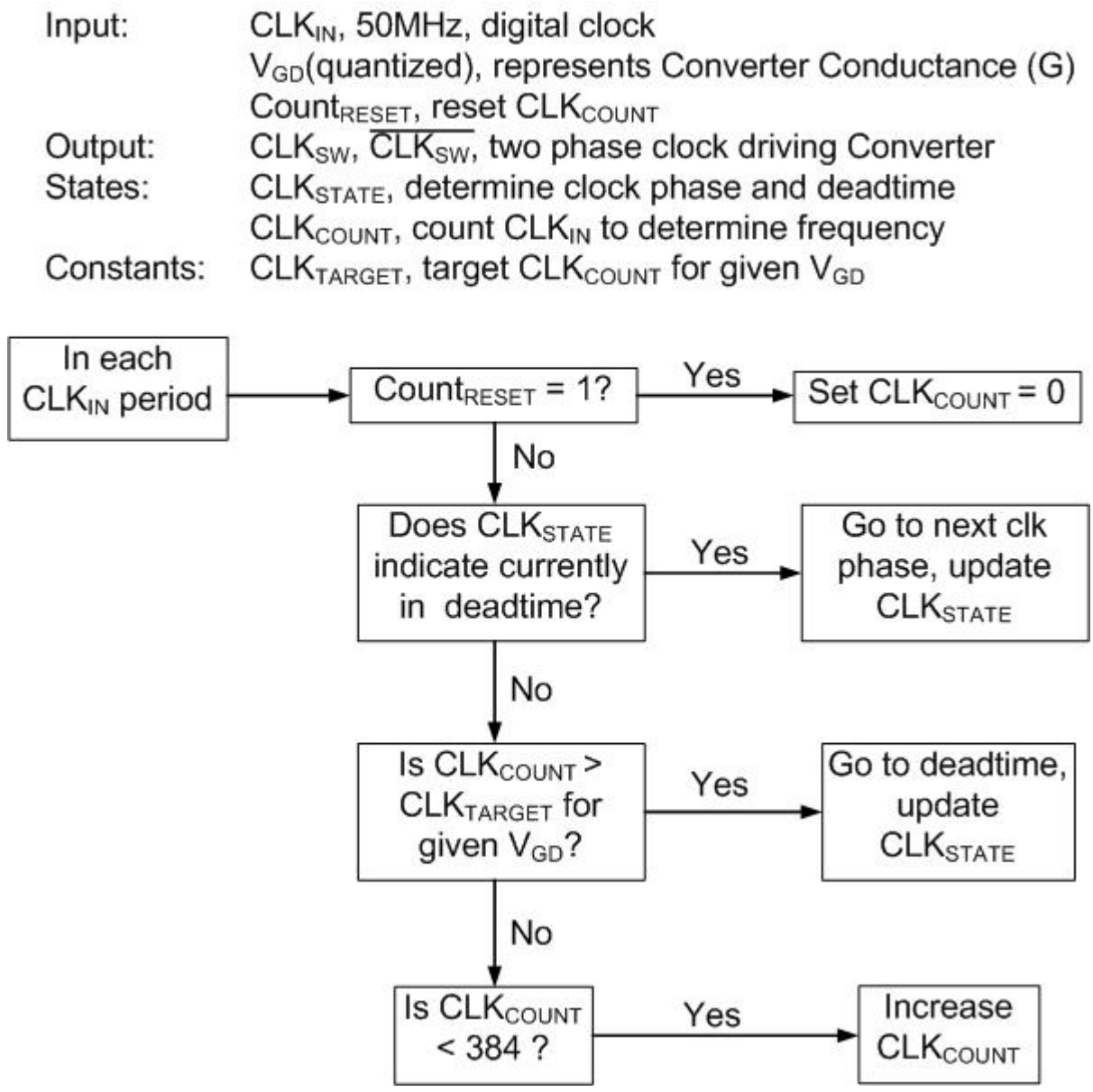


Figure 3.10: Decision flow diagram of the frequency controller

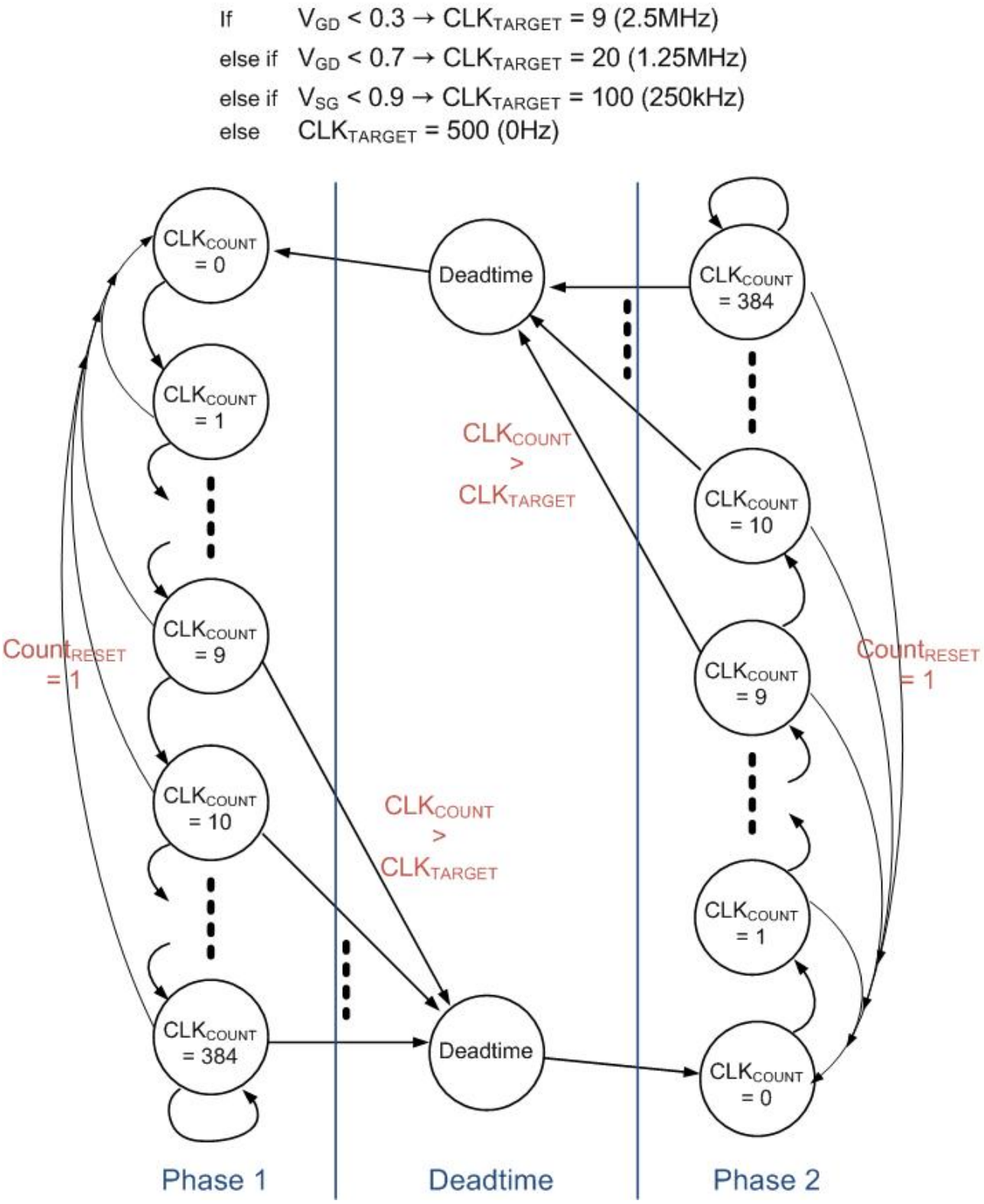


Figure 3.11: State machine of the frequency controller

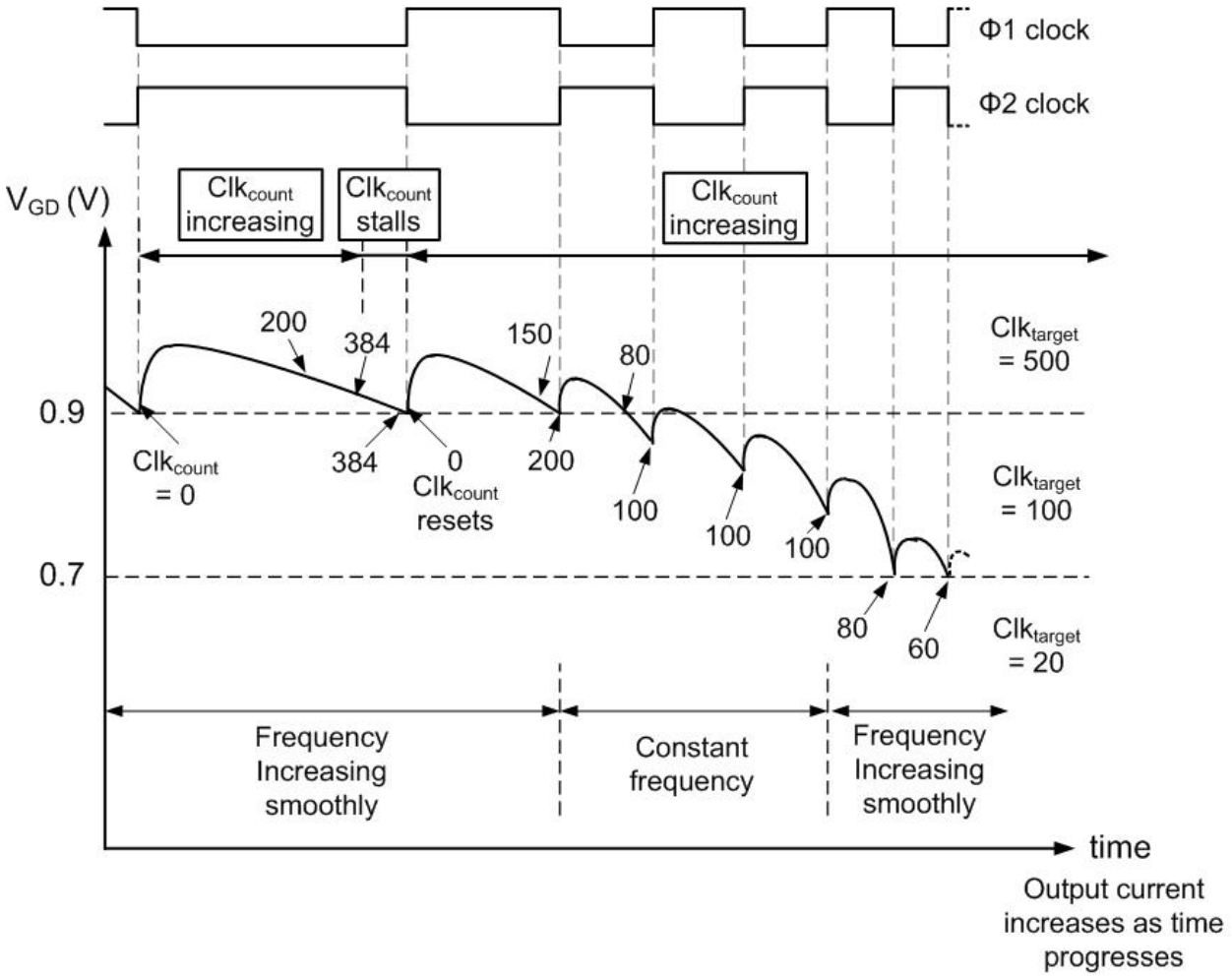


Figure 3.12: Timing diagram showing how switching frequency varies as output load current increases gradually. The two phase switching clock is also shown in the figure. There is a deadtime of 1 clock period between the two phase clock, but it is not shown here for simplicity.

figures 3.10 and 3.11 resets Clk_{count}. It is a signal from the outer loop controller, and will be discussed in subsection 3.3.4.

In order to allow the possibility of no switching action, Clk_{count} is stalled after it reaches count 384. This scenario corresponds to $V_{GD} > 0.9V$, with switches $S_{1,4,5}$ barely on for an extended period of time. Since $V_{GD} = 1.5V + A_{EA}\,(V_{OUT} - V_{ref})$, this means $V_{OUT} \sim V_{ref}$ without the converter supplying much current. Due to the light load current, the switching frequency should be reduced to reduce power loss. Stalling Clk_{count} allows switching frequency to possibly reduce to $0Hz$. The switching frequency will, however, transition smoothly instead of abruptly from $0Hz$ to $250kHz$ due to the algorithm of control. Figure 3.12 shows a conceptual timing diagram of the controller as output current increases gradually. In the beginning, when the load current is low, Clk_{count} increases up to 384, and stalls thereafter. The converter does not switch phase since the condition $Clk_{count} > Clk_{target} = 500$ is not met. When V_{GD} crosses the 0.9V boundary, Clk_{target} becomes 100, and the condi-

tion $Clk_{count} > Clk_{target} = 100$ is met. The converter switches phase, and Clk_{count} resets. Note that the converter changes phase once it hits the $V_{GD} = 0.9V$ boundary, and is effectively switching at a frequency between $0Hz$ and $250kHz$. As output current further increases, V_{GD} decreases and the converter switches at a constant frequency of $250kHz$ while $0.7V < V_{GD} < 0.9V$. As V_{GD} approaches the next boundary of 0.7V, the converter again changes phase at the boundary. The timing diagram shows that the converter switches at a constant frequency between boundaries, but frequency transitions smoothly from one frequency to another at the boundary. This is effectively a multi-boundary version of the lower-bound hysteretic control proposed in [5].

3.3.3 Outer loop controller algorithm

The outer loop controller determines the optimal conversion ratio, n, of the controller in order to maintain both regulation and efficiency. The control algorithm is shown in figure 3.13, and is based on the $G - V_{DROP}$ space discussed in section 3.2. Maximum conductance, G_{MAX}, is detected by sensing whether V_{GD} is less than 0.1V. As shown in figure 3.9, G approaches G_{MAX} at low V_{GD}, and thus $V_{GD} < 0.1V$ represents the scenario in which G_{MAX} is reached. The curved portion of the upper efficiency boundary in figure 3.6 is approximated by the straight line $G = G_{EB}$ in figure 3.13. This simplifies the complexity of detecting the efficiency boundary, although it introduces a region with more than one feasible conversion ratio and where efficiency may not be optimized. Detecting whether $G < G_{EB}$ is not implemented using V_{GD} because while the lower bound of V_{GD} is well controlled by the hysteretic nature of the frequency controller, the upper bound is prone to the ripple voltage transients. Instead, this controller makes use of $freq < 100kHz$ to approximate $G < G_{EB}$. The switching frequency of the converter is a monotonically increasing function of G controlled by the frequency controller, and thus contains the information of G as well. Further, the switching frequency is conveniently represented by the digital signal Clk_{count}, with $freq < 100kHz$ corresponding to $Clk_{count} > 250$. Thus using frequency instead of V_{GD} is a rather accurate and convenient way to approximate G_{EB}.

When compared with figure 3.6, region E is an additional region in figure 3.13. This region is defined by $V_{GD} > 1.4V$, and represents the scenario in which the output voltage continues to rise even though the gate drive voltage for switches $S_{1,4,5}$ is considerably lower than the threshold voltage. As V_{GD} is used to represent G, this represents a non-intuitive situation in which current continues to flow to the output even though G is already zero. This is not modeled in figure 3.8 or the $G - V_{DROP}$ space analysis in section 3.2. This scenario can happen when V_{IN} increases significantly or when a large unloading step occurs. Current may continue to flow to the drains of switches S_1 and S_4 in figure 3.7 via their body diodes. This allows current to flow to the output terminal even though the channel of PMOS transistors S_1 and S_4 are already turned off by the error amplifier. In a step-down Dickson converter, switches S_1 to S_4 can be replaced by passive diodes, but they are implemented with transistors in this work to reduce diode conduction loss. This scenario occurs when these switches operate as diodes, as they naturally do. If this scenario happens, the conversion ratio of the converter should be increased, as indicated in figure 3.13.

Region F in figure 3.13 is also a new region when compared to figure 3.6. This region represents a negative V_{DROP}, which can happen in transient due to a reduction in V_{IN}. The

converter is out of regulation in this region, but the control algorithm discussed so far will reduce conversion ratio until the converter is back in region B and under regulation. This is because the inner controller will increase G beyond G_{MAX}, and cause the outer loop controller to decrease conversion ratio. However, this response is based on feedback, and its speed is limited by stability considerations. One way to increase speed and break this requirement is to implement feedforward [27], which is the purpose of adding region F. When a negative V_{DROP} is detected, conversion ratio is reduced immediately and does not wait for the inner loop to increase G beyond G_{MAX}. Depending on the value of V_{DROP}, the conversion ratio is reduced by one or more steps and the response time is further reduced. The boundaries $V_{FF1} - V_{FF5}$ in figure 3.13 are only approximations since the exact number of steps required cannot be solely determined by V_{DROP} but also need to take into account the load current I_{OUT}. For simplicity, I_{OUT} is not measured, and this feedforward action is only designed to get the conversion ratio to roughly the correct value. The residual error is corrected by feedback action.

One may notice that region F is the only region that causes multiple step changes in n in figure 3.13. This is not only because region F is the only feedforward region, but also because other regions either lack the information, or only require one step change as in the case of region D. Region A lacks the information to determine the optimal n since the required G to maintain regulation with n_{cur} is no longer available once G saturates at G_{MAX}. Region C also lacks the required information unless it is subdivided into smaller regions by more efficiency boundaries. Subdivision of region C is not implemented in this work for simplicity, and also because the converter is under regulation in region C and a fast response is not needed. Region E probably requires at least two steps increase in n, but the exact number is difficult to determine since this is an unmodeled exceptional case. Thus for uniformity, all changes in n occur in one step, with the only exception of feedforward represented by region F.

Region G is the last additional region in figure 3.13. It is added to protect the converter from over-current conditions, and is detected by $G > G_{MAX}$ and $V_{DROP} > V_{OCP}$. Voltage V_{OCP} is given by:

$$V_{OCP} = \frac{I_{MAX}}{G_{MAX}} \tag{3.13}$$

where I_{MAX} is the maximum current rating of the converter. If I_{MAX} is reached, the power consumed by the converter may exceed its safety limit, and the converter should shut down. This is implemented by not reducing n, and allowing V_{OUT} to drop. As V_{OUT} reduces, the controller blocks will shut down automatically as V_{OUT} serve as their supply rail. The converter will stop switching and shut down. Thus this prevents the converter from supplying more current than designed, and protects it and the load from an over-current condition.

3.3.4 Outer loop controller state machine

Figure 3.14 shows the decision flow diagram of the outer loop controller, and figure 3.15 shows the state machine. The state machine has a number of states as shown in figure 3.14. State $Period_{Count}$ is used to count the number of clock phase periods that the converter has experienced after a change in conversion ratio. This number is reset after a conversion ratio

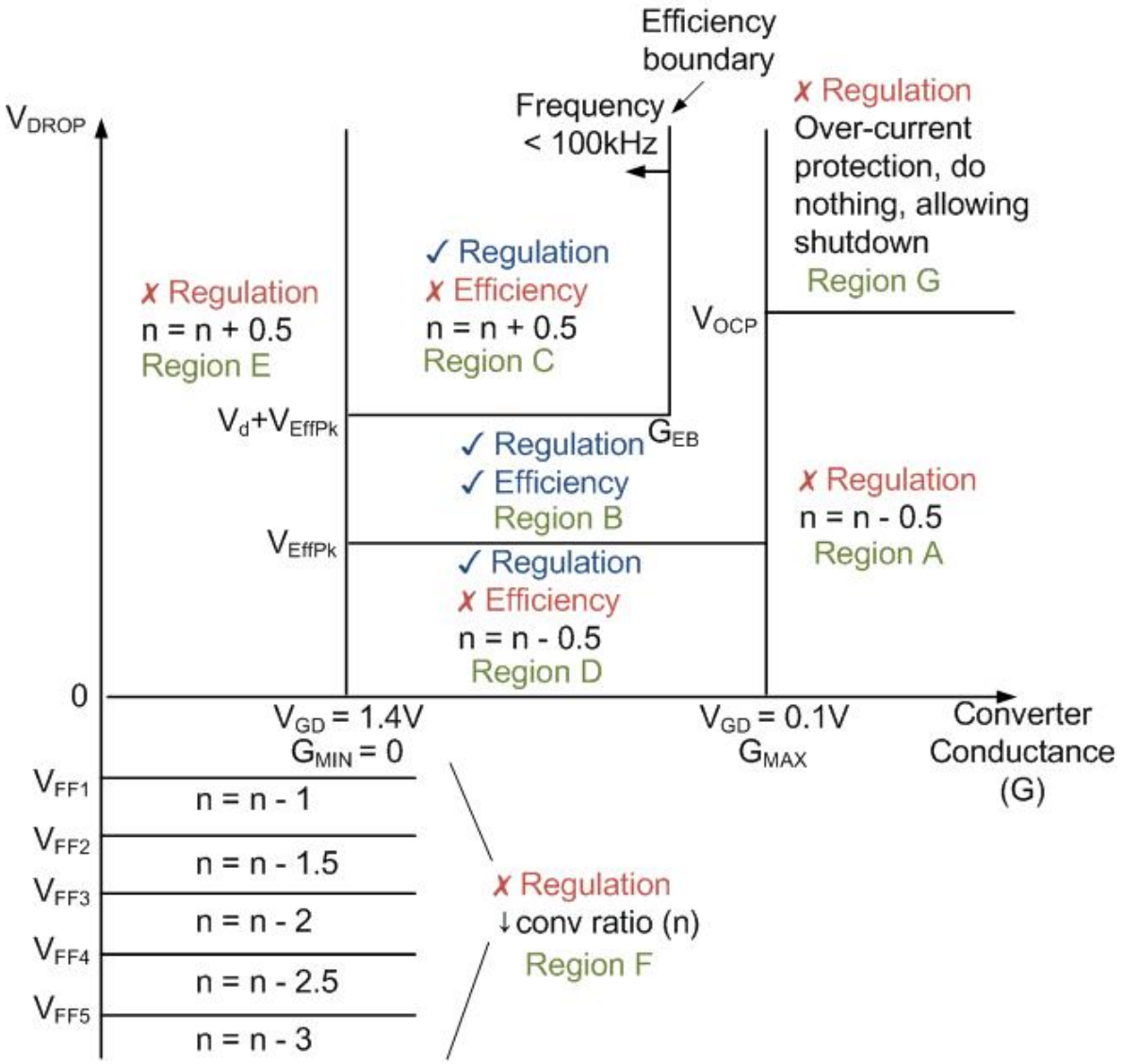


Figure 3.13: $G - V_{DROP}$ map showing the control algorithm of the outer loop controller

Input: CLK_{IN}, 50MHz, digital clock
CLK_{STATE} (from inner loop)
CLK_{COUNT} (from inner loop)
V_{GD}(quantized), gives switch conductance
V_{DROP}(quantized), gives linear regulator drop.
Output: n, conversion ratio of converter
Connect, whether to connect to input
$Count_{RESET}$, reset CLK_{COUNT} in inner loop
States: n, conversion ratio of converter
Connect, whether to connect to input
$Period_{COUNT}$, CLK_{SW} period after n changes

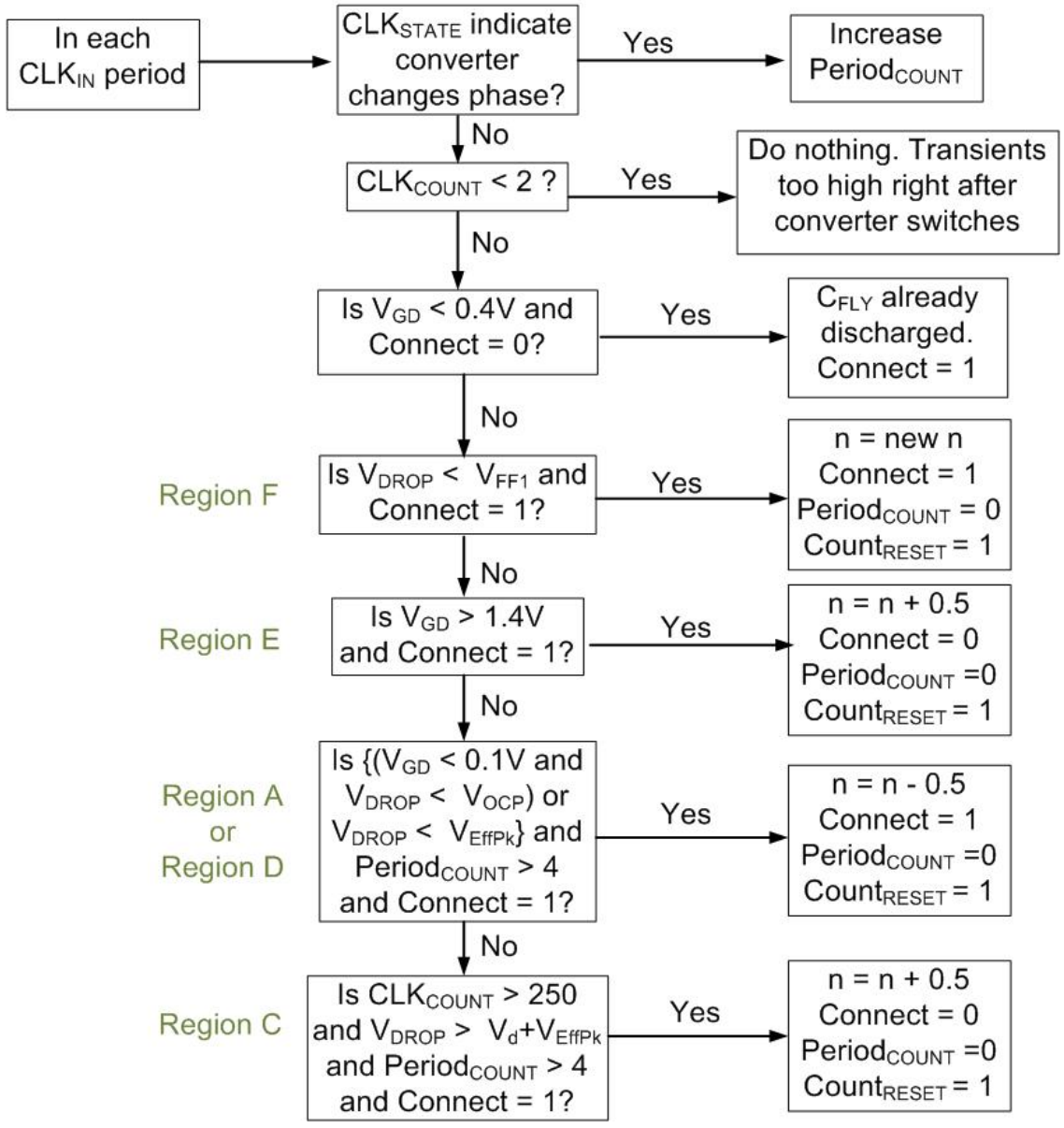


Figure 3.14: Decision flow diagram of the outer loop controller

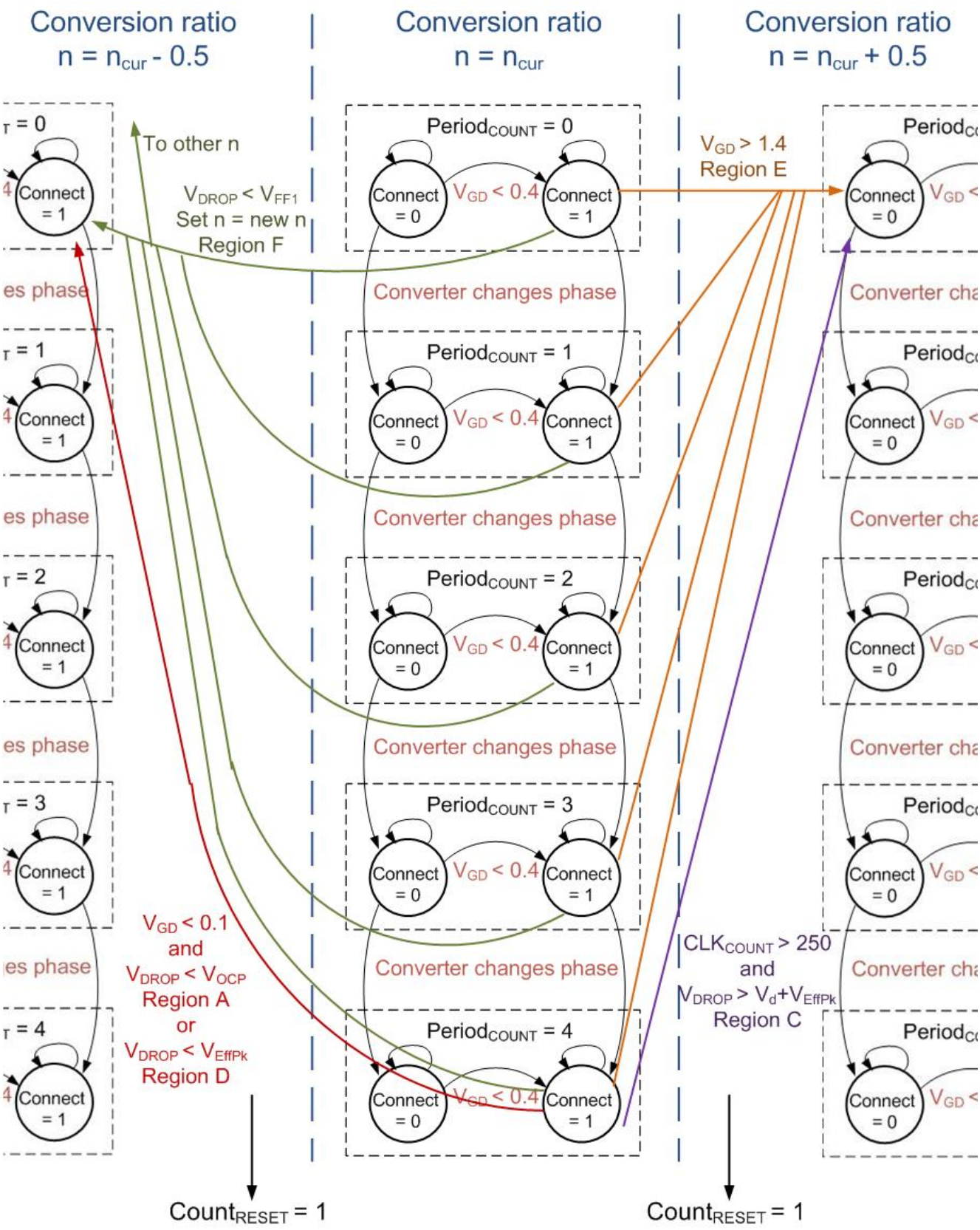


Figure 3.15: State machine of the outer loop controller

change, and is incremented by 1 each time the converter changes phase until $Period_{Count} = 4$ is reached. State $Period_{Count} = 4$ means the converter has changed phase four times, and thus 2 switching periods have elapsed. This information is used to determine whether the converter is still under a transient condition after a conversion ratio change, meaning the value of G does not yet represent a converged value. Waiting for the regulation to settle down before changing n again allows a more accurate decision, but it slows down the response if more than 1 step change in n is needed due to large variations in I_{OUT}. This design chooses an interval of 2 switching period as a compromise between these two requirements. If the converter enters into region A, C or D, the controller only changes n if $Period_{Count} = 4$. However, if the converter enters into region E or F, n is immediately changed regardless of $Period_{Count}$ because dynamics only causes uncertainty in G and these two regions do not depend on G. Region F is solely determined by V_{DROP}, and entry into region E can only be caused by a V_{IN} that is too high. The measurement results can however be affected by the ringing of the supply rails after a switch turns on and off, as discussed in subsection 4.11. This effect is avoided by introducing a blanking period implemented by no action if Clk_{Count} from the inner loop is less than 2.

As indicated in figures 3.14 and 3.15, there is a state called *Connect*, which indicates whether the converter is connected to the input source. The converter is disconnected from the input source after n is increased, and this is done by not turning on any of switches $S_{CV1} - S_{CV6}$ in figure 2.7. The reason for this is because the residual charge in the flying capacitor can cause V_{OUT} to overshoot when conversion ratio is changed with an increase in n. For example, when the conversion ratio is increased, the flying capacitors can push V_{OUT} to below its steady state value in a transient. The inner loop controller will respond to this dip in V_{OUT} by increasing G, and may even push G beyond G_{MAX} in the transient. One solution to prevent this transient from happening is to disconnect from the input terminal after an increase in conversion ratio, and wait until the voltages in the flying capacitors are drawn down before connecting back to the input. This operation corresponds to using the stored energy in the flying capacitors to supply the output load temporarily. If the converter is not disconnected from the input, some of the stored energy is actually being pushed back to the source during this transient. With the input disconnected, as the stored energy is being used, G will increase, and the converter is connected back to the input when $V_{GD} < 0.4V$. It is only after the converter is connected to the input that the controller will consider changing n again. During an unloading step that requires multiple step increases in n, this sequence can take a long time. However, since the converter is under regulation in this period of time, this is not a concern.

As discussed so far, the outer loop controller uses many signals from the inner loop, but the communication is actually two way, and the outer loop also affects the inner loop. Whenever the outer loop changes n, it instructs the inner loop to reset Clk_{Count}, and this is done by setting the signal $Count_{Reset} = 1$. Resetting Clk_{Count} after a conversion ratio change ensures that there is enough time for charge to flow among the power-train capacitors. After the converter changes phase or conversion ratio, charges start to flow among capacitors with time constant equal to that of an L-R-C network, where L comes from the parasitic inductance of the bondwires. Resetting Clk_{Count} ensures that the charges have at least 9 Clk_{IN} periods to flow, and so charge flow is not interrupted when the current peaks. Interrupting charge flow can cause significant ringings in the power rails, as discussed in

subsection 4.11.

3.3.5 Controller simulation results

Figure 3.16 shows a simulation of the converter for a moderate change in load current levels. The input voltage is at 12.5V, and the conversion ratio is maintained at 8:1 throughout the simulation because maximum converter conductance, G_{MAX}, has not been reached yet. This simulation is intended to show the behavior of the inner loop controller. As shown in the simulation, the output voltage level droops as output current increases. This change in output voltage is necessary to increase the input voltage to the error amplifier, which in turn increases G and keeps the converter under regulation. This is the familiar load-line behavior occurring in a buck converter controller and in a linear regulator. The simulation also shows that the switching frequency of the converter increases as output voltage droops. The simulation closely resembles the timing diagram of the frequency controller shown in figure 3.12. The region where the switching frequency remains constant, and where it is transitioning smoothly from one frequency to another at a boundary are also labeled in the simulation.

Figure 3.17 shows a simulation result for a large change in output current level. In order to accommodate this large output current, the converter changes conversion ratio, n, twice, as shown in the figure on the left hand side. After n changes, the output voltage increases because with a larger V_{DROP}, required G reduces, and thus the input voltage of the error amplifier also reduces. This reduction in G accompanies a reduction in switching frequency, and thus the ripple voltage increases after n changes. The significantly larger ripple for one clock cycle after the second n change is due to the residual charge in the flying capacitors. The simulation on the right hand side shows the behavior of the controller for a large current step. Although the current ramp simulation shows that n only needs to reduce twice for this I_{OUT} change, n reduces 3 times in the current step simulation. This is due to the controller responding to the large initial transient in V_{OUT}. The converter stays at the conversion ratio $n-3$ after the transient and does not change to $n-2$ due to the build in hysteresis region. One way to avoid this over-reaction is to wait for a longer period of time after n changes before allowing it to change again. However, in the cases where n indeed needs to change more than once, this can result in a significant transient in V_{OUT}. Thus this "wait time" needs to be chosen based on a compromise. Through ample simulations, a "wait time" of four clock period, around 80ns, is chosen, and thus the outer loop controller is not allowed to change conversion ratio when $Period_{Count} < 4$, as discussed in subsection 3.3.4.

As discussed in subsection 3.3.4, the converter disconnects from the input source after n increases, and uses the stored charge in the flying capacitors. Figure 3.18 shows a simulation of this behavior. The simulation begins with a step increase in I_{OUT} to get the controller to decrease conversion ratio. The change in conversion ratio is shown by the change in the least significant bit (LSB) of the conversion ratio. This is followed by an unloading step. As shown in the simulation, the converter is disconnected from the input source once n increases, as shown by the signal NoConnect. As the stored energy in the flying capacitors is being consumed, the converter switches faster. The converter finally connects back to the input source at around $180\mu s$.

Figure 3.19 shows a simulation of the behavior of the converter for changes in input

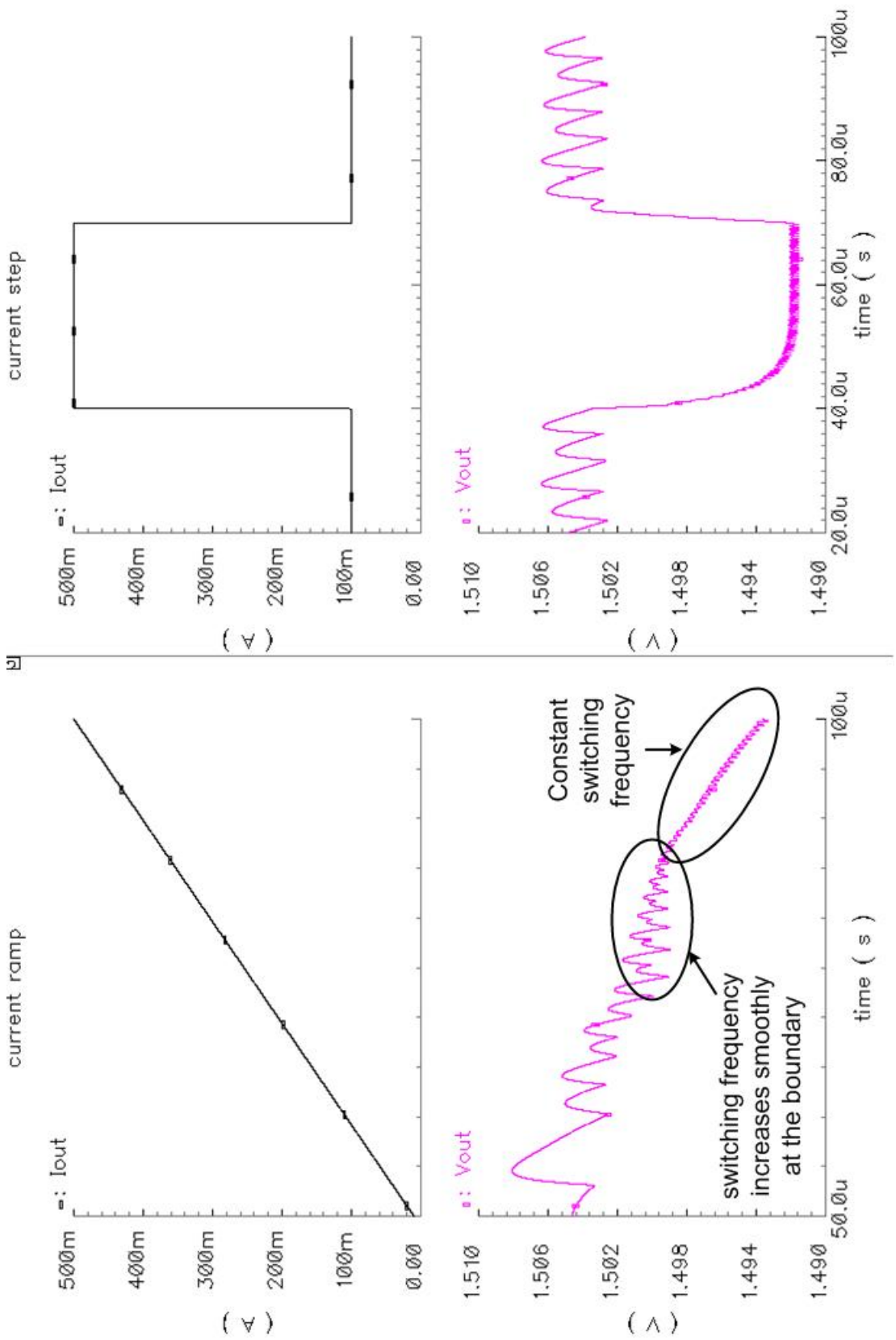


Figure 3.16: Simulation displays output voltage of the controller for a moderate change in output current level. The left hand side plot shows the response with a ramp change in output current whereas the right hand side plot shows the response with a step change in output current.

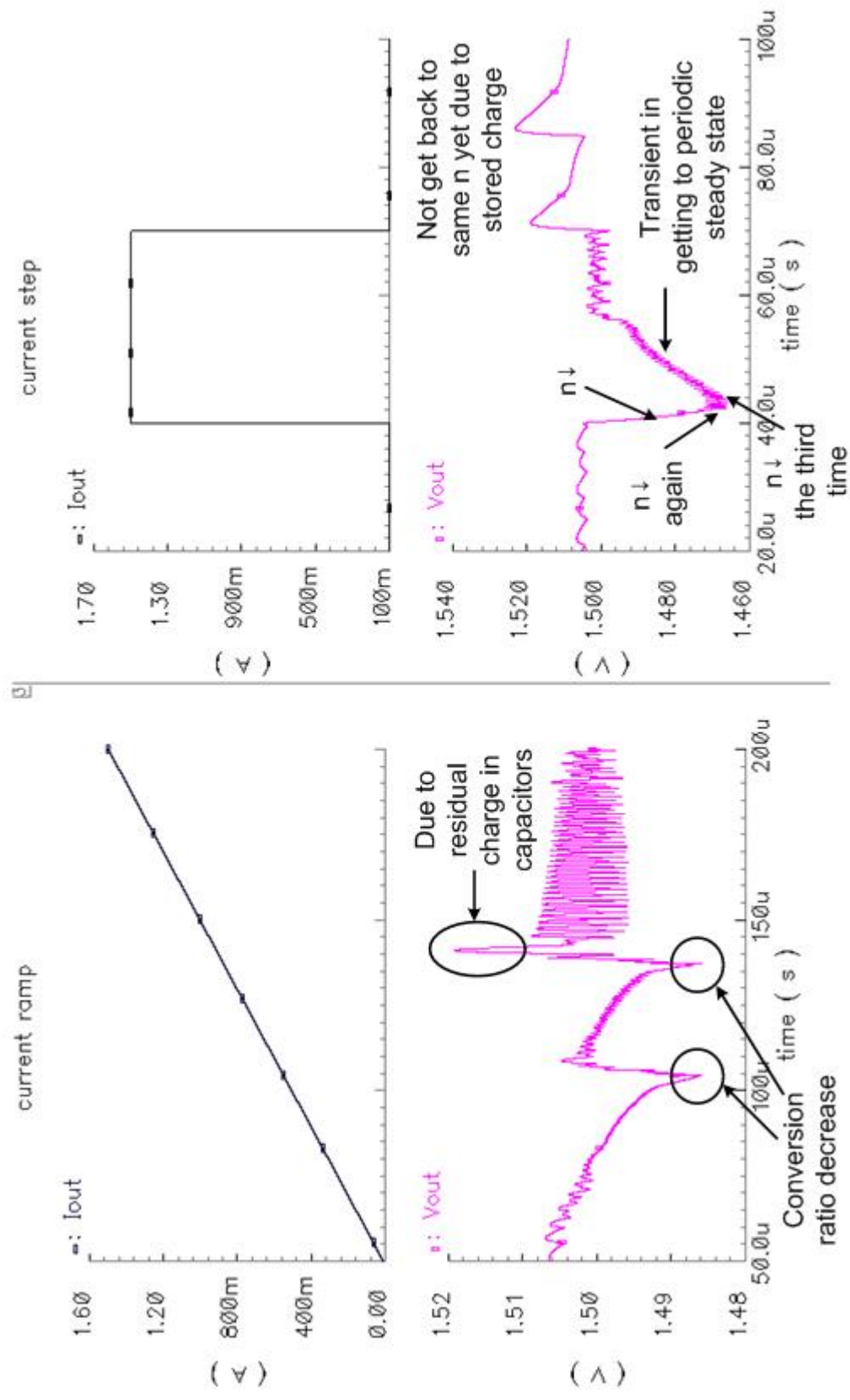


Figure 3.17: Simulation displays output voltage of the converter for a large change in output current level. The left hand side plot shows the response with a ramp change in output current whereas the right hand side plot shows the response with a step change in output current.

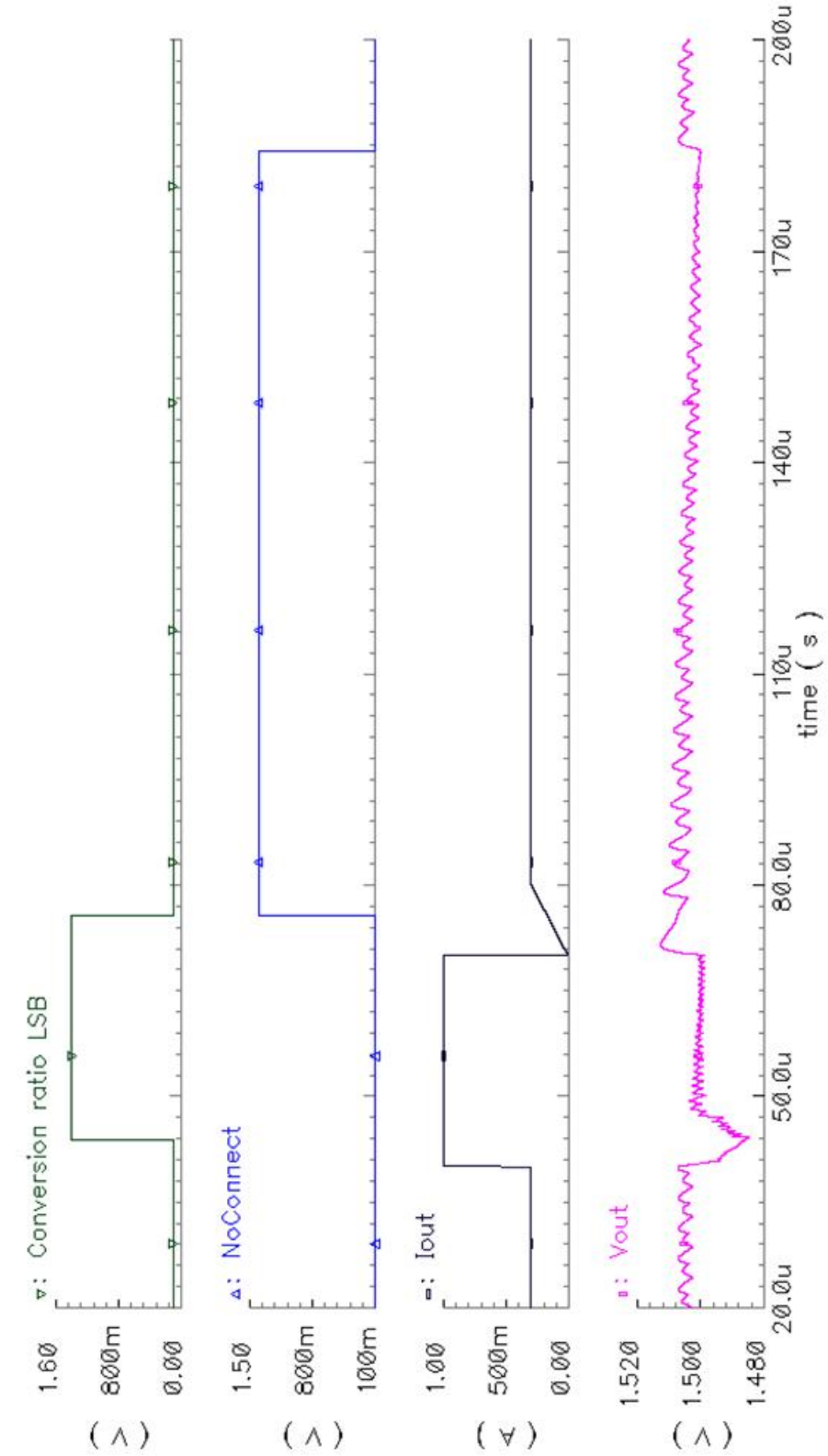


Figure 3.18: Simulation showing the converter connecting back to the input after an unloading step.

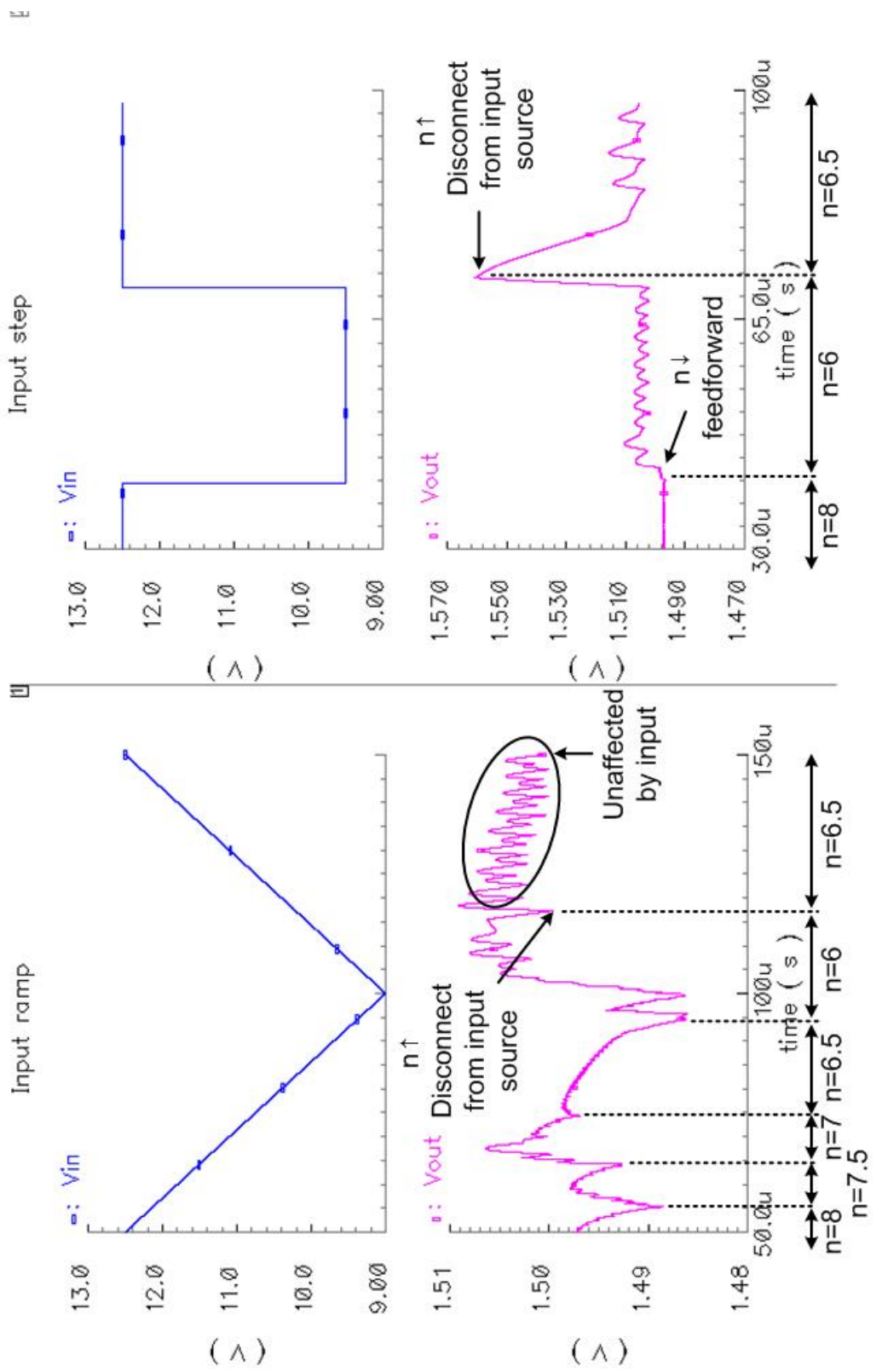


Figure 3.19: Simulation displays output voltage of the converter for changes in input voltage levels. The left hand side plot shows the response with a ramp change in input voltage whereas the right hand side plot shows the response with a step change in input voltage.

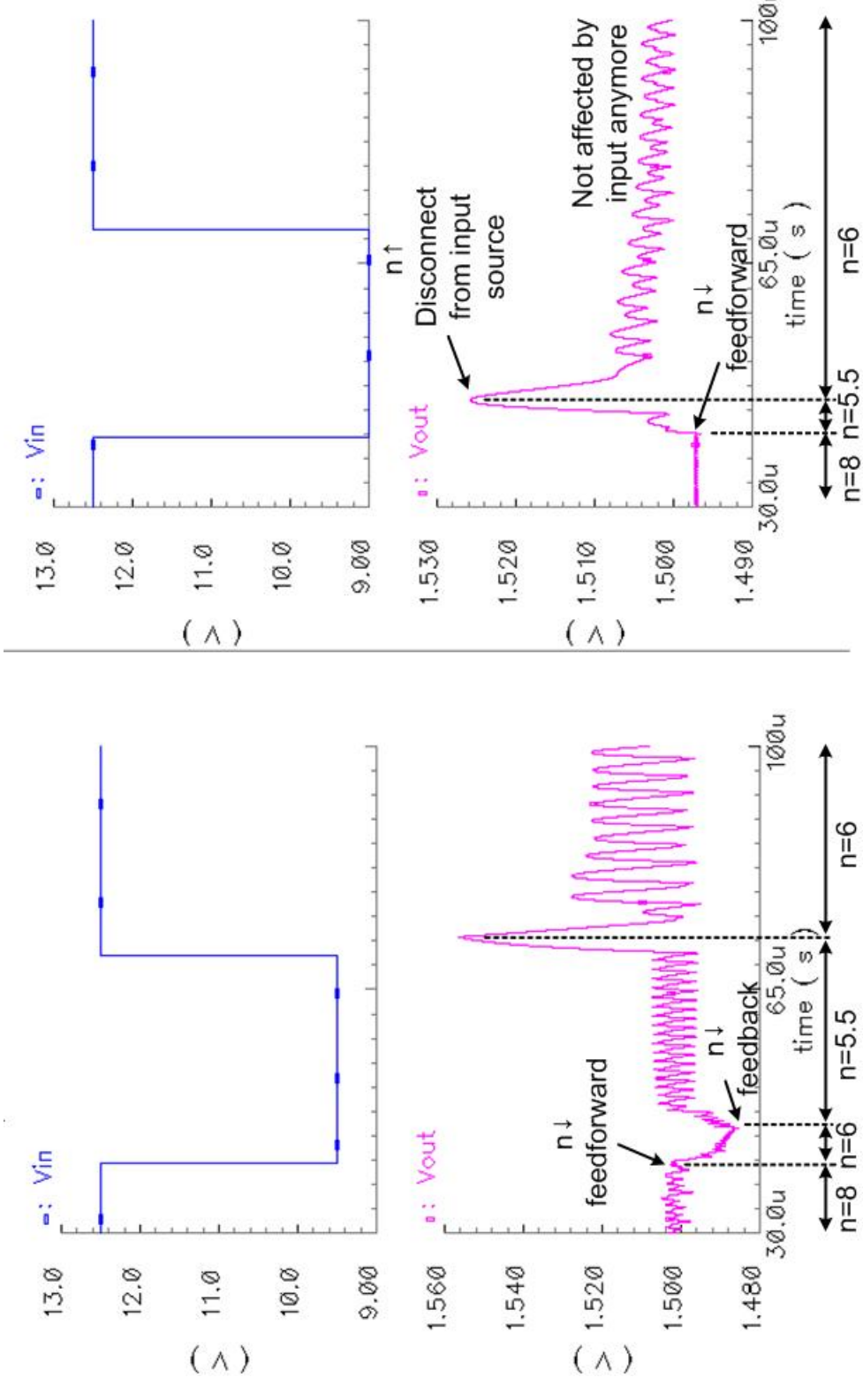


Figure 3.20: Simulation result in which feedforward action of controller does not acquire the correct conversion ratio. The left hand side plot shows the response with a ramp change in input voltage whereas the right hand side plot shows the response with a step change in input voltage.

voltage levels. In the left hand plot, when the input voltage reduces gradually, the converter decreases n by feedback action and with one step at a time. When the input voltage increases, the controller increases n, and disconnects from the input source. The output voltage is independent of V_{IN} variations during the interval in the disconnected condition. In the right hand plot, when the input voltage steps down, the converter decreases conversion ratio by several steps immediately due to feedforward, and the converter maintains regulation. When the input voltage steps back up, the converter enters region E in figure 3.13. The controller increases n immediately, and disconnects from the input source. The input voltage reduction step simulation shown in this figure is a case in which feedforward acquires the correct n and no substantial feedback action is needed afterward. This is not necessarily always the case, and the feedforward action may acquire an n one level too low or one level too high depending on the load current I_{OUT}. As discussed in subsection 3.3.3, this potential error may occur since the feedforward action is only dependent on V_{DROP} while determining the next setting of n, although the correct value of n also depends on I_{OUT}. This residual error in n after a feedforward action will be corrected by feedback action. Figure 3.20 shows two cases in which the feedforward action does not acquire the correct n. In the left hand plot, the feedforward is one step short. As a result, the output voltage continues to drop until n decreases again due to feedback action. In the right hand plot, the feedforward steps one step in excess. The output voltage thus increases until n increases by one step. This simulation shows the non-intuitive case in which the output voltage can actually increase when the input voltage decreases sharply. In both cases, the feedback action of the controller corrects for the discrepancy in the feedforward action, and maintains regulation.

3.3.6 Startup controller

The startup sequence of this converter, as discussed in subsection 2.5.2, is also implemented with digital control. The startup sequence is divided into two halves. In the first half of the sequence, the high voltage blocking switch in figure 2.9 is turned off while the linear regulator is turned on. The precharging regulator charges up the "output" terminal of the converter while the converter runs in boost mode to charge up the internal capacitors. Switches $S_5 - S_{13}$ in figure 2.7a are not used during this half of the startup sequence, but instead helper switches discussed in section 4.3 are used. This is because control signals cannot be conveyed to switches $S_5 - S_{13}$ before the voltage domains are charged up. Switches $S_1 - S_4$, on the other hand, reside in the same voltage domain as the controller, and thus they can be controlled and used. The controller causes the converter to change clock phase when there is enough charge stored in the output capacitors. This condition is detected by comparing the "output" voltage to $1.5V$, and this makes the controller behave as a single-boundary upper bound hysteretic controller, as opposed to the multi-boundary lower bound hysteretic controller discussed in subsection 3.3.2. As the flying capacitors are being charged up, less charge is supplied by the output capacitor in each clock phase, and the switching frequency of the converter increases. After the converter switches at maximum frequency for several dozens of clock cycles, the flying capacitors are mostly charged up, and the controller will move to the second half of the startup sequence. Figure 3.21 shows a simulation result of the startup sequence. The curves show the output voltage level and the voltage levels of the flying capacitors of the circuit shown in figure 2.2. As shown in the figure, the switching

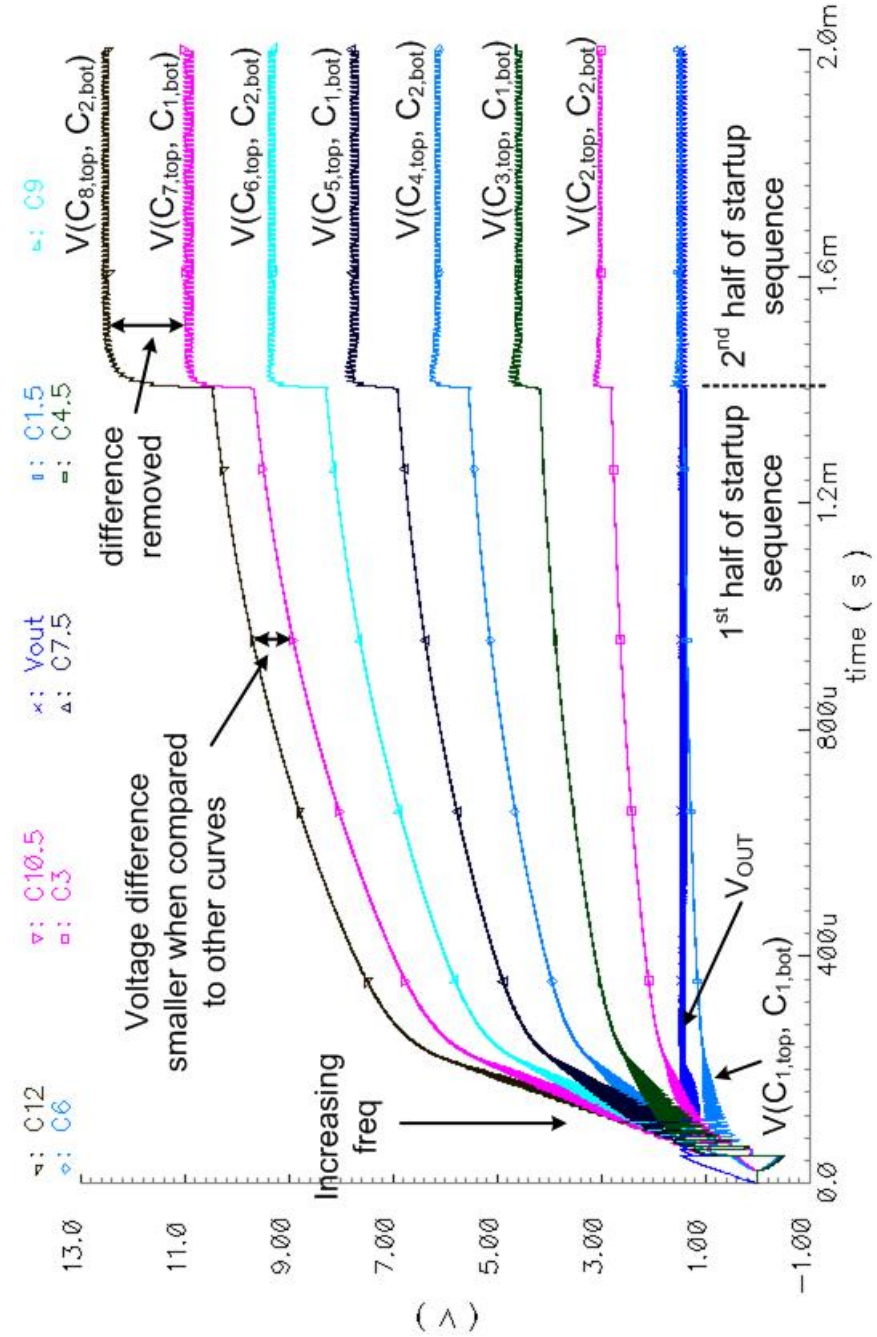


Figure 3.21: Simulation of the startup sequence showing the output voltage and the voltage levels of the various flying capacitors of the circuit shown in figure 2.2.

frequency of the converter increases during the first half of the startup sequence, and remains constant for a certain period of time before entering the second half of the startup sequence.

In the second half of the startup sequence, all the main switches $S_5 - S_{13}$ are utilized in order to fully charge up the flying capacitors. This is necessary because the helper switches are small in size, and thus cause voltage drop in the voltage levels of the flying capacitors. This can be explained with the fast switching limit of the output referred resistance of an SC converter, as discussed in section 1.1. As shown in figure 3.21, the voltage levels of the flying capacitors increase significantly as the converter enters the second half of the startup sequence. Further, as discussed in section 4.3, the helper switches cause a diode drop in the last voltage level, and cannot fully charge up the last flying capacitor. This is evidenced in the simulation by the smaller voltage difference between the top two curves when compared to the other curves in the first half of the startup sequence. With the voltage domains mostly charged up, the levelshifter circuits can now function, and the main switches can be used to eliminate the residual error in the flying capacitor voltage levels. In the simulation, the voltage difference among the curves becomes equal in the second half of the startup sequence. However, as discussed in section 4.1, the speed of the levelshifter circuit is greatly reduced when the voltage level of the top voltage domain is reduced. Thus the converter is designed to switch at 1/10 of the maximum frequency in this second half of the startup sequence. This reduced frequency is also visible in the simulation.

During the second half of the startup sequence, the high voltage blocking switch in figure 2.9 is turned on since it is no longer needed for protection. However, switches $S_{CV1} - S_{CV6}$ in figure 2.7a remains off so the converter is still effectively disconnected from the input source. The controller will make use of the information on V_{DROP} during this period of time to determine a rough estimate for optimal conversion ratio, n. After the converter runs for 64 cycles, or about 256ms, the startup sequence is done, and the converter will start running in normal mode with this newly determined n. The normal mode algorithm discussed in subsections 3.3.3 and 3.3.4 will correct for any remaining error in n. The precharging regulator is turned off after the startup sequence is completed.

Chapter 4

Circuits

Chapters 1 to 3 discuss the overall picture of this design, and this chapter focuses on the circuit details used to implement the design. The controller in this design powers from the output of the converter, as do most circuits discussed in this chapter, unless otherwise specified. For simplicity, the circuits are labeled as directly powering from the output, but in actual implementation, they power from a filtered supply connected to the output. This filtered supply uses on-chip capacitors to eliminate the transients on the output rail due to parasitic inductance and the switching action of the converter. There are two filtered supplies, one for the analog circuits and one for the digital circuits. The two supplies are separated so that the analog circuits, which are less power-hungry but more prone to noise, are not affected by switching noise of the digital circuits.

4.1 Levelshifters

As discussed in section 2.2, the converter is divided into various voltage domains, and thus levelshifters are needed to convey signals among them. Figure 4.1 shows the levelshifter design implemented in this work, which is similar to that in reference [28]. To obtain more voltage domains, as used in the converter shown in figure 2.2, voltage domain 2 is instantiated multiple times depending on the number of voltage domains required, but is only shown once in the figure for simplicity. The circuit consists of two strings of transistors connected at the top by a cross-coupled half-latch. It operates with either NMOS transistors M_1 or M_2 pulling down one string, and then the cross-coupled PMOS pair M_{11} and M_{12} pulling up the other string. Transistors $M_3 - M_{10}$ act as cascode devices to limit the voltage swing at each node, such that each transistor is only subjected to a fraction of the overall voltage level applied to these two strings of transistors. Capacitors $C_1 - C_6$ are added such that all the output signals ($V_{OUT1} - V_{OUT3}$) are initially low, and cause the main switches $S_5 - S_{13}$ in figure 2.7a to stay off during the first half of the startup sequence.

In order for the levelshifter to switch state, transistor M_{11} or M_{12} has to be overpowered, and thus the sizing of transistors in figure 4.1 have to be carefully chosen. Transistors M_1 and M_2 have to be sized stronger than transistors M_{11} and M_{12} in all cases. If the voltage level M_{11} or M_{12} of any voltage domain deviates significantly from design value, the relative strength of the transistors may change and the levelshifter will fail to switch state. This

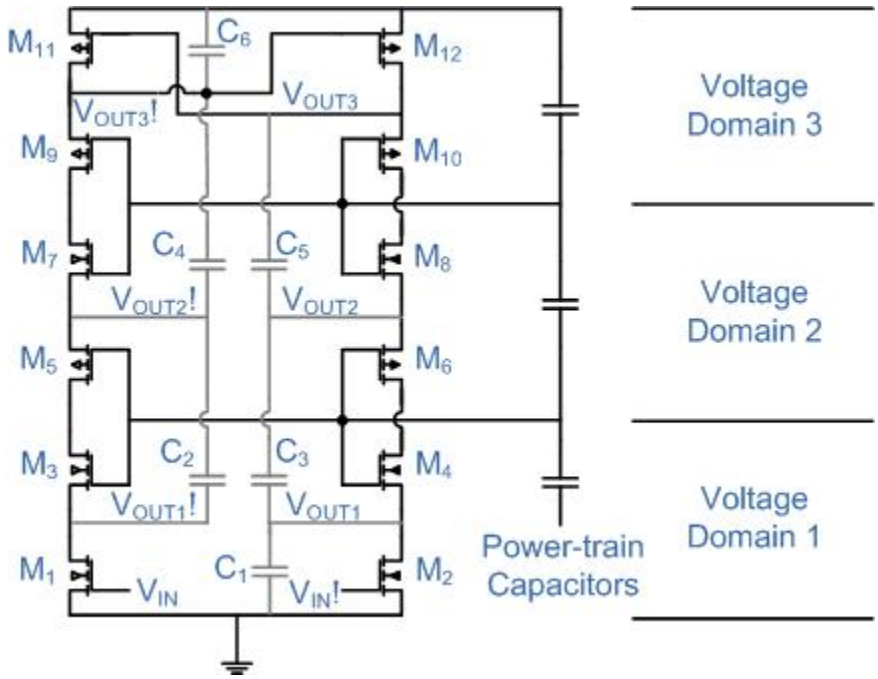


Figure 4.1: Levelshifter to convey signals among voltage domains. The circuit is divided into three voltage domains. Capacitors $C_1 - C_9$ are added to give initial states during startup.

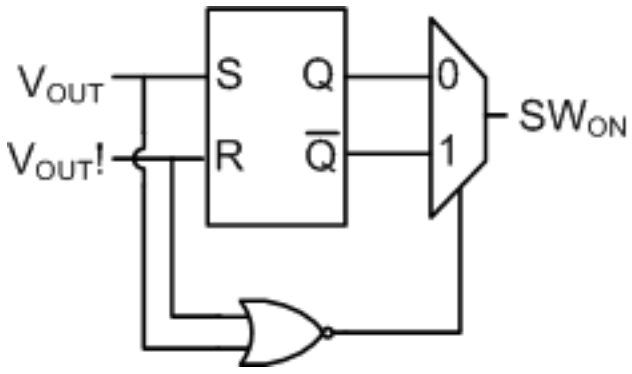


Figure 4.2: Figure showing the latch installed to interpret the output of the levelShifter circuit. When both V_{OUT} and $V_{OUT}!$ are low, this latch gives the inverse of the previous state. This speeds up the response time of the levelShifter during the transition period.

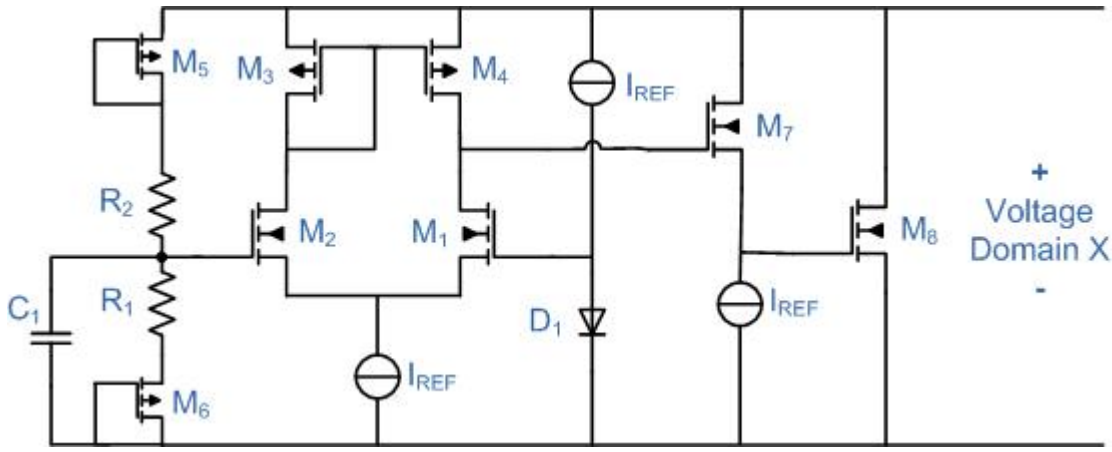


Figure 4.3: Detail of the shutdown protection clamp

consideration favors the ladder capacitor configuration over the star capacitor configuration discussed in section 2.1 since the ladder capacitor configuration ensures that when V_{IN} or conversion ratio, n, changes, all voltage domain voltage levels change in tandem. This ensures that the relative strength of the switches in the levelshifters are unaltered, and the chance of levelshifter malfunction is reduced. As discussed in section 3.3.6, at the end of the first half of the startup sequence, the voltage level of the top voltage domain is significantly lower than design value. Since this reduces the strength of transistors $M_{11,12}$, this does not cause the levelshifter to fail, but causes it to operate significantly slower. This problem is solved by running the converter ten times slower during the second half of the startup sequence. The requirement that transistors $M_{1,2}$ be stronger than $M_{11,12}$ in all cases also causes the rising edge of the levelshifter to be significantly slower than the falling edge. Simulations show that the delay of the falling edge is about 3ns whereas the delay of the rising edge is about 30ns. In order to avoid the delay in the rising edge, latches, shown in figure 4.2, are added to use the previous state to determine the next state when both outputs, V_{OUT} and V_{OUT}!, in each voltage domains are low during a transition. This allows the output of the levelshifter to switch state once a falling edge occurs, and thus effectively increases the speed of the levelshifters. Speeding up the levelshifters allows a reduction in the amount of deadtime required to ensure non-overlapping two-phase clock signals. The power consumption of the levelshifters is negligible when compared to the leakage power and switching power of the power switches. The area consumption of the levelshifters is about $0.25mm^2$ in total. The area consumption is not negligible because most transistors in the levelshifter have a separate well in order to avoid body effect from increasing the threshold voltages of the cascode transistors $M_3 - M_{10}$. An increase in threshold voltage will reduce the swing in the differential output signals, and in turn reduce the noise margin of these digital signals.

4.2 Shutdown protection clamps

As discussed in section 2.5.1, shutdown protection clamps are installed in each voltage domain to limit the peak voltage level at shutdown. This section discusses the detailed implemen-

tation of these shutdown protection clamps. A conceptual design of the clamp circuit was shown in figure 2.8, while its detailed schematic is shown in figure 4.3. The clamp consists of an NMOS differential pair that compares the divided voltage level of the voltage domain to a reference voltage, and turns on transistor M_8 if over-voltage is detected. This circuit is designed to draw minimal power such that the standby current of these clamps does not exceed the leakage current of the power-train switches. Since the clamp protects the converter from voltage drift in the power-train capacitor network during shutdown, it can be rather slow. Further, since 2V transistors and 5V transistors are used in 1.5V and 3V voltage domains respectively, the clamp turn on voltage is designed to be well above the working voltage domain levels, and thus high accuracy is not required in these clamps. With this specification, several features of these clamps are designed to strategically tradeoff accuracy and speed with power consumption.

The reference voltage is generated by passing a reference current, I_{ref}, through a pn diode, where all I_{ref} in figure 4.3 are generated by the current reference circuit discussed in section 4.9. The reference voltage from the bandgap reference discussed in section 4.10 is not used because it is more power hungry than the current reference, and is only implemented in voltage domain 1 in figure 2.2. On the other hand, protection clamps are required in all voltage domains, and thus the low power current reference is implemented in each voltage domain to provide the reference current for each clamp. Transistors M_5 and M_6 are added to reduce the voltage drop across the resistive divider, such that the current flow can be minimized. Due to the high resistance ($\sim 1M\Omega$ each) of resistors R_1 and R_2, the gate of M_1 is prone to capacitive coupling into the node. Since the clamp circuit resides in voltage domains that move relative to the the substrate ground in each clock phase, coupling can occur through parasitic capacitance to the substrate. Capacitor C_1 is added to reduce this coupling effect and to prevent the clamp from inadvertently turning on. A source follower consisting of transistor M_7 is added so that the differential pair can be of minimum size and consume minimal power. This source follower also levelshifts the output of the differential pair such that the V_{GS} of transistor M_8 is at 0V when it is turned off. Each clamp circuit is designed to draw about $200nA$ when off, and draw about $5mA$ when on. The area of the clamp circuits is mostly made up of the high resistance resistors R_1 and R_2, and is about $0.1mm^2$ in total. The total combined static power drawn by all the clamp circuits together is about $6\mu W$.

4.3 Startup helper circuits

As discussed in subsection 3.3.6, the main switches $S_5 - S_{13}$ in figure 2.7a are not utilized in the first half of the startup sequence but helper switches are used instead. Figure 4.4 shows the startup helper circuits implemented in this work, motivated by the scheme used in [18]. It consists of an inverter driving an NMOS transistor parallel to the main switch in each voltage domain. In the beginning of the startup sequence, switches $S_1 - S_4$ are driven in a two phase manner as indicated in the figure. Switches $S_5 - S_{13}$ all have gates connected to sources, but since the converter is running in boost mode during startup, the voltages are reversed and they act like diodes. Charges are thus being pushed up this ladder of capacitors sequentially as the converter changes clock phase. However, pushing charges through diodes

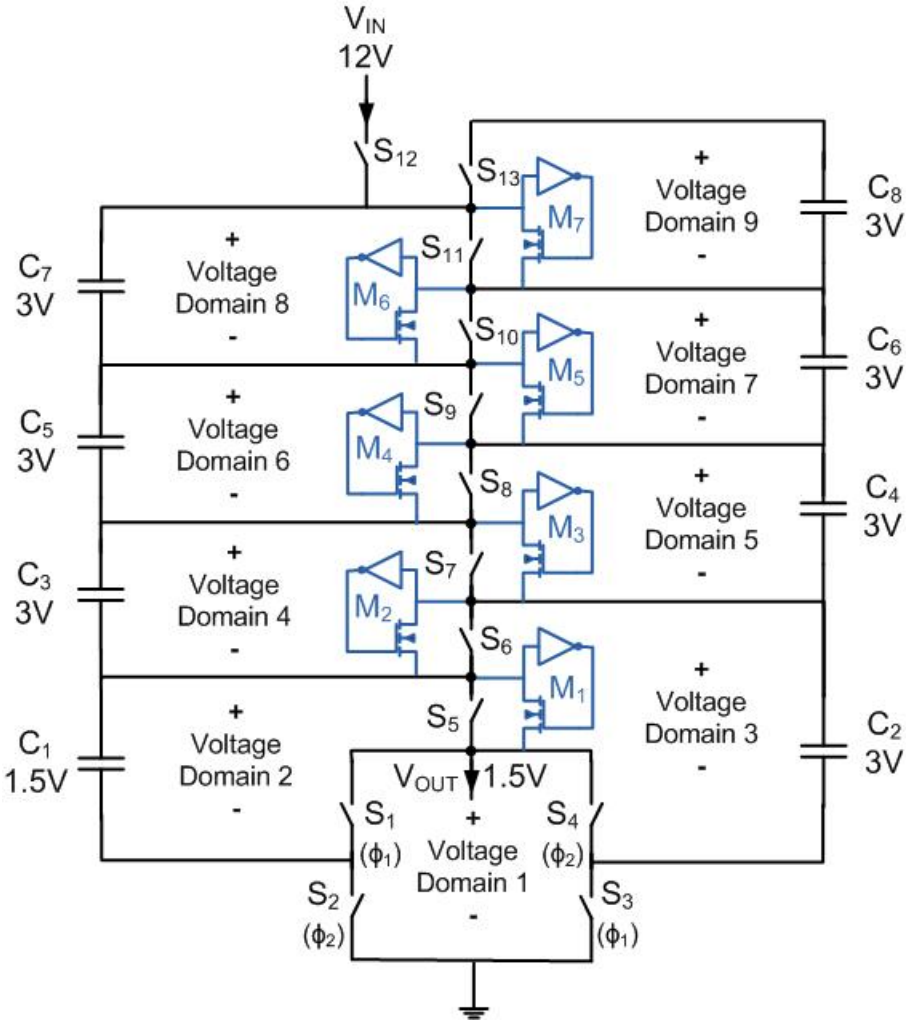


Figure 4.4: Startup helper circuits

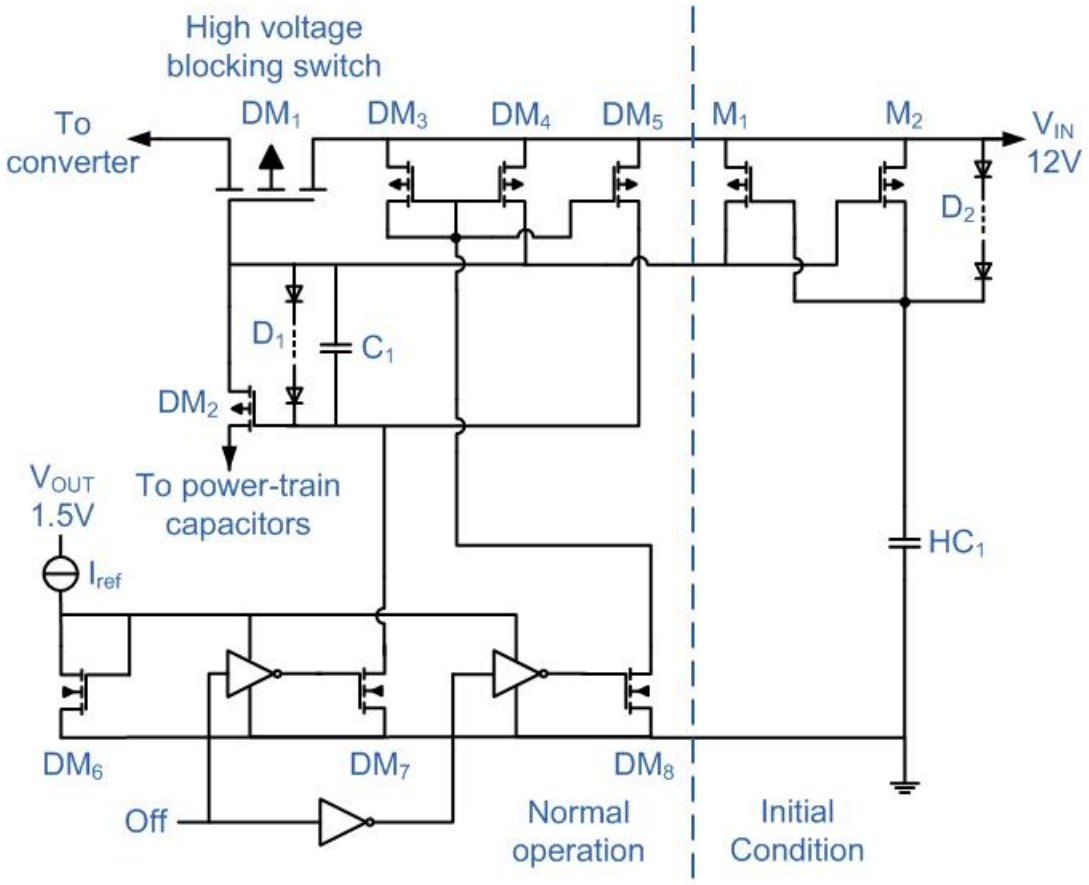


Figure 4.5: Schematic of the high voltage blocking switch used in startup and its drivers

requires voltage drop and the capacitors will not fully charge up to designed values in this simple scheme. In order to eliminate this diode voltage drop, helper transistors $M_1 - M_7$ are installed. The inverter of each helper switch is driven by the string of power-train capacitors, and turn on the helper switch when its parallel main switch is conducting as a passive diode. This driving scheme does not require control signals and thus can operate before the voltage domains are built up. These helper switches eliminate all diode drops except in the highest stage, corresponding to voltage domain 9. Voltage domain 9 cannot be fully charged up even with this scheme due to the lack of helper switch for switch S_{13}, and thus the second half of the startup sequence discussed in subsection 3.3.6 is required. For simplicity, these helper switches are not disabled during normal operation. They are designed to be more than 100 times smaller than the main switches, and thus do not interfere with the converter during normal operation and consume negligible power and die area.

4.4 High voltage blocking switch

As discussed in subsection 2.5.2, the converter is separated from the input source by a high voltage blocking switch in the beginning of the startup sequence. Figure 4.5 shows the schematic of the high voltage blocking switch and its drivers. Laterally diffused metal oxide

semiconductor (LDMOS) devices are available in this process, and are used to implement this high voltage switch. The LDMOS devices used can block 12V, while its gate-to-source voltage can withstand 5V. Device DM_1 is the high voltage blocking switch, whereas device DM_2 is used to connect the gate of this PLDMOS device to either the bottom plate of power-train capacitor C_3 or the top plate of power-train capacitor C_4 in figure 4.4 depending on the conversion ratio. Device DM_7 is used to turn on DM_2 which then turns on DM_1. Devices DM_3, DM_4, DM_5 and DM_8 are used to turn off DM_1 and DM_2. Devices DM_1 to DM_8 are all implemented with LDMOS devices, and since their gates can only handle 5V, a diode string D_1 is added to protect the gate of DM_2 from over voltage stress. This design has a constant current draw by either DM_7 or DM_8, and to limit this current, the gates of DM_7 and DM_8 are connected to the gate of DM_6 when either is on. The gate voltage of DM_6 is controlled by the current reference I_{ref}, which is provided by the current reference discussed in section 4.9.

Devices M_1 and M_2 are used to set the initial conditions of the high-voltage switch. When the converter is connected to the input source initially, the output voltage has not been charged up by the linear regulator yet, and thus neither DM_7 or DM_8 can work. Transistors M_1 and M_2 act as a half latch to ensure that the V_{GS} of DM_1 remains at 0V. A high voltage capacitor HC_1 is added to ensure that this half-latch attains the correct state at startup. There is no dedicated high-voltage capacitor technology in this process, and so this high-voltage capacitor is implemented with the n-well to p-substrate p-n junction capacitance. Transistors M_1 and M_2 do not need to block high voltages, and they are both implemented with 5V PMOS transistors. Diode string D_2 is added to protect the gate of M_1 from over voltage stress. Once DM_1 is turned on by DM_2 and DM_7, this half latch will switch state, and it will not interfere with the operation of the other circuits. Capacitor C_1 is also included to ensure that DM_2 remains off initially and does not interfere with the operation of the half-latch. Since the high-voltage switch is not switched during normal operation, it and its control circuits are designed to be slow and consume about $40\mu W$ of static power. The static power consumption mostly comes from the static current drawn by transistors DM_6 and DM_7 to keep DM_1 on. The area of pass switch DM_1 is not negligible in order to minimize series resistance. The total area including control circuits is about $0.27mm^2$.

4.5 Precharging regulator

As discussed in subsection 2.5.2, a precharging regulator is used to charge up the output of the converter during startup. Figure 4.6 shows the schematic of the precharging regulator implemented in this work. This regulator sources a constant current of 2A when on, and turns off when the output is charged to 1.5V.

Similar to the high-voltage switch discussed in section 4.4, this precharging regulator utilizes 12V LDMOS transistors since it needs to block high voltage levels. Transistors DM_1 to DM_8 are implemented with 12V LDMOS transistors, whereas transistors M_1 to M_4 are implemented with 1.8V transistors. Transistor DM_1 is the pass transistor of the precharging regulator, and it is pulled down by DM_2 to stay on. Diode string D_1 and resistor R_1 are added to protect the gate of DM_1 from over-voltage stress. High voltage capacitor HC_1

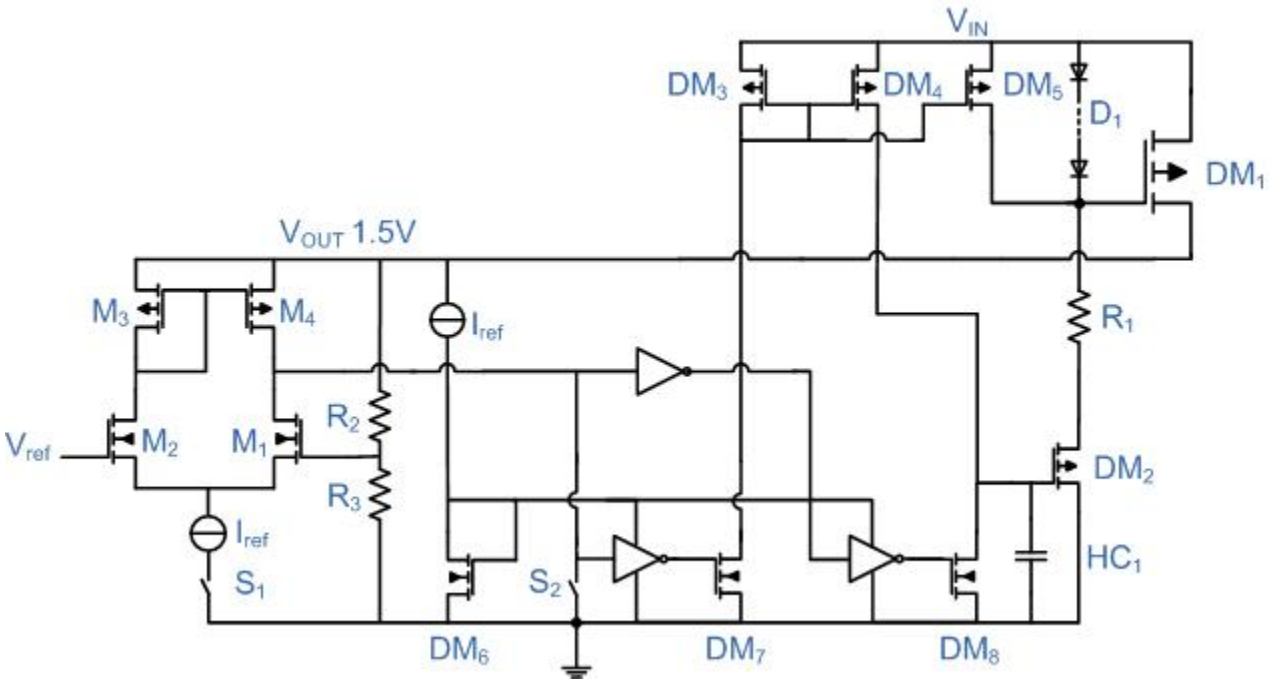


Figure 4.6: Schematic of the Linear Regulator

is added to ensure the precharging regulator is on initially. Devices DM_3 to DM_8 are used to turn on and off the precharging regulator, similar to the ones for the high voltage switch in figure 4.5. Device DM_6 and the current reference are shared with the high voltage switch, but are repeated here for clarity. The precharging regulator is turned on and off by the differential pair consisting of transistors M_1 to M_4. The differential pair compares a reference voltage V_{ref} to a divided version of V_{OUT}, and turns on the precharging regulator when V_{OUT} is lower than 1.45V. Unlike the reference voltage in the active clamp in figure 4.3, this V_{ref} is generated by the bandgap reference in section 4.10. This is because the more accurate bandgap reference is now available as both circuits are in the same voltage domain. The resistive divider consisting of R_2 and R_3 is part of the voltage divider discussed in section 4.7, but is repeated here for clarity. Due to the voltage levels of the two compared signals, NMOS source followers are added before the differential pair to levelshift the voltage levels, but are not shown here for simplicity. Switches S_1 and S_2 are used to turn off the precharging regulator when the converter is no longer in startup mode. The source followers not shown in the figure are also turned off by switches when the precharging regulator is disabled. The precharging regulator is designed to supply about 2A of current, and it takes up about $0.07mm^2$ of die area. When the precharging regulator is turned off during normal operation, it consumes about $40\mu W$ of static power. Most of the power is being consumed by transistor DM_7 to keep the precharging regulator off.

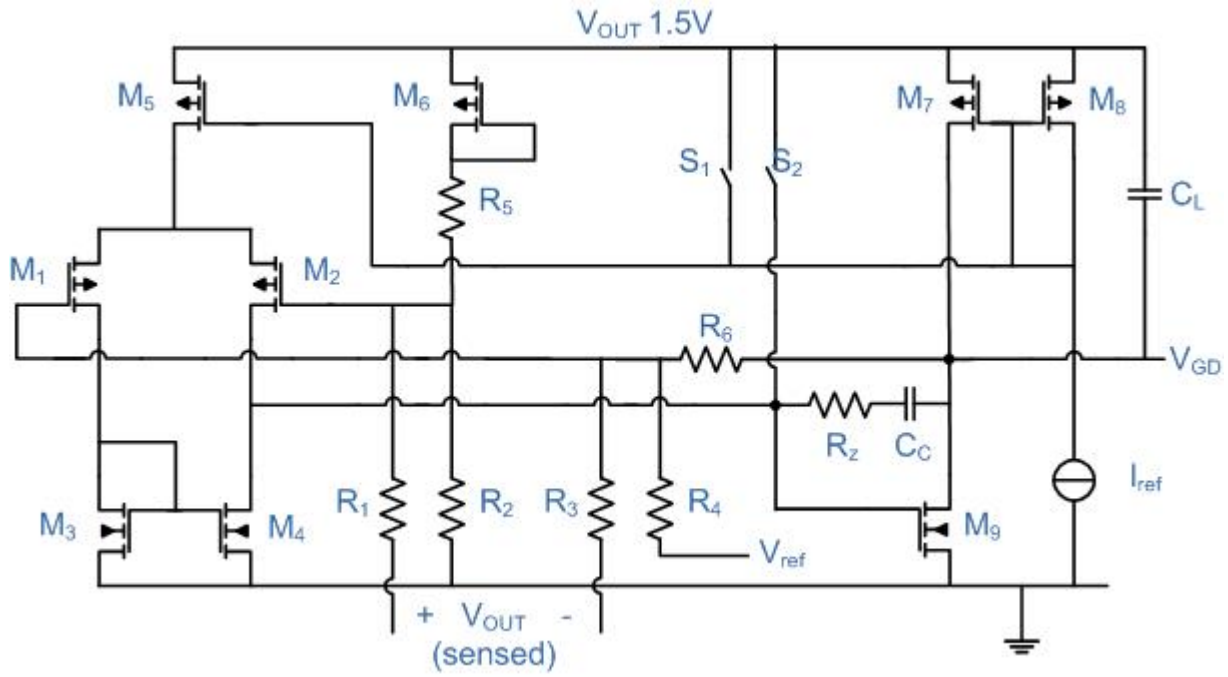


Figure 4.7: Schematic of the error amplifier making up the switch conductance modulation block in figure 3.7.

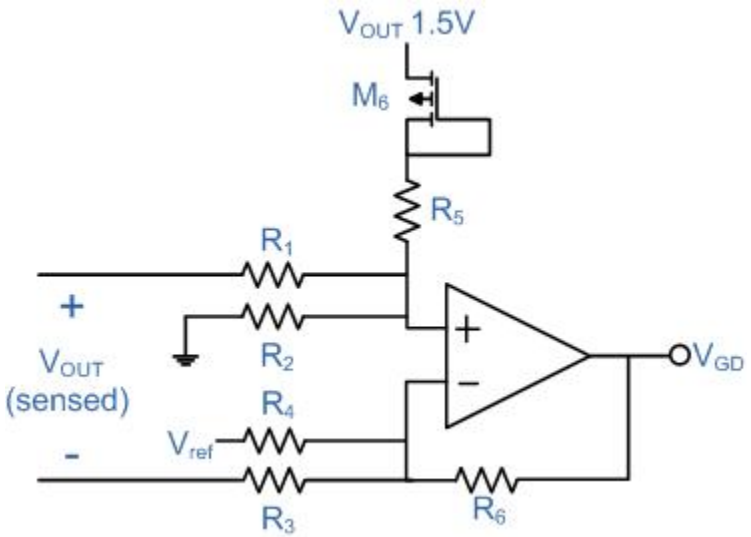


Figure 4.8: Simplified diagram of the error amplifier in figure 4.7.

4.6 Error amplifier

As discussed in section 3.3 and shown in figure 3.7, an error amplifier is used to achieve switch conductance modulation. Figure 4.7 shows the schematic of the error amplifier implemented in this work, and figure 4.8 shows a simplified version of the schematic. The error amplifier is a two-stage transconductance amplifier. A differential front end consisting of transistors $M_1 - M_5$ makes up the first gain stage, and a common source amplifier consisting of transistors M_7 and M_9 makes up the second gain stage. The output of this error amplifier is at the drains of M_7 and M_9 and is labeled as V_{GD}. Resistors $R_1 - R_6$ form a resistive feedback network and give a gain, A_{EA}, of 75. This error amplifier compares the differentially sensed off-chip output voltage, $V_{OUT}(sensed)$, with the bandgap reference voltage, V_{ref}, and sets

$$V_{GD} = 1.5V - V_{th} - A_{EA}\left(V_{OUT}(sensed) - V_{ref}\right) \tag{4.1}$$

where V_{th} is the threshold voltage of the 1.8V PMOS transistor. The offset voltage V_{th} is set by the diode connection of transistor M_6. As discussed in section 4.10, the bandgap voltage is about 1.17V, and in order to reduce loading on the bandgap reference, resistors R_2 and R_4 are chosen to be $156k\Omega$. Resistors R_1 and R_3 are set to be $200k\Omega$ and resistors R_5 and R_6 are set to be $1.5M\Omega$ in order to give a closed loop gain of 75. Switches S_1 and S_2 are used to turn off the error amplifier during startup. Since maximum drive strength of power-train switches S_1 and S_4 in figure 4.4 is desired during startup, transistor M_9 is turned fully on by switch S_2 of figure4.7 during startup.

The gain-bandwidth product of the DC-DC converter is estimated to be around *300kHz*, and since the closed loop bandwidth of this error amplifier forms the secondary pole of the converter feedback loop, it has to exceed *300kHz* for stability. In simulation, the converter is indeed stable if the error amplifier is made up of an ideal voltage source with an internal pole at *300kHz*. However, since the error amplifier has finite output resistance and has to turn on PMOS switches $S_{1,4,5}$ in figure 3.7 in every clock cycle, it needs time to reach steady state in a small fraction of each clock cycle. This increases the speed requirement of the error amplifier, and thus a higher closed loop bandwidth of *1.5MHz* for the error amplifier is used in this work instead. With a closed loop bandwidth of *1.5MHz* and internal feedback factor of *1/75*, the open-loop gain-bandwidth product of the error amplifier is given by $1.5MHz * 75 = 115MHz$. This requirement sets the design of C_C, M_1, M_2 and the current flow in M_5 in figure 4.7. The secondary pole of the error amplifier, which sets the third pole of the overall converter loop, is approximated by gm_9/C_L due to pole splitting [16], where gm_9 is the transconductance of transistor M_9. Capacitor C_L is the output capacitance of the error amplifier, and this third pole is usually set beyond the open-loop gain-bandwidth product of *115MHz* for stability. However, since the feedback factor of the error amplifier is fixed at *1/75*, this requirement can be relaxed, and this third pole only needs to exceed *1.5MHz*. This third pole is set to be at *3MHz* in this design. Capacitance C_L is given by the gate capacitance of switches $S_{1,4,5}$ in figure 3.7 and the additional decoupling capacitance added on this supply rail. This additional decoupling capacitance is designed to be about the same size as the gate capacitance in this work. Resistor R_z is added to remove the right half plane zero of the compensation scheme. The total current drawn by this error amplifier is about $250\mu A$, and it occupies a die area of $0.015mm^2$. The power drawn by the error

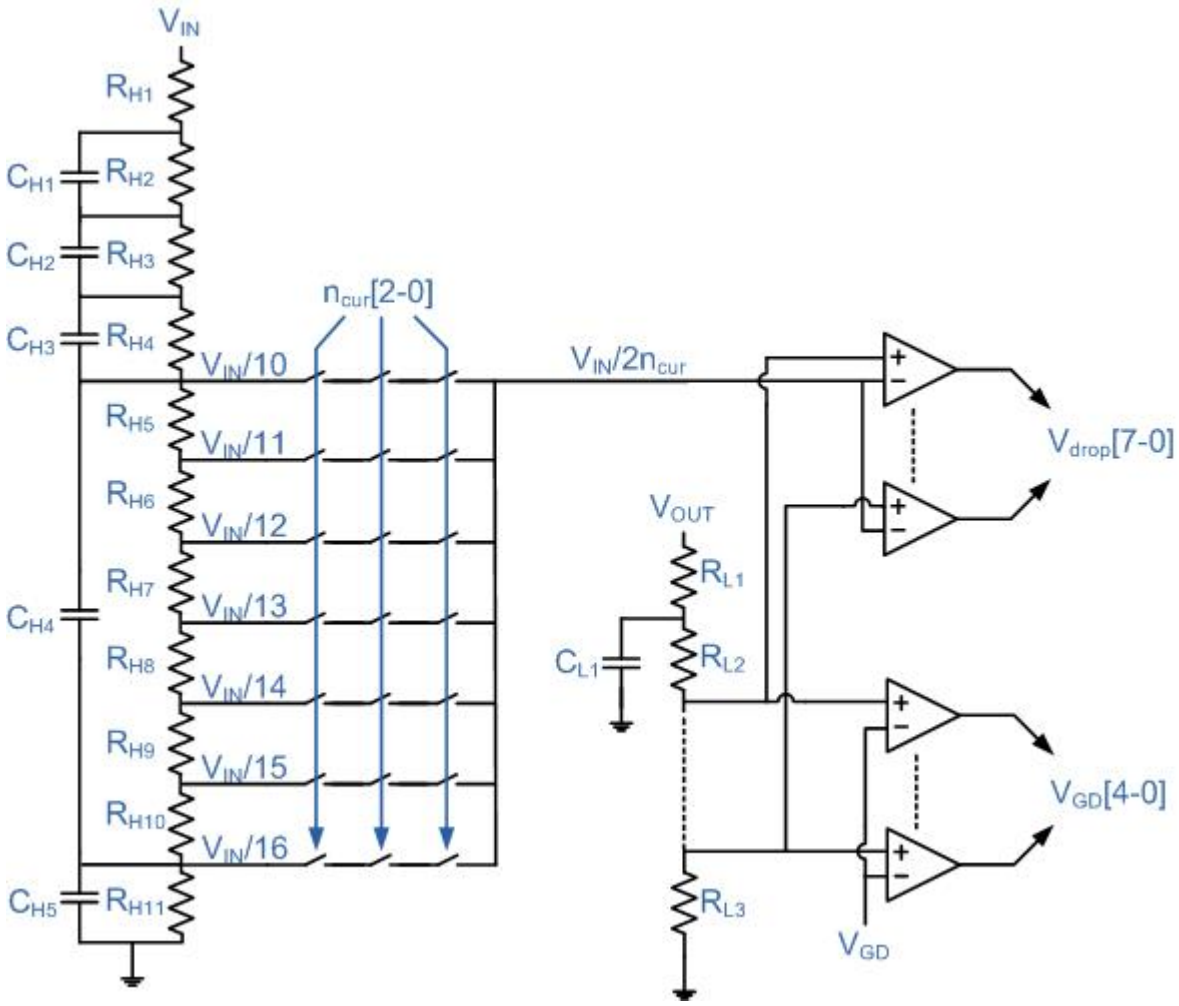


Figure 4.9: Schematic of the analog-to-digital converter

amplifier is thus about $375\mu W$ as the power supply is 1.5V. The error amplifier represents the most significant quiescent power drawn in this regulator.

4.7 Analog to Digital Converter

As discussed in section 3.3, a part of the controller is implemented in the digital domain, and thus an analog-to-digital converter (ADC) is required to convert signals V_{GD} and V_{IN}/n_{cur} in figure 3.7 into the digital domain. Figure 4.9 shows the architecture of the combined ADC implemented in this work. It is a flash ADC consisting of two resistor chains and thirteen comparators. The high voltage resistor chain, consisting of resistors $R_{H1} - R_{H11}$, is used to divide the input voltage by the current converter conversion ratio, n_{cur}, which is represented by a three bit digital signal. The conversion ratio of the converter is from 5 to 8, but the resistor chain divides V_{IN} by 10 to 16 times so that the resulting voltage level is closer to the mid point of the voltage domain (1.5V to ground) that the comparators reside in. Thus the signal obtained is $V_{IN}/2n_{cur}$ instead of V_{IN}/n_{cur}. This signal $V_{IN}/2n_{cur}$ is then compared

with $V_{OUT}/2$ to obtain the various V_{DROP} levels discussed in figure 3.13, where $V_{DROP} = V_{IN}/n_{cur} - V_{OUT}$. Since V_{OUT} is roughly maintained at 1.5V by the analog switch conductance modulation loop at all times, the various V_{DROP} values are obtained by comparing the signal $V_{IN}/2n_{cur}$ with a divided value of V_{OUT}. For example, to determine whether $V_{DROP} > 0.3V$, $V_{IN}/2n_{cur}$ should be compared with $V_{OUT}/2 + 0.15V$, but with $V_{OUT} \sim 1.5V$, it is instead being compared with $V_{OUT}/2 + V_{OUT}/10 = 6V_{OUT}/10$ for simplicity. The required set of divided values of V_{OUT} are obtained by the low voltage resistor chain, consisting of resistors $R_{L1} - R_{L3}$. Discrepancies in this comparison can be mitigated by increasing the margins, or the hysteresis area, in the outer loop $G - V_{DROP}$ map as discussed in subsection 3.3.3. This is not a big concern because this additional margin is negligible when compared to the hysteresis area introduced when the efficiency boundary is approximated by the two straight lines. Another signal that needs to be converted to the digital domain is V_{GD}. Gate drive voltage V_{GD} is also compared to a divided value of V_{OUT} for simplicity.

In figure 4.9, capacitors $C_{H1} - C_{H5}$ are added to compensate the resistive divider. However, a capacitor parallel to R_{H1} is omitted to introduce low pass filtering of high frequency noise at V_{IN}. For similar reasons, capacitor C_{L1} is added to the low voltage resistor chain to low pass filter the high frequency noise at V_{OUT}. The high voltage resistor chain is designed to be $12M\Omega$, and the low voltage resistor chain is designed to be $1.5M\Omega$. Each of the two resistor chains draws about $1\mu A$ of current, depending on V_{IN}, and make up most of the die area of the ADC. The total area of the ADC is about $0.1mm^2$. The power consumption of the ADC is dominated by the comparators, and will be discussed in the next section.

4.8 Comparators

Figure 4.10 shows the comparator design used in the ADC. Transistors $M_3 - M_6$ forms a cross-coupled latch, whereas transistors $M_1 - M_2$ form a differential pair to drive the latch. The differential pair is connected to the output of the latch instead of the bottom supply of the latch to maximize headroom of this comparator. This comparator is clocked at the same frequency as the digital controller. The comparator resets when Clk_{IN} is high, and operates when Clk_{IN} is low. The configuration of switches $S_1 - S_7$ in reset mode is shown in table 4.1. When Clk_{IN} goes low, the comparator goes into active mode, and starts to evaluate whether $V_i+ > V_i-$. The configuration of switches $S_1 - S_7$ in active mode is also shown in table 4.1. Current source I_{ref2} is added to limit the current flowing in the latch during active mode, so that the differential pair can easily over-power the latch. This ensures that the offset of the comparator is dominated by the mismatch of the input transistors $M_{1,2}$ instead of that of the latch transistors. Current source I_{ref1} is designed to sink $8\mu A$, whereas I_{ref2} is designed to sink $0.8\mu A$. After the comparator has finished its evaluation, the differential pair is turned off to reduce power consumption. The comparator goes into retain mode, and the switch configuration during this mode is also shown in table 4.1. Although current source I_{ref2} is not turned off, current flow in the latch is negligible since it is set by leakage current through transistors $M_3 - M_6$. Whether the comparator has finished its evaluation is determined by either V_O+ or V_O- attaining a low signal. An S-R latch, driven by V_O+ and V_O-, is designed for this purpose, but is not shown in figure 4.10 for simplicity. Capacitors C_1 and C_2 are included to minimize voltage swings within the comparator from coupling back

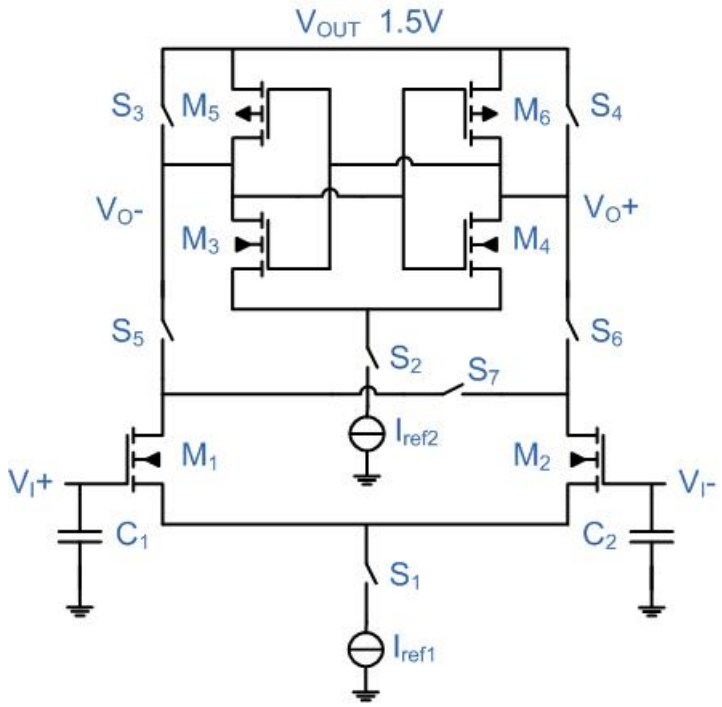


Figure 4.10: Schematic of the comparator used in figure 4.9

	when	S_1	S_2	S_3	S_4	S_5	S_6	S_7
Reset mode	$Clk_{IN} = 1$	Off	Off	*On*	*On*	Off	Off	*On*
Active mode	$Clk_{IN} = 0$ && $done = 0$	*On*	*On*	Off	Off	*On*	*On*	Off
Retain mode	$Clk_{IN} = 0$ && $done = 1$	Off	*On*	Off	Off	Off	Off	Off

Table 4.1: Switch configurations at different modes of the comparator

into the inputs. This is necessary since the inputs are each connected to one of the two high resistance resistor chains, as discussed in section 4.7. Simulation shows that the 3σ offset of this comparator is about $50mV$ when the input common mode voltage is at $1.2V$, and is about $10mV$ when the input common voltage is at $0.55V$. The offset of the comparator is higher at higher common mode voltages due to a reduction in differential pair gain as it goes into triode operation. As discussed in section 4.7, there are multiple comparators spanning a wide range of voltage levels. For some of these comparators, source followers are added to levelshift the input signals so that the input common mode voltage is between 0.55V and 1.2V.

There are 13 comparators in total in the ADC, and they dominate the power consumption of the ADC. Total power consumption of the ADC is dependent on V_{IN}, n_{cur} and V_{GD} since the comparators turn off after a comparison is made, and the speed of the comparison is dependent on the input voltage levels. Simulation shows that the ADC, including the resistive dividers, consumes about $35\mu A$ of current in most cases, or equivalently, $52.5\mu W$ of power.

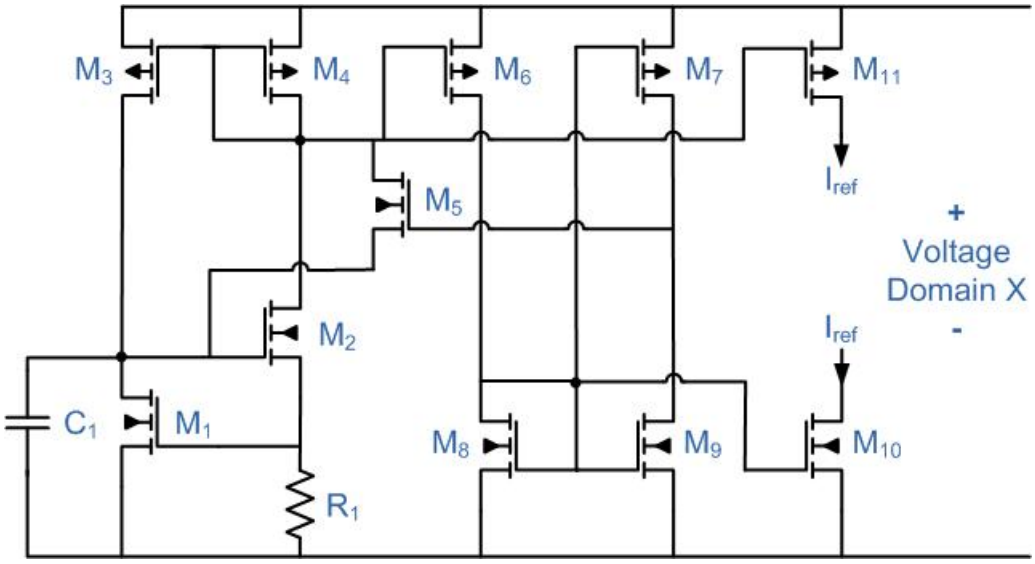


Figure 4.11: Schematic of the current reference installed in all voltage domains

4.9 Current reference

Many circuits discussed in this chapter require reference currents, and in particular, the over-voltage protection clamp present in each floating voltage domain, as discussed in section 4.2. Since this current reference is mostly used for supplying the tail current of differential pairs, it does not need to be highly accurate. On the other hand, it is implemented in each voltage domain, so it needs to draw minimal current. This work chooses a design that trades off accuracy for power consumption. Figure 4.11 shows the schematic of the current reference that is installed in each voltage domain [16]. Transistors M_1 to M_4 form a feedback loop that is the core of the current reference, and capacitor C_1 is installed to stabilize the loop. This design is called a threshold reference because it sets the current by approximately setting the threshold voltage of transistor M_1 across resistor R_1. Transistors M_5 to M_9 are installed to kick start the current reference during startup. Transistor M_7 is on even after startup, and thus it is designed to have a long gate length to minimize power consumption. Resistor R_1 is designed to be $2.5M\Omega$. The current reference is designed to draw about $300nA$ each. The total area of all the current reference is about $0.15mm^2$ and the total power consumption is about $9\mu W$.

4.10 Voltage reference

While the reference current in this work need not be accurate, the reference voltage needs to be accurate because its accuracy directly couples into that of the regulation scheme. This work chooses a bandgap reference design [30] for the voltage reference, and its schematic is shown in figure 4.12. A bandgap reference attains nominally zero temperature coefficient by adding a proportional to absolute temperature (PTAT) term to a complementary to absolute temperature (CTAT) term. In this circuit, the CTAT term comes from the V_{BE} of bipolar junction transistors (BJT) Q_3, and the PTAT term comes from flowing a PTAT current

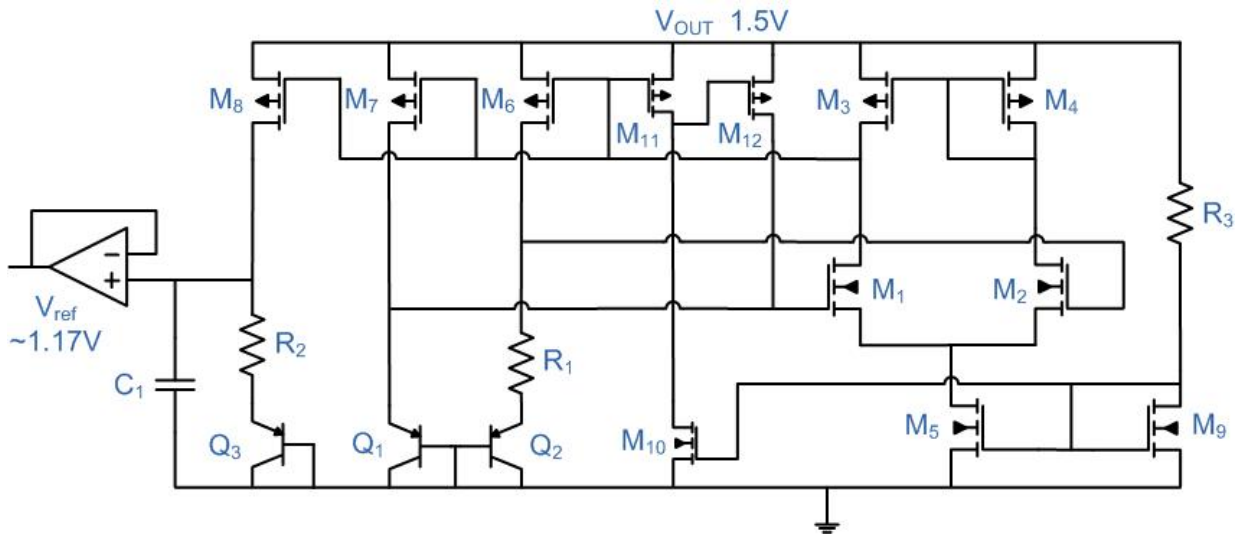


Figure 4.12: Schematic of the bandgap voltage reference

through resistor R_2. The current is PTAT since it is forced by the differential amplifier, consisting of transistors M_1 to M_5, to be $\triangle V_{BE}/R_1$. The term $\triangle V_{BE}$ is the difference between the V_{BE} of BJT Q_1 and Q_2. The two V_{BE} are different because Q_2 is eight times the size of Q_1 while the current through it is eight times smaller by sizing transistor M_7 to be eight times smaller than transistor M_6. Capacitor C_1 is added to reduce fluctuations in the reference voltage due to noise and interferences. A unity gain buffer, consisting of a simple five transistor differential pair, is added to reduce loading on the reference generator. The resulting reference voltage is about 1.17V, and has a temperature coefficient of $\sim 100\mu V/^oC$ in simulation. Transistors $M_{10} - M_{12}$ are added for startup purposes, and resistor R_3 is used to set the bias current in the differential amplifier. The whole bandgap reference is designed to consume about $40\mu A$ of current or $60\mu W$ of power, and occupy $0.025mm^2$ of die area.

4.11 Ringing protection scheme

When the switched capacitor converter changes clock phase, power switches are turned off and on. If there is still current flowing in the power switches at the end of a clock phase, the current is abruptly cut off. Since the power-train capacitors in this work are off-chip capacitors, this current flows through a path with non-negligible parasitic inductance, and thus ringing occurs in the switching nodes as a result. As discussed in section 2.2, these switching nodes define the voltage domains, and thus ringing in the switching nodes can cause significant voltage fluctuations in the voltage domains. Simulation shows that the voltage levels can fluctuate by $\pm 3V$ for a nominal 3V voltage domain. The voltage fluctuation is most significant during the deadtime in which all switches are off. Such large voltage fluctuations not only stress the devices, but can also cause errors in operation. On-chip decoupling capacitors are installed to reduce the effect of the ringing, but significant ringing will still occur unless the die area is increased by more than four times just for adequate decoupling capacitors. To reduce ringing without significantly increasing die area, helper

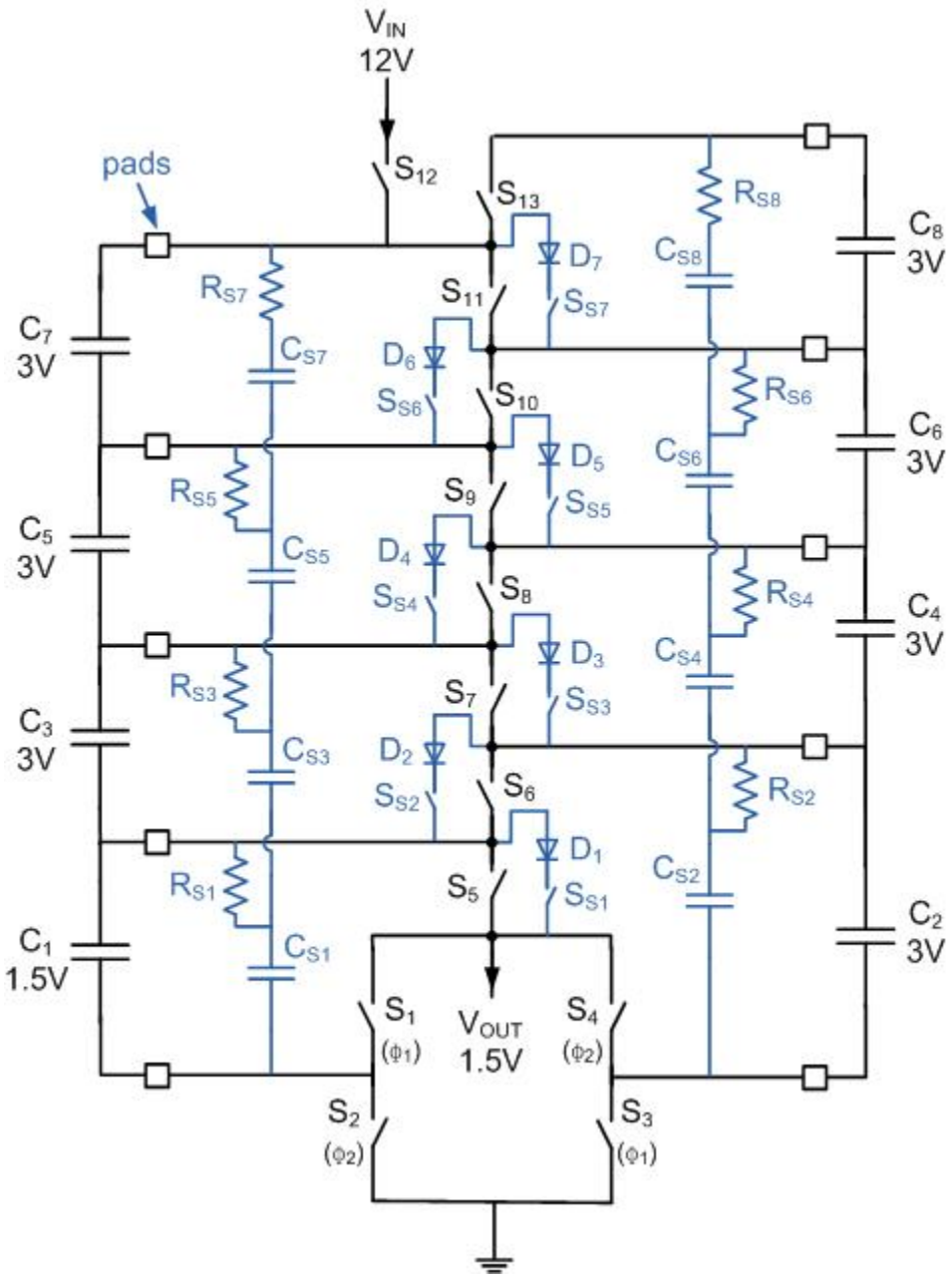


Figure 4.13: Schematic of the helper circuits to reduce effects of ringing

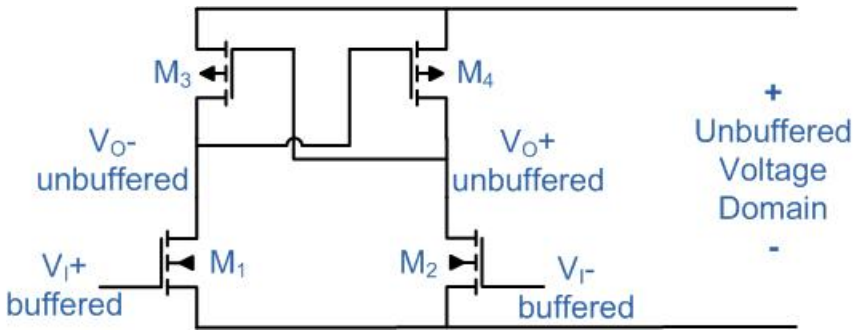


Figure 4.14: Interface circuit between buffered voltage domain and unfiltered voltage domain

circuits are implemented in this work, as shown in figure 4.13.

One way to reduce the ringing amplitude is to decrease the current gradually instead of abruptly. Auxiliary switches S_{S1} to S_{S7} are installed to provide an alternative path for the current to flow when power switches S_1 to S_{13} are turned off. Diodes D_1 to D_7 are installed so that there is a voltage drop when there is current flowing in this alternative path. This voltage drop helps to decrease the current quickly, and also allows a convenient way to detect current flow. These diodes are implemented with diode connected MOSFET transistors. The auxiliary switches are turned off when the voltage drop across the diode connected transistor drops below the threshold voltage, which indicates that the current has dropped to zero. As a safety precaution, the auxiliary switches are turned off immediately at the end of the deadtime. With the auxiliary switches, simulation shows that the voltage fluctuation in the voltage domains reduces to $\pm 1V$ for a nominally 3V voltage domain without decoupling capacitors. Although this is still a significant voltage fluctuation, the fluctuation now no longer causes the buffers driving the main switches to turn on accidentally. These auxiliary switches take up about $0.3mm^2$ of die area but consume negligible power. The energy stored in the parasitic inductance are burned off in this scheme, but with inductance in the nH range, the energy stored is negligible even when the converter is running with full load. The energy stored in the inductance is reduced at light load because current flowing among power-train capacitors is also reduced.

Even with the auxiliary switches, the voltage fluctuation is still too high for the levelshifter circuits and protective clamps present in each voltage domain. To ensure correct operation filtered supply rails, consisting of capacitors $C_{S1} - C_{S8}$ and resistors $R_{S1} - R_{S8}$, are used to supply power for these sensitive circuits. The drivers for the main switches are, however, not supplied by this buffered rail because they need to be referenced to the sources of the switches, which are connected to the unfiltered rail. Capacitors $C_{S1} - C_{S8}$ are about $5pF$ each and resistors $R_{S1} - R_{S8}$ are about $3k\Omega$ each. Simulation results show that the voltage fluctuation in the buffered supply rail varies by about $\pm 0.15V$ for a nominally 3V voltage domain. To ensure correct signal propagation between the buffered rail and unfiltered rail, interface circuits [29] shown in figure 4.14 are installed. Figure 4.15 shows the main circuit blocks in each buffered and unfiltered voltage domain. Auxiliary switches S_{S1-S7} and diodes D_{1-7} in figure 4.13 are in the unfiltered voltage domain but are not shown in figure 4.15.

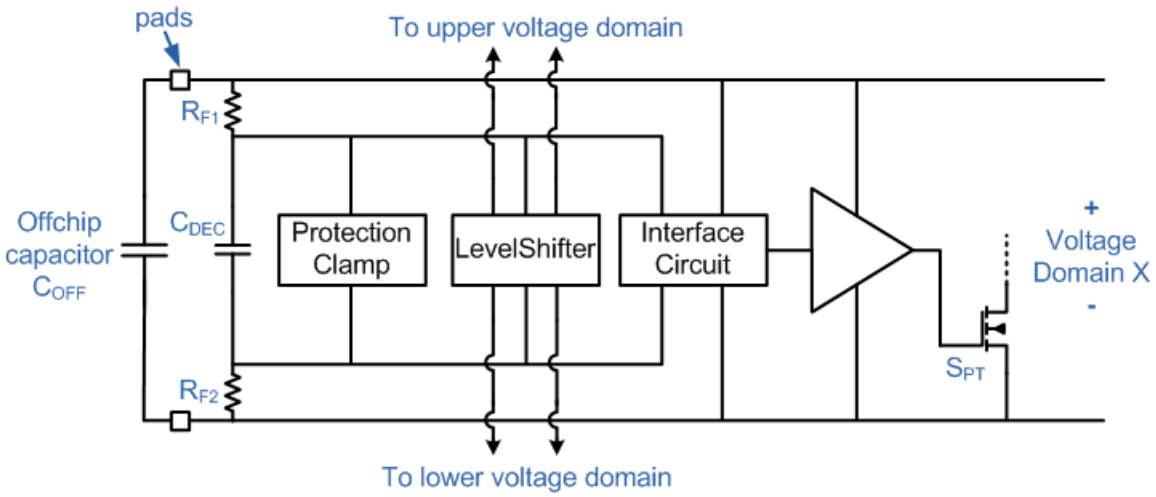


Figure 4.15: Schematic showing the main circuits in each unfiltered and buffered voltage domain

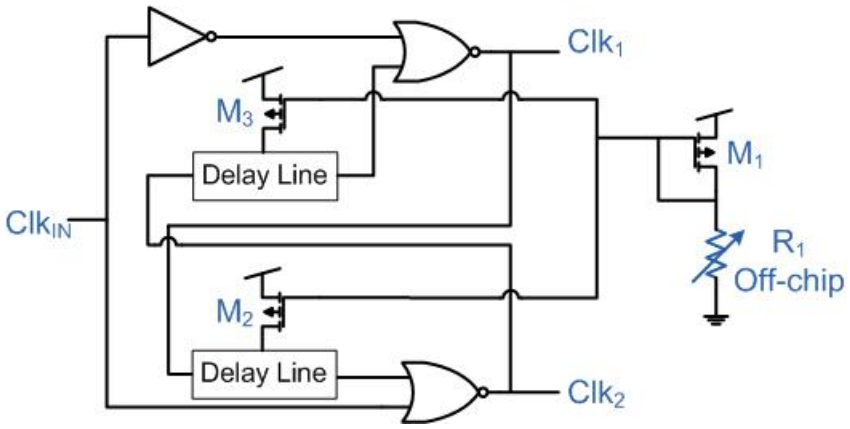


Figure 4.16: Schematic of the two phase non-overlapping clock generator

4.12 Non overlapping clock generator

The two phase clock signal in this converter is designed to be non-overlapping to avoid shorting out any power-train capacitors. In the first few implementations in test chips 1 and 2, the non-overlapping clock signal is generated by the analog circuit [29] shown in figure 4.16. The amount of deadtime is controlled by the tunable off-chip resistor R_1. The on-chip implementation of this clock generator is only $0.00045mm^2$, and the power consumption is also negligible. In the final test chip, the two-phase clock is generated by the digital controller, as discussed in subsection 3.3.2. The amount of deadtime is designed to be one clock period, $20ns$, of the digital $50MHz$ clock.

This $50MHz$ clock is generator on-chip with the circuit shown in figure 4.17. When the signal *In* is connected to ground, the circuit will free-run and generate a square wave with frequency determined by the RC time constant of the low pass filter and the hysteresis band of the Schmidt trigger. The nominal free-running frequency is $50MHz$ but can vary by up

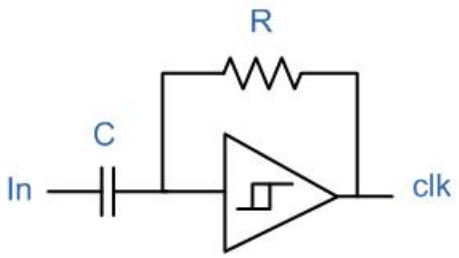


Figure 4.17: Schematic of the 50MHz clock generator

to 40% due to process corners. This clock signal can be overridden by driving the signal *In* with an external clock as long as the external clock has a frequency higher than *~1/5* of the free-running frequency. This circuit takes up about $0.0007mm^2$ of die area and consumes about $20\mu A$ of current or $30\mu W$ of power.

4.13 Digital circuits

The digital controller in this work is generated by digital synthesis of a verilog code. The synthesized digital circuit is about $0.01mm^2$ in die area and consumes about $150\mu W$ of power with the $50MHz$ digital clock. The digital circuits are designed to work up to a clock frequency of $100MHz$ to accommodate fluctuations in clock frequencies. The verilog code used to generate the controller is shown in the Appendix.

Chapter 5

Experimental Results

Experimental work was carried out with four test chips, each built in a $0.18\mu m/0.6\mu m$ process. This chapter discusses each test chip separately and points to the differences among them. While the final test chip is the most complete and robust of all, the earlier versions show better efficiencies since fewer efficiency compromising functions are implemented. Reading about all test chips can give the reader insights into how trade-offs are made, and how the expected performance could be improved if certain auxiliary functions were omitted. The interested reader is encouraged to read the whole chapter, but others may decide to focus on the final test chip only; in section 5.4. Discussions in the previous chapters have been mainly focused on the final test chip.

5.1 First test chip

The first test chip focused on the implementation of the power-train and realization of various voltage domains. None of the protection circuits, startup circuits nor regulation scheme was implemented in this test chip. Figure 5.1 shows the schematic of the converter in this design. In this design, the converter has a fixed conversion ratio of 8-to-1 and is powered from a fixed 12V power supply. The star capacitor configuration, instead of the ladder configuration, was used in test because regulation was not seriously considered yet, and the star configuration gives a lower R_{SSL}, as discussed in section 2.1. In the absence of startup circuits, the converter was initiated carefully using an external resistor chain to get all voltage domains to the designed voltage levels. Switches $S_1 - S_{12}$ are power-train switches, and they are all implemented with NMOS transistors for maximum carrier mobility. The arrows next to the switches indicate which driver blocks drive the switches. Capacitors $C_1 - C_7$ are the power-train capacitors, whereas capacitors $C_8 - C_{10}$ are decoupling capacitors added to provide gate-drive to power-train switches S_{11}, S_{12} and S_4 respectively. All capacitors are implemented with off-chip ceramic capacitors, and their values are given in table 5.1. Capacitor sizes and switch sizes are chosen based on the optimization scheme discussed in subsections 1.1.1 and 1.1.2. Table 5.1 also shows the estimated contribution of different components to R_{FSL}, and the design and estimated (from measured data) values of R_{SSL}, R_{FSL}, frequency-dependent switching loss, and fixed loss. As shown in Table 5.1, power loss at 1A load is dominated by conduction loss of bond-wire and on-chip metal resistances,

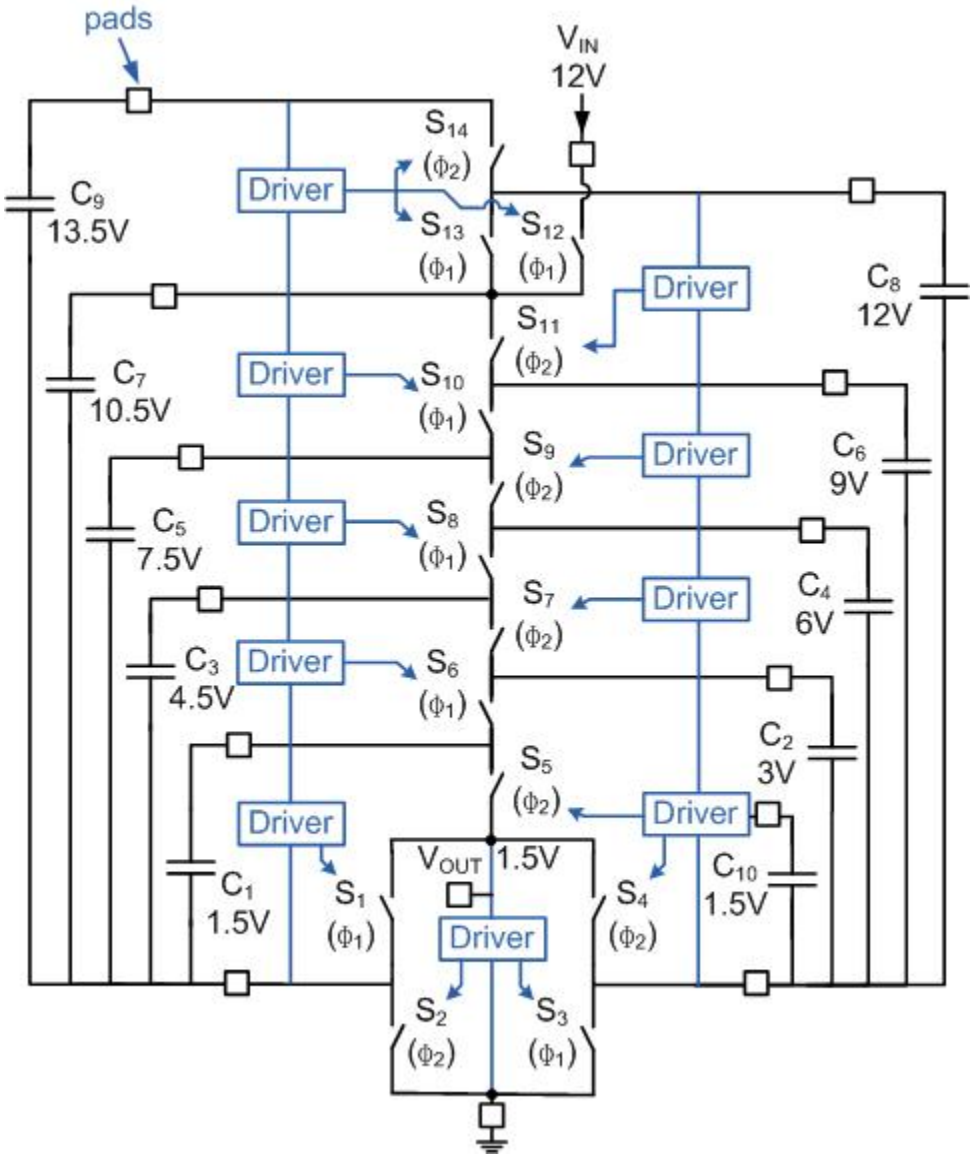


Figure 5.1: Schematic of the overall circuit in the first version of implementation

	Design	Estimation
Capacitor and switch sizes		
C_1, C_2, C_{10}	$2.2\mu F$	
C_3, C_4	$1\mu F$	
C_5, C_6	$0.68\mu F$	
C_7, C_8, C_9	$0.47\mu F$	
1.5V switches $S_1 - S_4$	$75mm$	
3V switch $S_5 - S_{12}$	$16mm$	
Contribution to R_{FSL}		
All switches	$64m\Omega$	
On-chip metal	$48m\Omega$	
Capacitor R_{ESR}	$18m\Omega$	
Bond-wire resistance	$200m\Omega$	
Socket resistance	$81m\Omega$	
Aggregate numbers		
R_{FSL}	$411m\Omega$	$505m\Omega$
R_{SSL}@$1MHz$	$125m\Omega$	$219m\Omega$
R_{OUT}@$1MHz$	$430m\Omega$	$550m\Omega$
Fixed Loss	$20\mu W$	$19\mu W$
Freq-dep Loss @1MHz	$7.45mW$	$7.7mW$

Table 5.1: The components used in the first test chip, and the different contributors to power loss.

rather than conduction loss due to on-chip MOS channel or power-switch gate-drive loss.

Figure 5.2 shows a die photo of the silicon implemented in this version, and table 5.2 shows the area of the constituent components in the layout. As evident in the photo, all switches are located at the periphery of the die to minimize the on-chip metal resistances, which contributes significantly to the conduction loss as shown in Table 5.1. Bond pads are designed to allow double bonding of 1 mil gold wire on each pad to minimize bond-wire resistances and inductance. Multiple bond pads are placed in parallel for each 1.5V switch terminal, which sees the biggest impact from parasitic resistance. These design considerations result in significant empty space in the middle of the die, which can otherwise be eliminated with a different packaging scheme. Figure 5.3 shows the measured efficiency of this chip at four different switching frequencies. Figure 5.3 also shows the best fit curve to the efficiency measurements by assuming power loss is given by equation 5.1 and extracting the four loss terms R_{SSL}, R_{FSL}, SW_{Loss} and $Fixed_{Loss}$.

$$Power_{Loss} = I_{out}^2 \left(R_{FSL} + \frac{R_{SSL@1Hz}}{Freq} \right) + SW_{Loss} Freq + Fixed_{Loss} \tag{5.1}$$

Efficiencies of the converter at 14 different switching frequencies were measured and used to fit the curve, but only four switching frequencies are shown in the figure for simplicity. The design values and extracted values of the four loss terms are shown in table 5.1. The extracted values are very close to the design values with the exception of R_{SSL}. This difference is likely

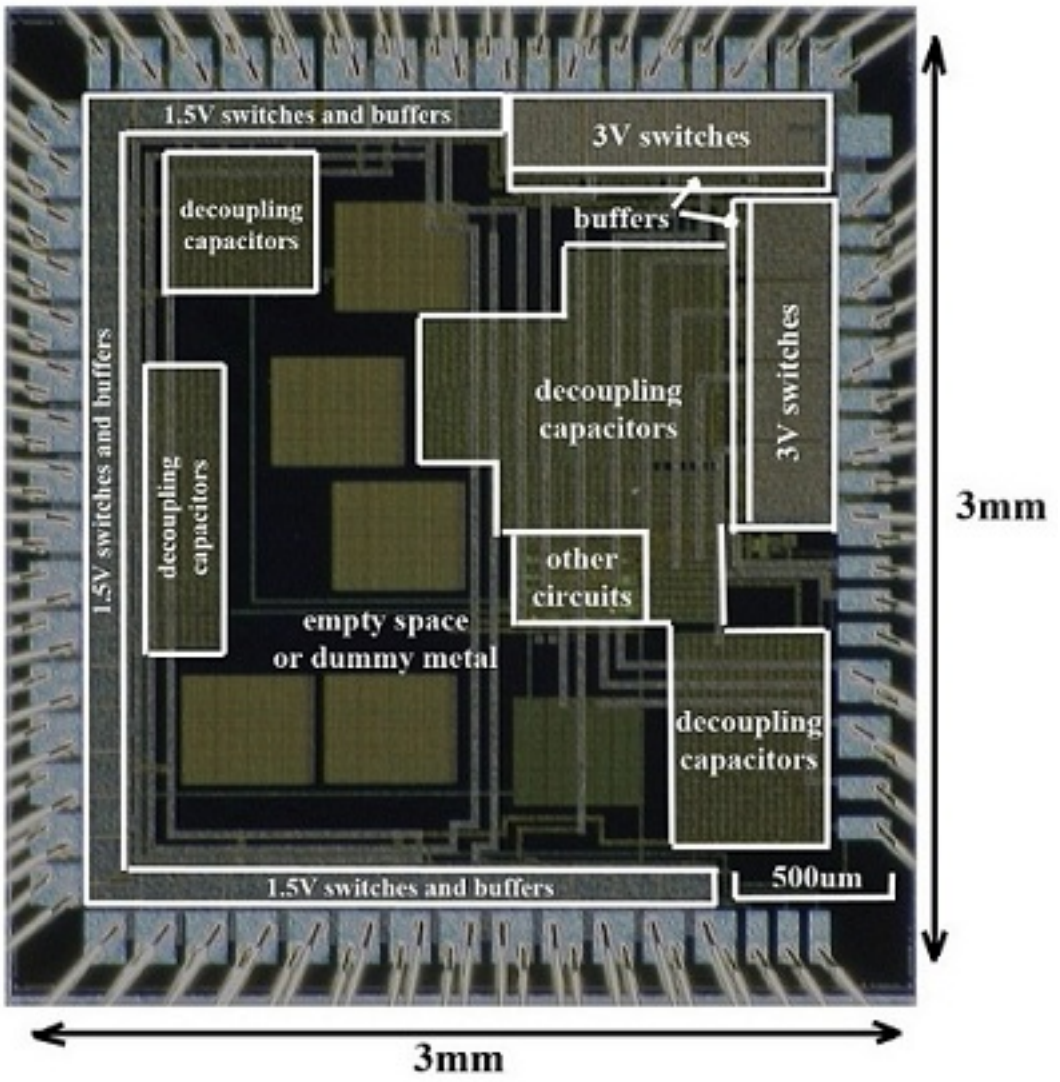


Figure 5.2: Die photo of the first test chip

	Area in layout
3V switches	$0.57mm^2$
3V switch drivers	$0.1mm^2$
1.5V switches	$0.5mm^2$
1.5V switch drivers	$0.06mm^2$
Other circuits	$0.13mm^2$
Decoupling capacitors	$1.56mm^2$
Total active area	$3mm^2$
Total area excluding pads	$6.7mm^2$
Total area including pads	$9mm^2$

Table 5.2: Area of constituent components in die layout for the first test chip

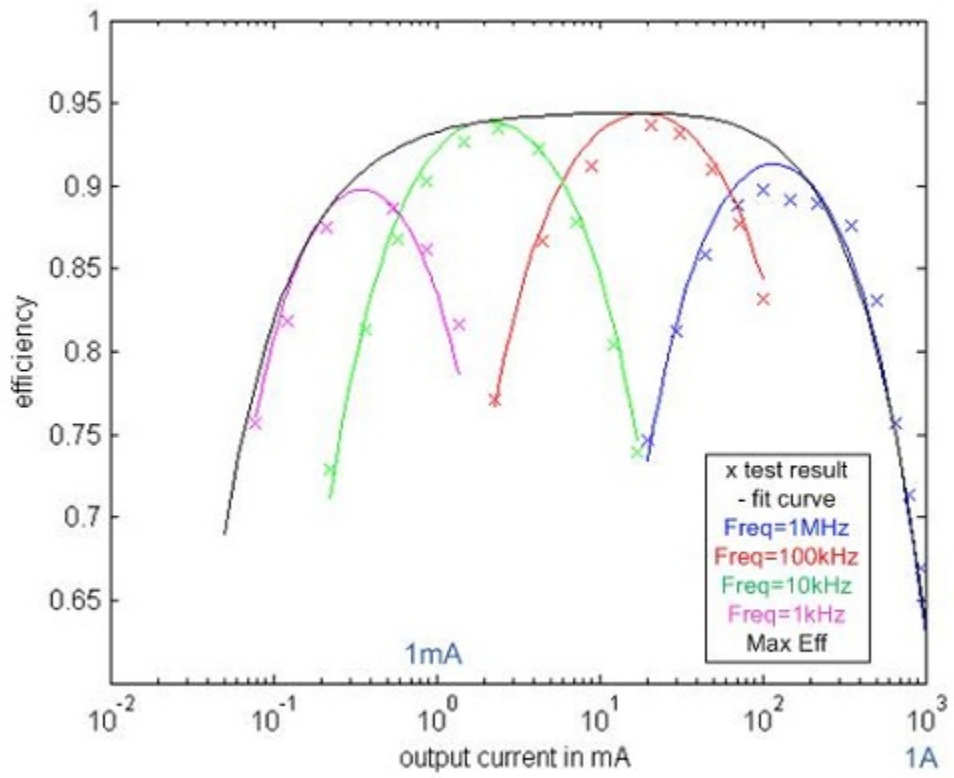


Figure 5.3: Efficiency test result and best fit efficiency curves for the first test chip

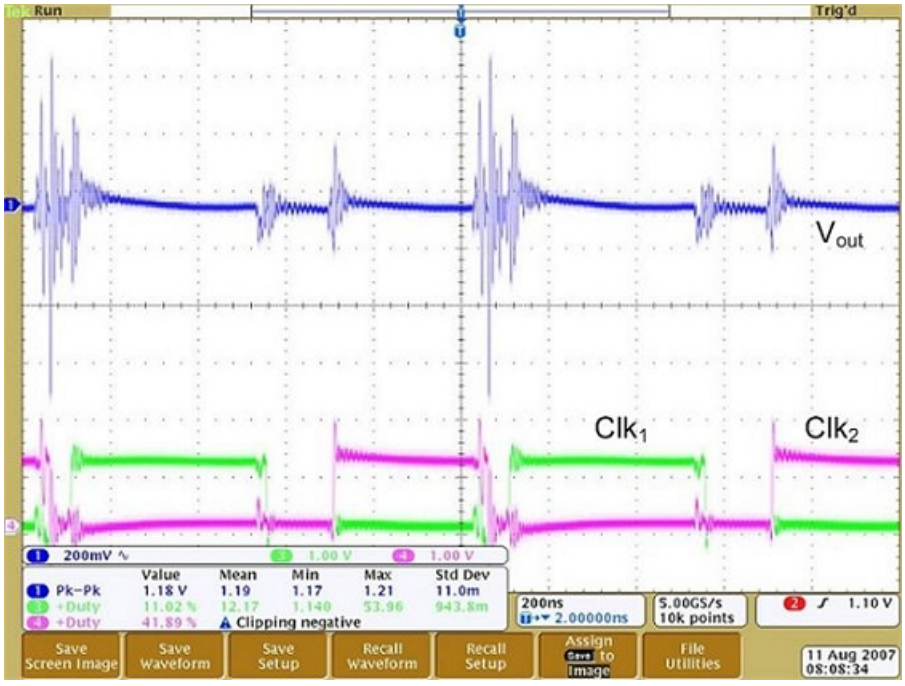


Figure 5.4: Oscilloscope shot of the first test chip at 1A load and 1MHz switching frequency. The top curve shows the output voltage with 200mV/div, whereas the bottom curves show the two phase clock signals with 1V/div. The time scale of the plot is 200ns/div.

	Area in layout
3V switches	$0.57mm^2$
3V switch drivers	$0.1mm^2$
1.5V switches	$0.5mm^2$
1.5V switch drivers	$0.06mm^2$
Other circuits	$0.25mm^2$
Decoupling capacitors	$1.56mm^2$
Total active area	$3mm^2$
Total area excluding pads	$6.7mm^2$
Total area including pads	$9mm^2$

Table 5.3: Area of various components in die layout for the second test chip

due to effective capacitance of ceramic capacitance being considerably smaller than stated values when a voltage bias is present. Figure 5.3 also shows the highest efficiency over a range of output current levels if switching frequency is optimized by equation 2.1. The converter achieves a very high efficiency over a very wide range of output current levels. Figure 5.4 shows an oscilloscope shot of the output voltage when the converter is operating at 1A load current with a switching frequency of 1MHz. The oscilloscope plot shows the two phase clock signal with a significant deadtime in between. This deadtime of about 180ns was required because the levelshifter circuit used was a design[31] that works considerably slower than the one discussed in section 4.1. The result and design of this test chip has been discussed in the master thesis [32], but the test data has since been refined, as reported here.

5.2 Second test chip

The second test chip focused on making the converter more robust. The levelshifter circuit was improved, and protection circuits and startup circuits were added. Figure 5.5 shows the die photo of this version of this test chip, and table 5.3 shows the sizes of the layout components. The die layout is basically the same as in the first implementation, with the exception that the "other circuit" block is larger. Figure 5.6 shows the measured efficiency of the chip at two different switching frequencies and the respective best-fit curves. Efficiencies of the converter at seven different switching frequencies were measured and used to fit the curve, but only two switching frequencies are shown in the figure for simplicity. The design values and extracted values of the four loss terms are shown in table 5.4. Figure 5.7 shows an oscilloscope shot of the output voltage and the two phase clock signal at 230mA load current with a switching frequency of 1MHz. Figure 5.8 shows the voltage levels on four power-train capacitors during startup.

When compared with the first test chip results, the second test chip sees the biggest improvement in reducing R_{FSL}. This is because with the chip robustness significantly improved, the test socket and the package can be removed. The chip is directly bonded onto the printed circuit board (PCB), and this allows a reduction in bondwire length and bondwire parasitic resistance. With the improvement to the levelshifter circuits, the deadtime between the two phase clock signals is reduced, as evident in figure 5.7. This allows a reduc-

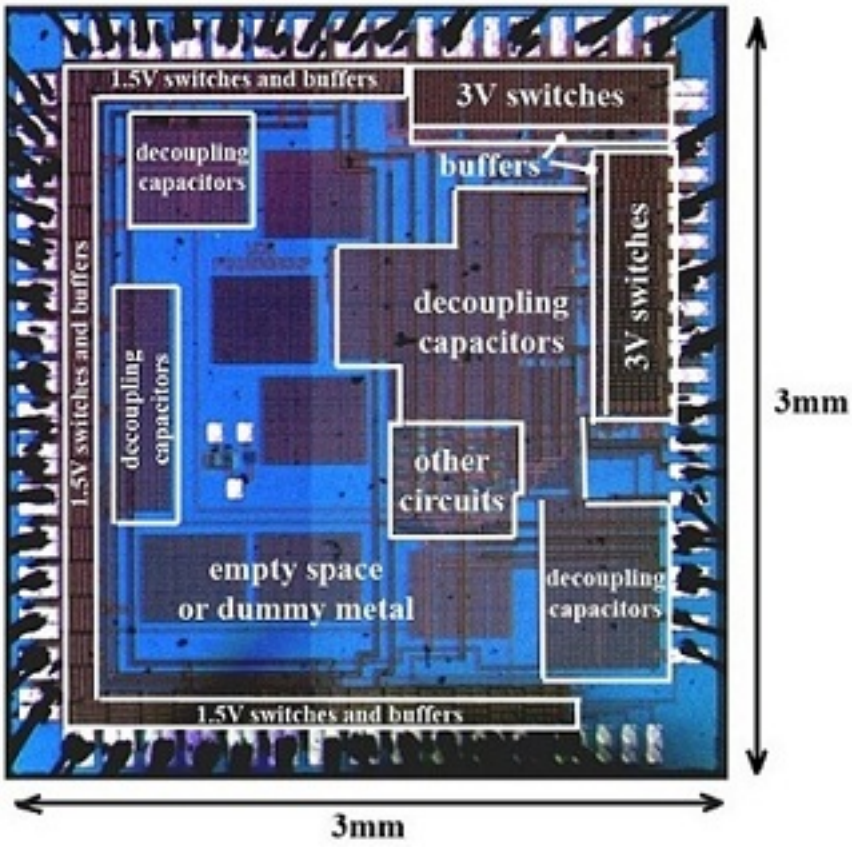


Figure 5.5: Die photo of the second test chip

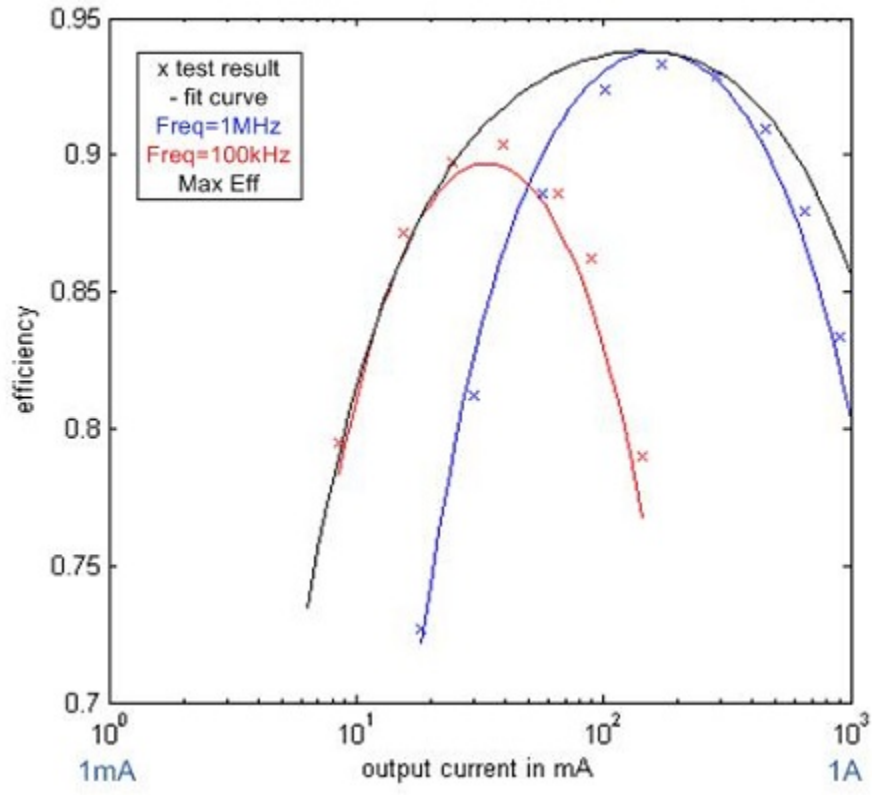


Figure 5.6: Efficiency test result and best fit efficiency curves for the second test chip

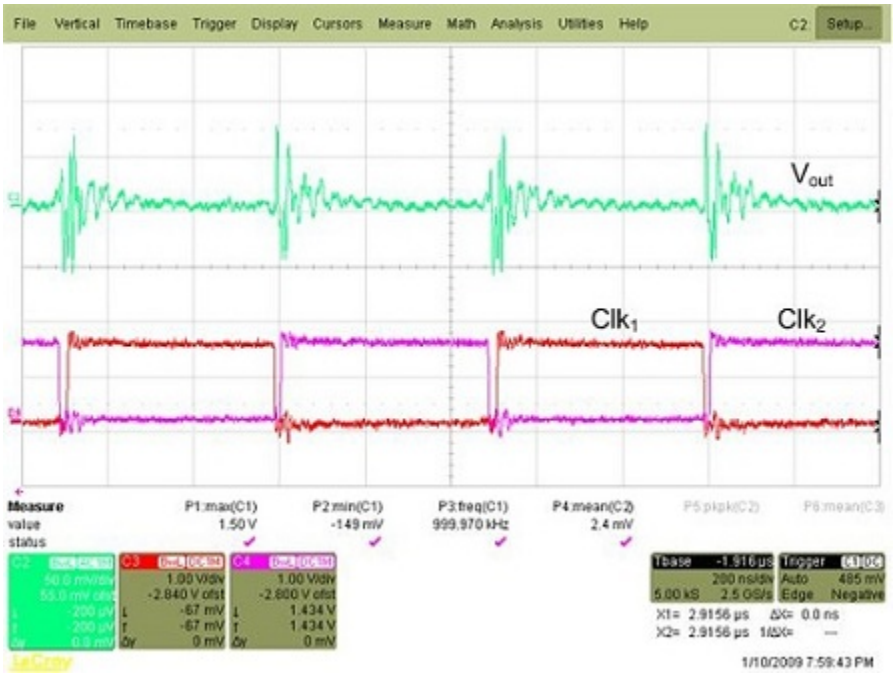


Figure 5.7: Oscilloscope shot of the second test chip at 230mA load and 1MHz switching frequency. The top curve is the output voltage with 50mV/div, whereas the bottom two curves are the two phase clock signal. The time scale is 200ns/div.

	Design	Estimation
Capacitor and switch sizes		
C_1, C_2, C_{10}	$2.2\mu F$	
C_3, C_4	$1\mu F$	
C_5, C_6	$0.68\mu F$	
C_7, C_8, C_9	$0.47\mu F$	
1.5V switches $S_1 - S_4$	$75mm$	
3V switch $S_5 - S_{12}$	$16mm$	
Contribution to R_{FSL}		
All switches	$51m\Omega$	
On-chip metal	$39m\Omega$	
Capacitor R_{ESR}	$15m\Omega$	
Bond-wire resistance	$65m\Omega$	
Aggregate numbers		
R_{FSL}	$170m\Omega$	$175m\Omega$
R_{SSL}@$1MHz$	$125m\Omega$	$228m\Omega$
R_{OUT}@$1MHz$	$210m\Omega$	$287m\Omega$
Fixed Loss	$0.28mW$	$2.1mW$
Freq-dep Loss @1MHz	$7.5mW$	$5.5mW$

Table 5.4: The components used in the second test chip, and the different contributors to power loss.

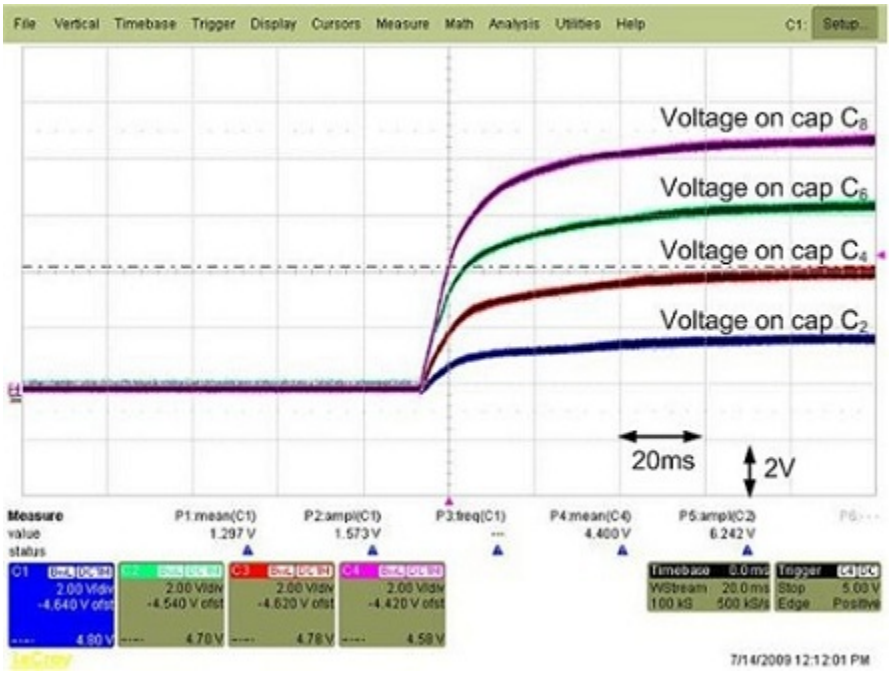


Figure 5.8: Oscilloscope shot of the startup waveform of the second test chip. The four curves shows the voltages on four power-train capacitors with 2V/div. The time scale is 20ms/div.

tion in the contribution of switch resistances, on-chip metal resistances and capacitor ESR to R_{FSL}. This reduction is due to an increase in duty ratio, D_j, in equation 1.6 even though the resistances remain the same.

There are two main design shortcomings in implementation for this test chip. The first one is the protection clamp circuits turned on unexpectedly by capacitive coupling into sensitive nodes as explained in section 4.2. This caused the fixed loss, as shown in table 5.4, to be significantly higher than expected. To solve this problem, capacitor C_1 in figure 4.3 was added to all subsequent implementation versions. Another error in this test chip was in the sizing of the startup helper circuits. The startup helper circuits were sized too small, and this caused the converter to startup in *40ms* instead of a designed value of $200\mu s$. This has also been diagnosed and fixed in subsequent implementations. The results of this implementation have been published in [33] and [34].

5.3 Third test chip

The third test chip focused on reducing power loss, and realization of a multi-conversion-ratio topology. Figure 5.9 shows the schematic of the converter in this test chip. The converter utilized the integer-step multi-conversion-ratio topology discussed in subsection 2.4.1. When compared with previous implementations, some of the power-train transistors were changed from NMOS transistors to PMOS transistors to reduce the number of voltage domains. This results in eliminating capacitors C_9 and C_{10} in figure 5.1 and a reduction in pin-counts. Choice of capacitors were switched from minimizing total ΣCV^2 of the capacitors to using the 0603 ceramic capacitor with highest capacitance, as discussed in subsection 2.3.1. Optimization of switches used the algorithm discussed in subsection 2.3.2, but with multiple conversion ratios, the switch sizes are chosen such that R_{FSL} is similar for the four different conversion ratios. In terms of packaging, flip-chip bonding was used in placed of bondwires to eliminate bondwire resistances and to reduce on-chip metal resistances. These resistances were main contributors to R_{FSL}, and reducing them would allow the converter to attain higher efficiencies and/or operate at higher load current levels.

Table 5.5 shows the components used, and the expected loss factors. Figure 5.10 shows the die photo and table 5.6 shows the area of layout components. By using flipchip packaging, the empty space in previous versions is eliminated, and this allows the converter to attain higher performance with an overall shrink in die size. Figure 5.11 shows the expected efficiency at various switching frequencies at a fixed conversion ratio of 8-to-1. The converter is expected to attain a higher peak efficiency, and also exhibit high efficiency over a wider range of load currents when compared to previous test chips. Unfortunately, the dies were manufactured and diced without being bumped. Numerous attempts were made to package the chip but without success. As a result, the expected results of this chip cannot be verified and the next test chip reverted back to bondwires to avoid repeating this problem. The expected result of this chip has been published in [34].

Although regulation was not implemented in this test chip, it is interesting to investigate the expected efficiency of the converter if the regulation scheme discussed in chapter 3 had been implemented. This will show the change in expected efficiency if having V_{OUT} tightly regulated is more important than converter efficiency, as in the case of most dc-dc converters.

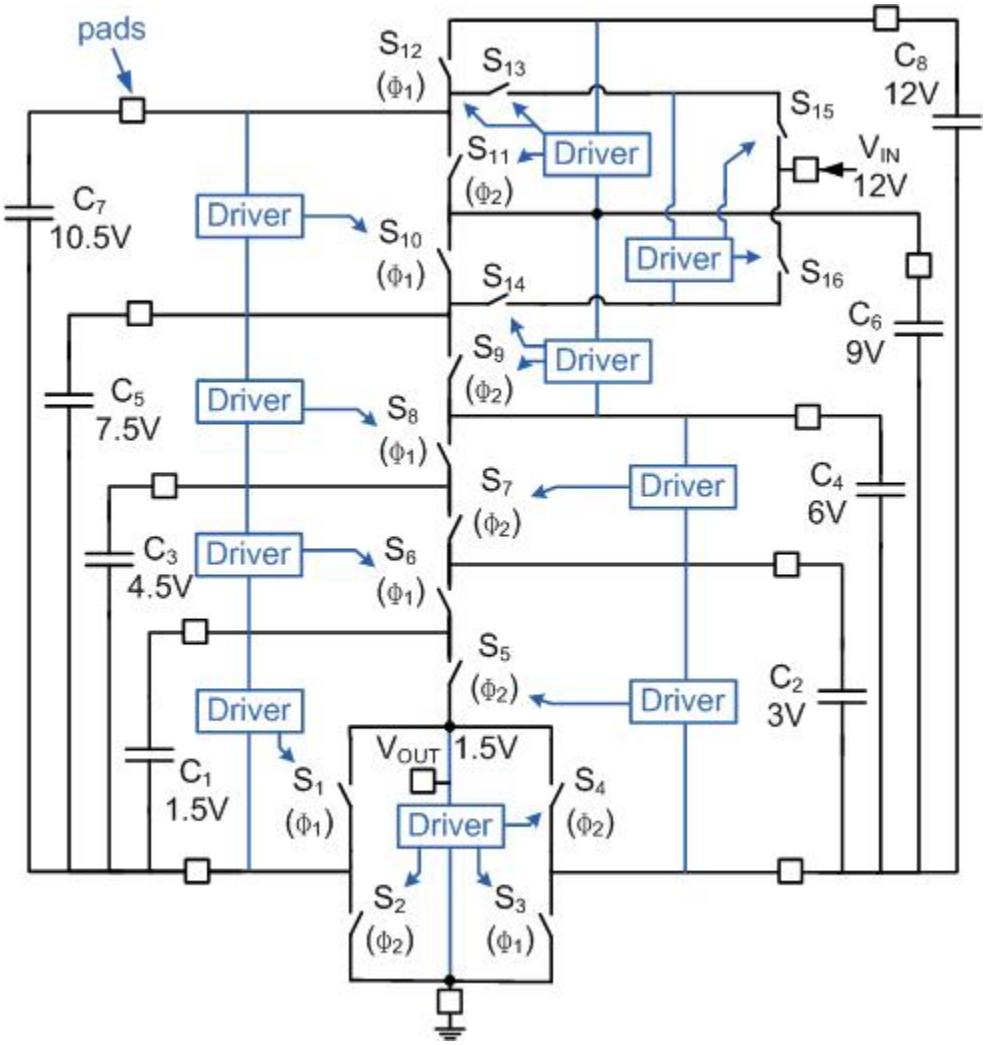


Figure 5.9: Circuit schematic for the third test chip

Capacitor and switch sizes	
C_1, C_2	$10\mu F$
C_3, C_4, C_5, C_6	$4.7\mu F$
C_7, C_8	$2.2\mu F$
1.5V switches $S_1 - S_4$	$200mm$
3V switch $S_5 - S_{12}$	$45mm$
Contribution to R_{FSL}	
All switches	$26m\Omega$
On-chip metal	$36m\Omega$
Capacitor R_{ESR}	$5m\Omega$
PCB trace resistance	$8m\Omega$
Aggregate numbers	
R_{FSL}	$75m\Omega$
R_{SSL}@$1MHz$	$24m\Omega$
R_{OUT}@$1MHz$	$79m\Omega$
Fixed Loss	$60\mu W$
Freq-dep Loss @1MHz	$20mW$

Table 5.5: The components used in the third test chip, and the different contributors to power loss.

	Area in layout
3V switches and drivers	$2.9mm^2$
1.5V switches and drivers	$2mm^2$
Other circuits	$0.8mm^2$
Decoupling capacitors	$2.3mm^2$
Total die area	$8mm^2$

Table 5.6: Area of constituent components in die layout for the third test chip

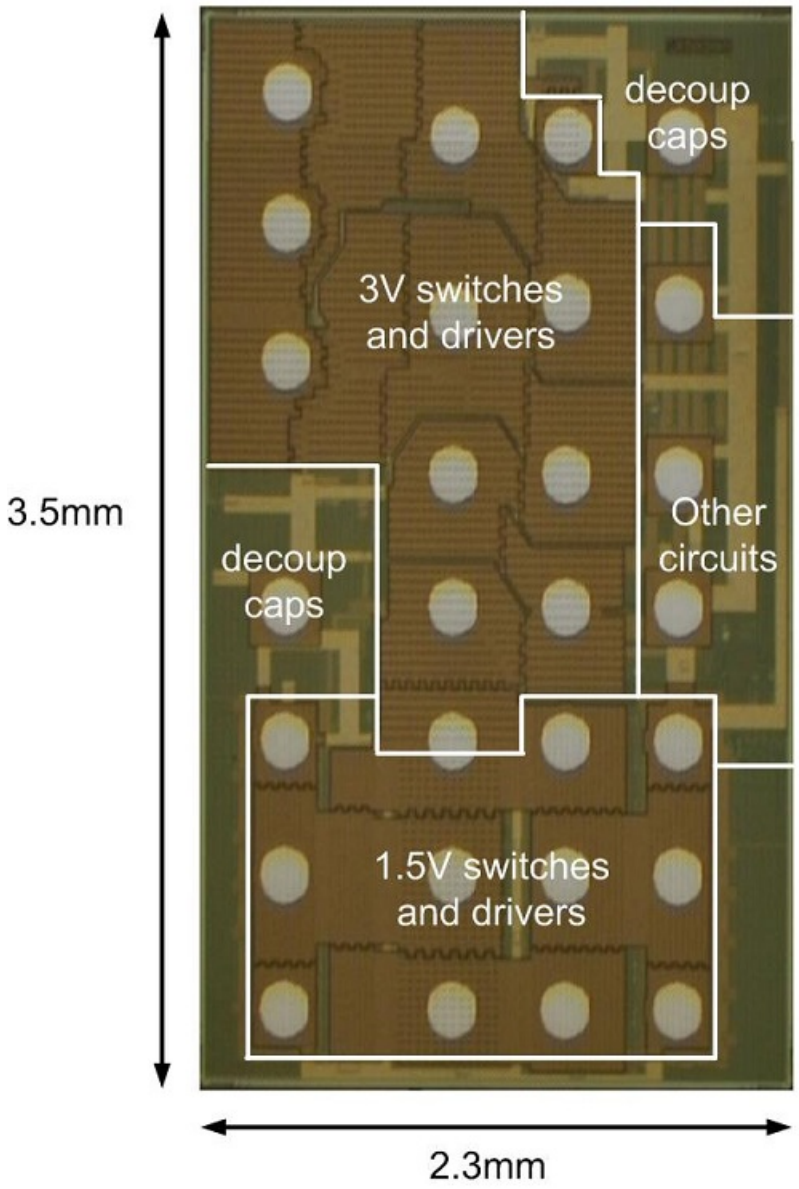


Figure 5.10: Die photo of the third test chip

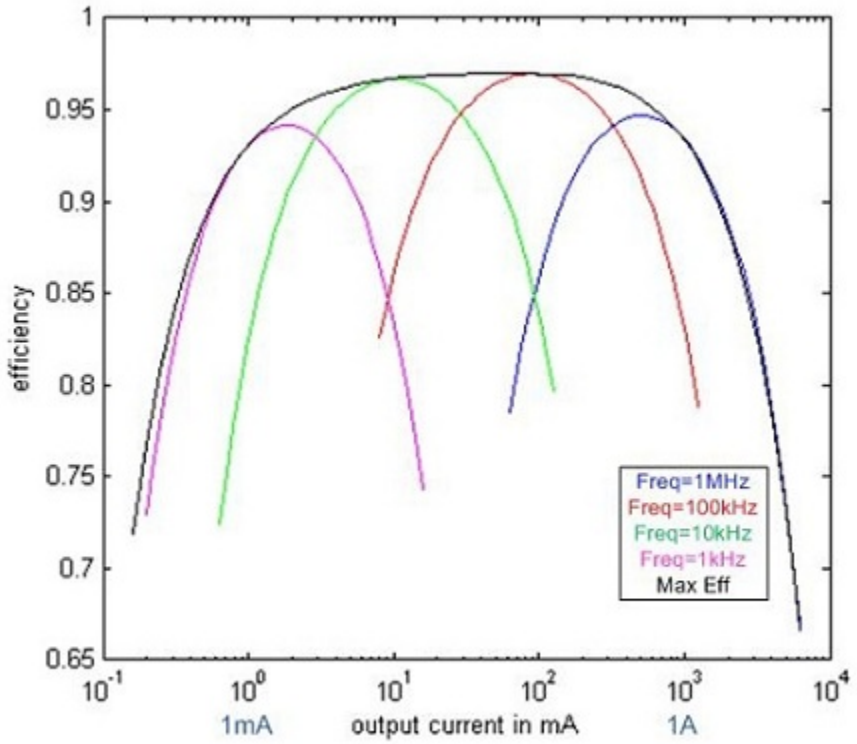


Figure 5.11: Expected efficiency of the third test chip at a fixed conversion ratio of 8-to-1

These results can be used to compare with those from the final test chip, as discussed in section 5.4. Since the final test chip is the only version with regulation implemented, its criteria in efficiency measurements will be different than in the first two versions. The sets of simulated efficiency results in the third test chip will serve as a bridge between solely measuring efficiency and measuring efficiency with regulation. Figure 5.12 shows the expected efficiency versus I_{OUT} of the third test chip at $V_{IN} = 12.5V$. When compared with figure 5.11, the converter suffers from low efficiency at very light load in both cases due to fixed losses. At intermediate I_{OUT} values, the difference in efficiency is due to switching frequency being chosen in figure 5.11 to maximize efficiency, whereas switching frequency was chosen to regulate V_{OUT} equal to 1.5V in figure 5.12. When calculating efficiency under regulation, R_{SSL} is set equal to $R_{FSL}/2$, and the conversion ratio is chosen to maximize efficiency, as discussed in chapter 3. These results do not include the impact due to the simplification made in implementing the controller, as discussed in section 3.3, but instead show the best efficiency if an ideal controller was used. At high I_{OUT} values, efficiency in figure 5.12 drops in steps as conversion ratio change is needed to maintain regulation, whereas efficiency in figure 5.11 drops gradually. Figure 5.13 shows the expected efficiency versus V_{IN} at $I_{OUT} = 100mA$. As the converter changes R_{OUT} and conversion ratio to maintain $V_{OUT} = 1.5V$, the efficiency shows a similar behavior as shown in figure 3.5 and discussed in section 3.2.3. The plot shows the efficiency of the converter varying significantly as a function of V_{IN}. As discussed in subsection 3.1.3, this motivates the use of finer conversion ratio step size topologies. Figure 5.14 shows a contour plot of the efficiency of the converter

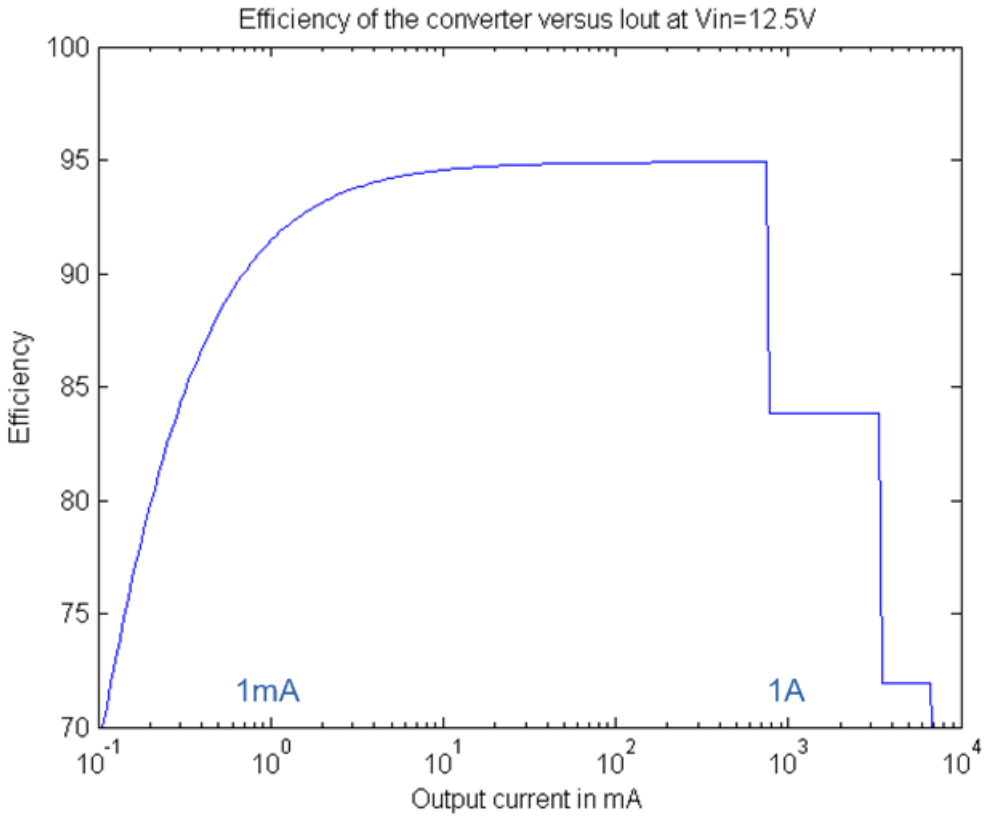


Figure 5.12: Efficiency versus I_{OUT} at V_{IN} = 12.5V of the third test chip if regulation was implemented and regulating V_{OUT} at 1.5V.

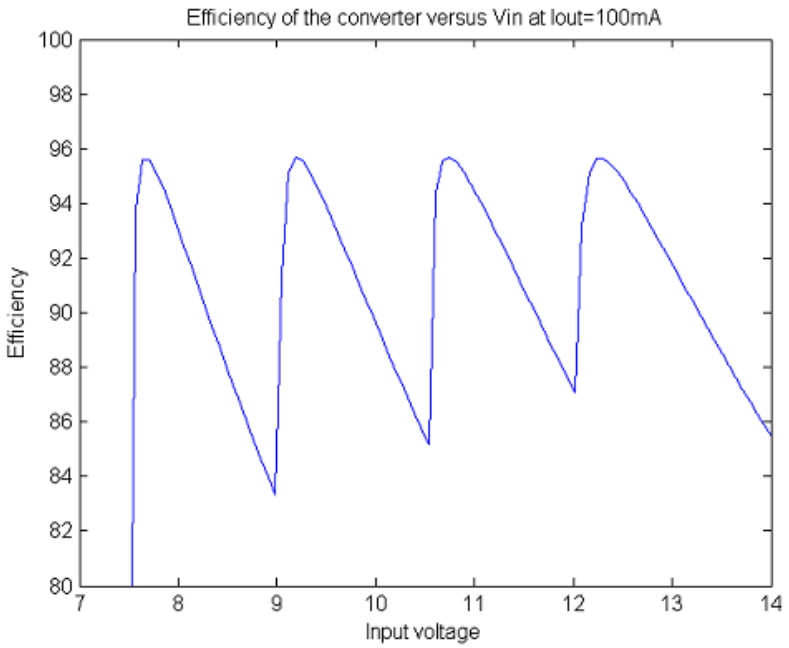


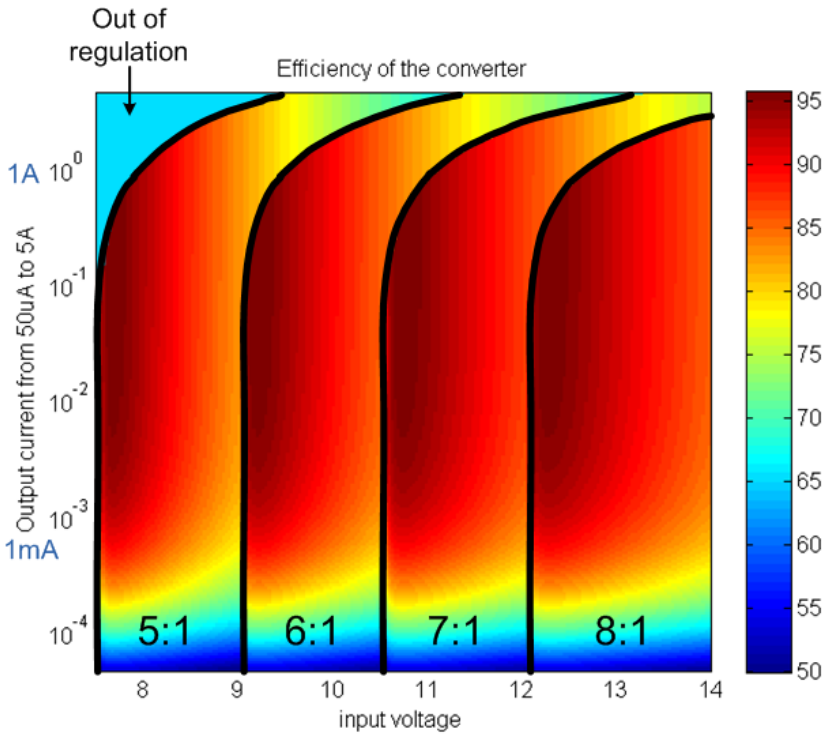
Figure 5.13: Efficiency versus V_{IN} at I_{OUT} = 100mA of the third test chip if regulation was implemented and regulating V_{OUT} at 1.5V.

versus both I_{OUT} and V_{IN}. The plots show how conversion ratio should be set in order to maximize efficiency.

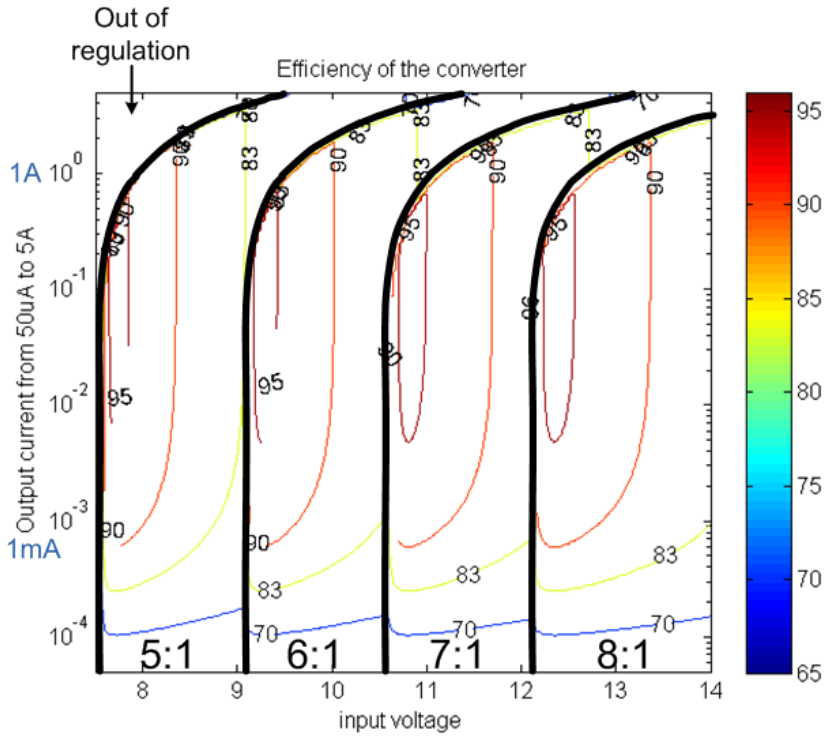
5.4 Fourth and final test chip

The fourth and final test chip of the converter focused on realizing the regulation scheme discussed in chapter 3. Figure 5.15 shows the schematic of the converter implemented in this version. Besides adding in the full controller, the converter architecture is the half-step multi-conversion-ratio topology for high efficiency across V_{IN} variations. The details of implementing the half-step multi-conversion-ratio topology are discussed in subsection 2.4.2. This implementation uses the ladder capacitor configuration for better regulation during line transients, as discussed in section 2.1. Table 5.7 shows the components used in this test chip, and the contributing factors to power loss. When comparing the power loss factors in table 5.7 with those of the third test chip, R_{FSL} is higher due to bondwire resistances, the additional regulation switches, and the 12V pass switch. The higher R_{SSL} is due to the use of the ladder capacitor configuration, resulting in use of lower energy density ceramic capacitors with lower voltage ratings, as discussed in section 2.1. The higher fixed loss is due to the additional circuits for regulation.

Figure 5.16 shows a die photo of this test chip, and table 5.8 shows the contribution of various components to the layout. In order to reduce parasitic resistances, 3 mil bondwires were used to reduce bondwire resistances, and power-train switches are sandwiched between two rows of bond-pads to reduce on-chip metal resistances, as evident in the die photo. Figure 5.17 shows the expected efficiency and measured efficiency of the converter versus I_{OUT} at



(a) Contour plot in color



(b) Contour plot in contour lines

Figure 5.14: Contour plot showing efficiency versus V_{IN} and I_{OUT} for the third test chip if regulation was implemented and regulating V_{OUT} at 1.5V.

around $V_{IN} = 8.7V$. The difference between expected efficiency and measured efficiency can be due to R_{SSL} being fixed at $R_{FSL}/2$ when calculating expected efficiency, but in reality this ratio can vary significantly due to the approximation used in the frequency loop, as discussed in subsection 3.3.2. Figure 5.18 shows the expected efficiency and measured efficiency of the converter versus V_{IN} at around $I_{OUT} = 50mA$ and $I_{OUT} = 220mA$. When compared with figure 5.13 of the third test chip, figure 5.18 shows significant improvement in efficiency variations across V_{IN} due to the availability of finer conversion ratio step size. Figure 5.19 shows the contour plot of the expected efficiency of the converter versus both I_{OUT} and V_{IN}.

In terms of load transients, figure 5.20 shows the behavior of the converter during loading and unloading steps of $I_{OUT} = 150mA$ at $V_{IN} = 13V$. In this case, the converter maintains regulation by changing switch conductance and switching frequency, but without changing conversion ratio. The gate drive signal in the figure is V_{GD} in figure 3.7 discussed in section 3.3. As evident in figure 5.20, the gate drive signal, V_{GD}, closely resembles V_{OUT} and reflects the behavior of the error amplifier discussed in subsection 3.3.1. As evident from the gate drive signal, V_{GD}, the converter changes clock phase at a particular value of V_{GD}. This behavior represents the lower-bound hysteretic control behavior in determining switching frequency, as expected from the frequency controller discussed in subsection 3.3.2. As evident in figure 5.20, the inner loop controller maintains V_{OUT} to be within a $20mV$ band during this load and unloading transient.

Figure 5.21 shows the behavior of the converter with an $I_{OUT} = 1A$ loading and unloading step at $V_{IN} = 9V$. In this case, one step change in conversion ratio is needed to maintain regulation. When the loading step occurs, V_{OUT} drops and causes a reduction in the conversion ratio from 5.5-to-1 to 5-to-1, as evident by the least significant bit (LSB) of the conversion ratio shown in the figure. This conversion ratio change causes V_{OUT} to rise back up to roughly the original level and maintain regulation. Conversely, the unloading step causes V_{OUT} to rise immediately, and causes the conversion ratio to increase back from 5-to-1 to 5.5-to-1. This quick increase in conversion ratio is due to the converter entering region E in the $G - V_{DROP}$ control space shown in figure 3.13, and discussed in subsection 3.3.3. As shown by the clock signal in the figure, despite the same I_{OUT} level, the switching frequency after the unloading step is lower than before the loading step. This is due to the available stored charge in the flying capacitors after the unloading transient. The stored charge allows the converter to maintain regulation with lower conductance. As the stored charge is drained away slowly by $I_{OUT} = 10mA$, the converter eventually reaches the same state as before the loading step. These behaviors match the simulation results shown in subsection 3.3.5, and confirm the performance of the outer loop conversion ratio controller discussed in subsection 3.3.3. As shown in the figure, the peak to peak variation in V_{OUT} is less than 30mV in this full loading and unloading step.

Figure 5.22 shows a loading and unloading transient in which two steps of change in conversion ratio are needed. As shown in the figure, the converter first changed from a conversion ratio of 6-to-1 to 5.5-to-1. However, this conversion ratio change was not enough, and V_{OUT} continued to drop. The converter then changed to a conversion ratio of 5-to-1 shortly after. The output voltage, V_{OUT}, then rose and settled at roughly the original voltage level before the loading transient. Although the converter experienced the same output current step in both figure 5.21 and figure 5.22, the number of conversion ratio change was not the same because the input voltage and initial condition of the converter

Capacitor and switch sizes	
$C_1 - C_9$	$10\mu F$
C_{IN}	$2.2\mu F + 10\mu F$
C_{OUT}	$10\mu F + 100\mu F$
1.5V switches $S_1 - S_4$	$120mm$
3V switch $S_6 - S_{11}$	$45mm$
regulation switches $S_{13} - S_{18}$	$40mm$
Contribution to R_{FSL}	
All switches	$70m\Omega$
On-chip metal	$25m\Omega$
Capacitor R_{ESR}	$7m\Omega$
Bond-wire resistance	$50m\Omega$
PCB trace resistance	$8m\Omega$
Aggregate numbers	
R_{FSL}	$160m\Omega$
R_{SSL}@$1MHz$	$75m\Omega$
R_{OUT}@$1MHz$	$177m\Omega$
Fixed Loss	$900\mu W$
Freq-dep Loss @1MHz	$26mW$

Table 5.7: The components used in the final test chip, and the different contributors to power loss.

was different in the two scenarios. When the unloading step occurred in figure 5.22, the conversion ratio switched back to 5.5-to-1 quickly. As discussed in subsection 3.3.3, the converter wait till the stored charges in its flying capacitors is used up before considering another increase in conversion ratio. This causes the conversion ratio to increase back to 6-to-1 at a later instance that is beyond the time frame of the scope in the experiment. As shown in the figure, the converter maintained regulation in the transient, and the variation in V_{OUT} was less than 45mV in the transient. The output capacitors used in these experiments are one $10\mu F$ 0603 ceramic capacitor and one $100\mu F$ 1210 ceramic capacitor, whereas the input capacitors used are one $2.2\mu F$ 0603 ceramic capacitor and one $10\mu F$ 1210 ceramic capacitor. Photos of the PCB used to test this chip are shown in figure 5.23. The layout of the chip and the various capacitors are labeled in the photo.

This test chip attains a high peak efficiency of 92% and enjoys efficiency higher than 80% over a wide range of output load current, namely from 5mA to 1A. While the performance of this test chip is superior to that of similar surveyed converters, as further discussed in section 5.5, this performance is not as impressive as the expected performance of the third test chip. This is because in this test chip, regulation was the main focus, and efficiency was sacrificed to obtain a robust regulation scheme. Although higher fixed loss is expected when regulation circuits are included in the design, there is ample potential to reduce this loss. As discussed in chapter 4, the largest contributor to constant power consumption is the error amplifier. As discussed in section 4.6, high error amplifier power consumption is needed because the error amplifier has to drive a large capacitive load while maintaining a bandwidth higher

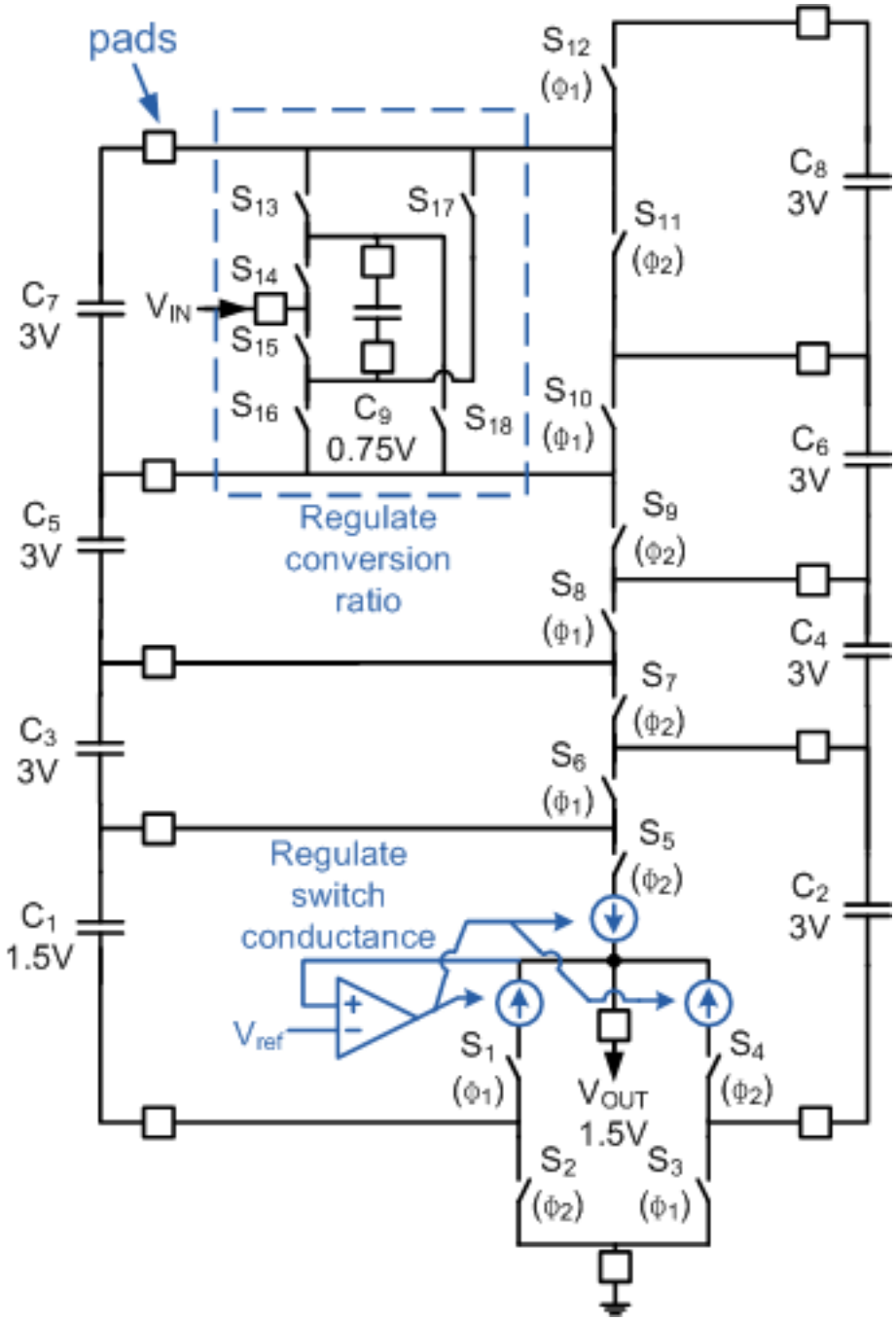


Figure 5.15: Circuit schematic of the final test chip

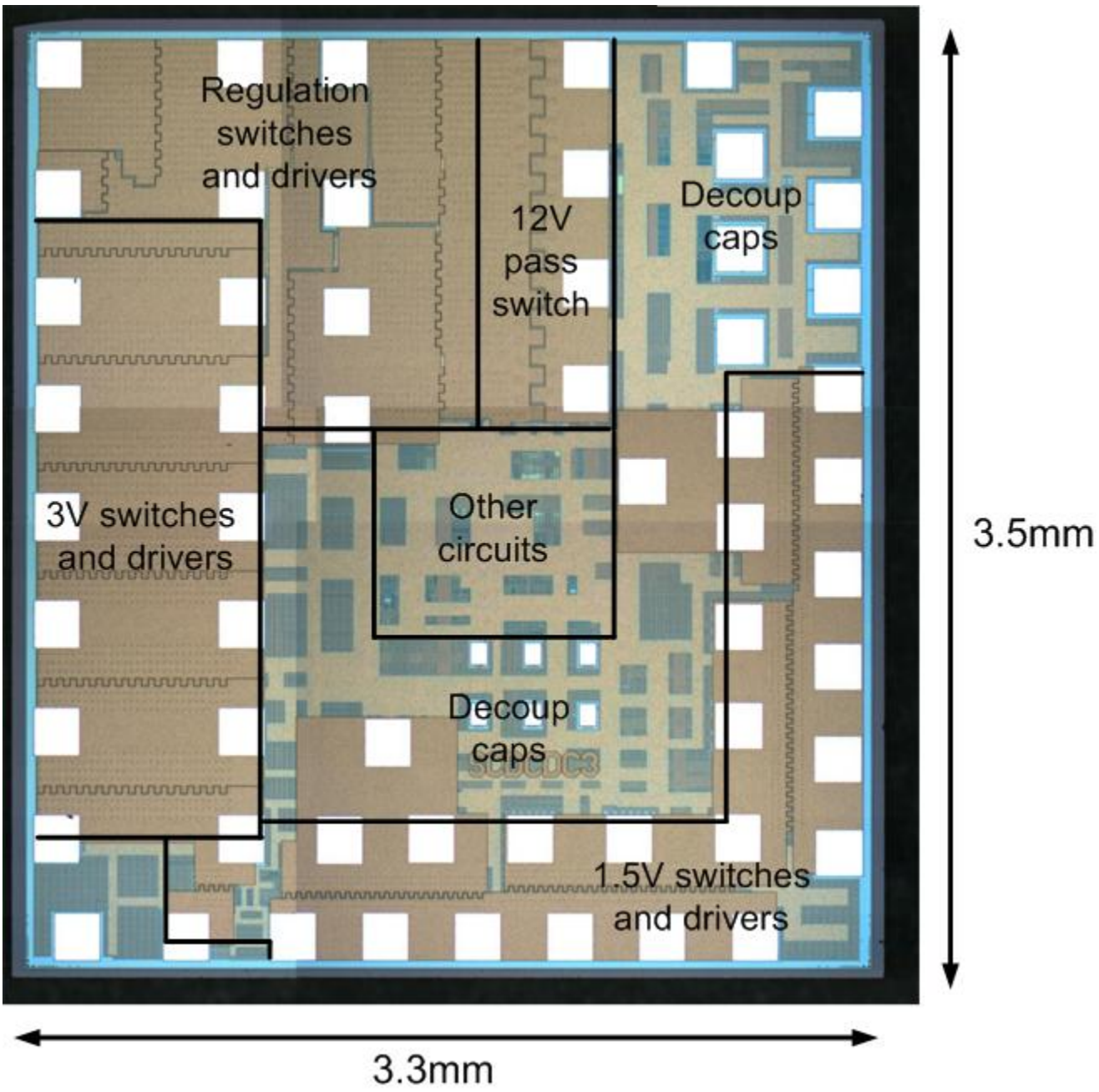


Figure 5.16: Die photo of the final test chip

	Area in layout
3V switches and drivers	$3.5mm^2$
1.5V switches and drivers	$0.6mm^2$
regulation switches and drivers	$1.5mm^2$
12V pass transistor	$0.25mm^2$
Other circuits	$0.66mm^2$
Decoupling capacitors	$3mm^2$
Total active area	$9.5mm^2$
Bond pads	$2mm^2$
Total die area	$11.5mm^2$

Table 5.8: Area of various components in die layout for the final test chip

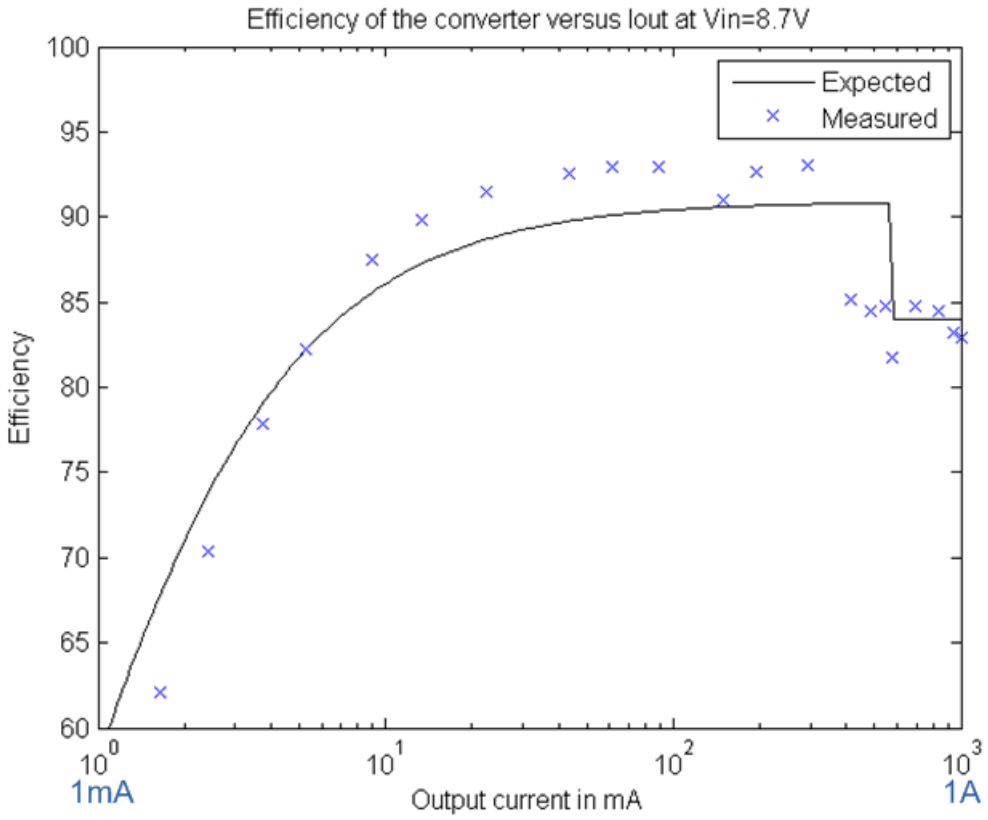
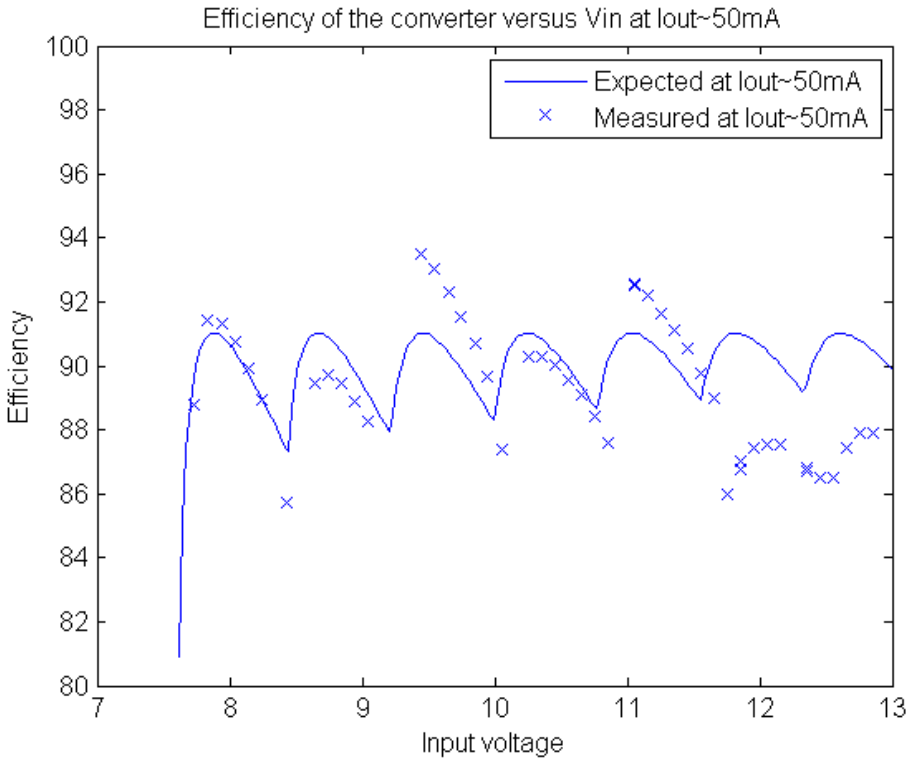
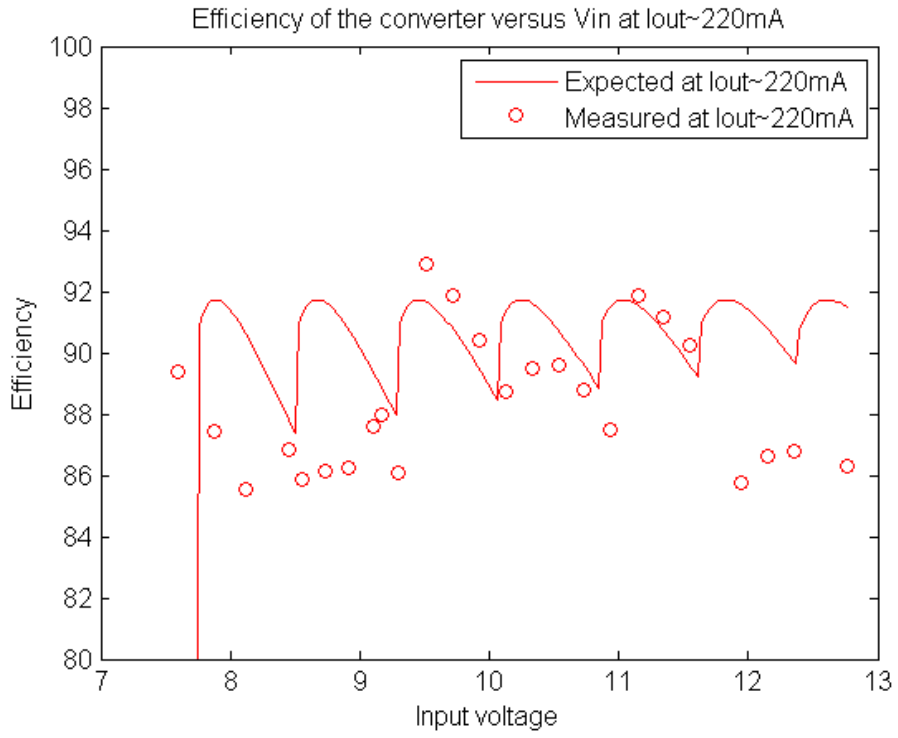


Figure 5.17: Efficiency versus I_{OUT} at around V_{IN} = 8.7V of the final test chip

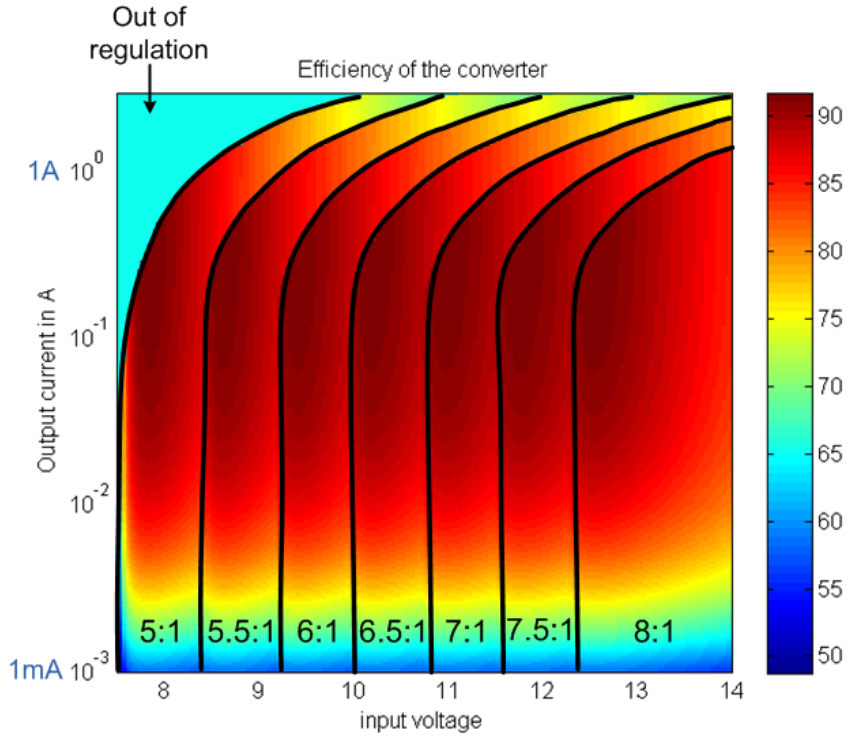


(a) Efficiency versus V_{IN} at I_{OUT} ~ 50mA

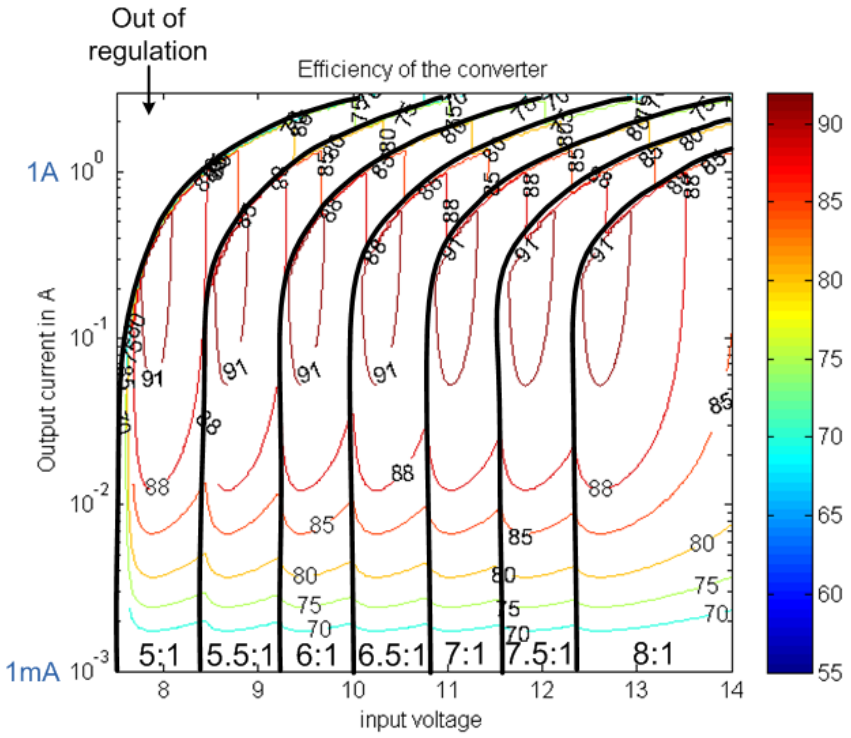


(b) Efficiency versus V_{IN} at I_{OUT} ~ 220mA

Figure 5.18: Efficiency versus V_{IN} at I_{OUT} ~ 50mA and 220mA of the final test chip



(a) Contour plot in color



(b) Contour plot in contour lines

Figure 5.19: Contour plot showing efficiency versus V_{IN} and I_{OUT} for the final test chip.

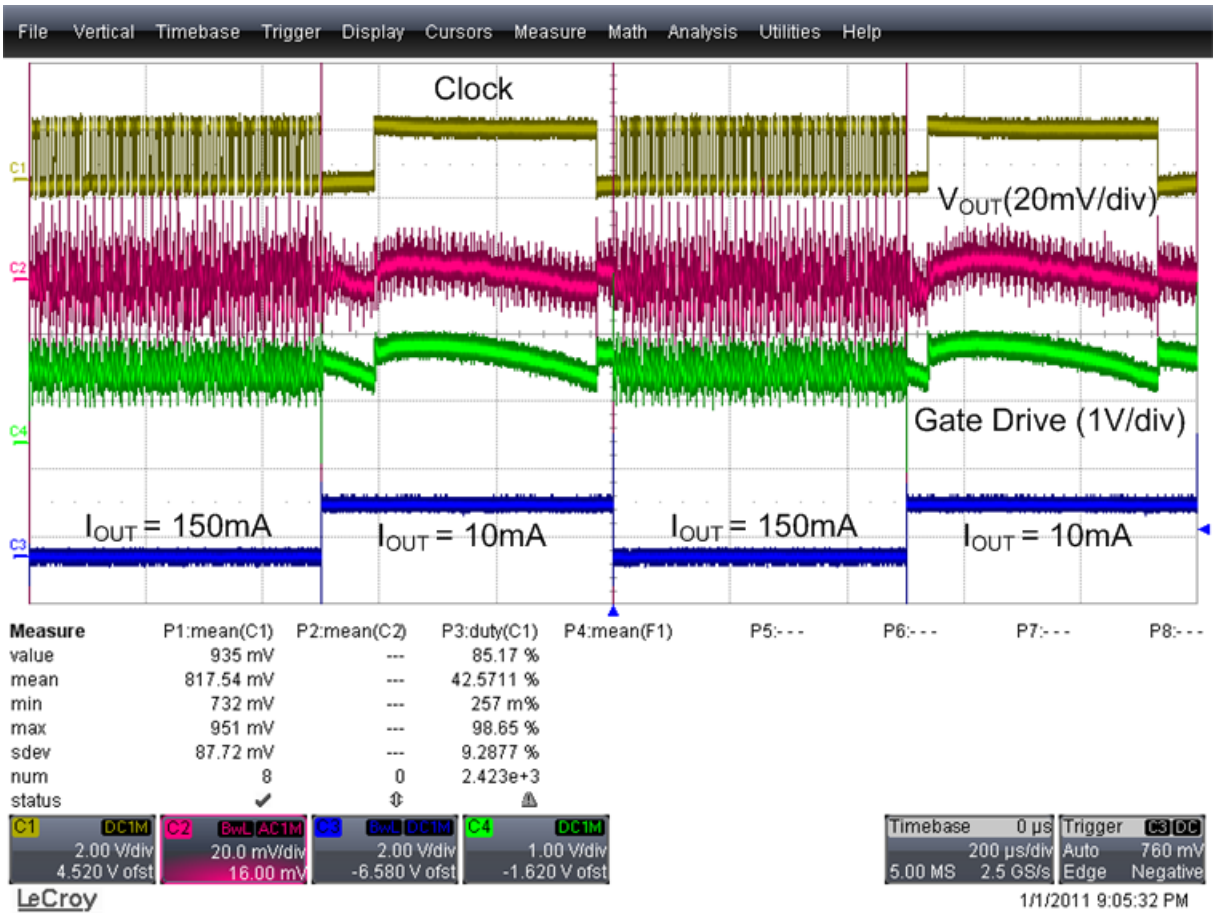


Figure 5.20: Oscilloscope shot of loading and unloading I_{OUT} step of 150mA for the final test chip. The top waveform is the switching clock of the converter. The second waveform is an AC coupled signal of the output voltage with 20mV/div. The third waveform shows the gate drive signal of switches $S_{1,4,5}$ in figure 5.15. The fourth waveform shows the drain of a MOSFET that switches in a 10Ω resistors in parallel to the output. This waveform represents the loading current step. The time scale is $200\mu s/div$.

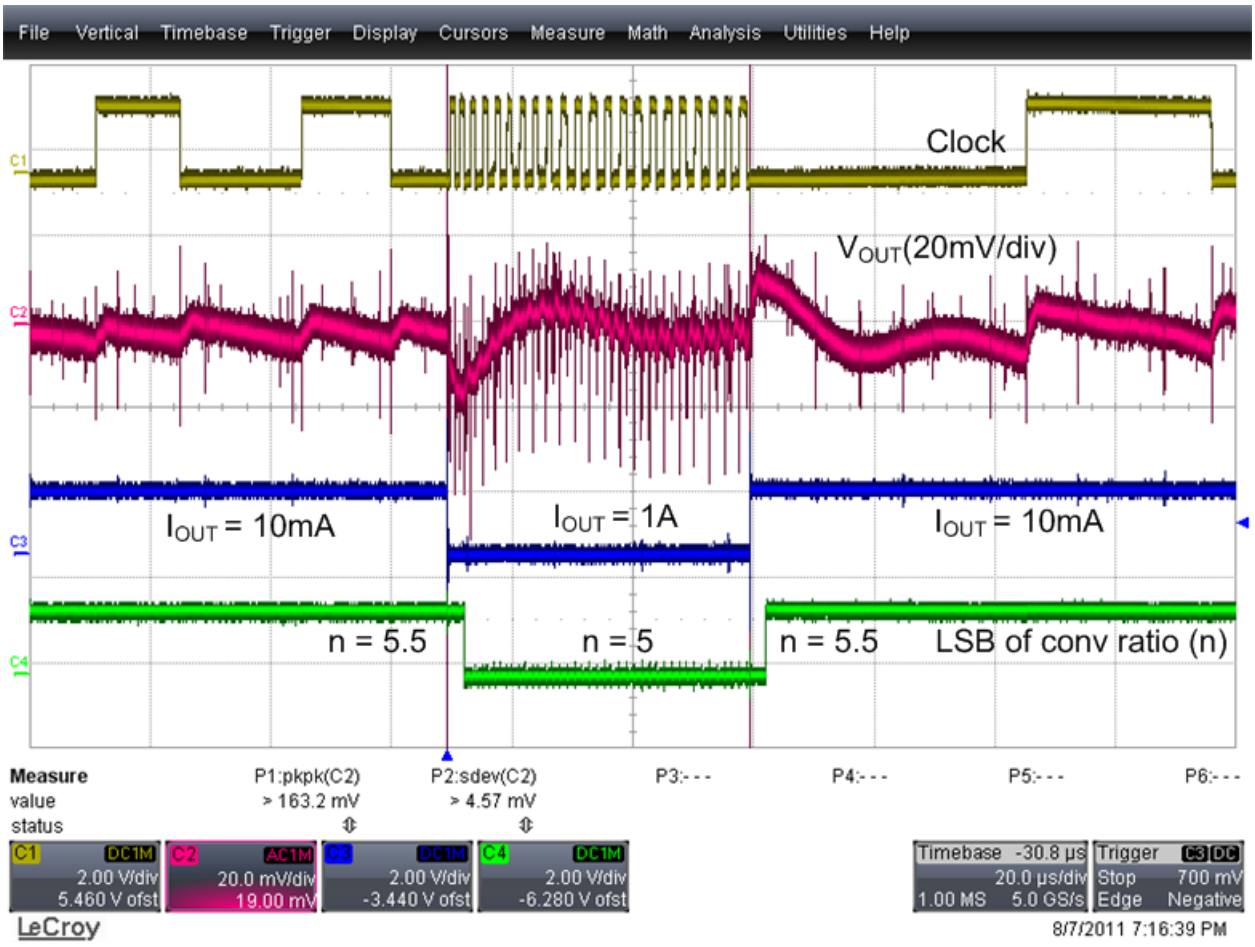


Figure 5.21: Oscilloscope plot of loading and unloading I_{OUT} step of 1A for the final test chip at $V_{IN} = 9V$. The top waveform is the switching clock of the converter. The second waveform is an AC coupled signal of the output voltage with 20mV/div. The third waveform shows the drain of a MOSFET that switches in three 4Ω resistors in parallel to the output. This waveform represents the loading current step. The fourth waveform shows the least significant bit of the conversion ratio, indicating that the converter changes conversion ratio back and forth by one step during the measurement. The time scale is $20\mu s/div$.

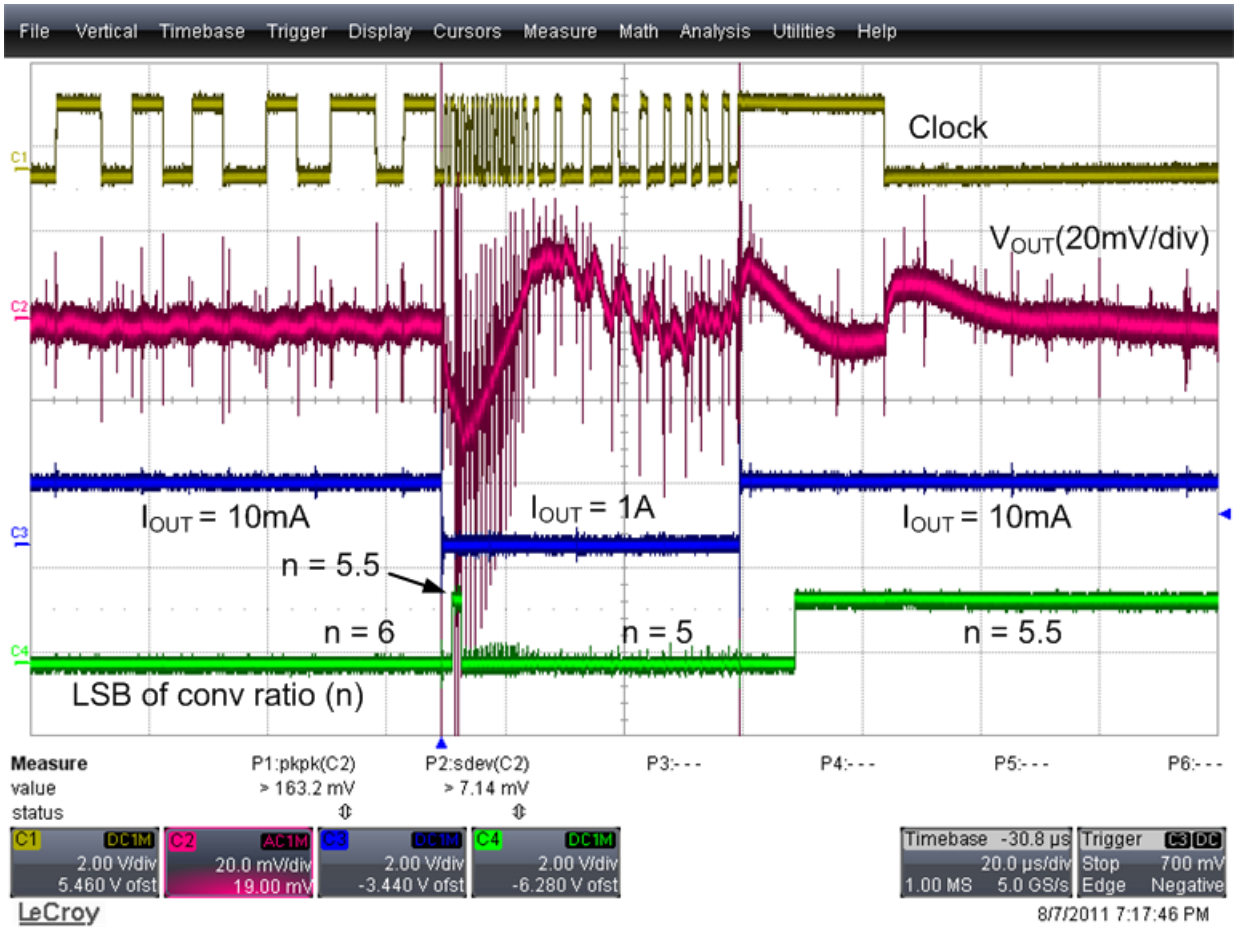
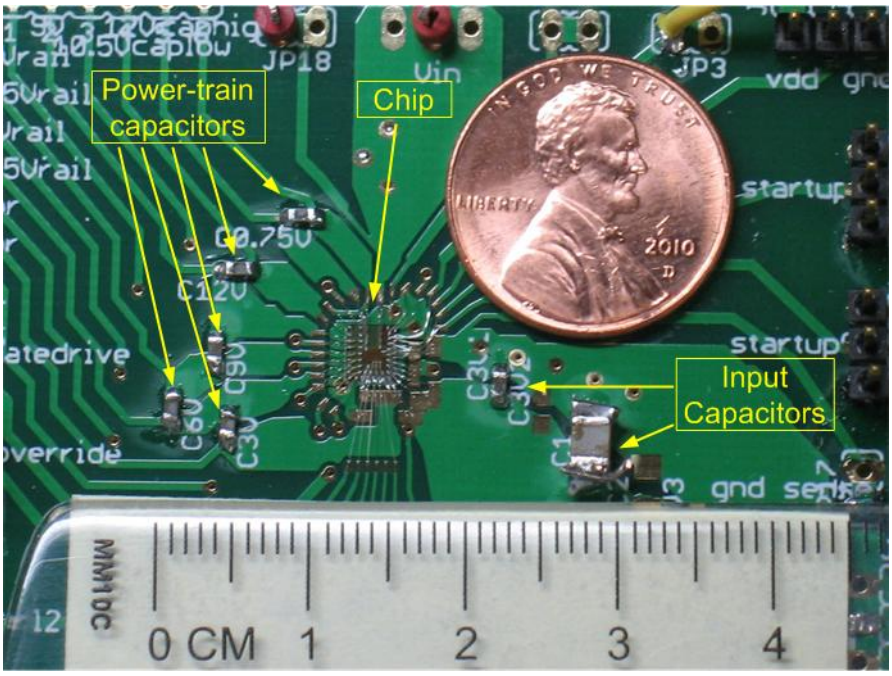
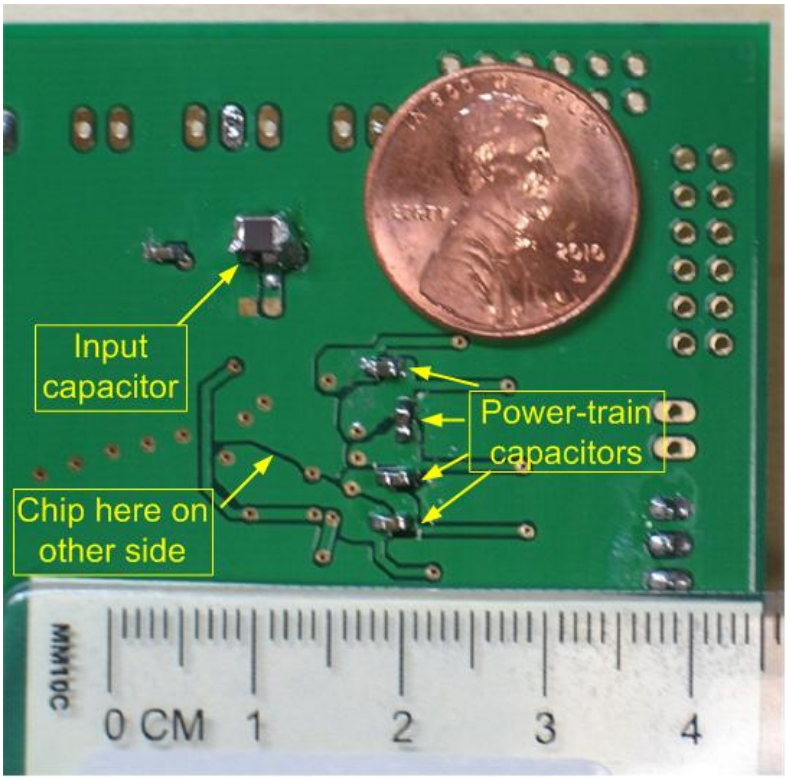


Figure 5.22: Oscilloscope plot of loading and unloading I_{OUT} step of 1A for the final test chip at $V_{IN} = 9.2V$. The top waveform is the switching clock of the converter. The second waveform is an AC coupled signal of the output voltage at 20mV/div. The third waveform shows the drain of a MOSFET that switches in three 4Ω resistors in parallel to the output. This waveform represents the loading current step. The fourth waveform shows the least significant bit of the conversion ratio, indicating that the converter changes conversion ratio by two steps after the loading step, and then back by one step after the unloading step. The time scale is $20\mu s/div$.



(a) Front side of PCB test setup



(b) back side of PCB test setup

Figure 5.23: The testboard used to test the final test chip

than the gain-bandwidth product of the overall feedback loop. This requirement can be removed if switch conductance regulation is eliminated and the inner loop controller only changes switching frequency. As discussed in section 3.1, this represents a potential trade-off between efficiency and ripple that the designer can make. Another potential improvement is to use a different architecture for the error amplifier, for example a class AB output stage may consume less power. The second largest constant power consumption occurs in the digital circuits. The error amplifier consumes about $375\mu W$ of power while the digital circuits consumes about $150\mu W$ of power, as discussed in chapter 4. The digital circuits consume significant power because they switch at *50MHz*, which is significantly higher than the *2.5MHz* maximum switching frequency of the converter. While a fast digital controller allows fast response, there may be limited degradation in regulation performance if the digital clock runs significantly slower, and there may be design choices to allow a reduction in switching frequency without compromising performance. All of these design choices are interesting topics to investigate but were not considered here because of the focus of this version of implementation. Thus while this version of implementation shows a reduction in efficiency in light load conditions, there is ample room for improvement and the results by no means represent a fundamental limit to the switched capacitor dc-dc converter.

5.5 Comparison with other works

Fig. 5.24 shows a comparison of the peak efficiency between the last test chip in this work and other works. All the surveyed buck and SC converters achieve respectable efficiency, but shows a general trend of reduced efficiency as conversion ratio increases. This trend mirrors the analysis in subsection 1.2.1. This work not only shows a significant increase in efficiency and conversion ratio when compared to surveyed SC converters, but also shows an improvement with respect to surveyed buck converters. Table 5.9 further compares the other important parameters of a dc-dc converter. This work maintains an efficiency higher than 80% over a very wide range of output load current, and wider than any of the surveyed converters. This work also obtains a similar or better peak to peak output transient with comparable input and output capacitance. In terms of passive components, this work achieves an overall reduction in PCB area and passive component cost when compared to dc-dc converters with similar ratings. While this work replaces the single inductor of the buck converter with 8 capacitors, the additional capacitors are considerably smaller and cheaper than the single inductor. This allows an overall reduction in aggregate PCB footprint and cost of the passive components. This comparison only considers input/output capacitors, inductors and power-train capacitors because other auxiliary passives required for compensation, start-up etc. are not fundamental and are eliminated or minimized in leading modern designs. The estimated cost of capacitors or inductors are based on large-volume purchase per-unit prices from Digikey.

This work demonstrates that SC converters not only can attain higher performance, but at the same time shrink the area and cost of passive components when compared with buck converters. The topology demonstrates superior performance compared to previous work largely due to improvements in the architecture, circuit design and device utilization.

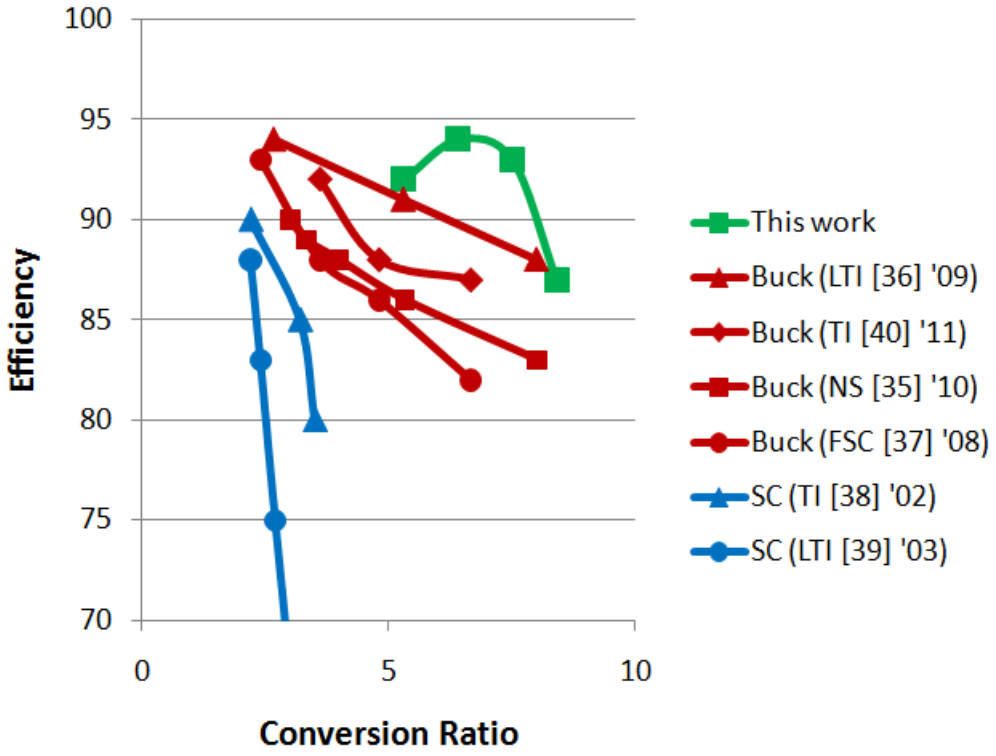


Figure 5.24: Comparison of peak efficiency between this work and similar works.

	input	output	peak I_{OUT}	peak Eff	>80% eff	pk-pk tran
This work	11V	1.5V	1A	92%	$5mA - 1A$	$45mV$
SC (TI '02,[38])	5V	1.5V	0.25A	85%	$2 - 200mA$	$50mV$
SC(LTI '03,[39]	5V	1.5V	0.5A	60%	-	$50mV$
Buck (NS '10,[35])	12V	1.5V	1A	83%	$0.35A - 1A$	$40mV$
Buck (LTI '09, [36])	12V	1.8V	1.5A	88%	$20mA - 1.5A$	$100mV$
Buck (FSC '08,[37])	12V	1.8V	2A	82%	$0.4A - 1.3A$	$500mV$
Buck (TI '11, [40])	12V	1.8V	2A	87%	$40mA - 2A$	$30mV$

	C_{IN}	C_{OUT}	Other main passives	PCB area	height	cost
This work	$12\mu F$	$110\mu F$	$10\mu F$ caps x8	$20mm^2$	*1.6mm*	$1
SC (TI '02,[38])	$2.2\mu F$	$10\mu F$	$1\mu F$ caps x2	$3.6mm^2$	*0.8mm*	$0.1
SC(LTI '03,[39]	$1\mu F$	$10\mu F$	$1\mu F$ caps x2	$2.7mm^2$	*0.8mm*	$0.1
Buck (NS '10,[35])	$10\mu F$	$100\mu F$	$10\mu H$ inductor	$57mm^2$	*4mm*	$1
Buck (LTI '09, [36])	$22\mu F$	$22\mu F$	$2.2\mu H$ inductor	$27mm^2$	*1.25mm*	$1.2
Buck (FSC '08,[37])	$10\mu F$	$22\mu F$	$15\mu H$ inductor	$57mm^2$	*3.9mm*	$1.74
Buck (TI '11, [40])	$20\mu F$	$44\mu F$	$2.2\mu H$ inductor	$30mm^2$	*1.25mm*	$1.46

Table 5.9: Comparison with other works

Chapter 6

Conclusion

The traditional inductor-based buck converter has been the default design for most switched-mode voltage regulators for decades. In its simplest form, the buck converter contains only two switches, one inductor, and the input capacitor[1]. Due to its relatively simple structure and control methodology, it is the dominant design for applications that require tight regulation (<10mV), high efficiency (>90%) and high output power (>100mW). Switched capacitor (SC) dc-dc converters, on the other hand, have traditionally been used in low power (<10mW) and low conversion ratio (<4:1) applications where neither regulation nor efficiency is critical. This work encompasses the complete successful design, fabrication, and test of a CMOS based switched capacitor dc-dc converter, addressing the ubiquitous 12V to 1.5V board-mounted point-of-load application. In particular, the circuit developed in this work attains higher efficiency (92% peak, and >80% over a load range of 5mA to 1A) than surveyed competitive buck converters, while requiring less board area and less costly passive components. The topology and controller enable a wide input range of 7.5V to 13.5V. Controls based on feedback and feedforward provide tight regulation under worst case line and load step conditions. This work shows that the SC converter can outperform the buck converter, and thus the scope of SC converter application can and should be expanded.

While this work shows the high potentials of SC converters, it is a only a step in fully recognizing the full benefit. It will be interesting to investigate the performance of the SC converters if capacitors that are more integrated are used to replace the discrete ceramic capacitors in this work. The capacitors can be fully integrated [8], or co-packaged on the die, or realized with deep-trench capacitors on an accompanying substrate. Using these capacitor technologies can further reduce the PCB footprint of dc-dc converters, and allow smaller sizes in electronic components where small is beautiful.

In terms of expanding the scope of SC converters, it may be interesting to further increase the output current level or the conversion ratio. It may be interesting to see how multi-phase can affect the operation and whether it provides significant reduction in the output capacitor as in the case of the buck converter [26]. In terms of regulation, there may exists other topologies that can give finer conversion ratio steps while keeping the complexity of the circuit at a minimum. With so many capacitors and switches, there may be different techniques for regulation. As discussed in section 3.3, this work simplifies the controller considerably, but there may be benefits in keeping some of the complexity in order to further increase the performance and efficiency of the converter. All of these methods show that

there are still many work that can be done on the SC converter to even further its potential advantage towards the traditional buck converter.

The benefits of the SC converter is clear, the only drawback is that it has not been fully understood yet. This work makes a step in understanding the SC converter, and shows that it has huge potentials. One day it may even dominate the market of dc-dc converters, and it will be the inductor-based buck converter that is limited to specific applications.

Bibliography

[1] J.G. Kassakian, M.F. Schlecht, and G.C. Verghese, *Principles of Power Electronics*, Addison-Wesley, 1991.

[2] M.S. Makowski and D. Maksimovic, "Performance limits of switched-capacitor dc-dc converters," *IEEE Power Electronics Specialists Conference*, vol.2, pp. 1215-1221, June 1995.

[3] M. Seeman and S. Sanders, "Analysis and Optimization of Switched-Capacitor DC-DC Converters", *IEEE Trans. on Power Electronics*, vol. 23, no. 2, March 2008.

[4] M. Seeman, V. Ng, H.-P. Le et. al, "A Comparative Analysis of Switched-Capacitor and Inductor-Based DC-DC Conversion Technologies", *IEEE Workshop on Control and Modeling of Power Electronics*, June 2010

[5] M. Seeman, "A Design Methodology for Switched-Capacitor DC-DC Converters", *PhD Dissertation*, UC Berkeley, May 2009.

[6] J.F. Dickson, "On-chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol 11, pp 376-378, June 1976.

[7] D. Wolaver, "Fundamental study of DC-DC conversion systems," *Ph.D. dissertation*, M.I.T., February 1969.

[8] H.-P. Le, M. Seeman, S. Sanders et. al, "A 32nm Fully Integrated Reconfigurable Switched-Capacitor DC-DC Converter Delivering 0.55W/mm2 at 81% Efficiency", *ISSCC Dig. Tech. Papers*, pp. 210-211, February 2010.

[9] J. Wibben and R. Harjani, "A High-Efficiency DC–DC Converter Using 2nH Integrated Inductors" *IEEE J. Solid-States Circuits*, vol 43, April 2008.

[10] J. Lee, G. Hatcher, L. Vandenberghe and C.K. Yang, "Evaluation of Fully-Integrated Switching Regulators for CMOS Process Technologies" *IEEE Trans on VLSI Systems*, vol 15, September 2007.

[11] R. Erickson and D. Maksimovic, " Fundamentals of Power Electronics" *Kluwer Academic Publishers*, 2001.

[12] K.H. Liu and F.C. Lee, "Zero-voltage switching technique in DC/DC converters", *IEEE Trans. on Power Electronics*, vol. 5, July 1990.

[13] F. Canales, F, P. Barbosa and F.C. Lee, "A zero-voltage and zero-current switching three-level DC/DC converter", *IEEE Trans. on Power Electronics*, vol. 17, November 2002.

[14] Werner Muth, "Matrix Method for Latch-up Free Demonstration in a Triple-Well Bulk-Silicon Technology", *IEEE Trans. on Nuclear Science*, vol 9, June 1992.

[15] S. Voldman et. al, "Latchup in merged triple well structure" *Proceedings of reliability physics symposium*, April 2005.

[16] P. Gray, P. Hurst, S. Lewis and R. Meyer, "Analysis and design of analog integrated circuits" *John Wiley & Sons Inc*, 2001.

[17] T. Tanzawa and T. Tanaka, "A dynamic analysis of the Dickson charge pump circuit" *IEEE J. Solid-States Circuits*, vol 32, August 1997.

[18] J.T. Wu and K.L. Chang, "MOS Charge Pumps for Low-Voltage Operation", *IEEE J. Solid-State Circuits*, vol 33, April 1998.

[19] C.C. Wang and J.C. Wu, "Efficiency Improvement in Charge Pump Circuits", *IEEE J. Solid-State Circuits*, vol 32, June 1997.

[20] G. Rincon-Mora and P. Allen, "A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator" *IEEE J. Solid-State Circuits,* vol 33, January 1998

[21] E. Bayer and H. Schmeller, "Charge Pump with Active Cycle Regulation - Closing the Gap between Linear- and Skip Modes" *IEEE Power Electronics Specialists Conference*, vol 3, pp. 1497-1502, August 2000.

[22] M.D. Seeman, S.R. Sanders and J.M. Rabaey, "An Ultra-Low-Power Power Management IC for Wireless Sensor Nodes", *IEEE Custom Integrated Circuits Conference*, pp. 567-570, September 2007.

[23] B. Gregoire, "A Compact Switched-Capacitor Regulated Charge Pump Power Supply" *IEEE J. Solid-States Circuits*, vol 41, August 2006.

[24] G. Zhu and A. Ioinovici, "Switched-Capacitor Power Supplies: DC Voltage Ratio, Efficiency, Ripple, Regulation" *IEEE Symp. Circuits and Systems*, vol 1, pp. 553-556, August 2002.

[25] S. Ben-Yaakov and A. Kushnerov, "Algebraic Foundation of Self-Adjusting Switched Capacitors Converters" *IEEE Energy Conversion Congress and Expo*, pp. 1582-1589, September 2009.

[26] J. Han, A. Jouanne, and G. Temes "A New Approach to Reducing Output Ripple in Switched-Capacitor-Based Step-Down DC–DC Converters" *IEEE Trans. on Power Electronics*, vol. 21, November 2006.

[27] G. Eirea, and S. Sanders, " Adaptive Output Current Feedforward Control in VR Applications" *IEEE Power Electronics Specialists Conference*, June 2007

[28] S. Rajapandian, K. Shepard, P. Hazucha and T. Karnik, "High-Voltage Power Delivery Through Charge Recycling" *IEEE J. Solid-States Circuits*, vol 41, June 2006.

[29] J. Rabaey, A. Chandrakasan and B. Nikolic, "*Digital Integrated Circuits: A Design Perspective*" Prentice Hall Electronics and VLSI series, 2003

[30] B. Razavi, "*Design of Analog CMOS Integrated Circuits*" McGraw-Hill Series in Electrical and Computer Engineering, 2001

[31] M. Seeman, S. Sanders and J. Rabaey, "An Ultra-Low-Power Power Management IC for Wireless Sensor Nodes", *IEEE Custom Integrated Circuits Conference*, Sept 2007

[32] V. Ng and S. Sanders, "A 98% Peak Efficiency 1.5A 12V-to-1.5V Switched Capacitor DC-DC Converter in 0.18um CMOS Technology", *Master's Thesis, EECS Department, University of California, Berkeley*, Jan 2008.

[33] V. Ng, M. Seeman, S. Sanders, "High-Efficiency, 12V-to-1.5V DC-DC Converter Realized with Switched Capacitor Architecture", *IEEE Symposium on VLSI Circuits*, June 2009

[34] V. Ng, M. Seeman, S. Sanders, "Minimum PCB Footprint Point-of-Load DC-DC Converter Realized with Switched Capacitor Architecture", *IEEE Energy Conversion Congress and Exposition*, Sept 2009

[35] National Semiconductor Inc (LMZ12001), "1A SIMPLE SWITCHER Power Module with 20V Maximum Input Voltage", June 2010

[36] Linear Technology (LTC3601), "1.5A, 15V Monolithic Synchronous Step-Down Regulator", 2009.

[37] Fairchild Semiconductor Inc (FAN8301), "2A, 16V, Non-synchronous Step-down, DC/DC Regulator", November 2008.

[38] Texas Instruments (TPS60503), "High Efficiency, 250mA step-down charge pump", Feb 2002.

[39] Linear Technology (LTC3251), "500mA High Efficiency, Low Noise, Inductorless Step-Down DC/DC Converter", 2003

[40] Texas Instruments (TPS54226), "4.5V to 18V Input, 2-A Synchronous Step-Down SWIFT Converter with Eco-Mode", Feb 2011.

[41] L. Salem, and R. Jain, "A Novel Switched-Capacitor DC-DC Converter Ripple Mitigation Technique", *IEEE International Symposium on Circuits and Systems*, June 2010

Appendix

Below is the verilog code used to generate the digital controller in this work.

```
//Verilog HDL for "tapeout4", "Controller_ideal11" "verilog"
//Clock is the input clock signal
//Clk1 and Clk2 are the two phase clocks

module Controller_ideal11 (FreqMax, Clock, reset, ComIn, dropIn, Clk1, Clk2, CtrlOut,
Clk1In, Clk2In, CtrlIn, override, NoConnectOut, ready, startupIn, LinReg, HVCon);

input FreqMax;          //means switch at maximum frequency
input Clock, reset;
input ready;            //use in startup means vdd ready
input [1:0] startupIn;  //indicate which startup phase should be in
input [4:0] ComIn;      //The switch control signal
input [7:0] dropIn;     //amount of drop in Rout
input Clk1In, Clk2In;   //override signal of Clk1, Clk2
input [2:0] CtrlIn;     //override signal of Ctrl
input override;         //override signal
output [2:0] CtrlOut;   //Control signal for the conversion ratio
output Clk1,Clk2;       //the two phase clock output
output NoConnectOut;    //indicate not connect to input
output LinReg;          //1 means linear regulator on
output HVCon;           //1 means High voltage switch on

reg [4:0] Com;          //latched Com signal
reg [7:0] drop;         //latched drop signal
reg [1:0] state;        //the state of the clock
reg [2:0] Ctrl;         //the control is stored
reg [8:0] CtrlWait;     //the cycles to wait before change conv ratio
reg NoConnect;          //not connect to input, used in lowering gear
reg [8:0] ClkCt;        //count the number of clock tick of clock
reg [8:0] TargetClk;    //the num of clk period before switch phase
reg [1:0] startup;      //indicate which startup phase should be in
reg [1:0] suMerge;      //merging info from startupIn and startup
```

```
//these parameters define the state, which many things depends on
parameter [1:0]         State01= 2'b00,         //in deadtime, next state is phase 1
                        State02= 2'b01,         //in deadtime, next state is phase 2
                        State1 = 2'b11,         //currently in phase 1
                        State2 = 2'b10;         //currently in phase 2

parameter [1:0] startup0 = 2'b00,       //normal operation mode
                        startup1 = 2'b01,       //startup phase 1
                        startup2 = 2'b11,       //startup phase 2
                        startup3 = 2'b10;       //active operation mode

//merging information from startup and startupIn
always @ (startupIn or startup)
        begin
        if ( (&{startupIn[1],~startupIn[0]}) ||
           (&{~startupIn[1],~startupIn[0],startup[1],~startup[0]}) )
                suMerge = 2'b10;        //active phase
        else if ( (&{startupIn[1],startupIn[0]}) ||
                (&{~startupIn[1],~startupIn[0],startup[1],startup[0]}) )
                suMerge = 2'b11;        //startup phase 2
        else if ( (&{~startupIn[1],startupIn[0]}) ||
                (&{~startupIn[1],~startupIn[0],~startup[1],startup[0]}) )
                suMerge = 2'b01;        //startup phase 1
        else                            //default case, should not happen
                suMerge = 2'b10;
        end


//set the clock period depending on switch conductance strength
always @ (FreqMax or Com or suMerge)
        begin
        if (FreqMax)
                TargetClk = 9;
        else if ( &{~suMerge[1],suMerge[0]} )
                TargetClk = 20;
        else if ( &{suMerge[1],suMerge[0]} )
                TargetClk = 200;
        else if (Com[4:3])
                TargetClk = 500;
        else if (Com[2])
                TargetClk = 100;
        else if (Com[1])
                TargetClk = 20;
        else
                TargetClk = 9;
```

```
        end

//things to be done at each clock tick
always @ (posedge Clock)
        begin
        Com <= ComIn;                   //latch these input values
        drop <= dropIn;
        if (reset)                      //reset the controller
                begin
                state <= State01;
                ClkCt <= 0;
                Ctrl <= 6;
                CtrlWait <= 0;
                NoConnect <= 0;
                startup <= 2'b01;
                end
        //startup phase 1
        else if ( &{~suMerge[1],suMerge[0]} )
                begin
                if (~state[1])                          //if in deadtime
                        begin
                        state <= ~state;
                        ClkCt <= 0;
                        end
                else
                        begin
                        if ((ready)&&(|ClkCt[8:4]))     //ready to switch
                                begin
                                if ((ClkCt<TargetClk) &&(&CtrlWait))
                                        begin           //change startup phase
                                        state[1] <= 0;
                                        startup <= 2'b11;
                                        CtrlWait <= 0;
                                        NoConnect <= 1;
                                        Ctrl <= 6;
                                        end
                                else if (ClkCt<TargetClk)
                                        begin           //count it
                                        CtrlWait <= CtrlWait + 1;
                                        state[1] <= 0;
                                        NoConnect <= 0;     //for safety, not used
                                        Ctrl <= 6;
                                        end
                                else                        //just switch
                                        begin
                                        state[1] <= 0;
```

```
                        NoConnect <= 0;       //for safety, not used
                        Ctrl <= 6;
                        end
                end
        else if (~&{ClkCt[8],ClkCt[7]})
                begin
                ClkCt <= ClkCt+1;
                NoConnect <= 0;               //for safety, not used
                Ctrl <= 6;
                end
        else
                begin
                NoConnect <= 0;               //for safety, not used
                Ctrl <= 6;
                end
        end
//startup phase 2
else if ( &{suMerge[1],suMerge[0]} )
        begin
        if (~state[1])                        //if in deadtime
                begin
                state <= ~state;
                ClkCt <= 0;
                end
        else
                begin
                if (ClkCt>TargetClk)
                        begin
                        state[1] <= 0;
                        if (|CtrlWait[8:6])
                                begin
                                startup <= 2'b10;
                                NoConnect <= 0;
                                CtrlWait[8:0] <= 9'b111111000;
                                end
                        else
                                begin
                                CtrlWait <= CtrlWait + 1;
                                if ((~|drop[7:4])&&(|Ctrl)&&(~FreqMax))
                                        Ctrl <= Ctrl - 1;
                                else if ( (&drop[6:0])
                                         &&(~&Ctrl[2:1])&&(~FreqMax))
                                        Ctrl <= Ctrl + 1;
                                end
                        end
```

```
                else if (~&{ClkCt[8],ClkCt[7]})
                        ClkCt <= ClkCt+1;
                end
        end
//active operation mode
else
        begin
        if (~state[1])                                  //if in deadtime
                begin
                state <= ~state;
                ClkCt <= 0;
                end
        else
                begin
                if (ClkCt > TargetClk)
                        begin
                        state[1] <= 0;                  //change phase
                        //no slow conv ratio change until waited enough
                        if (~|CtrlWait[8:2])
                                begin
                                CtrlWait <= CtrlWait + 1;
                                end
                        end
                //time to connect back to source
                else if (NoConnect && (~|Com[4:2]) &&(|ClkCt[8:2]))
                        begin
                        NoConnect <= 0;
                        end
                //feedforward
                else if ( (~NoConnect) &&(~&drop[4:0])
                        && (|Ctrl) && (|ClkCt[8:2]) && (~FreqMax))
                        begin
                        ClkCt <= 0;
                        CtrlWait <= 0;
                        NoConnect <= 0;
                        if (~drop[0])                   //reduce conv ratio by 6
                                Ctrl <= 0;
                        else if (~drop[1])
                                begin
                                if (&Ctrl[2:1])
                                        Ctrl <= 1;
                                else
                                        Ctrl <= 0;
                                end
                        else if (~drop[2])
                                begin
```

```
                if (Ctrl[2])
                        Ctrl <= Ctrl-4;
                else
                        Ctrl <= 0;
                end
        else if (~drop[3])
                begin
                if (Ctrl[2])
                        Ctrl <= Ctrl-3;
                else
                        Ctrl <= 0;
                end
        else
                begin
                if (|Ctrl[2:1])
                        Ctrl <= Ctrl-2;
                else
                        Ctrl <= 0;
                end
        end
//decrease conversion ratio
else if ( (~|Com) && (~&drop) &&(|Ctrl)
          && (|ClkCt[8:2]) && (|CtrlWait[8:2])
          &&(~FreqMax))
        begin
        Ctrl <= Ctrl-1;
        CtrlWait <= 0;
        NoConnect <= 0;
        ClkCt <= 0;                     //extend clock period
        end
//Output too high, increase conv ratio
else if ((&{Com,~NoConnect})
          &&(|ClkCt[8:2]) &&(~FreqMax))
        begin
        NoConnect <= 1;
        CtrlWait <= 0;
        ClkCt <= 0;
        if (~&Ctrl[2:1])
                Ctrl <= Ctrl+1;
        end
//drop too low
else if ((~|drop[7:5])&&(|Ctrl)&&(~FreqMax)
          &&(~NoConnect)&&(|CtrlWait[8:2])
          &&(|ClkCt[8:2]))
        //reduce conv ratio to increase eff
        begin
```

```
                    Ctrl <= Ctrl-1;
                    CtrlWait <= 0;
                    NoConnect <= 0;
                    ClkCt <= 0;
                    end
                //too slow, increase conv ratio
                //boundary is count = 256
                else if ((ClkCt[8])&&(&drop[6:0])&&(~NoConnect)
                     &&(~&Ctrl[2:1])&&(~FreqMax)
                     &&(|CtrlWait[8:2]))
                    begin
                    Ctrl <= Ctrl+1;
                    CtrlWait <= 0;
                    NoConnect <= 1;
                    ClkCt <= 0;
                    end
                //increase clock count if ClkCt < 384
                //so circuit does not switch if Com[3] is high
                else if (~&{ClkCt[8],ClkCt[7]})
                    ClkCt <= ClkCt+1;
                end
            end                     //end the else reset
        end                         //end the always statement

assign Clk1 = (override)?Clk1In:(&state);
assign Clk2 = (override)?Clk2In:(state[1]&(~state[0]));
assign CtrlOut = (override)?CtrlIn:Ctrl;
assign NoConnectOut = (override)?(1'b0):NoConnect;
assign LinReg = suMerge[0];
assign HVCon = suMerge[1];

endmodule
```