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Direct-Sequence Spread-Spectrum Techniques at the Antenna with CMOS SOI

A dissertation submitted in partial satisfaction
of the requirements for the degree

Doctor of Philosophy
in
Electrical and Computer Engineering

by

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To my parents.

Acknowledgements

I had the good fortune to work with Professor Jim Buckwalter, he has been a great mentor throughout my PhD career on personal and technical levels. Not only has he taught me a great deal technically but I have found his other lessons equally important.

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To my parents, thank you for your patience and unwavering support. I feel so lucky to have you as my parents. Your unconditional love and willingness to do anything for your children is beyond remarkable. I am so thankful to both of you.

Curriculum Vitæ

Hussam AlShammary

Education

2019	Ph.D. in Electrical and Computer Engineering (Expected), University of California, Santa Barbara.
2014	M.S. in Electrical and Computer Engineering, Carnegie Mellon University.
2011	B.Sc. in Electrical Engineering with first honors, King Fahd University of Petroleum & Minerals.

Publications

C.1 **H. AlShammary,** C. Hill, A. Hamza and J. F. Buckwalter, "Code Selective Filters in CMOS Processes for Full Duplex Communication and Interference Mitigation," GOMACTech, March, 2018

C.2 **H. AlShammary,** C. Hill, A. Hamza and J. F. Buckwalter, "A $\lambda/4$-Inverted N-path Filter in 45-nm CMOS SOI for Transmit Rejection with Code Selective Filters," International Microwave Symposium, June, 2018

C.3 C. Hill, C. Levy, **H. AlShammary,** A. Hamza and J. F. Buckwalter, "A 30.9 dBm, 300 MHz 45-nm SOI CMOS Power Modulator for Spread-Spectrum Signal Processing at the Antenna," International Microwave Symposium, June, 2018

C.4 A. Hamza, **H. AlShammary,** C. Hill and J. F. Buckwalter, "A 52-dB Self-Interference Rejection Receiver using RF Code-Domain Signal Processing," IEEE CICC, April, 2019

C.5 C. Hill, **H. AlShammary,** A. Hamza and J. F. Buckwalter, "A 1.5-dB Insertion Loss, 34-dBm P1dB Power Modulator with % 46 Fractional Bandwidth in 45-nm CMOS SOI," IEEE IMS, June, 2019

C.6 **H. AlShammary,** C. Hill, A. Hamza and J. F. Buckwalter, "A Code-Domain RF Signal Processing Front-end with 49.5-dB Receive Path Self-Interference Rejection to 12.1-dBm Power Compression and Transmit Path Power Handling of 34.3 dBm," RFIC, June, 2019

J.1 M.T. Abuelmaatti and **H. AlShammary,** "A new 555-timer based phase-to-voltage converter," Electronics World Magazine, Vol. 116, Issue 1894, October, 2010

J.2 A. Hamza, **H. AlShammary,** C. Hill and J. F. Buckwalter, "A Series N-path Code Selective Filter for Full-Duplex Communications," MWCL, January, 2019

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J.5 **H. AlShammary,** A. Hamza, C. Hill, and J. F. Buckwalter, "A Reconfigurable Spectrum Compressing Receiver for Non-Contiguous Carrier Aggregation in CMOS SOI," IEEE Journal of solid state circuits In press

J.6 **H. AlShammary,** A. Hamza, C. Hill, and J. F. Buckwalter, "A Code-Domain RF Signal Processing Front-end with 49.5-dB Receive Path Self-Interference Rejection to 12.1-dBm Power Compression and Transmit Path Power Handling of 34.3 dBm," IEEE Journal of solid state circuits, In press

J.7 **H. AlShammary,** A. Hamza, C. Hill, and J. F. Buckwalter, "A Non-binary RAKE Demodualtor At The Antenna For Frequency Diversity With CMOS SOI," IEEE Solid State Circuits Letters, In preparation

P.1 M.T. Abuelmaatti and **H. AlShammary,** "555 timer-based phase-to-voltage converter," US Patent : US8188734 B1. Granted on November, 2015.

P.2 **H. AlShammary** and J.F.Buckwalter, "LO Modulation for Non-Contiguous Carrier Aggregation," US Patent : submitted and available for licensing

Abstract

Direct-Sequence Spread-Spectrum Techniques at the Antenna with CMOS SOI

by

Hussam AlShammary

This dissertation provides an overview of challenges of modern wireless communications including frequency spectral efficiency, multiple-path fading, hardware complexity and un-utilized white spaces in the spectrum. By using Direct-Sequence Spread-Spectrum (DSSS) codes it is possible to overcome some of those challenges. Full-Duplex (FD) systems are improved with DSSS techniques by increasing the rejection of the Self-Interference (SI) form co-located transmitter (TX) as well as rejecting the TX replicas before and post the antenna. Out of band jammres are rejected as well relaxing the linearity requirements of the receive (RX) chain. Carrier Aggregation (CA) is possible with DSSS at a much lower power consumption and hardware complexity as well as much faster settling time. Spectrum Sensing (SS) to detect unused frequency bands is achieved with DSSS at lower power consumption. A frequency diversity technique is introduced to overcome the fading of wireless channel. To support theoretical analysis, experimental verification with CMOS SOI is discussed in detail and several designs are included.

Contents

Chapter 1

Introduction

Wireless communications offer mobility and ease of data access at the cost of interference among users. Traffic in mobile users has been growing at an exponential rate over the recent years. Fig. 1.1 shows monthly data rate transferred globally. This growth is attributed to an increase in the number of users as well as demand for higher content and quality of transferred data.

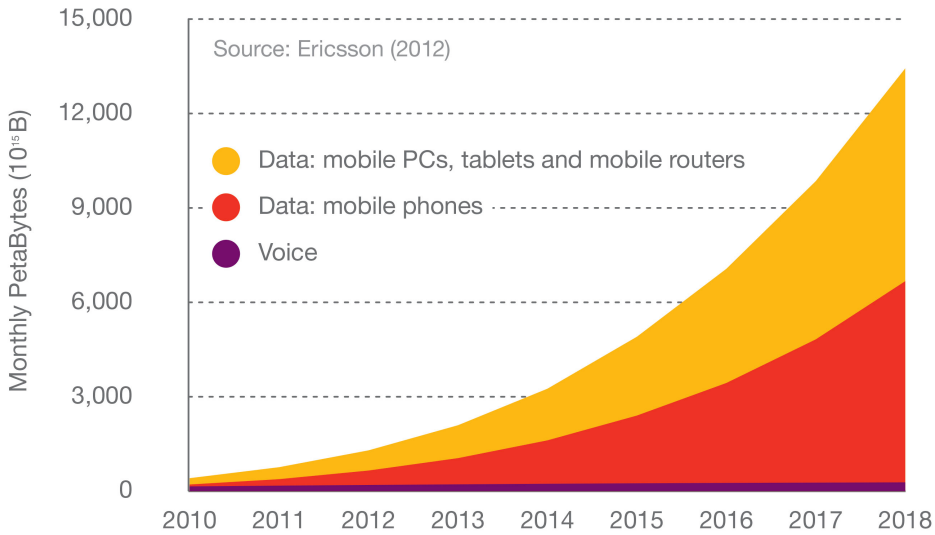


Figure 1.1: Monthly data traffic in recent years.

The spectrum and wireless channel, however, are finite resources with limited allocation and expansive price. Fig. 1.2 shows the allocated spectrum in the United States. In 2017 T-Mobile acquired 31 MHz in 600MHz band for $ 20,000,0000,000. Due to the increased demand for higher data rate through a limited and expansive channel, sophisticated techniques target increasing the efficiency of the channel.

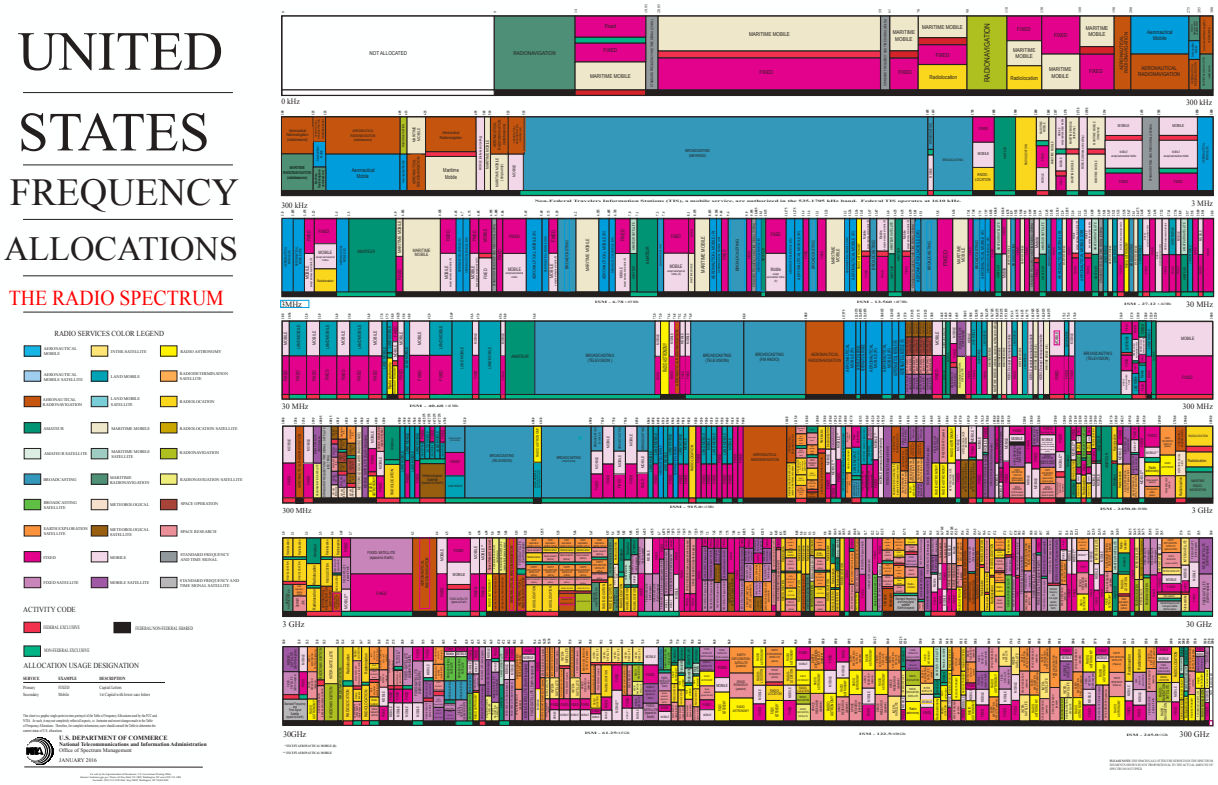


Figure 1.2: Allocated frequency spectrum in the United States.

1.1 Full-Duplex Communications

One potential access technique is Full-Duplex (FD). Unlike Frequency-Division Duplex (FDD) where the transmit uplink (TX) and receive downlink (RX) at different frequencies separated by a duplex space, FD targets transmitting and receiving at the

same frequency and at the same time, Fig. 1.3.a shows an illustration of this technique. The biggest challenge in FD communication is the leakage of co-located TX to the RX which is often characterized by TX Self-interference (SI). Classical FD systems produce a replica of the TX signal at various locations in the chain then subtract that replica from correct locations in RX chain as showing Fig. 1.3.b. To achieve a receiver sensitivity of -80 dBm it is desirable to have at least of total of 120 dB of TX-SI rejection for practical links as shown in Fig. 1.4.

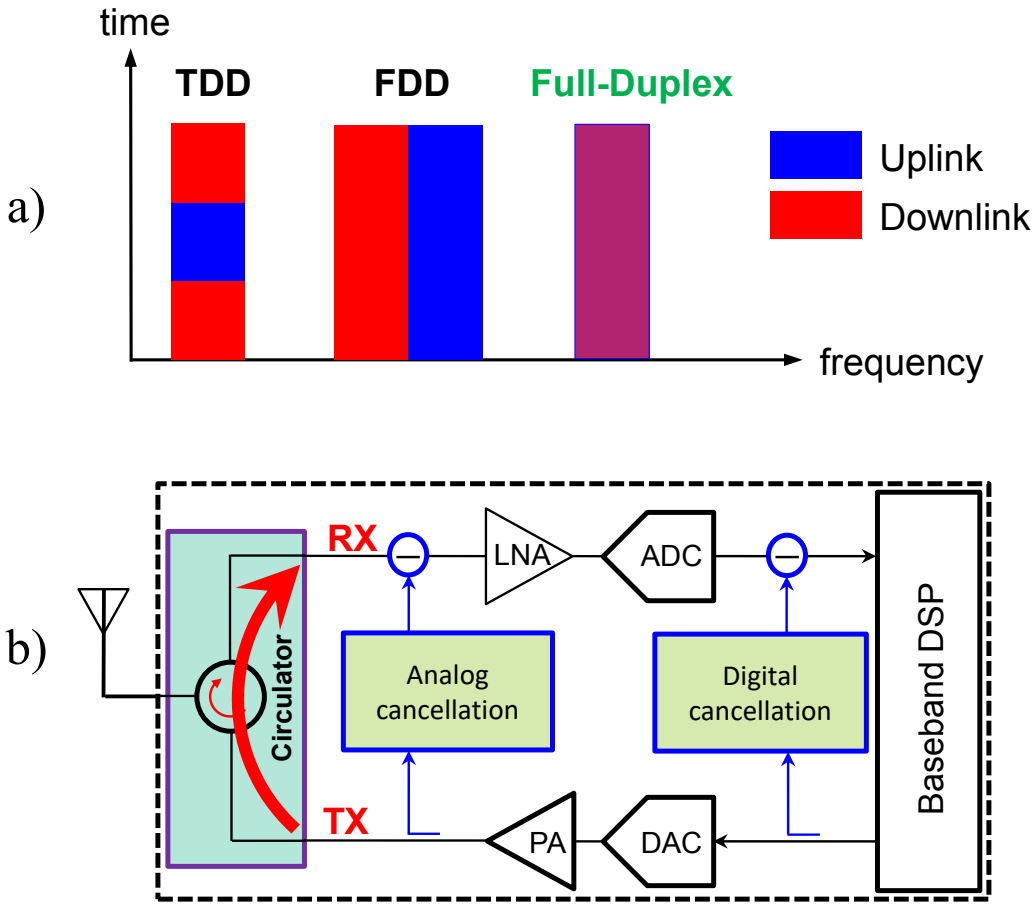


Figure 1.3: Frequency-Duplex in illustration in time-frequency a) and TX self interference to RX and classic rejection techniques [1].

As will be discussed in subsequent chapters, those classical techniques suffer from two issues: 1) Those technique reject the main component of TX-SI but any delayed copies

due to reflections post the antenna (environmental reflections) which can severely limit rejection and 2) it is often required by wireless standards to have a sensitivity that is much lower than -80 dBm demanding more than 120 dB of rejection by at least 20 dB.

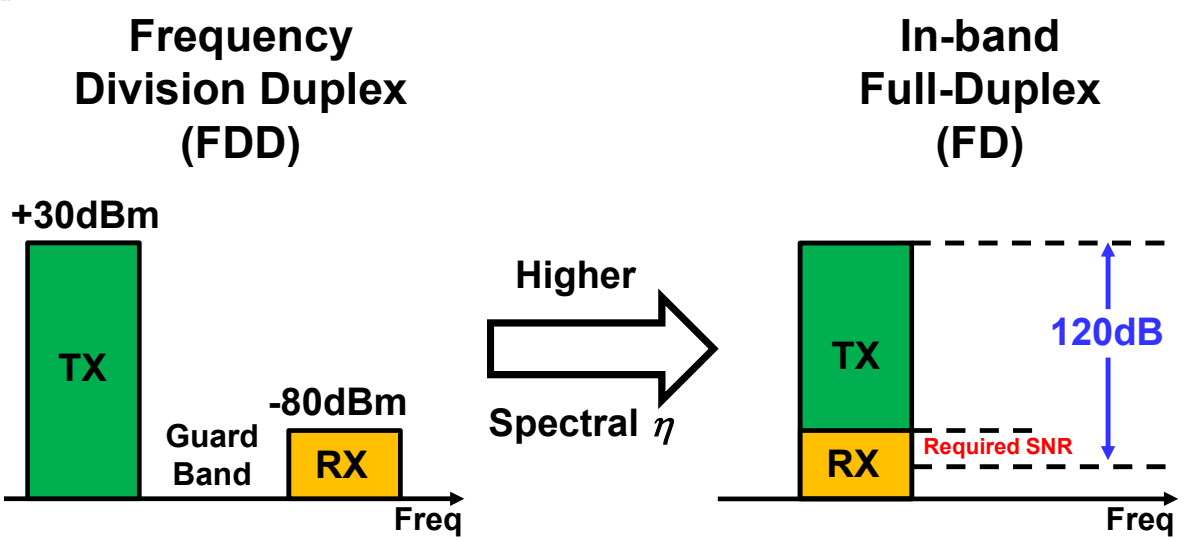


Figure 1.4: Frequency-Duplex in illustration in time-frequency a) and TX self interference to RX and classic rejection techniques [1].

1.2 Carrier Aggregation

Carrier aggregation (CA) is an attractive approach to increasing the data rate in wireless communication. In order to increase the data rate in wireless communication, two or more adjacent or non-adjacent RF channels can be joined together, thus proportionately raising the bandwidth and the capacity. Not only the data rate is increased, but due to the carriers having different frequencies and thus being independent, diversity of the link is increased and the performance is improved significantly as will be discussed later. In current state of the art carrier aggregation receivers (Fig. 1.5) separate receive chains are dedicated for each carrier location increasing the form factor significantly. Further more, separate Phase-Locked Loops (PLLs) or multiple Local Oscillators (LOs) are of-

ten needed to tune each RX increasing the power consumption significant.Furthermore, tuning a PLL is a slow process lowering the time response of the CA receiver considerably.

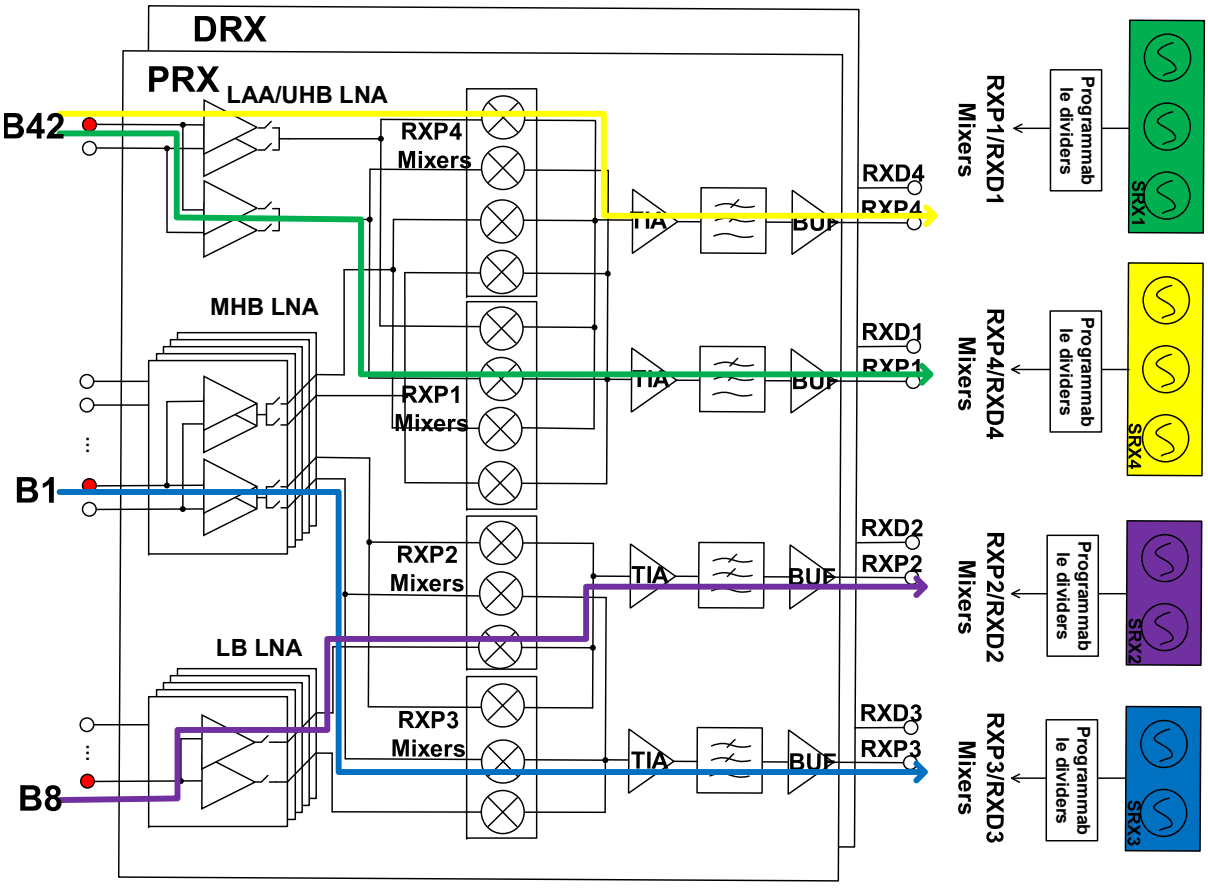


Figure 1.5: State of the art Carrier aggregation receiver with multiple branches [2].

1.3 Spectrum Sensing

As discussed before, the spectrum allocation is very crowded. On the other hand, users don't use the band very often. Fig. 1.6 shows the occupancy rate of various band near mobile range showing a significant portion of the spectrum not being used. In and out of band interferers can degrade the performance of the receiver due to various

reasons. By identifying and removing strong interferers in the wideband spectrum, the performance can be improved. Reliably detect the unoccupied spectrum band that can be exploited by the unlicensed secondary users can improve the spectrum utilization efficiency. State of the art spectrum sensing detect blockers passively without any rejection.

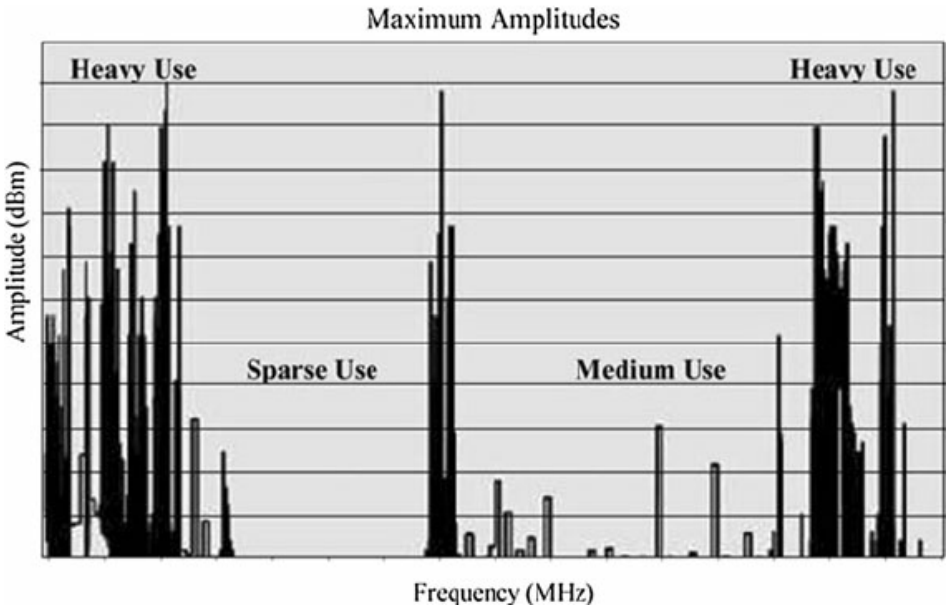


Figure 1.6: Spectrum occupancy [3]

1.4 Diversity Receivers

Unlike wired connections, wireless channel can provide multiple paths between the transmit and receive antenna. This can cause fading the RX antenna even when the SNR of the dominant path is high. Fig. 1.6 compares the probability of error P_e vs SNR of additive white Gaussian noise (AWGN) channel vs a wireless fading channel. In AWGN channel and when SNR is high enough, the performing is excellent and depends on SNR exponentially. On the other hand for a wireless channel, the multiple paths

provide an equivalent attenuation that can be characterized by an impulse response of the channel h(t). Theory expects the improvement in this case to be only inversely proportional to SNR. Fading is not the only challenge in wireless communication, as physical objects can block certain paths sometimes. Furthermore, moving antenna can change the channel completely causing deep fade to occur at some frequencies. Diversity techniques provide some independent "redundancy" improving the performance of the channel. This diversity is either in time, frequency or space. Chapter 6 is dedicated to a a frequency diversity front end with DSSS techniques.

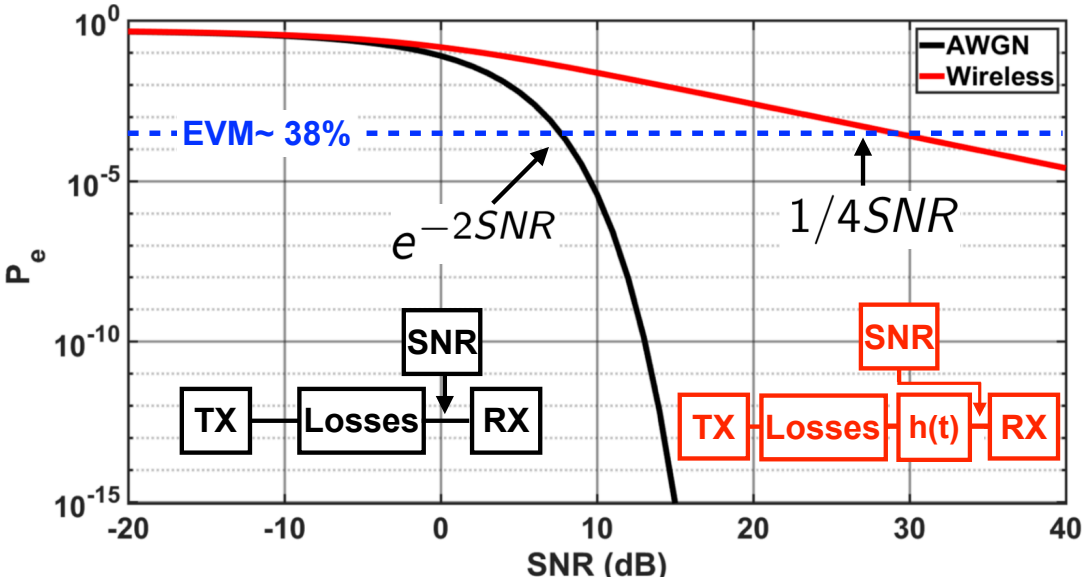


Figure 1.7: Performance of a wireless channel compared to additive white Gaussian noise channel [4].

1.5 Dissertation Organization

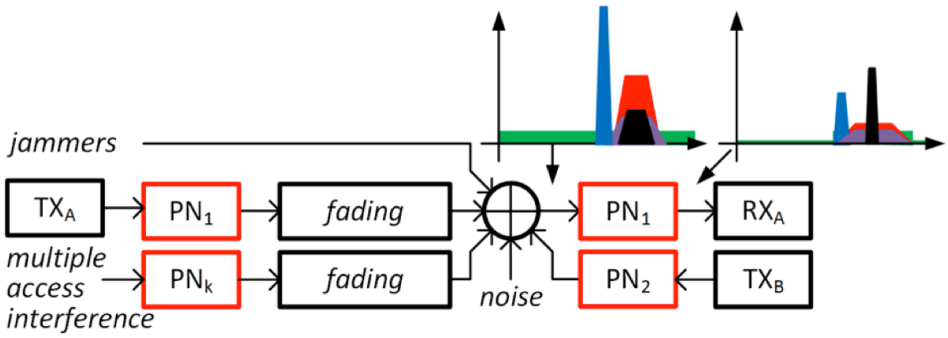


Figure 1.8: Illustration of DSSS techniques for modern transceivers.

This chapter provides an overview of challenges of wireless communications. Direct-Sequence Spread-Spectrum techniques use well known sequences (codes) that have noise-like properties. Fig. 1.8 illustrates some of the challenges of wireless communications and proposed solutions for modern transceivers. By modulating with a pseudo-noise (PN) code, the desired signal is spread (increased in BW). However, multiple spread signals can occupy the same BW thus enabling FD if each signal's code is orthogonal (low cross correaltion) to the other used codes. Also, using a wider BW of the signal lowers the possibility of deep fade. In addition to those attractive features, out of band jammers are rejected by the PN codes. Chapter 2 and Chapter 4 are dedicated to Full-Duplex communications based on DSSS techniques.

Modulating the LO with a PN code can cause the LO frequency to shift immediately without the need to re-calibrate the PLL saving time. Furthermore, the modualted LO (and depending on the PN code properties) can occupy multiple frequencies enabling Carrier Aggregation with one RX and one LO only. Chapter 3 is dedicated for CA with DSSS.

Spectrum Sensing is demanded for more efficient use of the spectrum. Chapter 5 is

dedicated for a spectrum sensing technique by injecting a PN code to mix with blockers at the same frequency (if any) to base-band through the non-linearity of the Low Noise Amplifier (LNA) allowing the detection with the same hardware and at much lower power consumption.

Chapter 6 is dedicated to a diversity technique by correalting with a non-binary code that resembles two propagation paths showing a resiliency against to either of the paths fading.

1.6 Permissions and Attributions

The content of chapter 2 was presented and published in the proceedings of the International Microwave Symposium (1MS) 2018 conference and expanded in the IEEE Transactions and Microwave Theory and Techniques (TMTT) in 2019. The content of chapter 3 is accepted to appear in the IEEE Journal of Solid State Circuits (JSSC). The content of chapter 4 was presented and published in the proceedings of the IEEE Radio Frequency Integrated circuits (RFIC) Symposium 2019 and was invited to appear IEEE JSSC journal in 2019. The content of chapter 5 is a result of a collaboration with Han Yan and Prof. Danijela Cabric from UCLA.

Chapter 2

Code-Selective Filters

2.1 Introduction

SCALED CMOS processes have enabled signal processing techniques to migrate towards the antenna by offering switch performance with low RF insertion loss, low gate power requirements and high bandwidth. Signal processing at the antenna could prove a key technology for simultaneous transmit and receive (STAR) systems where desired and undesired signals are filtered before a conventional receiver. For instance, a STAR technique based on direct-sequence spread-spectrum (DSSS) could enable full-duplex (FD) communication where the transmit (TX) signal falls within the receive (RX) band. Code-division multiple access for FD environment would encode data with a pseudonoise (PN) code of length M. Although the bit-rate R of each user is lower than the DSSS bandwidth $M \cdot R$, M users can share the spectrum due to the processing gain offered by the codes.

Here, CDMA is revisited to handle STAR transmit or user interference through code correlation at the antenna. Signal processing performed in the RF domain provides two advantages: 1) it rejects interference before the RF and baseband (BB) stages and 2)

it reduces the bandwidth of the signal before it is down-converted and digitized with an analog-to-digital converter (ADC) and relaxes the DSSS bandwidth to accommodate more users and higher signal bandwidth.

The proposed FD DSSS communication is shown in Fig. 1 where two transmitters produce a desired RX signal and undesired TX self-interference (SI) coded with PN codes C_1 and C_2, respectively, that potentially overwhelms the sensitivity of the receiver (RX). A code-reject code selective filter (CSF) coded with the code C_2 tags the TX signal and rejects it while passing the C_1 signal. The dual code-pass CSF passes the signal tagged with code C_1 while rejecting other signals including out-of-access jammers.

Prior work demonstrated transmit SI cancellation at various points in the RX chain. In [5], DSSS signal processming offers rejection of users sharing the same frequency. The rejection is limited by the finite on-resistance of the switch and requires large transistors to improve rejection. In [6][7], an integrated circulator was demonstrated using N-path Filters to offer between 20-40 dB of isolation at the antenna which relaxes the linearity of the low-noise amplifier (LNA). To overcome the sensitivity problem, extra rejection has been demonstrated at the mixer [5] by applying means of code-domain selectivity to the mixer (in this case an N-path Filter) providing up to 38.5 dB of SI cancellation. Cancellation in the analog path offers 20 dB of rejection [6].

CSFs distinguish themselves from previous work [5] (code-domain LNA/mixer) in two aspects: 1) The CSF produces either a low or high shunt impedance and thus does not correlate the RF signals (rather correlation is performed at base-band). 2) Due to the CSF having passive switches only, linearity can be much higher than previous work with IIP3 of -27 dBm mostly limited by the LNA. For those reasons, we propose the insertion of the CSF at the antenna to add extra rejection with the capability of handling high blocker power before the LNA/mixer as shown in Fig. 2.1. This paper extends earlier work that introduced the inverted shunt N-path and the code-selective

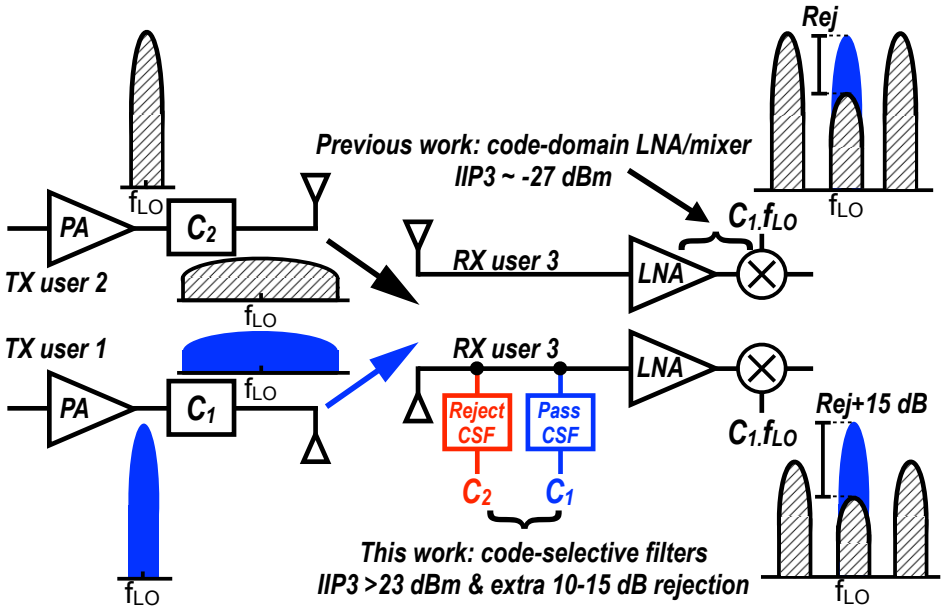


Figure 2.1: Code selective signal processing at RF front-end for STAR systems.

filter [8]. In SECTION II, we present the rejection and insertion loss for conventional N-path filters and present the $\lambda/4$ impedance-inverter using an N-path filter to improve the rejection and insertion loss in SECTION III. Here, the analysis shows that the rejection and linearity are improved. We develop an analytical expression for the input impedance of a CSF and compare this with simulation in SECTION IV. In SECTION V, we present expanded measurements of the CSF and inverted CSF are included for EVM, NF, LO spurious emission and rejection degradation as a function of signal bandwidth. Finally, a measured constellation of the CSF demonstrates processing gain and robust response against in-band jammers.

2.2 Review of N-path filters for TX rejection

CMOS-based N-path filters provide high quality factor (Q) band-pass [9] and band-reject [10] filter responses. The use of multiple band-pass and band-reject on the same

chip have been demonstrated and shows a combined response of both filters [11][12] and [12].

2.2.1 Shunt Band-Pass N-path filters

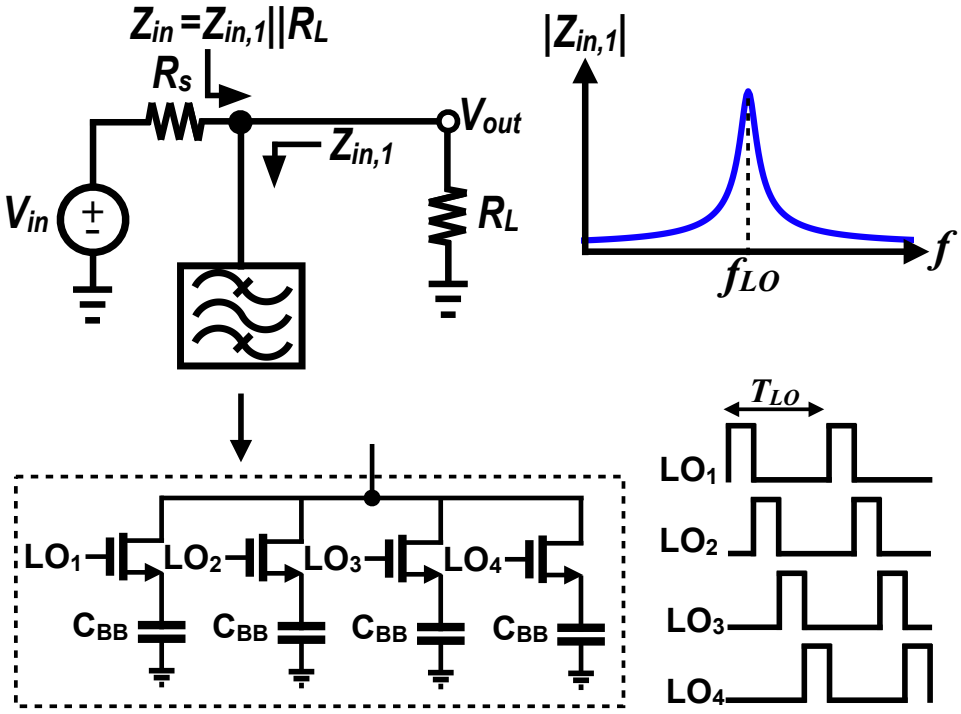


Figure 2.2: A shunt band-pass 4-path filter and its input impedance as a function of frequency.

A shunt 4-path filter is shown in Fig. 2.2 and consists of 4 paths each gated with a CMOS SOI switch and connected to a baseband capacitor. For RF frequencies offset from the LO frequency (f_{LO}), the filter produces a low impedance. Near (f_{LO}), the filter produces a large input impedance, producing a bandpass filter when connected along a 50-Ω transmission line. The input impedance of a 4-path filter [13] is given by

$$Z_{in}(\omega) = R_{SW} + R_{sh}||\frac{2}{\pi^2}Z_{BB}(\omega - \omega_{LO}), \tag{2.1}$$

where R_{SW} is the switch resistance. Appendix A shows a circuit-based derivation of R_{sh}. With approximations made near and well-offset from the LO, the input impedance becomes

$$Z_{in,1} = \begin{cases} \frac{8R+\pi^2 R_{SW}}{\pi^2-8} & f = f_{LO} \\ R_{SW} & f \not\approx f_{LO} \end{cases} \tag{2.2}$$

where $R = R_S||R_L$ is the impedance seen from the filter and R_{SW} is the switch on resistance. The insertion loss (IL) of a 4-path with a 50-Ω impedance ($R_s = R_L = 50\Omega$) is

$$IL = \frac{8R_S + 2\pi R_{SW}}{\pi^2 R_S + 2\pi R_{SW}}. \tag{2.3}$$

It should be noted that IL can be designed to be 0 dB by selecting an optimum value of R_L=R_{opt} [9], or choose R_L to be open [14]. However, the application illustrated in Fig. 1 uses a shunt filter cascaded with a radio chain in a 50 Ω impedance environment.

The rejection of a single-ended N-path filter is

$$REJ = \frac{R_{SW}}{2R_{SW} + R_S}. \tag{2.4}$$

In a 50-Ω environment, the N-path does not provide more than 15 dB of ultimate rejection [9]. The switch resistance can be reduced with a larger transistor size at the expense of higher switching power consumption at the gate.

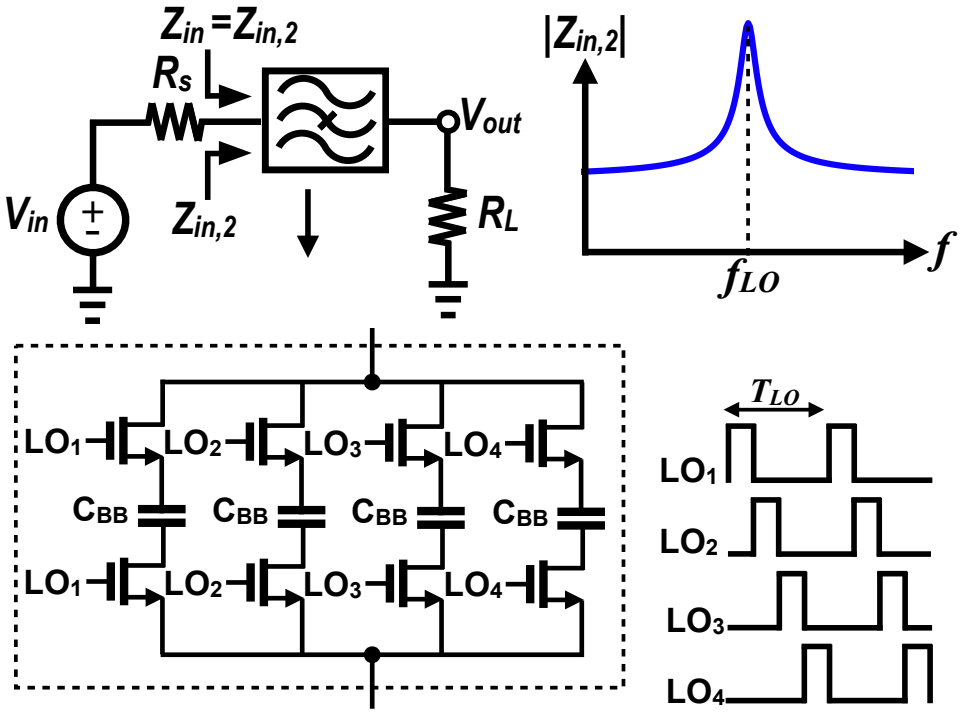


Figure 2.3: A series band-reject4-path filter and its input impedance as a function of frequency.

2.2.2 Series Band-Reject N-path filters

To improve the rejection, a series 4-path filter is shown in Fig. 2.3 and consists of a pair 4 switches with a series capacitor. When the f_{LO} is near the RF frequency, the filter produces a large impedance that will result in attenuation. For RF frequencies offset from f_{LO}, the filter produces a low impedance. Similar to a shunt 4-path, the impedance at f_{LO} is finite due to LO harmonics [9][10].

$$Z_{in,2} = \begin{cases} \frac{16}{\pi^2-8}R_S + \frac{2\pi^2}{\pi^2-8}R_{SW} + R_L & f = f_{LO} \\ 2R_{SW} + R_L & f \approx f_{LO} \end{cases} \tag{2.5}$$

Therefore, a series N-path filter needs twice the number of switches of a shunt N-path filter and the total width budget limits the power consumption.

$$R_{SW,SER} = 2R_{SW,SHU} \tag{2.6}$$

The IL of a series 4-path filter is

$$IL = \frac{R_S}{R_S + R_{SW}} \tag{2.7}$$

and the associated maximum rejection is

$$REJ = \frac{(\pi^2 - 8)R_S}{(\pi^2 + 8)R_S + 2\pi^2 R_{SW}}. \tag{2.8}$$

One of the most significant advantages of an N-path is the ability to tune over a decade using the LO frequency but in many systems the tuning range is not as important as the underlying performance, e.g. rejection, in a given band. For this reason, we propose to limit the tuning in favor of better rejection in the FD RF band.

2.3 Quarter-Wave Inverted N-path Filter

2.3.1 Theory of Inverted N-path filters

Previously, band-reject filters have been proposed using series N-path filters [9]. Here, we recognize that a quarter-wave $\lambda/4$ transmission line is inserted between the RF line and the shunt N-path filter, the impedance is inverted producing a band-reject filter as shown in Fig. 2.4 (N=4). The proposed approach constrains the tunability of the filter to the bandwidth of the impedance inverting network. However, the rejection will be shown to

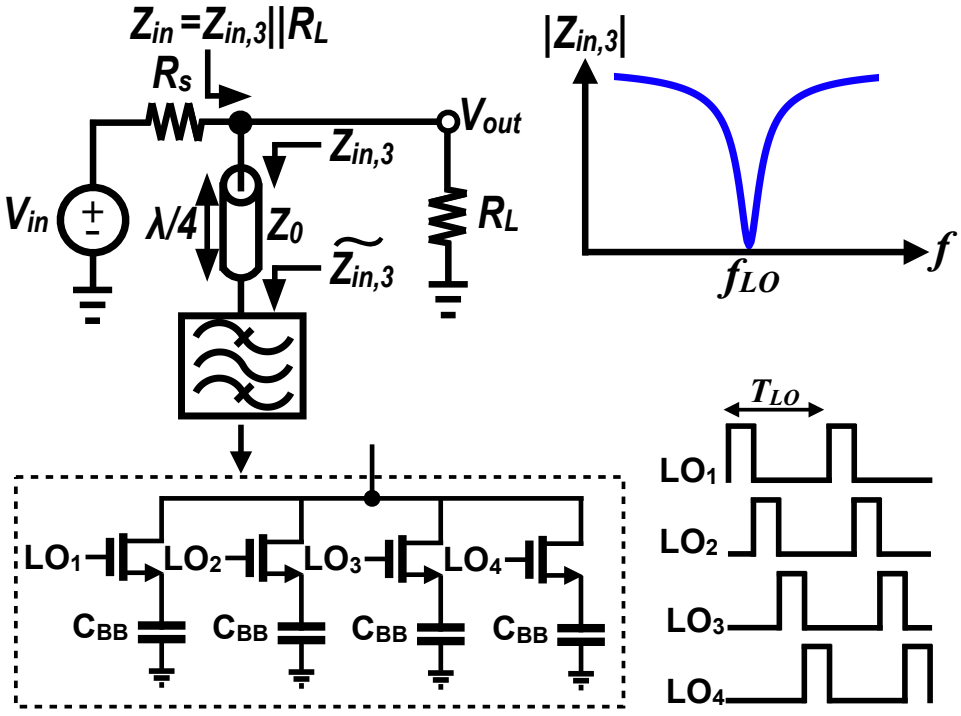


Figure 2.4: A quarter-wave inverted 4-path filter and its input impedance.

be independent of switch resistance and, therefore, the size of the switches. Additionally, the shunt N-path will subsequently implement a time-varying load impedance for code selective signal processing.

The input impedance near the LO frequency for a $\lambda/4$ impedance inverter [15] with a 4-path filter as the load is

$$\widetilde{Z_{in,3}}(f = f_{LO}) = \frac{16Z_o^2 + \pi^2 R_{SW} R_s}{(\pi^2 - 8)R_s}. \tag{2.9}$$

The impedance seen at the RF line is

$$Z_{in,3}(f = f_{LO}) = \frac{Z_o^2(\pi^2 - 8)R_s}{16Z_o^2 + \pi^2 R_{SW} R_s}. \tag{2.10}$$

The rejection is calculated is

$$REJ = \frac{Z_o^2(\pi^2 - 8)}{2Z_o^2(\pi^2 - 8) + 16Z_o^2 + \pi^2 R_{SW} R_s} \tag{2.11}$$

and can be compared to (2.4). Larger choices of N might be chosen to improve the rejection [16]. For frequency bands offset from f_{LO},

$$Z_{in,3}(f \not\approx f_{LO}) \approx \frac{Z_O^2}{R_{SW}}. \tag{2.12}$$

Now, a small R_{SW} realizes a large input impedance as seen from the transmission line and does not attenuate signals and the insertion loss is

$$IL \approx \frac{1}{1 + \frac{R_{SW} R_s}{2Z_o^2}}. \tag{2.13}$$

Note this resembles the IL found in (2.7).

2.3.2 Comparison with N-path filters.

Fig. 2.5 shows the theoretical and simulated IL and rejection of a band-pass 4-path and an inverted 4-path filters as a function of R_{SW}. Comparing the theory and simulation indicates strong agreement over a range of assumed switch resistances. slight difference can be explained as follows. First, in theory the switch resistance is fixed while in simulation the switch resistance depends on the LO waveform and thus the nonzero rise and fall times result in a switch resistance slightly larger than expected. Second, the parasitic capacitance in the components' models is captured in simulation resulting in higher losses compared to theory. As R_{SW} increases the inverted N-path maintains a flat ultimate rejection unlike the band-pass shunt N-path filter where the rejection degrades.

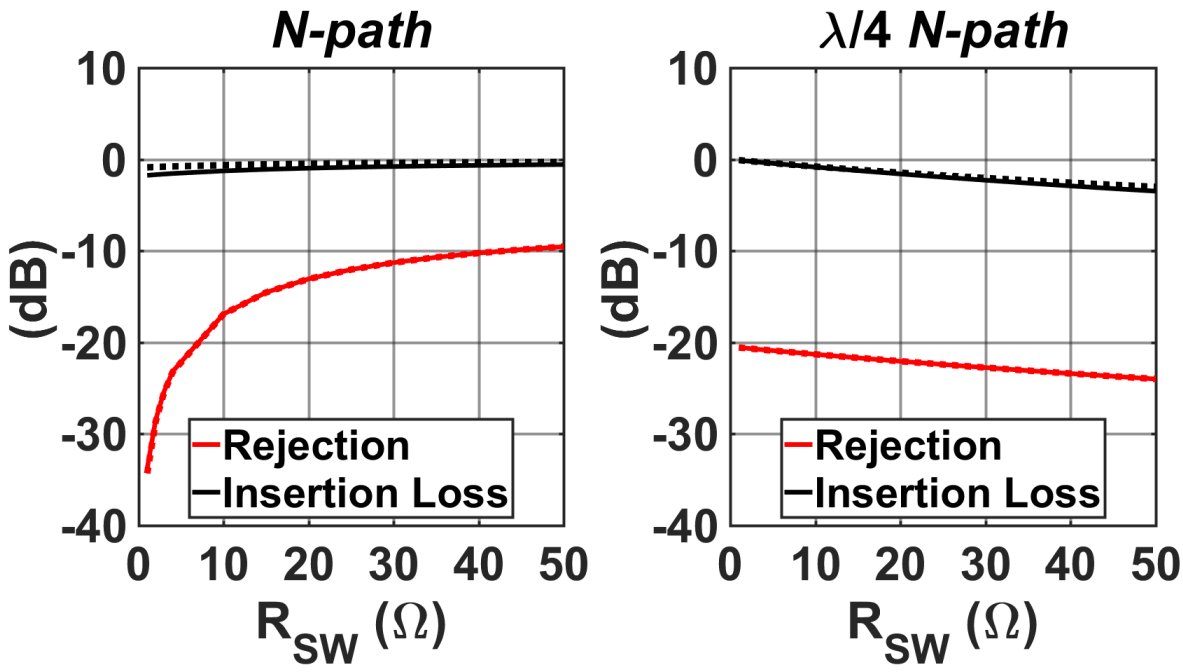


Figure 2.5: IL and rejection comparison between Inverted 4-path and band-pass shunt 4-path. Simulation in solid and theory in dashed.

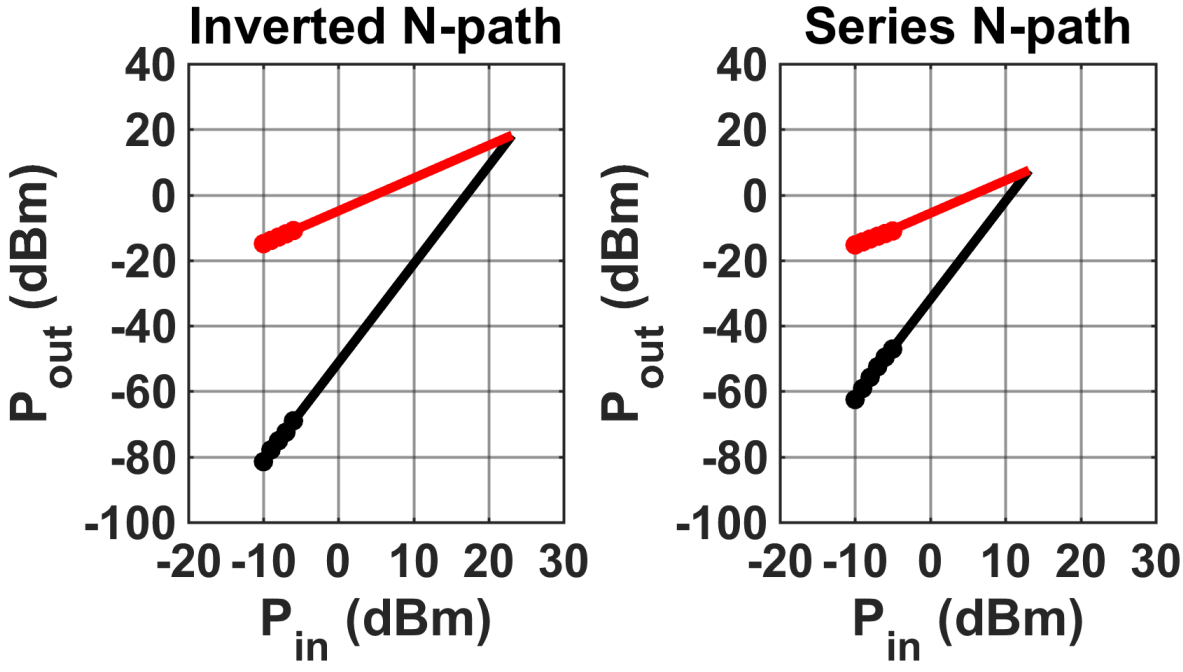


Figure 2.6: A linearity comparison between Inverted 4-path and series 4-path in simulation.

Therefore, the impedance-inverted filter provides a rejection that is relatively robust to switch resistance variation.

Fig. 2.6 shows a two-tone (IIP3) simulation of a band-reject series 4-path and an inverted 4-path filters for a fixed switches size and BB capacitance. For input tones at 700 MHz and 800 MHz, the IM3 tone is at 900 MHz while a 10 MHz notch occurs at f_{LO}=1 GHz. We find the out of band IIP3 of the inverted 4-path filter is 10 dB higher than the series 4-path filter since the series switches see the large signal swing while the $\lambda/4$-wave line inverts the voltage seen at the switches. Furthermore, an inverted N-path filter requires half the number of switches compared to the series N-path filter.

2.4 Code-Selective Filters

2.4.1 Theory of Code Selective Filters

While the N-path filters are inherently frequency selective, the filters can be reconfigured to process signals in a code domain [17][5]. Here, we compare code selective filters for code pass and code reject operations. To demonstrate these operations, we compare the impedances generated with different code sequences. Fig. 7 illustrates two ways to implement a code selective filter. The first is a code-pass filter that passes one code C_1 and rejects another code C_2. The rejection depends on the cross-correlation between C_1 and C_2. The second is a code-reject filter that is realized by adding a $\lambda/4$ transmission line as discussed in SECTION III to reject any signal with matching codes. Earlier work reported N-path filters driven by PN codes to mitigate LO spurious leakage [17]. The codes rapidly switched on and off two sets of switches depending on the code level. Since the code modulation is applied at the switch, this scheme can be described as a "Hard-switching" scheme. In [5], down-conversion rejection is demonstrated by modulating the

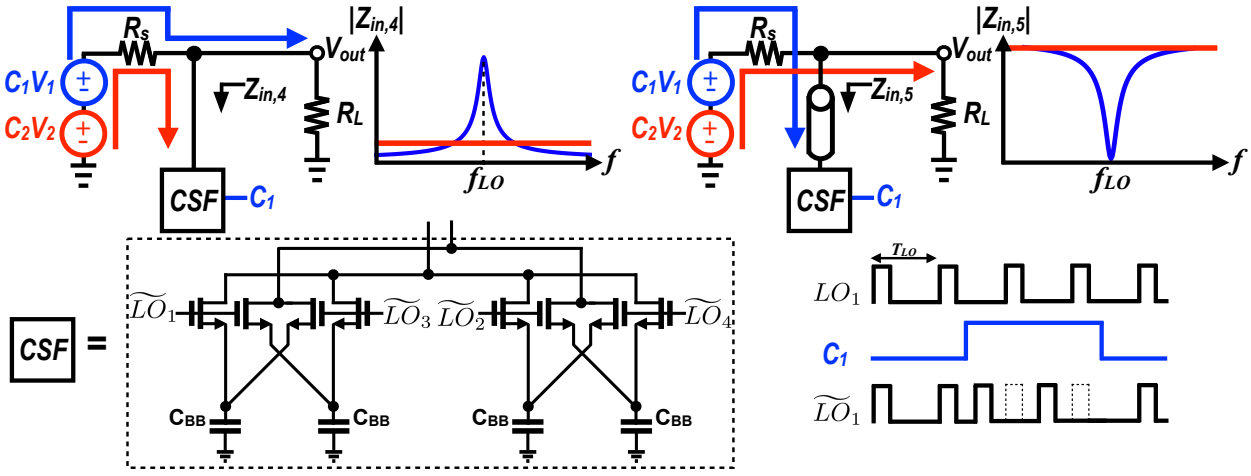


Figure 2.7: Pass and reject code selective filters and their input impedances.

2xLO of the mixer with a PN code that is generated off-chip. Since this scheme requires the use of only the original set of switches, it can be described as "Soft-switching". Here, we show that the hard-switching and soft-switching approaches produce the same code-selective impedance. A 25% duty cycle clock is shown in Fig. 2.7 and can be represented [13] as:

$$LO_i(t) = \begin{cases} 1 & \text{if } (k + \frac{i-1}{4})T_{LO} < t < (k + \frac{i}{4})T_{LO} \\ 0 & \text{elsewhere} \end{cases} \tag{2.14}$$

where $k \in Z$. $LO_i(t)$ has the equivalent Fourier series:

$$\sum_{n=-\infty}^{\infty} (-j)^{n(i-1)} b_n e^{jn\omega_{LO}t}, \text{ where } b_n = \frac{\sin n\frac{\pi}{4}}{n\pi} e^{jn\frac{-\pi}{4}}. \tag{2.15}$$

Defining a binary PN sequence α of length M (i.e $\alpha[n] \in \{0,1\}^M$). Now, the code

sequence $C_\ell(t)$ is the weighted sum of pulses.

$$C_\ell(t) = \sum_{k=1}^{M} \alpha[k] S_k(t), \tag{2.16}$$

where a pulse of period T_c is

$$S_k(t) = \begin{cases} 1 & \text{if } kT_c < t < (k+1/M)T_c \\ \\ 0 & \text{elsewhere.} \end{cases} \tag{2.17}$$

The equivalent Fourier series is expressed as

$$\begin{aligned} C_\ell(t) &= \sum_{m=-\infty}^{\infty} \sum_{k=1}^{M} \alpha[k](-j)^{\frac{4m(k-1)}{M}} a_m e^{jm\frac{\omega_c}{M}t} \\ &= \sum_{m=-\infty}^{\infty} \hat{a_m} e^{jm\frac{\omega_c}{M}t} \\ &\text{where } a_m = \frac{\sin m\frac{\pi}{M}}{m\pi} e^{jm\frac{-\pi}{M}}. \end{aligned} \tag{2.18}$$

We define the code-modulated $\widetilde{LO}(t)$ from positive LO pulses when $C_\ell(t) = 1$ and the negative LO pulses when $C_\ell(t) = 0$.

$$\widetilde{LO}_i(t) = C_\ell(t) LO_i(t) + (1 - C_\ell(t)) LO_i(t - \frac{T_{LO}}{2}) \tag{2.19}$$

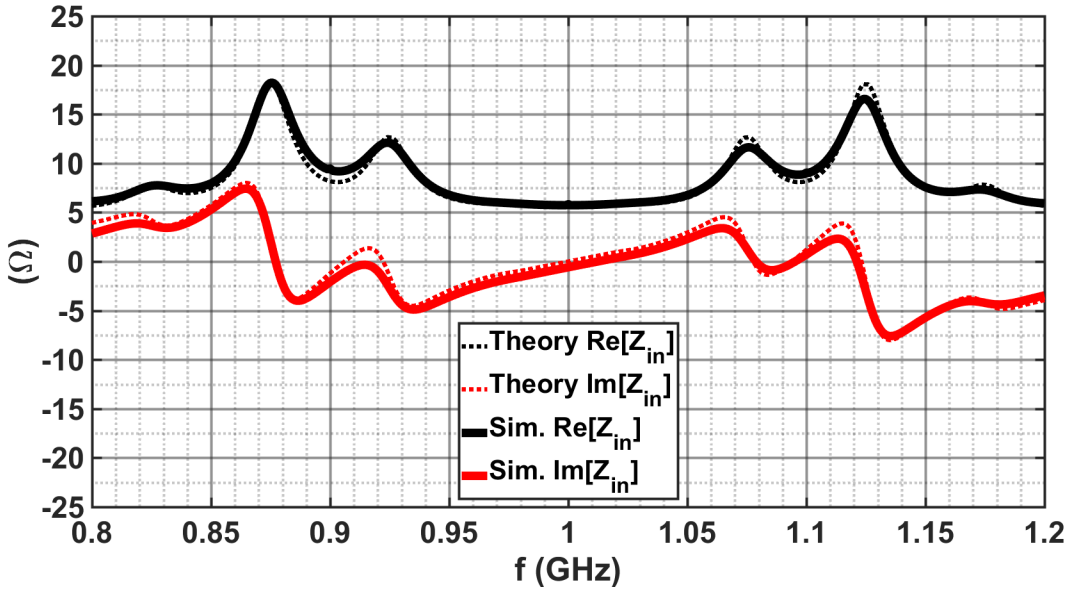


Figure 2.8: Analytical impedance from (2.22) compared to simulation (PSS+PSP) of the input impedance for CSF.

and has the following Fourier series expansion:

$$\widetilde{LO}_i(t) = \sum_{n=-\infty}^{\infty} \sum_{k=1}^{M} \sum_{m=-\infty}^{\infty} \Bigg\{ [\alpha[k] + (-1)^n (1 - \alpha[k])] \\ [(-j)^{n(i-1)+\frac{4m(k-1)}{M}}][b_n a_m e^{j(n\omega_{LO}+\frac{m\omega_c}{M})t}] \Bigg\}. \tag{2.20}$$

To simplify analysis, we make the following assumptions.

1) The baseband impedance $Z_{BB}(\omega)$ provides attenuation at the LO and its harmonics. In other words, we can exclude all terms in (2.20) for n$\neq \pm 1$.

2) Similarly, we design Z_{BB} to provide attenuation at the harmonics of f_c for proper correlation. In other words, we can exclude all terms in (2.20) for $m > |\frac{M}{2}|$.

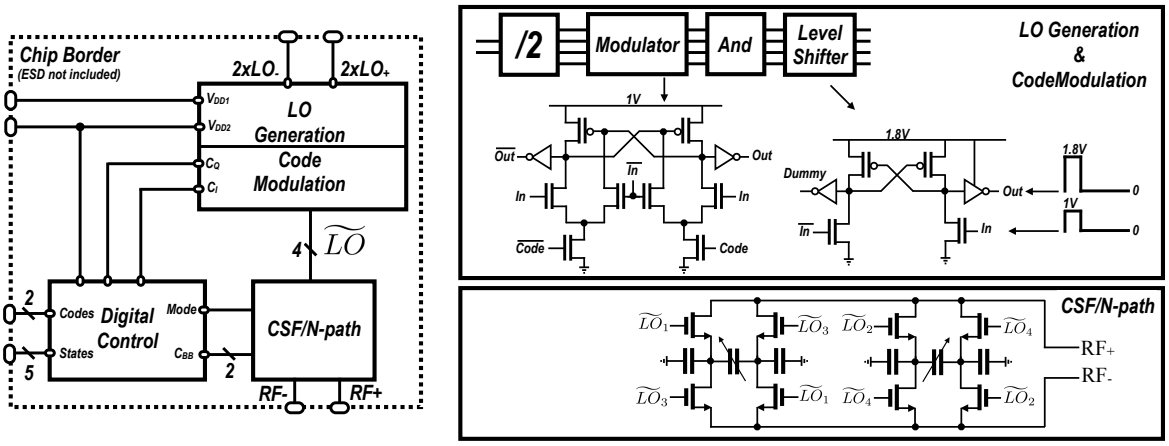


Figure 2.9: Implementation of the proposed filters.

These assumption allow the following simplification for (2.20):

$$\widetilde{LO}_i(t) \approx \sum_{k=1}^{M} \sum_{m=-\frac{M}{2}}^{\frac{M}{2}} \Bigg\{ [2\alpha[k]-1][(-j)^{\frac{4m(k-1)}{M}}] \\ [a_m e^{j\frac{m\omega_c}{M}t}][\frac{2}{\sqrt{2}\pi}\sin(\omega_{LO}t-(i-1)\frac{\pi}{4})] \Bigg\} \tag{2.21}$$

We observe that while we started with a binary sequence $\alpha[k]$ the term $2\alpha[k]-1$ in (2.21) is a linear mapping from $\{0,1\}^M \rightarrow \{-1,1\}^M$. Additionally, the PN modulation is captured by the terms $\hat{a_m}$ and, as a result, the input impedance looking into the CSF is a modulated and spread impedance of an N-path filter.

$$Z_{in}(\omega) = R_{SW} + \\ \sum_{m=-\frac{M}{2}}^{m=+\frac{M}{2}} (\hat{a_m})^2 R_{sh} || (\beta \frac{2}{\pi^2} Z_{BB}(\omega - \omega_{LO} + \frac{m\omega_c}{M})) \tag{2.22}$$

where β is the number of nonzero $\hat{a_m}$'s for a given code.

The input impedance indicates components that depend on the N-path circuit parameters modulated by the Fourier components of the code sequence. For instance, a

Walsh_1 code (which is the case of a classic N-path) has $\hat{a_m} = \delta[m]$ and thus $\beta = 1$. This simplifies (2.22) to (2.1). Fig. 2.8 compares theory to simulation (periodic steady state and periodic S-parameters) of a Walsh_{12} code.

Fig. 2.8 compares the real and imaginary parts of the input impedance for a particular Walsh code from (2.22). Circuit parameters include $R_S = 50\Omega$, $R_{SW} = 5\Omega$, $\text{C}_{BB} = 100$ pF and $T_c = 2.5$ ns. Clearly, the impedance from the analytical solution closely matches the simulation supporting the assumptions that were made. Near the LO frequency (1 GHz), the real part of the impedance becomes zero while the imaginary part of the impedance dominates the impedance. The equations derived in this SECTION apply to any family of codes. For example, Appendix B lists members of Walsh_{16} family. A complete graph of the impedances produced for an $M = 16$ length Walsh code is plotted in Appendix B. Although some of the codes produce the same impedance (e.g Walsh_6 and Walsh_8), these codes are orthogonal to each other and provide rejection when correlated as we will discuss in the measurements section. This orthogonality is preserved due to the phase shift between the codes.

2.4.2 Implementation of Code Selective Filters

Fig. 2.9 provides a detail of a *4*-path/CSF block diagram that can be used to operate in code-pass and code-reject modes.

The baseband impedances (Z_{BB}) are digitally-controlled, differential baseband capacitors (7.5 pF) in parallel with shunt capacitors (80 pF) providing a hybrid capacitance [16]. The differential caps provide better capacitance density however they are vulnerable to common mode noise and LO leakage. The shunt capacitors provide high capacitance to ground to shunt any common mode noise and leakage. Both capacitors are implemented with high density MIM caps. To provide high-linearity, thick-oxide NFETs are used for each of the switches with W/L=100μm/112nm. This high linearity is attributed to capability to handle larger LO swing.[16] The LO generation and code modulation are also shown. We implement the LO divider similar to [18] and the novel LO modulator (A differential XOR gate) is chosen to resemble the logic of the Divider. To provide the high LO swing and utilize the fast thin gate oxide switches, we chose to implement the core divider with thin gate transistors supplied with a 1-V while changing the high level of the waveforms before the switches with a level shifter. Without the level shifter, the intermediate LO will fail to drive the last inverter supplied with 1.8V [19]. To control the chip, a digital control takes in 5 state signals that selects the filter mode (i.e 4-path or CSF) as well as changing the differential capacitor value for BW tunning.

2.5 Measurements

The circuit is implemented in 45RF SOI CMOS (Stack 18) and occupies a chip area of 1.73 mm^2. The RFIC is reconfigurable based on the LO frequency and the code sequence. The RFIC can be tested as a code-reject or code-pass filter depending on the implementation. To evaluate the code reject operation, the RFIC is mounted on a printed circuit board (PCB) referred to as PCB1 with a quarter-wave transmission line to realize the impedance inverter. The RFIC is also mounted on a second PCB (referred to as PCB2) without the quarter-wave impedance inverter to test the code-pass response

as shown in Fig. 2.10. The chip consumes 6.18 mW from 1-V and 1.8-V supplies for 4-path mode and 9.37 mW for CSF mode both at $f_{LO} = 1$ GHz.

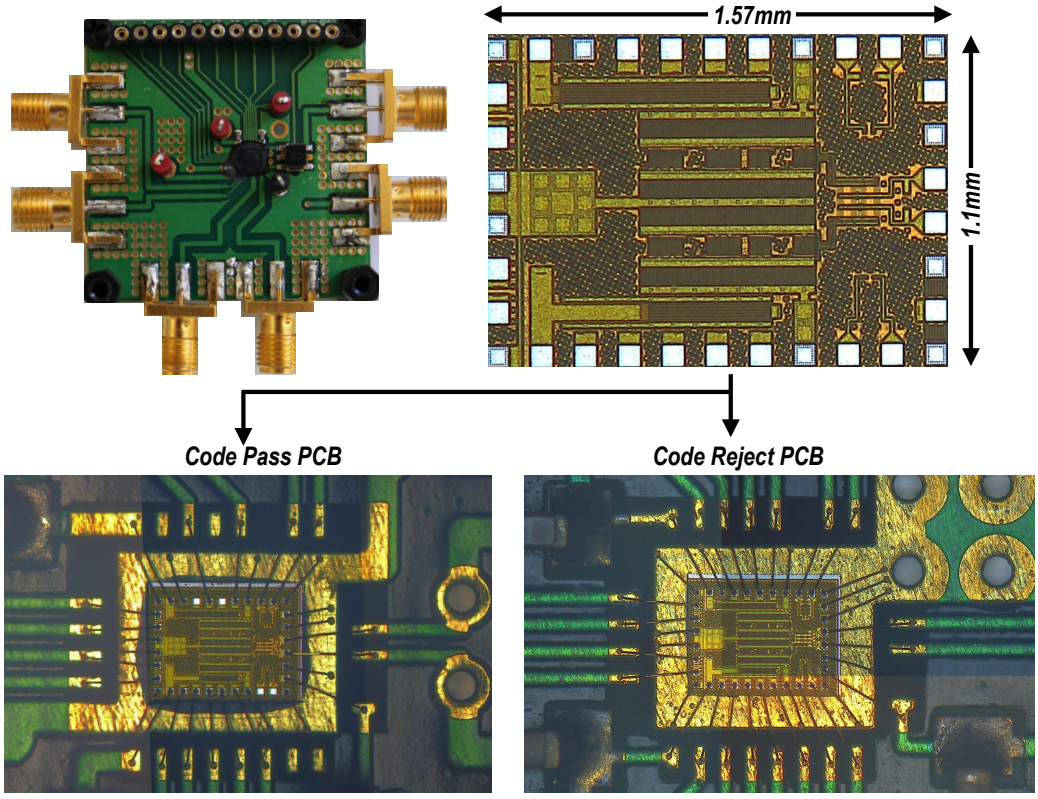


Figure 2.10: Chip micrograph and two PCB test set-ups.

2.5.1 S-Parameters of N-path Bandpass and Bandreject Response

For the chip mounted on PCB2, the measured S_{21} and S_{11} of the 4-path bandpass response are plotted in Fig. 2.11 (top). The insertion loss is 3.2 dB including the input and output off-chip baluns. While the LO tuning range covers 0.45 to 1.1 GHz (restricted by external baluns), the out-of-band rejection remains only around 15 dB across most of the band. S-parameters are compared to simulation in Fig. 2.11 (lower left). Also Fig. 2.11 plots the measured S_{21} and S_{11} of the N-path filter as a function of the digital

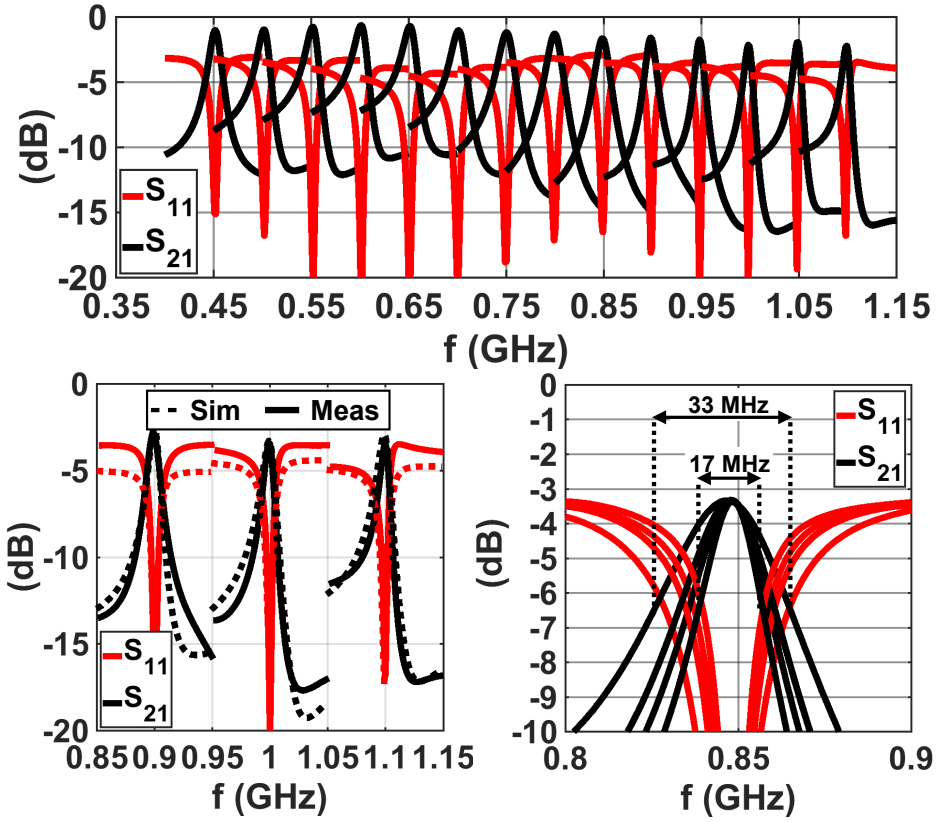


Figure 2.11: Measured S-parameters for the band-pass 4-path filter while sweeping f_{LO}.

control of the baseband capacitance (lower right). The tuned 3-dB bandwidth of the peak was measured to be 17 MHz to 33 MHz.

For the chip mounted on PCB1, the measured S_{21} and S_{11} of the inverted 4-path bandreject response are plotted in Fig. 2.12 while sweeping f_{LO} from 0.9 GHz to 1.1 GHz. The out-of-band insertion loss is around 3 dB. The tuning range in this case is limited to 200 MHz due to the fractional bandwidth of the quarter-wave line. The rejection exceeds 20 dB, and better than 10 dB over a 10 MHz bandwidth from 900 MHz to 1.1 GHz (top) and compared to simulation (lower left). Fig. 2.12 also shows the measured S_{21} and S_{11} of the inverted N-path filter when f_{LO} is 1 GHz while changing the digital control of the baseband capacitance value. The tuned 3-dB bandwidth of the notch was measured to be 12 MHz to 25 MHz.

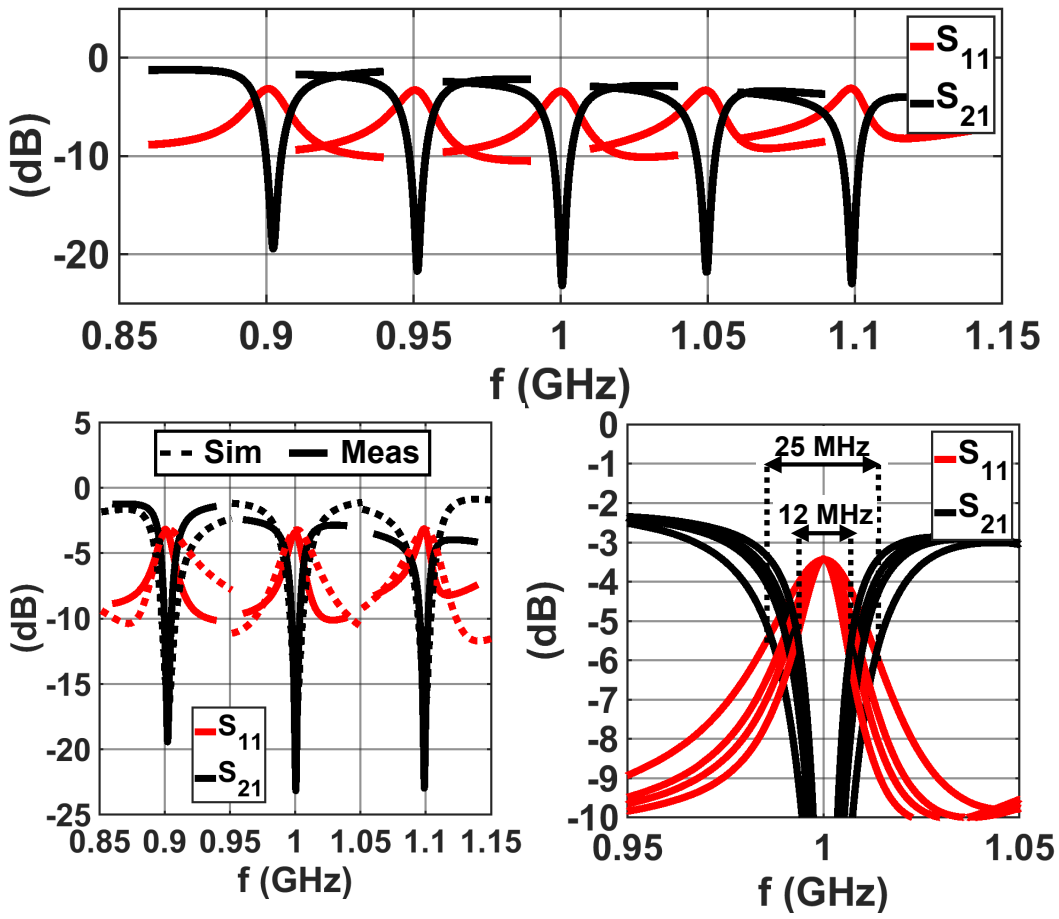


Figure 2.12: Measured S-parameters for the band-reject 4-path filter while sweeping f_{LO}.

2.5.2 S-Parameters of the Code-pass and Code-reject Filter

The S_{21} for the code-pass and code-reject responses are measured with orthogonal codes plotted in Fig. 2.13 when f_{LO} is tuned at 1 GHz when codes are enabled (CSF-mode, right of the figure) vs disabled (4-path mode, left of the figure). For code-reject operation (top), an orthogonal code should pass with an insertion loss that is approximately the same as the bandpass filter. The code reject filter is tested on PCB1 and the measured S_{21} is and the code applied to the RFIC is Walsh_2. The network analyzer is providing a CW signal (Walsh_1).

For code-pass operation (lower), an orthogonal code should be rejected. The code pass

filter is tested on PCB2 and the measured S_{21} is plotted when the applied code is Walsh_{16}. Also, S_{21} shows that the filter is rejecting all signals around f_{LO} due to the fact that each tone applied by the network analyzer is a CW tone and orthogonal to the filter's code with more than 10 dB of rejection. Around f_{LO}, the code-pass CSF rejects any out-of-band tone with rejection of around 15 dB. All measurements are compared to simulation and theory. Theory doesn't include the back-to-back baluns models and shows a symmetric response around f_{LO} and causes a slight deviation between theory and measurement at out of band frequencies. Simulation includes the back-to-back baluns models and thus is closer to measurement, nevertheless, the S_{21} remains consistent between theory, simulation and measurements.

2.5.3 Code Selectivity

The network analyzer provides limited capability to test code reject and code pass behavior in the CSF. To generate a code-modulated test tone, an M8195 Arbitrary Wave Generator (AWG) produces a Walsh code modulated RF signal. The test tone is passed through the PCB with he shunt filter (both code-pass and code reject PCB's), then terminated by an N9030B Spectrum Analyzer to measure power at different modes.

The frequency spectrum is shown in Fig. 2.14 when the input RF signal is a 1-GHz CW tone modulated with 13-length Barker code. In 4-path operation, the filter produces cancellation limited to the bandwidth of 20 MHz near f_{LO} as predicted by the notch characteristic in Fig. 2.11. Next, modulating the LO with a Walsh code allows the signal to pass with no rejection due to code orthogonality. When the RF input signal is modulated by a 13-length Barker code, the rejection extends across the spread-spectrum signal bandwidth of more than 300 MHz. In this case, the TX ultimate rejection, the difference between the insertion loss and the rejection, is 18.6 dB.

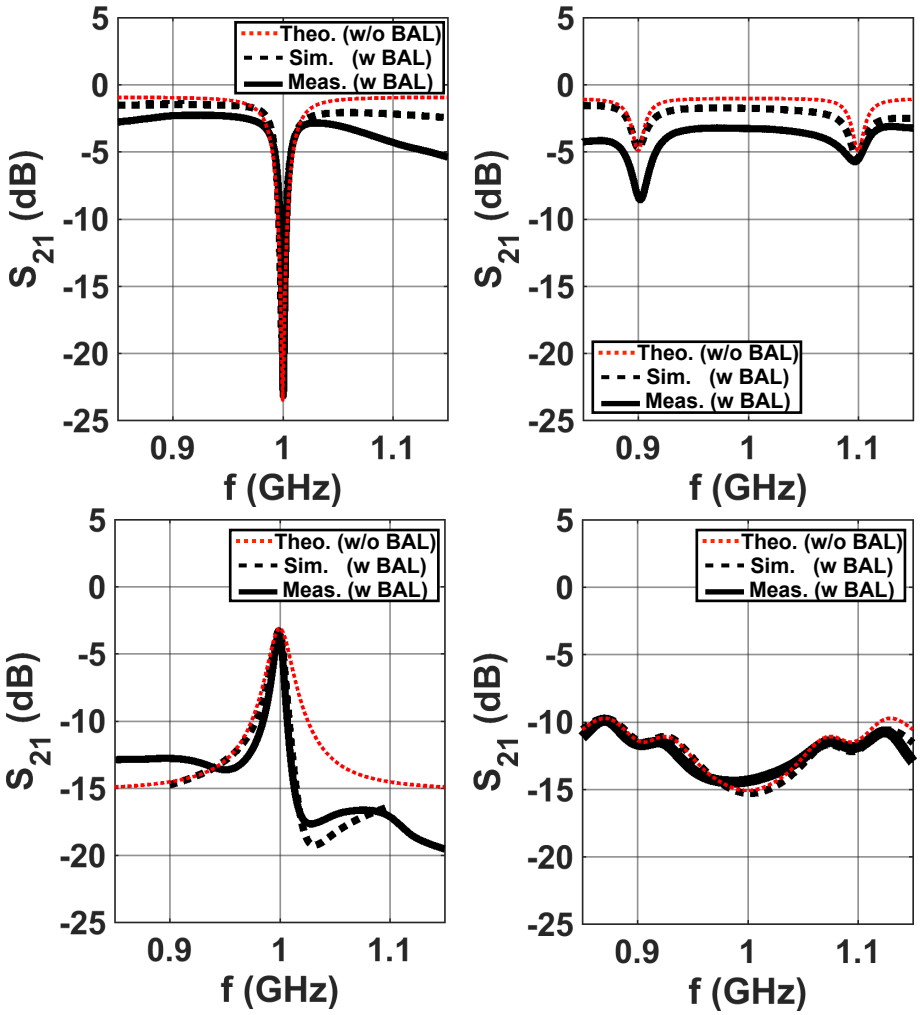


Figure 2.13: Measured S-parameters compared to simulation and theory for different modes at f_{LO}= 1GHz.

As the signal BW of the CW surpasses the max rejection BW (3-dB BW is 12 MHz), the rejection of the inverted CSF starts to degrade. Fig. 2.15 shows this degradation is less than 1 dB for a data rate of 1.92 Mbps.

Code selective operation in code-pass mode is illustrated in Fig. 2.16. A test CW tone at 0.85 GHz modulated with Walsh_{16} code. When the filter is disabled, the measured spectrum is shown with estimated loss of 1.2 dB (back-to-back baluns). When the code-pass filter is coded with the same code, the filter passes the signal with 2-dB IL. The

S_{21} measurement of total IL of around 3dB. When the filter is behaving as a classical 4-path, the rejection doesn't include tones close to f_{LO}=0.85 GHz and limited to around 10.7 dB. Finally, when the code-pass CSF is coded with an orthogonal Walsh$_7$ code, the response shows a rejection of 15.1 dB across the a 200MHz BW. The input power is -19 dBm to which all powers shown in Fig. 2.16 are normalized.

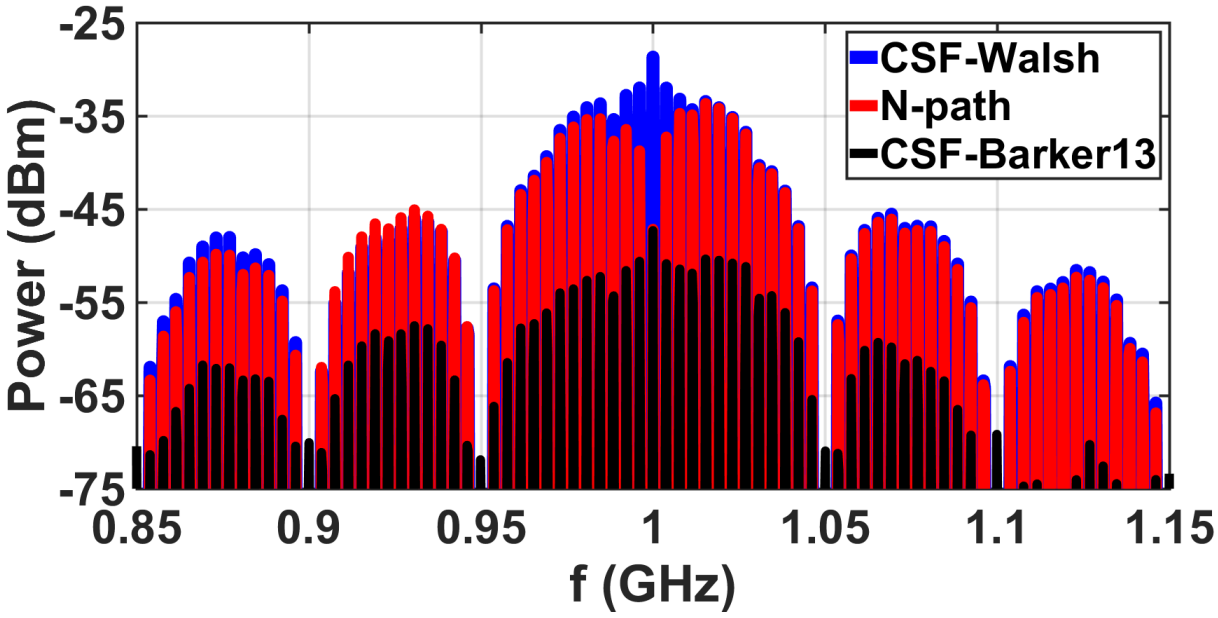


Figure 2.14: Measured RF spectrum power at code-reject CSF output for matched and unmatched codes and 4-path mode. The input is modulated with a Barker$_{13}$ code.

2.5.4 IIP3 and NF

The linearity of the inverted 4-path is tested with two tones at 999 MHz and 1000 MHz where f_{LO}=1.1GHz. Fig. 2.17 shows the in-band (of the receiver) IIP3 is 22.6 dBm. The CSF is tested with two tones at 999 MHz and 1001 MHz and Fig. 2.18 shows the IIP3 of the CSF vs f_{LO} and shown to be better than 23 dBm for a tunning range of 0.6 GHz.This high IIP3 is attributed to the thick-oxide based switches' capability of handling high LO swing. While previous work [16] implement all the digital logic in

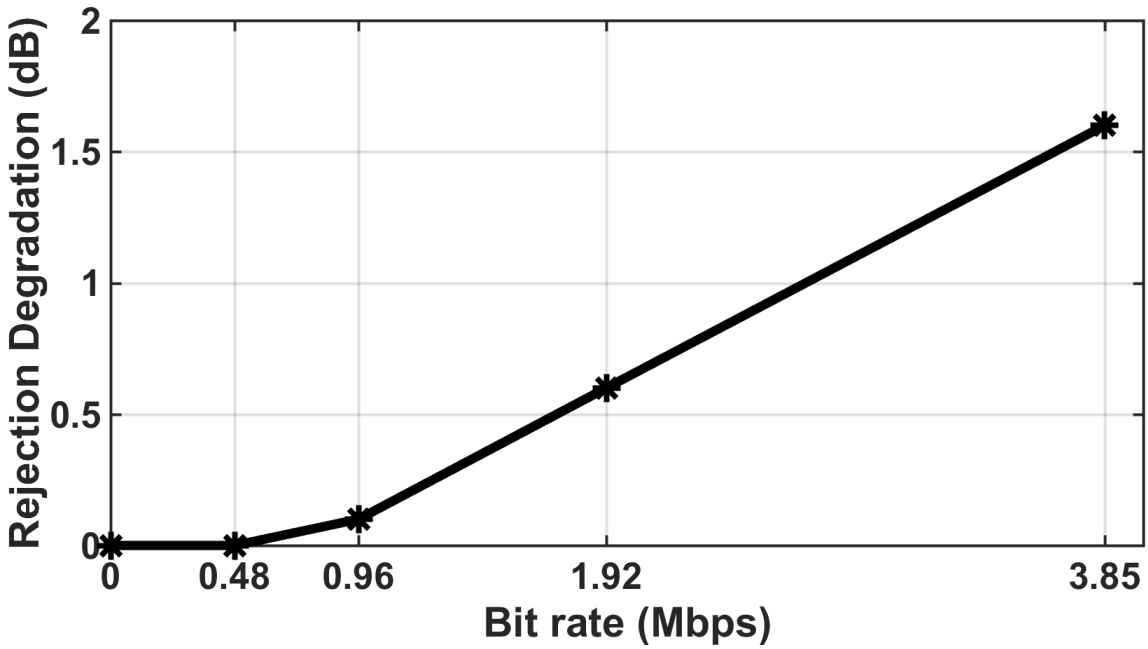


Figure 2.15: Tx rejection degradation vs signal bandwidth.

thick oxide connected to high-V_{DD} thus increasing the power consumption significantly ($\propto C_L V_{DD}^2$), here the digital level shifte (Fig. 2.9) allows high IIP3 with minimum power consumption. LO spurious emission is a known issue with N-path filters at the front-end. Earlier work suggests PN modulation of the clock can mitigate spurious emissions [17]. Fig. 2.19 plots a spectrum of the LO leakage for the inverted 4-path mode and measures LO leakage less than -70 dBc. After applying a Barker_{13} code, the LO spectrum is shown to be spread and, as a result, reduced by around 10 dB. Fig. 2.20 plots the measured NF. When the filter is behaving as an inverted 4-path, NF is about 4 dB. Around f_{LO}, the NF increases due to the notch in the frequency response as observed in a series N-path filter [9]. When a Walsh_{16} code is applied, the noise figure is constant across the frequency band at around 6 dB. The effect of phase noise and reciprocal mixing is a observed in N-path filters when applying a blocker at offset frequency from f_{LO} [18]. The noise contribution of the 4-path/CSF can be shown as follows: 1) The main contributor is the

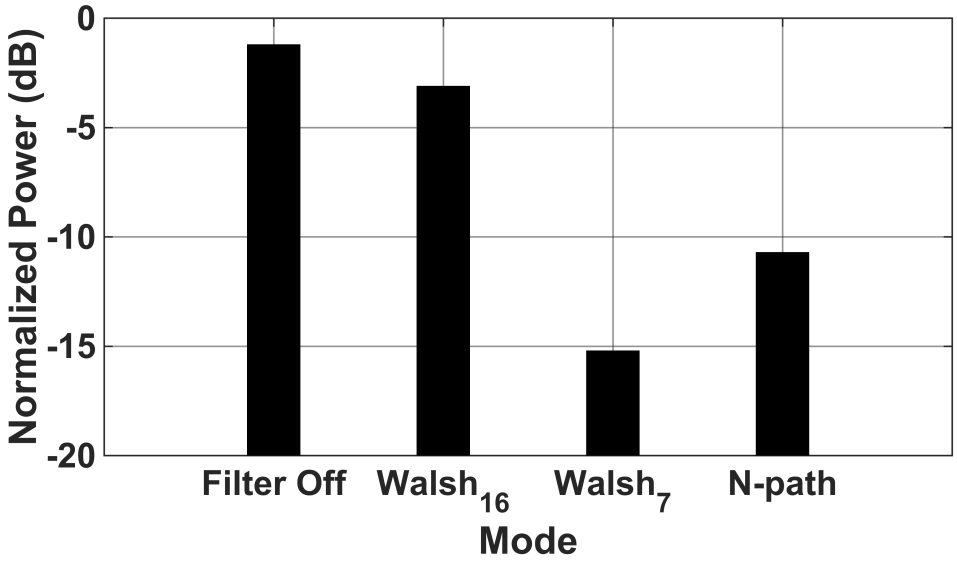


Figure 2.16: Measured RF spectrum power at code-pass CSF output matched and unmatched codes and 4-path mode. The input is modulated with a Walsh_{16} code.

IL of the filter (2.4 dB and 3.3 dB<) 2) The thermal noise of the switches ($\propto R_{SW}$) 3) The thermal noise of the parasitic resistance of baluns and QWTL (While it is possible to de-embed those losses, their NF contribution beyond their IL is accounted for). All these contributions result in a NF around 1.6-2.7 dB worse than the IL, which agrees with previous work [6-7]. In STAR systems, the blocker is at the same frequency as RX which is higher than the reciprocal mixing component by nearly 150 dB. Fig. 2.21 plots NF vs blocker power at the same frequency as RX. For N-path mode NF starts to degrade with power levels of -70 dBm (QPSK signal of 10 Mbps) while enabling the CSF mitigates the NF by 12 dB which equals to the ultimate rejection of the filter.

2.5.5 Constellation

To demonstrate the ability of the code-reject filter to pass a desired coded signal while rejecting an undesired coded signal, the AWG simultaneously produces two signals with different codes and modulated with different data streams. The QPSK waveform is

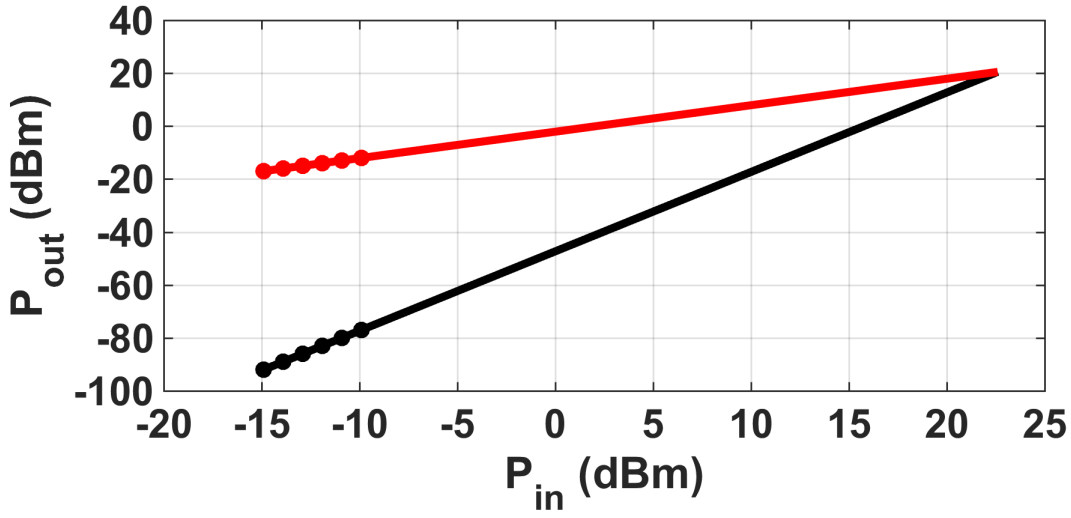


Figure 2.17: Measured IIP3 for inverted 4-path filter.

demonstrated for the code-reject CSF is shown in Fig. 2.22 for a bit rate of 1.33 Mbps. In the absence of an interfering TX (left plot), the QPSK signal is captured with EVM and demonstrates no EVM degradation. In the presence of an interfering coded TX with an interferer exceeding the signal by 20dB, the EVM is 22%.

2.5.6 Comparison With Prior Work

A performance summary is presented in Table I to summarize the measured results and compare the performance to recent work. Notably, the CSF achieves a higher IIP3 for a much lower power consumption while producing TX SI rejection. The proposed inverted 4-path filter provides a similar rejection to an 8-path series filter that demonstrated a notch filter [9] while requiring lower power consumption and one fourth the total number of switches. Compared to a code-domain mixer, this approach is a front-end filter solution that avoids the need to change the radio receive bandwidth [5]. Furthermore, the prior code domain mixer has a low IIP3 of -26dBm. Nevertheless, a high IIP3 CSF significantly relaxes the linearity requirements on the LNA and code-domain mixer.

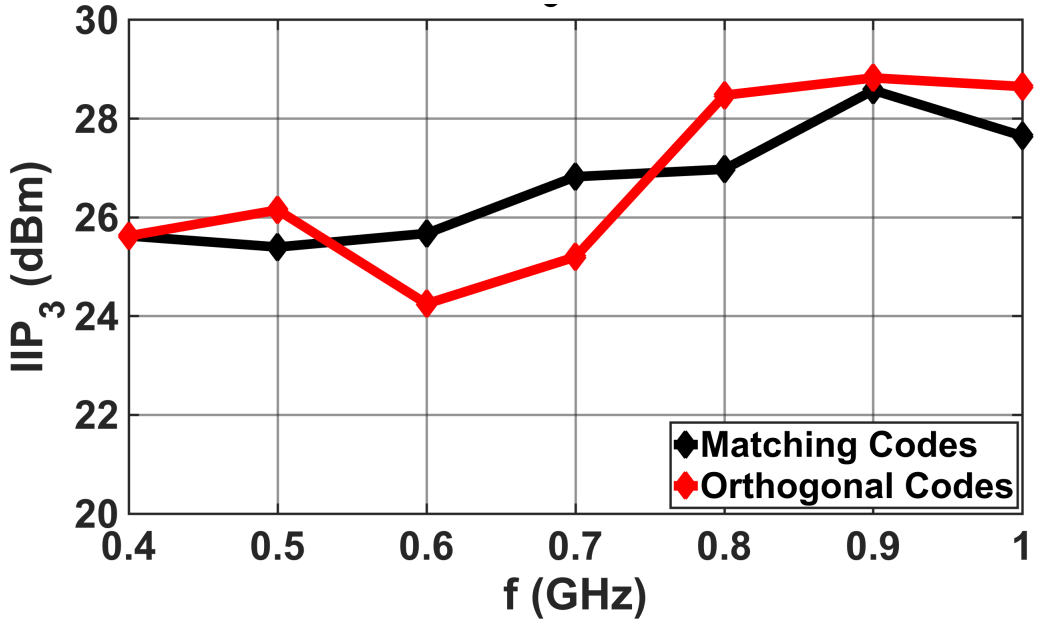


Figure 2.18: Measured IIP3 for code-pass CSF vs f_{LO}.

2.6 Conclusion

A code-selective RF filter was demonstrated for code-pass and code-reject operation using a quarter-wave impedance transformer for transmit rejection. By modulating the N-path filter with a pseudonoise sequence, the filter creates code-selective impedances. We demonstrate that the filter realized in 45-nm CMOS SOI consumes under 10 mW while offering up to 22.6 dB of rejection loss and and up to 22.6 dBm IIP3 with NF between 4-6dB depending on the applied codes.

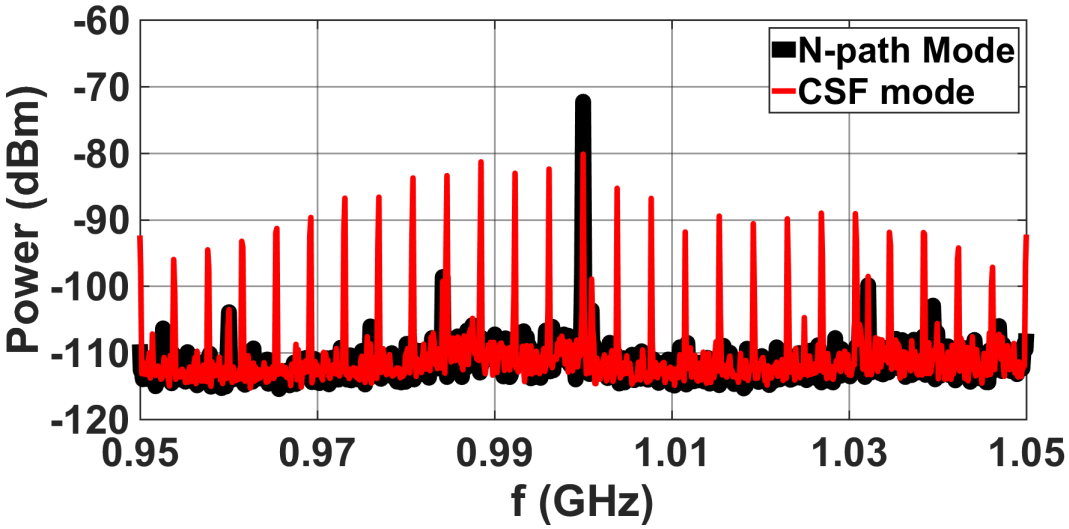


Figure 2.19: Measured LO leakage for 4-path and code-reject CSF with Barker_{13} code.

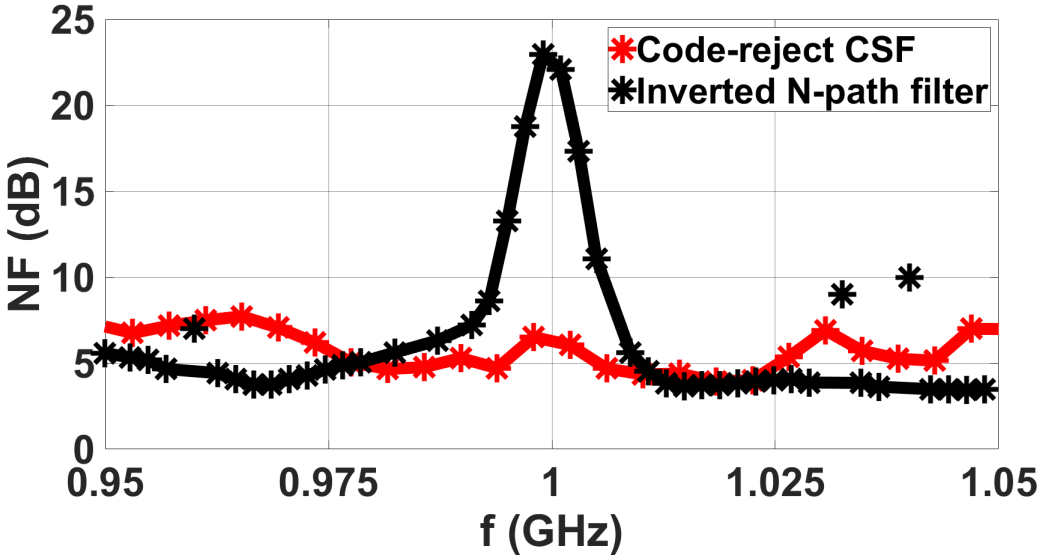


Figure 2.20: Measured NF for inverted 4-path and code-reject CSF with Walsh_{16} code.

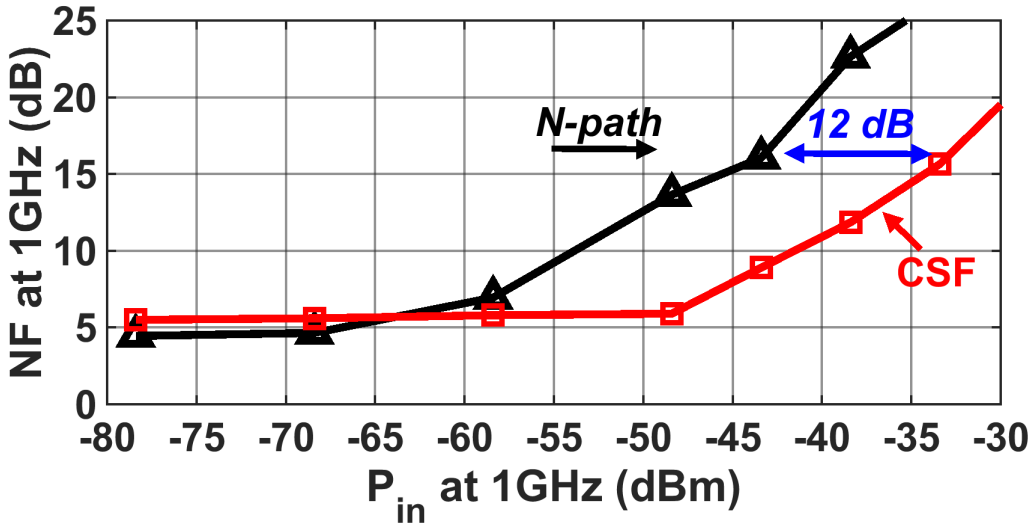


Figure 2.21: Measured blocker NF at 1GHz when applying a QPSK signal at $f = f_{LO}$ =1 GHz for band-pass 4-path filter and code-pass CSF.

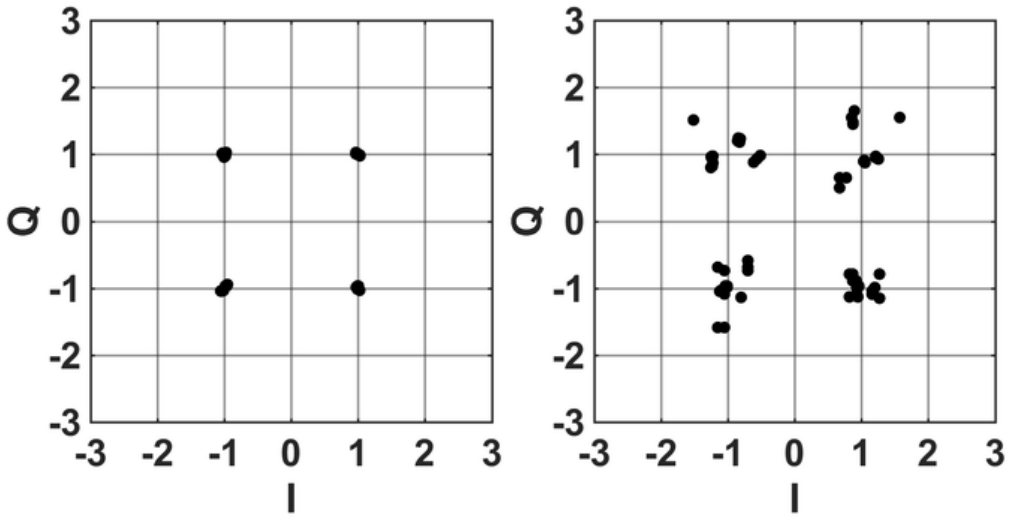


Figure 2.22: Measured FD constellation with and without SI.

TABLE I
COMPARISON WITH STATE OF THE ART

Spec.	**This work (N-path)**	**[9]**	**This work (CSF)**	**[5]**
Process (nm)	45	65	45	65
Topology	$\lambda/4$ shunt 4-path	Series 8-path	CSF at RF 4-path	Code domain 4-path Mixer
Area (mm^2)	1.77	0.87	1.77	0.31
Range (GHz)	0.9-1.1	0.1-1.2	0.4-1.1	0.3-1.4
BW (MHz)	12-25	N/A	300	1
Rejection (dB)	23	24	<21.9*	38.5**
IL (dB)	2.4	1.4-2.8	3.3*<	N/A
IIP3 (dBm)	22.6	>17	22.6*>	-26
NF (dB)	4-5	1.6-2.5	5-6*	2.5-4
P.Cons (mW)	6.18	30	9.37	36

*Code dependent

**TX attenuation is 3 dB and RX BB gain is 35.5 dB

Chapter 3

Spectrum-Compressing for Carrier Aggregation

3.1 Introduction

Future wireless systems will make opportunistic use of any available channel over a wide range of RF bands. Current 3GPP standards already support carrier aggregation (CA) to leverage multiple RF bands to improve capacity and reliability [20, 21]. To leverage CA, a receiver should also support spectrum sensing (SS) over a wide bandwidth with low sensing latency. A critical feature of SS and CA in a receiver is the ability to tolerate strong blockers within the RX band during SS or CA operation.

This paper proposes a spectrum-compressing receiver (SCRX) architecture with the ability to receive and demodulate several RF channels over a wide RF band simultaneously to support SS or non-contiguous CA operation. Fig. 3.1 shows the conventional approach to receiving multiple RF signals simultaneously. Individual RF channels are captured by independent RX chains each with a separate PLL and ADC. The RX chains are tuned via separate PLLs to the desired RF receive signals, f_1, f_2 and f_3. There are

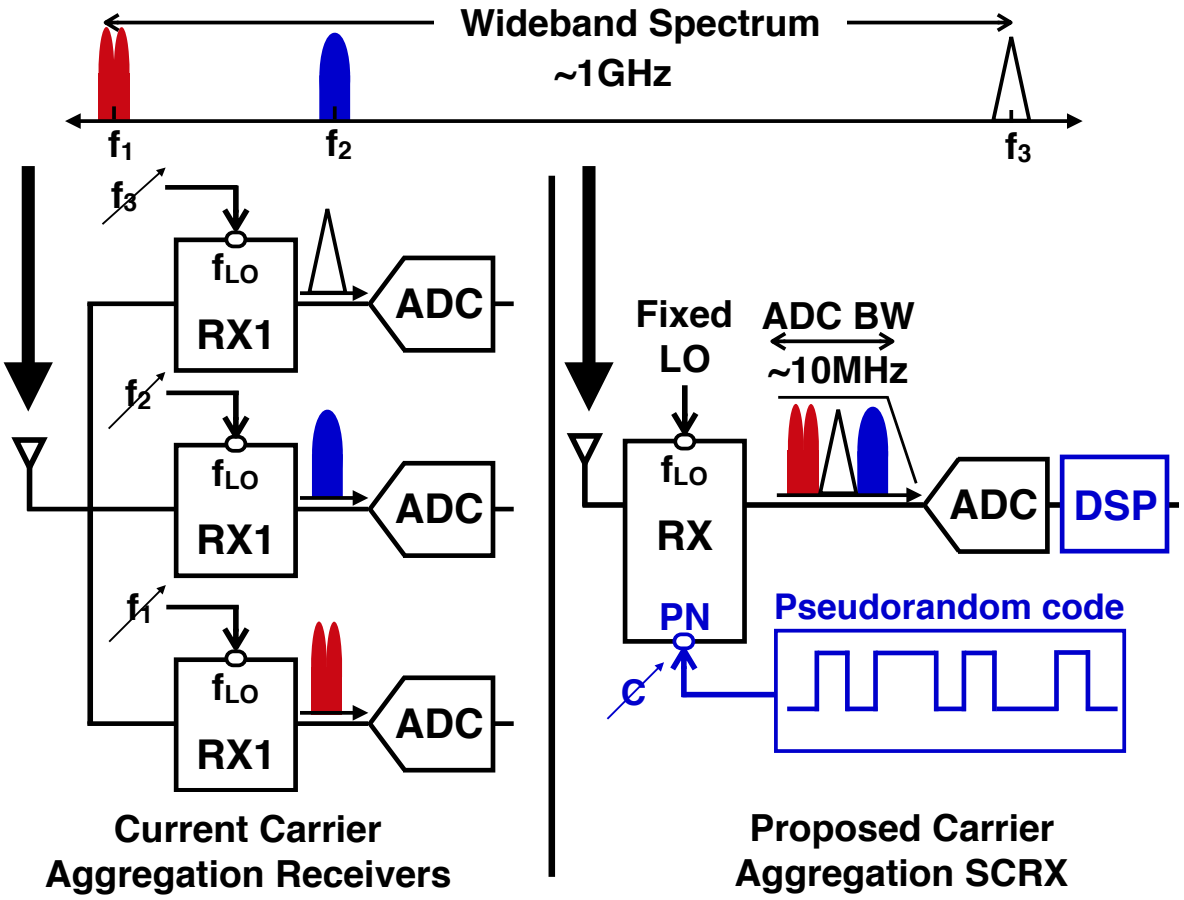


Figure 3.1: Conventional, multiband receiver and proposed non-contiguous carrier aggregation receiver using a fixed LO with PN modulation.

several undesirable features of the conventional scheme. Firstly, the RX chain offers no rejection to OOB blockers. Secondly, the power consumption and chip area scale with the number of received channels. Third, the independent tuning of multiple local oscillators (LOs) requires a PLL that demands long locking times. The coherence time (T_{coh}) of the wireless channel has been characterized in prior work and is defined as the time over which the channel spectrum power remains constant and is approximately 1 ms for a channel with 100 Hz Doppler spread at 1 GHz carrier frequency [4]. Consequently, dynamically switching bands based on SS requires detecting the available spectrum within 10 μs and transmitting the data over a roughly 100 μs period.

Recent research has demonstrated spectrum-sensing algorithms that can be implemented in CMOS RF front-ends [22–28]. However, the prior work detects blockers passively without any blocker rejection complicating the ability to use SS in an environment with multiple strong blockers. Other recent work relies on sweeping the LO and scanning the down-converted baseband (BB) signal. Typically, however, a state-of-the-art PLL will not settle faster than 5 μs [29] making detection over a wide frequency band (i.e. more than few channels) extremely slow. In a dynamic spectrum or blocker environment, a swept PLL may be inadequate to detect the occupied spectrum with high reliability.

Fig. 3.1 also shows the proposed SCRX architecture. A pseudonoise (PN) code is applied to modulate the LO and to simultaneously sample specific channels over a wide RF band. The individual channels are converted to a single IF with sufficient bandwidth for the CA channels where each channel is separated by a desired channel spacing and digitized with a single ADC operating at a sample rate high enough to process all three signals. The digital signal processing (DSP) can filter and demodulate the separate signals in the case of CA or detect spectral power density in multiple channels through SS filtering in DSP. Once the observation is complete, the DSP can change the modulated code to sample other channels without any change in the LO frequency for rapid reconfiguration. The PN sequence modulation for the SCRX modulates the LO with a PN sequences and does not require re-tuning the PLL or re-calibration at each frequency channel, thereby significantly reducing the scan time.

We present a review of the properties of a PN-modulated LO in the next section. In Section III, we demonstrate a high-linearity N-path based receiver that downconverts a wide RF spectrum onto IF sampling capacitors where the signal is amplified for quantization and DSP. In Section IV, we demonstrate the tuning range, dynamic range, and non-contiguous CA operation of the chip and verify this with an OTA demonstration.

3.2 LO Code Modulation for NC-CA and SS

PN codes have been implemented in CMOS transceivers [5, 17, 30–35]. A random code $C(t)$ of length M can be decomposed into Fourier coefficients based on the sequence values, $\alpha[k]$ [8].

$$C(t) = \sum_{m=-\infty}^{\infty} \sum_{k=1}^{M} \alpha[k](-j)^{\frac{4m(k-1)}{M}} a_m e^{jm\frac{\omega_c}{M}t} \\ \text{where } a_m = \frac{\sin m\frac{\pi}{M}}{m\pi} e^{\frac{-j\pi m}{M}}. \tag{3.1}$$

Here, $\omega_c = 2\pi f_c$ where f_c is the chip rate of the sequence. The Fourier domain representation of the periodic code gives insight into the ability to tailor the LO spectrum with weights at the different frequency taps. To simplify (3.1), we consider only the spectral components up to the chip rate.

$$C(t) \approx \sum_{m=-M/2}^{+M/2} a_m e^{j\frac{m\omega_c}{M}t} \sum_{k=1}^{M} \alpha[k](-j)^{\frac{4m(k-1)}{M}} \tag{3.2}$$

In other words, each M-length code has up to M frequency components spaced by f_c/M as well as a component at DC. The amplitude at each frequency component is

$$c_m = a_m \sum_{k=1}^{M} \alpha[k](-j)^{\frac{4m(k-1)}{M}}. \tag{3.3}$$

Therefore, the Fourier series is $C(t) \approx \sum_{m=-M/2}^{+M/2} c_m e^{j\frac{m\omega_c}{M}t}$. For example, a Walsh code of length 8 has 8 potential codes. The second Walsh code (W_2) has a sequence of $\alpha[k] = \begin{bmatrix} 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \end{bmatrix}$. After applying (3.2) to W_2, each frequency coefficient is weighted by $c_m = \begin{bmatrix} 1/\pi & 0 & 0 & 0 & \boxed{0} & 0 & 0 & 0 & 1/\pi \end{bmatrix}$ at frequency components $\begin{bmatrix} -f_c & -\frac{3f_c}{4} & \dots & +\frac{3f_c}{4} & +f_c \end{bmatrix}$.

When the code is multiplied by an LO frequency f_{LO}, the spectral components of the code are modulated around the LO, e.g. $\begin{bmatrix} f_{LO}-f_c & f_{LO}-\frac{3f_c}{4} & .. & f_{LO}+\frac{3f_c}{4} & f_{LO}+f_c \end{bmatrix}$. Therefore, the modulated LO has two components with 5 dB of loss relative to the LO, which potentially degrades the sensitivity. Since the DC component of a Walsh codes is always 0, e.g. $c_m = 0$, the RX can select different frequency components for CA without interference from the blockers near the LO frequency.

To aggregate two carriers at f_1 and f_2 without interference to an IF location, f_{LO} and f_c need to be tuned. The two RF carriers are down-converted to IF frequencies IF_1 and IF_2:

$$f_{LO} = \frac{f_1 + f_2 + IF_2 - IF_1}{2} \tag{3.4}$$

$$f_c = f_2 - f_1 + IF_2 + IF_1. \tag{3.5}$$

Assuming that the two desired carriers have a bandwidth BW, the receiver should allow that $IF_2 = IF_1 + BW$. Therefore,

$$f_{LO} = \frac{f_1 + f_2 + BW}{2} \tag{3.6}$$

$$f_c = f_2 - f_1 + 2IF_1 + BW. \tag{3.7}$$

If more than two carriers are to be aggregated, a different Walsh code can be selected. For Walsh 6 (W_6), $\begin{bmatrix} 1 & 0 & 1 & 0 & 0 & 1 & 0 & 1 \end{bmatrix}$ and the Fourier coefficients are $\begin{bmatrix} 0 & 0.256 & 0 & 0.132 & \boxed{0} & 0 & 0.132 & 0 & 0.256 & 0 \end{bmatrix}$ allowing the aggregation at 4 RF channels.

A comprehensive list of the frequency components and relative power levels of Walsh codes of length 16 are shown in Fig. 3.2. The relative amplitudes of the Fourier coefficients are indicated with darker contrast. The first Walsh code (W_1) is a sequence

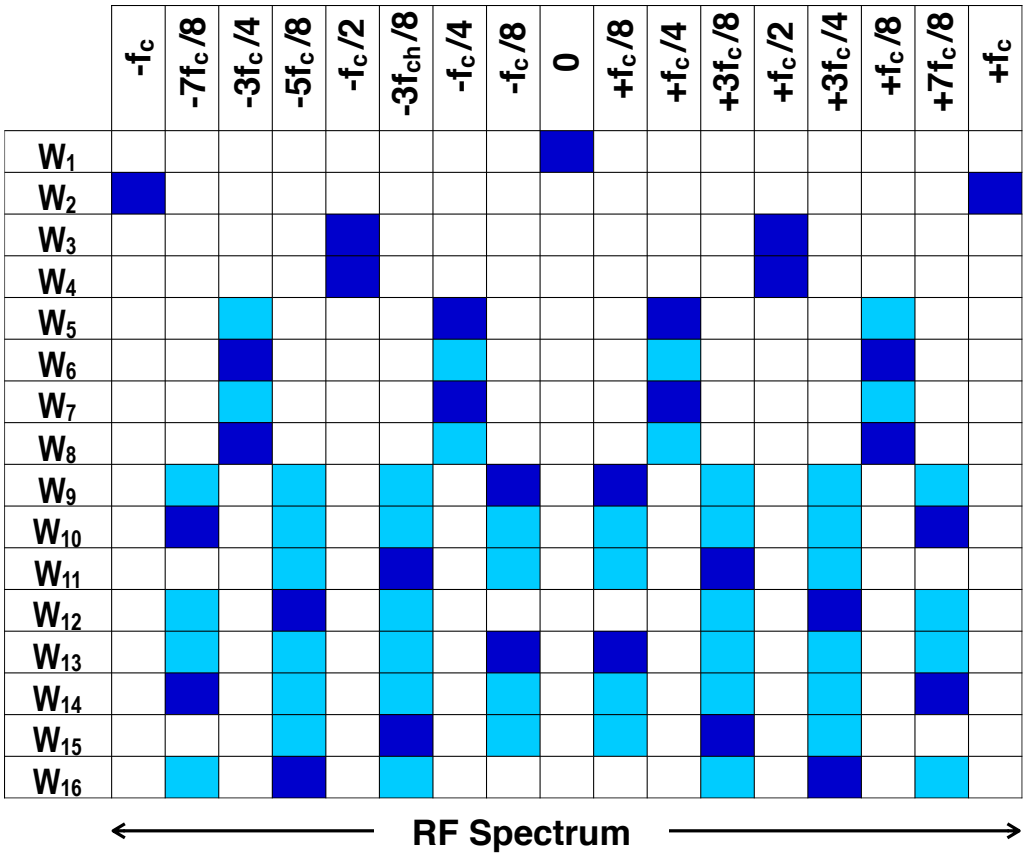


Figure 3.2: Approximated frequency components of Walsh family of length 16.

of ones so it only has a DC component and can select only one channel. The W_2, W_3, and W_4 codes select two channels simultaneously. Note that W_3 and W_4 are degenerate. The W_5-W_8 codes select 4 channels simultaneously. The W_9-W_{16} codes aggregate up to 6 channels. Given a fixed LO, changing the Walsh code can select any channel across the band in Fig. 3.2.

Fig. 3.2 suggests that reduced LO amplitude at each spectral component leads to higher spot noise figure (NF) due to reduced conversion gain. Nonetheless, the higher NF is offset by a significant advantage from the NC-CA diversity technique. Fig. 3.3 plots the probability of error (Pe) as a function of signal-to-noise ratio (SNR) for an additive white Gaussian noise (AWGN) channel and a fading wireless channel [4]. In the AWGN

channel, Pe improves exponentially with SNR suggesting that higher NF is undesirable.

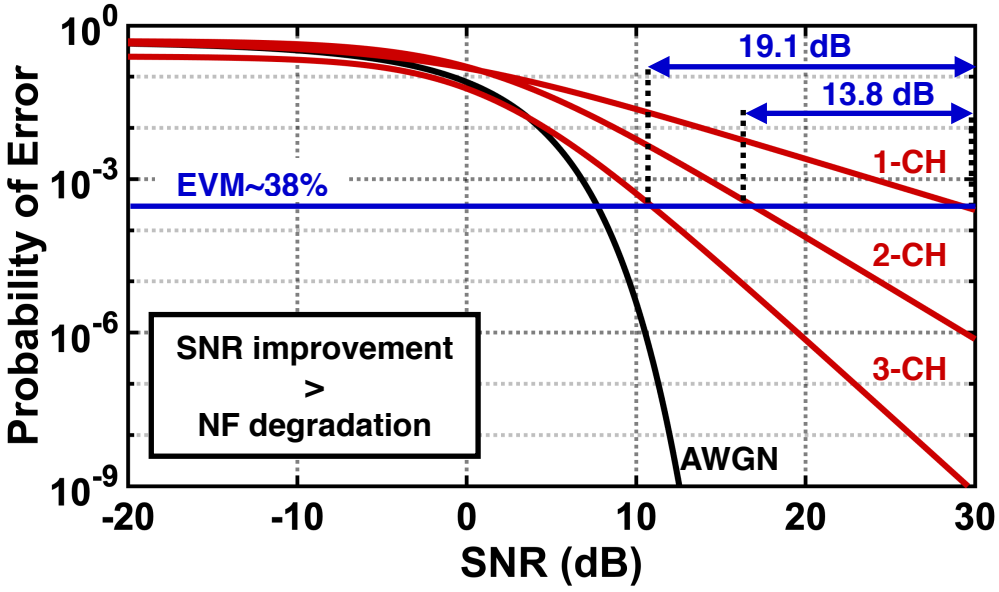


Figure 3.3: Performance of AWGN channel compared to a wireless channel at different diversity.

However, the multi-path fading channel does not provide a significant benefit due to SNR. Even when the RX SNR is large, the multiple paths can destructively interfere and degrade Pe inversely proportional to SNR. The NC-CA diversity improves the Pe of the wireless channel by adding an independent degree of freedom [4]. To achieve a Pe of $10^{-}3$ with a fading channel, the SNR needs to exceed 30 dB in the absence of diversity. With the diversity-2 channel, Pe of $10^{-}3$ is achieved with SNR of 13 dB. Considering an SNR degradation of 3 dB with the diversity channel, Pe of $10^{-}7$ is reached for 30 dB. In other words, carrier aggregation targets increased capacity of the wireless channel for high SNR where NF is not usually the limitation. In commercial products [**?**], the LNA gain is reduced or the LNA might be by-passed in CA mode to improve linearity of the RX to realize the diversity.

To eliminate aggregation from the out of band harmonics, a pulse shaping technique [**?**] shown in Fig. 3.4 a) can be used. Pulse width modulation at the edges mimics a

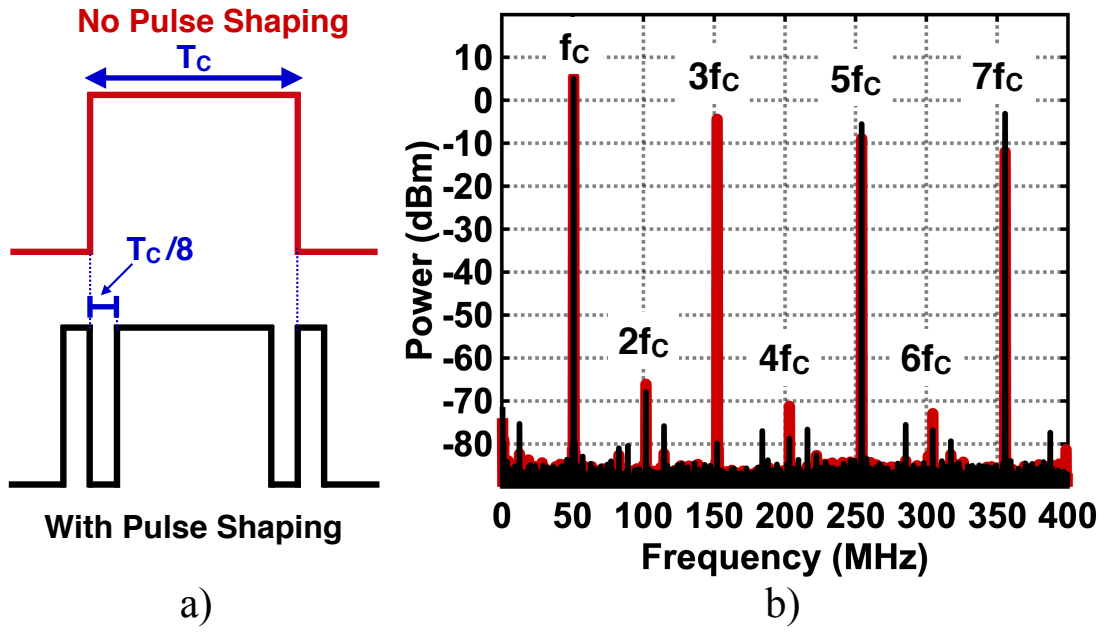


Figure 3.4: Illustration of pulse shaping technique to lower third harmonic a) and a measured spectrum of pulse generated by equipment b).

raised cosine filter and chosen to suppress third order harmonic. This comes at the cost of reducing the power of fundamental and increasing the power of higher order harmonics while increasing the chip rate by a factor of 8. Measured spectrum of generated waveform is shown in Fig. 3.4b)

3.3 Overview of Architecture

Fig. 3.5 illustrates a block diagram of the proposed spectrum compressing (SCRX). The RF signal is balanced into a differential signal and a PMOS N-path filter down-converts the signals to sample onto BB amplifiers. The SCRX can be taped onto a primary RX allowing for usage as a diversity RX. The 75% duty cycle LOs are generated and modulated on chip. We review the operation of each circuit block in the sections below.

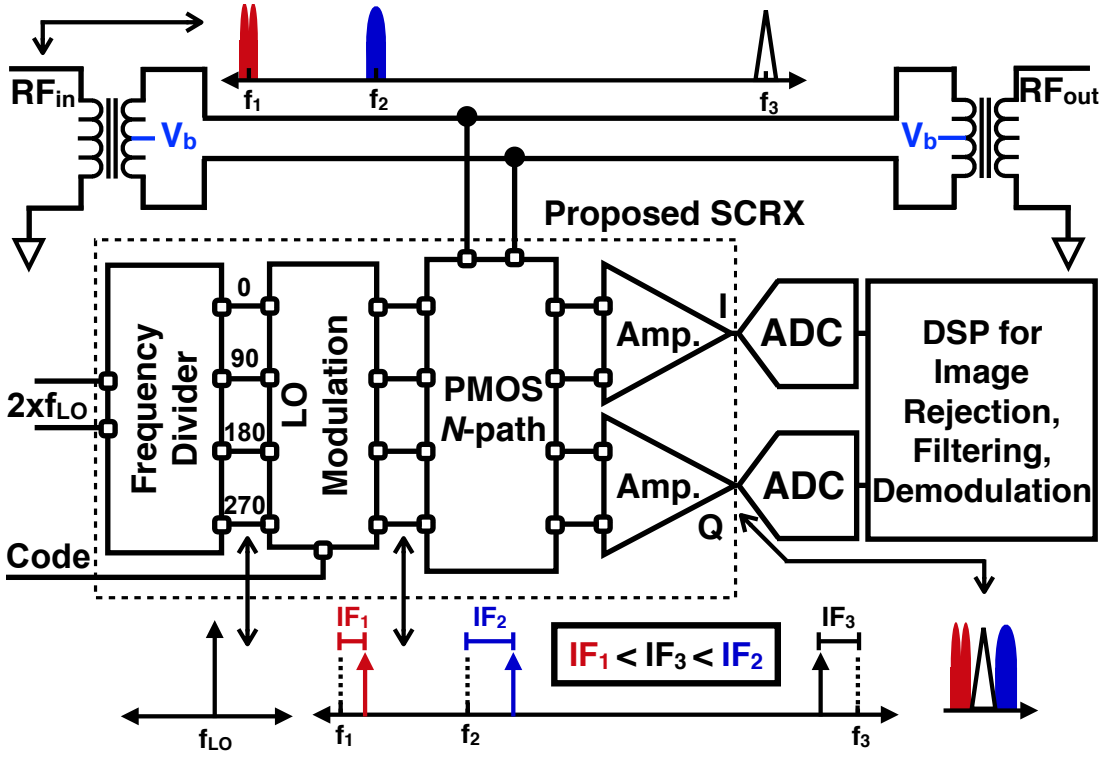


Figure 3.5: Block diagram of the proposed architecture.

3.3.1 PMOS N-Path Filter

Silicon-on-insulator (SOI) technology offers low $R_{on}C_{off}$ for improved switching speed. As the gate length of CMOS has scaled down, the gap between NMOS and PMOS switches has diminished. Fig. 3.10 shows a comparison between NMOS and PMOS $R_{on}C_{off}$ product (simulation) for different devices in a 45-nm RF SOI process. At the shortest channel length, the PMOS switches are only 14% slower than NMOS switches. Nonetheless, the PMOS devices may offer higher breakdown and improved linearity.

Fig. 3.7 compares simulated S-parameters of a shunt NMOS and PMOS-based N-path filter each with the same device geometry. The out-of-band (OOB) rejection is degraded by less than 1 dB while the insertion loss is slightly improved due to higher switch resistance and higher equivalent resistances (R_{SH}), respectively. However, another

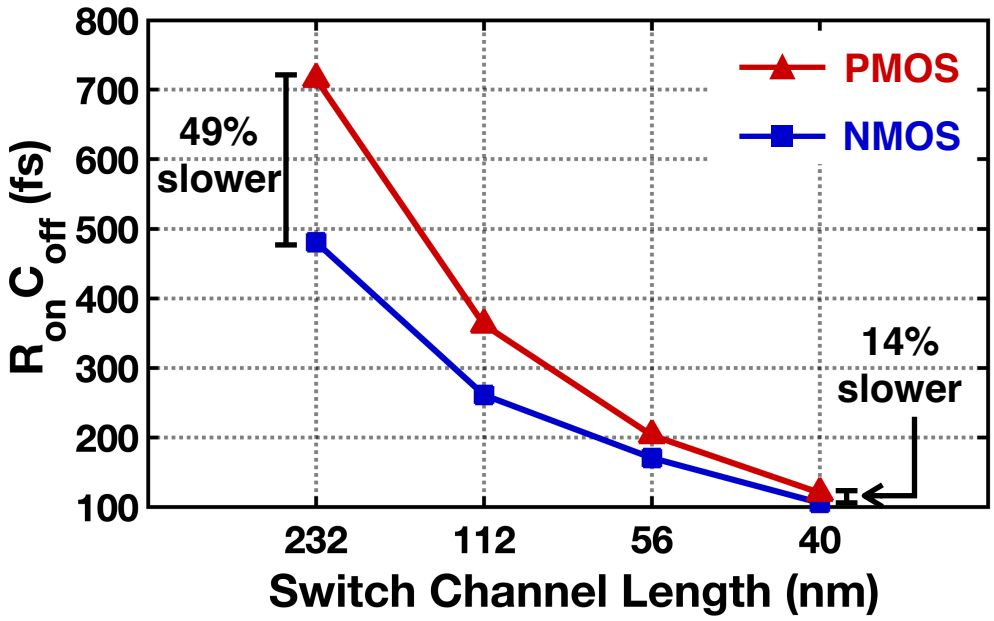


Figure 3.6: $R_{on}C_{off}$ of NMOS and PMOS switches

advantage of using PMOS switches is the relatively high common-mode voltage ($V_{DC} \approx 1V$) applied at the source and drain to keep the switch off when the LO is high. The high common-mode voltage allows an NMOS baseband amplifier to directly sample the IF capacitors on the N-path filter. The baseband amplifiers will be demonstrated in subsequent sections as well as the need to realize high common-mode rejection ratio. Third, simulated input P1dB of PMOS N-path is 0.95 dB than NMOS N-path.

The proposed PMOS N-path filter is shown in Fig. 3.8 and consists of 4 paths. The size of the switches is 106.4 μm/ 40 nm while the BB capacitors are based on hybrid capacitor bank [16] with high-density capacitors and shunt capacitors to improve OOB rejection and CM noise generated on chip from LO leakage, the equivalent capacitance value is 124.9 pF.

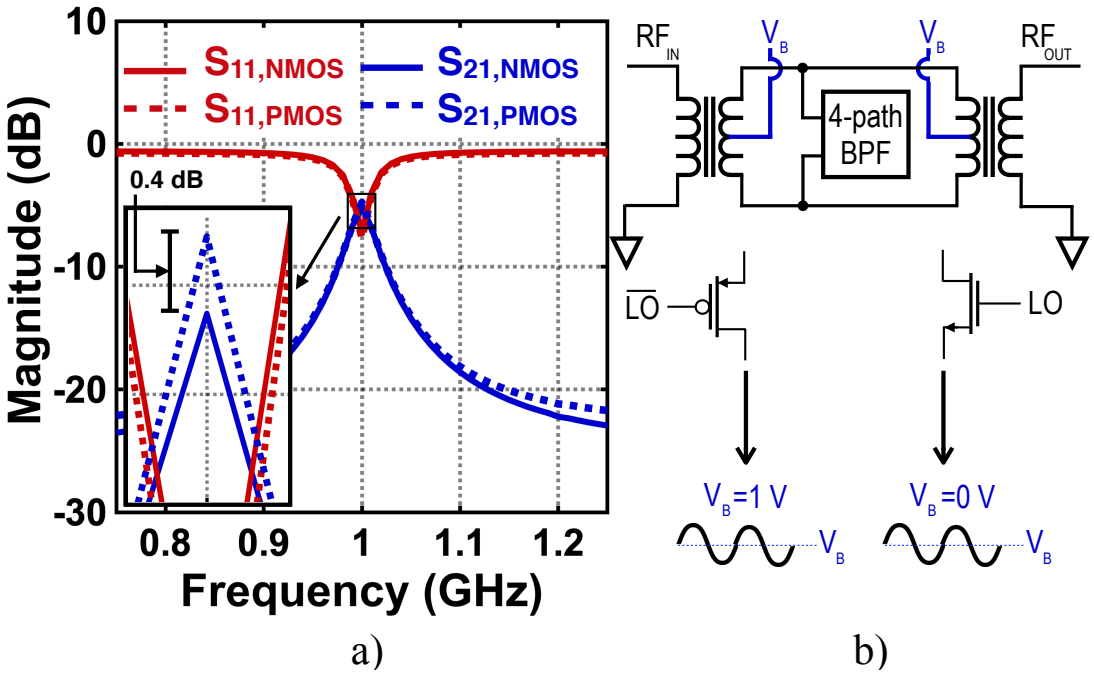


Figure 3.7: Comparison of S-parameters for N-path filters based on NMOS and PMOS switches.

3.3.2 LO Generation and Modulation

The PN-modulated LO generator allows the adjustment of LO phase overlap with the PN sequence. Digitally XORing the LO phase with the sequence value (Fig. 3.8) produces the spectral components of the LO that shift the band-pass impedance of the N-path to the desired frequency channel. The LO generation is implemented with D flip-flops (DFFs) based on thin-oxide devices with 1-V supply (as shown in fig. 3.8) for speed and thus the common voltage on the RF and BB nodes is 1 V.

Fig. 3.10 shows the simulated spectrum of the LO before modulation showing a peak at f_{LO} of 1 GHz. When modulated with a W_{16} code, the LO is spread to different locations resembling the profile shown in Fig. 3.2. To study the impact of nonlinear buffers on the modulated LO, the harmonic components are shown as the modulated LO is passed through two inverters showing no change in the amplitude of the LO components. The even harmonics show an undesirable increase of around 30 dB but remain around -100

dBc.

Fig. 3.11 compares the theoretical conversion gain for the PN-modulated N-path filter when modulated with W_{16}. The simulation indicates close agreement with theory at six distinct peaks (-20 dB conversion gain) and some small discrepancy at the weaker harmonics. The conversion gain is normalized to the unmodulated LO.

Typically, the frequency divider and LO modulator degrade the LO phase noise [36]. A gating technique [18] is extended here to clean the phase noise of the divider and modulator as shown in Fig. 3.9. The code is sampled with a DFF clocked with the LO to make sure the modulation begins at the beginning of LO waveform. At the code transitions, the only vulnerable edge occurs when the rising edge of the $2f_{LO}$ overlaps the jittery LO to transfer phase noise of the divider and modulator to the LO.

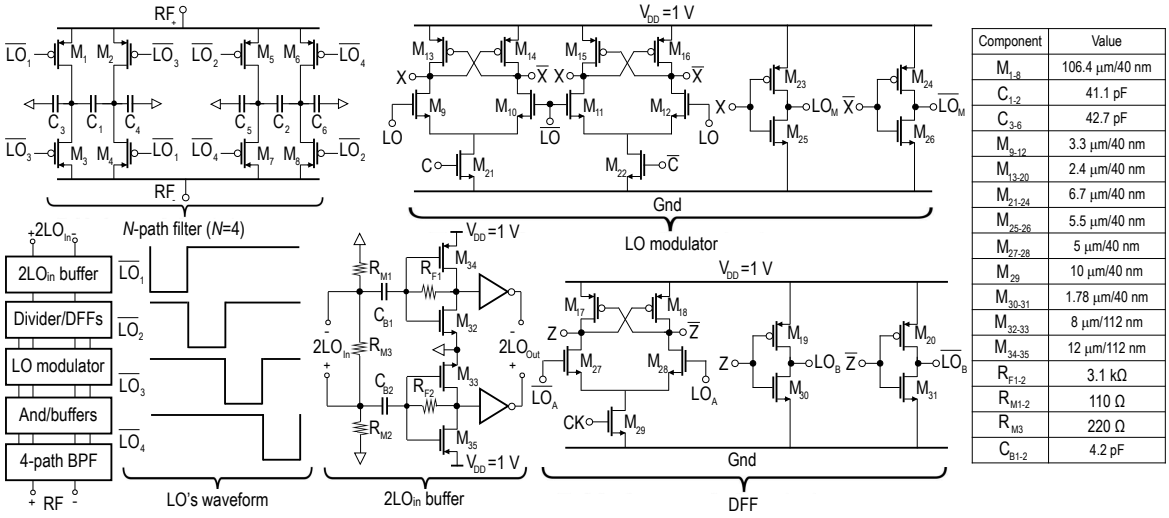
3.3.3 Baseband Amplifier with High CMRR

Fig. 3.12 shows the proposed baseband (BB) amplifier structure that samples the IF capacitors with a G_m-cell and a transimpedance amplifier (TIA). The BB is implemented with thick-oxide devices operating at 1.5 V. Unlike earlier work that realized the N-path as a mixer-first [37] structure such that the BB impedance is low at DC for impedance matching (current-mode N-path) requiring a TIA-based BB amplifier, the proposed CA receiver presents a high impedance such that the desired RF signal power passes through the filter and matches to the output port, e.g. voltage-mode N-path [9].

The DC level on the PMOS switches sets the common-mode voltage for the G_m-cell. Referring to Fig. 3.12, the input common-mode voltage range is [38]

$$V_{th1,2} + V_{od1,2} + V_{sat5} \leqslant V_{IN,CM} \leqslant V_{DD,A} - |V_{sat3,4}|. \tag{3.8}$$

Typical values of $V_{th1,2} = 0.35$ V, $V_{od1,2} = 0.15$ V, $V_{DD,A} = 1.5$ V and V_{sat5}=$|V_{sat3,4}|$ =



Component	Value
M_{1-8}	106.4 µm/40 nm
C_{1-2}	41.1 pF
C_{3-6}	42.7 pF
M_{9-12}	3.3 µm/40 nm
M_{13-20}	2.4 µm/40 nm
M_{21-24}	6.7 µm/40 nm
M_{25-26}	5.5 µm/40 nm
M_{27-28}	5 µm/40 nm
M_{29}	10 µm/40 nm
M_{30-31}	1.78 µm/40 nm
M_{32-33}	8 µm/112 nm
M_{34-35}	12 µm/112 nm
R_{F1-2}	3.1 kΩ
R_{M1-2}	110 Ω
R_{M3}	220 Ω
C_{B1-2}	4.2 pF

Figure 3.8: Transistor-level schematic of the PN-modulated RX and digital modulation blocks.

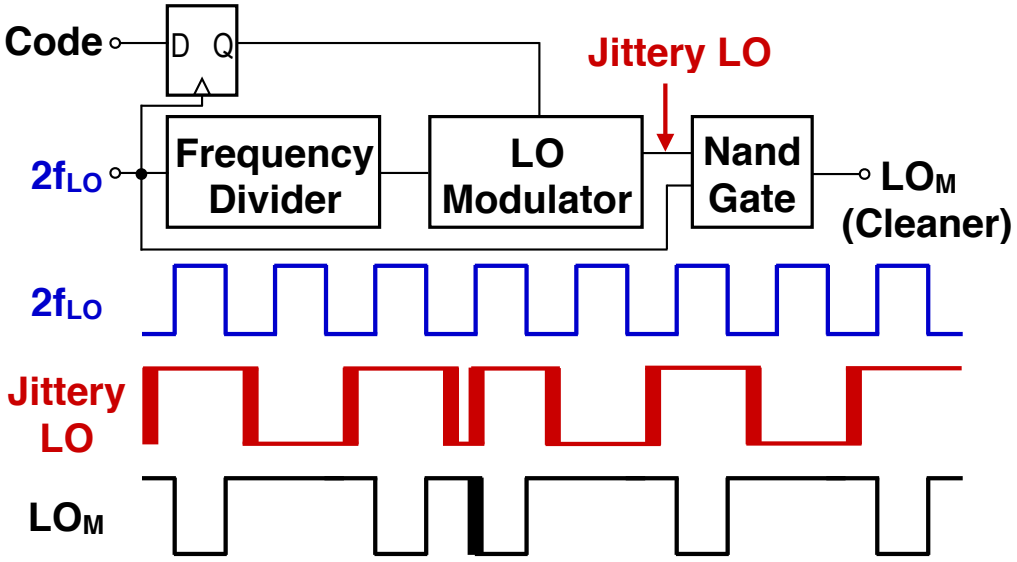


Figure 3.9: Clock gating self-cleans the phase noise of frequency divider and LO modulation.

0.2 V suggests a range of 0.7 V$\leqslant V_{IN,CM} \leqslant$ 1.3 V. Consequently, choosing $V_{IN,CM}$ = 1 V provides the maximum input voltage swing and improves linearity. Considering a G_m-cell with PMOS input devices, the common-mode voltage requirement is between 0.2 V $\leqslant V_{IN,CM} \leqslant$ 0.8 V. However, a common-mode approach to bias the NMOS switches at a voltage slightly higher than 0 V (around 0.5 V) to set the common-mode level of the PMOS input devices of G_m-cell has two issues:

1) decreasing on-resistance of the switch lowering the OOB rejection and 2) PMOS analog devices have lower mobility and thus lower transconducance for the same current compared to NMOS switches which results in lower gain and higher NF. Consequently, we have chosen PMOS-based switches with an NMOS-based baseband amplifier.

The main amplifier has high transconductance (g_m) to lower the NF. The CMFB is

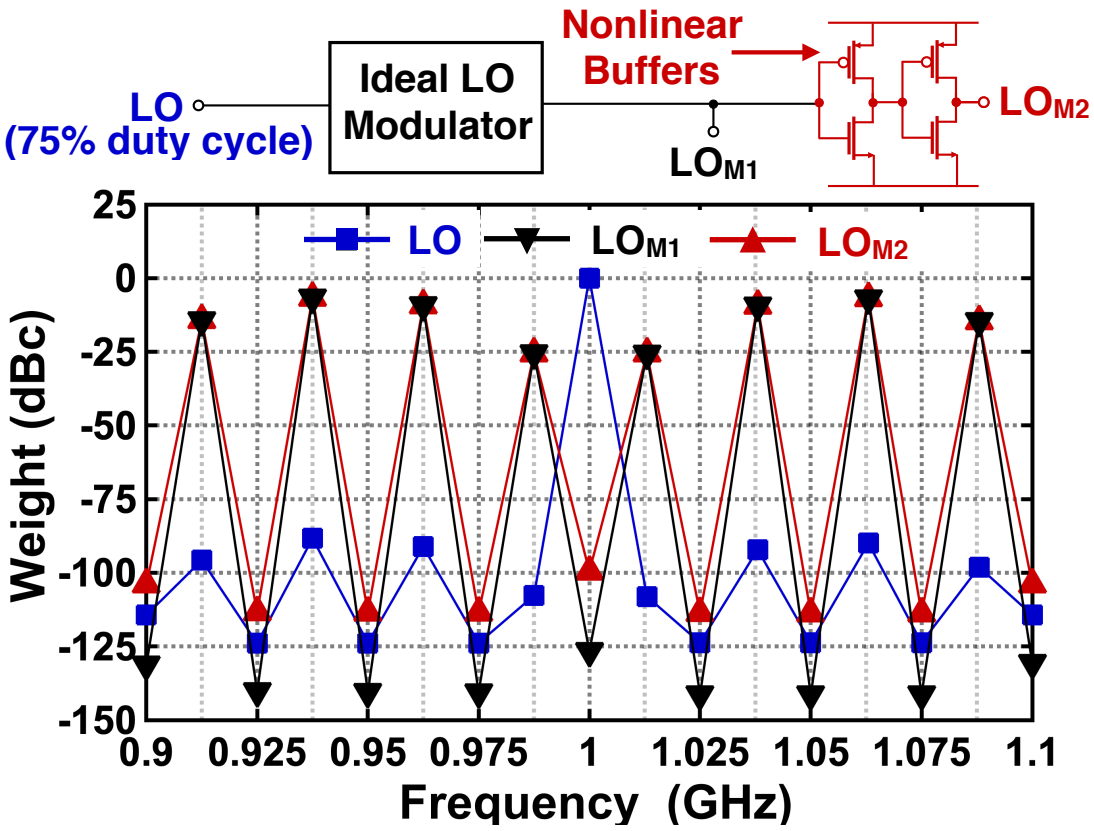


Figure 3.10: Simulated impact of nonlinear buffer on a modulated LO with W_{16}

sized to be 1/8 smaller than the main amplifier. To stabilize the CMFB, a load capacitor is added to the feedback node and two Miller capacitors are added across the second gain stage of the feedback. The TIA is similar to the G_m-cell with a feedback resistor and capacitor to set the baseband bandwidth. The gain of each of the BB amplifiers is approximately 36 dB.

3.4 Measurements

The SCRX was fabricated in the GlobalFoundries 45-nm CMOS SOI process and mounted on a PCB for testing. Fig. 3.13 shows a microphotograph of the chip indicating the relative size of the circuit blocks. The chip occupies an area of 0.82 mm^2 including the pads and ESD circuitry. The active area is 0.55 mm^2. The power consumption of the N-path is 6.7 mW

from 1 V supply (dynamic switching power) at $f_{LO} = 1$ GHz and sensing sequence rate

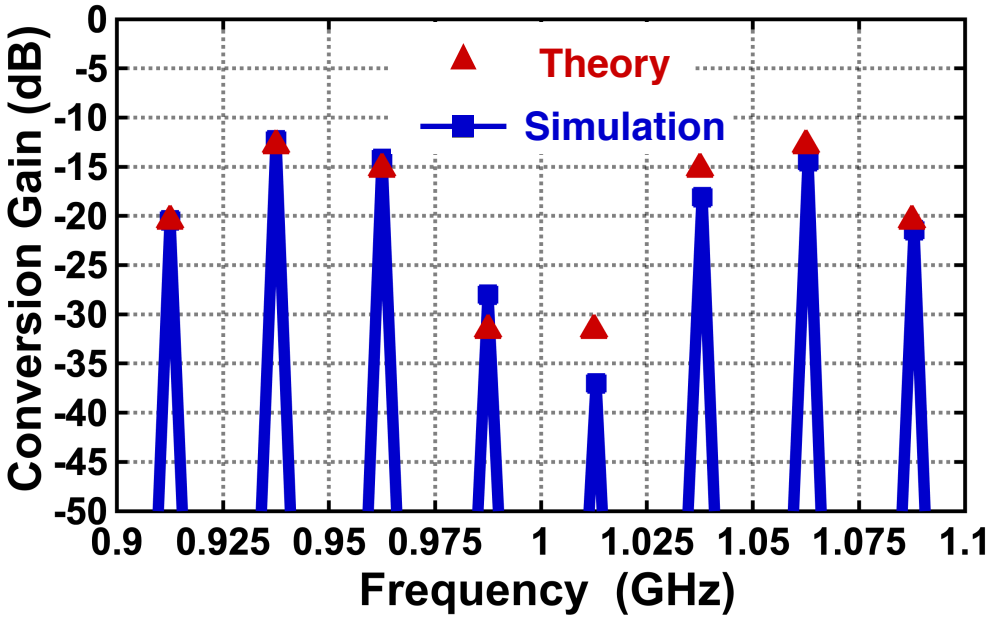
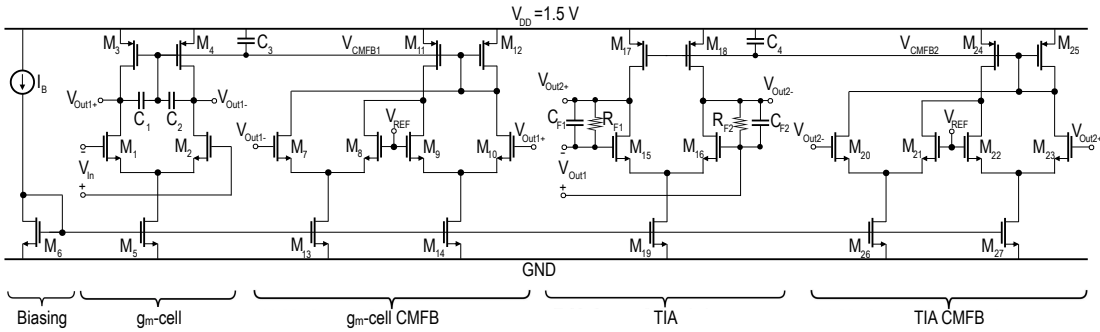


Figure 3.11: Comparison of theory and simulation of W_{16} conversion gain (normalized).



Component	Value	Component	Value	Component	Value	Component	Value	Component	Value
M_{1-2}	96 µm/232 nm	C_{1-2}	1.22 pF	M_{13-14}	12 µm/232 nm	M_{20-23}	12 µm/232 nm	R_{F1-2}	9 kΩ
M_{3-4}	32 µm/232 nm	C_3	1.26 pF	M_{15-16}	48 µm/232 nm	M_{24-25}	8 µm/232 nm	C_{F1-2}	0.7 pF
M_5	192 µm/472 nm	M_{7-10}	12 µm/232 nm	M_{17-18}	32 µm/232 nm	M_{26-27}	12 µm/232 nm	V_{REF}	1-V
M_6	24 µm/472 nm	M_{11-12}	8 µm/232 nm	M_{19}	96 µm/472 nm	C_4	0.7 pF	I_B	175 µA

Figure 3.12: Transistor-level schematic of the BB amplifier.

f_c = 300 MHz while the two BB amplifiers consume 16.5 mW from 1.5 V supply. The RX is tested under two scenarios: single carrier during which the W_1 code is used to modulate the LO and non-contiguous CA (NCCA) with two or more RF signals located

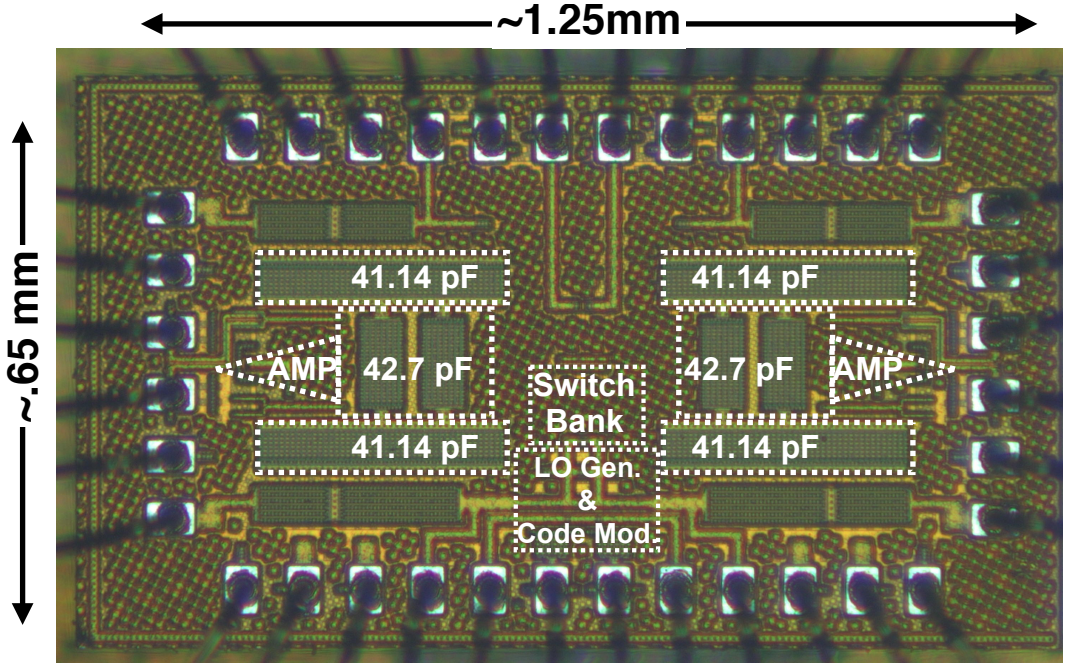


Figure 3.13: Chip microphotograph of the proposed SCRX in GF 45 nm RF SOI.

around f_{LO} during which a Walsh code with multiple frequency components, e.g. W_2 or higher, modulates the LO.

The measured S_{21} and S_{11} for the SCRX is plotted in Fig. 3.14. The LO is tuned from 0.1 to 1.2 GHz and illustrates the passband behavior over the frequency range. Notably, the peak S_{21} occurs around 0.6 GHz.

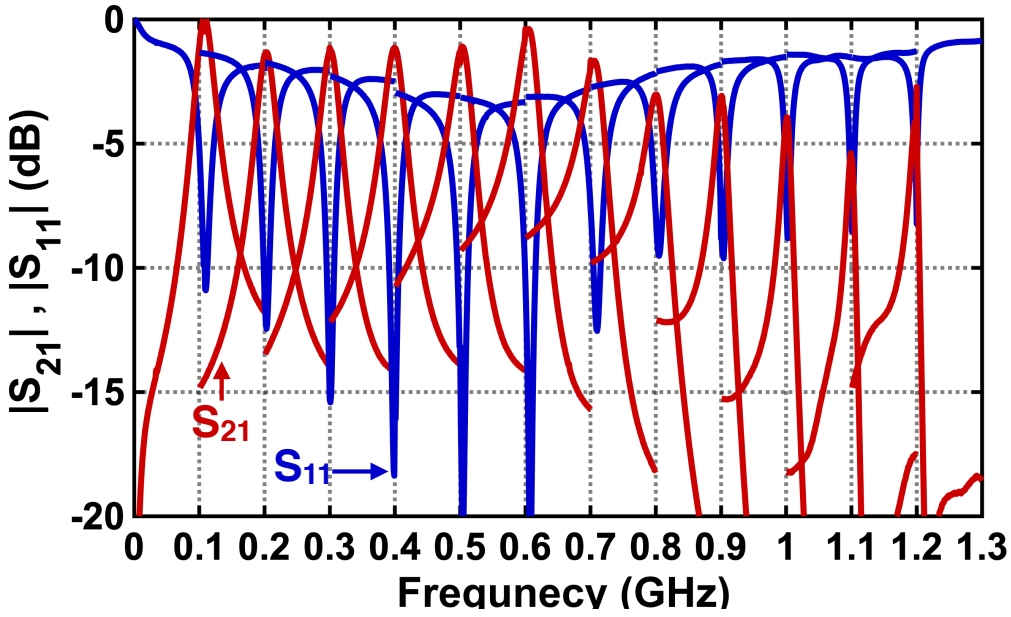


Figure 3.14: Measured S_{21} and S_{11} for different f_{LO} frequencies.

Fig. 3.15 plots the simulated and measured conversion gain as a function of the RF frequency while the LO frequency is fixed at 900 MHz. During this measurement, the chip rate of the W_2 code is increased to sample RF bands further from the LO. The tuning range 3-dB bandwidth is 1 GHz while the tuning frequency extends to 1.4 GHz. The frequency response is limited to the external on-board balun frequency response which rolls-off at 1.4 GHz.

The transient response is plotted in Fig. 3.16 for the BB output voltage as a function of time over an interval when the code is switch between W_1 and W_2. When the signal is 54 MHz away, we expect the receiver to amplify the signal at baseband when using W_2

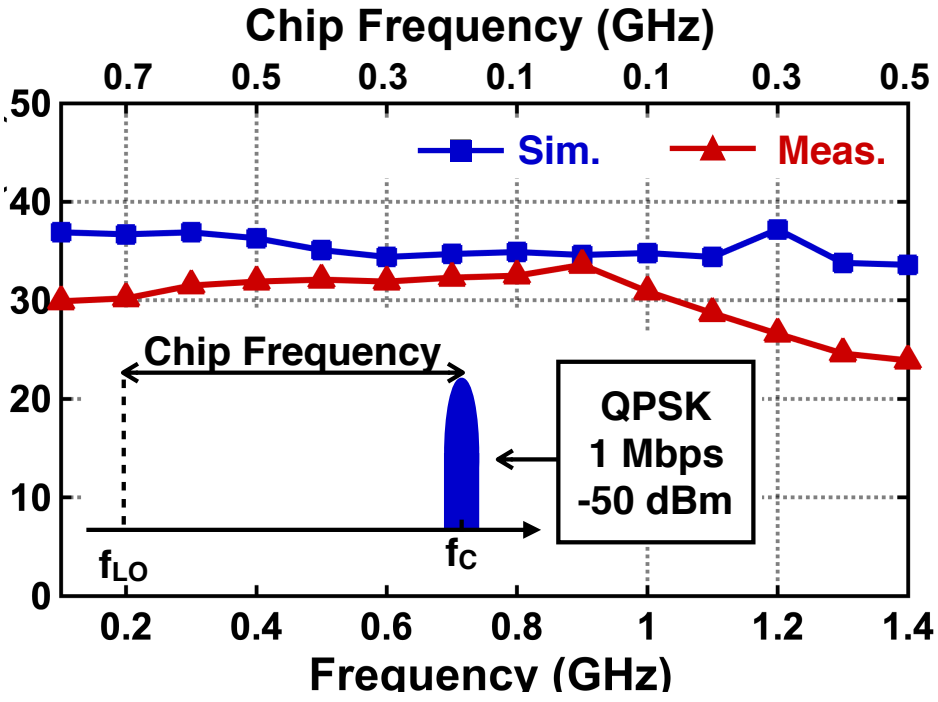


Figure 3.15: BB gain at f_{LO}= 900 MHz while sweeping the chip rate to select different RF channels.

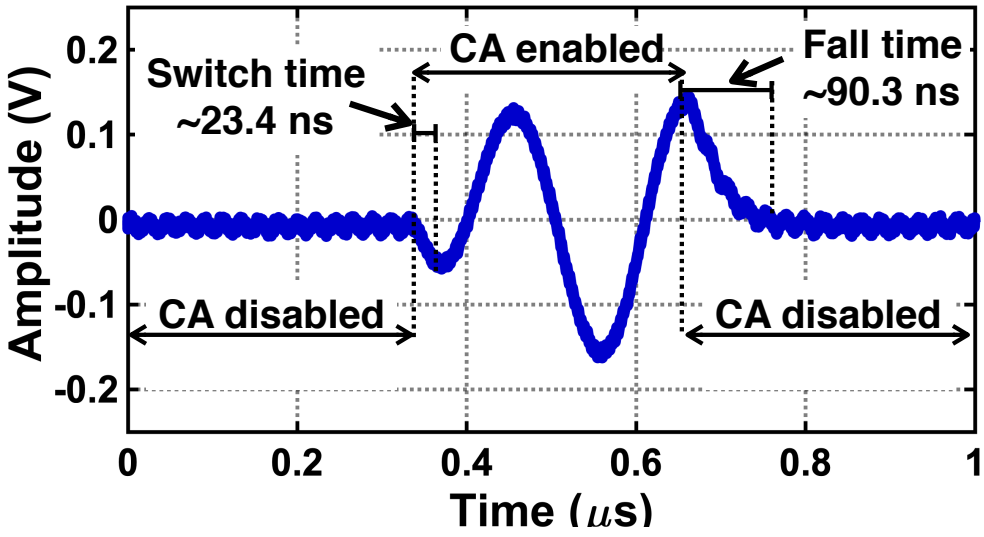


Figure 3.16: Measured BB time-domain waveform while rapidly changing the carrier location.

at a chip rate of 100 Mcps. Initially, the RX uses W_1 and no output voltage is observed. When the code is switched to W_2, the RF signal is amplified as shown by the envelope signal starting at $\sim$ 23.4 ns. After, the code is switched back to W_1. The rise and fall times are due to the inherent time constant $\tau = (R_S + R_{SW})(4C_{BB})$ of the N-path filter.

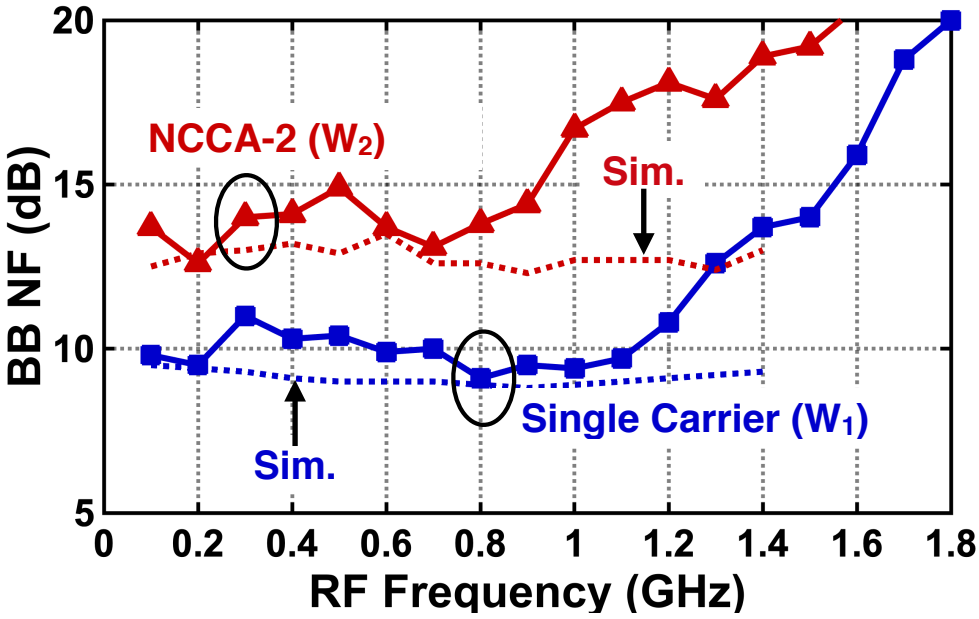


Figure 3.17: Measured NF for SC mode and NC-CA as a function of RF frequency.

Fig. 3.17 plots the measured NF for single carrier (W_1) and NCCA (W_2) modes. For the single carrier mode, the typical NF value is around 10 dB due in part to the NF of the baseband amplifiers. When NCCA mode is enabled at 40 MHz offset from the LO, the NF degrades by 2-5 dB depending on the RF frequency. The NF increase of 3 dB is anticipated due to the noise folding from the image of the LO modulated at the chip frequency. Note that the DSB NF can be achieved by using image rejection DSP techniques in post-processing. Alternatively, adding a ultrawideband sub-2 dB NF LNA before the chain could improve NF at the expense of the blocker tolerance [39][40].

To test the linearity of the receiver, two in-band tones are applied at 1.5 MHz and 2 MHz offsets from f_{LO} for the single carrier mode with f_{LO}= 900 MHz while the IM3

is observed at BB at 1 MHz. The extrapolated IIP3 is -14.5 dBm while OIP3 is +19.4 dBm. For NCCA mode, the in-bands tones are applied at 1.5 MHz and 2 MHz away at 40 MHz offset from f_{LO}= 900 MHz and with chip rate of 80 Mcps, similarly the IM3 is observed at BB at 1 MHz giving an IIP3 of -9 dBm and OIP3 of +15.6 dBm. The IIP3 of NCCA mode is about 5 dB better than SC due to the 5 dB addition to the filter IL.

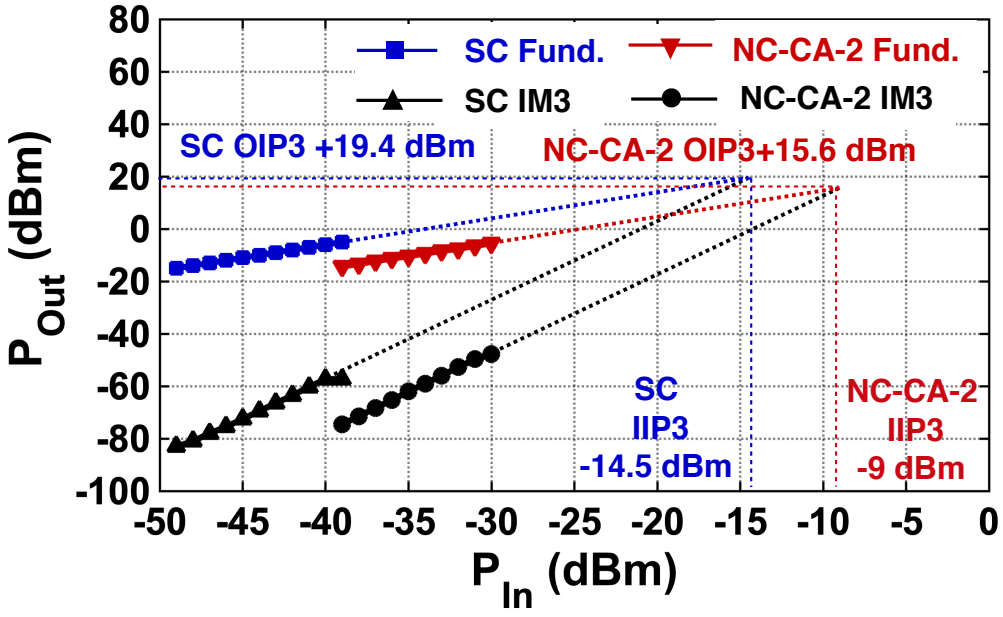


Figure 3.18: Measured IIP3 for SC and NC-CA modes

3.4.1 Single Carrier Rejection

A -30 dBm QPSK signal with a symbol rate of 1 Mbps is located near f_{LO} of 900 MHz modulated at a chip rate f_c of 100 Mcps. Fig. 3.19 shows the spectrum at the BB output for an RF signal located at f=f_{LO}+53 MHz. The signal is downconverted with around 30 dB of gain. When the signal is moved adjacent to the LO at f=f_{LO}+3 MHz, the signal is rejected by 49 dB relative to the maximum conversion gain. Despite the proximity of the interferer to the LO, the PN-modulated LO provides significant rejection to improve the channel selectivity of the SCRX.

Fig. 3.20 shows the conversion gain for out of band harmonics normalized to the aggregation from fundamental frequency. The worst case is at the third harmonic of around 10 dB. When applying the pulse shaping technique discussed in Section II the third-harmonic rejection is improved by 27.3 dB at the cost of increased IL by 1.3 dB and higher conversion gain at higher harmonics of the chip code.

To evaluate the EVM over the SCRX tuning range, we apply a 1 Mbps QPSK signal with -50 dBm power at 100 MHz offset from the LO in Fig. 3.21. As the LO is swept from 200 to 2000 MHz (f_{RF} from 100 to 1900 MHz), the EVM remains better than -30 dB even above the balun roll-off at 1400 MHz. As the carrier frequency exceeds this balun frequncy, the signal is attenuated but due to the BB gain the received signal remains above the noise floor of the ADC resulting in reasonable EVM values up to 1700 MHz. Sample QPSK constellations are shown in P_1-P_3 for different LO frequencies.

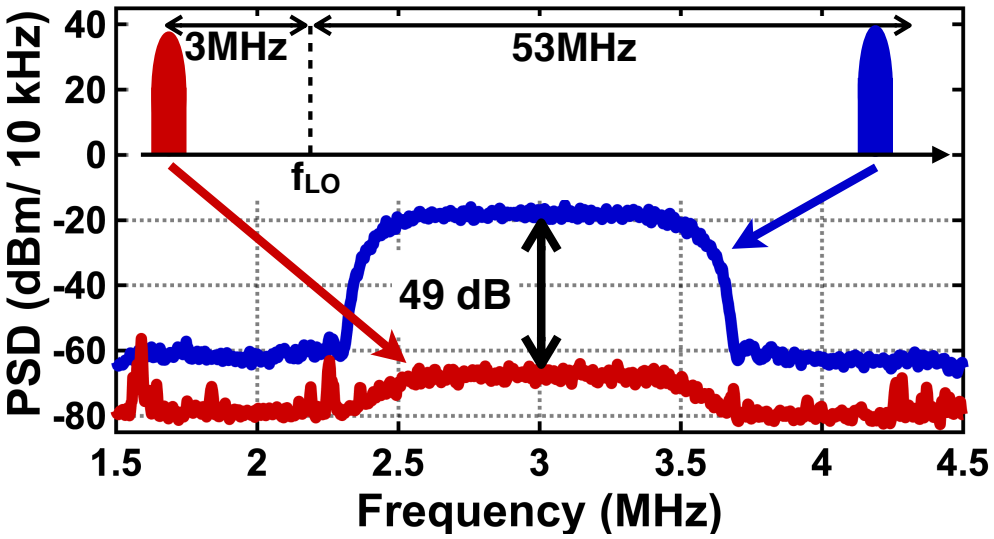


Figure 3.19: Illustration of RF spectrum and measured BB spectrum for different cases at f_{LO}= 900 MHz while applying a Walsh code. Both signals are QPSK 1Mbps at -30 dBm and applied separately.

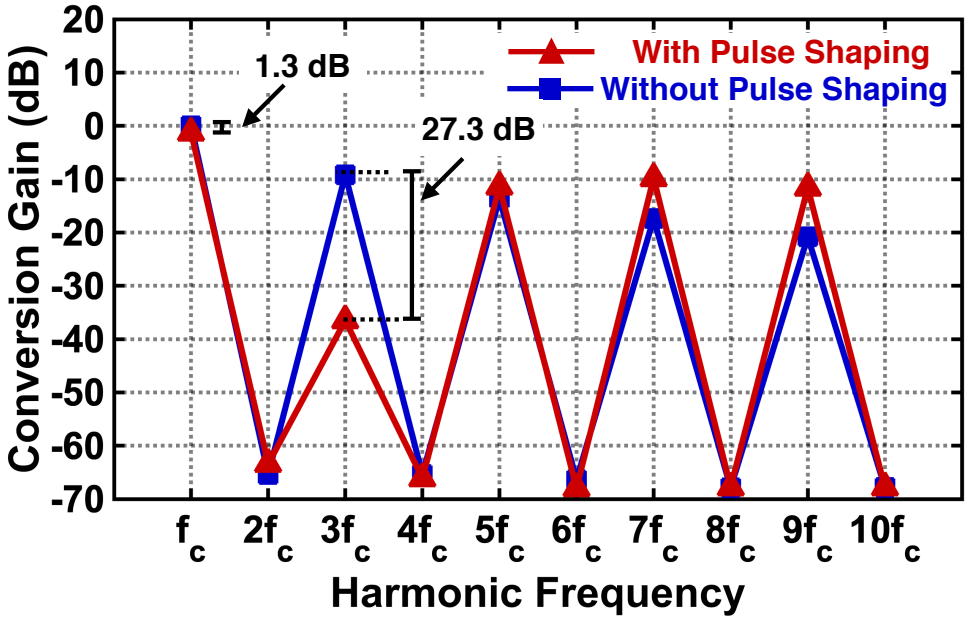


Figure 3.20: Measurement for out of band rejection at different harmonics of the code chip frequency.

3.4.2 Non-contiguous Carrier Aggregation

To test non-contiguous CA with large frequency separation between the RF carriers, two signals are applied with more than 1 GHz offset as shown in Fig 3.22. A continuous wave (CW) at 402 MHz and a 1 Mbps QPSK at 1404 MHz both at -50 dBm power are simultaneously produced at the input. Both tones are down-converted to an IF with a nominal 2 MHz of separation and gain greater than 30 dB.

Next, two carriers are applied at RF with QPSK and QAM. A similar scenario will later be presented for the OTA measurement. The frequency spacing between the aggregated carriers is swept while observing EVM values of the QPSK constellation in Fig. 3.23. For a frequency spacing greater than 1 MHz, the two carriers no longer overlap and the receiver is capable of simultaneously receiving both signals at an EVM of around -34 dB. When the aggregated carriers are 1 MHz offset, they are not overlapping but the adjacent carrier leakage degrades the EVM to around -20 dB. Finally, when the carriers

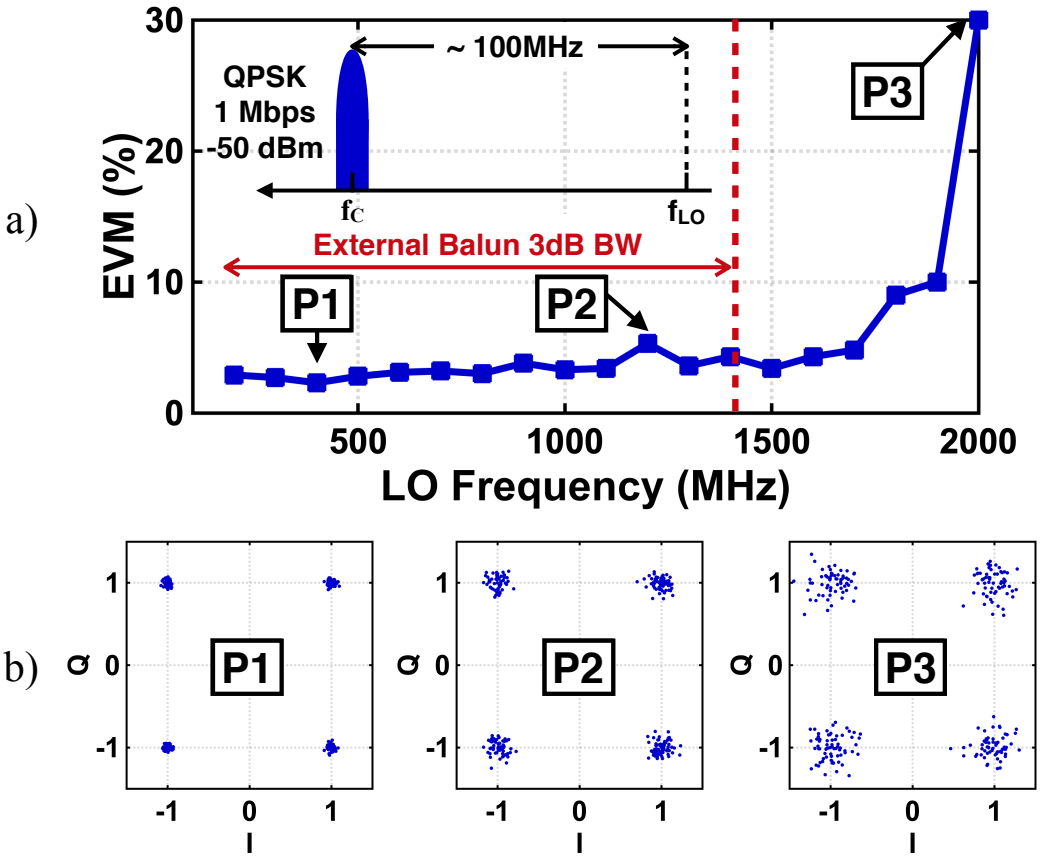


Figure 3.21: Illustration of spectrum at RF_{in} and measured EVM vs f_{LO} frequency (a) and selected measured constellations (b).

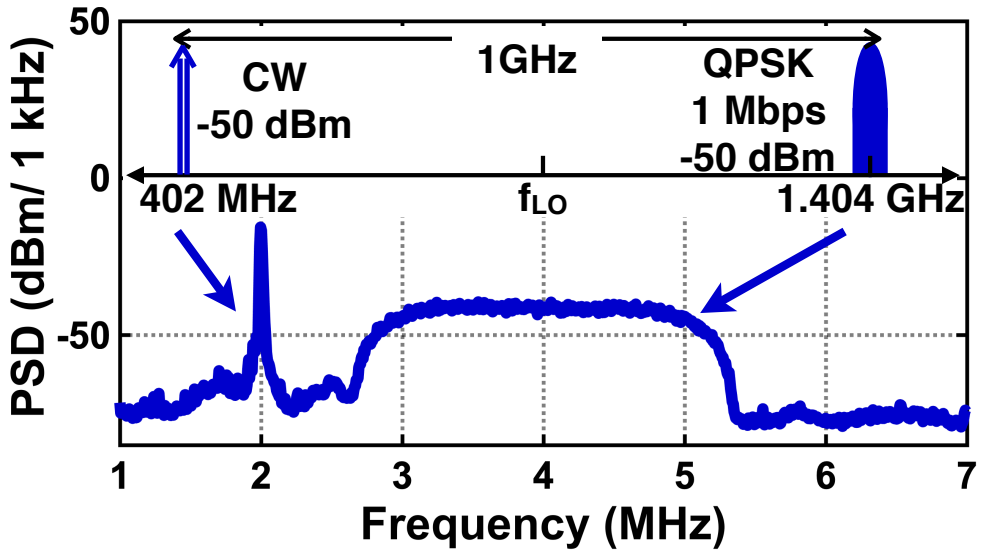


Figure 3.22: Illustration of spectrum at RF_{in} and measured BB spectrum waveform while aggregating two RF carriers separated by more than 1 GHz.

are 0 MHz offset and completely overlapping and the reception is corrupted.

Next, the dynamic range is measured based on the difference between the minimum detectable signal and the 1-dB compression power in Fig. 3.24. The DSP channel equalization is performed once at input power -30 dBm and remains constant for all other power levels. For a QPSK, the EVM at equalization point reaches -40 dB. As the power increases, the EVM degrades to -20 dB at 3 dBm input power. The EVM increases to -9 dB at -86 dBm input power and indicates a 7dB penalty relative to theoretical minimum detectable signal calculations. Sample constellations are shown shown in P_1-P_6. For QAM16, the lowest power level was -77 dBm represented

by P_1 with EVM of -14 dB. Typical EVM of -25 to -30 dB are represented with P_2-P_3. We quantify the dynamic range of the SCRX as better than 90 dB based on the QPSK EVM remaining below a BER of 10^{-3}.

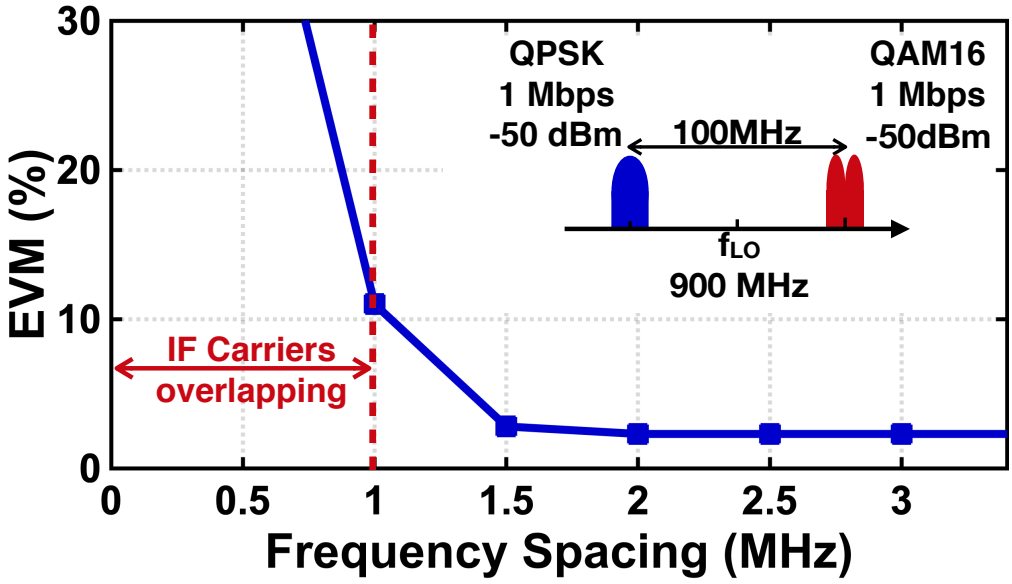


Figure 3.23: Illustration of spectrum at RF_{in} and measured EVM as a function of separation frequency between carriers at BB.

3.4.3 Over-the-Air Measurement

An OTA experiment was performed to to test aggregating two carriers from different transmitters separated by 10 ft. As shown in Fig. 3.25, NI USPR 2900 was used for the first carrier with 1 Mbps QAM16 while a vector signal generator was used to transmit a second carrier with 1 Mbps QPSK. Both TX power levels are set to 0 dBm and corresponds to less than -50 dBm power at the SCRX port. Two antennas (VERT900) with

TABLE I
COMPARISON AGAINST STATE-OF-THE-ART

Spec.	**This work**	[41]	[42]	[2]	[43]	[44]
Process	**45nm**	28 nm	28 nm LP	28 nm	45 nm	65 nm
Frequency (GHz)	**0.1-1.4**	1.4-2.7	1.93 - 1.99	3.3-4.2	1.96-2.04	0.6-2.2
CA Span (GHz)	**1**	0.07	Fixed	0.8	Fixed	210 MHz
Limited by PLL set. time?	**No**	Yes	Yes	Yes	Yes	Yes
Switch Time (ns)	**<25**	NA	10000	NA	NA	NA
CA Sensitivity (dBm)/ Modulation type	**-86/ QPSK -77/QAM16**	-100/ NA	NA	NA/ 64QAM NA/ 256QAM	NA/ QPSK NA/ 64QAM	-70/QAM16
Power Cons. (mW)	**23.1**	34 mA	46	370	15	98.2-115
BB Gain (dB)	**36**	NA	NA	43.5	37	48
NF (dB)	**9.8-17.1**	3.5	5.9	6	3.9	1.3-3.2
IB IIP3 (dBm)	**>-14.5**	NA	NA	NA	-13.7	-12.5
Dynamic Range (dB)	**>90**	NA	NA	NA	NA	NA
OOB Rejection (dB)	**49**	NA	33	NA	> 70	46
Active Area (mm^2)	**0.55**	24.9	0.75	27	0.16	1.1

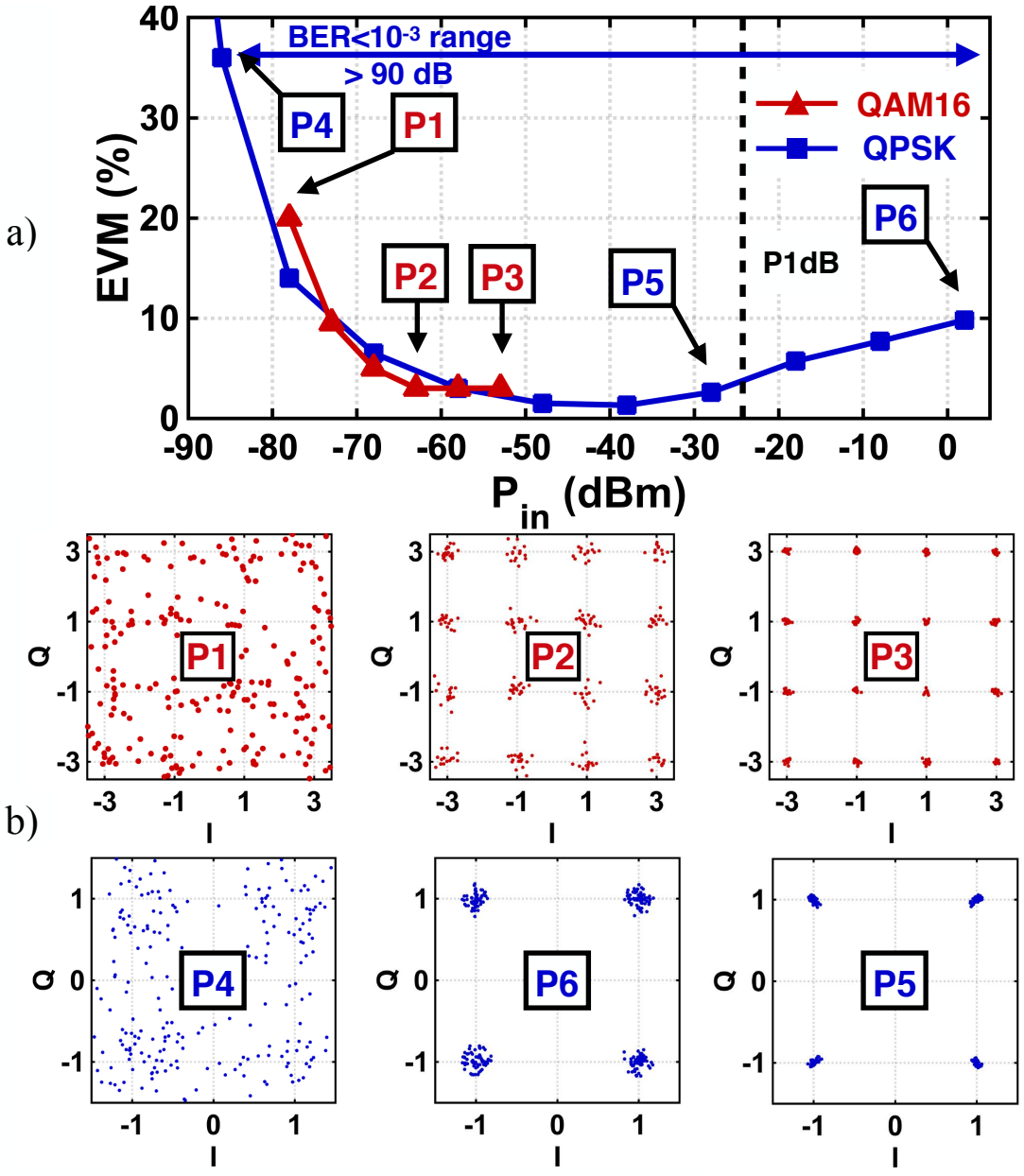


Figure 3.24: Measured EVM vs P_{in} for QPSK and QAM16 (a) and selected measured constellations (b).

center frequency at 900 MHz and 80 MHz BW were used. Due to the limited antenna bandwidth, the two carriers were chosen at 943 and 861.5 MHz to simulate the use of cellular bands for CA. Ferrite circulators (CF1020) were used at the antenna to prevent each carrier reflecting back at TX port of the other carrier. The W_2 code was used with

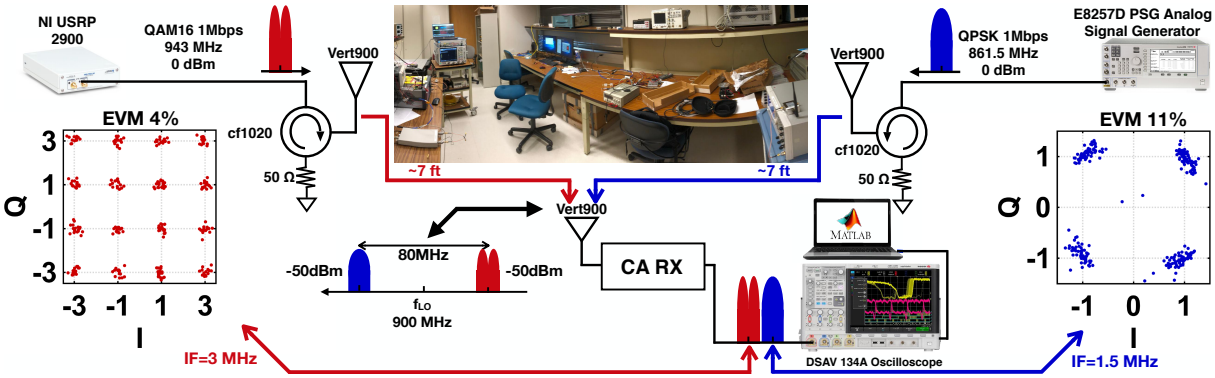


Figure 3.25: Over-the-air experiment set-up and measured constellations and EVMs for both carriers.

160 Mcps resulting in the DUT down-converting and amplifying both carriers at 1.5 and 3 MHz IFs and 0.5 MHz guard channel. The BB nodes are sampled with a realtime oscilloscope to perform EVM evalution in MATLAB. The 943 MHz carrier is down-converted to a 3 MHz IF with EVM of -28 dB.

The 861.5 MHz carrier is down-converted to 1.5MHz IF with EVM of -20 dB.

3.4.4 Comparison with the State-of-the-Art

Table I compares the proposed SCRX with the state-of-the-art for carrier aggregation [2, 41–44] and spectrum sensing receivers. While previous work relies on a PLL to tune for CA, this work eliminates the need to tune and calibrate a PLL. The proposed SCRX achieves significant reductions in power consumption and active area to realize a wideband receiver capable of extremely high dynamic range. The relatively high NF is observed in all previous mixer-first RX circuits [45] and trades off with high OOB IIP3 of the N-path filter or mixer.

3.5 Conclusion

We present a reconfigurable spectrum-compressing receiver capable of non-contiguous carrier-aggregation that eliminates the need for a wideband PLL. The proposed approach uses PN-modulated codes to develop an arbitrary spectrum for mixing with the desired RF channels and strong agreement is demonstrated between theory, simulation and measurement. The proposed receiver demonstrates high dynamic range with a non-zero IF for the N-path filter when receiving CA channels. The instantaneous RF tuning range is more than 1 GHz and is a 100-fold higher that the BW of the BPF due to the PN codes. Over-the-air measurement with an actual antennas and circulators shows EVM better than -20 dB for CA mode.

Chapter 4

Code-Domain RF Signal Processing Front-end

4.1 Introduction

Simultaneous transmit and receive (STAR) within the same band offers the potential to estimate the channel response in multiple-input multiple-output (MIMO) systems and support full-duplex (FD) communication. Additionally, proprietary defense communications systems use spread-spectrum access techniques but do not support FD operation since the co-located transmitter (TX) typically has a peak power level exceeding 33 dBm and produces significant receive (RX) band interference. Even with more than 20 dB isolation between the TX and RX, self-interference (SI) power levels exceeds 13 dBm in the RX path, demanding high in-band linearity (>20 dBm) and high-rejection (>40 dB) at the LNA.

Prior work on STAR has been demonstrated using a variety of RF signal processing techniques [5–7, 30–33, 46, 47] illustrated in Fig. 4.1. In [48], a combination of electrical balanced duplexer with a 3-dB TX power penalty, and analog cancellation before and

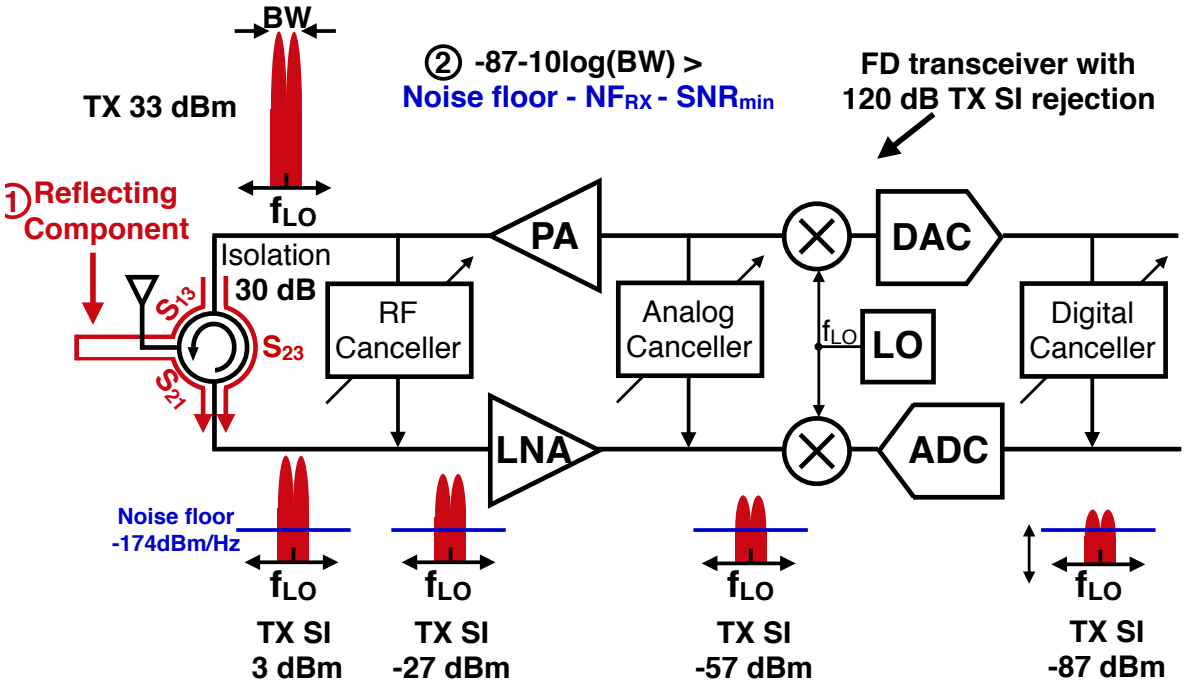


Figure 4.1: Limitations of cancellation in full-duplex systems with transmitter self interference.

after the LNA offers 70 dB of rejection, but is limited to low TX SI power levels to maintain reasonable signal-to-noise ratio (SNR). Furthermore, analog and digital cancellation techniques only address internal leakage interference and do not reject other multiple access interference including multipath TX reflections are nearby transmitters as shown in Fig. 4.1.

An acceptable SNR in the presence of TX SI requires both TX isolation and RX filtering before DSP cancellation is effective. As illustrated in Fig. 4.1, a circulator provides around 30 dB of transmit isolation over a given signal bandwidth, reducing the incident power at the RX to around 3 dBm. However, reflections near the antenna can also prove problematic for low insertion loss between the TX/RX and antenna. If the signal is reflected less than a meter from the antenna, SI could also be on the order of 0 dBm and delayed by several nanoseconds. A nearby transmitter using the same band

poses similar interference concerns.

A code-domain approach ([49]) uses RF signal processing to augment a conventional narrowband transceiver to reject high-power TX SI, multipath, and multiple access interference without placing additional constraints on ADC/DAC resolution and system bandwidth and reducing baseband power. Such a code domain front-end is illustrated in Fig. 4.2 and introduces a TX modulator and RX correlator that filters TX SI before the LNA to relax the linearity requirements. Prior code-domain receivers demonstrated 38.5 dB of rejection [5], however, without the capability of handling strong TX SI (in-band P1dB = -11.8 dBm). Code-domain approaches [5][31] also assume TX coding prior to the power amplifier (PA) which increases the required PA bandwidth to several hundred MHz and limits the overall system efficiency. Furthermore, spreading before the PA does not include the PA non-linearity in the RF canceller (Fig. 4.1) which limits rejection.

This paper presents RF signal processing circuit techniques for a code-domain transceiver with the first fully integrated code modulator and demodulator. In the TX, we demonstrate a high-power, high-switching speed direct sequence spread spectrum (DSSS) modulator for Watt-level signals. In the RX, we demonstrate a high-linearity, high-switching speed correlator based on a hybrid transmission gate switch. With optimum biasing, the chopper switch achieves an in-band P1dB of 12.1 dBm, exceeding in-band linearity of previous N-path implementations which have insufficient linearity to handle strong interferers present in a STAR system [9, 37, 50]. The receive correlator is implemented using an N-path filter [50] with reset circuitry to implement an integrate and dump (IAD) feature to improve rejection and reduce inter-symbol interference (ISI), and lower the system noise.

This paper extends an earlier RFIC presentation [51] to demonstrate analysis and simulation of the high-rejection IAD RX correlator, code construction for synchronization, high power compression of the RF switch, and additional measurements of synchroniza-

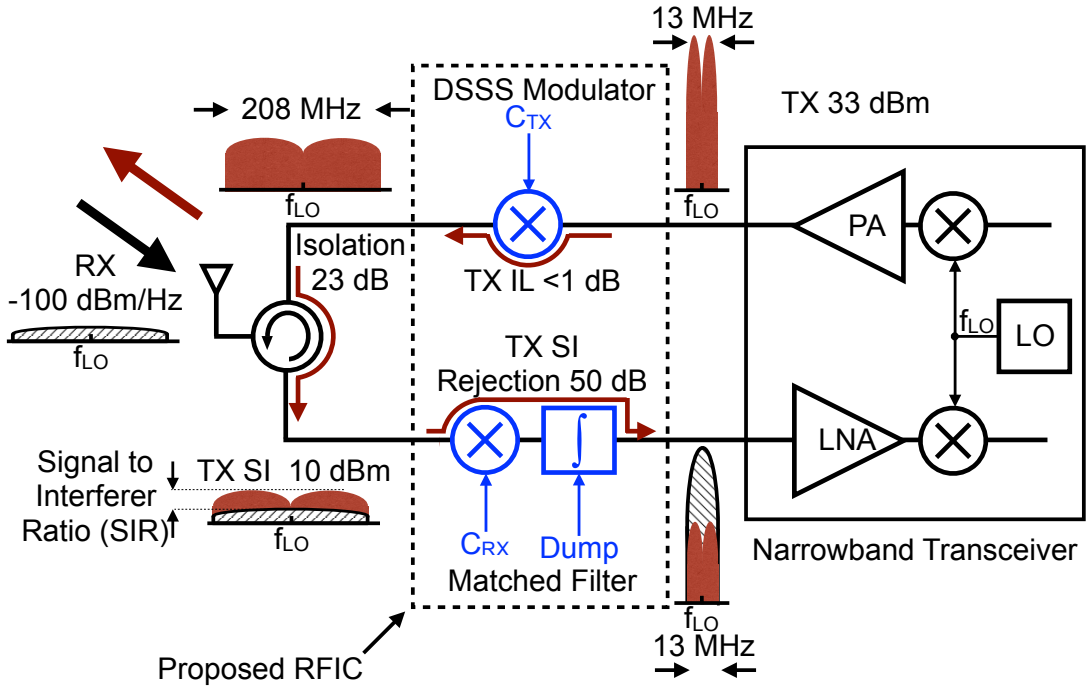


Figure 4.2: Proposed DSSS modulator and matched filter with RF code correlator and integrate and dump.

tion and ISI rejection.Section II discusses the IAD correlator and the benefits to higher rejection of TX SI and multiple access interferers. The following section reviews the circuit techniques for the high-power DSSS modulator, the linear code correlator, IAD filter, and timing circuitry. The measurements demonstrate the rejection of the RX as well as the insertion loss and power handling of both the TX and RX circuitry. EVM measurements indicate that the proposed solution can handle TX power of 30 dBm and rate of 12.5 Mbps with nearly 38 dB of SI rejection while the RX still achieves an EVM under 20% for a QPSK signal.

4.2 Integrate-and-Dump Code RF Signal Processing for SI Rejection

Several problems exist with current solutions for full duplex. Most notably, RF cancellers do not address multipath RX and high-power TX SI as well as in-band jammers. To solve these issues, the proposed approach is shown in Fig. 4.2. In the TX path, the DSSS modulator is a fast, high-power BPSK modulator and multiplies the original TX waveform by a code sequence C_{TX} to spread the signal bandwidth by a factor of L, the length of the code. The TX signal is then isolated from the RX by more than 20 dB using a circulator or duplexer technique.

In the RX path, the RF signal is correlated with code C_{RX}. For matched codes, the RX signal is increased by the processing gain and concentrated within the signal bandwidth. For orthogonal codes, the RF signal is spread out of band (OOB) and the remaining OOB spectral components are rejected by the receive filter as shown in Fig. 4.2. The RX signal must be filtered further before reaching the LNA. With 50 dB of RF filtering, the TX SI is reduced to -47 dBm. Additionally, an RF code filtering approach is capable of rejecting SI as long as the multipath delay is longer than one code chip. In this work, code chip rates of typically 200 Mc/s or around 5 ns are investigated.

The operation of the IAD correlator is modeled in Fig. 4.4. The TX signal is modulated with the TX code and passed through the channel. The input RF signal consists of a modulated signal, $x(t)$, with a symbol period, T_s, mixed with a code sequence $C_{TX}[k]$ that changes every chip period $T_c = T_s/L$. The correlator is multiplied by the RX code and integrated on a capacitor. When the received signal is mixed by the chopper against the RX code sequence, $C_{RX}[k]$, the resulting product is integrated over the symbol pe-

riod. The chopped RF voltage is integrated over L code values.

$$y(t) = \int_{kT_s}^{(k+1)T_s} \sum_{l=0}^{L-1} x(t) C_{TX}[l] p(t - lT_c) \cdot C_{RX}[l+m] p(t - (l+m)T_c + \tau) \mathrm{d}t \tag{4.1}$$

where $p(t)$ is a unit pulse of period T_c and τ is the delay between the code sequences up to T_c. Since the symbol is constant over the integration period, the integrated voltage is

$$y(t) = x(t) \frac{T_c - \tau}{T_c} \sum_{l=0}^{L-1} C_{TX}[l] C_{RX}[l+m]. \tag{4.2}$$

The sum is the cross correlation $R_{C_{TX}C_{RX}}[m]$ between the TX and RX codes. In the case that the codes are matched, e.g. $C_{TX} = C_{RX}$, and the code lag is zero, $y(t) = x(t)\frac{T_c - \tau}{T_c}$. Therefore, the received signal is maximized when the delay between the RX and TX codes is aligned. In the case that the codes are orthogonal, $y(t) = x(t)\frac{T_c - \tau}{T_c} R_{C_{TX}C_{RX}}[m]$. Therefore, the interference is eliminated when the RX and TX codes are shifted to minimize the cross correlation. Consequently, the integration needs to be aligned coarsely over the code sequence and with fine tuning over the code period. To achieve the high rejection in the RX before the LNA, we propose an IAD filter to correlate against the RX code sequence and reject the TX SI and multiple access interference simultaneously.

The IAD is reset after each code correlation interval to eliminate ISI of rectangular pulse shape and improve the autocorrelation with the desired code and reduce crosscorrelation between the desired RX code and undesired TX code. The IAD improves the ability to reject TX SI but requires synchronization to appropriately correlate the desired RX signal in the IAD filter.

The spectrum of the cross-correlation between the TX and RX signals is shown in

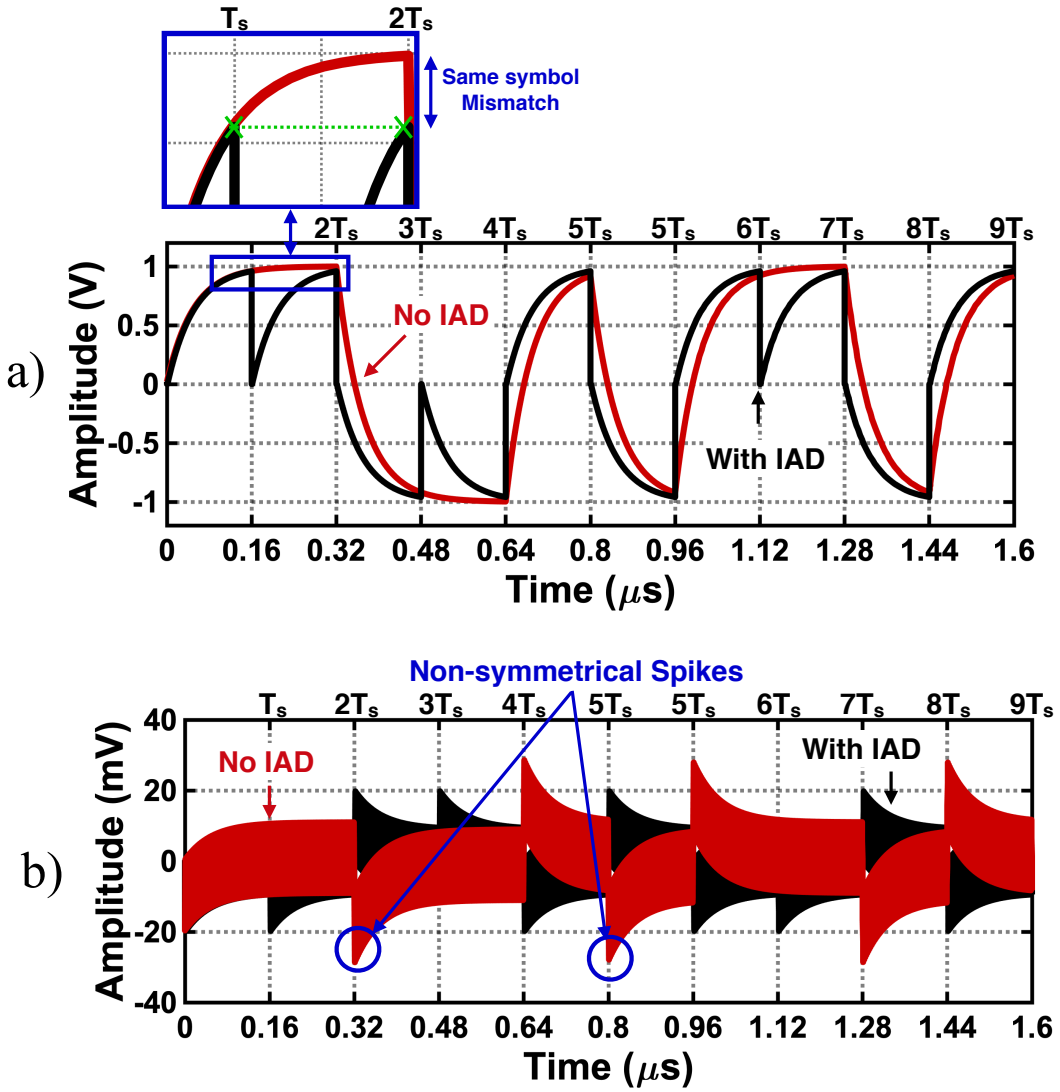


Figure 4.3: Simulation of integrate-and-dump: a) Improvement of auto-correlation b) Improvement of cross-correlation.

Fig. 4.4 with and without the IAD function. Within the signal bandwidth, the IAD rejects the signal power by around 8-10 dB. The IAD increases the signal power out-of-band (OOB) due to the dump switching function. However, baseband filtering can reject the OOB signal components. The figure also indicates the rejection of the signal as a function of the baseband capacitance. As the baseband capacitance increases, the rejection is improved. In theory, the rejection is increased by more than 10 dB over the

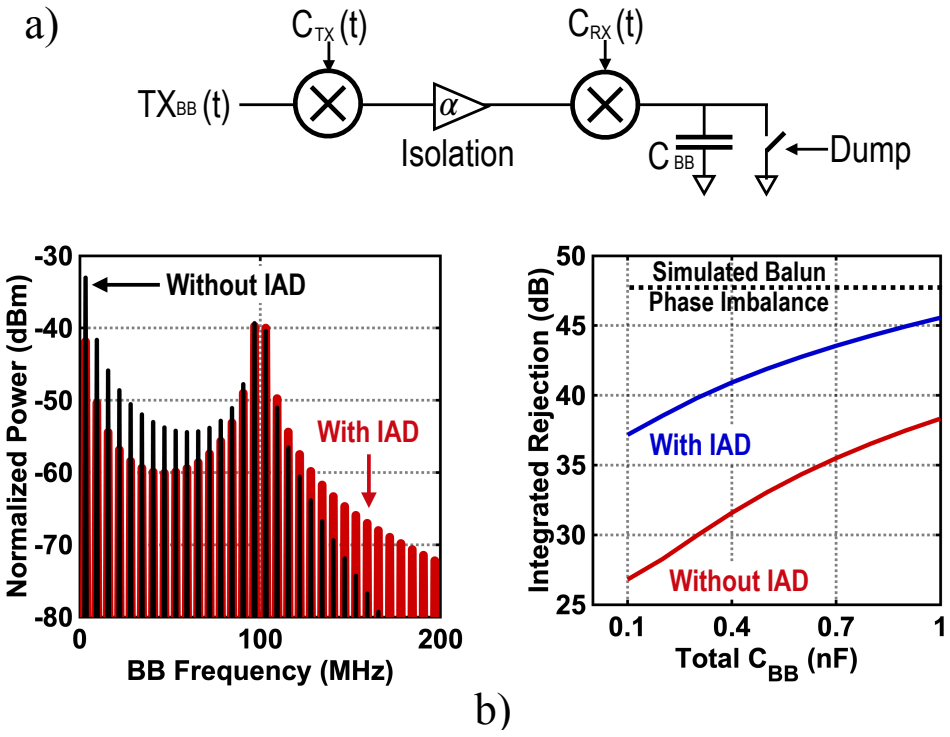


Figure 4.4: Simulated rejection with and without IAD using Walsh codes.

range when the IAD is activated.

To address the need for synchronization of the RX code against the desired signal in the IAD filter, the choice of code impacts the synchronization. Walsh codes have excellent orthogonality properties due to near zero cross-correlation between the codes when aligned and yielding high TX SI rejection. However, their auto-correlation properties are poor resulting in two challenges. First, it is difficult to determine the beginning of the code impeding synchronization and the ability to receive the desired RX. Second, after synchronization is achieved, multi-path components [4] of RX can appear at the RX port and disrupt the received signal resulting in deep channel fading. A sample of a Walsh code of length 16 is shown in Fig. 4.2 a) while its auto-correlation function (ACF) is plotted against lag showing no clear peak.

Barker codes, on the other hand, have an ACF with a distinct peak as shown in

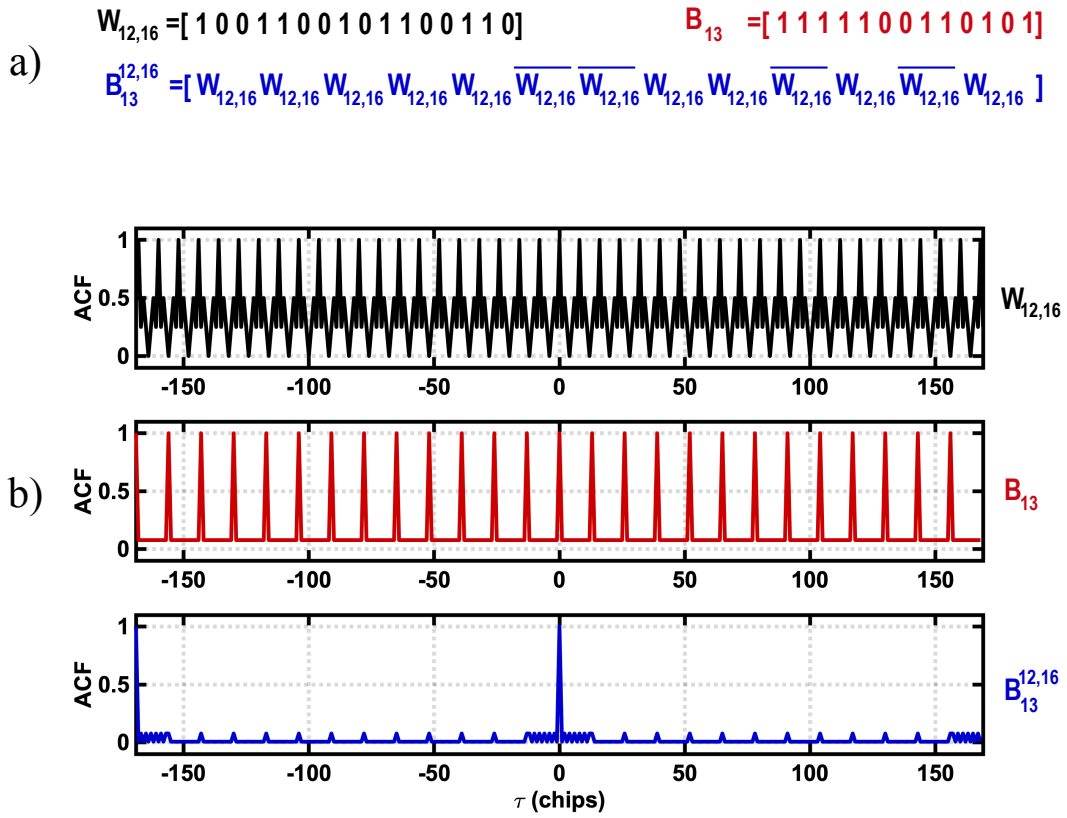


Figure 4.5: Construction of a nested Barker code and Walsh code and resulting ideal autocorrelation.

Fig. 4.2 with non-zero rejection. To synthesize codes with both advantages, prior work proposed [5] to multiply a Walsh code with a Gold code to achieve better ACF properties. While this technique provides good ACF, the resulting code has finite rejection limited by the Gold code due to "multiplying" the two codes. Here, we propose the repetition of a Walsh basis code that alternates phase based on a Barker code sequence as shown in Fig . Now the ACF has a clear peak and high rejection over most lags while maintaining excellent orthogonality against different Walsh codes.

Unfortunately, the ideal Barker code autocorrelation is limited by the ability to perform correlation in the RF domain. Rather than integrate with a windowed function, the *RC* time constant of the integration becomes a non-ideal limitation. Fig. 4.6 compares the simulated auto-correlation function (ACF) of a Barker code based on first-order *RC*

filter against ideal filter for a 11 length code. Due to the non-ideal filter shape compared to ideal integrator, the ACF is asymmetrical across the peak. Specifically, when the multiplication of the original Barker with the shifted code yields quickly charging and discharging the capacitor, the ACF is lower than ideal. Reducing the capacitor size yields faster charging and discharging of the capacitor resulting in lower ACF similar to Fig. 4.4. This motivates RF signal processing that approximates the ideal ACF based on an IAD function.

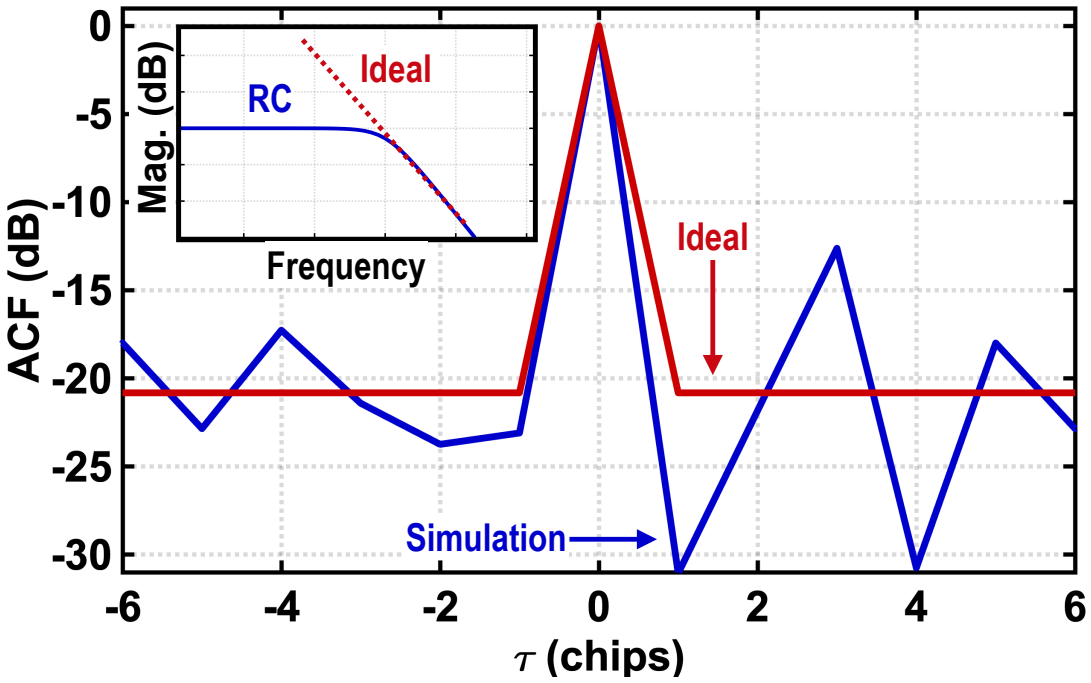


Figure 4.6: Simulated auto-correlation function of RC-limited Barker code.

Another circuit non-ideality is the amplitude and phase mismatch of the balun. By adding an imbalance around the RF correlator, Fig. ??b illustrates the maximum TX rejection as a contour plot of the amplitude and phase imbalance at 1 GHz. To achieve a rejection of 50 dB, a total phase imbalance of less than 2 degrees and amplitude imbalance of less than 1.25 dB must be satisfied.

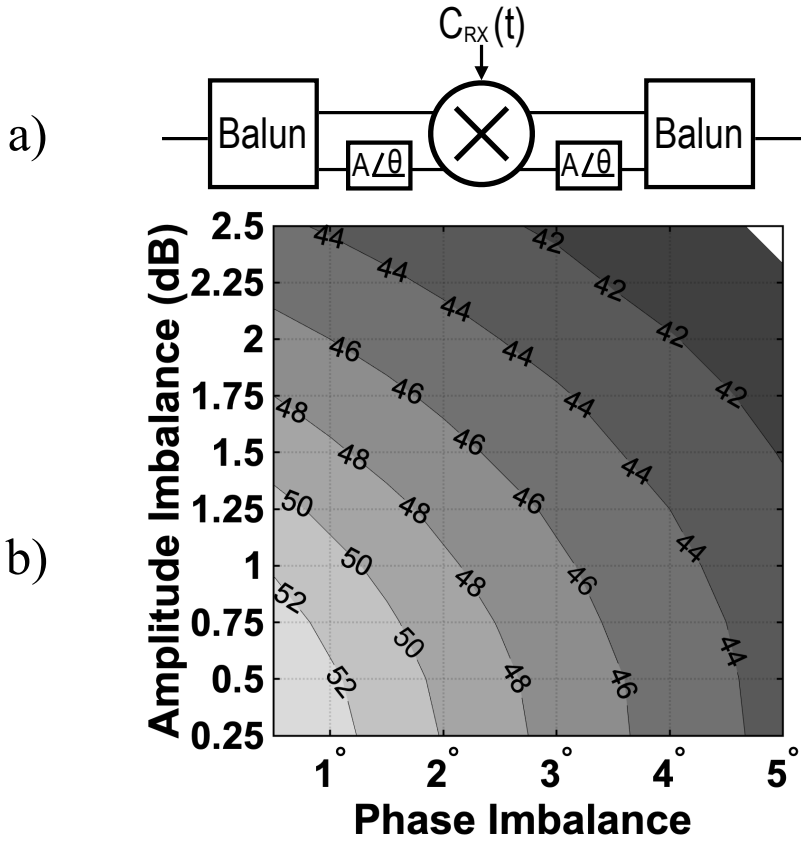


Figure 4.7: Setup for phase and amplitude imbalances a) and rejection due to code cross-correlation as a function phase and amplitude imbalance b).

4.3 Code-domain Transceiver Circuit

Fig. 4.8 shows a block level diagram of the proposed transceiver chip with off-chip passive components for code-domain signal processing. The transmitter consists of a pair of high-power RF switches designed to add a PN code as a BPSK signal. The receiver is designed to realize RF-domain code domain signal processing with high input power compression. Both transmitter and receiver were integrated on a single die to share the code generation circuitry and simplify synchronization between the TX and RX. The transceiver is built upon the high-power and high-linearity RF switches available in the 45-RF CMOS SOI process. These switches have an $R_{ON}C_{OFF}$ product on the order of

130 fs and support the low loss RF signal processing functions.

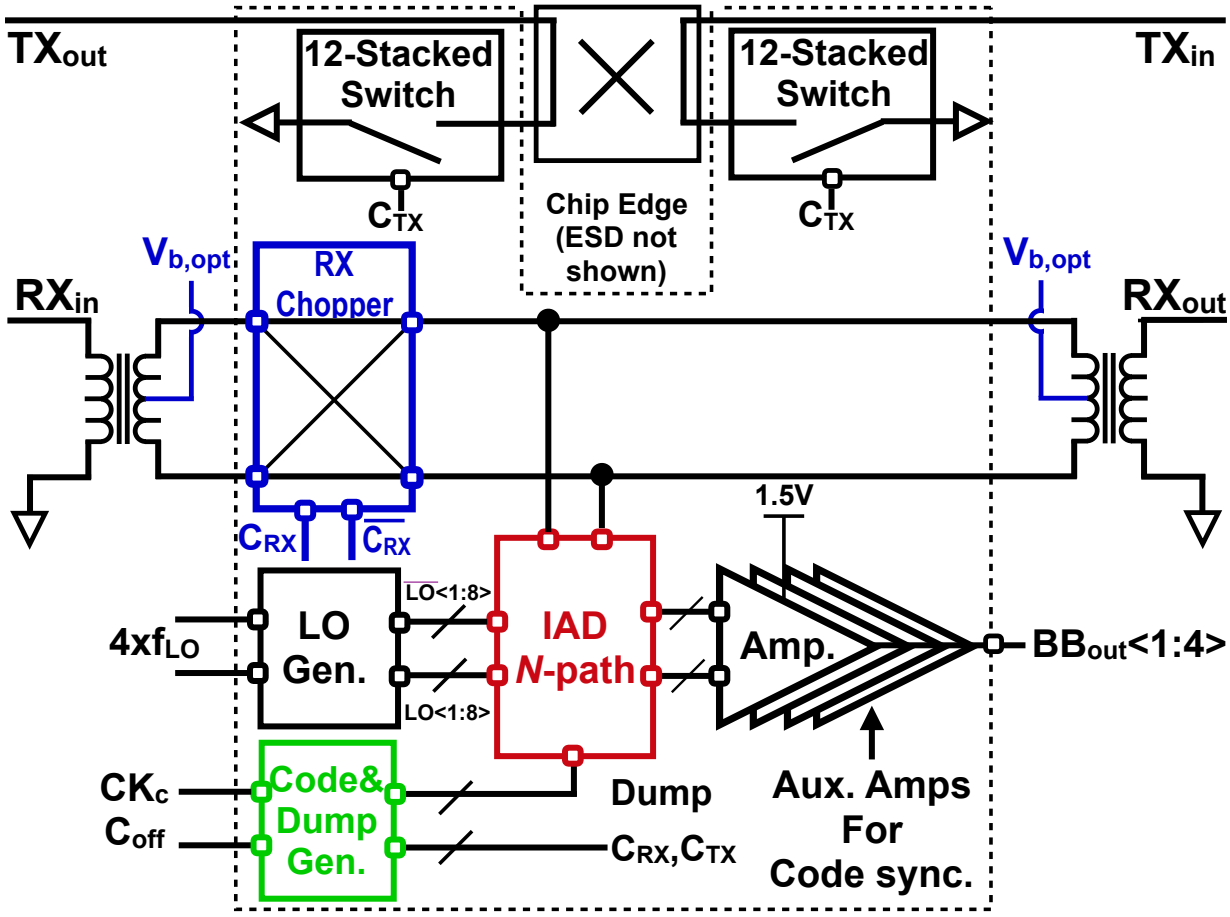


Figure 4.8: Block diagram of the code domain transceiver for STAR applications.

4.3.1 High-power TX Modulator

The TX DSSS modulator includes two 35-dBm RF CMOS SOI switches connected to the isolated and coupled port of an off-chip 90° hybrid coupler. The principle of the BPSK modulator is presented in [52] and uses a reflection phase shifter to alternate between 0 and 180 degree phases. When turned off (open), the switches create an in-phase reflection and produce no phase shift on the RF signal. When turned on (short), the switches produce a 180° reflection. The use of open and short reflections adds additional

design challenges in the RF switch design since the open reflection doubles the incident voltage while the short reflection results in a high current through the switch.

To handle the high voltage under the open condition, the RF switch is based on a 12-stack CMOS SOI FET with 1.8mm NFET and auxiliary PFET/NFET switches shown in Fig. 4.9 (a) and sized according to the 12-stack switch in [52]. The device stacking distributes the voltage swing between the transistors and prevents breakdown without inhibiting switching speed [53]. The progression of drain voltages across the switch devices is shown in Fig. 4.9 where it is clear that the voltage drop across each device is approximately 1 V. Most notably, tapering the size of the B and C devices in the auxiliary switches supports high power handling along with high switching speeds on the order of 3ns for high fractional bandwidth. To differentiate this design from [52], the high-power switches are integrated onto the same silicon die as the receiver circuits posing additional design challenges since the overall usable space for wide ground planes and multiple wirebonds are required to maintain a low ground impedance when the switch is on and high currents are passed through the chip. Even relatively small wire-bond inductance becomes an issue at high RF power levels at 1 GHz since the switches are driven with standard CMOS logic levels, e.g. 0 to 1 V, and voltage ripple in the ground plane can lead to premature device turn-off and therefore power compression.

The effect of wirebond inductance on power handling is simulated in Fig. 4.9 (c) which shows that power handling is limited to below 35 dBm even with ground inductance as small as 400 pH at 1 GHz. To mitigate this problem, large area of decoupling NCAPs were used to connect the digital ground/power and RF ground planes. Additionally, multiple ground pads were placed on perpendicular edges of the chip to minimize inductive coupling and overall ground inductance between them. This can be seen later in Section IV, Fig. 4.15. To prevent additional interference in the RX path from the TX signal, the TX modulator and RX correlator are constructed with separate on-chip

grounds which are connected together off-chip.

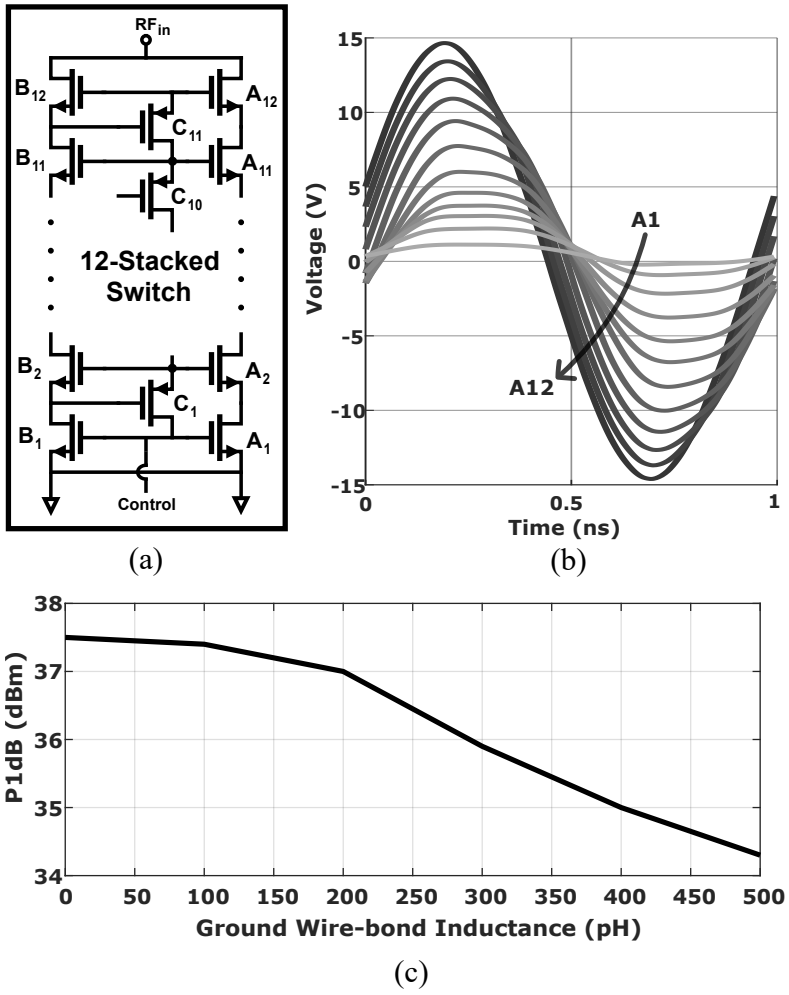


Figure 4.9: Diagrams of (a) the circuit used to build the high-power switches, (b) the drain voltage on each subsequent primary A device, and (c) the simulated compression point of the modulator for different wire-bond inductance.

4.3.2 High-linearity RX Correlator

Demodulation of PN codes have been incorporated with N-path filters in LO modulation [5, 8] as well as turning on and off the switches [30]. In the RX path of this work, the incoming RF signal is modulated with a chopper to correlate the RF signal against a desired code sequence. As opposed to earlier work on code-domain signal processing with

N-path filters, the chopper is designed to minimize insertion loss (IL) while maintaining high linearity at the code chip rate, rather than at the LO frequency. Schematics of the RX chopper and IAD N-path filter are shown in Fig.4.10. The chopper resembles the structure of a FET ring mixer but the gates are driven with the code sequences at up to 200 Mc/s. Since the code sequence is around one-fifth the LO frequency, the linearity of the chopper switch is improved with transmission-gate (TG) switches, which will be subsequently discussed.

After chopping the signal, the RF signal has either been spread out of the signal bandwidth in the case of an undesired signal or has been concentrated in the case of the desired signal. Now, the signal is then passed through a high-Q bandpass filter to eliminate the OOB spectral components. The filter is realized as a differential 8-path that incorporates an integrate-and-dump (IAD) switch to reset the N-path filter capacitors after the correlation against a code sequence. The processed correlated signal is available at the RF output port for a conventional receive path as well as for demodulation from sampling the voltage on the N-path baseband capacitors (in contrast to current-mode [37]) and amplifying the desired signal. The on-chip baseband receiver becomes a necessary feature for aiding in the synchronization process.

The IAD feature is built into a standard N-path filter as a switch which equalizes the differential voltage on the N-path when the dump signal is active to reset accumulated charge and avoid ISI resulting from the imperfect integration of the correlated circuit. As shown in Fig. 4.10, the IAD N-path filter has a hybrid capacitor bank [16] with high-density capacitors and shunt capacitors to improve OOB rejection and common-mode noise generated on chip (e.g. LO leakage, dump leakage, etc.).

A frequency domain simulation of the high-linearity chopper and N-path filter is plotted in Fig. 4.11 for matched and unmatched codes. The plot compares the use of an ideal balun with the characteristics of an SMT balun model. Notably the balun does

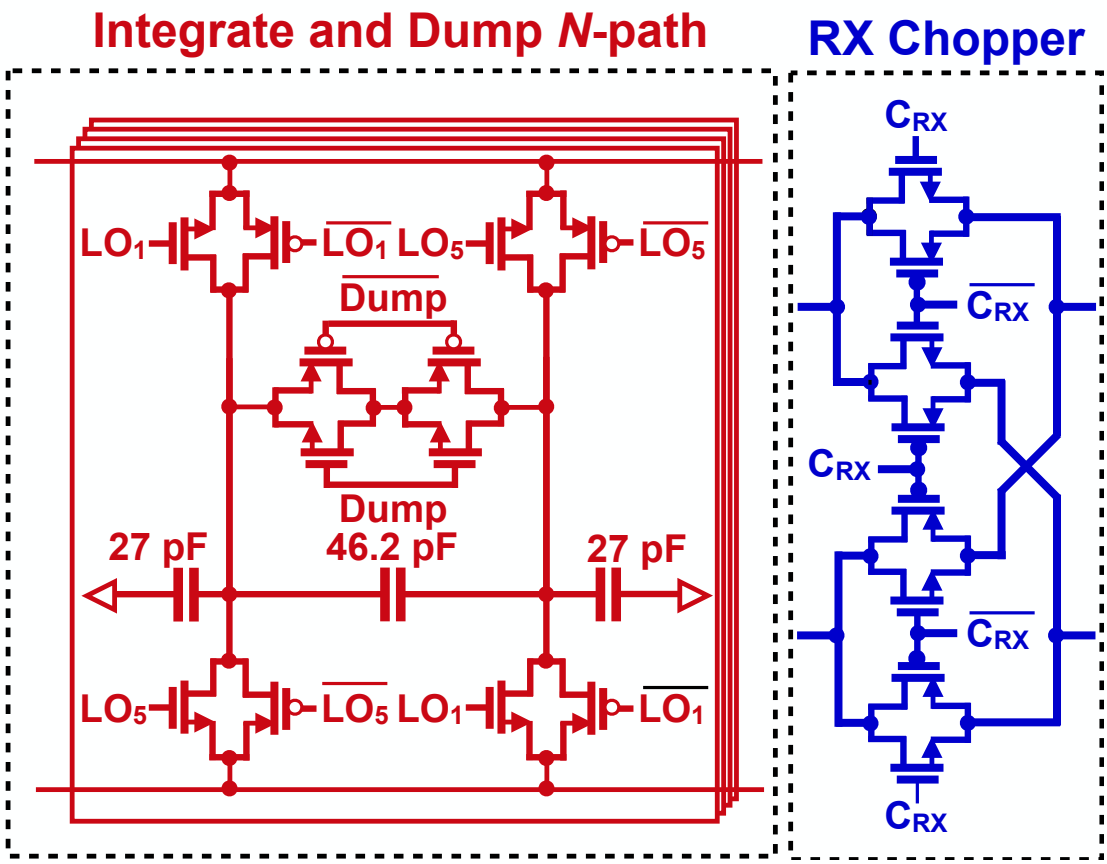


Figure 4.10: Circuit schematics for RF receiver blocks including the 10-dBm RX chopper and a single path of the integrate and dump N-path filter.

not strongly effect the OOB spectral characteristics for unmatched codes but the in-band signal power difference is substantial. While the ideal balun offers a rejection of 60 dB, the real balun model reduces the potential rejection to around 50 dB.

4.3.3 High-linearity RF TG Switch

While NFET devices are typically preferred for RF switches, high-linearity suggests that scaled CMOS devices should have relatively flat on resistance when the switch is conducting. Consider the series on device in a double-pole double-through (DPDT) switch based on NFET. The opposite polarity switch remains off for low amplitude voltages of

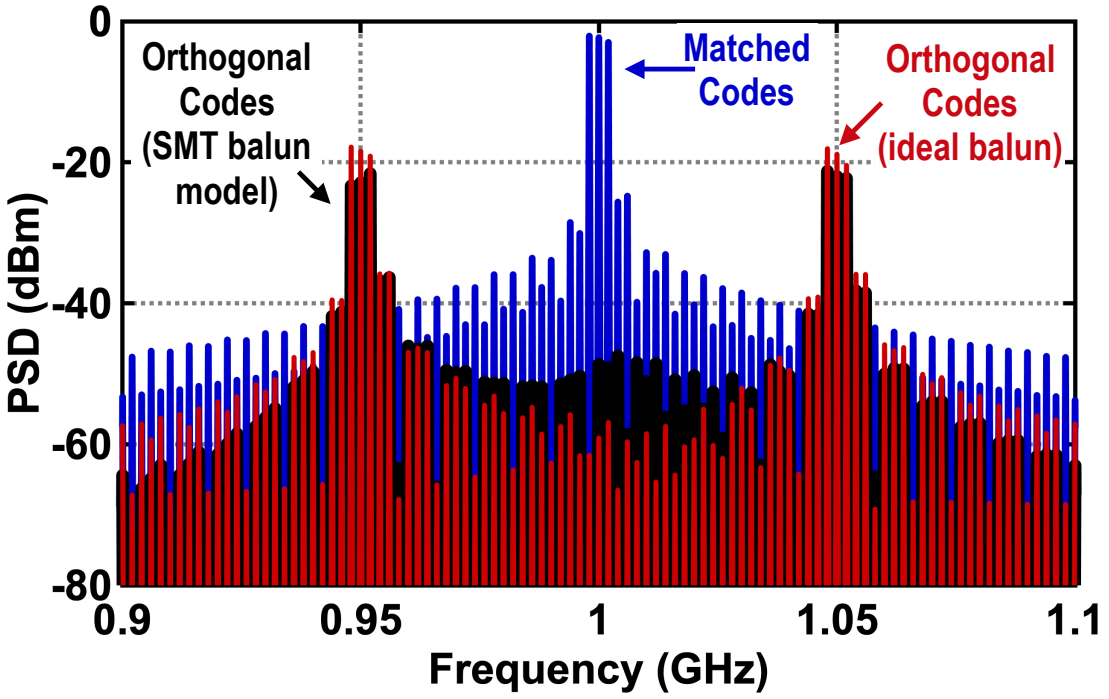


Figure 4.11: Simulated spectrum for matching and orthogonal codes and the effect of non-ideal balun on rejection

the input signal. In other words, the gate-source voltage of the off switch remains less than the threshold voltage ($V_{GS} < V_{TH}$). As the amplitude of the input signal increases, the off switch conducts undesirably resulting in compression due to the source terminal swinging below $-V_{TH}$ due to the logic low $V_L = 0V$. In this case, the P1dB might be estimated to be associated with a voltage swing of V_{TH}. In a scaled CMOS process, $V_{TH} \approx 0.3V$ and the P1dB is around 0 dBm, which generally agrees with prior work [50]. Sub-threshold conduction and other body effects might lower the actual measured value. A conventional practice improves the large signal linearity is through a negative-voltage generation (NVG) so that $V_L < 0V$ allowing the larger signal swing before conduction is observed. A challenge with implementing this technique is the large settling time of the NVG compared to LO period less than 1 ns making this only feasible with relatively slow switching speeds such as found in transmit/receive (T/R) applications.

Fig. 4.12 shows the simulated switch on resistance for a PFET which predicts an opposite trend from the NFET. While the flatness of NFET and PFET is poor around their respective bias points, the TG has a flatter on-resistance improving the small signal linearity (IIP3). The ratio of sizing is chosen to maximize the flatness. As the amplitude of blocker signal increases, the switch resistance drops and increasing filter's OOB rejection.

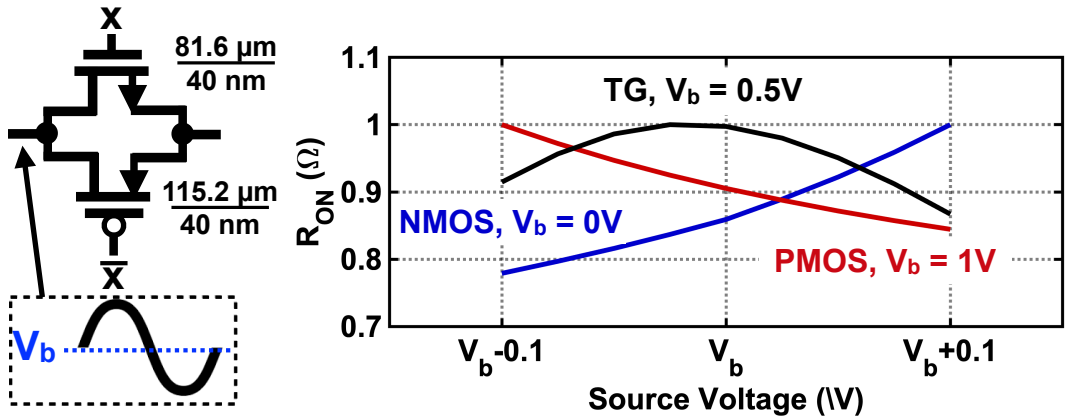


Figure 4.12: TG implementation and normalized switch on resistance vs bias voltage of TG, NMOS and PMOS switches

An alternative improvement is to bias the input signal at a voltage level higher than 0 V to allow larger input amplitude without hindering the switching speed. This comes at a cost of increased switch resistance and insertion loss (IL). A bias of $V_{DD}/2 = 0.5V$ improves the P1dB to 8 dBm. The RF TG switch comprises back-to-back PFET and NFET, as opposed to a single NFET, as illustrated in Fig. 4.12. Other recent work also proposed using TG switches and measured an in-band 1-dB power compression (P1dB) of -17 dBm ($\Delta f/BW = 0$) [34]. Our simulations and measurements of the TG RF switch based on a CMOS SOI design in Fig. 4.13 demonstrate that a properly designed TG RF switch extends the in-band P1dB to 10.1 dBm with an optimum bias ($V_b = V_{b,opt}$) that maintains the proper state of the switches (i.e. on/off) under high RF swing. All TGs

are of the same size as shown in Fig. 4.12.

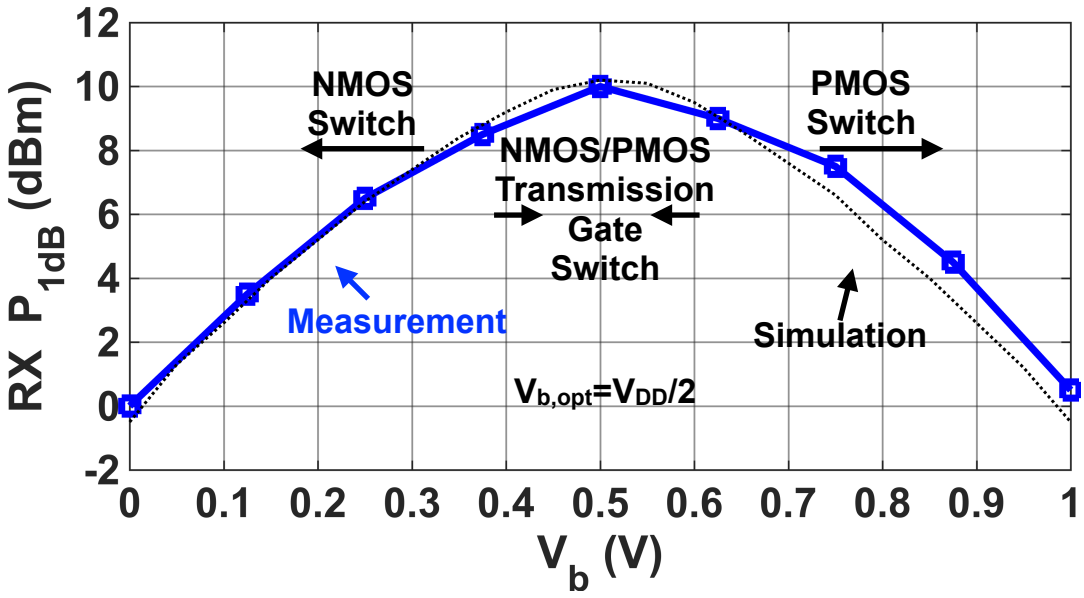


Figure 4.13: Simulated and measured 1-dB power compression of the receive front-end vs bias voltage.

4.3.4 Code Time Alignment and Synchronization

The chip also includes CMOS-based clock circuitry to generate non-overlapping clocks to drive the switches of the N-path filter. The code and dump signal generation produces signals to drive the RX chopper, dump switches and DSSS modulator. On-chip logic generates Walsh (for a better rejection) and Barker codes (for synchronization phase) as well as a bypass for an off chip code.

PN codes have been used in CMOS transceivers [5, 17, 22, 30–35] but mostly without on-chip generation or code time alignment. The on-chip clock generation includes 4 bit coarse tuning for control on the order the chip period T_c of C_{RX} and fine tuning on the order of T_{LO} of C_{RX}. Additionally, the logic will select between Walsh or Barker codes or a specific sequence from the Walsh codes. Control logic enables or disables the dump function in the IAD as well as the source of the code sequence. Fig. 4.14 shows details of

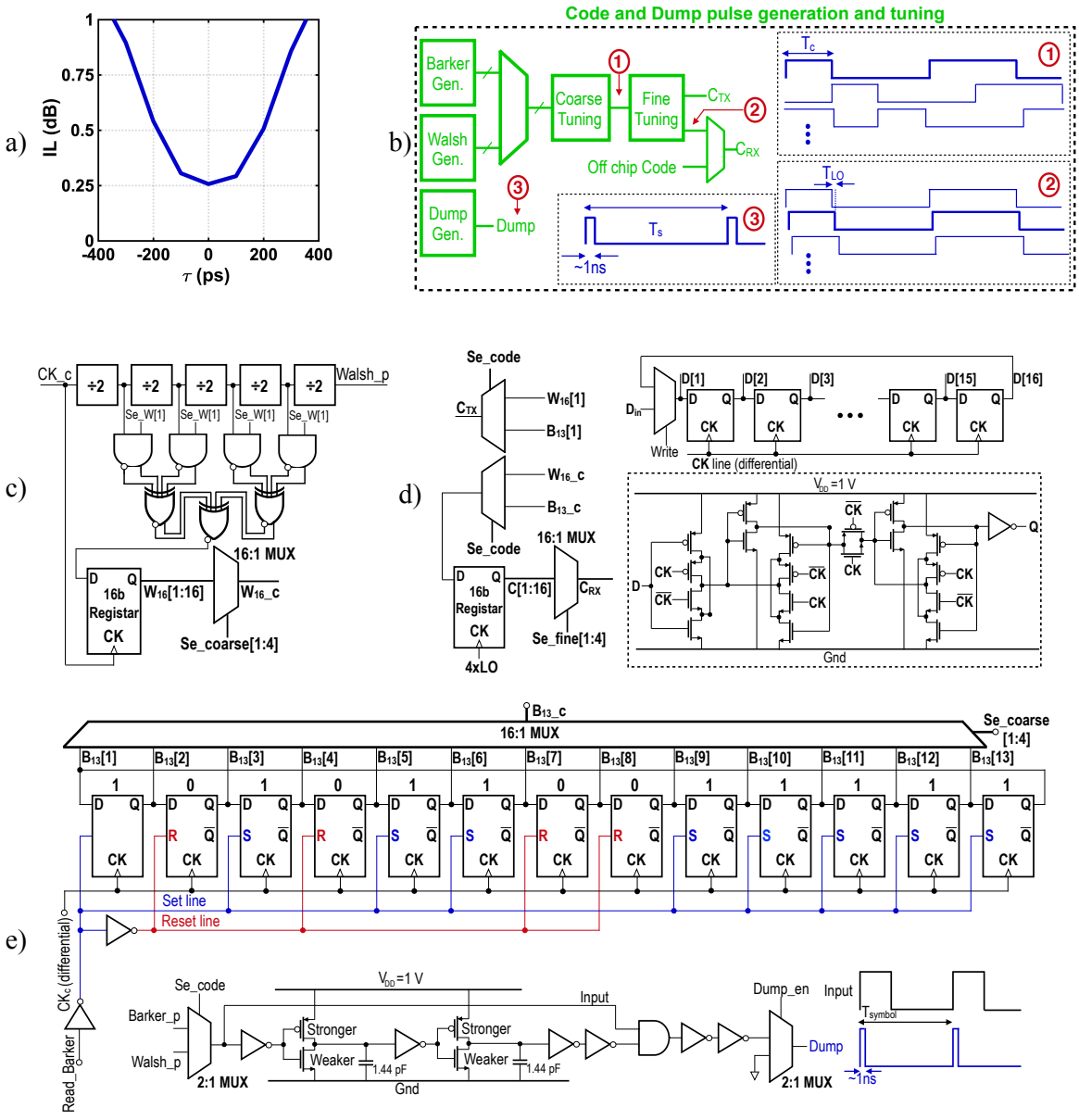


Figure 4.14: IL of matched codes as a function of delay mismatch between codes at T_c=10ns a) Block diagram of on chip generation and tuning for codes and dump pulse b) Walsh code generation c) coarse tuning of Walsh code and fine tuning d) Barker generation and its coarse tuning and e)

code generation circuitry. A 16 bit register is used as illustrated in Fig. 4.14 to change a generated code from serial to parallel (S/P) sampled with a CK equal to 4xLO used in LO generation giving a fine resolution of 1 ns. A 16:1 MUX is used to select the desired

resolution. Details of the register and its D-flip flops are also shown in Fig. 4.14.

A slower CK_c is used as a reference clock. A desired member of Walsh family is selected by setting Se_W to the desired value while a square pulse Walsh_p with a rising edge at the beginning of the code triggers the dump pulse generation to be discussed shortly. Then the code sequence is passed through a 16-bit register clocked with CK_c to provide a coarse tuning.

The metastability of the DFF introduces an imperfection that limits the rejection. A second mechanism of reduced rejection is duty cycle distortion of the codes due to meta-stability of sampling DFF. Simulation shows a potential distortion of about 5 ps for codes changing chips right before the CK edge while no distortion is noted for codes changing after the CK edge. With a maximum of 16 DFF for the registers, chip period should be limited to 0.8 ns to ensure no degradation to rejection of 40 dB.

4.3.5 Dump Pulse and Barker Code Generation

Fig. 4.14 shows the details of dump pulse generation on chip. While the code generation can be selected between on chip of form an off chip code, the generation of dump pulse entails a number of challenges. First, the dump is periodic with a relatively slow frequency equal to the symbol rate yet the pulse needs to be brief in order to make the RF losses minimum. second the pulse can't be too short due to the finite on switch resistance of the dump switches. The time constant is $\tau = R_{on}C_{BB}$ and the pulse width is chosen to be about $4\tau = 1$ns. All these make it desirable to limit the generation of the dump pulse to on chip. As shown in Fig. 4.14 a MUX selects the reference for the start of the dump pulse to either the Walsh or Barker code.

The selected pulse is passed through a delay element with around 1 ns then the original pulse and delayed pulse are passed through AND gate. The delay element is

chosen to be a skewed inverter allowing delay during falling edge only with an added load capacitance. The size of weaker NMOS and its load capacitance are chosen to give the twice time Constant as the BB capacitors and main switches. Careful attention must be paid when routing the dump signal due to rich harmonics content. After the dump is generated, a MUX is used to enable the pulse for comparison.

Fig. 4.14 shows details of the Barker code generation. Since a Barker code is unique and has an odd length, it can't be generated with an even length shift register as demonstrated for the Walsh code. It is generated however by a pre-programmed unique cascade of different variations of DFFs chosen in a reversed order as the bits of the Barker code. The DFF for bit value "1" is called a set DFF and forces an output of "1" when set is high, while the dual is called a reset DFF and forces an output of "0" when reset low. When a Read-Barker control is enabled, set and reset functions are disabled and the previous value stored in the DFFs (which is the desired Barker code) is rotated with a 16bit register with chip symbol equal to CK_c.

The 13 outputs of the tailored register are passed through a MUX to select the desired coarse tuning. Due to mismatch in the number of input and outputs, the outputs are repeated at the end based on cyclic prefix algorithm. To generate the Barker_p with rising edge at the beginning code, a second tailored 13 bit register is used with "1" at the beginning followed by zeros. The outputs are passed through a similar MUX and coarse tuning and not shown in the figures for brevity.

4.4 Measurements

The proposed code domain transceiver was fabricated with GlobalFoundries 45-nm RF SOI process. The die is shown in Fig. 4.15 and occupies an area of 2.59 mm^2 including the pads and ESD circuitry while the active area is 1.12 mm^2. The RX power

consumption was less than 18 mW including digital circuitry at $f_{LO} = 4f_{RF} = 4$ GHz and code rate of 200 Mcps from 1-V supply and four baseband amplifiers from the 1.5-V supply.

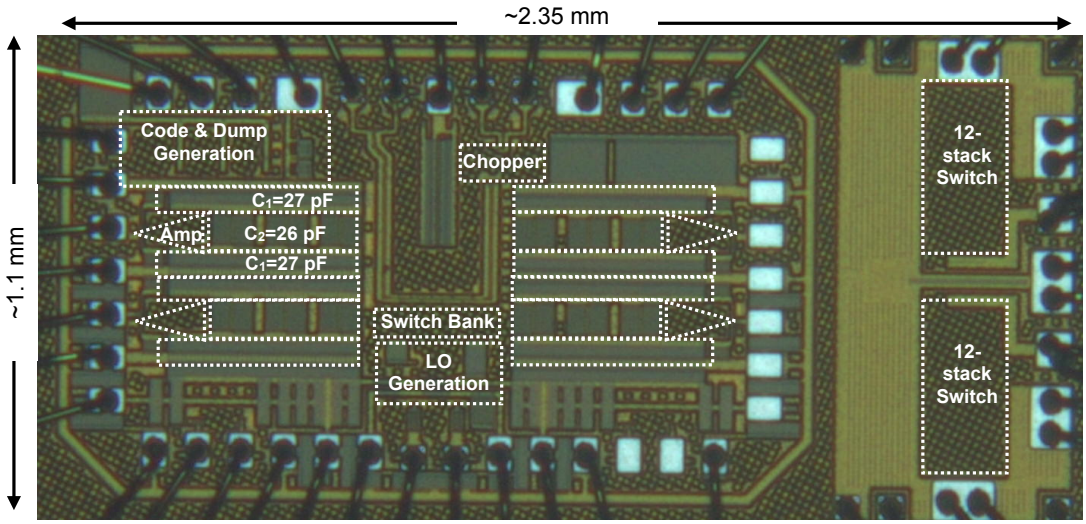


Figure 4.15: Chip microphotograph of the code-domain transceiver.

The TX modulator 1-dB bandwidth extends from 400 MHz to 1 GHz and insertion loss (IL) is less than 1.6dB up to a 1-dB power compression of 34 dBm at 600 MHz as shown in Fig. 4.16 (top). The simulated insertion loss indicates good agreement in terms of the IL and the power compression. The switching time is under 3 ns which enables a 300 MHz spreading bandwidth. The TX IIP3 is measured to be 50 dBm using a two-tone measurement setup.

The IL of the RX correlator is 0.8-3.55 dB across a tuning range from 0.4 to 1.1 GHz with P1dB of 10.1 dBm and 12.6 dBm depending on the balun impedance ratio as shown in Fig. 4.16 (bottom). The simulated RX IL closely agrees with the measurement. The in-band IIP3 is better than 23.1 dBm across the tuning range Fig. 4.19 shows the best and worst IIP3 across the tuning range. The NF for the measured RX_{out} is between 2.6 and 5.6 dB depending on f_{LO}. The gain of the auxiliary amplifiers is measured to be

around 30 dB. The measured RF signal 3dB-BW of the RX correlator is 13 MHz.

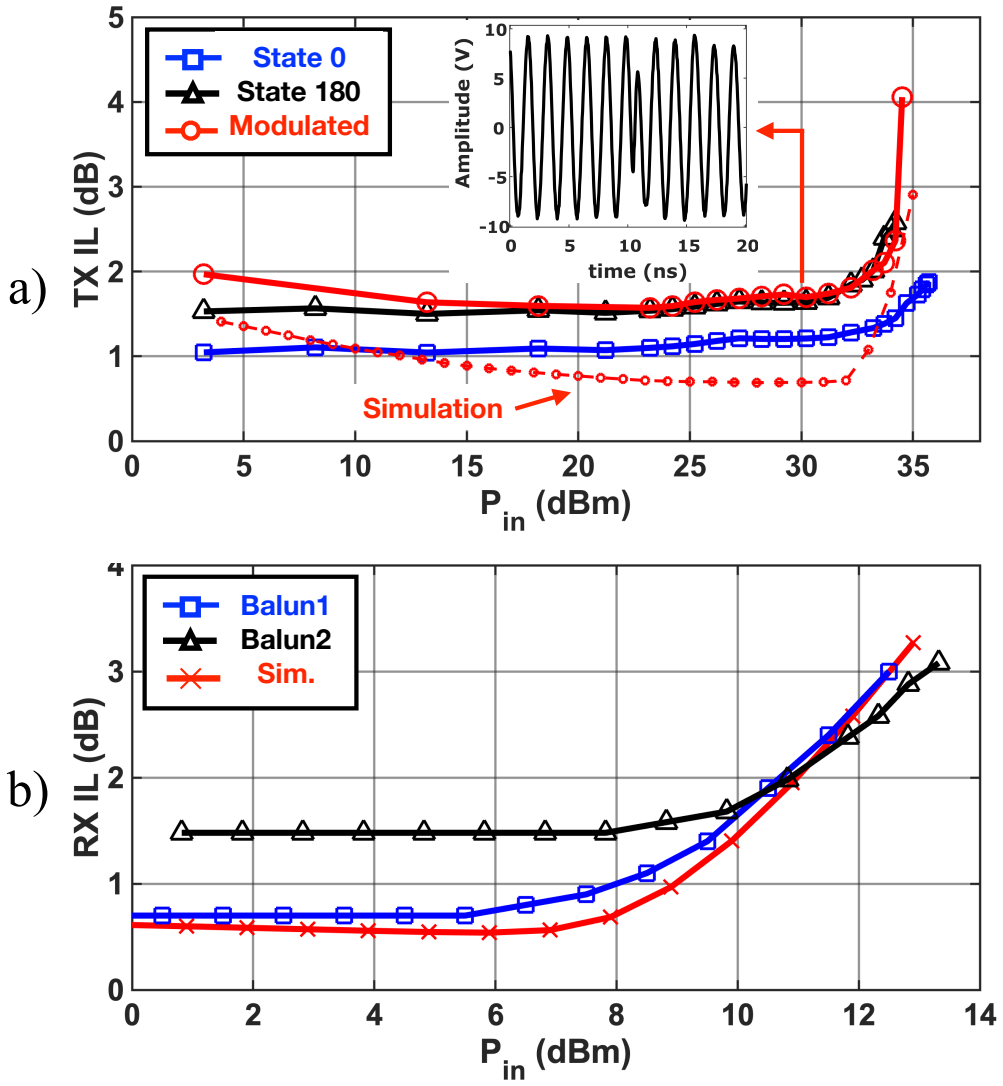


Figure 4.16: Measured in-band IL compression point of the transceiver RFIC: TX (top) and RX (bottom).

Fig. 4.17 plots the spectrum for matched and orthogonal Walsh codes (code lengths of M = 64) for a QPSK signal with symbol rate of 3.125 MSps resulting in a spreading BW of 100 MHz. The autocorrelation of the matched codes concentrates the power into the signal bandwidth. Correlation against the orthogonal code spreads the undesired signal power out of band, in this case, into two peaks 50 MHz above and below the

carrier frequency. When measured within the signal bandwidth, the rejection is 47 dB.

The measured rejection is plotted on Fig. 4.17 (bottom) for varying data rates but fixed spreading bandwidth of 100 MHz. The rejection is 49.5 dB for a 0.5 GHz CW signal and reduces to 42 dB for a 12.5 MSps with the on-chip DSSS modulator operating at 30 dBm. At a 1 GHz carrier, the rejection is around 40 dB and reduces slightly with higher symbol rates.

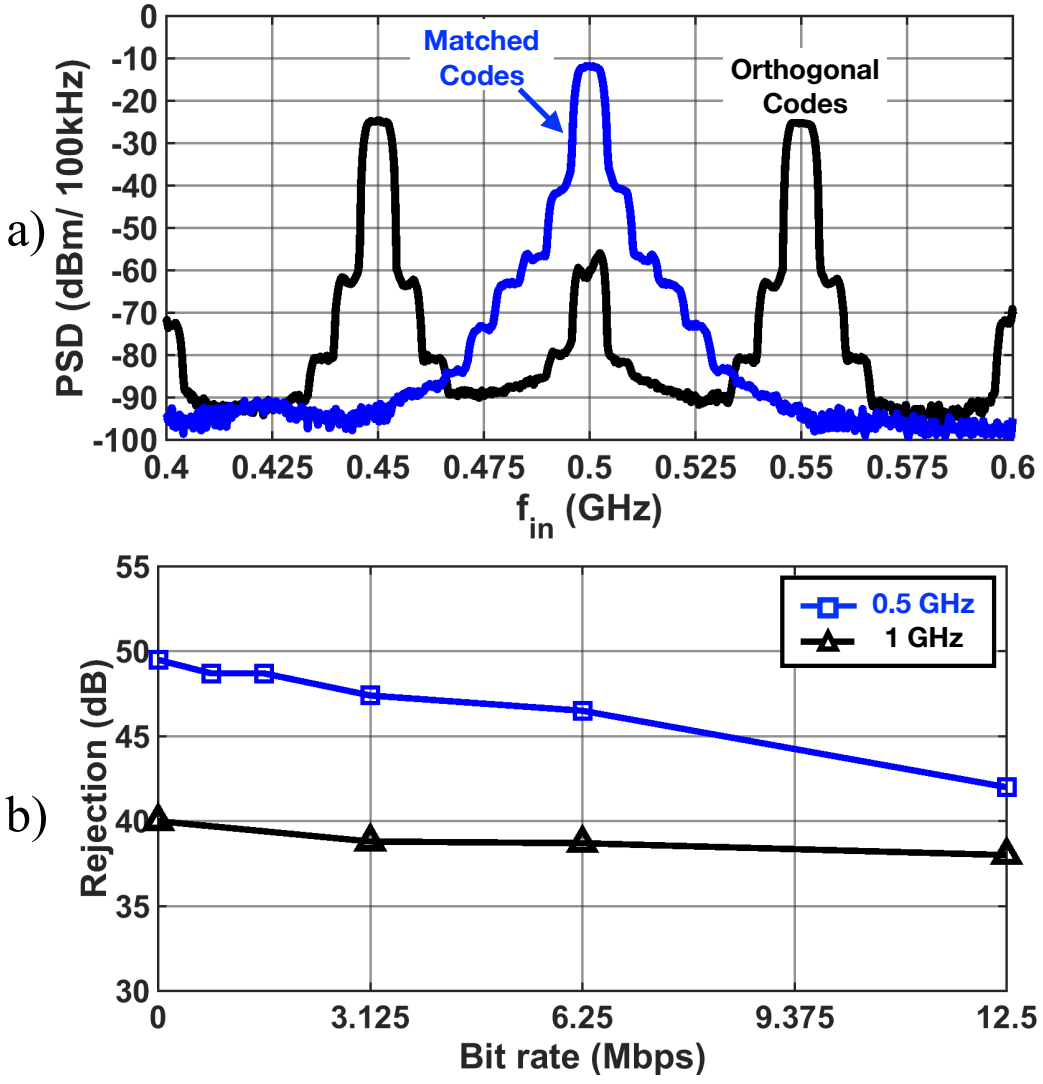


Figure 4.17: Measured spectrum for matched and orthogonal codes (top) and orthogonal rejection as a function of data rate.

To characterize the RX correlation in the presence of both a desired and undesired signal, the EVM is recorded as a function of the signal-to-interference ratio (SIR). The signal power is maintained at a constant level to keep the SNR of the desired signal constant while the interference power is increased. The EVM is plotted as a function of the signal-to-interference ratio (SIR) in Fig. 4.18 for a RX signal power of -18 dBm when the TX and RX are both at 0.5 GHz. For SIR greater than 30 dB, the noise floor limits the EVM (i.e. SNR $\approx$ 30 dB) to around 1%. In the absence of any TX rejection, the EVM degrades to 10% as the SIR reduces to 18 dB. When RF correlation is applied, the EVM curve is shifted by 38 dB such that the same EVM is tolerated for an SIR of -28 dB. The QPSK (bit rate of 12.5 Mbps for RX and 12.4 Mbps for TX) constellation is shown for TX SI of +10 dBm.

Fig. 4.20 a) plots the measured improvement in rejection for a rectangular pulse shape when enabling the integrate-and-dump filter due to the elimination of inter-symbol interference (ISI). In Fig. 4.20b), a CW tone is dumped every 160 ns introducing asymmetric voltage offset that results in reducing the rejection. However, a modulated signal introduces ISI between the symbols. The dump voltage offset still introduces asymmetry, however, it is lower than the measured ISI plotted in Fig. 4.20c) showing input and output wave-forms with and without IAD. When the RF signal modulated with a BPSK signal, the use of dump reduces most of the residual ISI, improving rejection by more than 8 dB. This is expected as the IAD is the ideal matched-filter for rectangular pulse shape. It should be noted that using raised-cosine pulse shape or Gaussian pulse shape provide better rejection at the cost of the need of a matched filter while the IAD provides the required matched filtering before the ADC without the need of a separate filter. The 8-dB improvement in the rejection is extended from QPSK to 64-QAM waveforms when the IAD is enabled.

Fig. 4.22 shows the measured output of the code generation circuitry for different

coarse timing values. To facilitate measuring with 50 Ω equipment, buffers are implemented on the PCB with ADA4817 OpAmps. Due to limited slew rate of the buffers, the chip code is limited at this setup, code generation is verified up to 1 Gcps. Fig. 4.21 shows the measured output of code generation for different fine tuning steps to demonstrate the resolution of around 1 ns when the 1 GHz LO.

Finally, we demonstrate the STAR operation over a short-range link with two prototype RFIC circuits mounted on PCB. We investigate code synchronization for the receiver which was not fully addressed in earlier work [5]. Fig. 4.23 demonstrates an over-the-air (OTA) measurement of the proposed STAR system when the transmit and receive signal are at 900 MHz. Transmitter TX_A transmits a CW tone at 900MHz modulated with a 100 Mcps Barker code of length 11. An off-the-shelf circulator isolates the TX and RX. After propagating over a 1-m channel, the signal is received at receiver RX_B and correlated against the 11 possible timing lags for the Barker code through the observation receiver. The delay mismatch between the two transceivers (T_1) can be estimated by interpolation between the highest two peaks in the autocorrelation function. The variation in the receive power indicates a processing gain of the RX signal of at least 12 dB. The asymmetry across the peak in Fig. 4.23 is attributed to the non-ideal RC shape of the filter compared to an ideal integrator. Nevertheless, this filter shape is accurate to identify the highest peak.

Table 1 provides a comparison with the state-of-the-art work on full-duplex transceivers. The proposed code-domain transceiver provide higher rejection at the antenna while also handling higher power levels and higher levels of integration. Furthermore, this work demonstrates the highest N-path linearity in terms of 1-dB compression for in-band blockers.

TABLE I
COMPARISON AGAINST STATE-OF-THE-ART

Spec.	[5]	[54]	[55]	[30]	[31]	[8]	[56]	This work
CMOS Process	65 nm	65 nm	180 nm	45 nm	45 nm	45 nm	65 nm	45 nm
Frequency (GHz)	0.30-1.40	0.61-0.97	0.86-1.08	0.30-0.675	1.10-2.50	0.90-1.10	0.40-1.00	0.40-1.10
BW (MHz)	1	20	6.8-37.4	10	1	300	NA	13
TX-RX isolation (dB)	0	20	25-40	0	31	0	NA	0
Pre-LNA SI Rej. (dB)	0	0	0	23.2	20	21.9	33	49.5
Post-LNA SI Rej. (dB)	38.5	0	0	0	0	0	0	0
BB SI Rej. (dB)	0	0	0	0	0	0	0	0
TX SI (dBm)	NA	-26	-5 to +10	NA	NA	NA	NA	+10
IB RX P1dB (dBm)	-11.8	NA	21	2	NA	NA	NA	+12.1
IB RX IIP3 (dBm)	>17	-26	36.9	6.3	NA	21.6	NA	>+23.1
RX Power Cons. (mW)	37	36	NA	28.2	50	9.37	24	18
TX Power Cons. (mW)	NA	59	170	NA	NA	NA	24	<40
TX P1dB (dBm)	NA	8	+30.7	NA	15	NA	NA	+34.3
TX IL (dB)	NA	1.8-3.2	2.1	NA	NA	NA	NA	1.6
Active Area (mm^2)	0.31	0.94	16.5	0.9	1.4	1.77	3.1	1.12

4.5 Conclusion

This paper presented a fully-integrated code-domain transceiver consisting of a TX DSSS modulator and RX RF matched filter with a correlator and integrate-and-dump N-path filter that improves rejection by reducing self-interference, multiple access interference, and inter-symbol interference. The RFIC was fabricated in GF 45nm CMOS RF-SOI process and achieves the highest reported spread-spectrum modulator TX power handling of $>$ 34 dBm and receive path P1dB and IIP3 of better than 10 dBm and 23 dBm respectively for in-band blockers while maintaining less than 60 mW power consumption. We demonstrate an acceptable EVM for TX signals as strong as 10 dBm. An over-the-air link demonstrates the synchronization of the RX IAD filter.

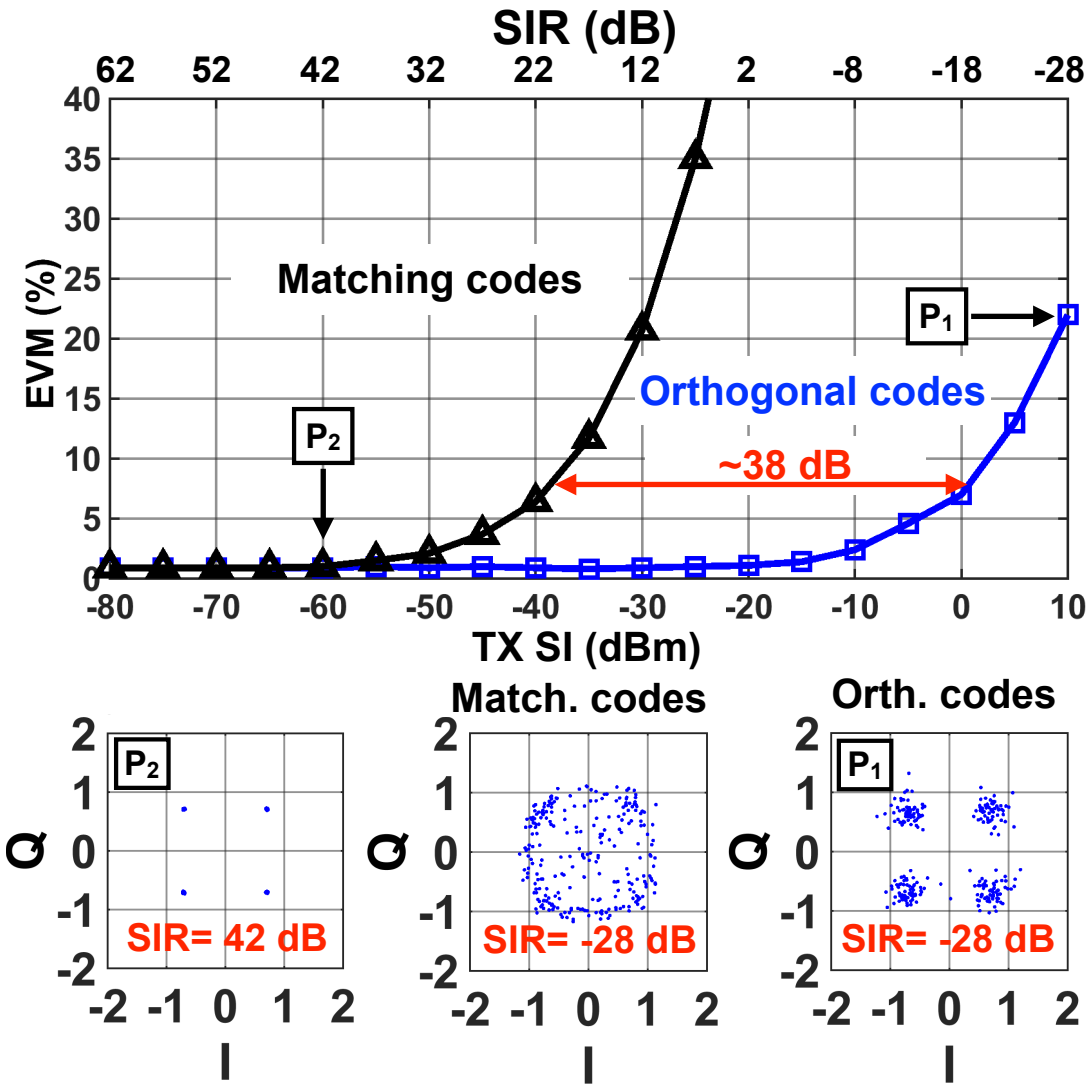


Figure 4.18: EVM as a function of transmit power and normalized to signal-to-interference ratio (SIR) and QPSK constellations at selected points.

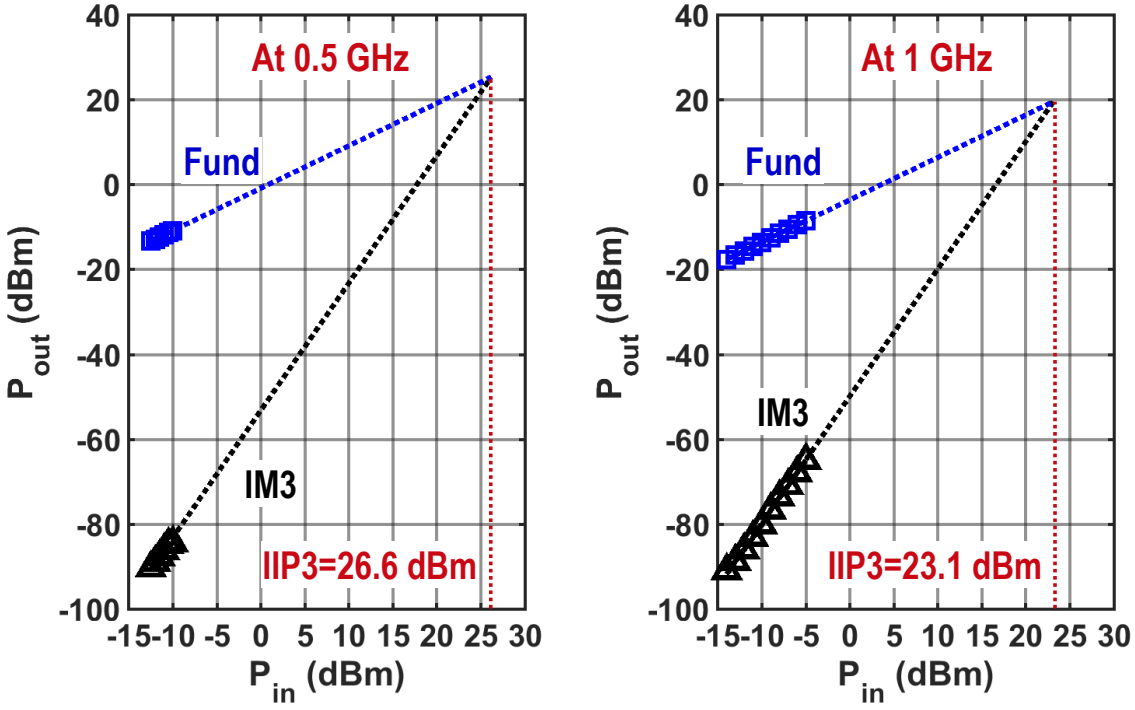
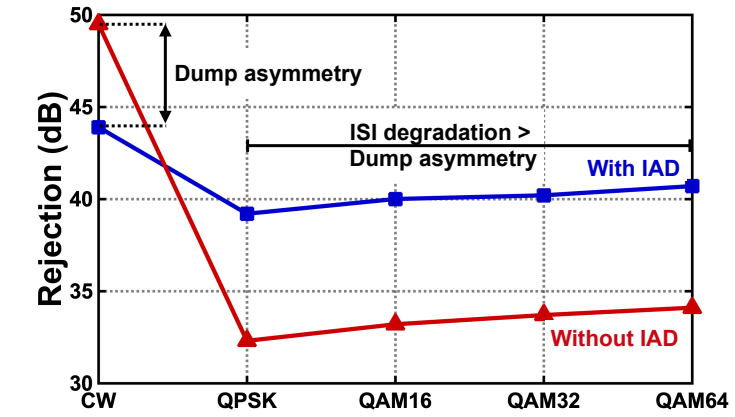
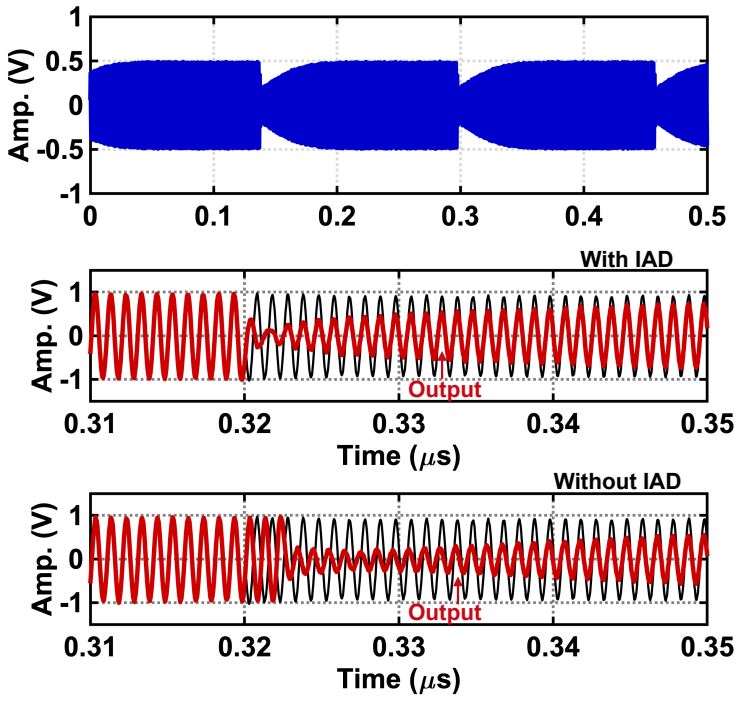


Figure 4.19: Best and worst measured IIP3 of the RX front-end



a)



b)

Figure 4.20: Measured rejection for different constellations with and without IAD a) IAD every 160 ns of a tone and ISI component with and without IAD c).

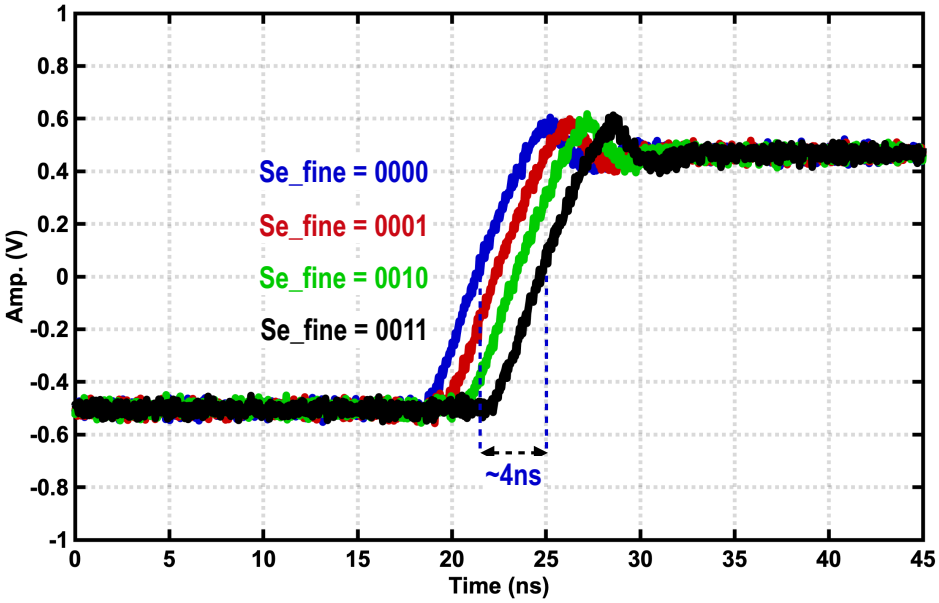


Figure 4.21: Measured CRX when generated Barker as the fine tuning control is changed.

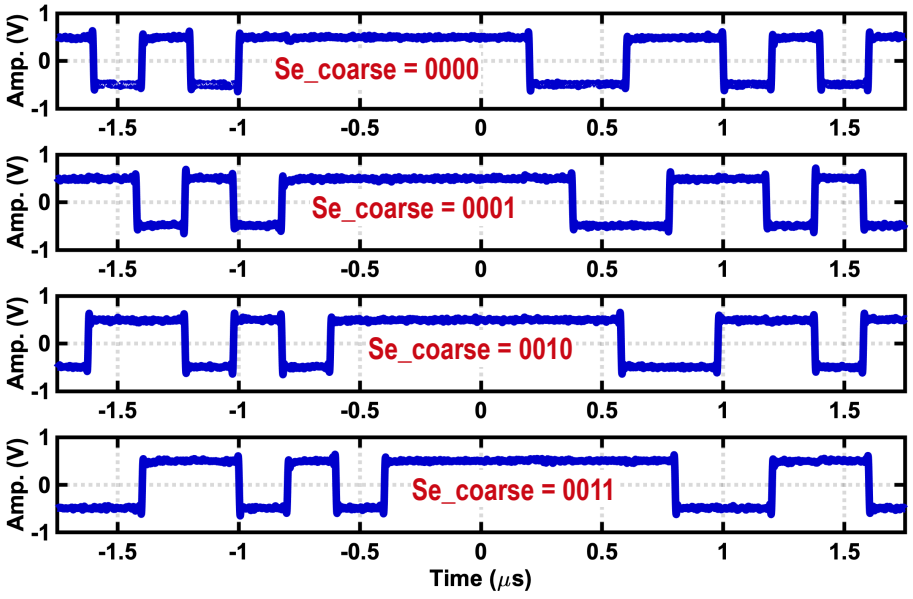


Figure 4.22: Measured CRX of generated Barker code with different coarse control.

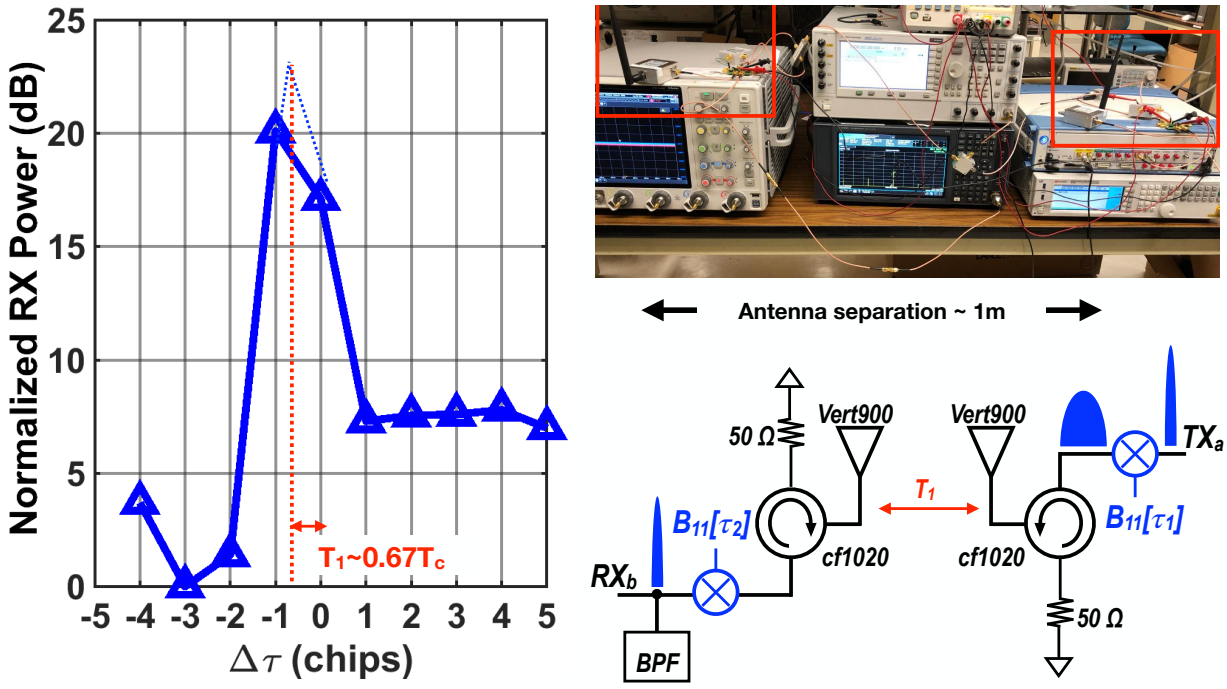


Figure 4.23: Over-the-air measurement for code synchronization and its set-up.

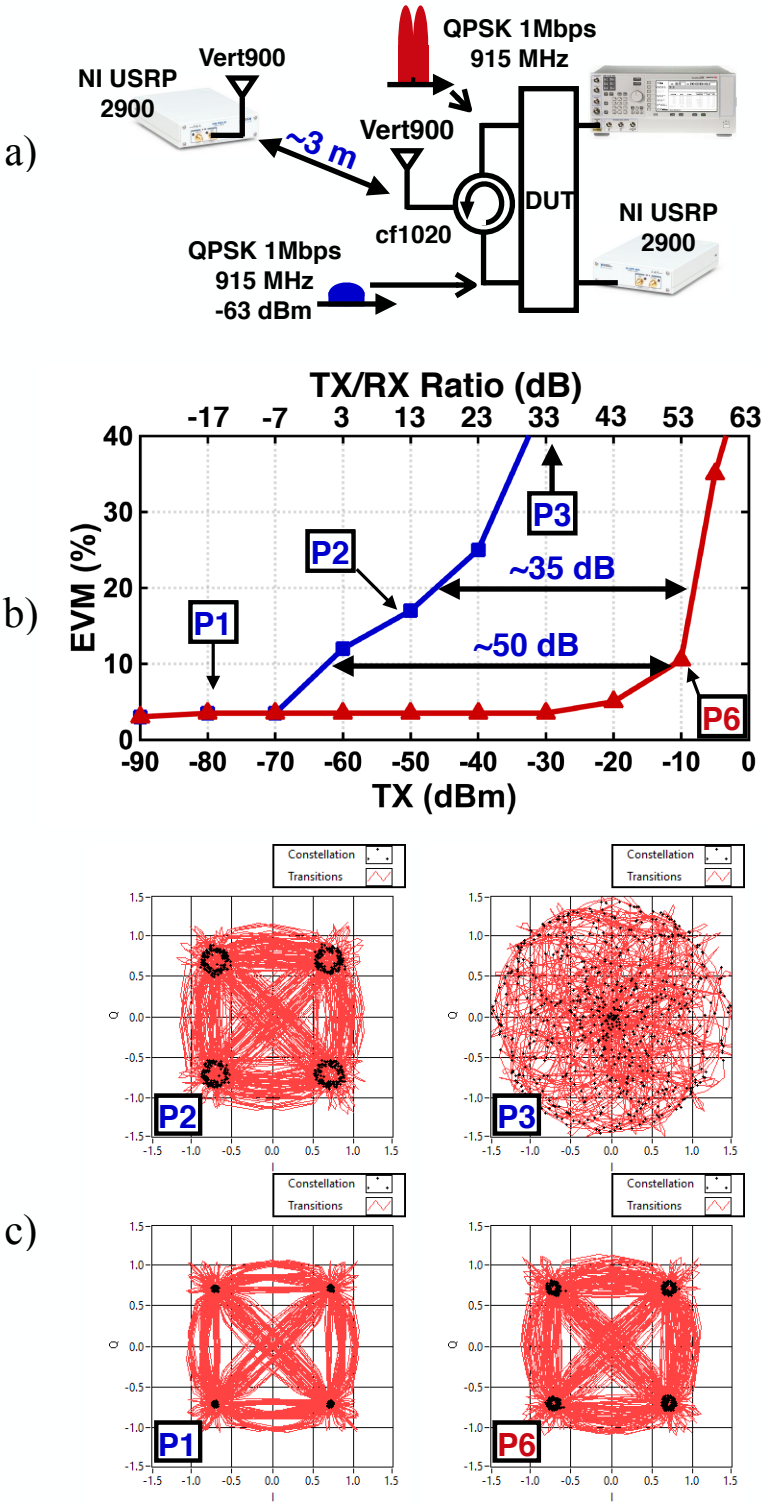


Figure 4.24: Setup for STAR operation OTA a) EVM vs TX and TX/RX at different modes and few constellation points c).

Chapter 5

Agile Blocker Tagging

In cognitive radio, wideband spectrum sensing greatly ac- celerates detection of unoccupied spectrum bands by sens- ing more than 100 MHz spectrum each time. However, the wideband sensing receiver becomes extremely vulnerable to interferers. According

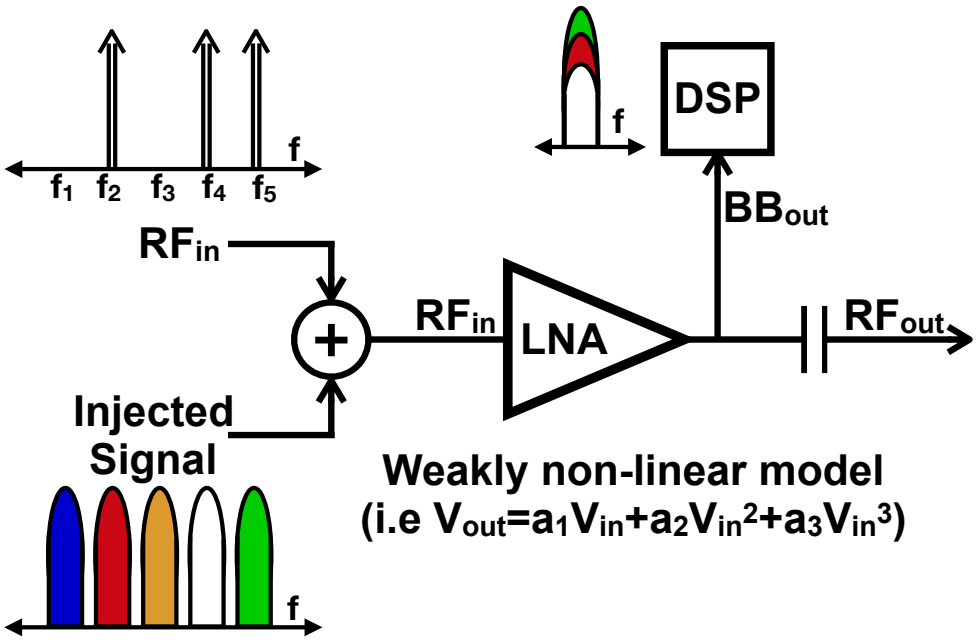


Figure 5.1: Concept of blocker tagging through nonlinear of LNA.

to IEEE 802.22, the input interferers power level at receivers could be up to -8 dBm . Due to the limited linearity of front-end, these strong signals introduces inter-modulation distortion (IMD), which prevents reliable sensing. Fig. 5.1 shows the proposed technique that depends on the non-linearity of the LNA. A weakly non-linear system is usually modeled by the first three non-linear terms:

$$Y = a_1 X + a_2 X^2 + a_3 X^2. \tag{5.1}$$

Blockers are often assumed to be a CW tone $ACos(w_c t)$ while the injected signal (IS) modulated with PN sequences is:

$$IS = \sum_{i=1}^{L} PN_1(t) A_i Cos(w_c i t). \tag{5.2}$$

When one of the terms in 5.2 has the same frequency as the blocker, a base-band term is introduced through the second order non-linearity in 5.1. More blockers can be be down-converted to BB without loosing information as the PN terms in 5.2 are orthogonal. Further processing after the analog-to-digital converter is required to identify the exact location of the blockers. What is appealing about this scheme is the ease of implementation with classical transceivers as shown in Fig. 5.2. To enter SS mode, the co-located TX simply transmits the injected signal yielding a power at the RX of about -20 dBm while the LNA is connected to lower supply to degrade the non-linearity intentionally and lowering the power consumption.

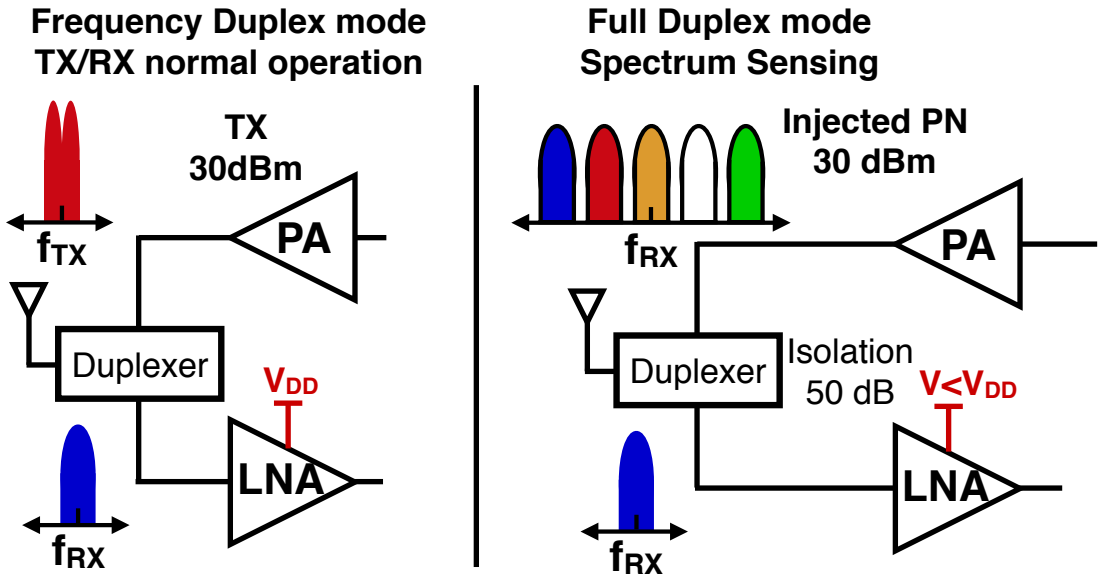


Figure 5.2: Implementation of Blocker Tagging algorithm with frequency-duplex transceivers.

Fig. 5.3 shows the chip micro-graph of an LNA taped-out in 45nm RF SOI process which is packaged with a 3mmx3mm QFN package and mounted on a PCB for testing. A power combiner before the LNA is mounted on PCB as well as a SMD component, in reality the leakage of the duplexer is the means of injecting the PN signal.

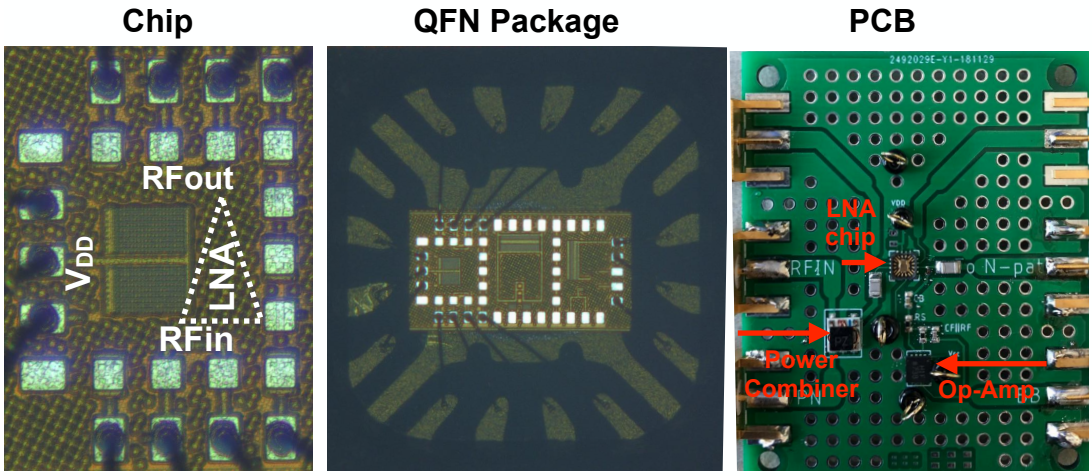


Figure 5.3: Implementation of LNA in CMOS-SOI, QFN package and PCB.

Fig. 5.4 shows measured S-parameters of the DUT compared against simulation showing a good agreement. The measured S_{21} is slightly lossy compared to simulation due to PCB losses that can't be accounted in simulation. The measured values are limited to 1.3 GHz due to limited range of network analyzer.

Fig. 5.5 compares the third order non-linearity of the DUT showing an IIP3 of around 10 dBm while Fig. 5.6 compares the second order non-linearity of the DUT showing a measured IIP2 of around 29 dBm. 5.6 shows the 1-dB compression point of the DUT. Measurement shows a P1dB of about -0.65 dBm. Those linearity tests are performed at 1.8 GHz.

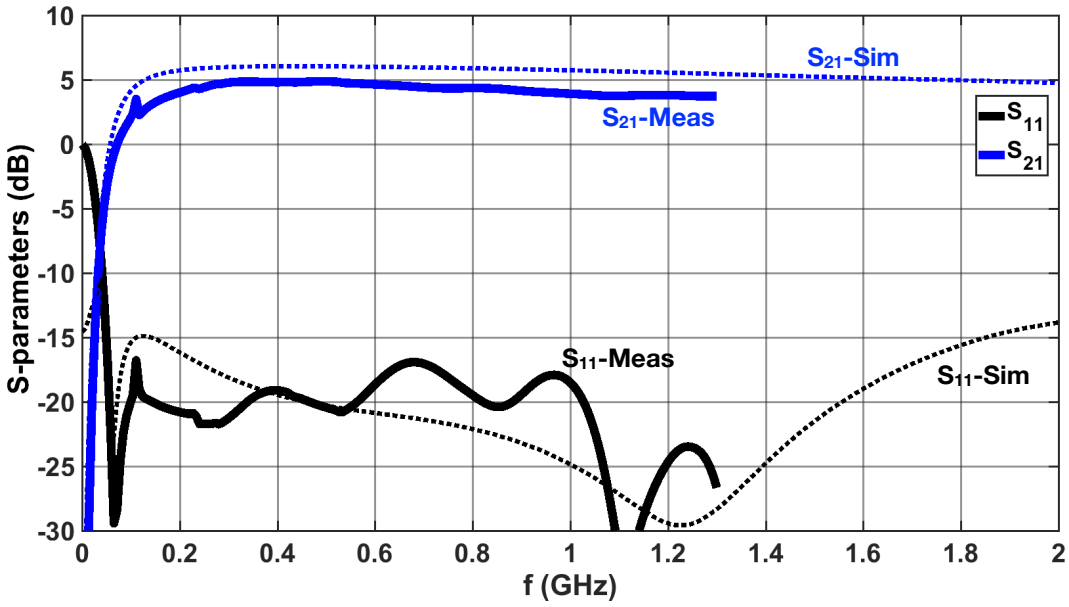


Figure 5.4: Measurement of S-parameters compared against simulation including power combiner and PCB and package losses whiteout any de-embedding

To degrade the linearity of the LNA, it is suggested to reduce the supply voltage of the LNA allowing earlier clipping and more distortion. Fig. 5.8 plots the measured power at BB vs supply voltage. Two tones are applied around 1 GHz with 5 MHz separation and power of - 20 dBm, IM2 is observed at BB at 5 MHz showing a maximum power for IM2 at around - 60 dBm. Since this power is lower than the quantizataion noise of the ADC and to filter the RF signal, the IM2 tone is filtered and amplified with on PCB OP-Amp. The signal is analyzed with MATLAB. Fig. 5.9 shows the experimental set-up. while Fig. 5.10 shows a sample of captured spectrum with illustration of RF waveform,

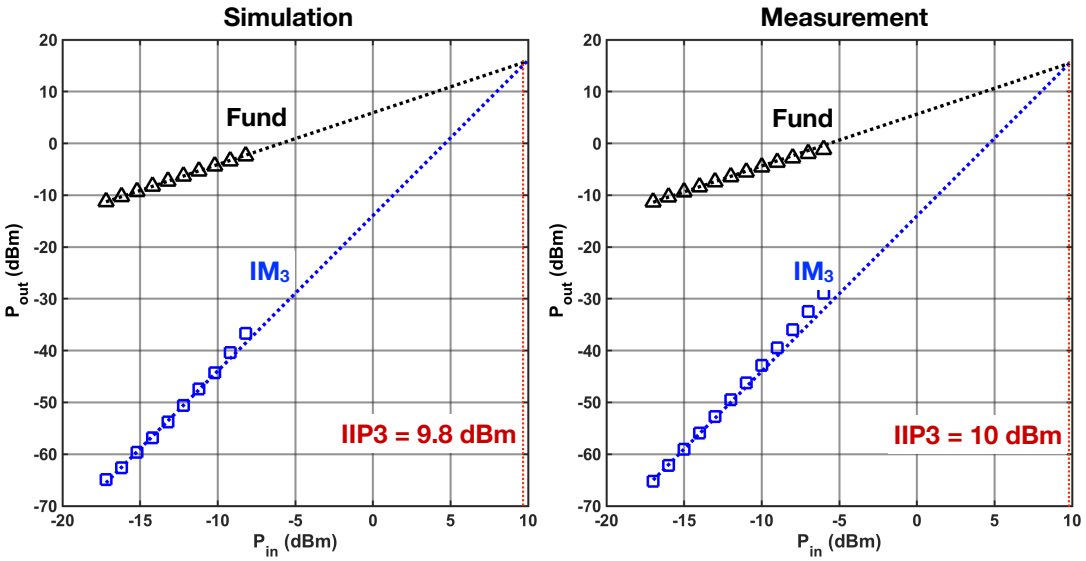


Figure 5.5: Measurements of IIP3 compared against simulation.

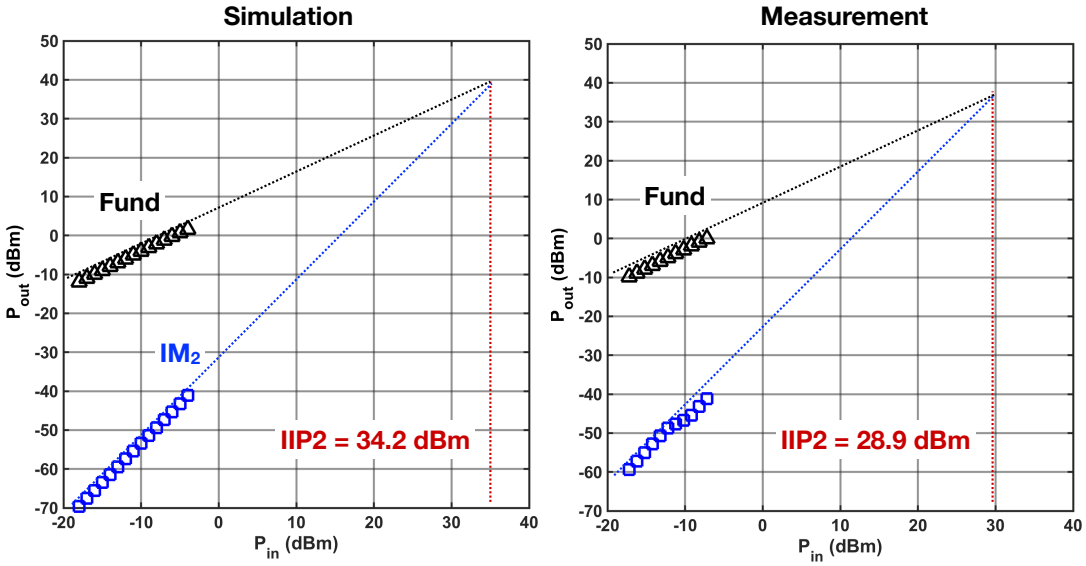


Figure 5.6: Measurements of IIP2 compared against simulation.

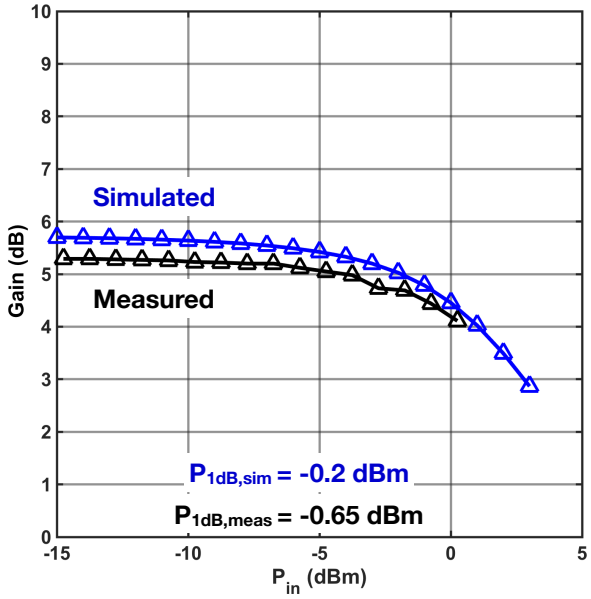


Figure 5.7: Measured P1dB compared against simulation.

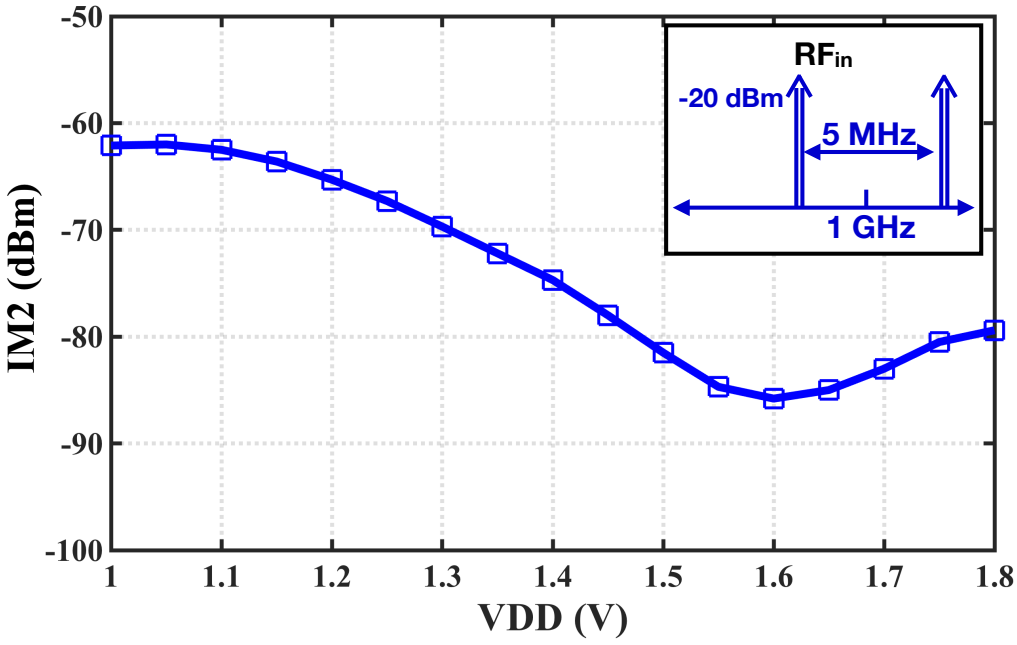


Figure 5.8: Measured IM2 vs supply with Illustration of spectrum at RFin.

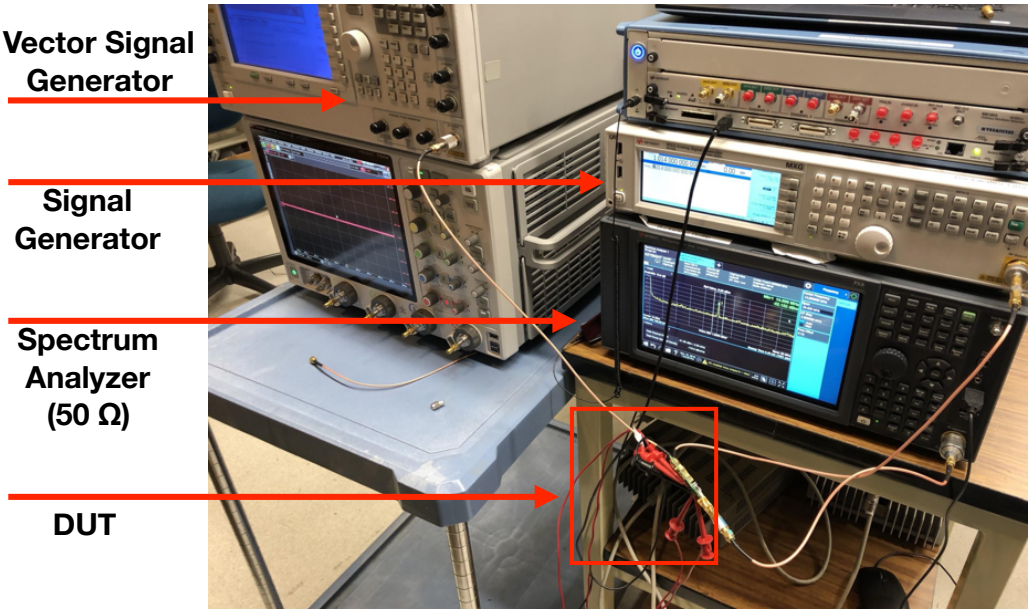


Figure 5.9: Experimental setup for blocker tagging measurement.

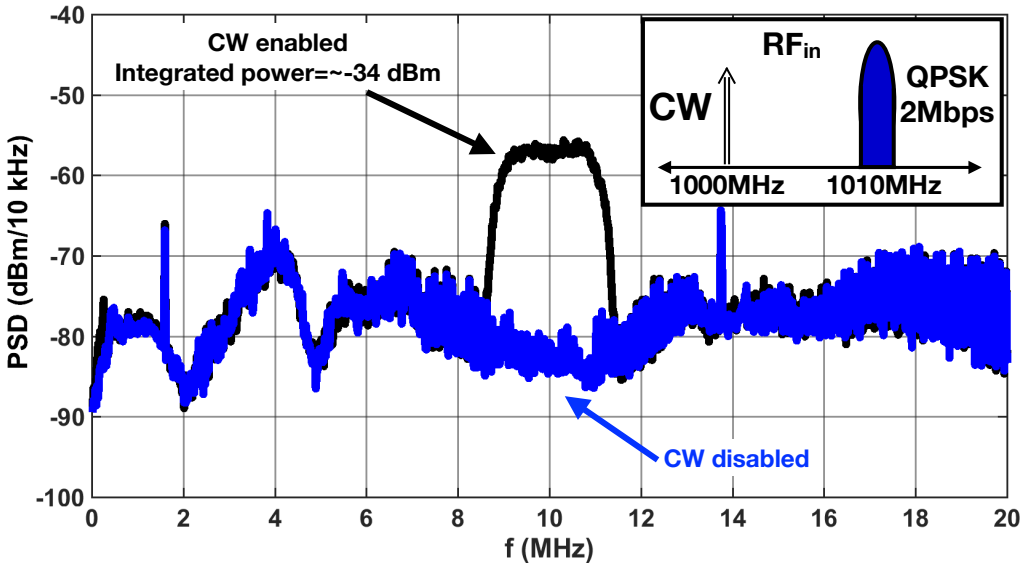


Figure 5.10: Measured spectrum at BBout Illustration of spectrum at RFin.

Chapter 6

Rake Modulator for Multi-path Links

6.1 Introduction

Wireless communications offer mobility at the cost of high interference among users. Due to multiple paths, a wireless channel can suffer fading lowering the performance significantly. Fig. 6.1 shows a wireless channel with three paths as an example. Depending on propagation times with respect to the symbol rate T_s, path 1 consists the first tap and the other two paths revolve in a second tap. It is anticipated that Inter-Symbol-Interference (ISI) will occur at the receiver (RX).

Direct-Sequence Spread-Spectrum (DSSS) [31,32] techniques can reduce ISI but they do not improve the performance of the wireless channel. To understand this, Fig. 6.1 shows a case where a physical blocker or moving object cause loss of information even with DSSS techniques. Fig. 6.2 shows theoretical probability of error vs signal-to-noise ratio for different channels. Wirle-line channel is additive-white Gaussian-noise (AWGN) and the only degradation is when the noise power is relatively high compared to the

desired signal. On the other hand, wireless channel are often fading even when SNR is high at the RX.

To improve the performance of the channel, diversity techniques must be used where information is sent through multiple independent parameters of the channel. This paper demonstrates a one RAKE demodulate that correlates with two codes at the same time achieving a diversity of 2 with one RX hardware only. Section II discusses theory and implementation of the proposed rake modulator while Section III includes measurements of an RFIC prototype including over the air measurements. Section IV is dedicated for conclusion.

6.2 Non-Binary RAKE Demodulator Circuit

If the transmit signal is coded with $PN(t)$

$$TX(t) = PN(t)[I(t)\cos(2\pi f_c t) + Q(t)\sin(2\pi f_c t)] \tag{6.1}$$

In a multi-path environment with L-taps (see TABLE I), the received signal is

$$\begin{aligned} RX(t) &= \sum_{i=1}^{L} \alpha_i TX(t-\tau_i) \\ &\approx \alpha_1 PN(t-\tau_1)[I(t)\cos(2\pi f_c(t-\tau_1))] \\ &+ \alpha_1 PN(t-\tau_1)[Q(t)\sin(2\pi f_c(t-\tau_1))] \\ &+ \alpha_2 PN(t-\tau_2)[I(t)\cos(2\pi f_c(t-\tau_2))] \\ &+ \alpha_2 PN(t-\tau_2)[Q(t)\sin(2\pi f_c(t-\tau_2))] \end{aligned} \tag{6.2}$$

where approximation for highest two taps and assuming the code chip rate T_s is much

smaller than the symbol rate T_s, a common feature of DSSS techniques.

If we correlate with $PN(t-\tau_1)$ only, we get ISI reduction due to low auto-correaltion between $PN(t)$ and $PN(t-\tau)$ for τ ¿ T_c. However, information is received from one tap only. The same is true when correlating with $PN(t-\tau_2)$. In other words:

$$\begin{aligned} RX_1(t) = &\quad \alpha_1[I(t)+Q(t)] = I_1(t)+Q_1(t) \\ &\quad and \\ RX_2(t) = &\quad \alpha_2[I(t)+Q(t)] = I_2(t)+Q_2(t) \end{aligned} \tag{6.3}$$

A better receiver utilizes both taps to improve the performance of the wireless channel by correlating with the code: $PN(t-\tau_1)+PN(t-\tau_2)$ which takes three levels unlike the basis code that are binary levels.

On the other hand if we correlate with C_1+C_2 we get a better response:

$$\begin{aligned} I_{1,2} = I_1 + AI_2 + BQ_2, \quad \text{and } Q_{1,2} = Q_1 + AQ_2 + BI_2 \\ \text{where } A = \alpha_1 + \cos(\Delta\phi)\alpha_2, \quad \text{and } B = \sin(\Delta\phi)\alpha_2 \end{aligned} \tag{6.4}$$

showing a diversity gain is 2 and coding gain of $1+\alpha_2/\alpha_1$. If- for any reason- one of the paths disappear, equation(6.4) reduces to either entries of equation (6.3) which provides the diversity.

Eq.(6.3) shows there is an IQ leakage when τ_1 and τ_2 differ by a non-integer multiple of the carrier period T_ch. Fortunately this can be remedied by a simple rotation at DSP as will be shown in measurement section.

To understand a correlation process with non-binary codes the following example is provided. Assuming a Barker code of length 11 is used code with a a sequence of

C_1=[1 1 1 -1 -1 -1 1 -1 -1 1 -1] where the box indicates the beginning of the code. The auto-correlation R(m) = $1/N \sum_{n=0}^{N} C_1(n).C_1(n-m)$ and equals to 1 and -1/11 for m = 0 and 1. The non-binary code $C_{12} = C_1 + C_2$=[0 2 2 0 -2 -2 0 0 -2 -2 -2]. The cross-correlation between C_1 and $C_1$2 is 1-1/11=10/11. The same is true for C_2 and $C_1$2. In other words, C12 has information about both codes C_1 and C_2. On the other hand, the corss-correlation between C_3 and C_{12} is -2/11 indicting that codes are orthogonal.

Fig. 6.3.a) shows the proposed 3-state modulator to correlate against a non-binary code like C_{12} to increase diversity of the output. It is like a double-pole double-through switch. On chip logic takes in two codes C_1 and C_2 and generates three states. The first state is to pass the signal with 0 degrees phase shift when the two codes equal to high value. When the codes are equal to low value, the switch pass the signal in 180 degree phase shift. Finally when the two codes are not equal, the modulator enters a hold state where the RF signal is blocked from passing. Two resistors are added across each port to prevent wave reflection during the hold state. The equivalent Resistance including the switches is about 100Ω. The switches are chosen to be of transmission gate topology to improve isolation and linearity. Fig.6.3.b shows wave-forms illustrating different states.

TABLE I
INDOOR OFFICE TEST ENVIRONMENT
(MEDIAN PARAMETERS)

Tap	Relative Delay (ns)	Average Power (dB)
1	0	0
2	100	-3.6
3	200	-7.2
4	300	-10.8
5	400	-18
6	700	-25.2

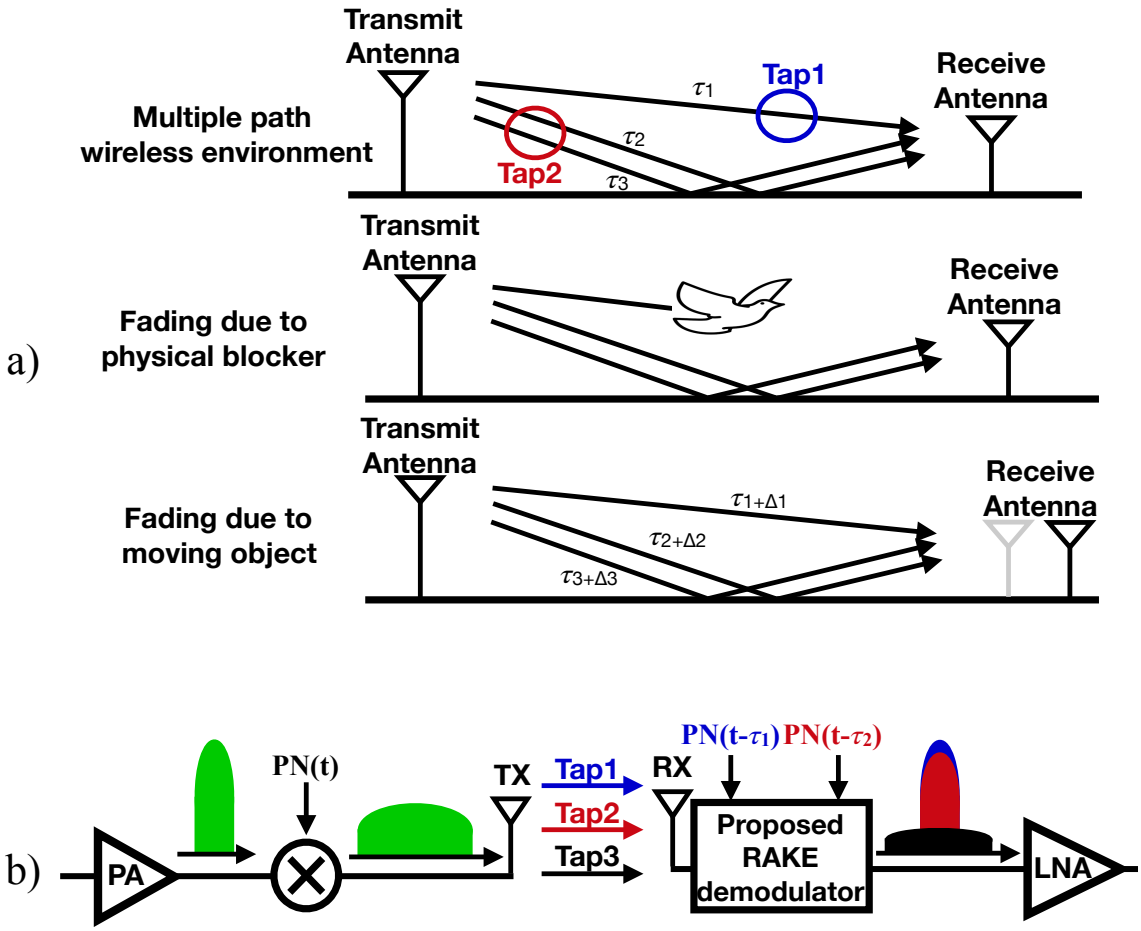


Figure 6.1: Proposed DSSS modulator and matched filter with RF code correlator and integrate and dump.

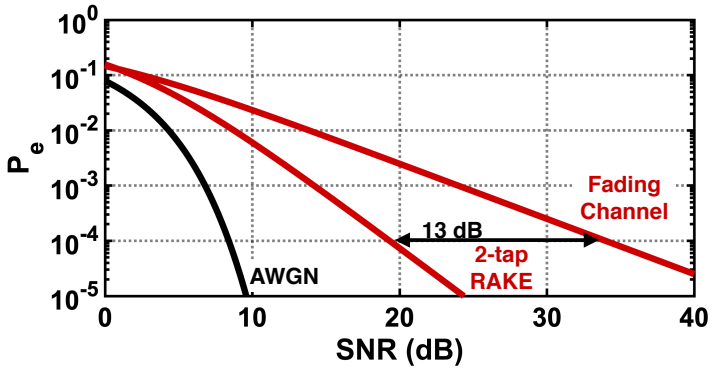


Figure 6.2: Proposed DSSS modulator and matched filter with RF code correlator and integrate and dump.

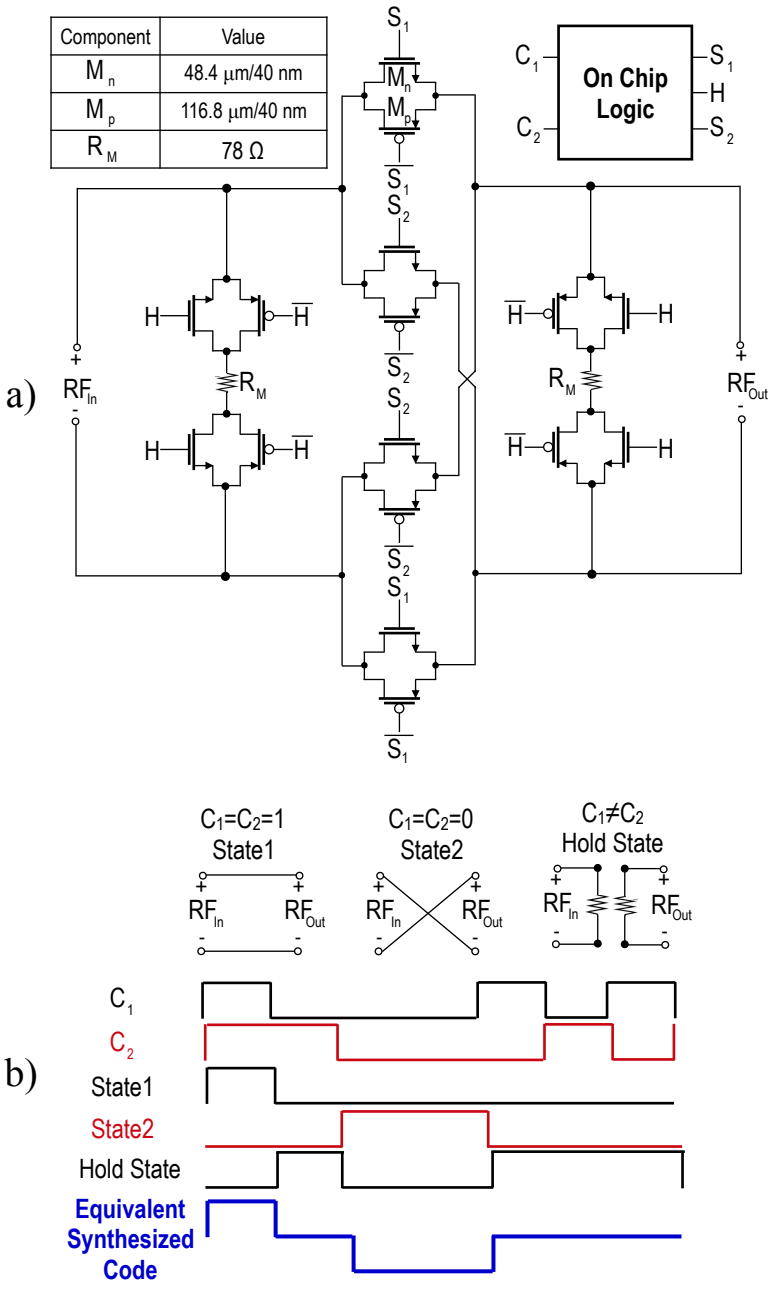


Figure 6.3: Block diagram of the code domain transceiver for STAR applications.

6.3 Measurements

The proposed system was fabricated with GlobalFoundries 45-nm RF SOI process. The die is shown in Fig. 6.4 and occupies an area of 2.59 mm^2 including the pads and ESD circuitry while the active area is 1.12 mm^2. The fabricated chip was packaged with a QFN 2mmx2mm package and mounted on a PCB for testing. SMD baluns of TC4 of 1.4GHz BW were used and limit the frequency range. RX power consumption was less than 1 mW including digital circuitry with code rate of 200 Mcps from 1-V supply.

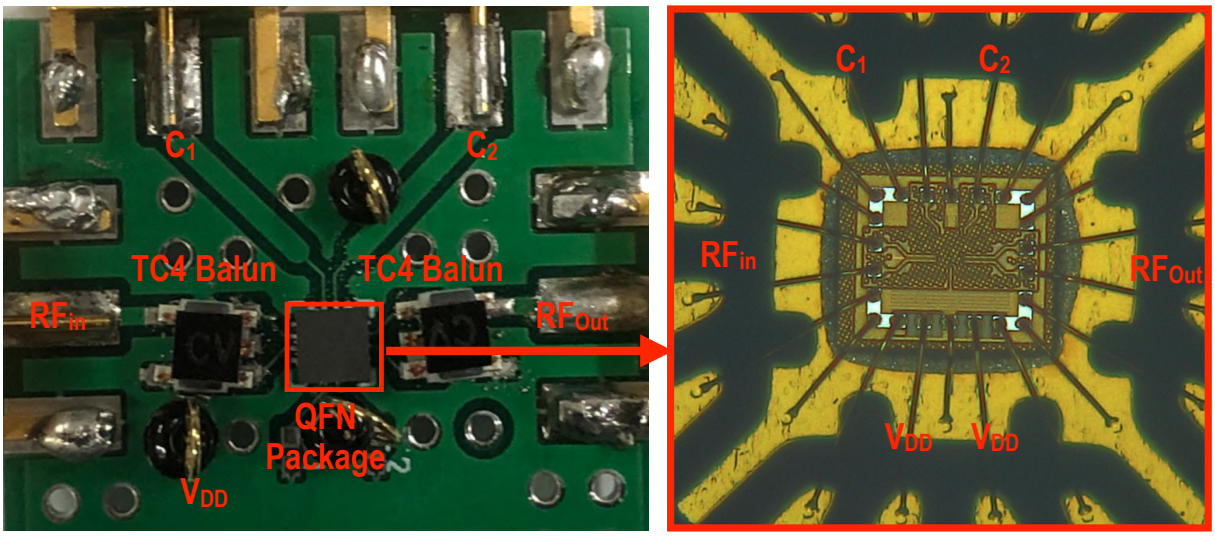


Figure 6.4: Chip micro photograph of the Rake modulator and PCB.

Fig. 6.5 shows measured S-parameters of the packaged chip as well as the PCB and baluns without any de-embedding showing a total IL of around 2.5 dB and return loss better than 10 dB.

Fig. 6.7 shows operation of RAKE demodualtor in time domain. A CW waveform is split and modualted with two shifted versions of a Barker11 code to mimic multi-path environment and then de-modulated with the proposed RFIC. When two paths are present, RX is able to pass the correct symbol (green). Other cases show the demodualtor

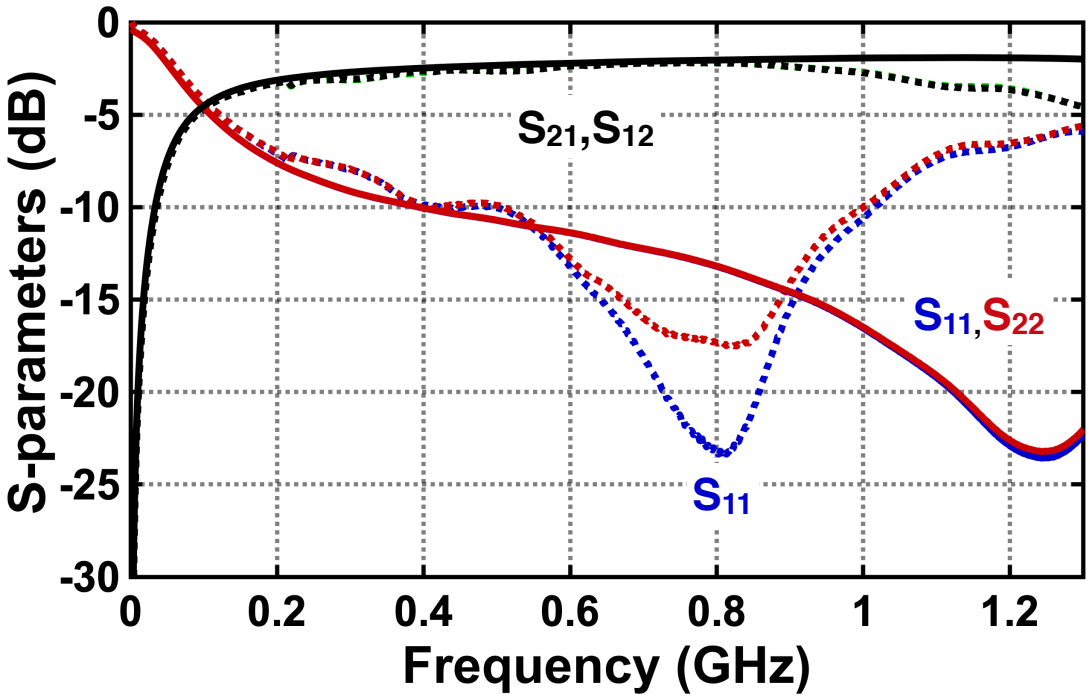


Figure 6.5: Measured S-parameters (dashed) compared to simulated S-parameters (solid) Including baluns and package.

is able to produce the same result even in the present of complete fading of the path showing a second diversity. Fig. 6.8 shows operation of RAKE demodualtor. A CW waveform is split and modualted with two shifted versions of a Barker11 code to mimic multi-path environment and then de-modulated with the proposed RFIC. When two paths are present, RX is able to pass the correct symbol (green). Other cases show the demodualtor is able to produce the same result even in the present of complete fading of the path showing a second diversity.

Table II shows a comparison with state of the art work. The proposed front-end is the first code-domain RAKE modualtor that provides a second diversity.

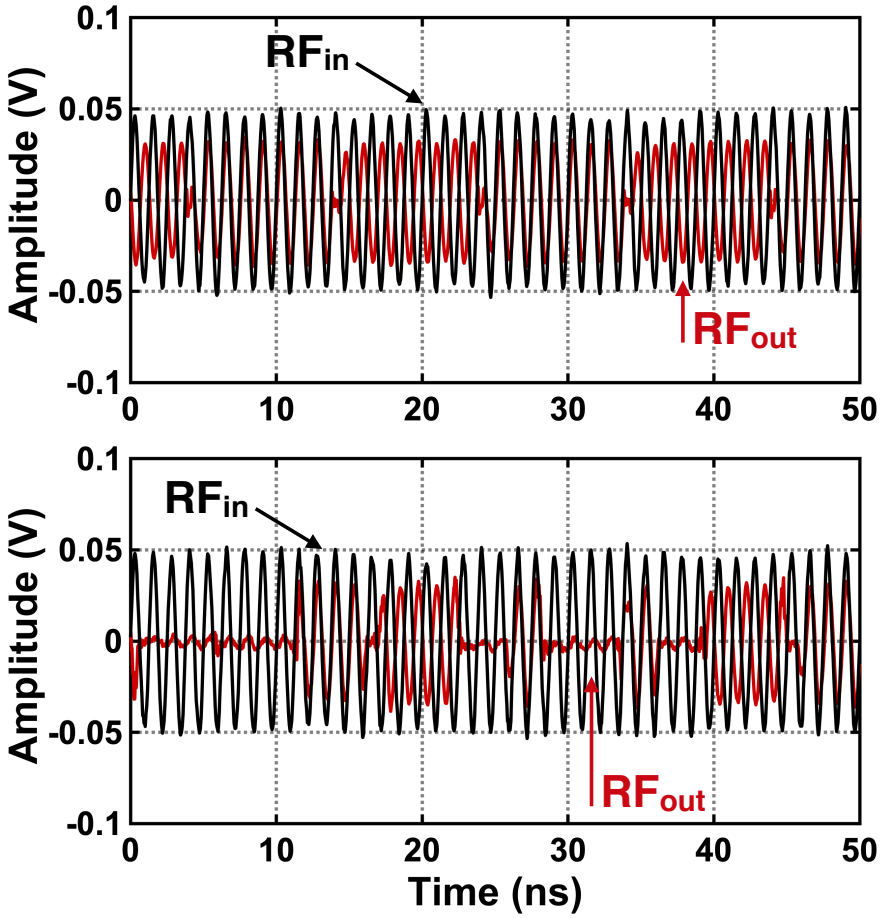


Figure 6.6: Measured time domain waveform for modulating a CW tone at RF_{in} with a) binary code b) non-binary code.

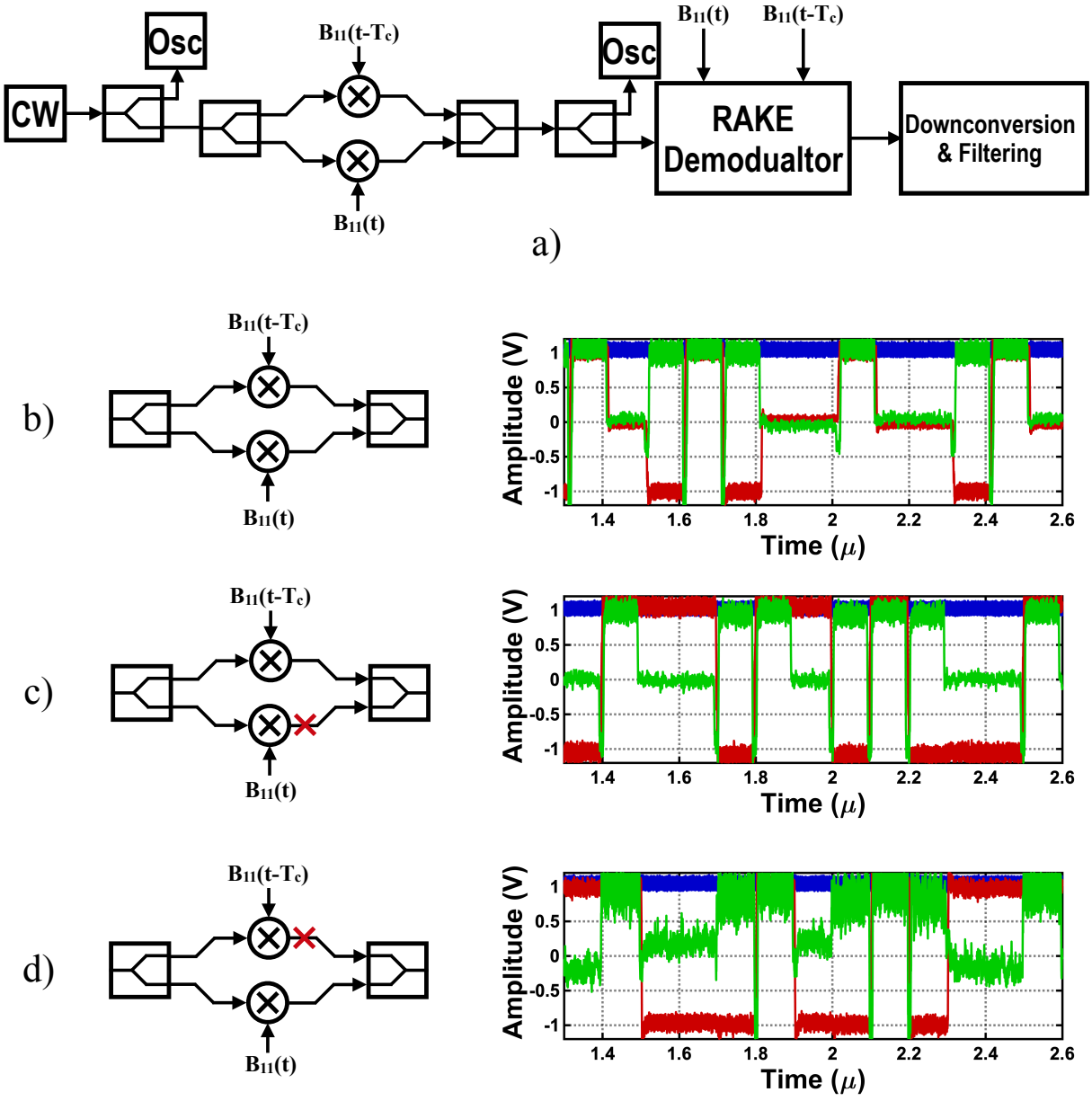


Figure 6.7: Illustration of test-setup a) BB time domain waveforms when two paths are utilized b) BB time domain wavefomrs when one path fades completely: first c) and second d)

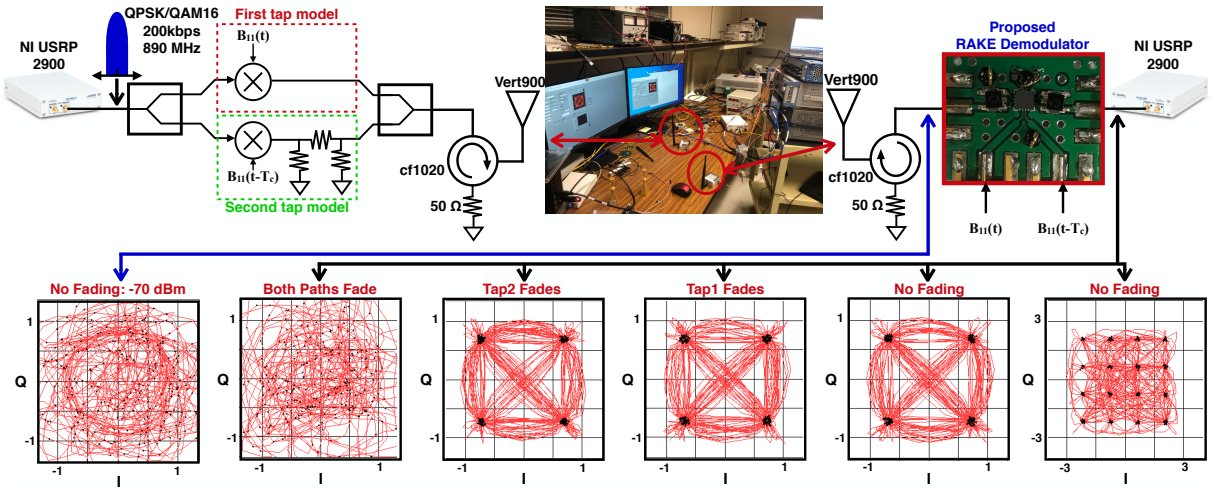


Figure 6.8: Measured time domain waveform for modulating a CW tone at RF_{in} with a) binary code b) non-binary code.

6.4 Conclusion

A novel non-binary modulator can provide a diversity of 2 improving the reliability of wireless channel. Theory is verified with experimental results using CMOS SOI and over-the-air measurement.

Appendices

Appendix A

Derivation of R_{sh}

N-path filters translate the baseband impedance Z_{BB} to f_{LO} and scale the impedance by the Fourier coefficient of the first harmonic, e.g $a_1^2 = \frac{2}{\pi^2}$ for 4-path filter. If the baseband impedance is a capacitor, the N-path provides infinite impedance at f_{LO} and has no insertion loss. In reality, simulation and measurement demonstrates the impedance is actually finite due to an equivalent resistor R_{sh} must assumed and have been theoretically attributed to radiation at higher harmonics [37][13][9]. Previous derivations lack a circuit interpretation. Here, a circuit-based derivation of R_{sh} is illustrated. By applying a test voltage V_T as shwon in Fig. 23, the current flowing into the N-path is calculated. For a 4-path, the voltage at node V_x is an approximation with up to 4 levels [37] to the test voltage. The voltage during $LO_1(t) = 1$ is

$$V_{x,1} = \frac{1}{\frac{\pi}{2}} \int_0^{\frac{\pi}{2}} A \sin(2\pi f_{LO} t) dt = \frac{2}{\pi} A \tag{A.1}$$

The voltages at other phases can be related to $V_{x,1}$:

$$V_{x,1} = V_{x,2} = -V_{x,3} = -V_{x,4}. \tag{A.2}$$

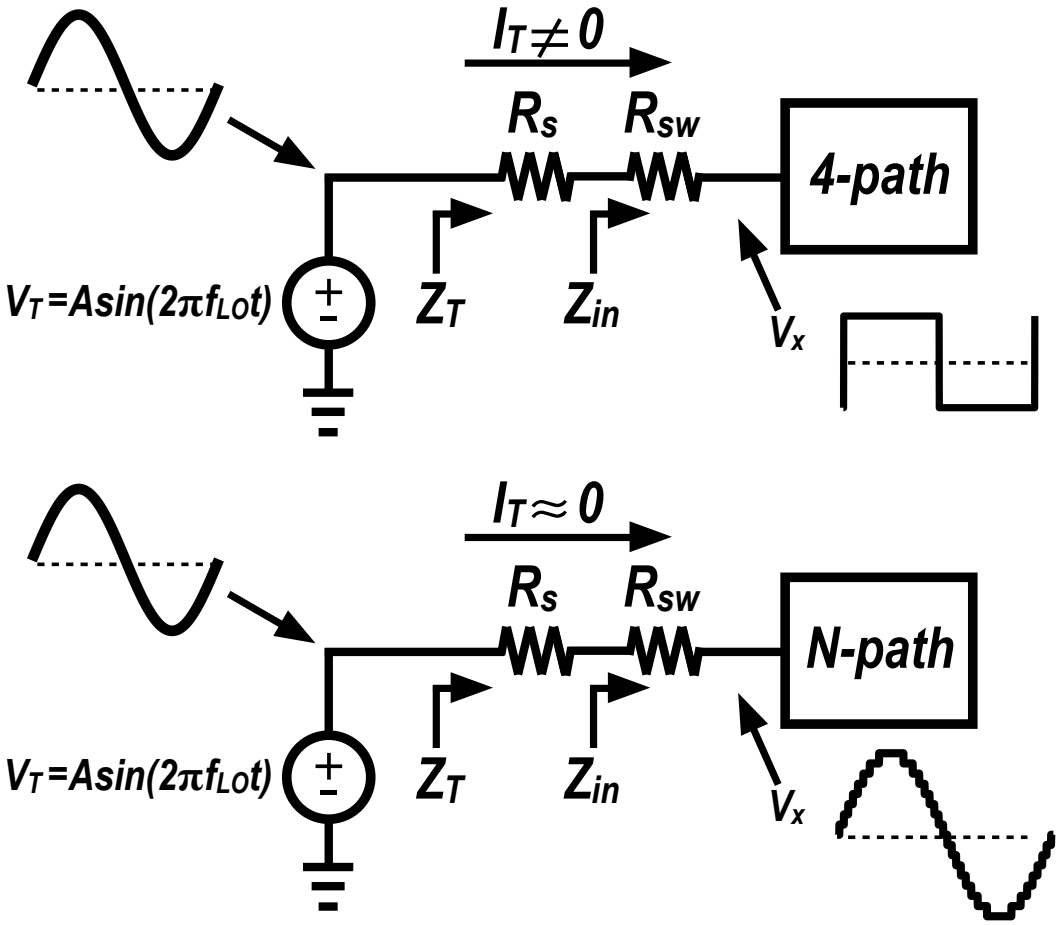


Figure A.1: Waveforms for a 4-path filter and a generalized N-path filter.

In other words, the voltage at node x is a square wave at the same frequency as V_T toggling between $\pm\frac{2}{\pi}A$. The fundamental of this square wave has amplitude of $(\frac{4}{\pi})\frac{2}{\pi}A$. The fundamental current I_T is

$$I_T = \frac{(1-\frac{8}{\pi^2})}{R_s + R_{SW}} A \sin(2\pi f_{LO} t). \tag{A.3}$$

Thus, the test impedance is

$$Z_T = \frac{V_T}{I_T} = \frac{\pi^2}{(\pi^2 - 8)}(R_s + R_{SW}) \tag{A.4}$$

and the input impedance is

$$\begin{aligned} Z_{in} =& Z_T - R_s = \frac{8}{(\pi^2 - 8)} R_s + \frac{\pi^2}{(\pi^2 - 8)} R_{SW} \\ =& R_{SW} + R_{sh}. \end{aligned} \tag{A.5}$$

This expression suggests that R_{sh} is the result of non-zero current at the fundamental due to approximation of the waveform at the input of the N-path filter. Increasing N provides a more accurate approximation and the current I_T becomes negligible which in turn results in a larger R_{sh}.

Appendix B

$\mathbf{Walsh}_{16}$ Family

The Walsh codes produce code-dependent impedances as shown in Fig. B.1. (M=16)Fig. B.1 shows the input impedance when applying different codes from Walsh of length-16 family to the CSF.

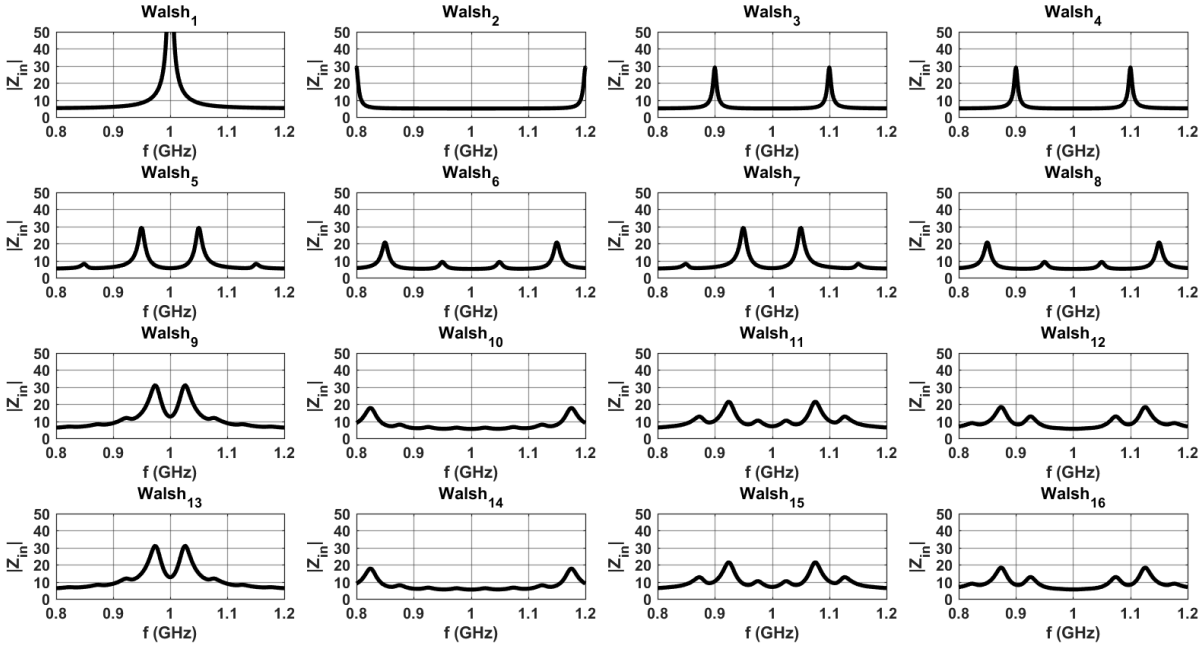


Figure B.1: Theoretical input impedance of CSF for different Walsh codes.

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