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Design of Bulk Thermoelectric Modules for Integrated Circuit Thermal Management

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***Abstract*—Various parameters affecting the performance of bulk thermoelectric (TE) modules used for integrated circuit (IC) thermal management are studied. An effective circuit model is developed that takes into account various ideal and nonideal effects in the module. It is shown that there is an optimum module thickness and an optimum operating current which depend on the overall heat dissipation and on the external thermal resistances. Optimized TE modules with ZT ∼0.8, will have a cross section over leg length ratio of 0.037 m, can increase the chip operation power by 15% in comparison with the case without a TE cooler while maintaining the chip temperature below 100 °C. This is for a package thermal resistance of 0.2 K/W. Prospects for TE material with higher ZT values and the effect of contact resistance on the power dissipation density are also discussed. The results presented in this paper can be used in applications other than in the IC thermal management when external thermal resistances dominate the performance of TE modules.**

***Index Terms*—Contact resistance, equivalent circuit models, external thermal resistance, integrated circuit (IC), thermal management, thermoelectric (TE) modules.**

I. Introduction

CONTROLLING the operating temperature of microelectronic devices has become more important in recent years because heat generated by the devices has increased substantially due to device miniaturization and increased switching speeds. Recently, most integrated very large scale integrated (VLSI) circuits are designed with cooling systems to further increase clock speeds. Among the various cooling systems, thermoelectric coolers (TECs) have a lot of advantages compared with nonrefrigeration systems. For example, TECs can reduce the operating temperature of electric devices below the ambient temperature, or the temperature could be reduced compared to passive systems in some cases; additionally they are compact, quiet, and have no moving parts. However, a TEC's performance is not always superior to that of nonrefrigeration systems, such as a cooling fan or natural convection, because TECs need to dissipate the pumped heat as well as the Joule heat generated by the operating current at the hot end, which sometimes degrades the overall system performance. Therefore, it is very important to design a TEC to be effective.

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Color versions of Figs. 7–10 are available online at http://ieeexplore.ieee.org.
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Previously, Phelan *et al.*, Simons *et al.*, and Solbrekken *et al.* predicted the performance of a conventional bulk BiTe-based TEC in an electronic package environment [1]–[5]. In Phelan's paper [1], they assumed the optimum operating current $I_{\rm opt}$ to be $I_{\rm opt} = \alpha T_c G/\rho$, where a α is the Seebeck coefficient, T_c is the cold side temperature, ρ is the electrical resistivity of the TE element, and G is a geometrical factor equal to the cross-sectional area divided by the leg length of each element in a couple. This assumption is valid if the value of the thermal resistance between the hot end of the TEC and the ambient air (R_2) can be neglected compared with the value of the thermal resistance of TEC (R_{th}). However, R_2 can't be neglected in most cases and a new optimum current should be calculated [2], [3], [5]. This will have significant impact on TEC's performance to reduce the operating chip temperature $(T_{\rm chip})$ for a given power dissipation [2], [3], [5]. Also, although it is basically difficult to change the TE material properties, the geometrical factor (G) can be easily changed to maximize the TEC performance from the viewpoint of the system design. Therefore, if the operating current and TEC geometry are optimized at the same time by taking into account the external thermal resistance such as R_2, it will increase the TEC's potential furthermore.

In this paper, we extend the previous work and predict the cooling performance of the conventional bulk TEC integrated with an integrated circuit (IC) chip and heat sink. In order to maximize the TEC performance in a package environment, the operating current and TEC geometry factor (G) are optimized to minimize the chip temperature by taking into account the external thermal resistance. An one-dimensional (1-D) electrothermal model was developed to conduct numerical studies for a simple estimation. At the beginning, the improvement of the TEC performance by optimizing the operating current as well as by modifying TEC geometry will be discussed. Finally, the effect of material properties and contact resistance on a power dissipation density in various package environments will also be discussed.

II. Device Modeling

Fig. 1(a) and (b) illustrate a schematic representation of a chip with and without a TEC. In both situations, the heat generated by a chip flows through a chip, (TEC module) and heat sink to the ambient air. In the case with the TEC shown in Fig. 1(a), some heat is electrically pumped from the cold side to the hot side of the TEC based on the Peltier effect. Meanwhile, there is Joule heating generated inside the TEC due to the operating current and electrical resistance.

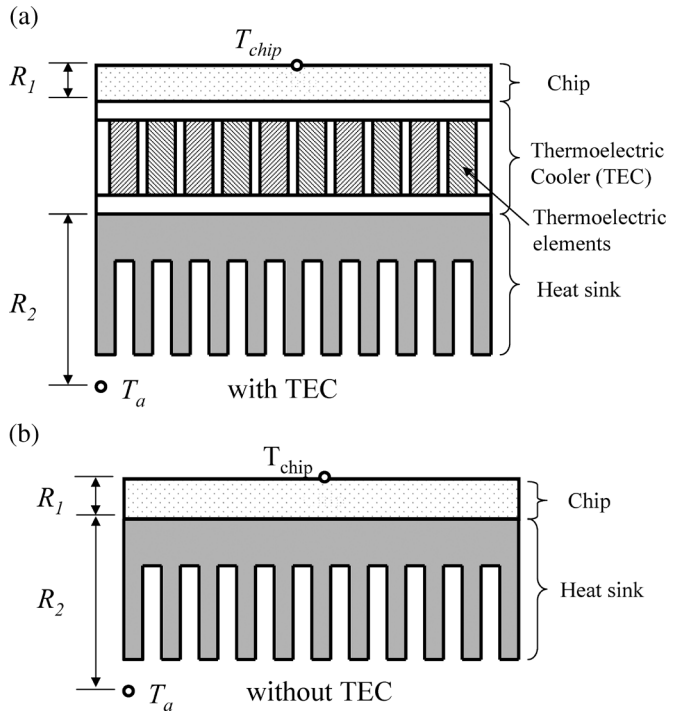


Fig. 1. Schematic representation of a chip (a) with and (b) without a TEC. The external thermal resistances (shown as R_1 and R_2) are described for the chip and hot side of TEC to ambient.

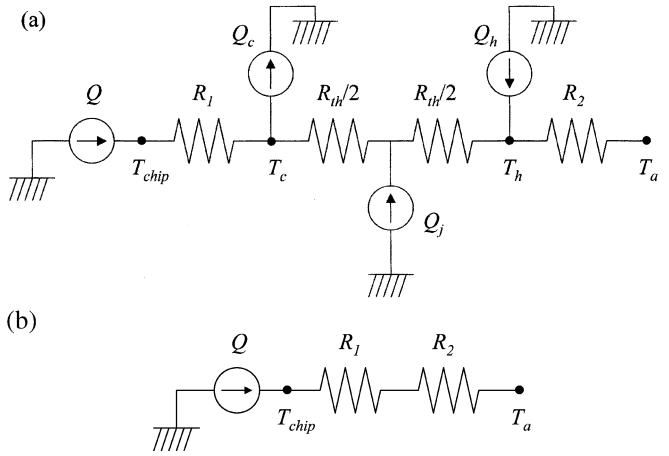


Fig. 2. Equivalent circuit device model for a chip (a) with and (b) without a TEC.

Fig. 2(a) and (b) show the equivalent circuit device models of chips with and without a TEC. Resisters represent thermal resistances. Here, Peltier cooling and heating and Joule heating are modeled with current sources. There are two Peltier effects and one Joule heating in the model with a TEC shown in Fig. 2(a). The two Peltier effects include Peltier cooling at the cold side of the TEC (Q_c) and Peltier heating at the hot side of the TEC $(Q_{\rm h})$. It is simple to show that one can always put the Joule heating current source (Q_j) in the middle of the TEC thermal resistance (R_{th}) regardless of the thermal boundary conditions at the two ends [6]. Furthermore, in the case of the model with the TEC, R_1 is the sum of the thermal resistance of the chip substrate and the interface thermal resistance between the chip and the cold side of the TEC, and R_2 is the sum of the interface thermal resistance between the hot end of the TEC and the heat sink and the thermal resistance of the heat sink to ambient air, indicating external thermal resistances. Q_j is given by $2NI^2R_e$, where N is the number of couples in the TEC, I is the operating current, and $R_e = \rho/G$ is the electrical resistance of the TEC. $G = S/L$ is a geometrical factor described by the ratio of the leg's cross-sectional area (S) to its length (L), and ρ is the electrical resistivity of the TE element, which is assumed to be equal for the n-type and p-type elements. $Q_{c,h}$ can be described by the equation $Q_{c,h} = 2N\alpha IT_{c,h}$, where T_c is the cold side temperature of the TEC and T_h is the hot side temperature of the TEC. R_{th} can be described by the equation $R_{th} = 1/2NkG$, where k is the thermal conductivity of the TE elements, which is also assumed to be equal for the n-type and p-type elements. T_a is a constant voltage source modeling the ambient temperature and $T_{\rm chip}$ is the actual operating temperature of the chip. In the model with the TEC, if heat that flows from the chip (Q) and the operating current (I) are given, we can easily calculate $T_{\rm chip}$, T_c, and T_h by using Kirchhoff laws from the circuit model.

In order to compare our calculation results with Phelan's results, we used the same TEC design based on a commercially available TEC from Melcor, Model CP5-31-061 [1]. According to the date sheet published by Melcor [7], the device geometry is $55\times55\times4.9$ mm, the maximum heat-pumping rate $(Q_{\rm max})$ is 125 W, and the maximum cooling temperature difference (ΔT) is 67 °C at the hot side temperature of 25 °C. The parameters used for the calculation are N =31, G = 0.01196 m, k = 1.5 W/mK, $\rho = 10^{-5}$ Ωm, $\alpha = 2 \times 10^{-4}$ V/K. In all calculations, the ambient temperature (T_a) is assumed to be 25 °C. To evaluate the effectiveness of a TEC, $T_{\rm chip}$ for no TEC system was also calculated assuming the same value of R_1 and R_2 as the TEC system by using the equivalent circuit model shown in Fig. 2(b). The temperature dependence of material properties is not taken into account in this calculation for the simplicity.

III. Results and Discussion

In order to calculate the relationship between the heat dissipation (Q) and the chip temperature $(T_{\rm chip})$, the value of R_1 and R_2 must be determined. To compare our results with Phelan's calculation, the same value was assumed for R_1 and R_2; R_1 = 0.571 K/W, R_2 = 0.049 K/W [1]. For these conditions, the results of the two calculations are compared in Fig. 3(a). This figure shows the relationships between dissipated power, Q, (or q: heat dissipation density) and the chip temperature, $T_{\rm chip}$, calculated by the different models. In this figure, one plot is calculated by using Phelan's model and another plot is calculated from the equivalent circuit model. Here, q is calculated by assuming the TEC area of the TEC is 5.5×5.5 cm^2. For reference, the result with no TEC is also shown in the same graph. In our calculation, I was determined to minimize $T_{\rm chip}$, indicating that I is optimized by considering the value of R_2. There is little difference between Phelan's results and ours. This is attributed to the small value of R_2 compared with the thermal resistance of the TEC (R_{th}). In our model, the optimum current $(I_{\rm opt})$ that can minimize $T_{\rm chip}$ is expressed by

$$I_{\rm opt} = \frac{\alpha(R_{th}T_c - \Delta TR_2)}{R_e(R_{th} + 2R_2)} \tag{1}$$

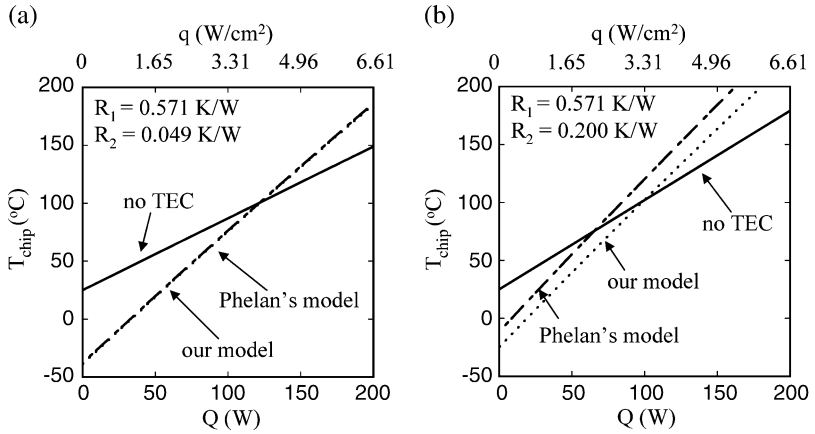


Fig. 3. Relations between the chip operating temperature ($T_{\rm chip}$) and the heat dissipation (Q) or the heat dissipation density (q) calculated by the different models are shown for (a) $R_2 = 0.049$ K/W and (b) $R_2 = 0.2$ K/W. The no TEC case is also shown as a solid line. Since the TEC is 5.5 × 5.5 cm^2, Q axis could be translated to heat power density (q) in W/cm^2 removed from the chip.

where ΔT is a temperature difference between the hot side and cold side of TEC, defined by $T_h - T_c$. If $R_{th} \gg R_2$ in the (1), $I_{\rm opt}$ is given by $I_{\rm opt} \approx \alpha T_c G/\rho$, which is consistent with the optimum current for Phelan's model. At above calculation condition, $R_{th} = 0.899$ W/K and $R_2 = 0.049$ K/W are used, which means that $R_{th} \gg R_2$. Therefore, our calculation result should be almost the same as the Phelan's calculation result.

Furthermore, as Phelan *et al.* noted previously, it can be seen that the TEC can be effective and cool the chip only when $Q < Q_{\rm max} = 125$ W, suggesting that the TEC is not always superior to that of nonrefrigeration systems. In other words, the TEC is beneficial if it is used below its maximum capacity in this condition.

Other important advantages offered by the TEC can also be seen from this figure. The minimum $T_{\rm chip}$ without a TEC is the ambient temperature, however, the minimum $T_{\rm chip}$ with a TEC is around -40 °C at $Q = 0$. This result indicates that the TEC can reduce the chip temperature below the ambient temperature, which is impossible for non-refrigeration systems.

Generally, the value of R_2 strongly depends on the heat sink. When we consider the total cost of the TE system, we might use a heat sink with a higher R_2 to reduce the cost. In order to investigate the effects of R_2 on the cooling performance, we changed the value of R_2 from 0.049 to 0.2 K/W, a value that is approximately the same level as typical thermal resistance of ArctiCoolers [8]. Fig. 3(b) shows the results for $R_2 = 0.2$ K/W, while keeping other calculation parameters same with the calculation in Fig. 3(a). A big difference between Phelan's calculation and ours is observed. It can be seen that the TEC calculated by our model exhibited at least 10 °C temperature reductions, compared with $T_{\rm chip}$ for the TEC calculated by Phelan's model in all cases. This result indicates that the current optimization taking into account R_2 provides significant effect to enhance the TEC potential. Solbrekken *et al.* reached a similar conclusion in [2], [3]. Furthermore, we can see that when $Q \approx 100$ W $T_{\rm chip}$ calculated by our model corresponds to that of no TEC, which is different from Fig. 3(a). This result indicates that the range of Q where the performance of TEC is better than that of no TEC becomes smaller as the value of R_2 is increased. Therefore, it can be said that the value of R_2 is a very important factor that can determine the performance of a TEC.

The geometrical factor (G) is another parameter influencing the TEC's performance because it changes the value of R_e and R_{th}. In our paper, the TEC geometry factor (G) is defined by the equation $G = S/L$, where S is the TE element's cross-sectional area and L is its leg length. In order to further improve the performance of the TEC, G and I were optimized at the same time without changing other parameters. A comparison of the results with and without TEC is shown in Fig. 4(a) for $R_1 = 0.571$ K/W and $R_2 = 0.2$ W/K. In the calculation for the case with TEC, the G and I were determined to minimize $T_{\rm chip}$ at a given Q (or q). q is also calculated by assuming the device area of the TEC is 5.5 × 5.5 cm^2. A great improvement is observed from this figure. Optimized TE modules calculated by our model can increase the heat dissipation power Q by at least 15% in comparison with the case without TEC while maintaining the chip temperature below 100 °C. Furthermore, one can see that $T_{\rm chip}$ for the TEC is always lower than that for no TEC in the entire range of this calculation for all Q. The results show that G optimization of the TE elements is also very useful to decrease the chip operating temperature if the heat flow rate generated by the chip can be determined.

Fig. 4(b) shows the value of the optimized G calculated for different levels of heat dissipation. It can be seen that the optimized G increases as Q increases. This result indicates that the optimum TEC leg length $(L_{\rm opt})$ is thinner as the chip power increases, assuming a constant cross-sectional area of the elements. Therefore, it can be said that there is an optimum leg length that gives the highest heat dissipation density to the IC chip and further thinning or thickening of its length degrades the TEC cooling performance. For example, at $Q = 100$ W, assuming the cross-sectional area of an element is 5 × 5 mm^2 (or 2 × 2 mm^2), the optimum length of each element becomes approximately 769 μm (or 123 μm), which is thinner than the leg thickness of a commercially available TEC (2–3 mm).

It was previously noted that R_2 is an important factor influencing the device performance although the value of R_1 was not critical [1]. Fig. 5 shows the relationships between R_2 and $T_{\rm chip}$ for a constant $Q = 100$ W with and without a TEC. The optimized I and G were used for this calculation. For the purpose of comparison, the result calculated by the Phelan's model (without the optimization of G and I considering R_2) is shown

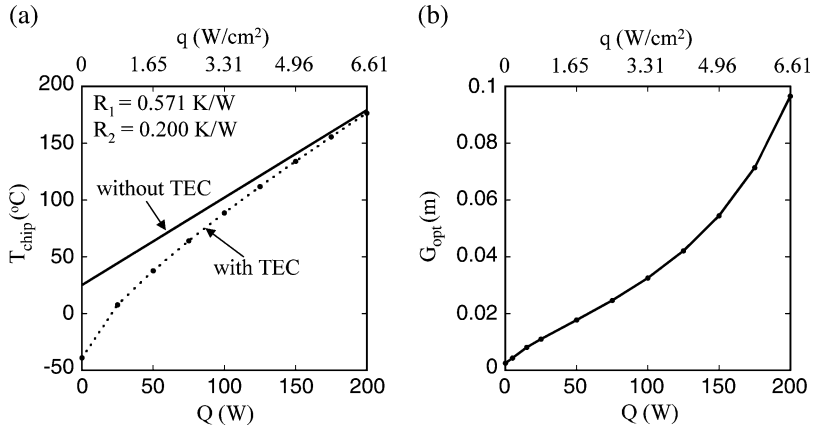


Fig. 4. (a) Relationship between $T_{\rm chip}$ and Q (or q) calculated by using optimized G and I is shown for $R_1 = 0.571$ K/W and $R_2 = 0.2$ K/W. The result for no TEC is also shown as a solid line. (b) The optimized G for different levels of Q is shown. Here, G is a geometrical factor equal to the cross-sectional area (S) divided by the leg length of each element (L) in a couple.

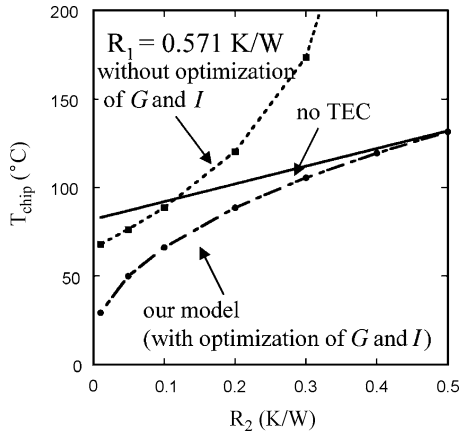


Fig. 5. Relationship between R_2 and $T_{\rm chip}$ for a constant $Q = 100$ W with and without a TEC are shown. The result calculated without the optimization of G and I is also shown as a dotted line.

as a dotted line. In this calculation range, optimally designed TEC is able to lower the chip temperature compared to the no TEC case in the entire range although the effectiveness of TEC is reduced as R_2 increases. At high values of R_2 heat generated by TEC can't be sufficiently dissipated to ambient air and thus TEC does not give any improvement. On the other hand, if G and I are not optimized, $T_{\rm chip}$ increases exponentially with R_2. Therefore, it can be said that this optimization method is very effective to increase the TEC potential at various external thermal resistances.

We have discussed the way to improve device performance without changing material parameters so far. Generally, the material property is expressed by using the figure of merit Z, which can be described by the equation $Z = \alpha^2/\rho k$ [9]. Recently, a new way to improve the material property was proposed by using low dimensional structures, thermionic emission and by reducing phonon transport [10]–[13]. For example, $ZT = 2.4$ was achieved with the $\rm Bi_2Te_3$ superlattice structure by Venkatasubramanian *et al.* [12]. Harman *et al.* demonstrated the PbSeTe/PbTe quantum dot superlattice with $ZT = 1.6$ [13]. Additionally, there is no physical limitation on how large ZT could be for a material. Therefore, the ZT for commercial devices is expected to reach 2 or 3 in the near future. Fig. 6(a) shows the results for various ZT values with and without TEC for $R_1 = 0.571$ K/W and $R_2 = 0.2$ K/W. As shown in the equation of Z, it is possible to change Z by controlling three material properties: α, ρ, and k. Even though Simmons *et al.* [5] claimed that α is a more important factor to improve maximum cooling performance of TEC module in a packaged system, we found that improving Z by each of the three parameters has approximately the same effect when TEC is used to cool the whole chip. This is due to full optimization of both TEC operating current I and its geometry factor G to minimize $T_{\rm chip}$. Therefore, Z is improved by changing α in this calculation. All other material parameters such as k and ρ are unchanged. On the other hand, in cases when the TE element is used for hot spot removal directly on the chip, we have shown that Z is not the main parameter determining the maximum cooling. In these particular applications, Seebeck coefficient plays a more important role due to 3-D heat and current spreading [14], [15].

In this calculation, G and I for TEC case are also optimized to minimize $T_{\rm chip}$. It can be seen that the performance of TEC can be improved dramatically as ZT increases. At $Q = 100$ W, the difference of $T_{\rm chip}$ between the value of $ZT = 3$ and no TEC reaches about 70 °C. This result indicates that the TEC will be a more beneficial technique to cool the chip compared with other cooling technology at higher ZT values. From these results, we can conclude that the device design which takes account of R_2 as well as the improvement of material properties is key factor to increase the TEC's potential in IC chip thermal management.

Fig. 6(b) shows the optimum current and consumed power as a function of Q at various ZTs. The optimum current increases with an increase of Q at any ZTs. One may point out that the value of the optimum current at higher Q is quite large to drive the TEC. However, it should be noted that the operating current of TEC module could be reduced (at the expense of higher voltages) by using larger number of elements and smaller cross section for each element but keeping the cooling power the same. Meanwhile, the consumed power of all the plots saturates at some point, and decreases especially in case of the plot for $ZT = 0.8$. This is due to a reduction of the TEC's electrical

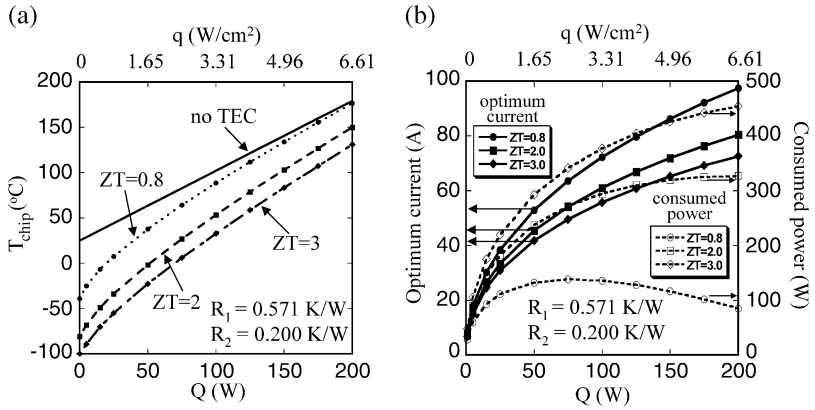


Fig. 6. (a) Relationship between $T_{\rm chip}$ and Q (or q) is shown for the various ZTs with and without a TEC for $R_1 = 0.571$ K/W and $R_2 = 0.2$ K/W. The result for no TEC is also shown as a solid line. (b) The optimum current for maximum cooling and consumed power as a function of Q at various ZTs.

resistance (R_e) because an optimum G, which changes R_e, increases with an increase of Q. Both of the optimum current and consumed power increase when the ZT is larger, indicating that there is a tradeoff between lower $T_{\rm chip}$ achievement and consumed power.

Until now, we basically discussed the heat dissipation of the TEC module (Q in W) instead of the heat dissipation density (q in W/cm^2). As we mentioned previously, if the TEC area is fixed, q can be calculated from the geometry. For example, assuming the device geometry of the TEC is 5.5 × 5.5 cm^2, Q of 100 W could be translated to heat power density (q) of 3.31 W/cm^2 removed from the chip. However, we can use any combination of the cross-sectional area (S) and leg length of the TE elements (L) at the constant $G = S/L$, suggesting the maximum cooling capacity itself may be changed even if G is constant.

The analytical solution for the cooling capacity of the TEC obtained from the circuit model in the package environment, can be expressed by

$$Q = \frac{2NI\alpha(T_c R_{th} - \Delta T R_2) - NI^2 R_e(R_{th} + 2R_2) - (T_a - T_c)}{(R_{th} + R_2)} \tag{2}$$

where $T_c = T_{\rm chip} - QR_1$. The external unit thermal resistances $(R^*_{1,2})$ of the package are given by the equation $R^*_{1,2} = R_{1,2}A$ where A is the area of contact and $R_{1,2}$ is the external thermal resistance [1]. If we assume that the area of the TE elements $(2NS)$ is a half of the total area of the TEC (50% coverage), and that R_1 and R_2 are inversely proportional to the total area of the TEC, the heat dissipation density of the TEC in the package environment can be given by

$$q = \frac{Q}{2 \cdot 2NS} = \frac{I^*\alpha\left(T_c\frac{L}{k} - \Delta T\frac{R_2^*}{2}\right) - I^{*2} \cdot \frac{\rho L}{2}\left(\frac{L}{k} + \frac{2R_2^*}{2}\right) - (T_a - T_c)}{2\left(\frac{L}{k} + \frac{R_2^*}{2}\right)} \tag{3}$$

where $T_c = T_{\rm chip} - qR_1^*$, I^* is a current density given by the equation $I^* = I/S$, R_1^* is the unit thermal resistance between the IC chip and the cold side of TEC described by the $R_1^* = R_1 \times 4NS$ and R_2^* is the unit thermal resistance between the hot side of TEC and ambient described by the $R_2^* = R_2 \times 4NS$. From the (3), one can understand that the heat dissipation density (q) is independent of N and S. In other words, q is only dependent of L and I^* when the material properties and unit thermal resistance are given. Therefore, if the total area of the TE elements $(2NS)$ is changed by increasing S, it induces only the decrease of I^*.

Generally, the chip operating temperature has to be less than 100 °C to avoid significant degradation due to electromigration or oxide breakdown. Therefore, the maximum heat dissipation density at $T_{\rm chip} = 100$ °C $(q_{\max})$ was calculated as a function of R_2^* and ZT. R_1^* at $R_1 = 0.571$ K/W and R_2^* at $R_2 = 0.2$ K/W are estimated to be 1.73×10^{-3} and 6.05×10^{-4} m^{2}K/W, respectively, assuming A is 5.5 × 5.5 cm^2 (the area of TEC module). In real configuration, the contact area of the IC chip could be different from the total area of TEC module, and a spreading resistance should be introduced.

Fig. 7(a) shows a contour plot of $q_{\max}$ as a function of R_2^* and ZT. We fixed $R_1^* = 1.73 \times 10^{-3}$ m^{2}K/W and other device and material parameters except for α and L in our calculation, and then found $q_{\max}$ for each value of R_2^* and ZT. In this calculation L and I^* are also optimized to minimize $T_{\rm chip}$. For the purpose of comparison, $q_{\max}$ calculated from no TEC case is shown on the top of graph. From Fig. 7(a), we can clearly see that $q_{\max}$ is maximized at high ZT and low R_2^*. When R_2^* is reduced from 6.05×10^{-4} (current technology value) to 1.61×10^{-4} m^{2}K/W (a factor of 3.75), the value of $q_{\max}$ is changed from 3.70 to 5.44 W/cm^2 at $ZT = 0.8$; nearly a factor of 1.47 higher. Meanwhile, the value of $q_{\max}$ is changed from 3.70 to 5.52 W/cm^2 at $R_2^* = 6.05 \times 10^{-4}$ m^{2}K/W; nearly a factor of 1.49 higher, when ZT is varied from 0.8 to 3.0 (a factor of 3.75). This result indicates that the decrease of R_2^* has the almost same effect on the device performance as the increase of ZT. Furthermore, in this calculation range, it is clear that $q_{\max}$ of TEC is always higher than that of no TEC case.

Fig. 7(b) shows calculation results of the optimized TE leg length $(L_{\rm opt})$ for each $q_{\max}$ as a function of R_2^* and ZT. $L_{\rm opt}$ becomes shorter as R_2^* and ZT decreases. For example, at $R_2^* = 6.05 \times 10^{-4}$ m^{2}K/W and $ZT = 0.8$, the optimum length of each element becomes approximately 662 μm which is shorter than

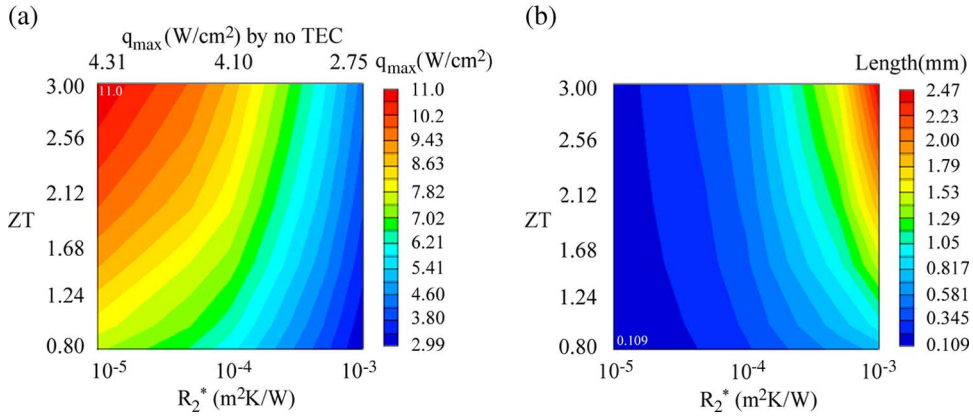


Fig. 7. Effect on R_2^* and ZT on $q_{\max}$(W/cm^2) at $T_{\rm chip} = 100\ ^\circ$C and optimum leg length is shown. (a) Contour plot of $q_{\max}$(W/cm^2) at $T_{\rm chip} = 100\ ^\circ$C as a function of R_2^* and ZT. (b) Contour plot of optimized leg length for each $q_{\max}$ as a function of R_2^* and ZT. $R_1^* = 1.73 \times 10^{-3}$(m^{2}K/W) is assumed for the calculation.

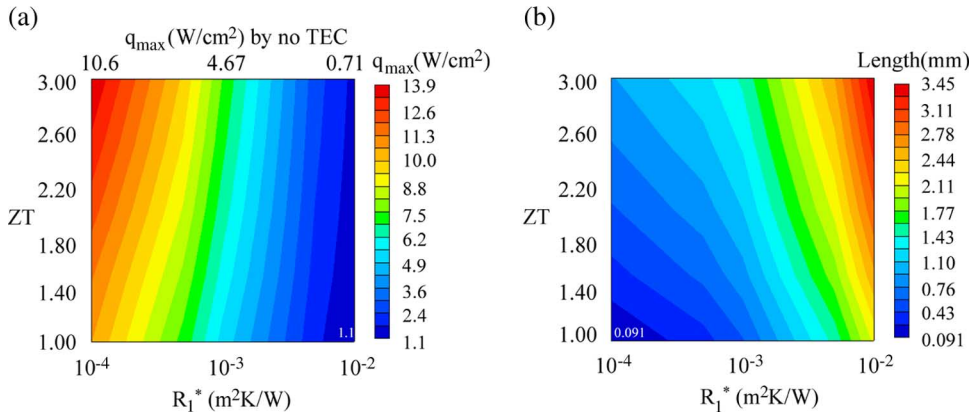


Fig. 8. Effect on R_1^* and ZT on $q_{\max}$(W/cm^2) at $T_{\rm chip} = 100\ ^\circ$C and optimum leg length is shown. (a) Contour plot of $q_{\max}$ as a function of R_1^* and ZT. (b) Contour plot of optimized L for each $q_{\max}$ as a function of R_1^* and ZT. $R_2^* = 6.05 \times 10^{-4}$ m^{2}K/W (current technology value) is assumed.

the leg thickness of a commercially available TEC (2–3 mm). Since the TEC with the short leg has a smaller thermal resistance between cold and hot sides, more heat conduction occurs across the TEC. Therefore, a short leg TEC with low ZT basically needs lower R_2 or R_2^* to dissipate the high heat flux at the hot end to the ambient air for the better performance.

We also investigated the R_1^* effect on $q_{\max}$. Fig. 8(a) shows a contour plot of $q_{\max}$ as a function of R_1^* and ZT. We fixed $R_2^* = 6.05 \times 10^{-4}$ m^{2}K/W (current technology value) and similar calculation to Fig. 7 was carried out. For the purpose of comparison, $q_{\max}$ calculated from no TEC case is also shown on the top of the graph. One can also see that $q_{\max}$ is maximized at high ZT and low R_1^*. Under our calculation conditions, $q_{\max}$ for TEC case is always higher than that for no TEC case. When R_1^* is reduced from 1.73×10^{-3} (current technology value) to 4.61×10^{-4} m^{2}K/W (a factor of 3.75), the value of $q_{\max}$ is changed from 3.70 to 7.19 W/cm^2 at $ZT = 0.8$; nearly a factor of 1.94 higher. This result indicates that the decrease of R_1^* is the most effective to enhance the maximum heat dissipation density under our conditions, compared with an increase of ZT or decrease of R_2^*. Fig. 8(b) shows calculation results of the optimized TE leg length ($L_{\rm opt}$) for each $q_{\max}$ as a function of R_1^* and ZT. As similar to Fig. 7(b), $L_{\rm opt}$ become shorter at lower ZT and R_1^*.

Form these results, it can be said that the TEC with the thin leg length is necessary to increase the TEC performance as the external thermal resistances are improved. However, if the leg length of element (L) becomes shorter, the effect of the contact resistance may become significant for the TEC performance because this may induce an additional Joule heating. In the following calculation, the effect of the contact resistance on the maximum heat dissipation density was investigated. In our model, the contact resistance (ρ_c/S) can be added to the electrical resistance of the TEC as $R_e = \rho/G + 2\rho_c/S$ for a simple calculation, assuming that the contact resistance is equally distributed between the hot and cold sides [16]. The factor 2 in the second term of right hand is due to the both sides' contact with the metal electrode. Therefore, the heat dissipation density of TEC module including the effect of the contact resistance can be expressed by

$$q = \frac{Q}{2 \cdot 2NS} = \frac{I^*\alpha\left(T_c\frac{L}{k} - \Delta T\frac{R_2^*}{2}\right) - I^{*2}\cdot\frac{(\rho L + 2\rho_c)}{2}\left(\frac{L}{k} + \frac{2R_2^*}{2}\right) - (T_a - T_c)}{2\left(\frac{L}{k} + \frac{R_2^*}{2}\right)} \quad (4)$$

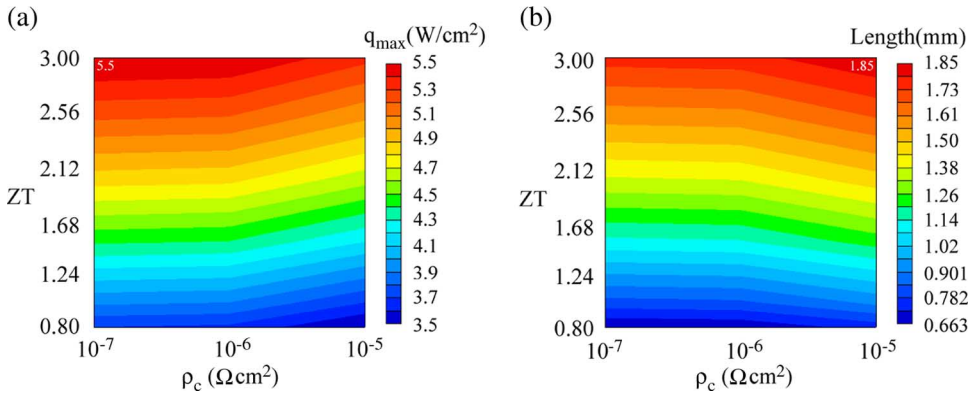


Fig. 9. Effect of ρ_c and ZT on $q_{\max}$(W/cm^2) at $T_{\text{chip}} = 100$ °C and optimum length is shown. (a) Contour plot of $q_{\max}$ as a function of ρ_c and ZT. (b) Contour plot of optimized L for each $q_{\max}$ as a function of ρ_c and ZT. $R_1^* = 1.73 \times 10^{-3}$ m^{2}K/W and $R_2^* = 6.05 \times 10^{-4}$ m^{2}K/W (current technology values) are assumed for the calculation.

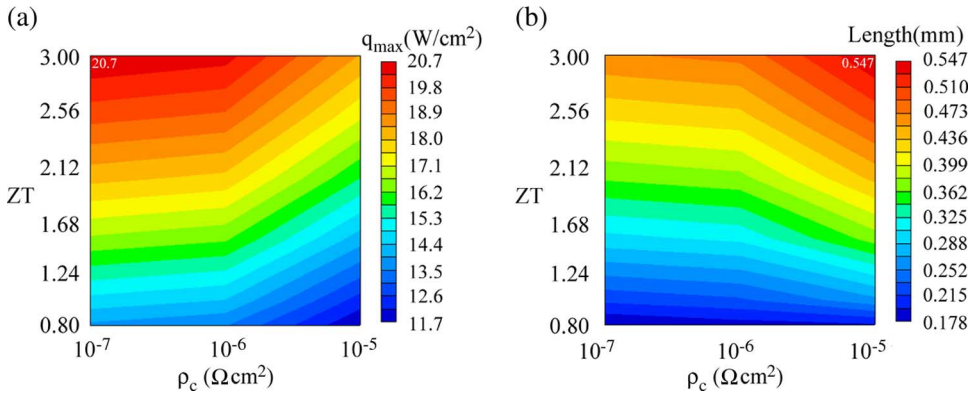


Fig. 10. Effect of ρ_c and ZT on $q_{\max}$(W/cm^2) at $T_{\text{chip}} = 100$ °C and optimum length is shown when R_1^* and R_2^* are improved by a factor of 3.75 compared with the current technology values. (a) Contour plot of $q_{\max}$ as a function of ρ_c and ZT. (b) Contour plot of optimized L for each $q_{\max}$ as a function of ρ_c and ZT. $R_1^* = 4.61 \times 10^{-3}$ m^{2}K/W and $R_2^* = 1.61 \times 10^{-4}$ m^{2}K/W are assumed.

where ρ_c is the contact resistivity. To investigate the contact resistance effect, ρ_c was changed in the ranges from 10^{-5} to 10^{-7} Ωcm^2, and the similar calculation to Fig. 7 was performed. The calculation results are shown in Fig. 9(a) and (b). Fig. 9(a) shows a contour plot of $q_{\max}$ at $T_{\text{chip}} = 100$ °C as a function of ρ_c and ZT. $R_1^* = 1.73 \times 10^{-3}$ (m^{2}K/W) and $R_2^* = 6.05 \times 10^{-4}$ m^{2}K/W (current technology values) are assumed for the calculation. When ρ_c less than 10^{-6} Ωcm^2, the effect of ρ_c on $q_{\max}$ is very small (less than 1% reduction compared with no ρ_c case) because the optimum length is also changed to minimize the additional Joule heating in our calculation as shown in Fig. 9(b). Meanwhile, when ρ_c approaches to 10^{-5} Ωcm^2, the effect of ρ_c on $q_{\max}$ become significant (approximately 6% reduction at $ZT = 0.8$) even if the current and TE leg length are optimized. Therefore, it can be concluded that the contact resistivity should be reduced less than 10^{-6} Ωcm^2 to avoid the significant reduction of $q_{\max}$ in the current packaging technology. Fig. 9(b) shows the contour plot of the optimum leg length as a function of ρ_c and ZT. One can see that the optimum leg length decreases when ρ_c is larger, which is due to the avoidance of the excess additional Joule heating.

Finally, the effect of ρ_c on $q_{\max}$ was investigated when both R_1^* and R_2^* are improved by a factor of 3.75 compared with the current technology values. Fig. 10(a) shows a contour plot of $q_{\max}$ at $T_{\text{chip}} = 100$ °C as a function of ρ_c and ZT at $R_1^* = 4.61 \times 10^{-3}$ m^{2}K/W and $R_2^* = 1.61 \times 10^{-4}$ m^{2}K/W. As similar to Fig. 9(a), it can be seen that $q_{\max}$ is not so sensitive to ρ_c when ρ_c is less than 10^{-6} Ωcm^2 (less than 3% reduction compared with no ρ_c case). However, $q_{\max}$ is reduced by 11%∼16% in comparison with the case without contact resistance at $ZT = 0.8 \sim 3.0$ when ρ_c reaches to 10^{-5} Ωcm^2. Therefore, it is clear that the reduction of the contact resistance becomes important as the external thermal resistances are improved. A contour plot of optimum leg length as a function of ρ_c and ZT is shown Fig. 10(b). One can clearly see that the optimum leg length shown in Fig. 10(b) is much shorter that shown in Fig. 9(b). Therefore, it can be said that the reason why the contact resistance gives the significant effect to $q_{\max}$ when the external thermal resistance is improved is due to lower optimum leg length. As similar to the conclusion from Fig. 9, it is very important that the contact resistivity is reduced less than 10^{-6} Ωcm^2 to avoid additional Joule heating effect even if the external thermal resistance is improved.

IV. Conclusion

The BiTe-based TEC integrated with an IC and heat sink was analyzed by the 1-D equivalent circuit model. When the thermal resistance between the hot side of a TEC and ambient temperature (R_2), is not negligible compared with the thermal resistance

of the TE element (R_{th}), our calculation shows the current optimization considering R_2 is very effective to maximize the TEC performance. Furthermore, if we can optimize the geometrical factor (G) as well as I considering R_2 at a given heat dissipation, optimally designed TE modules calculated by our model can increase the chip operation power by at least 15% in comparison with the case without a TEC while maintaining the chip temperature below 100 °C. Therefore, it can be concluded that the optimization of G and I considering the external thermal resistance at a given Q has significant impact on a TEC's performance to reduce $T_{\rm chip}$. With existing package level thermal resistance ($R_1 = 0.571$ K/W and $R_2 = 0.200$ K/W), optimum TE module length is 0.612–1.76 mm and maximum heat dissipation density should be 3.70–5.52 W/cm^2 with a ZT of 0.8–3.0. There is 13.3% to 41.9% improvement compared to no TEC case. By improving external thermal resistances, TE modules with a thinner leg length and higher ZT can increase the heat dissipation density. The effect of the contact resistance on the power dissipation density was investigated. The reduction of the power dissipation density was less than 3.0% compared to no contact resistance model when the contact resisitivity is less than 10^{-6} Ωcm^2 even if the external thermal resistance is improved.

REFERENCES

[1] P. E. Phelan, V. A. Chiriac, and T. Y. Lee, "Current and future miniature refrigeration cooling technologies for high power microelectronics," *IEEE Trans. Compon. Packag. Technol.*, vol. 25, no. 3, pp. 356–365, Sep. 2002.

[2] G. Solbrekken, K. Yazawa, and A. Bar-Cohen, "Chip level refrigeration of portable electronic equipment using thermoelectric devices," presented at the International Electronic Packaging Technical Conference and Exhibition (InterPack'03), Maui, HI, Jul. 6–11, 2003, [CD ROM].

[3] R. Taylor and G. Solbrekken, "An improved optimization approach for thermoelectric refrigeration applied to portable electronic equipment," presented at the International Electronic Packaging Technical Conference and Exhibition (InterPack'05), San Francisco, CA, Jul. 17–22, 2005, [CD ROM].

[4] R. Simons and R. Chu, "Application of thermoelectric cooling to elecric equipment: a review and analysis," in *Proc. 16th IEEE SEMI-THERM Symp.*, 2000, pp. 1–9.

[5] R. E. Simons, M. J. Ellsworth, and R. C. Chu, "An assessment of module cooling enhancement with thermoelectric coolers," *Trans. ASME*, vol. 127, pp. 76–84, 2005.

[6] D. Vashaee, J. Christofferson, Y. Zhang, A. Shakouri, G. Zeng, C. LaBounty, X. Fan, J. Piprek, J. E. Bowers, and E. Croke, "Modeling and optimization of single-element bulk SiGe thin-film coolers," *Microsc. Thermophys. Eng.*, vol. 9, pp. 99–118, 2005.

[7] Melcor, Inc., "Thermoelectric cooler," Tech. Rep. CP5-31-06, 2006 [Online]. Available: http://www.melcor.com/CP_Series/CP5-31-06L.PDF

[8] G. Wagner, "Optimization of the arcticooler for lowest thermal resistance in a minimum volume," in *Proc. Intersoc. Conf. Thermal Phenom.*, 2000, pp. 180–184.

[9] D. M. Rowe, *CRC Handbook of Thermoelectrics*. New York: CRC, 1995.

[10] L. D. Hicks and M. S. Dresselhaus, "Thermoelectric figure of merit of a one-dimensional conductor," *Phys. Rev.*, vol. B47, pp. 16631–16634, 1993.

[11] D. Vashaee and A. Shakouri, "Improved thermoelectric power factor in metal-based superlattices," *Phys. Rev. Lett.*, vol. 92, p. 106103, 2004.

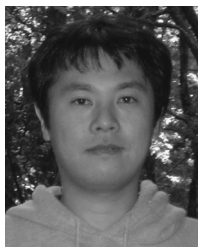
[12] R. Venkatasubramanian, E. Siivola, T. Colpitts, and B. O'Quinn, "Thin-film thermoelectric devices with high room-temperature figures of merit," *Nature*, vol. 413, pp. 597–602, 2001.

[13] T. C. Harman, P. J. Taylor, M. P. Walsh, and B. E. LaForge, *Science*, vol. 297, pp. 2229–2232, 2002.

[14] K. Fukutani and A. Shakouri, "Optimization of thin film microcoolers for hot spot removal in packaged integrated circuits," in *Proc. SEMI-THERM'06*, Dallas, TX, Mar. 14–16, 2006, pp. 130–134.

[15] Y. Zhang, G. Zeng, A. Bar-Cohen, and A. Shakouri, "Is ZT the main performance factor for hot spot cooling using 3D microrefrigerators?," in *Proc. IMAPS Therm. Manag.*, Palo Alto, CA, Oct. 26–28, 2005, [CD ROM].

[16] G. Nolas, J. Sharp, and H. Goldsmid, *Thermoelectrics: Basic principles and New Materials Developments*. New York: Springer, 2001, p. 167.



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