MEMS Applications of CMP

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Abstract— In order to keep pace with tight designs for MEMS, CMP has started to be adopted. In this report, some MEMS devices fabricated with CMP are shown, and some possible areas in which CMP can make contribution to are suggested.

Keywords: CMP, MEMS, SUMMiT, and multi-level structures.

1. Introduction

Like IC devices, multi-level structures have been widely used in the MEMS devices. Micro engines, pressure sensors, micromechanical fluid pumps, micro mirrors, and micro lenses are good examples of these structures. Since these devices include moving parts within the multi-level structures, planarity issues have attracted attention for a long time.

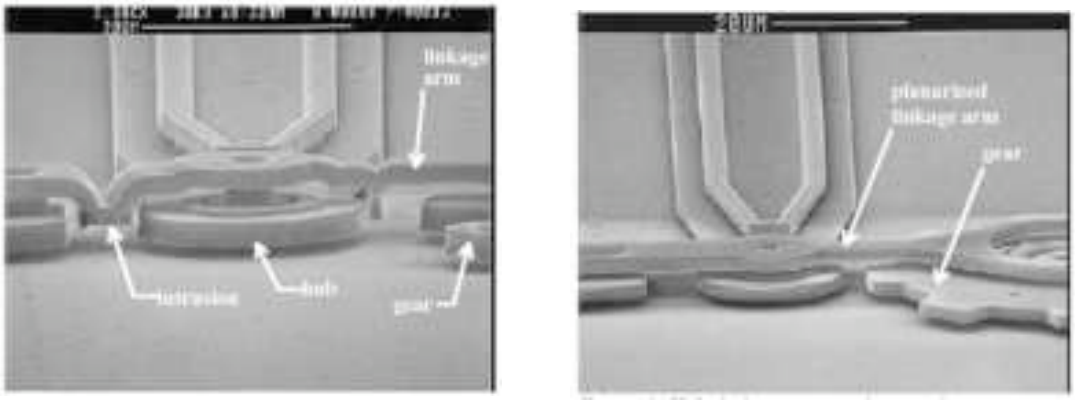

Figure 1. Micro-engine without CMP (left) and with CMP (right).

In order to address these planarity issues, CMP has emerged as a solution. For example, the *Sandia* Ultra-planar, Multi-level MEMS Technology (SUMMiT™) fabrication process, one of the big MEMS foundries, employs the multi-layer polycrystalline silicon surface micromachining process. This process polishes the silicon dioxide sacrificial layers every time before depositing another polycrystalline silicon layer. The reason being is that intrusion of upper polycrystalline levels into gaps, left between lower polycrystalline silicon levels, complicates the design and limits layout flexibility, in addition to causing undesirable areas of stress concentration. The intrusions are inevitable without the help of CMP, but these problems are completely overcomed by the use of CMP in fabrication. One typical example is shown in Figure 1. Figure 2 also shows the

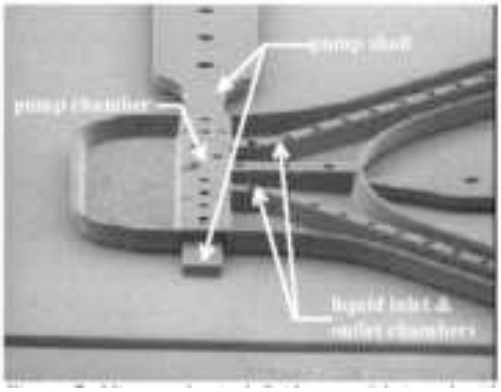

Figure 2. Micromechanical fluidic pump fabricated using with CMP.

benefit of adopting CMP in the fabrication of a micromechanical fluid pump. The planar top surface of the pump chamber indicates that there is no protrusion of the top polycrystalline silicon into the enclosed pump mechanism. Other examples are the optical MEMS devices - micro mirrors, micro lenses – and field emission devices. As the operating wavelength gets smaller, the flatness requirement for lenses is stringent. Researchers at Case Western have used to improve the optical quality of mirrored surfaces produced on polycrystalline silicon, suface-micromachined devices, by reducing the roughness of the polycrystalline silicon. Improved performance of a lateral field emission device using CMP is also reported.

2. Discussion

There is no major difference between polishing MEMS devices and IC devices, because the same materials are used and the same machine can be used. The only and interesting difference between MEMS and IC from the CMP perspective is the involved step height. While the step height for IC is at most 1.0 μm, the step height for MEMS can be as large as 5 μm. The large step height associated with MEMS devices might present a challenge, since it will affect, especially at earlier times in the processing, a lot of factors such as pad deformation, slurry flow, uniformity, etc.

3. Outlook

At this point, the CMP process used in MEMS is not as critical as it is in IC. It seems that there is not much benefit from using the CMP process in multi-level structure MEMS devices. However, the time will come when people will revise the processes in order to accommodate shrinking device sizes. In order to seize the moment, experiments on larger step heights (~5 um) and step height evolution versus time under various process conditions need to be conducted.

The first area that can possibly benefit the best from CMP is the optical MEMS area, which is emerging nowadays. The surface of a micro-mirror or micro-lens used in optical MEMS requires flatness as well as nano-scale surface finish. The importance of the surface will become more evident as the wavelength of a light source gets smaller and smaller. CMP will be the method of choice that people will look for, since CMP has successfully solved very similar problems in IC.

Overall process steps for the SUMMiT-V process

1. Start with a Si substrate
2. Grow 0.6um of oxide thermally
3. CVD 0.8um of Si_3N_4
4. Dry-etch Si_3N_4 (thru)
5. Etch thermal oxide
6. CVD 0.3um of polySi (the layer called Poly0)
7. Dry-etch Poly0
8. CVD SacOx1 and CMP to leave 2um of SacOx1 from poly0
9. Do a Dimple1 Cut (dry-etch, 1.5um)
10. Dry-etch SacOx1 Cut (2um)
11. CVD 1um of Poly1
12. Pinjoint Cut (dry-etch)
13. Pinjoint Undercut (dry-etch oxide)
14. Pinjoint undercut (wet-etch oxide)
15. Dry-etch Poly1 (1 um)
16. CVD SacOx2 and CMP to leave 0.3um
17. Dry-etch SacOx2 (0.3um)
18. CVD 1.5um of Poly2
19. Dry-etch Poly2 (up to 2.5um)
20. CVD SacOx3 and CMP to leave 1.6um
21. Dimple3 Cut (dry-etch)
22. Dimple3 backfill, CVD
23. SacOx3 dry etch (0.4 um)
24. CVD Poly3 and CMP to leave 2.2um
25. Dry-etch Poly3 (2.2um)
26. CVD SacOx4 and CMP to leave 1.8um
27. Dry-etch Dimple4 Cut
28. Dimple4 backfill, CVD
29. Dry-etch SacOx4 (1.8um)
30. CVD 2.2um of Poly4
31. Dry-etch Poly4 (2.2um)
32. CVD 0.4 um of Aluminum
33. MMetal wet etch (thru Al)
34. RELEASE structure.