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High-efficiency, high-speed VCSELs for optical interconnects

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Abstract High-efficiency, high-speed, tapered-oxide-apertured vertical-cavity surface-emitting lasers (VCSELs) emitting at 980 nm have been demonstrated. By carefully engineering the tapered oxide aperture, the mode volume can be greatly reduced without adding much optical scattering loss for the device sizes of interest. Consequently, these devices can achieve higher bandwidth at lower current and power dissipation. In addition, the parasitics are reduced by implementing deep oxidation layers and an improved *p*-doping scheme in the top mirror. Our devices show modulation bandwidth exceeding 20 GHz, a record for 980 nm VCSELs. Moreover, 35 Gb/s operation has been achieved at only 10 mW power dissipation. This corresponds to a data-rate/power-dissipation ratio of 3.5 Gbps/mW. Most importantly, our device structure is compatible with existing manufacturing processes and can be easily manufactured in large volume making them attractive for optical interconnects.

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1 Introduction

Through scaling and integration, the performance of microprocessors is consistently improving to the point that current copper-based interconnects are slowly becoming the bottleneck due to their physical limitations [1]. More and more power and chip real state have been devoted to interconnects. In addition, signal loss, distortion, and cross-talk in electrical interconnects become worse as frequency increases. In order to keep up the advance of microprocessors, new technology is required.

Optics is a viable alternative to copper interconnects because it offers the advantages of short signal delay, high bandwidth, low power dissipation, and freedom from electromagnetic interference. In the past several years, vertical-cavity surface-emitting lasers (VCSELs) have received renewed interest for potential applications in optical interconnects [2]. Compared with edge emitters, VCSELs have several benefits: they have smaller footprint; they are easier to fabricate in arrays; they support on-wafer testing; they require less power to achieve high-speed operation; and they usually are less expensive to manufacture.

Recently, data rate up to 40 Gb/s with a 24 GHz bandwidth has been demonstrated for 1.1 μm wavelength VCSELs [3]. 30 Gb/s operation has also been reported for 850 nm wavelength VCSELs [4]. Here we present our work on high-efficiency, high-speed VCSELs emitting at 980 nm wavelength. Our devices show >20 GHz bandwidth and 35 Gb/s operation at only 10 mW power dissipation corresponding to a very high data-rate/power-dissipation ratio of 3.5 Gbps/mW.

2 Device structure

In optical interconnects, the transmitters convert signals from electrical to optical domain at comparatively high data rates, usually within compact systems with many active components but limited heat sink. Therefore, these devices must be capable of operating at speeds at least 20 Gb/s, be efficient to minimize power dissipation, be compatible with silicon electronics, and most importantly, be manufacturable in large volume with high yields and low costs.

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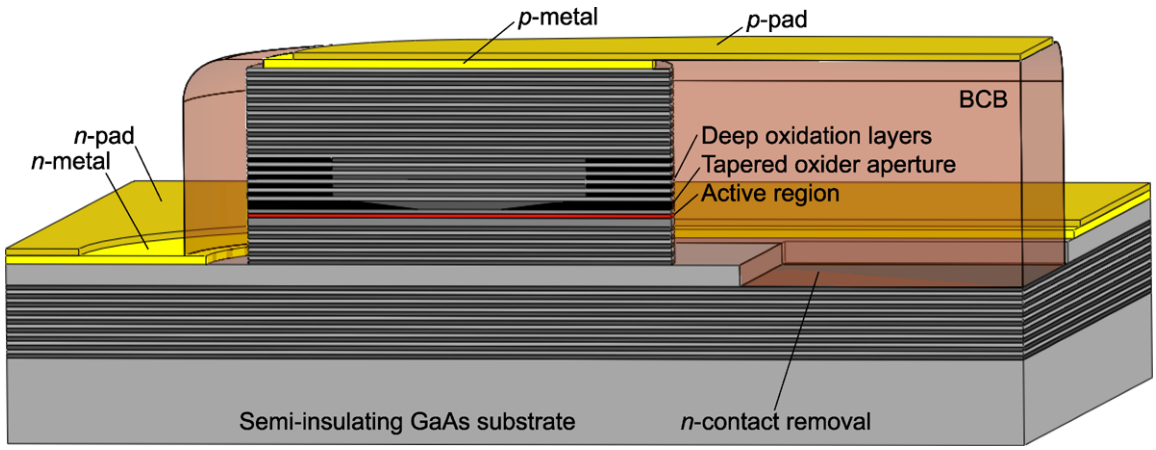

Fig. 1 Cross-sectional schematic of the device

In order to meet these requirements, *n*-intracavity, bottom-emitting, tapered-oxide-apertured structure, shown in Fig. 1, is used. Emission wavelength of 980 nm is chosen so that strained InGaAs/GaAs quantum wells (QWs), which provide higher gain at low carrier densities, can be used. In addition, this wavelength is transparent to GaAs substrate and hence enables us to use bottom-emitting structure. Bottom emission along with *n*-intracavity means that flip-chip bonding can be used to directly integrate VCSEL arrays with silicon electronics. This eliminates the need of individual wire bonding and the parasitics associated with bond wires. Moreover, backside microlenses can be fabricated to collimate output beams, which increase the alignment tolerance and reduce packaging costs [5].

The sample was grown on a semi-insulating GaAs (100) substrate by molecular beam epitaxy. The bottom mirror consists of a 14-period undoped AlAs/GaAs distributed Bragg reflector (DBR) followed by a five-quarter wavelength thick *n*-GaAs contact layer and a 4-period *n*-type $Al_{0.9}Ga_{0.1}As$/GaAs DBR. The *n*-contact layer is setback 4 periods to reduce the free carrier absorption loss and improve longitudinal mode confinement for high-speed consideration. The active region has three InGaAs/GaAs QWs embedded in a $Al_{0.3}Ga_{0.7}As$ separate confinement heterostructure (SCH) layer to form the cavity.

On top of the SCH is the oxide aperture. To achieve high bandwidth at low power dissipation, we redesigned our tapered oxide aperture for better lateral mode confinement. The aperture thickness increases from quarter-wavelength to half-wavelength thick and the taper length is also reduced from 4.3 to 4 μm. According to our simulation, this aperture yields a 31% improvement in relaxation resonance frequency for 3 μm diameter devices over our original design. In addition, the static performance is not sacrificed because the optical loss does not increase noticeably for device sizes down to 3 μm in diameter.

The top mirror has a 30-period AlGaAs/GaAs DBR. The aluminum fraction of the first 5 periods of DBR is increased from 85 to 93% to form deep oxidation layers [6]. When oxidizing the aperture, these high aluminum content layers oxidized comparatively faster than the other DBR periods forming thicker dielectric layers in the perimeter of the mesa. These oxidized layers effectively increase the equivalent capacitor thickness and reduce the parasitic capacitance. Compared with ion implantation commonly used to reduce the parasitic capacitance, our approach is simple and cost effective.

The parasitics are further reduced using the following approaches: The *p*-doping in the top mirror is carefully optimized to reduce the series resistance without introducing too much optical loss. The pad capacitance is reduced by (a) removing the part of the *n*-contact layer (RF ground) beneath the *p*-pad metal (RF signal), (b) inserting low dielectric constant resin Benzpcyclobutene (BCB) underneath the *p*-pad, and (c) shrinking the *p*-pad dimension to $40 \times 70\ \mu m^2$. Details of the fabrication can be found in [7].

3 Device results

Figure 2 shows the voltage, output power, and power dissipation against current curves for a 3 μm diameter device at 20°C.

The lasing wavelength is around 990 nm. The device has a slope efficiency of 0.67 W/A, corresponding to a differential quantum efficiency of 54%. The threshold current is only 0.144 mA, comparatively low for typical high-speed VCSELs with diameters ranging from 5 to 8 μm. This low threshold along with high slope efficiency indicates that our new tapered oxide aperture with shorter taper length does not introduce excess optical loss even down to 3 μm diameter range. The threshold voltage is 1.47 V, very low for such a small device, as it is only 220 meV larger than the photon

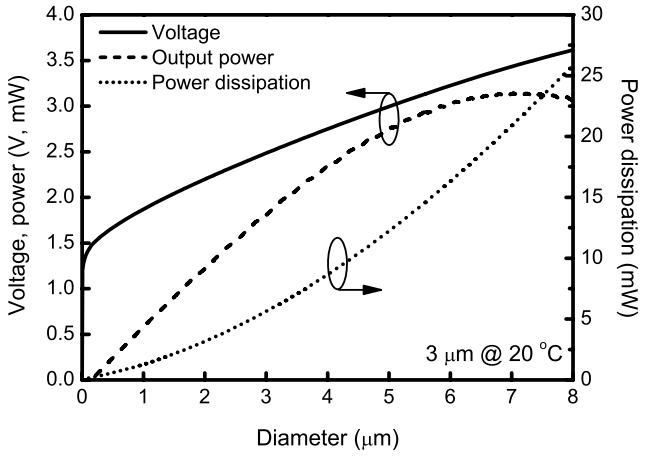

Fig. 2 Voltage, output power, and power dissipation against current curves for 3 μm diameter device at 20°C

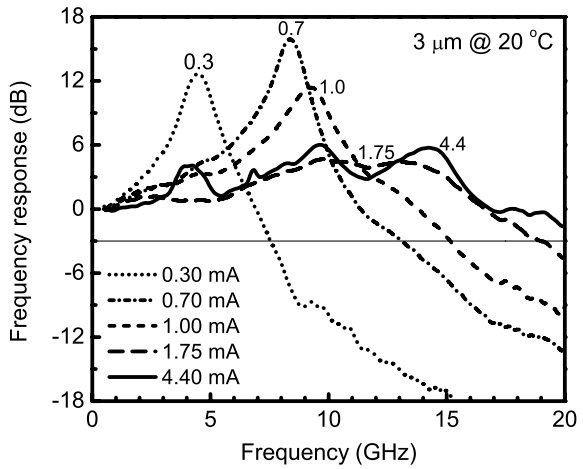

Fig. 3 Frequency responses for 3 μm device at 20°C under different bias currents

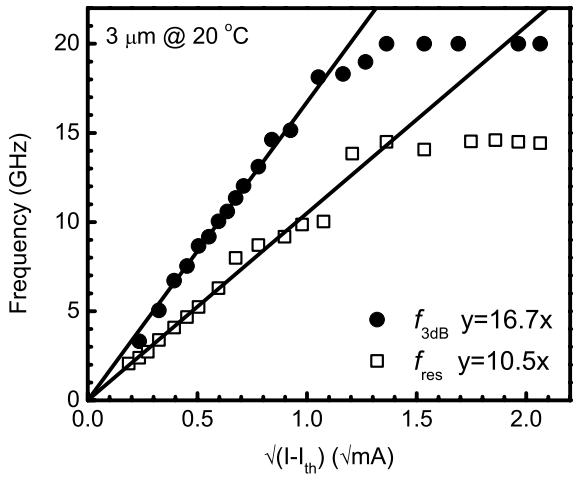

Fig. 4 Relaxation resonance frequency (f_{res}) and 3 dB frequency ($f_{3\,\mathrm{dB}}$) versus square root of the current above threshold

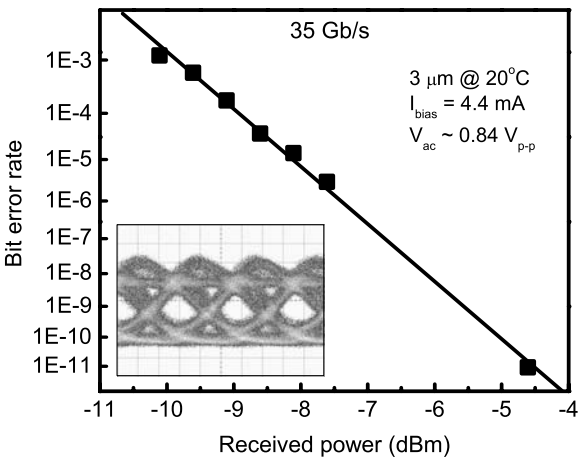

Fig. 5 Bit error rate curve at 35 Gb/s for 3 μm diameter device. This device was biased at 4.4 mA and a RF voltage swing of 0.84 $V_{p\text{-}p}$ was used. The inset shows the corresponding optical eye diagram with an extinction ratio of 5.4 dB

energy. This low threshold voltage is the consequence of our optimized p-doping scheme and low threshold current. The series resistance is approximately 250 Ω at a bias current of 4.4 mA, where the large-signal modulation experiments were performed. The thermal impedance is 3.3°C/mW, calculated by measuring the wavelength shift at different stage temperatures and at different biases [8]. At a bias current of 4.4 mA, the power dissipation and temperature rise are 10 mW and 33°C, respectively. The peak wall-plug efficiency, occurring at 1 mA, is 31% and the maximum output power is 3.1 mW.

Figure 3 shows the small-signal modulation responses for a 3 μm device under different bias currents. Bandwidth of 15 GHz is achieved with a bias current of only 1 mA. Limited by the instruments, frequency response could only be measured up to 20 GHz. However, it is evident that bandwidth exceeding 20 GHz has been achieved, highest for 980 nm VCSELs.

Figure 4 plots the relaxation resonance frequency, f_{res}, and 3 dB frequency, $f_{3\,\mathrm{dB}}$, as a function of the square root of the current above threshold. The modulation current efficiency factor (MCEF), defined as $f_{3\,\mathrm{dB}}/\sqrt{(I - I_{\mathrm{th}})}$, is 16.7 GHz/mA$^{1/2}$, very close to the highest reported value of 16.8 GHz/mA$^{1/2}$ for QW-based VCSELs [9]. This high MCEF is mainly due to better lateral mode confinement, consequence of our improved tapered oxide aperture design. The ratio of the slopes of $f_{3\,\mathrm{dB}}$: f_{res} is 1.59, close to the theoretical value of 1.55, indicating damping is not severe in our devices.

Figure 5 plots the bit error rate (BER) curve at 35 Gb/s for a 3 μm diameter device at 20°C. The experimental setup is given in [10]. The input was a non-return-to-zero (NRZ) signal with 2^7–1 word length. The bias current was 4.4 mA and the RF voltage swing was ~0.84 $V_{p\text{-}p}$. The inset of the

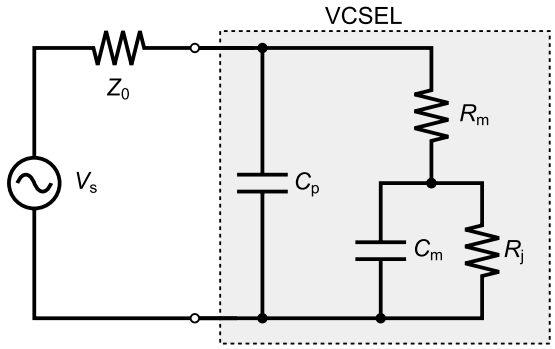

Fig. 6 Small-signal equivalent circuit model for the device. The device is represented by C_p, R_m, C_m, and R_j. V_s is the RF voltage source and $Z_0 = 50\ \Omega$ is the characteristic impedance of the instruments

figure shows the corresponding optical eye diagram. The eye is clearly open with an extinction ratio of 5.4 dB. In the BER curve, all the data points except the lowest one were taken with a variable optical attenuator (VOA). Owing to the ∼3 dB insertion loss of the VOA, the BER in the range of 10^{-4} to 10^{-7} could not be measured. Thus, the lowest data point at a received power of −4.7 dB was taken without the VOA. The BER is 9.2×10^{-12}, gated for 30 min with total 583 errors to ensure the accuracy of the measurement.

Since both high data rate and low power dissipation are desired for optical interconnects, a good figure-of-merit is the data-rate/power-dissipation ratio. At a bias current of 4.4 mA, the power consumption and dissipation of our devices, excluding the RF circuitry, were only 12.5 and 10 mW, respectively. This corresponds to a very high data-rate/power-dissipation ratio of 3.5 Gbps/mW.

Small-signal equivalent circuit model is useful to understand the bandwidth limitation due to parasitics. The circuit model for our devices, shown in Fig. 6, includes four elements: C_p, R_m, C_m, and R_j. The pad capacitance, C_p, represents all the capacitances between the p- and n-contacts outside the mesa. The mesa resistance, R_m, includes the contact resistances, DBR mirror resistances, and spreading sheet resistance associated with the n-contact layer. The mesa capacitance, C_m, includes the capacitances from the deep oxidation layers, oxide aperture, intrinsic layer beneath the aperture, and diode junction. R_j denotes the diode junction resistance for the active region. For the RF driving circuit side, V_s is the RF voltage source and $Z_0 = 50\ \Omega$ is the characteristic impedance of the instruments. Z_0 has to be included to account for the RF reflection due to impedance mismatch.

The values for these circuit elements can be determined by fitting S_{11} parameter as a function of frequency and bias current. Table 1 lists the extracted small-signal circuit elements for a 3 μm diameter device.

We have assumed R_m and C_p to be bias independent, which neglects any heating effects. C_m increases with current due to the increased diffusion capacitance and R_j deceases as current increases. Due to smaller size of our devices, R_j and R_m are larger than typical high-speed VCSELs. C_p is very small thanks to n-contact removal, BCB insertion, and pad-size reduction. C_m is also very small, resulting from the incorporation of deep oxidation layers and thicker oxide aperture.

Table 1 Extracted small-signal circuit elements for 3 μm diameter device at different bias currents. R_m and C_p are fitted to be 102.9 Ω and 29.1 fF. f_{rc} is the parasitic 3 dB frequency

Current (mA)	1.0	2.0	3.0	4.5	6.0
R_j (Ω)	274.4	192.7	168.2	146.5	126.7
C_m (fF)	57.1	66.7	75.4	87.9	100.0
f_{rc} (GHz)	27.0	25.9	24.6	22.8	21.8

The influence of the parasitics on modulation bandwidth is determined by calculating the transfer function of the current flowing through R_j over V_s. The −3 dB frequency of this transfer function, f_{rc}, is also listed in Table 1. At a bias current of 4.5 mA, f_{rc} is 22.8 GHz, indicating our devices are still partially limited by parasitics.

4 Conclusion

We have fabricated and characterized high-efficiency, high-speed 980 nm VCSELs. These devices are based on a structure that is compatible with existing manufacturing processes and can be easily mass produced. The 3 μm diameter devices demonstrated 35 Gb/s operation at a bias current of 4.4 mA, corresponding to only 10 mW power dissipation. This represents a data-rate/power-dissipation ratio of 3.5 Gbps/mW. Combined with high-speed operation, low power dissipation, and manufacturability, these devices are very attractive for optical interconnects. With improvements in active region design, suppression of higher-order modes, and reduction in parasitics, 40 Gb/s operation and beyond can be expected.

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References

1. D.A. B Miller, Int. J. Optoelectron. **11**, 155 (1997)
2. L. Schares, J.A. Kash, F.E. Doany, C.L. Schow, C. Schuster, D.M. Kuchta, P.K. Pepeljugoski, J.M. Trewhella, C.W. Baks, R.A. John, L. Shan, Y.H. Kwark, R.A. Budd, P. Chiniwalla,

F.R. Libsch, J. Rosner, C.K. Tsang, C.S. Patel, J.D. Schaub, R. Dangel, F. Horst, B.J. Offrein, D. Kucharski, D. Guckenberger, S. Hegde, H. Nyikal, C.-K. Lin, A. Tandon, G.R. Trott, M. Nystrom, D.P. Bour, M.R.T. Tan, D.W. Dolf, IEEE J. Sel. Top. Quantum Electron. **12**, 1032 (2006)
3. T. Anan, in *Proc. International Symposium on VCSELs and Integrated Photonics*, E3 (2007)
4. R.H. Johnson, D.M. Kuchta, in *Conf. Laser and Electro-Optics*, CPDB2 (2008)
5. E.M. Strzelecka, G.D. Robinson, M.G. Peters, F.H. Peters, L.A. Coldren, Electron. Lett. **31**, 724 (1995)
6. Y.-C. Chang, C.S. Wang, L.A. Coldren, Electron. Lett. **42**, 1281 (2006)
7. Y.-C. Chang, C.S. Wang, L.A. Coldren, Electron. Lett. **43**, 396 (2007)
8. D.B. Young et al., IEEE J. Quantum Electron. **29**, 2013 (1993)
9. K.L. Lear, A. Mar, K.D. Choquette, S.P. Kil-coyne, R.P. Schneider Jr., K.M. Geib, Electron. Lett. **32**, 457 (1996)
10. Y.-C. Chang, C.S. Wang, L.A. Coldren, Electron. Lett. **43**, 1022 (2007)