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EXPERIMENTAL RESULTS OF SELECTION AND BIASING OF FET'S  
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Richard C. Jared and George W. Kilian

Lawrence Radiation Laboratory  
University of California  
Berkeley, California

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ABSTRACT

The experimental results are shown for the variation of resolution, gate voltage, and transconductance of a field-effect transistor by variation of the B plus voltage applied to the drain resistor. A short description of the selection technique of field-effect transistors for use in high-resolution systems, the preamplifier used, and several spectra showing the resolution obtained are presented.

## I. INTRODUCTION

The results an experimenter can obtain from lithium-drifted silicon or germanium detectors in low-energy electron-,  $\gamma$ -, or x-ray spectroscopy are limited by the resolution of the system. System resolution is controlled almost entirely by the resolution of the detector and the first amplifying device used in the preamplifier.

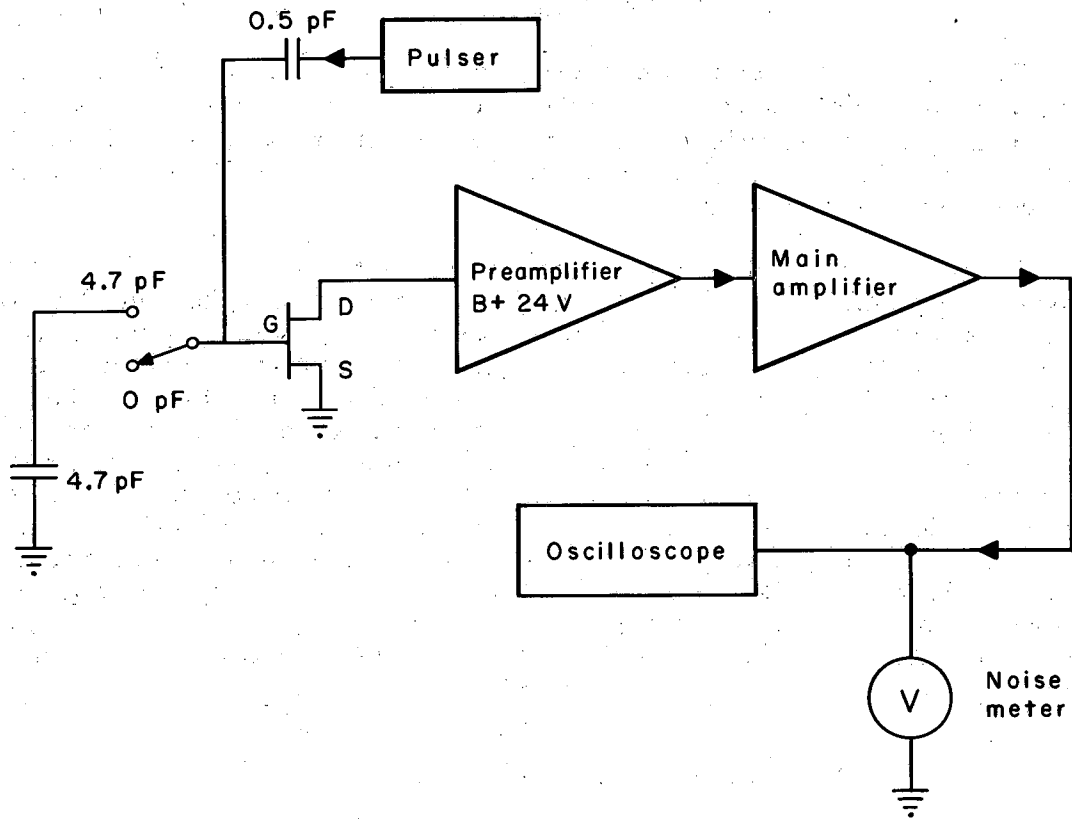
In attempting to obtain good resolution with detectors of 1 to 10 pF in the low-energy range 3 keV to 1 MeV, having rise times (60 nsec) suitable for crossover timing when a coincidence system is required, a procedure was developed for testing field-effect transistors (FET) at room temperature. This procedure allows the selection of FET's which have high probabilities of performing well when used in the amplifying system; it also incorporates the practice of varying the B plus voltage applied to the FET drain resistor in the preamplifier to set the gate bias at the optimum point. These procedures are described and the experimental results presented herein. A preamplifier of the type described by Elad and Nakamura<sup>1</sup> was first used in this study. However, it was found that faster rise times were required and a modified design was developed. A description of the modified design is given. A resolution of 0.56 keV (FWHM) for x rays of 8.03 keV input was obtained by using a selected 2N3823 FET.

## II. FET SELECTION PROCEDURE

The initial selection of an FET operated at room temperature with high Gm and low Cgd and Cds for use with detectors having a capacity of 1 to 10 pF has been reasonably successful. The FET was mounted in the circuit as shown in Fig. 1, and the following test procedure was used to find a figure of merit for the FET's.

The test procedure was as follows:

1. The pulser was set to a fixed output of approximately 20 millivolts.
2. An FET was placed in the circuit and the main amplifier adjusted for a signal output amplitude of 8 volts on the oscilloscope.
3. The pulser was disconnected.
4. The noise meter voltage was observed and recorded.
5. The FET input capacity switch was placed in the 4.7-picofarad position.
6. The pulser was reconnected.
7. The main amplifier was adjusted for an 8 volt output as observed on the oscilloscope.
8. The pulser was disconnected.
9. The noise was read and recorded.
10. The noise values from step 4 and step 9 were divided into the 8 volt value of the signal to obtain two signal-to-noise ratios shown in Table I.
11. The procedure was repeated for the next FET beginning at step number 2.



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Fig. 1. A test circuit for the selection of FET's.



The signal-to-noise ratio served well as an indicator of the quality of the FET's, as may be seen by the results listed in the fourth column of Table I. The ratio of signal to noise is a relative test, and shows only that one FET may be better than another if it has a larger signal-to-noise ratio. This test will not select all the high-quality FET's, but the majority may be found in this way with the expenditure of very little time and effort.

### III. EFFECT OF VARYING THE B PLUS VOLTAGE

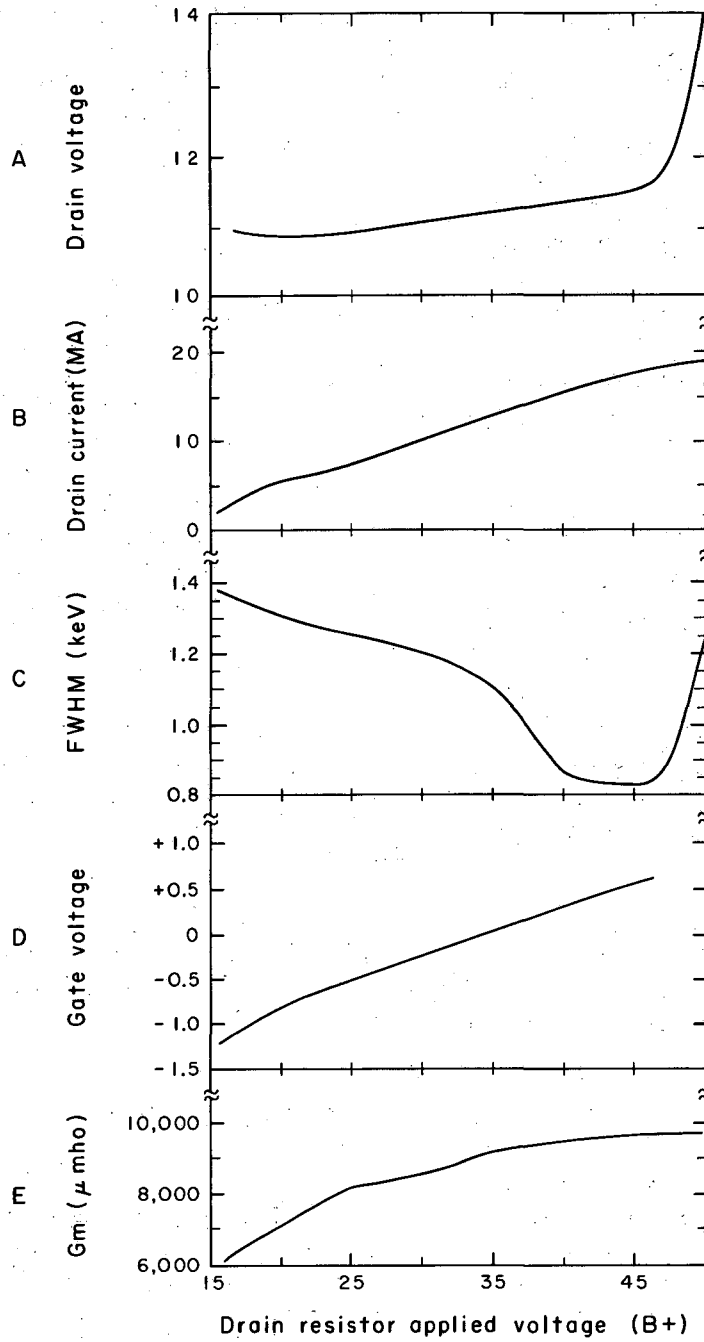
It was noted in using the selected FET's that the resolution of the system could be optimized by varying the B plus voltage applied to the drain resistor in the preamplifier with no gate resistor, as was shown by Elad and Nakamura.<sup>2</sup> The variations of the different parameters of the FET as a function of the B plus voltage applied to the drain resistor are shown in Figs. 2, 3, and 4. Figures 2 (a, b, and c) were constructed from measurements taken with a voltage-sensitive preamplifier having no gate resistor and a 6-pF Si(Li)-drifted detector connected in series with the gate lead (see Fig. 5). Figure 2 (d) was obtained by disconnecting the detector and replacing it with a bias supply which was adjusted to give the same values of  $V_D$  as shown in Fig. 2(a) for a given B plus voltage. The value of the bias was then measured and recorded as the gate voltage. The  $G_m$  values were calculated by using the corresponding values of  $V_D$ ,  $I_D$ , and  $V_G$ , given in Figs. 2(a), 2(b), and 2(d) respectively, together with a Tektronix curve tracer; they are plotted in Fig. 2(e). Figures 3 and 4 were constructed in the same way as Figs. 2(a) and 2(c), using (a) a Union Carbide UC 150 and (b) a TMC SP 17 to compare the conditions which exist in FET's made by other manufacturers.

The graphs show (as expected) that resolution improves as  $G_m$  increases. Maximum  $G_m$  occurs when the FET gate is biased at about 0.5 V positive. When the FET is biased at 0.5 V positive, the input capacitance is slightly larger than for negative bias.

### IV. MODIFIED PREAMPLIFIER

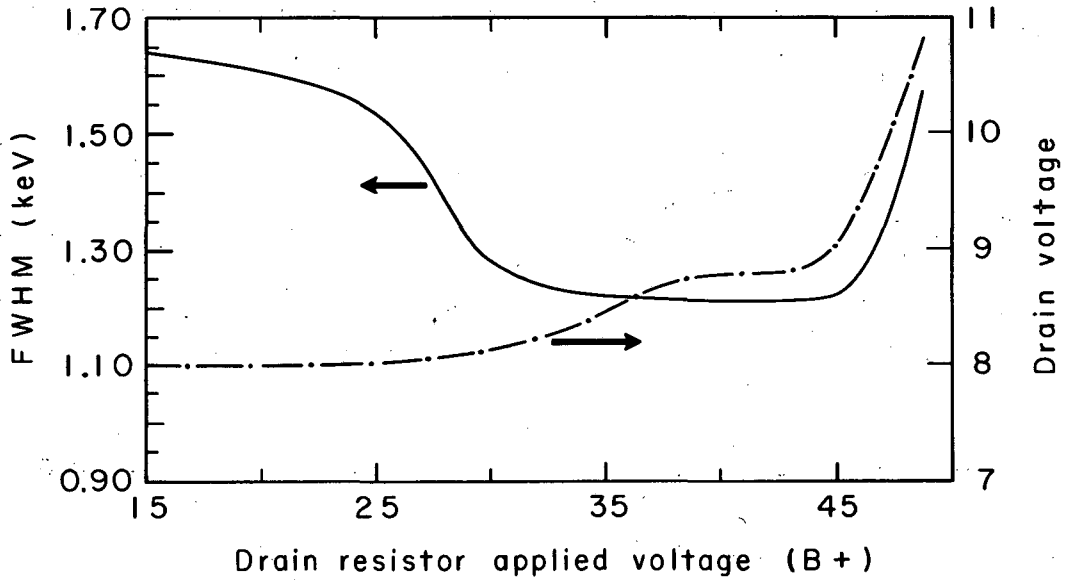
In Fig. 6 is shown a schematic sketch of the modified preamplifier used for coincidence systems. The  $10^8$ - $\Omega$  resistor,  $R_1$ , and the 0.1- $\mu$ F 5-kV capacitor,  $C_1$ , integrate the high voltage when it is turned on so that large changes in voltage do not appear at the gate of the FET.  $C_1$  also provided an ac ground for the detector.  $Q_1$  operates as a low impedance path ( $\approx 30$  ohms) for the changes in current at the FET drain. These changes in current are developed across  $R_D$ , and are passed on to the rest of the preamplifier through the emitter followers  $Q_2$  and  $Q_3$ . The presence of  $Q_1$  also minimizes the Miller effect in the FET, allowing the output amplitude of the first stage to be high enough to make the noise added by the second stage negligible. The differentiation is accomplished by the time constant of the parallel FET drain resistance and  $C_2$ .

Stability has not been a problem because the critical stages are cooled to liquid nitrogen temperature and maintained within a few degrees. In applications where gain stability was critical, the digital gain stabilizer of LaPierre and Nakamura<sup>3</sup> has been used satisfactorily. One should



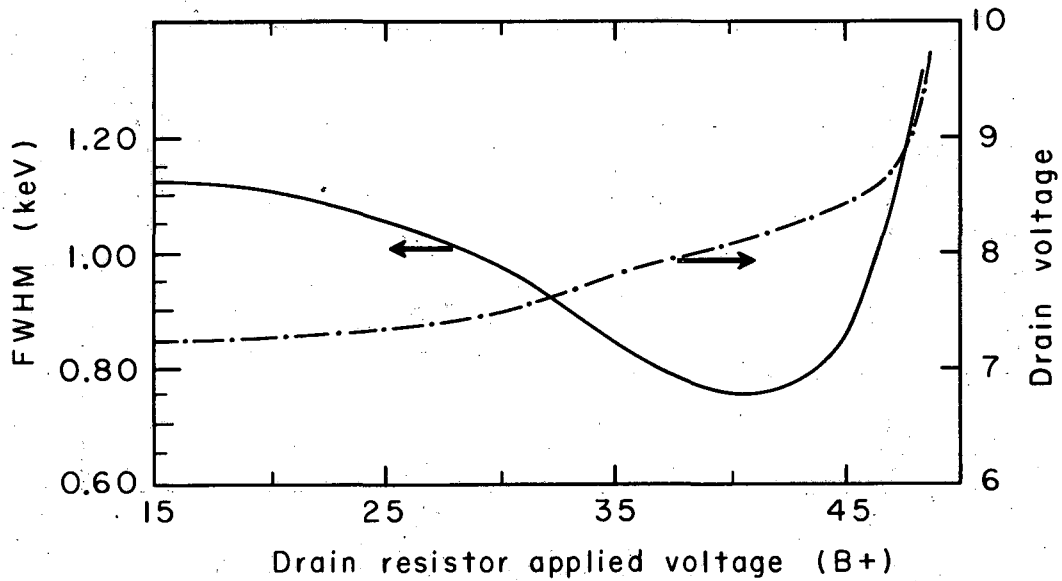
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Fig. 2. The variation of drain voltage, drain current, resolution, gate voltage, and Gm of a 2N3823 as a function of the drain resistor applied voltage (B plus) with a drain resistor at 1.9 k.



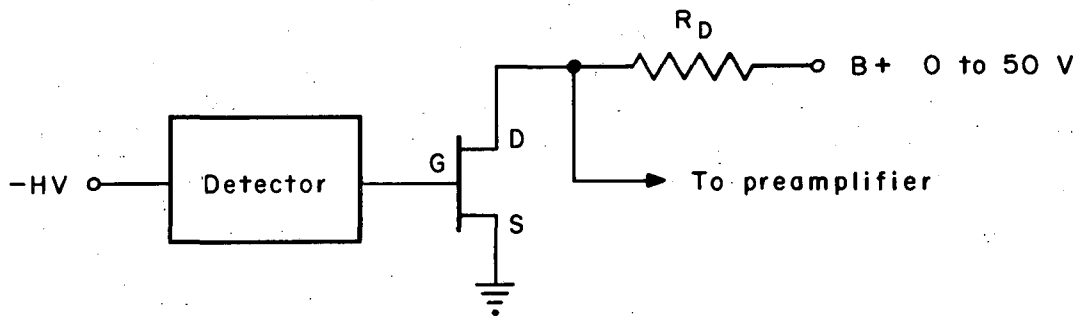
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Fig. 3. The variation of drain voltage and resolution versus B plus voltage of a Union Carbide UC 150 under the following conditions: Det. 1.2 pF Si(Li), Det. Bias 500 V,  $R_D = 1.7$  K, and resolution measured on the 14 keV  $N_P$  L x ray from  $\alpha$  decay of  $^{241}\text{Am}$ .



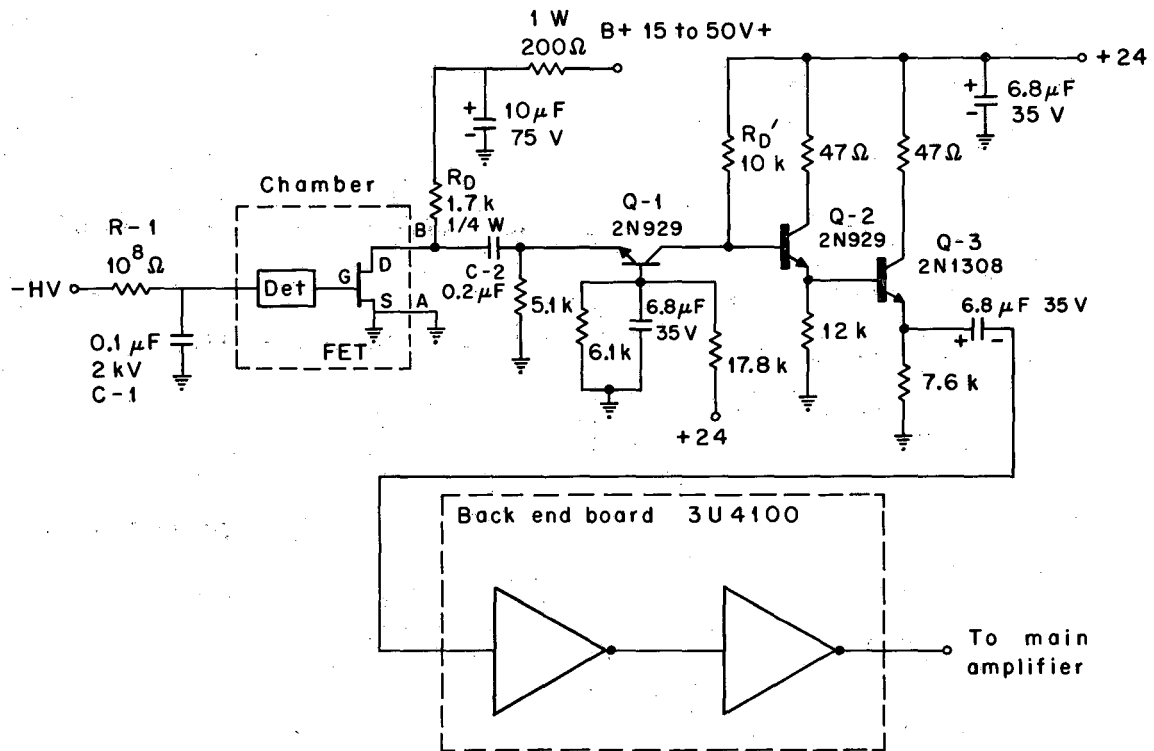
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Fig. 4. The variation of drain voltage and resolution versus B plus voltage of a Technical Measurement Corporation SP 19 under the following conditions: Det. 1.2 pF Si(Li), Det. Bias 500 V,  $R_D = 1.7$  K, and resolution measured on the 14 keV Np L x ray from  $\alpha$  decay of  $^{241}\text{Am}$ .



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Fig. 5. Detector-FET-Preamp connections.



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Fig. 6. Schematic of modified preamplifier (back end board from Goulding, Ref. 4).

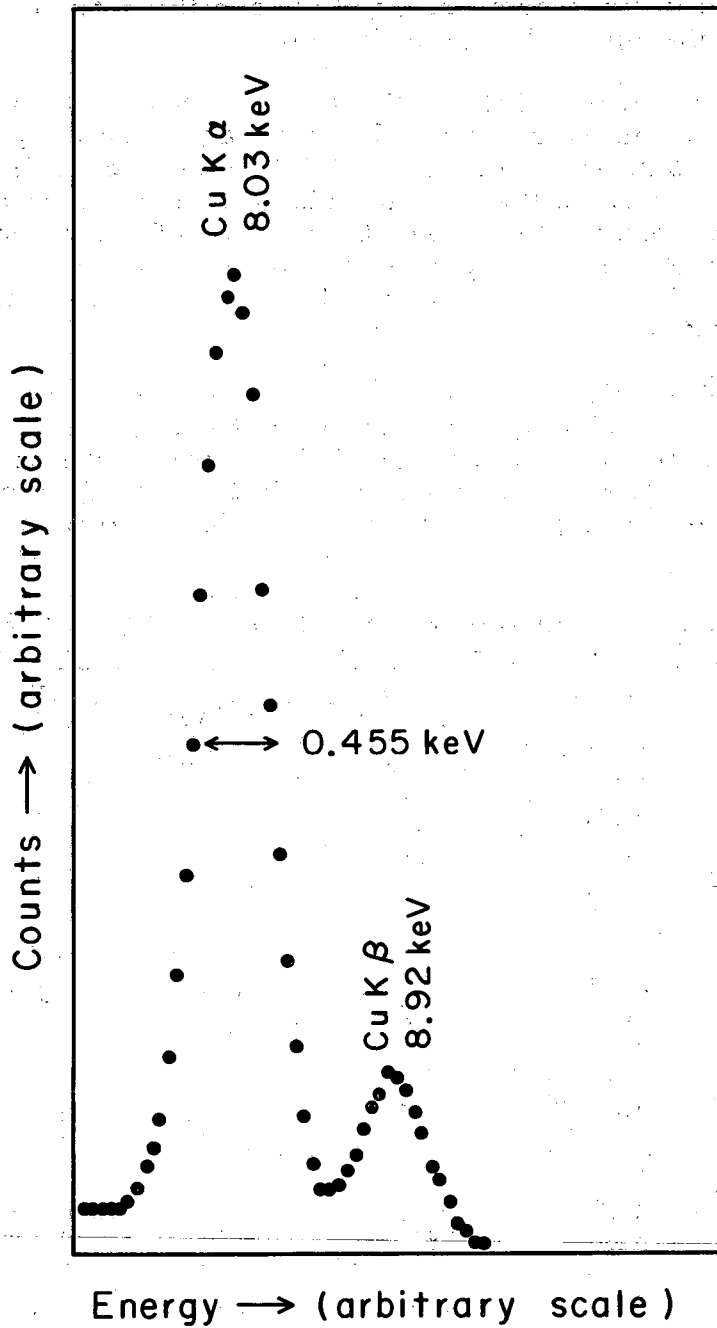
remember that voltage-sensitive preamplifiers are sensitive to high count rates as well as to varying count rates, in which the gate voltage varies because of accumulation of charge at the input.

A bistable condition of the FET has been observed when the above method of gate bias was used. If the drain voltage should equal the B plus voltage, the FET would stay in cutoff. This can be accomplished by putting too great a negative step on the detector bias during turn-on or by decreasing the B plus to a low voltage (less than 20 V). The FET may be returned to its normal operating condition by reducing the detector bias. This bistable state has been observed only during the turn-on and adjustment procedures, never during operation.

Figures 7 through 10 show the spectra obtained by use of all the above conditions. The amplifying system used in measuring these spectra consisted of a preamplifier followed by a 100- $\mu$ H choke terminated into 125 $\Omega$  at the amplifier input. The amplifier was used with 2- $\mu$ sec RC integration and differentiation, and the output was fed to a multichannel pulse-height analyzer.

Table I. Results of room-temperature tests on Type 2N3823 FET's.

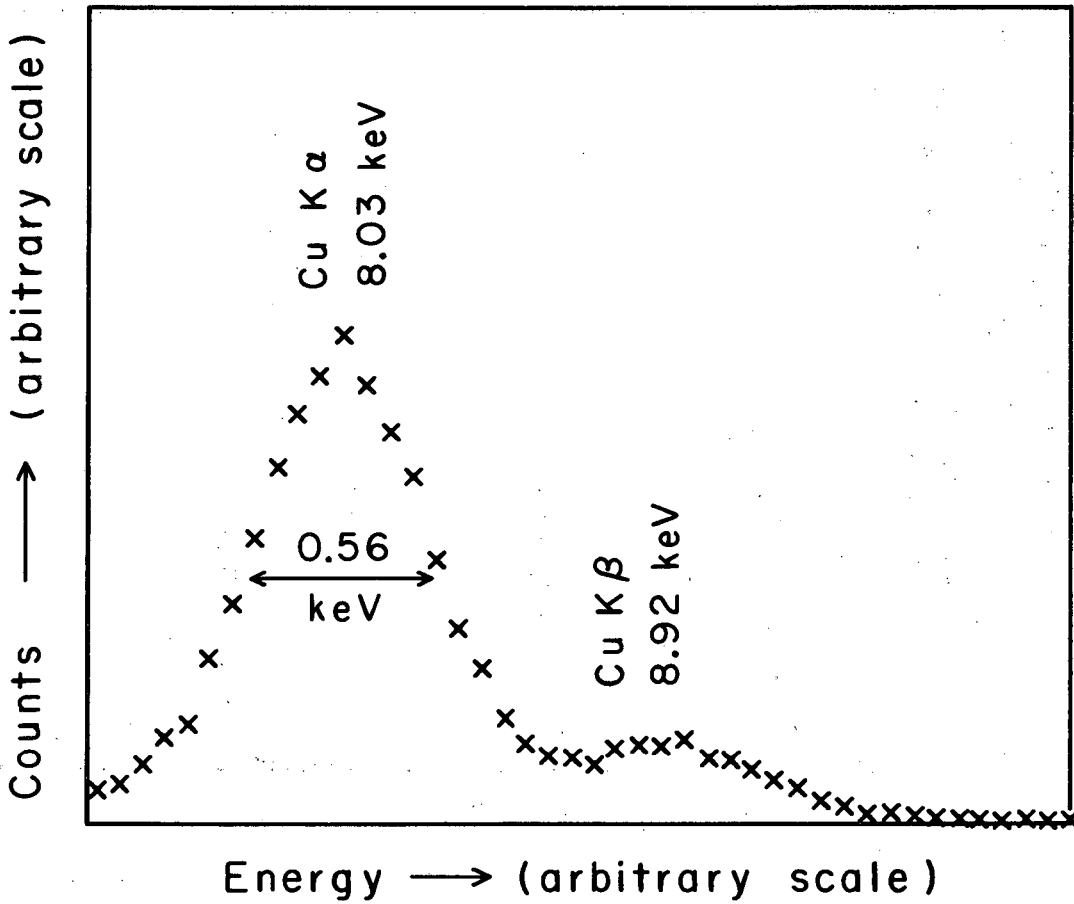
FET number	Signal-to-noise ratio		Result at LN temp if used		
	OpF	4.7 pF	B+ voltage	FWHM at 14 keV	Si(Li) drifted detector capacitance
1-	30.8	25.0			
2-	16.0	8.7			
3-	26.5	20.0	38V	1.10 keV	1PF
4-	30.8	25.8			
5-	30.8	26.6	45V	0.67 keV	3PF
6-	27.0	21.1			
7-	31.0	26.8	40V	0.69 keV 0.90 keV	3PF 6PF
8-	30.8	25.0			
9-	29.6	25.0			
10-	30.8	25.8	40V	0.83 keV	6PF
11-	27.6	22.8	30V	1.15 keV	1PF
12-	25.0	18.6			
13-	29.2	24.6			
14-	30.8	24.9	38V	0.96 keV	1PF
15-	30.9	25.0			
16-	30.9	25.6	45V	0.62 keV 0.85 keV	3 PF 6 PF



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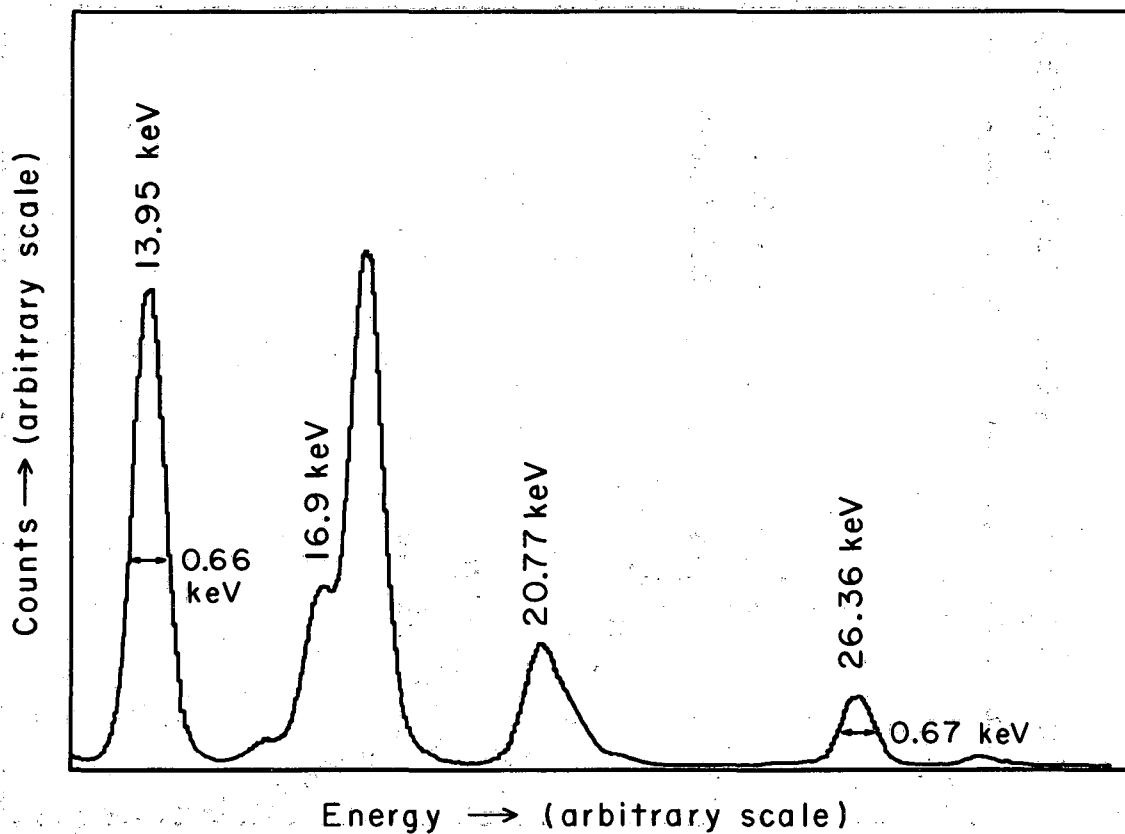
Fig. 7. Spectrum of copper x rays taken under the following conditions: B plus 42 V, FET TMC SP 19, Det. Bias 1 kV, Det. Cap. 1.2 pF, and Det. Si(Li).





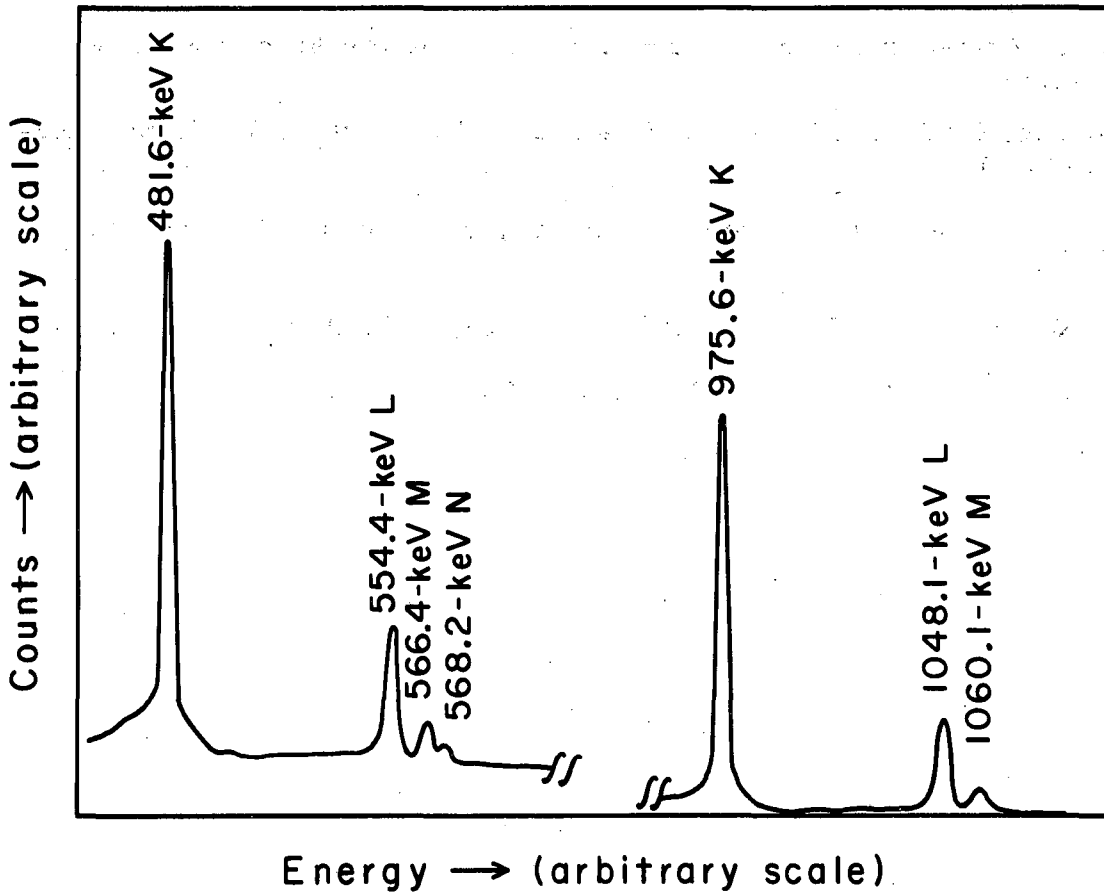
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Fig. 8. Spectrum of copper x rays taken under the following conditions: B plus 41 V, FET 2N3823, Det. Bias 1.6 kV, Preamp. Ref. 1, and Det. Ge(Li).



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Fig. 9. Spectrum of Np L x ray from  $^{241}\text{Am}$   $\alpha$  decay taken under the following conditions: B plus 45 V, FET 2N3823, Det. Bias. 1K, and cap. 3 pF, and Det. Si(Li).



XBL676-3321

Fig. 10. Spectrum of conversion electrons from decay of  $^{207}\text{Bi}$  taken under the following conditions: B plus 42 V, FET 2N3823, Det. Bias. 1 kV, Det. Cap. 6 pF, and Det. Si(Li).

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\*Work performed under auspices of the United States Atomic Energy Commission.

1. Emanuel Elad and Michiyuki Nakamura, IEEE Trans. Nucl. Sci. NS-14, 523 (1967).
  2. Emanuel Elad and Michiyuki Nakamura, Nucl. Instr. Methods 42, 315 (1966).
  3. M. Nakamura and R. LaPierre, Nucl. Instr. Methods 32, 277 (1965).
  4. F. Goulding, UCLRL Board Number 3U4100
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