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Los Angeles

Tunnel Field Effect Transistor

Based on Few-Layer Black Phosphorus

A dissertation submitted in partial satisfaction

of the requirements for the degree of Doctor of Philosophy

in Electrical and Computer Engineering

by

HUSSAMALDEEN SAIF QASEM

2019

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2019

ABSTRACT OF THE THESIS

Tunnel Field Effect Transistor

Based on Few-Layer Black Phosphorus

by

Hussamaldeen Saif Qasem

Doctor of Philosophy in Electrical and Computer Engineering

University of California, Los Angeles, 2019

Professor Kang Lung Wang, Chair

Aggressive scaling of Silicon based MOSFETs in the past decades have contributed immensely to the performance increase of modern electronics. However, at extreme scaling nodes, what was a solution is now the problem when power dissipation in its static and dynamic form have magnified and already reached the cooling limits. The static power dissipation is related to the short channel effect and can be limited by using other material systems that is immune to the short channel effect such as, two-dimensional semiconductors. The dynamic power dissipation can be reduced by allowing the frequency to increase without costing power dissipation. This can be a possible if the device is not designed on a thermionic injection which is limited by the subthreshold swing of 60 mV/dec, but rather on a tunneling transport mechanism which in theory can go far beyond the 60 mV/dec. It is however the low saturation ON current of the Si based T-FETs that hinder their progress. In our work, we combine the high mobility two-dimensional semi-conductive black phosphorus material, which has a 1) low effective mass value, 2) favorable band gap value, and 3) short electrostatic length and therefore immune to the short channel effect and, with the vital device

design of Tunnel-FETs. A combination of scrupulous black phosphorus FET device optimization process, e-beam lithography microalignment skill, and shadow deposition technique was used to realize our black phosphorus-based T-FET device. We have achieved high ON current values (1.4 uA/um), high ON/OFF ratio (10^5), high mobilities (300-400 $cm^2V^{-1}S^{-1}$), and low subthreshold swing (0 mV/dec). We have also marked these T-FET metrics against different temperatures, and also against the crystal orientation of the two-dimensional material. This research proof the applicability of Van der Wal materials in tunnel FET devices in particular, and low power electronics in general, and widen the path for greener, high-performance, and energy-efficient devices.

The thesis of Hussamaldeen Saif Qasem is approved.

Mark S Goorsky

Oscar M Stafsudd

Chee Wei Wong

Kang Lung Wang, Committee Chair

University of California, Los Angeles

2019

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1 Introduction

1.1 The current trend of the microelectronics and nanoelectronics industry

One of the last century's major technological development was the introduction of the transistor. Transistors are the elemental unit that can be designed and connected to form logic gates, which in turn constructs integrated circuits, and eventually composing processors that are employed in devices that are used every day, and everywhere by, and around, us. Currently, the number of transistors integrated in a 1 cm^2 microprocessors have reached 9 orders of magnitude. The technological breakthrough of transistors and integrated circuits in the semiconductor industry in the late 1940s and early 1950s, which granted their innovators the Nobel prize, were followed by continues effort to miniaturize the metal oxide field effect transistor (MOSFET). Miniaturization of MOSFET have allowed denser microchips, which was the central reason of the continues improvement of microchips performance, speed, and storage for the past decades. This miniaturization process has followed a temporal pattern that was predicted by Gordon Moore in his famous Moore's law, which states that the number of transistors per chip doubles every 18 months. However, in 2005, this trend has started to depart slowly from Moore's law. In that particular period, the ITRS nodes have started to have channel length of 65 nm and, with aggressive and innovative technology the node of 2008 was of 7 nm, ten times the size of an atom. The short channel effect (SCE) have started to present itself as the central challenge of the semiconductor industry and has the ability to render the silicon electronics industry absolute. When the channel becomes comparable to the depletion region, the electrostatic integrity of the MOSFET will be greatly compromised and will initiate short channel effect. The short channel effect is a packet of problems that initiate when the channel length reaches below a micron. Such problems are the drain induced barrier lowering (DIBL), the increase of the off state current, hot electron effects,

velocity saturation, band to band tunneling, threshold voltage shift, screening effect, and subthreshold slope degradation. Each of this problem will be explained in depth in the following chapters. Several ideas were undertaken by the semiconductor industry to counterattack the problem of short channel effect. Strained silicon, high-k materials, silicon on insulator (SOI), and FinFET structure were the most important ideas that pushed MOSFET into further miniaturization, as the regular planar MOSFET started to grow detrimental disadvantages. The International Technology Road for Semiconductors (ITRS) forecasts that additional new strain of materials and device geometries will be needed to effectively handle the issue of scaling for the next two decades. The ITRS main mandate is to evaluates the technology requirements for the next generation semiconductor devices and present them in a detailed report every two years. They present the detrimental scaling metric as the channel length, although from 2007, the connection between the node label (e.g. 7 nm) and the actual channel length, or pitch length have been totally divorced, and it is currently used as a commercial and marketing name for a slightly updated fabrication process. The performance, size, and density of transistors are, currently, not matched between foundries, the Intel 10 nm node is comparable to the 7 nm of foundries stand out as an example. Table 1 shows a glossary of metrics needed for future nodes as put by the ITRS.

In order to push for further miniaturizations and meet the future ITRS requirements (consistent with Moore's law), it is vital to scale down the channel length. Two-dimensional materials have the ability to effectively keep the electrostatic integrity of the gate bias on the channel due to its lower channel capacitance when compared to the geometrical oxide capacitance. This allows for a shorter electrostatic length, and finally, a tight control of the conduction band potential of the channel material. The figure of merit τ is an important metric for the MOSFET operation on the ON state, which is represented in the following equation

$$\tau = \frac{C_g V_{dd}}{I_{dd}} \qquad 1.1.1$$

C_g is the gate capacitance, while V_{dd} and I_{dd} are the drain voltage and current, respectively. As device engineers, this equation is not extremely helpful since it does not have terms that a device designer could use to fine-tune and enhance the MOSFET performance, hence we need to derive other proportionate equation from that figure of merit, to include terms that designer could use. The I_{dd} term can be replaced with the following long derived format

$$\mathrm{I_d} = Q_d v = W c_g (V_{GS} - V_{th})\, \mu \frac{dV}{dx} \qquad 1.1.2$$

Integrating both sides with the appropriate boundaries

$$\mathrm{I_d} = \frac{W\mu}{L} c_g \left[(V_{GS} - V_{th}) V_{DD} - \frac{1}{2} V_{DD}^2 \right] \qquad 1.1.3$$

The C_g term can be replaced with the following gate geometrical capacitance equation

$$C_g = W\, L\, c_g \qquad 1.1.4$$

Substituting in the figure of merit (τ) main equation, we arrive to the following equation

$$\tau = \frac{\mathrm{C_g V_{dd}}}{I_{\mathrm{dd}}} \propto \frac{L^2}{\mu} \frac{V_{dd}}{(V_{dd} - V_{th})^2} \qquad 1.1.5$$

It is apparent that in order to keep τ as minimum as possible, we need to minimize the channel length (L), and at the same time increase the mobility (μ) via choice of material for example.

1.2 Scaling and power consumption

As the power consumption rising with continues miniaturization, so is heat dissipation. The power consumption has already reached the limit of cooling capability of ($100\ \frac{W}{cm}^2$). Moreover, and as an example of the monumental amount of power consumption, every time an internet user hit a research button on Google, a 0.3 Watt-hour is consumed at the server centers as a result. If we multiply that with the number of daily search hits, we can estimate that the daily consumption is on the order of 200×10^6 watt, this is almost equivalent to half a nuclear power plant production. To have a better image of the scale of that consumption of that specific case and excluding everyday life consumption which will magnify the numbers to several orders of magnitudes, we have to know that the US have 60 nuclear power plant, and the world has 450. To reduce the power consumption and heat dissipation in large server centers, we need to reduce it on the elemental level, i.e. the level of transistor. In order to reduce the transistor's heat dissipation and power consumption, we need to look at the power consumption equation, and in light of that see which metrics needs to be modified.

The power consumption equation of a MOSFET consists of two terms, the first term represents the dynamic power consumption, i.e. power consumption in the ON state, while the second term represent the static power consumption, i.e. power consumption in the OFF state.

$$\mathrm{P} = \overbrace{V_{DD} I_{leak}}^{STATIC} + \underbrace{AC_{total}(V_{DD})^2 f}_{Dynamic} \qquad 1.2.1$$

It is apparent from the face value of the equation that reducing V_{DD} have an immediate positive effect on both terms of the power consumption equation. However, reducing the V_{DD} compromise the MOSFET performance significantly, as shown in figure 1.2-1. It is apparent that the switching speed between the ON state and the OFF state as a function of the applied gate is constant and

causing the I_{leak} to grow orders of magnitude higher. This transition rate of change between the ON state and OFF state in the subthreshold regime of the MOSFET is called the subthreshold swing (SS).

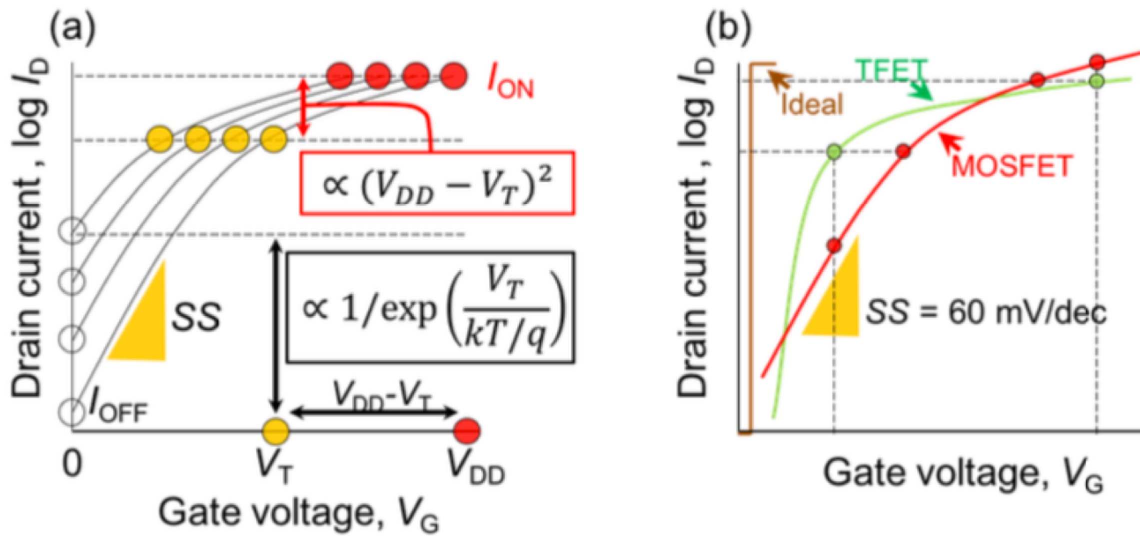


Figure 1.2-1 Transfer characteristics of a MOSFET switch showing an exponential increase in OFF current because of the thermionic limit of the subthreshold swing SS. Here the simultaneous reduction of the supply voltage V_{DD} and the threshold voltage, keeping the same ON current by keeping the (V_{DD}-V_T) constant. (b) Qualitative comparison of the MOSFET switch (red) with a TFET (green) which has a steep off-on transition and a lower I_{OFF}. At low V_G, because of the sub thermionic SS, the TFET offers a better performance and power reduction. At high V_G, the MOSFET switch becomes a better solution for higher performance thanks to the higher I_{ON}. [1]

At room temperature, the SS is thermionically set to need 60 mV in order to increase the current by a single order of magnitude. The equation of the subthreshold swing is as follow

$$SS = \left(\frac{\partial \log I_d}{\partial V_{gs}}\right)^{-1} = \ln 10 \left(\frac{\partial I_d}{\partial V_{gs}} \frac{1}{I_d}\right)^{-1} \quad 1.2.2$$

Upon decomposing the partial derivatives to the relation between potential profiles and gate potential, we can write the following

$$SS = \ln 10 \left(\frac{\partial I_d}{\partial \varphi_f} \frac{\partial \varphi_f}{\partial \varphi_g} \frac{\partial \varphi_g}{\partial V_g} \frac{1}{I_d}\right)^{-1} \quad 1.2.3$$

Assuming a perfect linear relationship between gate potential and conduction band profile, and assuming diminishing losses, we can notice that the terms between the brackets can be written as

$$\frac{\partial I_d}{\partial \varphi_f} = \frac{-I_d}{KT} \quad 1.2.4$$

$$\frac{\partial \varphi_f}{\partial \varphi_g} = 1 \quad 1.2.5$$

$$\frac{\partial \varphi_g}{\partial V_g} = -e \quad 1.2.6$$

We can rewrite the equation as the following

$$\mathrm{S} = \ln 10 \left(e \frac{I_d}{KT} \frac{1}{I_d} \right)^{-1} \quad 1.2.7$$

while the minimum subthreshold swing is at

$$S = \ln 10 \frac{KT}{e} = \frac{60\ mV}{dec} \quad 1.2.8$$

where K is the Boltzmann constant, T is the temperature (300K in this case), and e is the electron charge absolute value. It is concluded that as we reduce V_{DD} while keeping the dynamic current in the same level, we will have an exponential increase of the I_{leak}.

Having a low I_{leak} and high I_{dd} would require a steeper rate of change beyond the limit of $60\ mV/dec$. Steep-slope switches are a family of devices that offer a steeper change between the ON and OFF levels. From a device design point of view, they can permit further power scaling. Tunnel FETs (T-FET) and negative-capacitance FETs (NC-FET) are the most well-known devices of that category [2].

1.3 Tunnel field-effect transistors (T-FET) and scaling

Contrary to the MOSFET, where charge transport has a thermionic injection mechanism over the potential barrier controlled by the gate, tunnel field effect transistors (T-FETs) uses the tunneling phenomenon as a mechanism of charge transport[3–5]. Tunneling from a conduction band to a valance band through a tunneling barrier, or vice versa, is called band-to-band tunneling (BTBT). In his investigation of electric breakdown in dielectrics in 1934, C. Zener, was the first to witness the band-to-band tunneling in the strong reversed bias p-n junctions, i.e. simple diodes[6]. Upon applying that bias, the band structure bends, which leaves the valance band and conduction band of the opposite doped materials in strong proximity, from an energetic point of view. This explains the breakdown mechanism of the simple diode. Analogously, T-FET uses the same approach of initiating tunneling conduction through strongly biased P-I-N band profile. Figure shows the mechanism. A standard TFET is comprised of P-I-N band profile, with I of the P-I-N representing the intrinsic region in the middle. The detailed operation is as follow, upon the application of small gate bias, the conduction from the source valance band to the drain conduction band is held back by the intrinsic region gap, which is considered the OFF state of the T-FET. However, when a high gate voltage is applied, the valance band of the drain along with the conduction band of the source are brought to the same energetic level, charge carriers can tunnel from a band to the other seamlessly, hence, the ON state of the T-FET. Ideally, the switching between conduction states is extremely faster than the MOSFET, since the thermal tail of the injected electrons is suppressed by the upper portion of the valance band, while the OFF-state current is orders of magnitude suppressed when the fermi level is within the gap of the intrinsic region. This specific advantage will allow low subthreshold electronics to have values less than 60 mV/dec.

In 1978, The first theoretical proposal for that gated PIN structures was proposed by Quin et al[7]. It was not until 1992 where the first TFET was fabricated and experimented by Baba using III-V

material systems[8]. Reddick et al reported the first silicon based TFET, which was in 1995[9]. In the year 2000, Hansch et al, reported on vertically-structured silicon-based TFET, the fabrication was based on molecular beam epitaxy (MBE)[10]. 4 years later, an inventive work of TFET was then proposed by Ayden et al using silicon on insulator technology (SOI)[11]. In the last decade, several material systems have been experimented as TFET materials, such materials include but not limited to carbon, silicon-germanium (SiGe), and the composition of the three-five groups. These devices have been showing excellent performances in ON current, and the subthreshold swing (SS) in the lower supply voltage regime (less than 0.5V). However, disadvantages are also present in such devices including necessitating intense gate control, and their degraded transfer characteristics due to the presence of different types of defects (interface, or bulk) which enable the trap-assisted tunneling which ultimately worsen the OFF state current[12,13]. It is important to note that BTBT studies of two-dimensional materials have been conducted before. For example, Lan et al, have conducted a dual mode BTBT study of MoS_2 based on a hot electron transistor structure[14,15].

1.4 Two-dimensional materials and scaling

As for the interfacial and bulk defects, Van der Walls materials, i.e. two-dimensional material, offers a better alternative, since they have a smooth surface that is free from dangling bonds, and the diminishing thickness that does not allow much room for bulk-defects[16,17]. The Van der Walls materials are bonded, as the name suggest, by Van der Wall bonding force between layers of the material, hence the smooth surface and freeing of dangling bonds that affect the interface with the gate oxide. Additionally, two-dimensional materials offer a great solution to the power scaling issue since that their depletion capacitance is far smaller than the oxide capacitance, and allows for smaller electrostatic length λ, which means better control of the gate[18–23]Xiaodan . As a general rule of thumb, λ should be at least three times greater than the channel length (L). To derive a

formula for the electrostatic length we start with assuming the oxide capacitance C_{ox} to equal 10 times the depletion capacitance C_d.

$$C_{ox} = 10\ C_d \qquad 1.4.1$$

We will substitute for the capacitance terms of the following

$$C_d = \varepsilon_o \varepsilon_{ch} \frac{W d_{ch}}{L} \qquad 1.4.2$$

$$C_{ox} = \varepsilon_o \varepsilon_{ox} \frac{WL}{d_{ox}} \qquad 1.4.3$$

Where L is the channel length, $d_{ch}$is the thickness of the channel, d_{ox} is thickness of the gate oxide W is the width of the device, and $\varepsilon_{ch}\ and\ \varepsilon_{ox}$ is the permittivity, i.e. dielectric constant, of the channel and oxide, respectively. Upon substituting in equation 5

$$\varepsilon_o \varepsilon_{ox} \frac{W \cdot L}{d_{ox}} = 10 \times \varepsilon_o \varepsilon_{ch} \frac{W \cdot d_{ch}}{L} \qquad 1.4.4$$

Rearranging, and grouping the right terms into a single symbol λ

$$L^2 = 10 \times d_{ox} d_{ch} \frac{\varepsilon_{ch}}{\varepsilon_{ox}} = 10 \times \lambda^2 \qquad 1.4.5$$

λ, the electrostatic length, becomes

$$\lambda = \sqrt{\frac{\varepsilon_{ch}}{\varepsilon_{ox}} d_{ox} d_{ch}} = 3.16\ L \qquad 1.4.6$$

Hence the need to make

$$\lambda > 3L \qquad 1.4.7$$

Assuming we would like to achieve the node of L = 5 nm, for the conventional semiconductor industry such as Si, Ge, GaAs, we would need d_{ch} to be as following

Table 1.4-1 The thickness required per material to be immune from the short channel effect

Material	*ε*	*d*
Si	11.7	0.82 nm
Ge	12.9	0.74 nm
GaAs	16.2	0.58 nm

It would be unfathomable to have smooth surfaces for these covalently bonded materials with such single- or two-layer thicknesses. The mobility will be degraded so much that it will render the structure unusable. Hence we can see that Van der Walls materials, offer the combined package of necessary mobility, necessary thickness, and the scaled short channel lengths to achieve the node of $L = 5\ nm$.

Merging the TFET device ability to 1- achieve higher ON state current and 2- achieve higher switching speeds, i.e. steeper subthreshold swing (SS), with the properties of two-dimensional materials which offer 1- better electrostatic length, i.e. better gate control and lower OFF state current, and 2- diminishing interface and bulk traps could prove to be a successful merge, and that is the work of this thesis.

1.5 Dissertation outline

In Chapter 2, we will discuss the electrophysical properties of two-dimensional materials in general, and two-dimensional semiconductors in particular such transition metal dichalcogenides

(TMDCs) and elemental black phosphorus. A brief on the conventional and most recent approaches in controlled preparation and growth methods will be presented, especially efforts in growing single-crystalline wafer-scale two-dimensional semiconductors. A discussion on the rule of two-dimensional semiconductors in the micro- and nanoelectronics applications will follow. Finally, A holistic view of the most persistent challenges that faces two-dimensional electronics such as , electrical contacts, scattering of the charge carriers, and most-importantly, short channel effect in two-dimensional materials.

In Chapter 3, we will present the work of tunnel field effect transistor based on few layer black phosphorus as a channel material. We will present our work in achieving excellent FET performance as a gateway for the ultimate goal in achieving excellent TFET performance, given the extremely unstable nature of the material during fabrication. We will also discuss the device design and the fabrication procedures. Followingly, we will discuss the work done in terms of micro-alignment of the split gate structure, along with the shadow deposition process, in order to achieve minimal physical gap between the split gate structure. Finally, we will present the electronic characteristics of the device with a temperature dependence as well as crystal orientation dependence.

An all-in-all conclusion of the dissertation, along with a prospect of two-dimensional semiconductors research in nanoelectronics are presented in chapter 5

2 Two-Dimensional Semiconductors

2.1 Brief History of two-dimensional materials

Up to 2004, it was initially believed -theoretically- that single-layer, or few-layers, systems cannot exist due to the thermodynamic instability in these dimensions. This believe was proven inaccurate when layer isolation technique of Graphyne, a single layer of graphite, was discovered in 2004 by A. Geim and K. Novoselov[24]. This discovery has opened a new frontier of research in several fields, including material sciences, physics, electro-physics, chemistry, medicine, and biomedical research, with electro-physics and neotectonics having the lion share of published studies[25–30]. One of the main properties that made 2D materials a prime candidate for electronic application is their exotic electronic properties, such as extreme mobility of Graphene[31]. Since the isolation of Graphene, new Van der Wal materials have been discovered in similar manners and thousands of publications are being put forward on a yearly basis[32–34]. In this chapter we will discuss the electrophysical properties of two-dimensional materials in general, and two-dimensional semiconductors in particular such transition metal dichalcogenides (TMDCs) and elemental black phosphorus[22,23]. A brief on controlled preparation and growth methods will be presented, along with important electronics application. And finally, a holistic view of the most persistent challenges that faces two-dimensional electronics such as, electrical contacts, scattering of the charge carriers, and most-importantly, short channel effect in two-dimensional materials.

2.2 Electronic properties of two-dimensional materials

The two-dimensional material family, in the scope of electronics, ranges from zero band-gap materials, to low- and medium- bandgap materials, all the way to deep band gap materials. In other words, all the functional materials of 2D semi-metals, semiconductors, and insulators have been produced in the past decade[21,35–38]. On semi-metals, Graphene is the most famous material. It consists of SP-2 hybridized carbon atoms latticed in a hexagonal honeycomb structure with the

hybridization between the s-orbital and two p-orbitals results in a trigonal planar assembly with σ bonds being the essential bonding mechanism between atoms of carbon. Perhaps the most important electronic property of graphene is the possession of massless relativistic Dirac fermions, which is a result of the linear dispersion in the E-K diagram of graphene[37]. Graphene's carrier transport is intensely subjected to the interplay between different scattering mechanisms[39–41]. The significance of each scattering mechanism varies considerably across different substrate, thermal systems, and sample quality. Consequently, the room temperature mean-free-path of graphene changes from micrometers regime in suspended graphene and graphene on inert substrate [42], to low nanometers when situated on rough substrates such as SiO_2 [39]. The carrier mobility also varies considerably from ideal settings of 100,000 cm2 /V.s (suspended), and 25,000 cm2 /V.s (on h-BN substrate) to less than ideal settings of about 10,000 cm2 /V.s (on SiO_2 substrate) and 3000 cm2 /V.s to 6000 cm2 /V.s when synthesized by Cu-mediated chemical vapor deposition (CVD). Table 2.2.2 shows the discrepancies of graphene electronic metrics under different conditions.

Table 2.2-1 the discrepancies of graphene electronic metrics under different substrate, and growing conditions

	Suspended graphene	Graphene/h-BN	Graphene/$\boldsymbol{SiO_2}$	CVD Graphene
Mean free path	micrometers	micrometers	100s nm	<200 nm
mobility	>100,000	>25,000	>10,000	3000-6000

The 2D materials family goes far beyond graphene. The revolution included atomic crystals such as elemental black phosphorus[43], and h-BN[38], to transitional metal dichalcogenides compounds which take the form of MX2 such as MoS_2[22], $MoSe_2$, WS_2[44–47], WSe_2[48–50], and $NbSe_2$[51–53], to transition metal oxides composites such as MoO_3[32,54,55], $WLiCoO_2$[56,57], to members of the III-VI/V-VI Compounds such as Ga_2Se_3[58], In_2Se_3[59], Bi_2Se_3[60,61], and Bi_2Te_3[62–64]. As mentioned

earlier, this results to a tremendously resourceful system of two-dimensional materials whose constituents varies from metal, semi-metal, to semiconductors.

Moreover, topological insulating along with superconducting property could be harnessed by these 2D material systems. Figure 2.2 will show a brief representation of the most famous 2D materials along with their most important electrophysical properties.

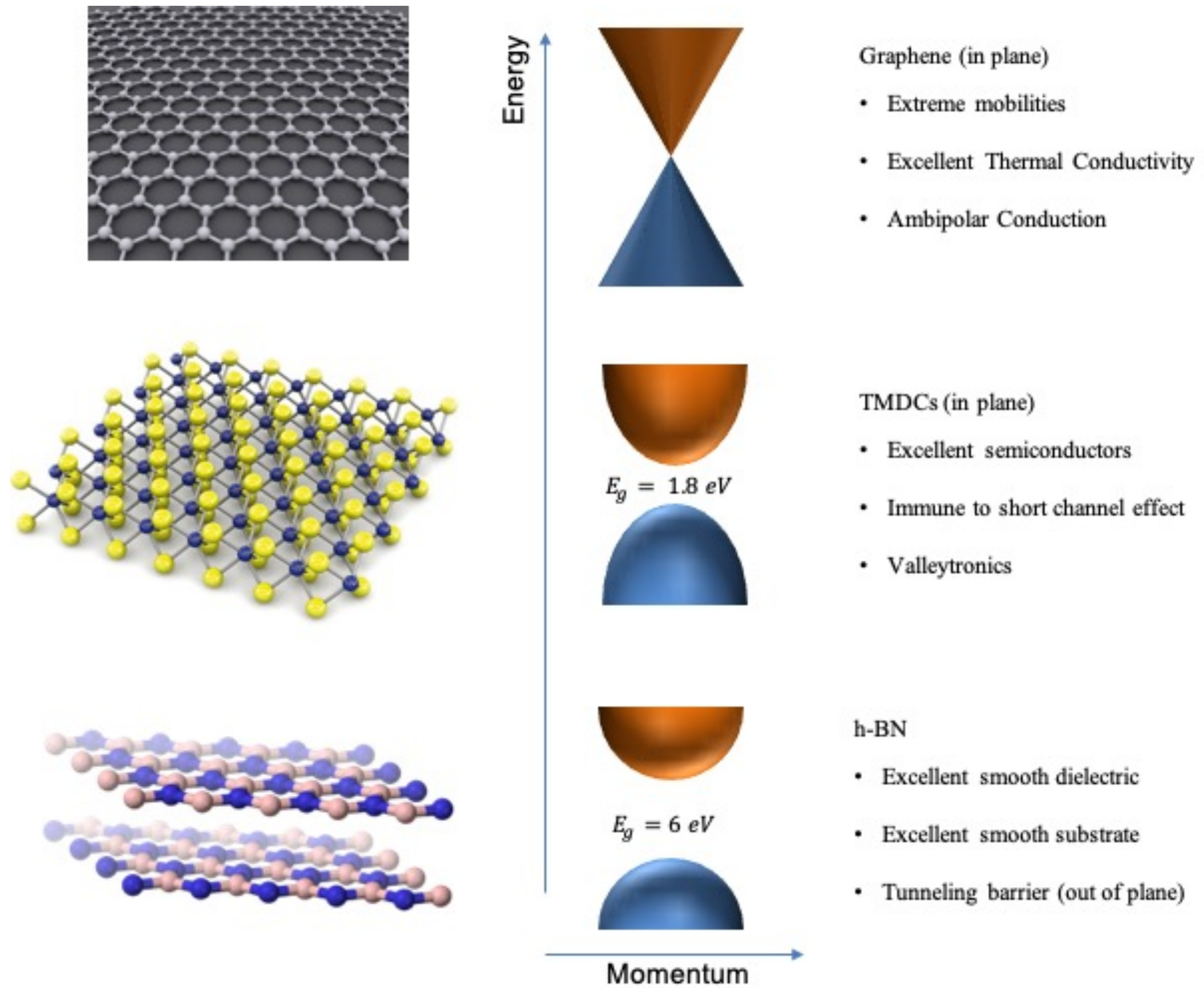


Figure -2.2-1 A brief representation of the most famous 2D materials along with their most important electrophysical properties

Table 2.2-2 Electrophysical properties of TMDCs

	$-S_2$	$-Se_2$	$-Te_2$
Mo	Semiconductor 1.8 eV	Semiconductor 1.5 eV	Semiconductor 1.1 eV
W	Semiconductor 2.1 eV	Semiconductor 1.7 eV	Semiconductor 1.1 eV
Ta	Metal Superconductors Charge Density wave	Metal Superconductors Charge Density wave	Metal
Nb	Metal Superconductors Charge Density wave	Metal Superconductors Charge Density wave	Metal

2.3 Preparation of two-dimensional materials

There are generally four methods of preparing two-dimensional materials, with each having its advantages and disadvantages as well. The first method is isolation through exfoliation using scotch tape[24], indeed this method was the first method that gave us the first single-layer graphene. The exfoliation through scotch tape proven to give us the best material quality. The record mobility that was registered in graphene was prepared by that method. This method is usually preferred for deep and advance physical studies that usually has minimalistic fabrication process and requires the utmost material quality. However, this process is laborious, time-consuming, and cannot result in large-scale flakes. Liquid-phase exfoliation through different kind of solvents and intercalations provides robust and relatively cheap method to produce large quantities of two-dimensional flake[65,66]. However, the quality of liquid-phase exfoliation is not suitable for electronics applications, and the flakes size produced is very small as well. High-temperature vapor-phase deposition techniques have shown to be a promising approach to produce large-scale, good-quality, and low-cost single layer materials. Techniques such as chemical vapor deposition (CVD),

metal-organic chemical vapor deposition (MOCVD), and physical vapor deposition (PVD) are all part of the vapor-phase deposition technique and have been tried in growing several types of 2d materials. Fig 2.3 shows atomic MoS_2 sample prepared in our lab with the Raman scan.

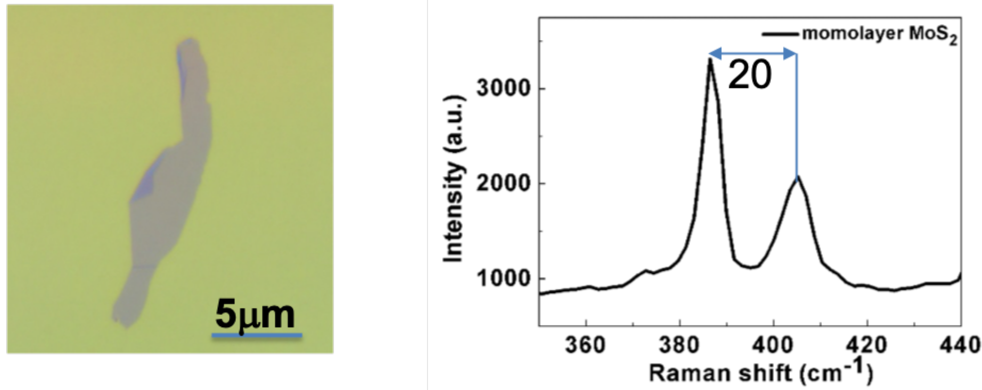


Figure 2.3-1 atomic MoS_2 sample prepared with its Raman scan

2.4 Central challenges in two-dimensional electronics

Figure 2.4-1 shows the most important challenges facing two-dimensional semiconductor electronics. We will be explaining each point in the following section

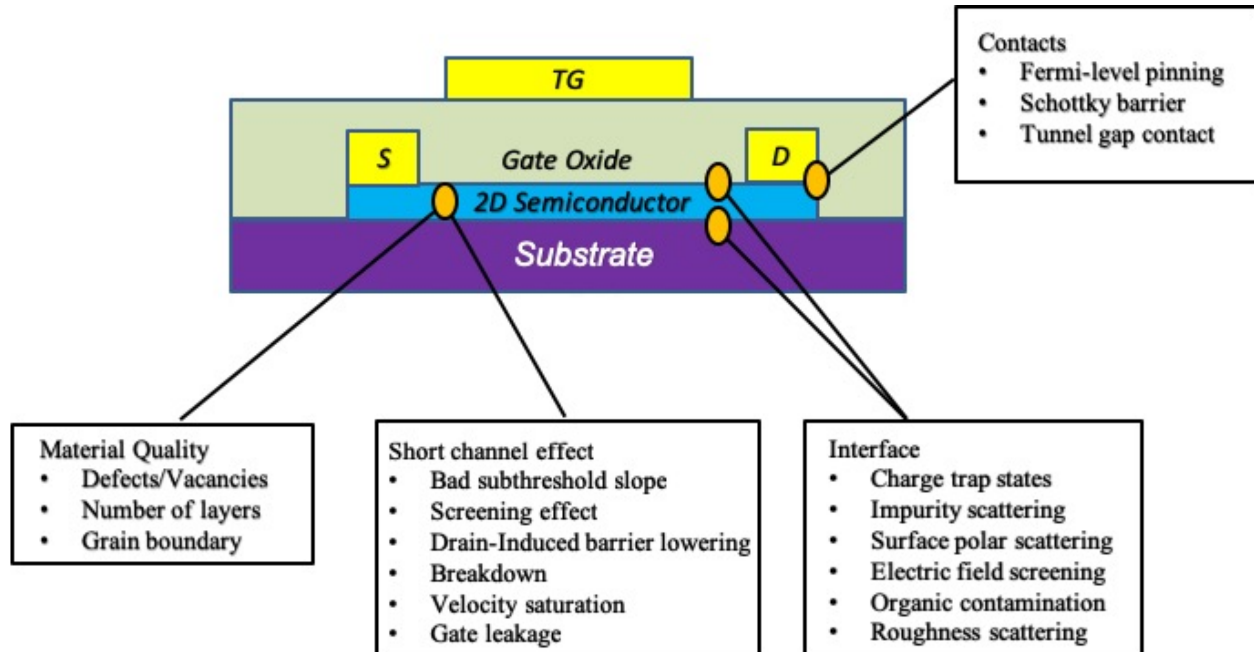


Figure 2.4-1 The most important challenges facing two-dimensional semiconductor FET realization

2.4.1 Electrical contacts

The electrical contacts are of great importance to 2d nanoelectronics for several importance reasons. The first reason is that the contact resistance becomes comparable to the channel resistance, or even dominate, in nanoelectronics due to their diminishing sizes.

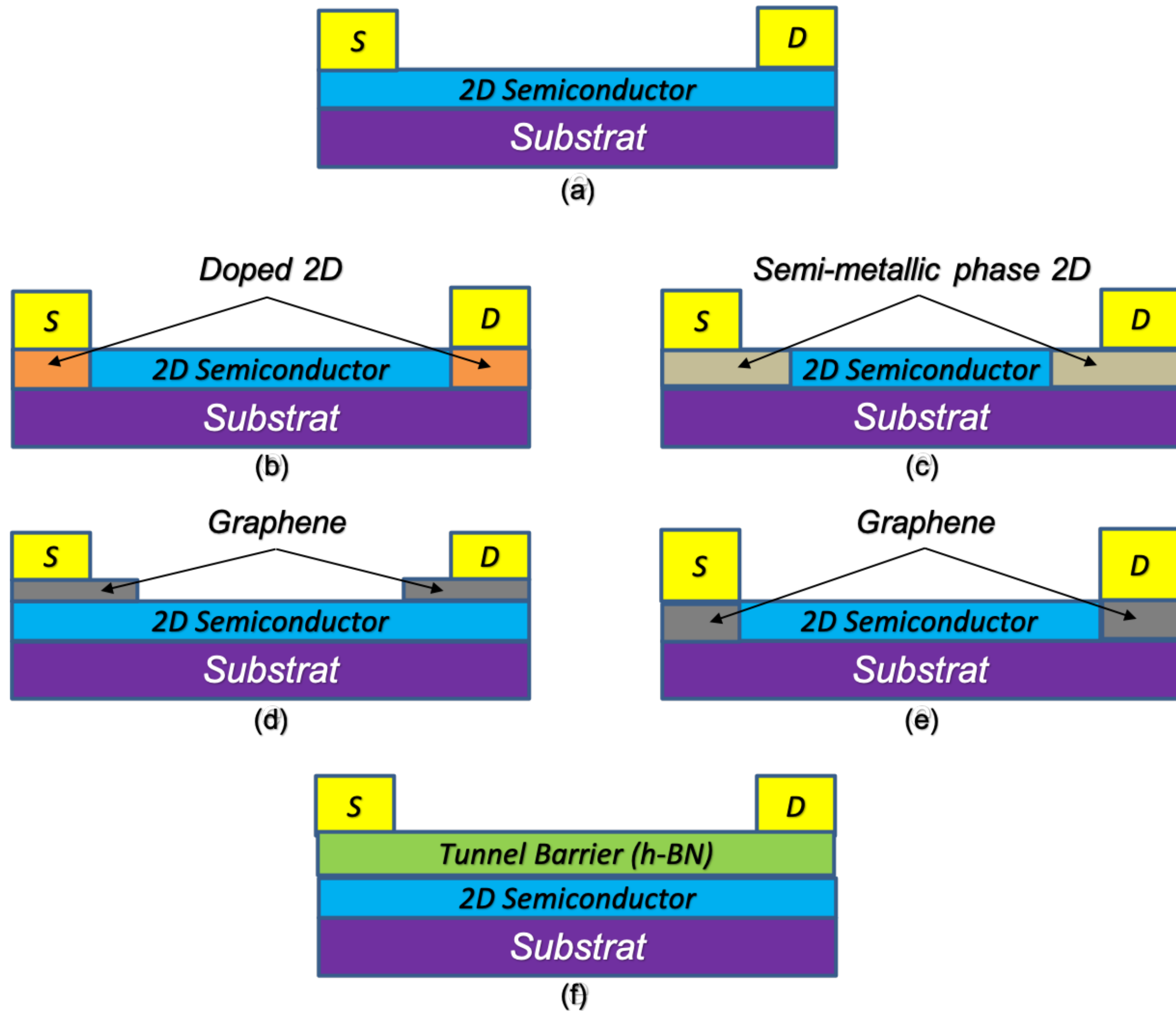


Figure 2.4-2 The most important techniques adopted in 2d nanoelectronics to decrease the contact resistance

The second reason being the inability of the 2d semiconductor surface to bond strongly to the contact material due to the Van der Walls nature of the surface, hence, an increase in contact resistance takes place. The third reason is the inability to adequately dope the material under the

contact, just like the regular practice in the silicon technology, due to the atomic thickness of the material, any attempt to dope the 2d materials conventionally will result in the damage of the flake. The forth reason is the small coverage area of contacts, which is needed because of the smallness of the flake and device, hence, this will increase the contact resistance. Figure 2.4-2 shows a cartoon of five most important techniques adopted in 2d nanoelectronics to decrease the contact resistance, a briefly on each method will be presented. The first method as shown in Figure 2.4-3 (a) is the tailoring of the work function of the metal contacts to align it favorably to the energy band of the channel. This has a direct effect of determining wither the contacts are ohmic or have a Schottky barrier behavior. The Schottky barrier height is characterized by the following equation

$$\varphi_{SB} = \varphi_M - \chi \qquad (2.4.1.1)$$

where $\varphi_{SB}$is the barrier height, $\varphi_M$is the metal work function, and χ is the electron affinity. Upon tailoring φ_M, a device could bae fabricated to diminish the barrier height[41,48,67–69]. Das et al have experimented 4 metals (Sc, Ti, Ni, Pd) contacts with MoS_2, and has proven that Sc, with its lower work function of 3.5 eV shows the best arrangement of contact-channel interface[70]. As figure 2.4-2 (b) shows, one can also use specific doping method to decrease the contact resistance. Javey et al have shown that upon doping WSe2 with potassium or NO2, a significant increase of the ON current takes place, however, this method is still under experiment to test its applicability to other 2D materials [48,68]. Figure 2.4-2 (c) shows the third approach, which is forming a 1T/2H metallic/semi-conductive phase to create a buffer area between the contact and the channel. Chowalla et al have employed this method on MoS_2 and have a record low contact resistance of 200 Ω [71]. Similar approach have been experimented on other 2D materials and have shown similar low contact resistance[71–73]. Figure 2.4-2 (d,e) show the employment of graphene as a top contact, and also as and edge contact. Graphene has a semi-metallic behavior and lacks any bandgap, at the same time, it can be electrically tuned to have a perfect alignment. Duan et al. have experimented

with top graphene contact and have demonstrated a barrier free contact in the low temperature regime of 1.9K [74]. However, one could see that the top contact has a Van der Wals band gap between the graphene and the 2D semiconductor, which might result in less than perfect contact. Hone et al, and Park et al, have studied this structure and realized a device with edge contact of graphene, one with exfoliated sample, and the other CVD grown sample, which have shown an ohmic contact both in the room temperature and liquid helium temperature[75,76]. The fifth approach, shown in figure 4(e), is to use h-BN tunneling barrier that covers the whole 2d semiconductor as a tunneling contact. Liao et al, have shown that upon using the method of the tunneling barrier contact on MoS_2, he could reduce the contact resistance from 5.1 KΩ to 1.8 KΩ[77].

2.4.2 Charge scattering

Perhaps the large difference between the theoretical prediction of electronic properties such as mobility and ON current, and the experimental measurements are due to the presence of charge scattering mechanisms. Charge trap states, impurity scattering, surface polar scattering, electric field screening, organic contamination, and roughness scattering are all part of the scattering mechanism effecting the mobility and current levels. Sandwiching the 2d semiconductors with h-BN, which has a very smooth surface yet insulating, is a suitable approach to reduce much of these scattering mechanism[78,79]. Cui et al have employed this method on MoS_2 and have achieved mobility of 1000 $cm^2V^{-1}s^{-1}$ at low temperature[75]. Xu et al have achieved a mobility of 6000 $cm^2V^{-1}s^{-1}$ when sandwiching an WSe2 2d material with h-BN[80]. In the low temperature regime, the phonon scattering is quenched, and the only apparent scattering are due to the interfacial scattering sources. Nevertheless, and even when trying to use very smooth substrates such as h-BN, the mobility values are not close to the experimented values. Hence, structural defects or vacancies on the two-dimensional semiconductors have a strong presence, polar scattering,

material roughness, and the contamination from the fabrication and transferring process cause a major degradation of electronic properties.

2.4.3 Short channel effect in two-dimensional semiconductors

Although two-dimensional semiconductors possess the ideal properties for further device scaling, e.g. short electrostatic length and smooth surface, yet the discrepancy between the theoretical predictions and experimental results still high. Nevertheless, certain short channel effects such as DIBL and GIDL have proven to be better in 2D materials[81,81–83]. For example, compared to the ultra-thin body silicon, MoS_2 shows 50% lower DIBL than UTB silicon[84]. A famous demonstration by Javey et al was done to demonstrate short channel MoS_2 device of 1 nm, which shows a DIBL of 290 mVV^{-1}, which in theory could go below 25 mVV^{-1} when certain dielectric material and thickness is deployed[85]. On the other hand, velocity saturation is another effect of short channel device that has a huge discrepancy between theoretical and experimental results in two-dimensional materials. In MoS_2, the velocity saturation could cut down the mobility to 50% of its 2 um channel long channel value[22,86]. In bP FETs, that reduction could compromise the mobility from 200 to 20 $cm^2V^{-1}s^{-1}$ [23,87].

3 Tunnel field-effect transistor based on black phosphorus

Pairing 2D materials, which proved to be relatively immune to the short channel effect, with the Tunnel-FET technology offers great potential to overcome the short channel effect barrier, minimize the energy consumption, and increase the switching speed in the device. This combination is the core of this dissertation. In this work, the 2D material of choice will be few-layers Black Phosphorus (5-10 nm/10-20 layers). A brief presentation of the properties on black Phosphorus two-dimensional semiconductor will be presented at the beginning before diving into the project outcomes.

3.1 Electronic and optoelectronic properties of black phosphorus

Unlike other semi conductive 2D materials, black Phosphorus has a direct bandgap that is in the optimum range for tunnel FET devices (0.1-0.4 eV), although it's band gap can be modulated to be 2 eV on the single layer regime, fig 3.1.1 (C, D). A single layer bP has a hexagonal honey comb lattice, with Van der Walls spacing of 5.3 angstroms, Fig 3.1.1 (A, B). Unlike graphene, this lattice structure has a puckered surface. In terms of effective mass, both charge carriers of electron and holes effective masses are strongly anisotropic. The lower effective mass is oriented toward the armchair direction of $m^{*}\approx 0.15\ m_0$, while the zigzag direction have a high effective mass of $m^{*} > 1\ m_0$ [16]. BP has a high carrier mobility of > 400 $cm^2V^{-1}s^{-1}$ at room temperature, large on current (~300 µA/µm), sizable on-off current ratio of 10^7, and to its extraordinary in-plane anisotropic electrical, optical and phonon properties[23,43,87–90]. Moreover, the material, by mere luck, bridges the electromagnetic spectrum between the zero-gap (far IR) Graphene and the wider bandgap (visible) transition metal dichalcogenides such as molybdenum disulfide (MoS_2) [91], figure 3.1.2 (A). The mobility VS on/off ratio values of b-P have shown a bridging behavior also between the

semi metallic semi-metallic graphene and the hard semiconductor counterparts such as TMDCs, figure 3.1.2(B).

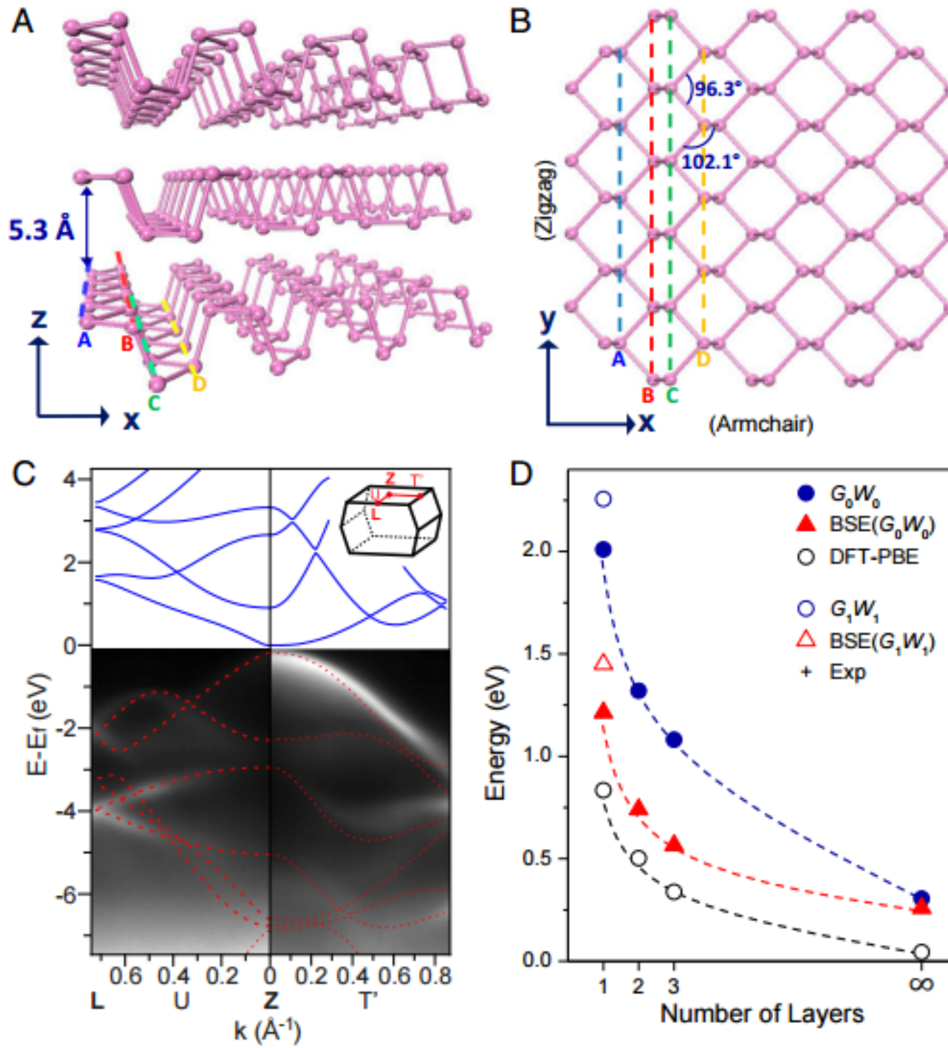


Figure 3.1-1 (A,B) The crystal structure of black phosphorus, (c) the bandstructure of black phosphorus using ARPAS, (D) modulation of black phosphorus layer number against band gap for diferent sources[91].

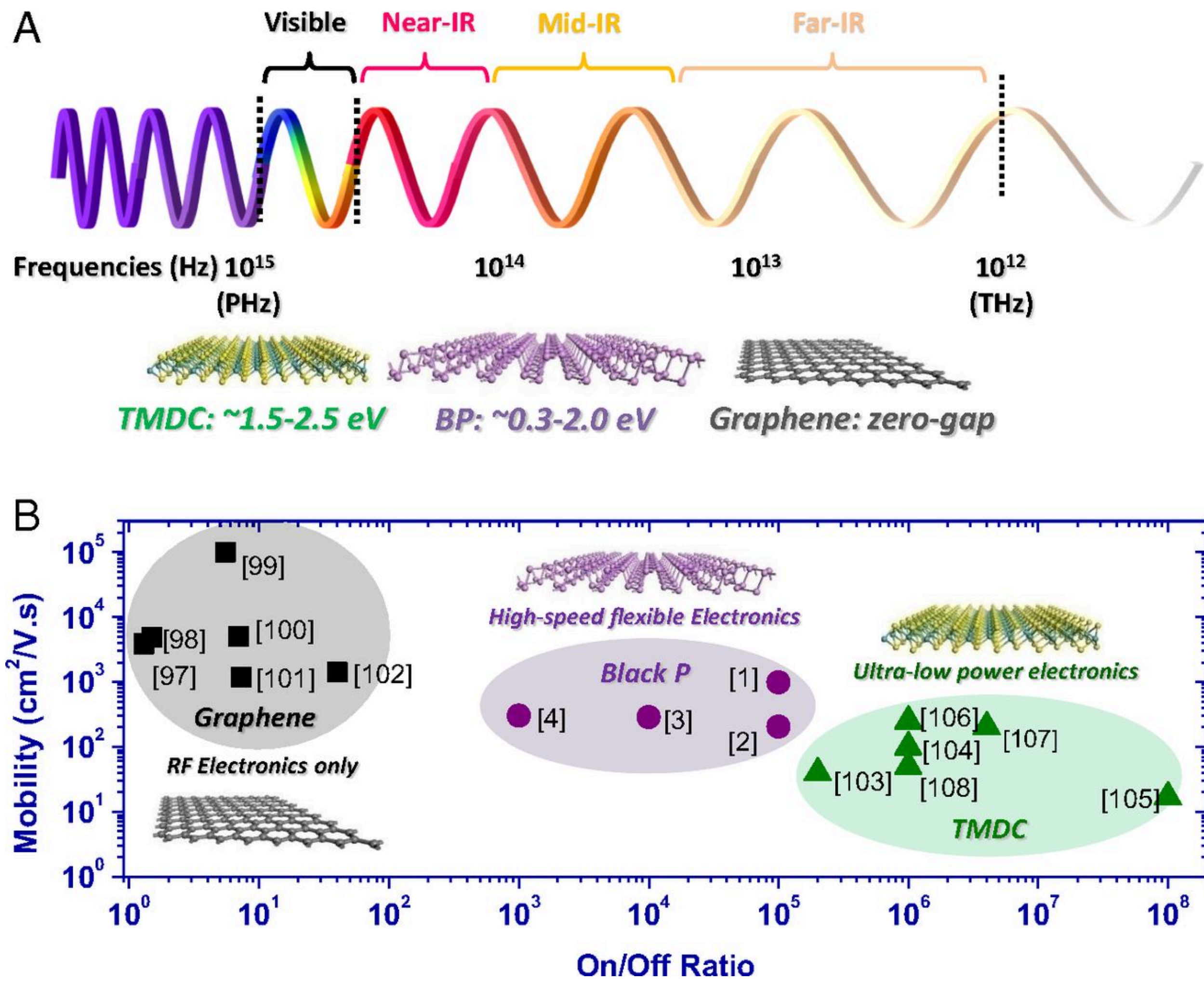


Figure 3.1-2 (A) The electromagnatic region that corrosponds to black phosphorus bandgap. (B) Mobility vs ON/OFF ratio of black phosphorus against Graphene and TMDCs [91].

The transport metrics of b-P field effect transistors depends on several design metrics, such as the channel length, the material thickness, the type of gate oxide, and fabrication procedures which could greatly affect the contamination of the device. A survey of the field effect transistor made by b-P is presented in Table 3.1.1 and Table 3.1.2. The literature survey looks at the hole mobility, electron mobility, and the ON/OFF ratio with regards to different material thicknesses and chanell length. The two tables are categorized by the type of gate oxide. The first table containing FET with SiO_2 gate oxide, while the other has different kind of high-k oxide, novel oxides, and 2d materials oxide.

Table 3.1-1 Survey of black phosphorus FET metrics in literature (Backgated with SiO2)

Thickness (nm)	Ch. L. (um)	Holes mobility	Electrons mobility	Holes ON/OFF	Electrons ON/OFF	Ref
10	1.6	984	-	10^5	-	[43]
5	1	286	-	10^4	-	[92]
-	2	116	-	10^5	10^3	[93]
4.8	-	214	1	10^4	-	[94]
5	1	205	-	10^5	-	[89]
-	-	300	-	10^3	10	[95]
-	-	100	0.5	10^3	-	[96]
18.7	3	170	-	10^2	10^2	[23]
5	0.69	155	0.18	10^4	-	[97]
-	-	25.9	-	10^4	-	[98]
-	-	200	27	-	-	[94]
1.6	0.45	35	12	600	-	[99]

The SiO_2 gated b-P had holes mobilities ranging from 20 to 1000, and ON/OFF ration ranging from 10^2 to 10^5. The large discrepancy is largely due difference in channel thickness, but most importantly, material and interface quality. Considering the extremely unstable nature of b-P, implementation of a fabrication technique that preserves the pure quality of 2D materials and averts various chemicals and fabrication processes from contaminating the 2D channels is of a great importance. This procedure can be prepared by constantly passivating the 2D semiconductor throughout fabrication and transfer steps, in that case, the passivation layer will take all the contamination from various fabrication steps instead of the functional material itself. The Second table included b-P FETs with different oxide materials. It is apparent that FETs with smooth

surfaced h-BN have provided the best mobility (1350) and ON/OFF ratio of (10^5). That is due to the fact that interfacial defect density, and different scattering mechanism have been kept to a minimum. Other gate oxide materials did not provide any edge over the SiO_2 FETs, let alone, h-BN sandwiched FETs.

Table 3.1-2 Survey of black phosphorus FET metrics in literature (Top gated with h-BN, high-k materials, and others)

2D Thickness (nm)	Ch. L. (um)	Gate Oxide	Holes mobility	Electrons mobility	Holes ON/OFF	Ref
8.5	0.3	HfO2	400	-	10^3	100
10.7	0.17	HfO2	44	-	10^3	101
11.5	1.5	Al2O3(T)	-	22	-	102
1.9	2	SiO_2 (B)/AL2O3(T)	172	38	2×10^4	103
8.9	-		49	-	7×10^3	104
6	0.5		95	-	10^4	105
15	2.7	Polymide(B)/Al2O3(T)	310	89	10^4	103
47	-	SiO_2 (B)/PMMA-MMA(T)	600	-	100	106
20	-	DEME-TFSI	190 (low k)	20 lowk	5×10^3	107
5	-	Ionic Liquid	510	-	-	108
-	-	H-BN	25	0.1	10^4	109
-	-	H-BN	400	-	10^5	110
8	-		1350	-	10^5	111
10	-		400	83	-	112

In terms of Hall mobility, a few-layer black phosphorus flake sandwiched between 2 h-bn substrates could yield very high mobilities. Long et al have fabricated a device structured as h-bn-bp-h-bn, and have measured room temperature Hall mobilities of 5200 $cm^2V^{-1}s^{-1}$, and can reach to up to 25,000 $cm^2V^{-1}s^{-1}$ in cryogenic temperatures[113], figure 3.1-4.

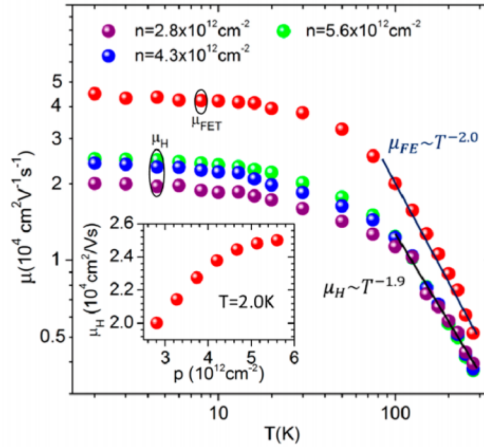


Figure 3.1-3 FE mobility (red) and Hall mobility at different carrier densities (green: 5.6; blue: 4.3; purple: 2.8 × 1012 cm−2) as a functions of temperature[113].

As mentioned earlier, the puckered orthorhombic structure of black phosphorus in the D_{2h} point group induce a strong anisotropy in effective mass between the zigzag and armchair direction, which accounts for 10 times differences between them, with the zigzag effective mass larger than that of the armchair direction[114,115]. This has consequences not only to anisotropy in electronic properties, but it extends to optical, and phononic properties. Other TMDCs also have this anisotropic phenomenon, such as rhenium disulfide (ReS_2) and rhenium diselenide ($ReSe_2$), which can open the door, when combined with black phosphorus, for a multi-variant combination of electronic, optoelectronic, and phonon engineered devices. Figure 3.1.3 shows cartoon the anisotropic plasmonic and thermoelectric behavior of black phosphorus.

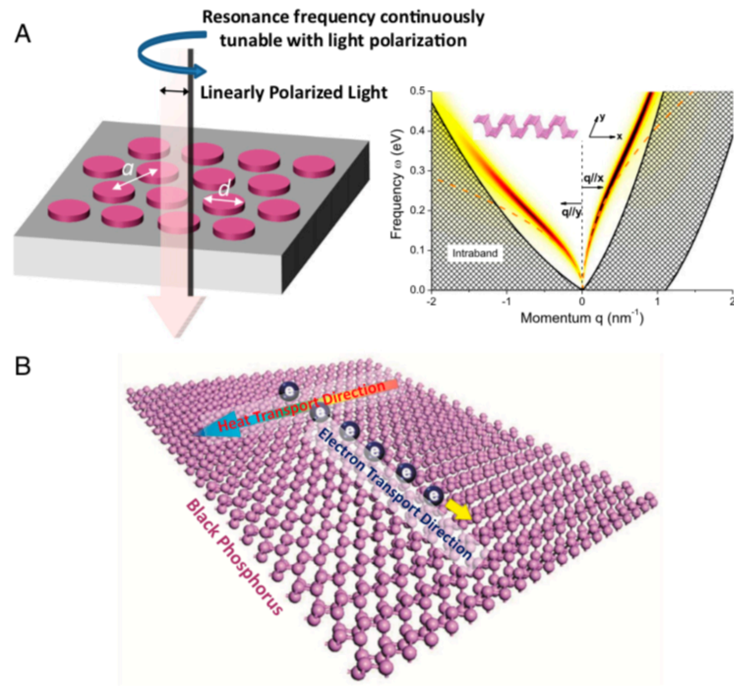


Figure 3.1-4 The anisotropic plasmonic and thermoelectric behavior of black phosphorus[91]

3.2 Project flow, and device design

The design of the device structure of our black phosphorus T-FET is shown on Figure 3.2.1. It consists of an exfoliated black phosphorus flake through scotch tape method, on top of an 〖SiO_2 oxide. A source and drain on top of the flake are followingly deposited, and an oxide layer on top, with a split gate structure on top of the top gate oxide. A detailed description of the fabrication process will be presented in the following sections.

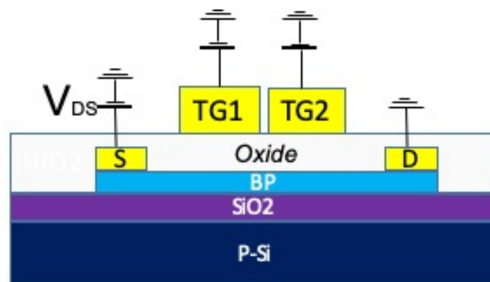


Figure 3.2-1 The design of the proposed black phosphorus TFET device

An important point to out is that since it is practically difficult to dope the channel area chemically, or physically, due to the atomic thickness of the material, we would have to dope it electrostatically, and we have chosen the split gate structure to insure minimum physical gap and increase probability of tunneling between the p and n regions. The split structure has been done on black phosphorus devices before by Buscema et al to fabricate a black phosphorus-based solar cell, using electrostatic pn junction through the top split gate structure[109], figure 3.2-2. However, the spacing between the gates was huge, and is easily judged unsuitable for tunneling devices. Hence a minimum physical gap is required, and a specific fabrication technique are required to go below 100 nm spacing. In general, in order for this device to operate as a black phosphorus-based T-FET, we would need to achieve three major milestones successfully. The first is to insure outstanding field effect transistors performance in terms of mobility, ON/OFF ratio, and subthreshold swing value. Since we have chosen the shadow deposition technique to form a minimal physical spacing between the split gate, a micro alignment of the e-beam lithography writing process is of a vital importance. It is important to form a single contact on the exact middle of the channel area to make it ready for shadow deposition technique. Which brings us to the third milestone, it is the process of shadow e-beam deposition to form a minimum physical gap without any shorting between the top split gate structure. Figure 3.2.3 shows a cartoon of the three main milestones regarding the fabrication of the black phosphorus T-FET device. A complete and detailed description of each process will be presented in the following sections.

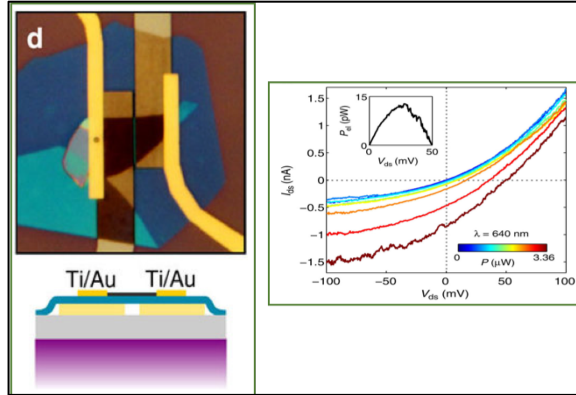


Figure 3.2-2 The split gate structure in this work done to enduce pn junction and followingly, set the device as a solar cell device[109]

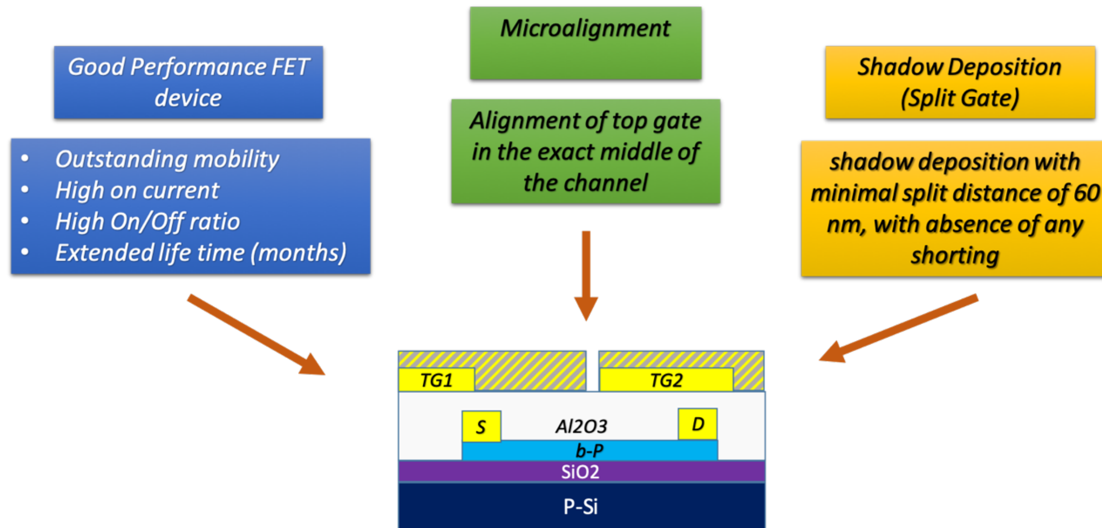


Figure 3.2-3 The three main milestones regarding the fabrication of our black phosphorus T-FET device

3.3 Fabrication technique

As mentioned earlier in Section 2.3, there are various types of two-dimensional material preparation techniques such as direct growth by chemical vapor deposition (CVD), liquid phase exfoliation, metal-organic chemical vapor deposition (MOCVD), and physical vapor deposition (PVD). In our work, we use the classic scotch tape mechanical exfoliation method to prepare few-layer black phosphorus samples, which as mentioned before provides great- quality flake of a size up to 10×10 μm. In a detailed description, a minor portion of smooth black phosphorus crystal

which was bought Smart Element of 99.998% purity was selected and attached to the high-grade blue wafers tape. Afterwards, the tape is folded around and pressed gently, followed by cleaving the closely pressed two sections, this will thin down the black phosphorus crystal by diffusing the Van der Waals force between the layers. A careful and gentle repeat of this folding and cleaving process for several times, between 10 and 20, will yield a large coverage area of thin black phosphorus flakes on the adhesive tape. Due to the strong interlayer force between black phosphorus layers, the puckered lattice structure of the flake, and the instable nature of black phosphorus under air, the mechanical exfoliation of bP is far more complicated than graphene or TMDCs. For that purpose, most of the exfoliation process is done diligently, and in a glove box environment which has a positive pressure of continuously flowing and purified Nitrogen. The adhesive tape with BP flake coverage on it is then flattened gently on a 300 nm SiO_2substrates which was grown on its native Si wafer and marked with numbers and shapes since its essential for e-beam lithography process, and also to put an address on the place of the desired flake for optical detection. The adhesive tape is then removed gently after being rubbed on for approximately 2 minutes. A significant amount of randomly shaped, and randomly sized black phosphorus flakes is transferred to the SiO_2 substrate as a result. A high-resolution optical microscope is then used to detect suitable few-layer black phosphors flakes. By suitable, we mean that the flake has to be thin-layered which is evident by the color of the flake under microscope, has to be relatively large of around 5X5 um to be suitable for our T-FET device, has to be uniform, and finally, it has to be clean. It is hard to perform thickness and quality characterization for every detected flake since they will have extensive air exposure that will damage the flake. Instead, we use our experience to rapidly detect few flakes under the microscope, and then, plan the physical characterization such as AFM and Raman on few chosen candidates. Figure 3.3.1 shows a typical exfoliated BP flake on 300 nm SiO_2/Si substrate, with an AFM scan. From the optical contrast

color, we can judge that this flake has approximately 10-30 layers, which corresponds to 15-20 nm, and is suitable for our electronic experimentation.

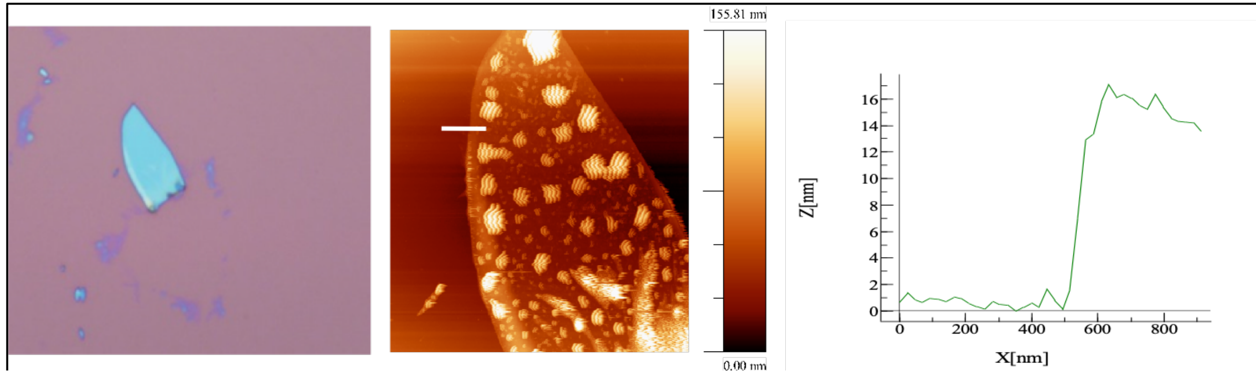
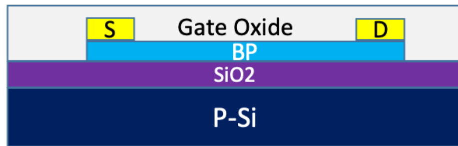


Figure 3.3-1 A typical exfoliated black phosphorus flake, along with AFM scan, and measurement of the flake thickness

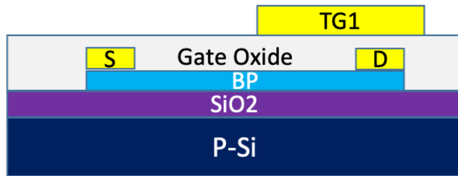
The small sizes of these flakes have required the fabrication to be done through electron beam lithography process. The working principle of e-beam lithography relies is on electron beam accelerated by voltages that range from 10 to 100 keV to bombard the photoresist coated on the sample. Nanofeatures can be prepared upon careful designing of the writing field pattern. It worth noting to mention that lithography technology has pushed the semiconductor industry to a new frontier of fabricating micro-, Nano-, low cost, and high-integration electronics. There several kinds of lithography techniques other than electron lithography. Photolithography being the most famous and widely used, and some other lesser famous ones, such as Ion-beam lithography, and X-ray lithography. Electron beam lithography strength is the low diffraction limit of less than 100 nm, which allows for higher accuracy. In our fabrication we will divide the fabrication round into three sections, Figure 3.3-2. The first fabrication section is to fabricate the core high performance FET device. Firstly, we spin coat our chip with a positive photoresist (PMMA 450) at 2000 RPM, the SiO_2 chip coated has all the exfoliated bP flakes that we intend to experiment on, Figure 3.3.3 (a-d). A positive photoresist will develop the areas where electron bombardment from e-beam takes place, which is in contrast to negative photoresist, where bombarded areas are polymerized

and undeveloped, while bombarded area are the developed areas. Since the PMMA has some solvent in it, it is important to bake the chip for 2 minutes under 180° C.



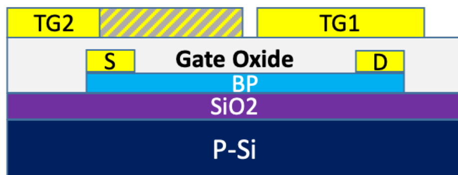
First Fabrication Section

- Exfoliation and transfer of bP on SiO2
- 1st layer Ebeam lithography to write source and drain
- Gate oxide deposition using ALD



Second Fabrication Section

- Micro-alignment of one of a split gate contact in the exact middle of the channel
- E-beam lithography, and E-beam metal deposition



Third Fabrication Section

- Angle resolved shadow deposition, gap < 100nm
- E-beam lithography, and E-beam metal deposition
- Encapsulation

Figure 3.3-2 The three sequential sections of our fabrication process

However, in our experiment, we use black phosphorus which is highly unstable and can oxidize easily under air and moisture. The baking of our sample under 180° C will accelerate this oxidation process, hence, we have customized the standard operation to make the baking temperature at 100° C for 8 minutes. We then spin coat a second layer of photoresist of different concentration (PMMA 950) at 4000 RPM, another baking session of 100° C for 8 minutes will take place. Followingly, the standard EBL procedure is conducted. The EBL process is performed in a converted SEM instrument JOEL JSM 6610, figure 3.3.4 (a). The exposed pattern is designed by Nanometer Pattern Generation System (NPGS) and designCAD. The vacuum chamber under which the e-beam operation takes place is at (~10^{-6} mbar). After accurately aligning the substrate to address the flake, we start writing the pattern. Afterwards development of the sample is done by submerging the sample in an MIBK:IPA 3:1 mixture solution to remove the developed PMMA Figure 3.3.3 (e). E-beam metal deposition (CHA industries, figure 3.3.4 (b)) is performed next to deposit the

contacts, usually Cr/Au of 2nm/50nm, Figure 3.3.3 (f). The result is a sample that is fully covered by Cr/Au, which nictitate a submerge in Acetone to lift off that layers, and only keep the contacts, Figure 3.3.3 (g). The final process of the core device fabrication can take two routes, the first being encapsulating the device, and perform device measurement through the back-gate oxide of 〖SiO_2. The second route, which we use in our experiment, is to use atomic layer deposition (ALD Fiji figure 3.3.4 (c)) to deposit oxide composites as a top gate oxide such as Al2O3, Hf2O3, and others, Figure 3.3.3 (h).

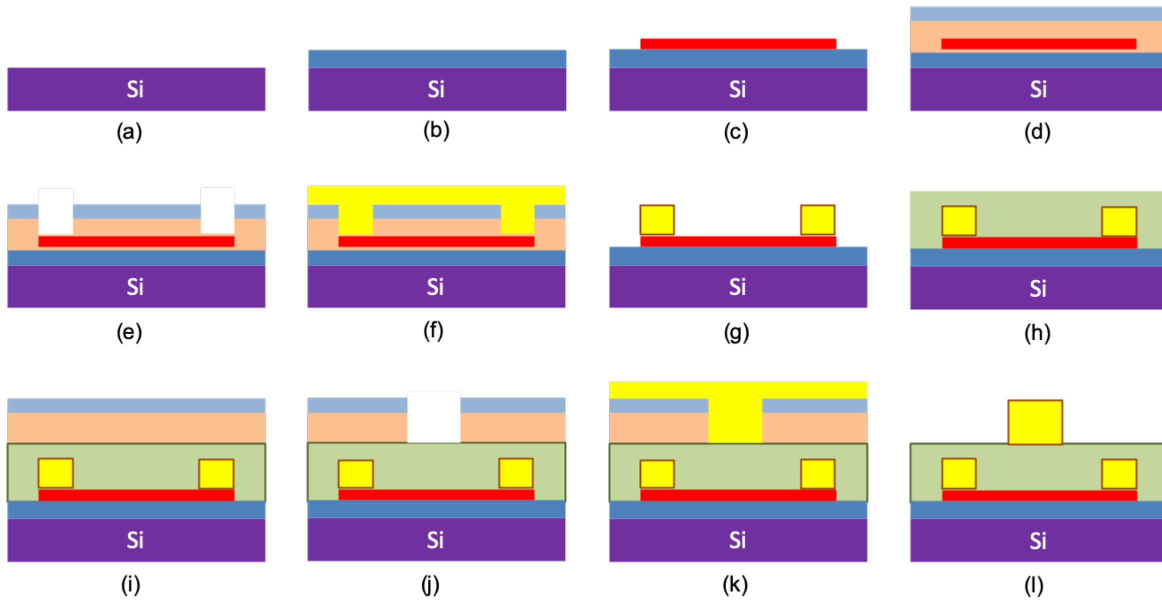


Figure 3.3-3 The fabrication steps of the core FET device, (a) prepare the wafer. (b) grwo the insulating substrate. (c) exfoliate bp crystal. (d) spin coat photoresist. (e) e-beam lithography. (f) e-beam metal deposition. (g) lift-off. (h) top oxide layer. (i) spin coat photoresist. (j) e-beam lithography. (k) metal deposition. (l) lift-off.

It is worth mentioning that we apply a seed layer of 1 nm through e-beam metal deposition to insure better interface when applying ALD. For example, if we intend to apply Al2O3 in the ALD, then the seed layer of the e-beam metal deposition would be Aluminum. Another round of photoresist, EBL writing, developing, E-beam metal deposition, and lift-off is done to write the top gate Au contact, figure 3.3.3 (i-k). A flow chart of the process is presented in figure 3.3.5. Figure 3.3.6 show a finalized back gated FET (a), and a hall-bar structured device (b).

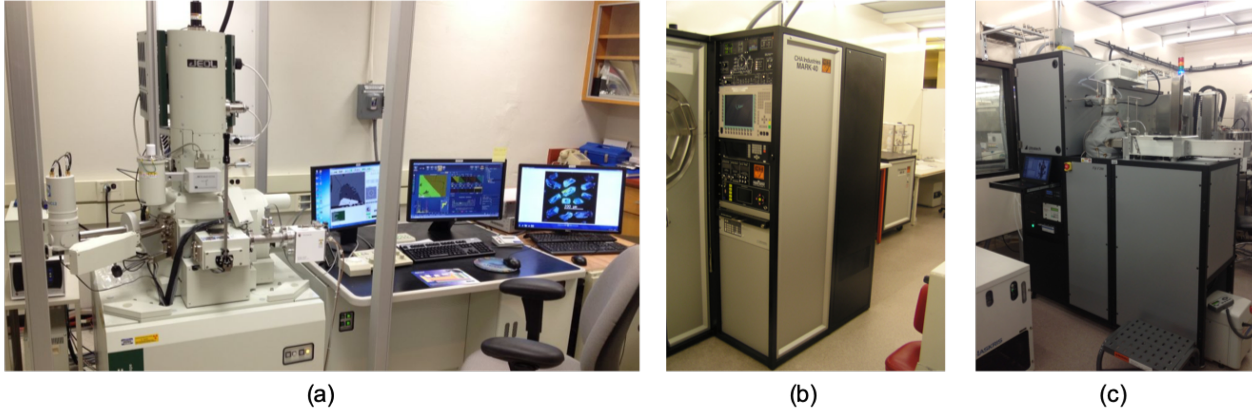


Figure 3.3-4 (a) JOEL systems for electron beam lithography. (b) E-beam metal deposition machine, CHA industries. (c) Fiji ALD deposition system.

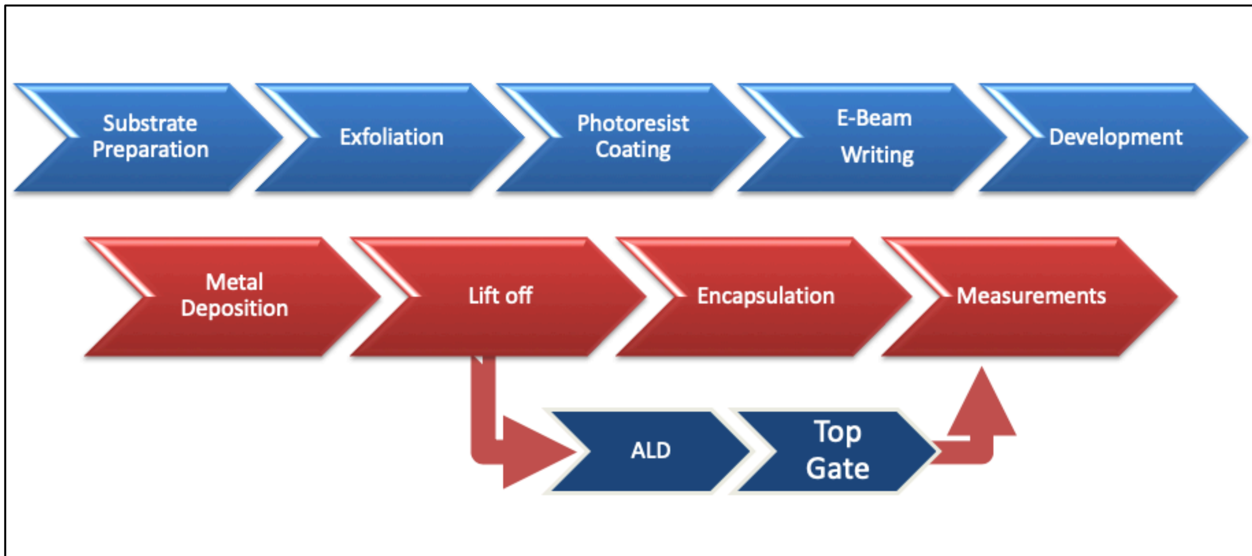


Figure 3.3-5 A flow chart of the fabrication process

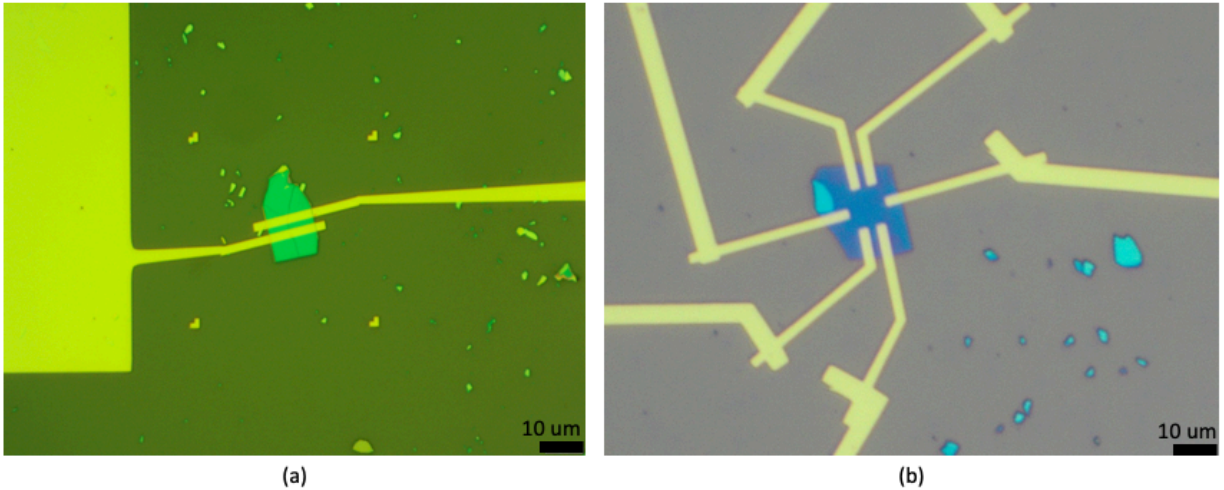


Figure 3.3-6 (a) a finalized back gated FET, and (b) hall-bar structured device..

The second fabrication section is a preparation for the third section of shadow deposition. In order to insure proper shadow deposition in the exact middle of the channel which will result in the desired split gate structure with a minimal physical gap, a top contact is micro-aligned and patterned through e-beam lithography. The micro-alignment requires several layers of markers patterning, the first set of marks will be good for the core FET device fabrication, however, the error of alignment in the writing field of the first layer is on the order of 1 um. Meaning the written pattern could be shifted one way or the other by 1 um without compromising the device integrity. If we use the same writing field size to write the top contact in the middle and considering that the channel length is less than 2 um it is impossible to write it exactly in the middle. A smaller writing field on the e-beam lithography is required through stitching windows of markers that spans from 200x200 um all the way to 20x20 um writing field size. Accompanied with that, a precise recipe of dosage, and exposure time have to be optimized in order to insure sharp exposure. Over-development is a serious problem in our fabrication, specially that we are dealing with very small features. Not only the dosage, current, accelerating voltage, and exposure time has to be optimized, but also an optimization of the photoresist type, thickness, and viscosity has to be absolutely fine-

tuned. In addition, the development solution could etch extra region around the developed area, although it is minimal, but with extremely fine and small features, the development time in the MIBK:IPA solution need also to be optimized. Figure 3.3.7 shows a small feature structure with the university logo attached with the Center of Excellence of Green Nanotechnology logo that we made with features of almost 300 nm including the design picture, the developed sample, and the metalized sample. We were able to achieve micro-alignment of less than 100 nm position error. We will be expanding our discussion on the micro-alignment issue in section 3.5.

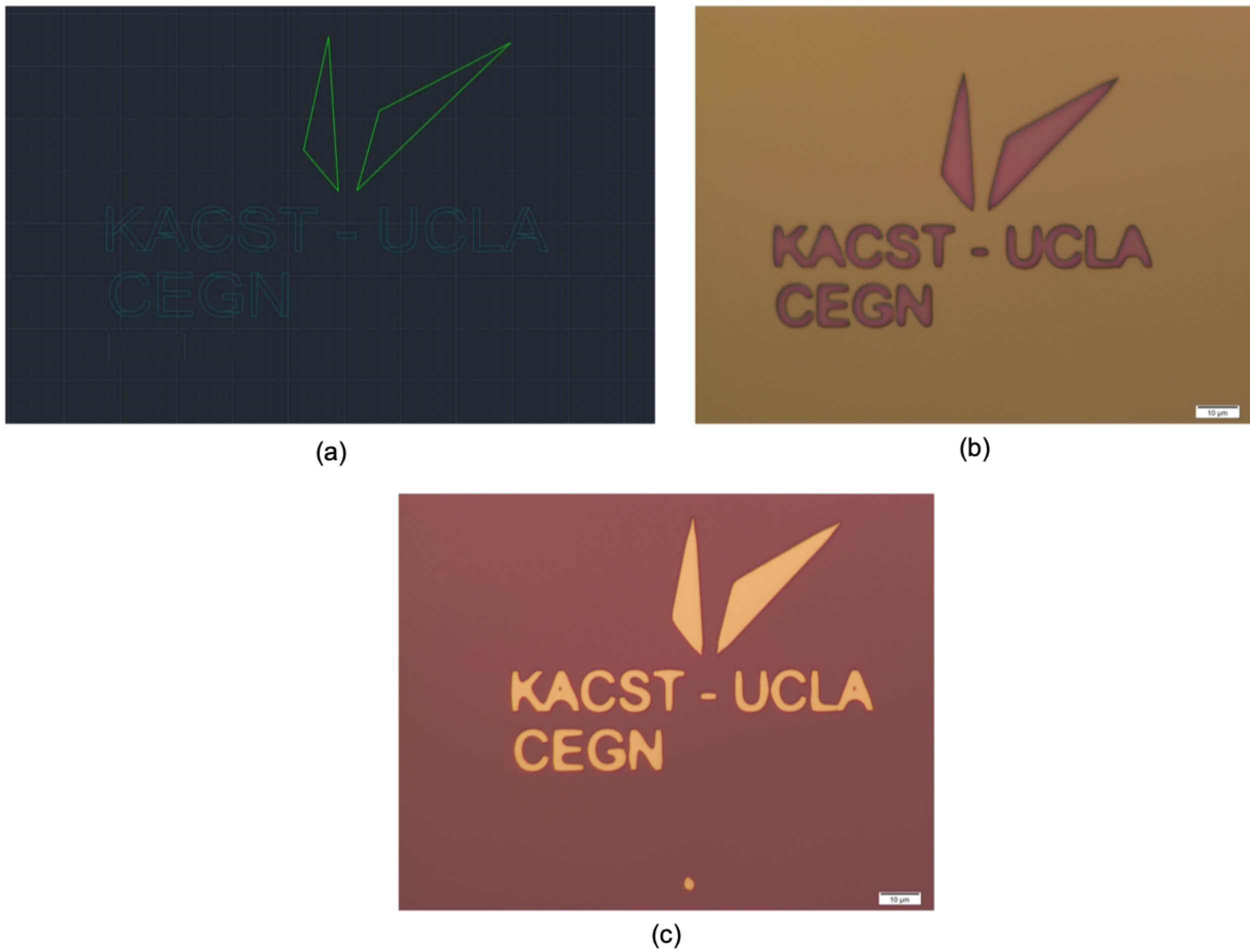


Figure 3.3-7 a small feature structure with the university logo attached with the Center of Excellence of Green Nanotechnology logo, smallest feature size of 300 nm

The third fabrication section is the shadow deposition, in order to chive minimum physical gap between the gates we will use the shadow deposition on the previously deposited top contact in the middle of the channel. Figure 3.3.8 shows a carton of the shadow deposition process; an extensive discussion of that process will be done in section 3.6.

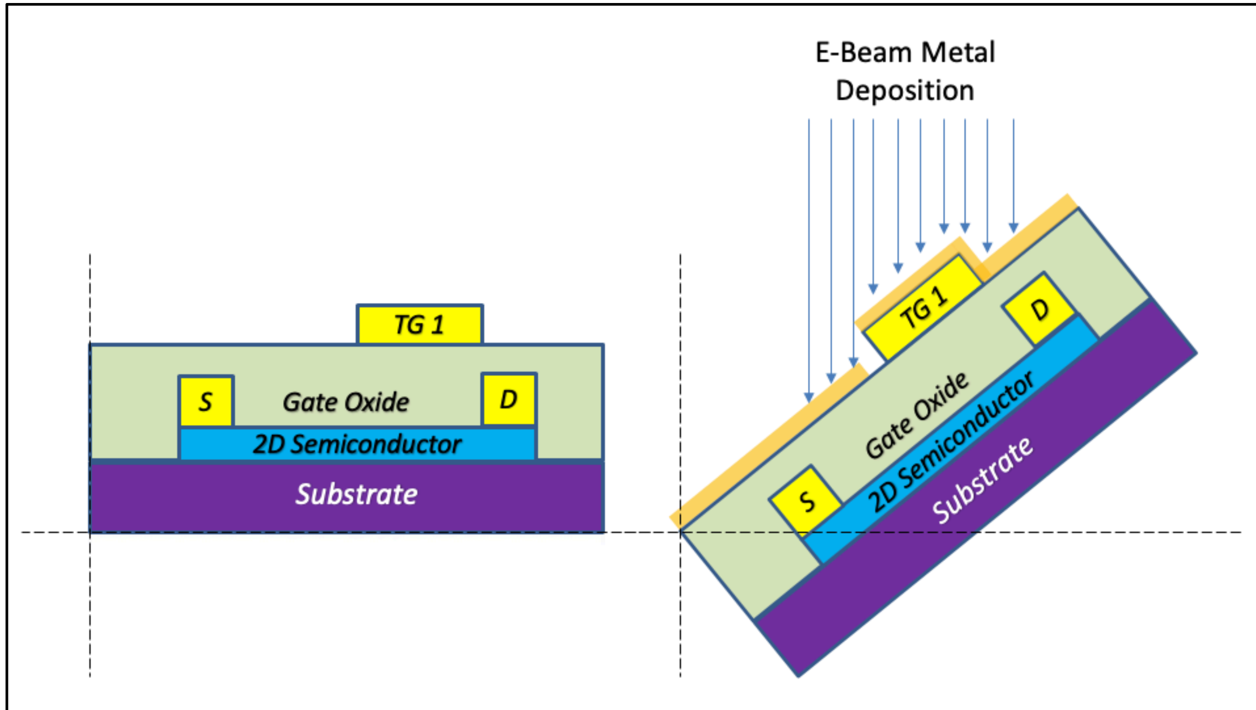


Figure 3.3-8 The shadow e-beam metal deposition concept

3.4 Insuring outstanding FET performance

In order to acquire clean tunneling behavior, and have an optimum T-FET performance device, an optimization of the foundational first layer FET is of a critical importance. Figure 3.4-1 shows an optical microscope image of the core FET device along with a cartoon of the device structure.

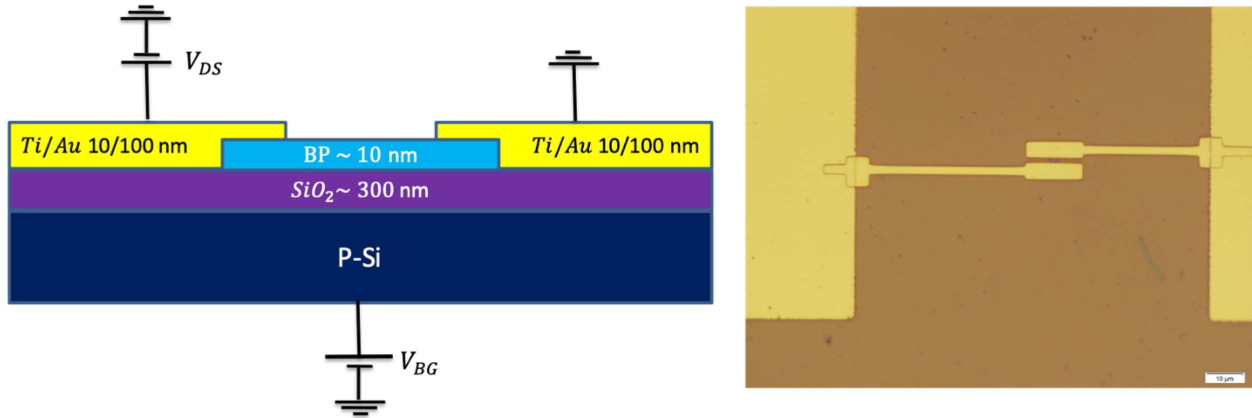


Figure 3.4-1 Optical microscope image of the core FET device (right) along with a cartoon of the device structure (lift).

Black phosphorus crystal was exfoliated on a 300 nm SiO_2, patterned through e-beam lithography with gate channel of 1 um, and metalized through e-beam metal deposition of Ti/Au of thicknesses, 10 and 100 nm, respectively. Figure 3.4-2 shows the output (left) and transfer characteristic (right) of the device. The output characteristic of the device had a current levels in the tens of Nano regime which indicate lower conductivity. Moreover, the slop is not entirely linear in the low V_{ds} and V_{bg}values, which indicates the presence of contact resistance and fermi-level pinning. The transfer characteristics shows an ON/OFF ration of 1000, and a saturation current level of 1 uA, note that we have the dual sweep from negative to positive V_{bg}values induced a hysteresis window, an indication of deep band gap traps. Figure 3.4-3 (a,b) shows the hysteresis direction of different starting point, and a cartoon of the possible mechanism. When the current is swept from negative to positive V_{bg}, the trap levels get filled with charge carriers, however, when we sweep on the opposite direction, these levels start to dump their charge carriers and increase the current level, which induces the hysteresis. The order of the subthreshold swing was in the level of 1000 mV/dec, which was the result of poor oxide interface.

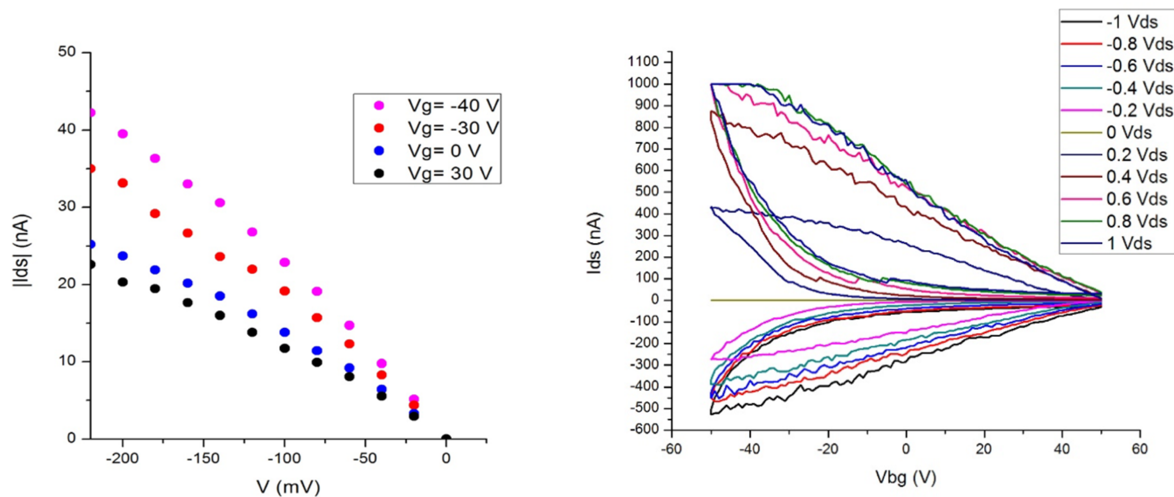


Figure 3.4-2 The output (left) and transfer characteristic (right) of the initial bP FET device

The reason of the trap level that was evident by the hysteresis is the existence of interface defects between the black phosphorus and the back-gate oxide (SiO_2), in addition to the formation of P_2O_5 oxide layer on top of the unencapsulated black phosphorus. The electronic characteristics of the black phosphorous device drops significantly within minutes of exposure, figure 3.4-3 (c) shows the compromise of the modulation ability of the device after few minutes of the first measurement run. It was a strong lesson that we learned during black phosphorus device fabrication, that even a delay of minutes, a long duration of the fabrication process, and an undiligent handling of each step of the device build up could redeem the device useless, and the long hours spent in the clean room wasted. The modified fabrication process was presented in section 3.3.

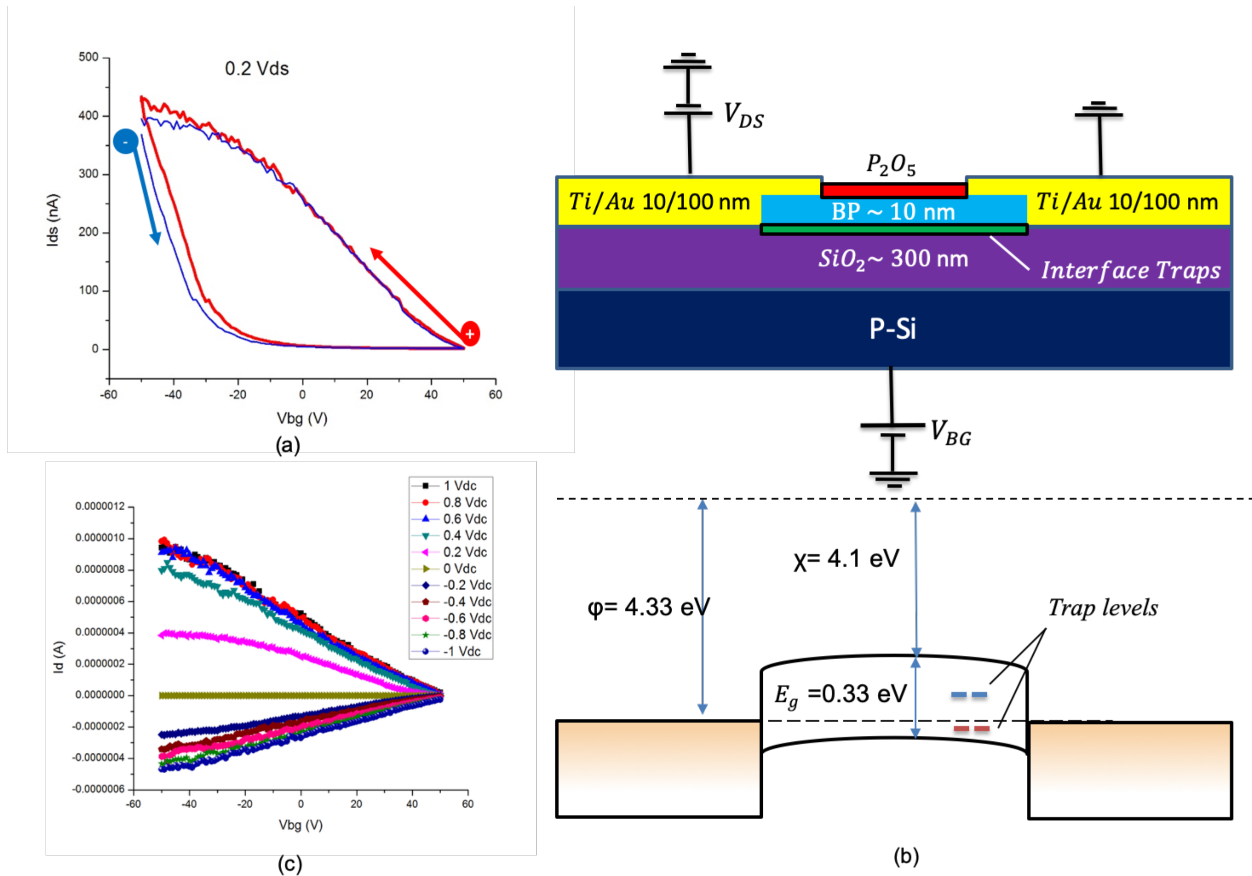


Figure 3.4-3 (a) The hysteresis direction of different starting point. (b) Cartoon of the origin of the interfacial trap on top of the bP flake, and at the back-gate oxide interface. (c) The compromise of the modulation ability of the device after few minutes of the first measurement run from 3.4-2.

Hence, in order to proceed with obtaining excellent FET device performance we needed to address three main points

1. Understand the oxidation behavior the black phosphorus few-layer material and propose ways to reduce it.
2. Enhance the contact resistance of the device.
3. Enhance the ON/OFF ratio, mobility, and subthreshold swing level of the device.

To address the first issue, we tried to understand the oxidation behavior of the black phosphorus flake, and see if we can answer questions, such as, what is the rate of the oxidation process, and what method can we apply to deem the device workable for an extended time frame.

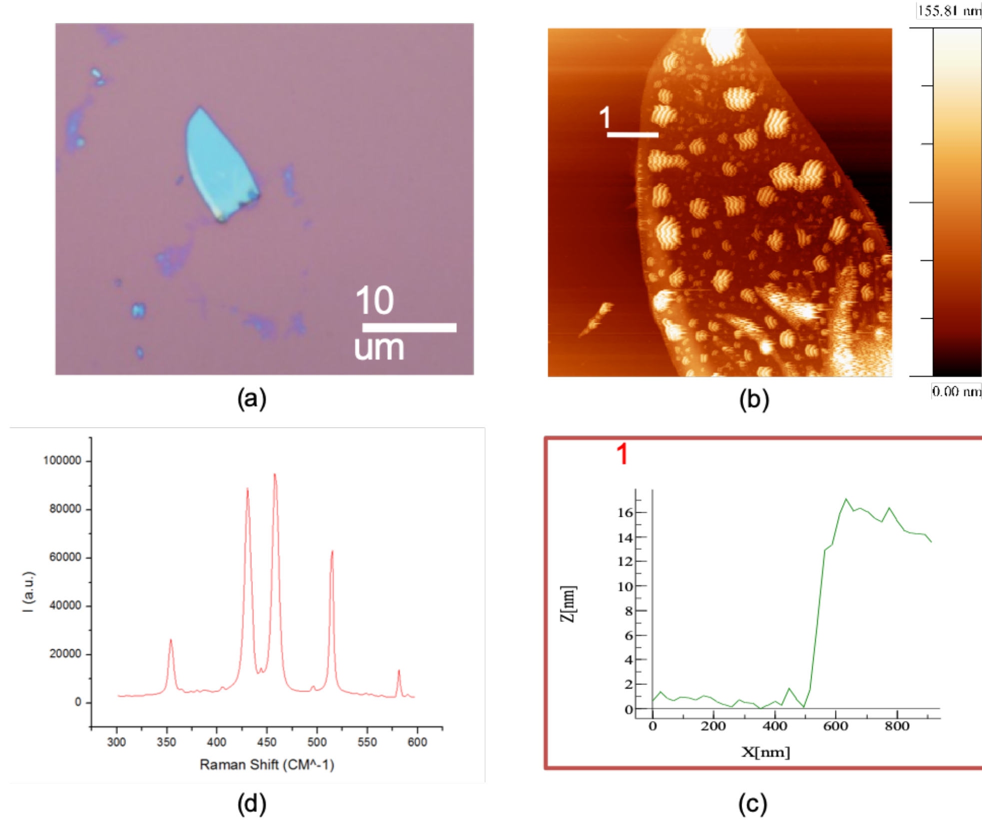


Figure 3.4-4 (a) microscopic image of a bP few-layer flake. (b,c) AFM scan of the flake along with thickness measurement of a portioned lined in AFM scan. (d) Raman scan of the flake showing the unique signature of bP peaks.

For that, we have exfoliated a black phosphorus flake near an AFM machine, and right away after detecting the flake using optical microscope, we inserted the substrate in the AFM instruments. The time that took us to exfoliate, detect, and set it up on the AFM machine measurement is less than 5 minutes. We will call that time as the zero-point time, or the "as exfoliated flake" phase. Figure 3.4-4 shows the microscopic (a) and AFM image (b,c) of the black phosphorus few-layer flake, along with the Raman measurement of the flake (d). The flake was around 16 nm of thickness, and the surface was not entirely uniform, the flake had few bumps on the surface which are due to the start of the oxidation of the material. The Raman measurement shows a clear signature of black phosphorus Raman spectrum of A_g^1 of 360 cm^{-1}, B_{2g} of 438 cm^{-1}, and A_g^2 of 466 cm^{-1}. Leaving the flake for a full day have made this small bumps volumize 10 times their original size, an indication of the formation of P_2O_5 bubbles on the surface of the flake, figure 3.4-

5 shows the difference between as exfoliated black phosphorus few-layer flake, and after one day in ambient air. A question that we presented is whether this process reversible, and whether we could extract these. We have experimented to treat the oxidized few-layer black phosphorus with UV radiation (30 s), and we have noticed a reduction of the size of the oxidation bump and also a thinning of the flake, figure 3.4-6. The flake went down in size from 16 nm to 10 nm. The oxidized region went from a height of 140 nm to 60 nm. We have also noticed the same behavior when we experimented with other bP flake by putting it under a vacuum of 10^{-6}Pa for 1 night, figure 3.4-7. The flake accumulated oxidation regions and volumized and went down in volume after the high vacuum treatment, the flake itself thinned just as we've seen with the UV treatment outputs. Hence, we conclude that P_2O_5 material that are forming on top of the flake are actually gaseous bubbles, and they undergo bursting under either UV treatment, or when just simply put under high vacuum treatment. Hence, we can answer our question of the reversibility of the oxidation process that takes place from an experimental point of view that it is impossible, since the material turn into gaseous compound and leave the material surface, which exposes the new surface to further oxidation, and thinning. From a theoretical point of view, Schlesinger et al have shown that the Gibbs energy calculation for bulk black phosphorus is irreversible since it had a G value of less than 0 [50].

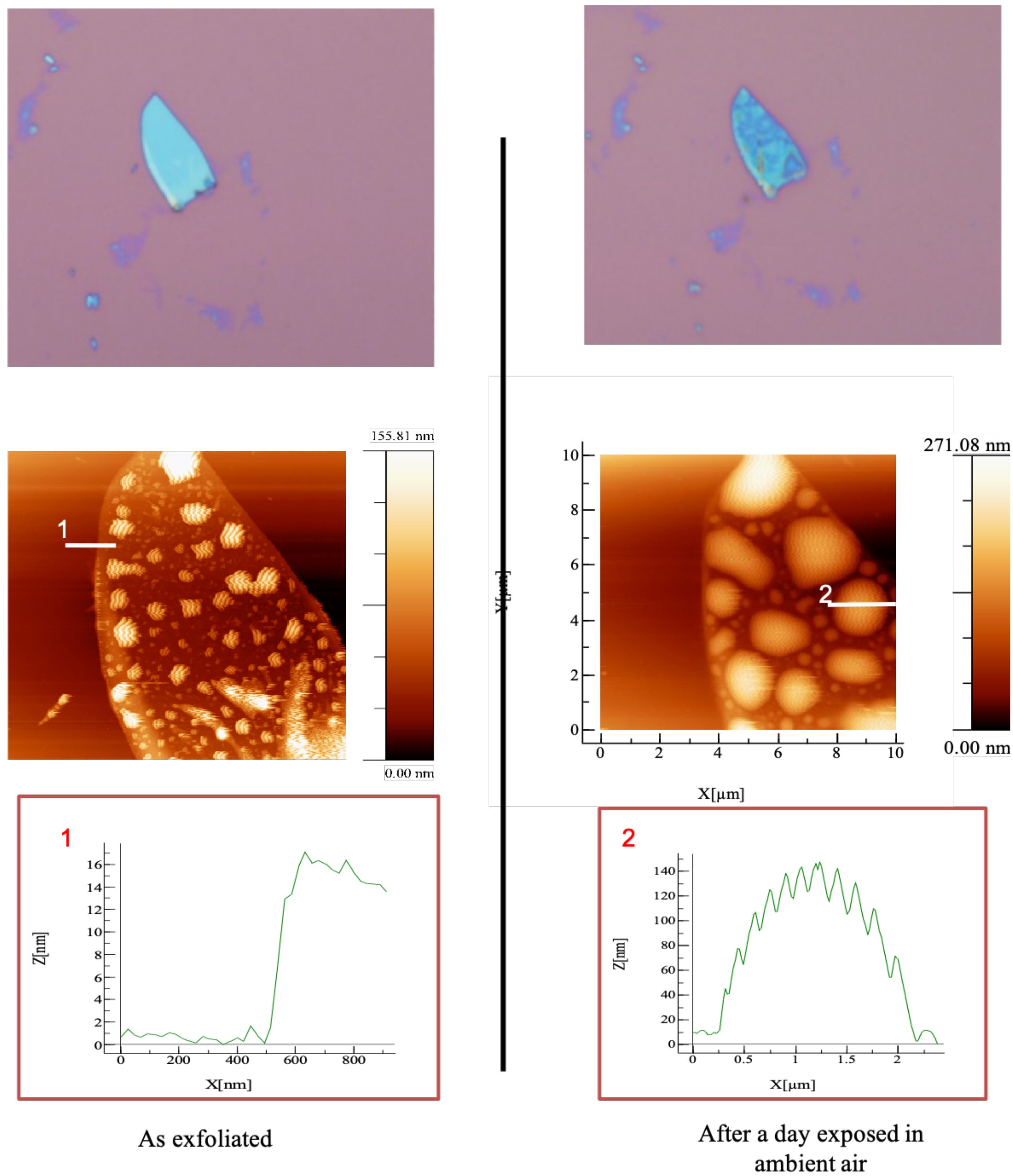


Figure 3.4-5 The difference between as exfoliated black phosphorus few-layer flake, and after one day in ambient air in terms of optical microscope image, Raman, scan, and thickness of the same segment in both measurement. The flake was volumized due to the oxidation of the bP flake, and the transformation of elemental bP into bubbles of phosphorus-oxide compound.

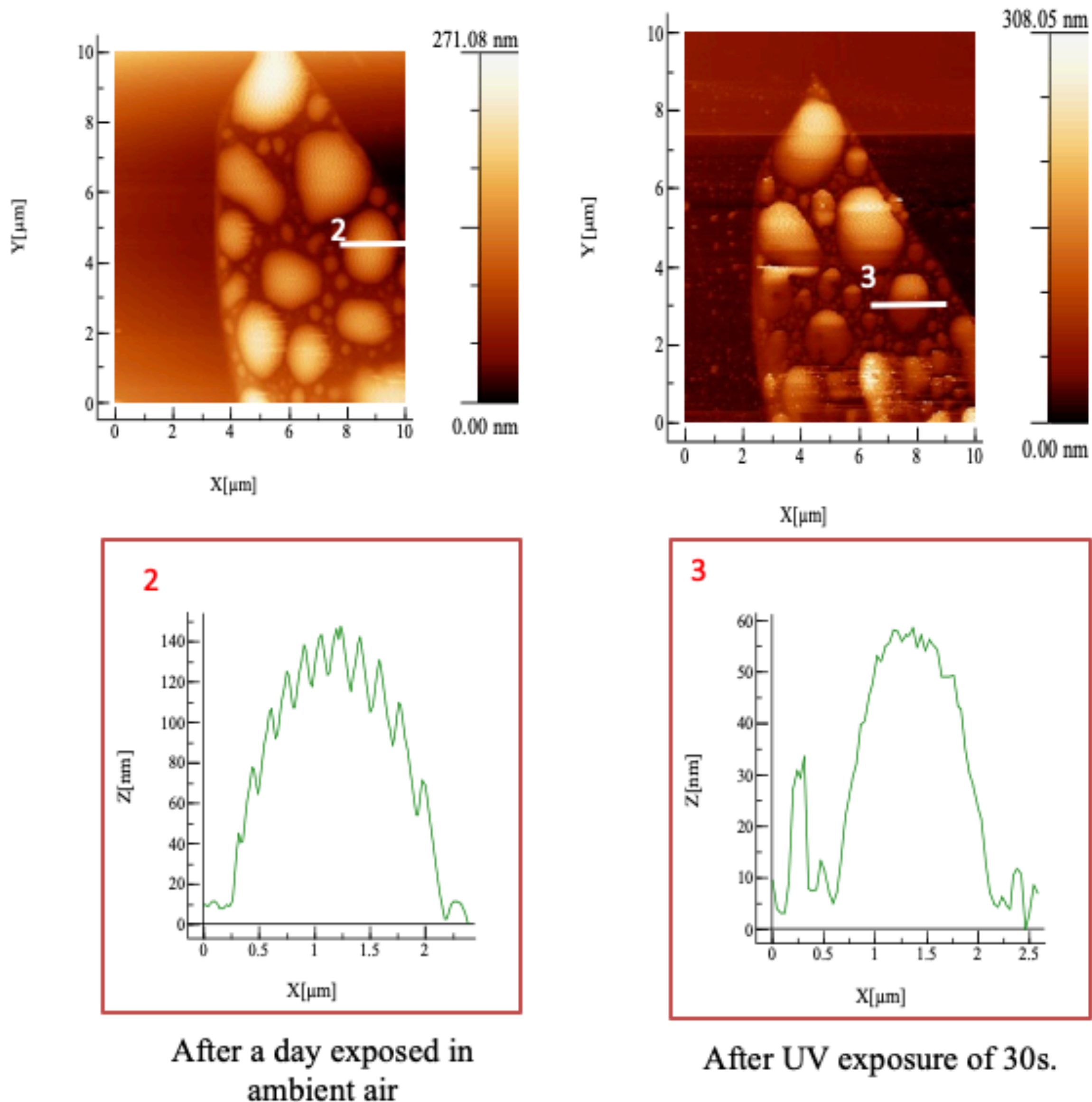


Figure 3.4-6 Thinning of the flake, and phosphorus-oxide compounds bursting and volatizing after 30s of UV light exposure.

It is important to note that the study of the oxidation behavior is not the scope of this project, however, it was important to shed a brief light on how to understand the problem in order to either avoid it or reverse it, to ultimately increase our FET device metric. Since we ruled out reversal of oxidation, we come to how to avoid the oxidation. We have encapsulated the flake with Poly (methyl methacrylate) (PMMA), which is the same material that we use as our photoresist material. In this case it used as a transparent and insulating thermoplastic to shield the flake from oxygen

and moisture. It is of course, a porous material, and oxygen can defuse at lower rates, but our Raman measurements have a shown a stability of encapsulated few-layer bP for 7 days by comparing A_g^1/Si ratio degradation over time, with normalizing it with the exfoliated Raman measurement, figure 3.4-8. Studies have shown the correlation between the A_g^1/Si ratio and oxidation [99].

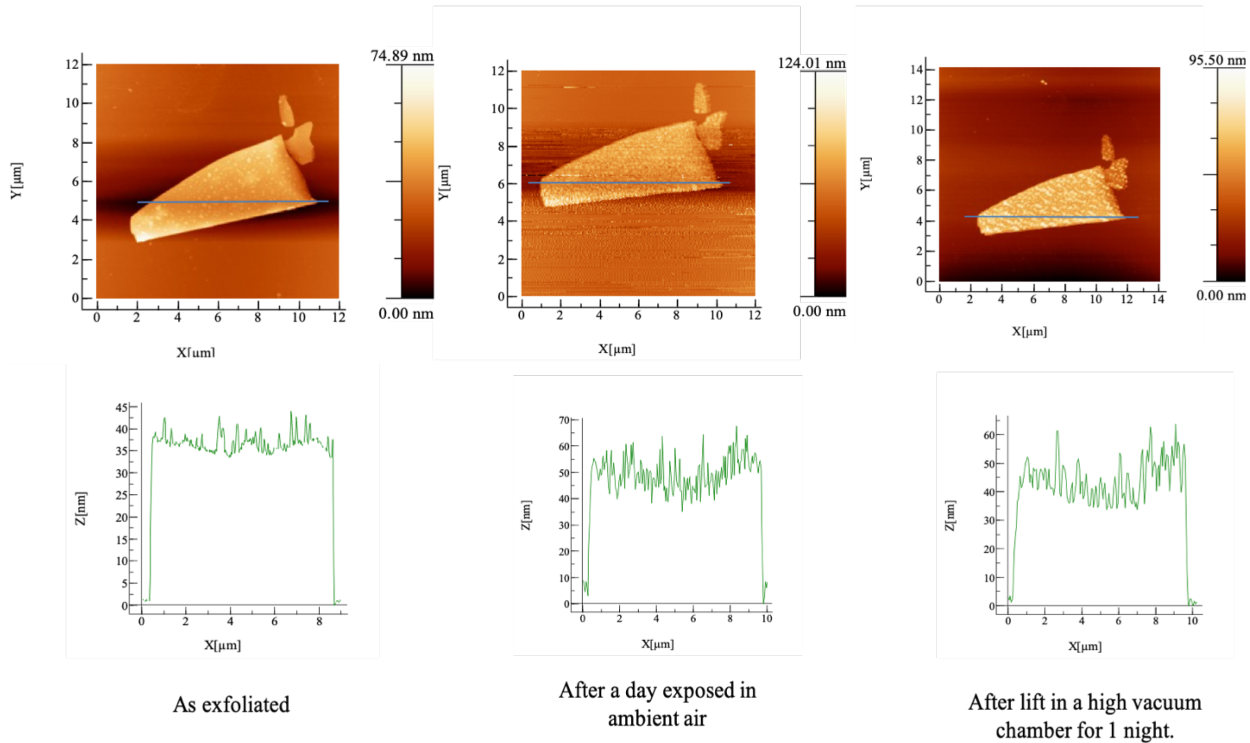


Figure 3.4-7 AFM of as-exfoliated flake (lift). AFM of the same flake after being exposed in the ambienf air for a inght (middle). Thinning of the flake, and phosphorus-oxide compounds bursting and volatizing after 1 night in a high vacuum chamber of 10^{-6}*Pa (right),*

It is important to note that the optical and phononic properties are as sensitive as the electronic transport properties of the deice, and we can deduce that, this method of encapsulating the device with PMMA will yield similar protection against oxidation, and electronic metrics should hold for extended periods, similar to what the Raman measurement experienced. In consistence with our observation, Wang et al have found that a 2% of distributed vacancies have shown to lead to 80% degradation of the material quality factor[116]. In a more detailed study, Huang et al shown with

controlled experimental result that bP quality rabidly degrade with the presence of oxygen but almost unaffected when exposed to deaerated water[117]. This process is realized by oxidation involving a superficial dissociative chemisorption of O2, whereas H2O molecules are weakly physiosorbed and do not dissociate on the BP surface. Oxidation (by O2) turns the hydrophobic pristine BP surface progressively hydrophilic[117]. They have reach to their conclusion in tandem with ours, but we have to point out, again, that the study of oxidation is not the scope of this project, but rather a brief light on it to help us avoid this problem during the fabrication process and acquire a n excellent FET metrics.

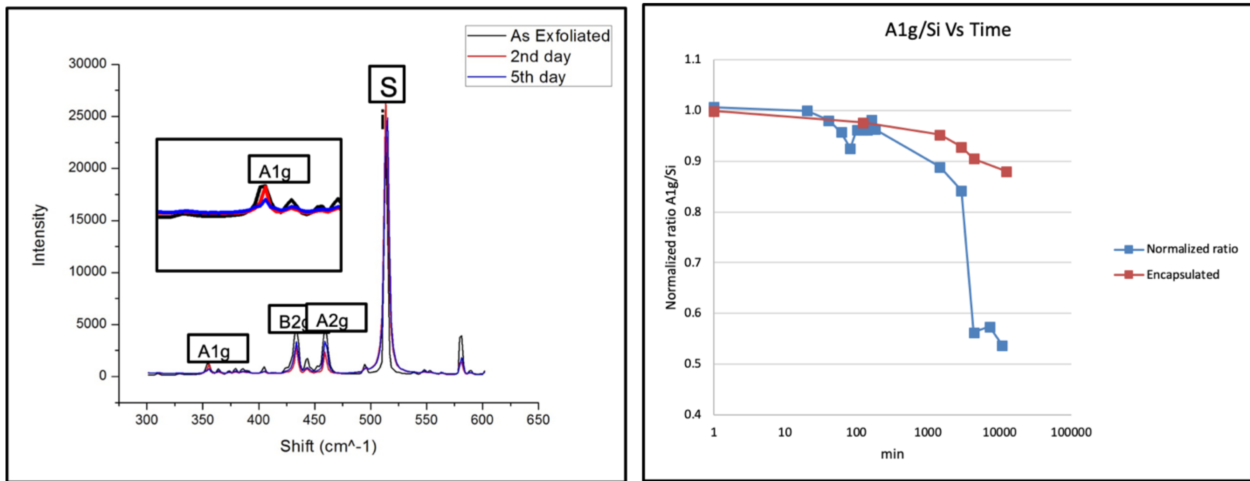


Figure 3.4-8 Raman measurements (lift), inset showing the peak corollate to the device oxidation. Sstability of encapsulated few-layer bP for 7 days by comparing A_g^1/Si ratio degradation over time, with normalizing it with the exfoliated Raman measurement against non-encapsulated flake (right).

The next modification is on the contact resistance front, high work function metals such as Sc, Ni, Pd, Ti and Cr have been used extensively in the bP device research[23,118,119]. Du et al, had gathered the first record on current values using Ni, and Pd contacts, with a pronounced ambipolar behavior using both materials[23]. The most recent ON current record was done by Li et al, when they employed scandium (Sc) as a contact material of 580 uA/um, it however, had a very poor ON/OFF ratio and SS of 800 mV/dec[118] .Ni, and Pd are not good candidates for our T-FET device since it helps the ambipolar behavior, and could overlap with our tunneling current. Hence, chromium (Cr)

and titanium (Ti) have the most suitable band alignment, and are relatively suppressant to the ambipolar behavior. We have found that Ti was not yielding good amount of working device due to the possibility of the metal reacting with black phosphorus, and just eating away the material upon deposition, figure 3.4-9 shows a sample of the failed Ti-contact devices with bp broken down or etched away from the contact are, most of the devices shows no conductivity, and the vicinity around the gold contacts are just SiO_2 substrate.

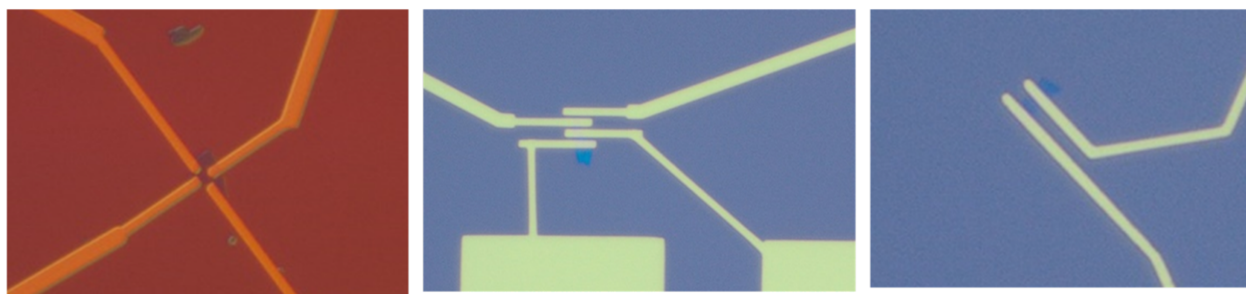


Figure 3.4-9 Sample of the failed Ti-contact devices with bP broken down or etched away from the contact are, most of the devices shows no conductivity, and the vicinity around the gold contacts are just SiO_2 substrate due to the reactive nature of Ti with bP.

Considering the low yield nature of black phosphorus devices; and considering the complexity of our T-FET device which consists of at least 24 fabrication steps per device that extends for several days; and considering that we would like to suppress ambipolar behavior to detect a more pronounced tunneling current rather than hole injection current, we have chosen Cr/Au to be the contact material. The standard thickness of the Cr/Au contact for Nanodevices are taken to be 10/100 nm. However, we tried to investigate the best thickness of the material. Figure 3.4-10 shows the contact resistance against different thicknesses of chromium. The measurement was conducted on 2 flakes with a total of 7 devices. We can deduce that the less the thickness of the active contact material, the better the conductivity, which can be attributed to the adhesion ability of the Cr material, actually in low thicknesses such as 0.5 nm, the chromium material is not uniformed on top of the black phosphorus flake, it is rather forming large scattered islands that anchors the Au on top of it and, hence causing better adhesion. After the above adjustments were conducted, a

device were fabricated and it had a good FET performance, figure 3.4-11 (a) shows a microscopic image of the device. The Id-VD characteristic was ohmic, the contact resistance was in the level of 1 Ωmm, Figure 3.4-11 (b). The transfer characteristics shown an ON/OFF ratio of nearly 10^3 and a 60 mA/mm current, however, the mobility was less than 50 $cm^2V^{-1}s^{-1}$, and the SS value was of the order of 400 mV/dec, figure 3.4-11 (c).

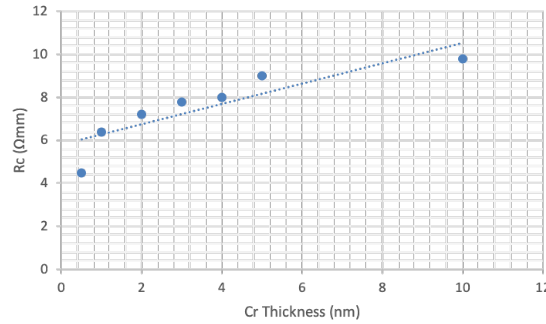


Figure 3.4-10 The contact resistance against different thicknesses of chromium, the lower the thickness the higher the conductivity.

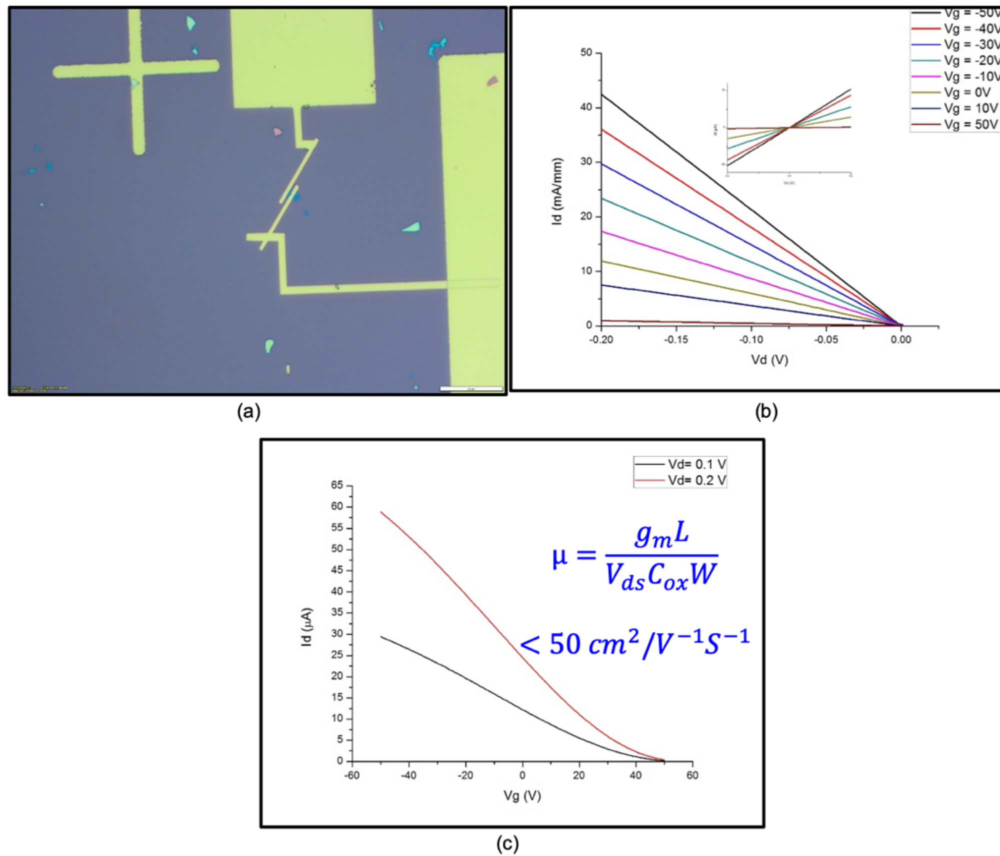


Figure 3.4-11 (a) Microscopic image of the bP FET device. (b) output characteristics showing an ohmic contact behavior. (c) The transfer characteristics of the enhanced bP FET device.

To take our device to the next level of performance in terms of enhancing the ON/OFF ratio, the SS value, and mobility, we went to a top gate approach. We have fabricated a device, with high-k top oxide of AL2O3 of thickness (10 nm), on top of a 10 nm black phosphorus device contacted by Cr/Au of 1/50 nm. The top gate then contacted with 100 nm Au, and the device length was 450 nm. Figure 3.4-12 shows an optical microscope image of the device, while figure 3.4-13 shows the transfer characteristic of the device.

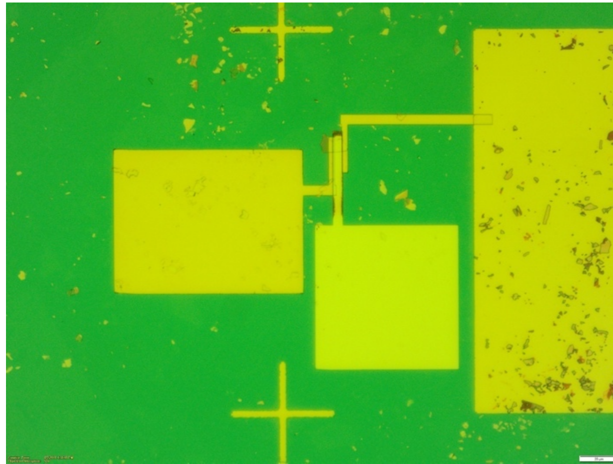


Figure 3.4-12 An optical microscope image of the top-gated bP FET device

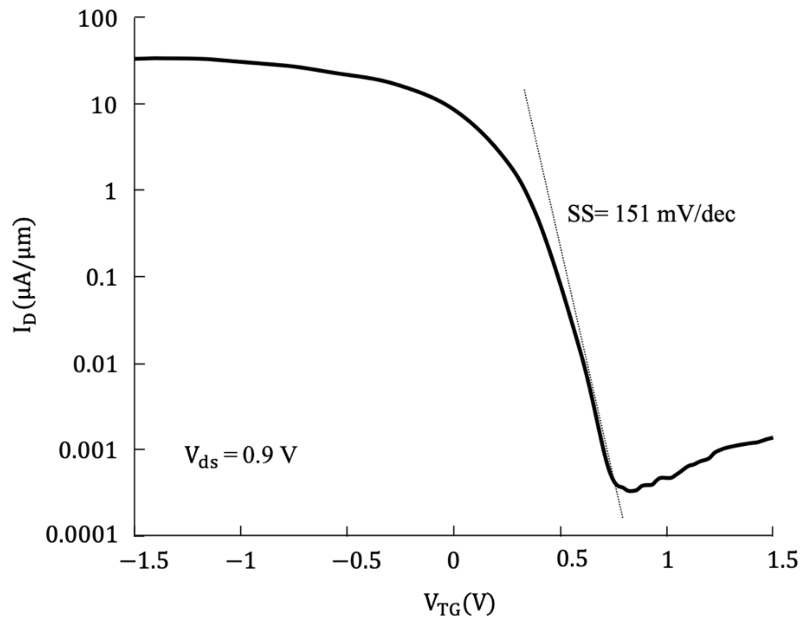


Figure 3.4-13 The transfer characteristic of the top-gated bP FET device.

The ON/OFF ratio of the device was in the order of 10^5, the saturation current was in the value of 59 uA/um, the SS was 151 mV/dec, and the FET mobility of the device extracted from the linear transfer curve to be 350 $cm^2V^{-1}s^{-1}$, the top gate leakage current was in the order of 1 pA/um, and finally a low hysteresis difference of less than 0.25 V, which is the difference between when scanned from the positive top gate values to the negative or vice-versa. These metrics of our bP FET can constitute an excellent foundation to build the split gate structure on top of it and extend the FET device into a T-FET device.

In order to use black phosphorus as the active channel material in field effect transistors, the assimilation with nm-thick high-k gate dielectric films is of great importance to the performance of the device[120]. So, high-k dielectric films without pinholes, with sub-nanometer thickness, and with low electrical defect density at and near the interface with the 2D semiconductor in general, and to black phosphorus in particular, are needed. Atomically thin high-k dielectric films of less than 2 nm have been successfully integrated into Si-based FET industry by using atomic layer deposition (ALD) technique[121,122]. Atomically-thick deposition control, and conformality over structured substrates due to the self-limiting chemical reaction between the precursor and the nucleation reactive sites of the surface are the great strength of the ALD technique[123]. In terms of Si surfaces, atomic layer deposition technique of high-k dielectrics is well recognized and studied. The significance of a high-level nucleation density for speedy layer termination is well-known and the means of nucleation have been thoroughly explored. Crucial for a speedy layer closure is that the preliminary surface offers sufficient reactive sites for reactions with the ALD precursors. Depending on the substrate material and deposition metrics, several successful nucleation preparation techniques have been proposed and studied depending on the substrate and the deposition metrics such as the fully hydroxylated SiO2 layer for the deposition of hafnium oxide, or the use of TMA composition on an H-terminated Si surface to form island-like ALD layer,

instead of the continues films. Hence, a proper functionalization of the surface is of great importance to insure best outcomes. The formation of nucleation site for depositing high-k material on top of black phosphorous is not yet understood. In our device, we use a seed layer of 0.5 nm Aluminum using E-beam metal deposition, due to the very low thickness of this layer, the seed layer is not continuance, but rather a form of islands-like nucleation sites of Aluminum that oxidized instantly upon exposing it to air. Considering the black phosphorus nature of reacting with moisture and oxygen, and considering the fact the Al2O3 deposition in ALD technique is rich with H2O and O2, and considering the high temperature requirement for this technique, we have revised the recipe to be a low-temperature (90°), high-cycle duration recipe which resulted in a very smooth surface of Al2O3 with almost no pinholes on the surface of black phosphorous, figure 3.4-14 shows an SEM of the ALD deposition morphology of 20 nm (45 cycles) thick layer, before(a) and after(b) using the revised recipe and the seeding Al layer, while (c) shows a carton of the nucleation sites creation and the final layer deposited on top of it.

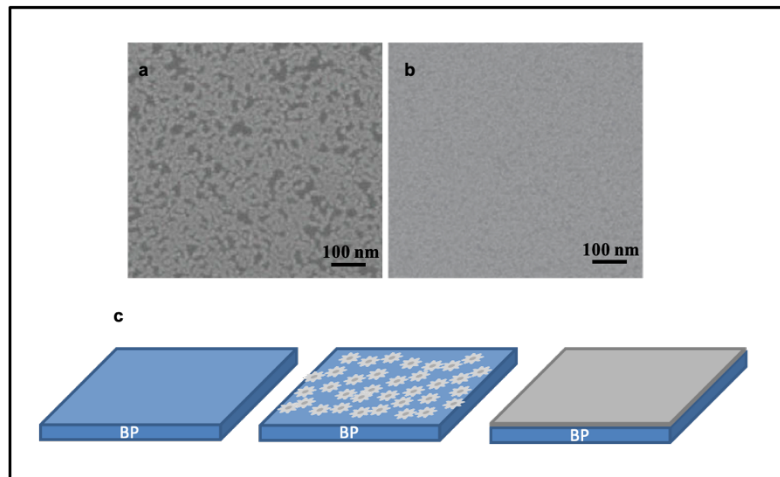


Figure 3.4-14 (a) ALD deposition of 45 cycles (20 nm) Al2O3 on black phosphorus with a standard recipe of 200° temperature and short cycle pulse duration. (b) Modified ALD deposition of 45 cycles (20 nm) Al2O3 on black phosphorus recipe with a 90° temperature and long cycle pulse duration, with nucleation cites provided from the seed 0.5 nm al layer. (c) Cartoon of the steps of surface preparation, seed layer deposition, and ALD deposition.

3.5 Insuring critical alignment of E-beam lithography

E-beam lithography machines expose patterns in one of the following means

- Scanning a focused electron beam over the target substrate.
- Projecting basic shapes created by an aperture.
- Projecting the whole pattern created by a mask.

A standard e-beam lithography machine has four fundamental components, the first is an electron-optical column which consists of electron source, beam deflectors, and electron lenses. The second is substrate positioning stage which consists of precession stage and laser infrometer that could have errors of positions go down to the micrometer regime. The third is the pattern generator which transforms a computerized design pattern to a series of beam deflections coordinates according to a desired exposure strategy. Fourthly, the electron-sensitive resist, or the substrate photoresist, in order to be able to register the beam pattern. The electron sources must demonstrate good current stability for dose homogeneity and sufficient brightness. Such sources include thermionic emitters, field emitters, and photoemitters. For thermionic emissions, thermal energy are used to provide electrons with the necessary energy to exceeds the potential barrier at the emitter surface. While in the field emission, electric field is used to provide that energy to the electrons. In photoemitters, the photoelectric phenomenon is used to eject electrons with sufficient light energy (frequency), and intensity. The tradeoff between thermionic emitters and field emitters is stability vs beam brightness or dose. Thermionic emitters exhibit outstanding current stability but weak brightness, while the case is turned around in field emitters. When electrons are created with any of these means, they get accelerated from the tip by a strong applied electric field. For lithography purposes electron possess energies between 1-100 keV. Table 3.5-1 shows the level of electrons energy corresponded to the suitable application

Table 3.5-1 Level of electrons energy corresponded with the suitable applications

Electron Energy level (keV)	Applications
1-30 keV	E-beam lithography, and SEM
100 keV-1.5 MeV	TEM
20 MeV	Localized cancer treatments
6 TeV	Large hydron collider

The optical column comprises of a sequence of lenses/deflectors which aim the electron beam on the wanted substrate point. Electric or magnetic fields are what constitute electron lenses. On the other hand, capacitor plates, and magnetic coils are what constitute electron deflectors. Interfering apertures in the column decrease the beam current and control the numerical aperture of the optical column. Since electron beam is limited by the area in which it could be deflected, a precision stage is required to form patterns. Since EBL systems function in vacuum, stages normally use roller bearings. Accurately positioned mirrors alongside each stage axis allow the use of a laser-interferometer for accurate positioning in more sophisticated EBL systems. The principle of interferometer in EBL is to compare a reference mirror to the stage mirror position. Presently, commercial laser interferometers can measure changes in position to up to 0.5 nm. The pattern generator transforms a computer scheme pattern into a sequence of beam deflections/blankers signals. The design normally comprises of polygons to write desired shapes of contacts and patterns. Usually, these polygon design will be broken down into trapezoids for the vector-scan pattern generator to fill these polygons. The dwell-time of the beam at each pixel dictated the amount of dosage on the exposed area. The raster scan beam then is swept across the writing field, with signals to deflectors and blankers being send instantly to expose or blank a specific pixel. The proposed path to form the minimum physical gap between the split gate contacts of the T-FET device is through shadow deposition. The physical gap is to be present at the exact middle of the channel to ensure proper tunneling performance and normalized electrostatic doping level in the p

and i region. Hence, it is after we fabricate our core top-gated FET device, we proceed with micro alignment process to ensure that we pattern a contact in the middle of the channel. It is a challenge to control your ebeam process, starting with photoresist type, photoresists thicknesses, baking temperature and duration, EBL accelerating voltage, EBL current/dosage, EBL dwell time, and EBL charge concentration to ensure optimized patterning, in other word, to a large degree, the deviation between the computerized design pattern and the actual developed pattern should be as minimum as possible. In the case of alignment and micro alignment, this add another layer of complexity to the operation. The maximum accuracy is dictated by the writing field size, the writing field for the FET device patterning is 200x200 um, this is usually too large in order to write the second layer contact, since the error factor will be in the order of 5 um. It is important to pattern markers along with first device patterning with lower writing field size in order to pattern the contact within a minimum error of accuracy. In our work, we have stitched 2 writing fields to achieve this minimum accuracy. The first field is having markers of 200x200 um size, while the second alignment marker field has a writing field of 50x50 um, which will yield a minimum of 100 nm error of accuracy. The JEOL system does not possess infrometer set up, and hence it is for the alignment markers to be within the writing field of the EBL, which means it is necessary to expose the area of pattern briefly to roughly align the markers. Figure 3.5-1 show a schematic representation of the second stage of microalignment, while figure 3.5-2 shows the marker set up in the CAD patterning file which shows (lift) the markers of the FET device and (right) the markers for the micro aligned top contact.

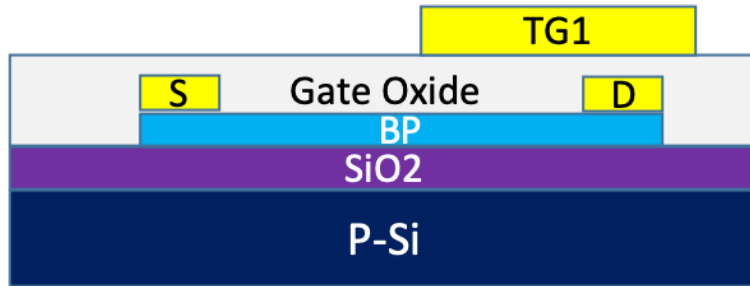


Figure 3.5-1 Schematic representation of the second stage of microalignment

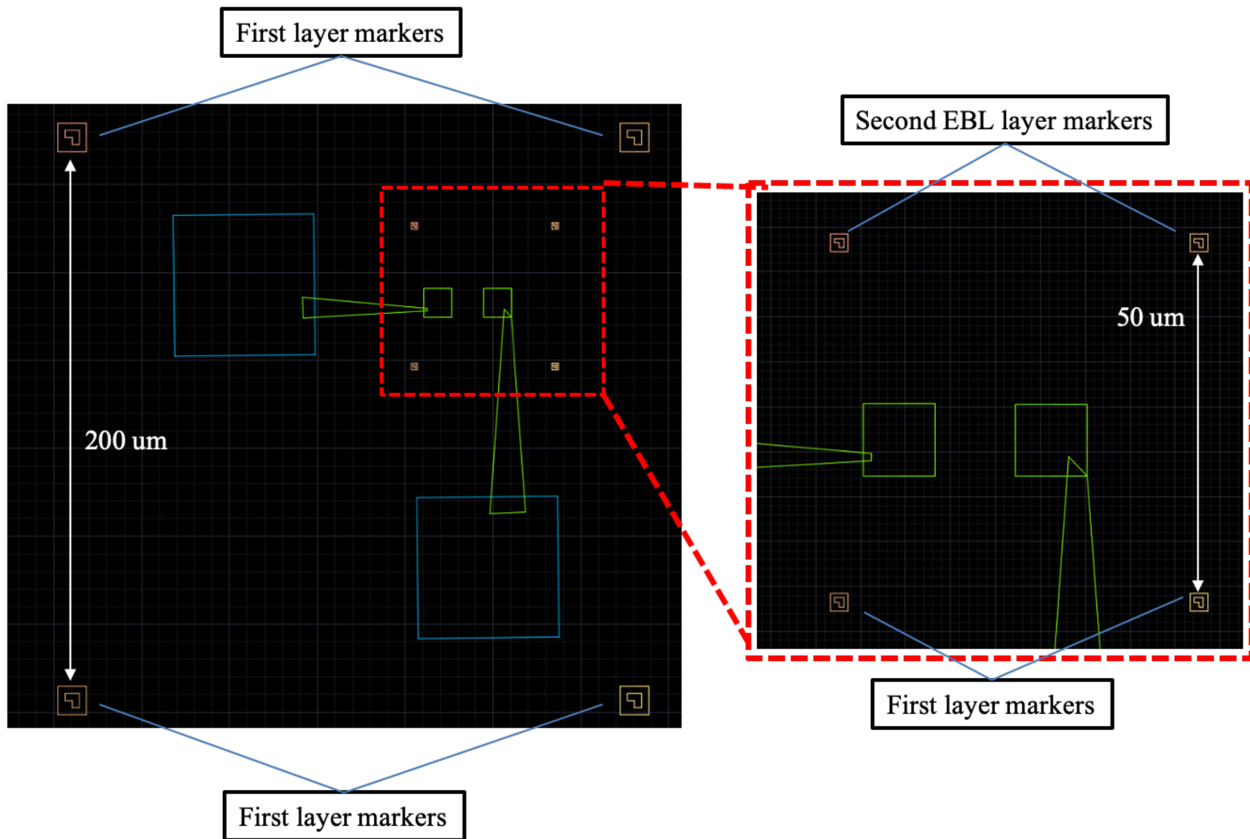


Figure 3.5-2 The marker set up in the CAD patterning file which shows (lift) the markers of the FET device and (right) the markers for the micro aligned top contact.

We proceed with designing the top contact on the CAD platform, and pattern it on EBL, we have achieved just little of minimum accuracy of 100 nm, and we got our error around 130 nm. The top contact was patterned on top of oxide, which is on top of the channel area, with one edge of the

contact right on the vertical middle of the channel. Figure 3.5-3 shows the CAD file design, and figure 3.5-4 shows an optical microscope image of the patterned top contact.

Microalignment of the Top Gate on the Middle of the Channel

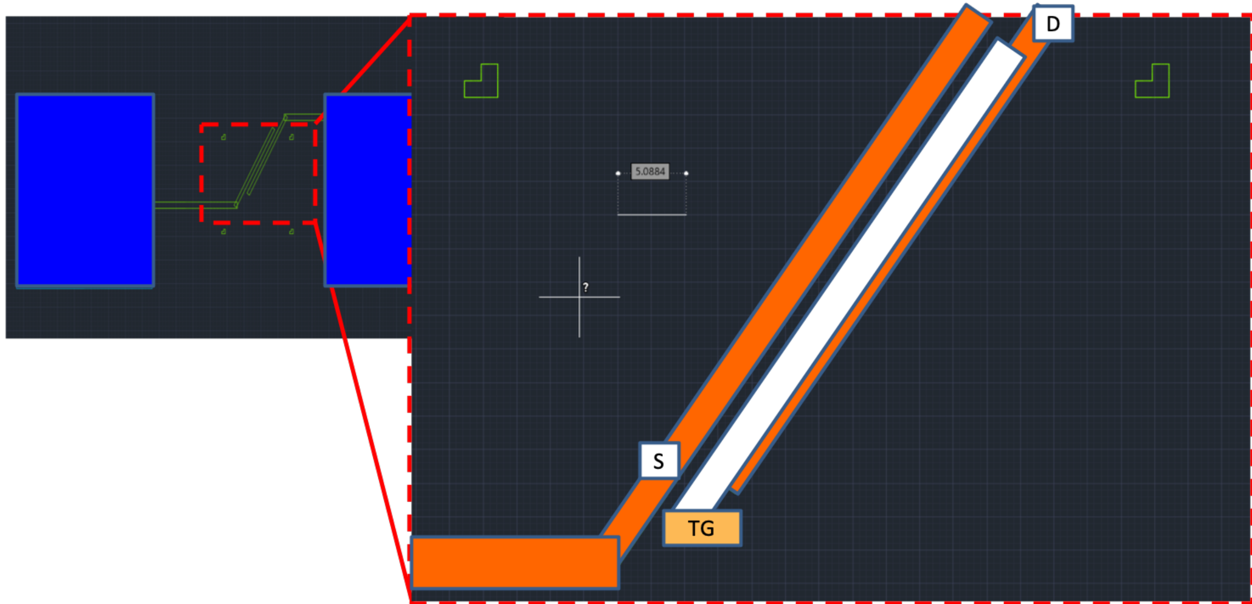


Figure 3.5-3 The CAD file design of the microalignment process of the top contact

Figure 3.5-4 An optical microscope image of the patterned top contact with one edge being in the middle of the channel area.

As mentioned earlier, it was impossible to go to a lower writing field size, e.g. better accuracy with a third layer of markers, because these markers will interfere with the device structure and could possibly short contacts. Figure 3.5-5 shows the crowded nature of the structure and the difficulty of stitching another smaller writing field.

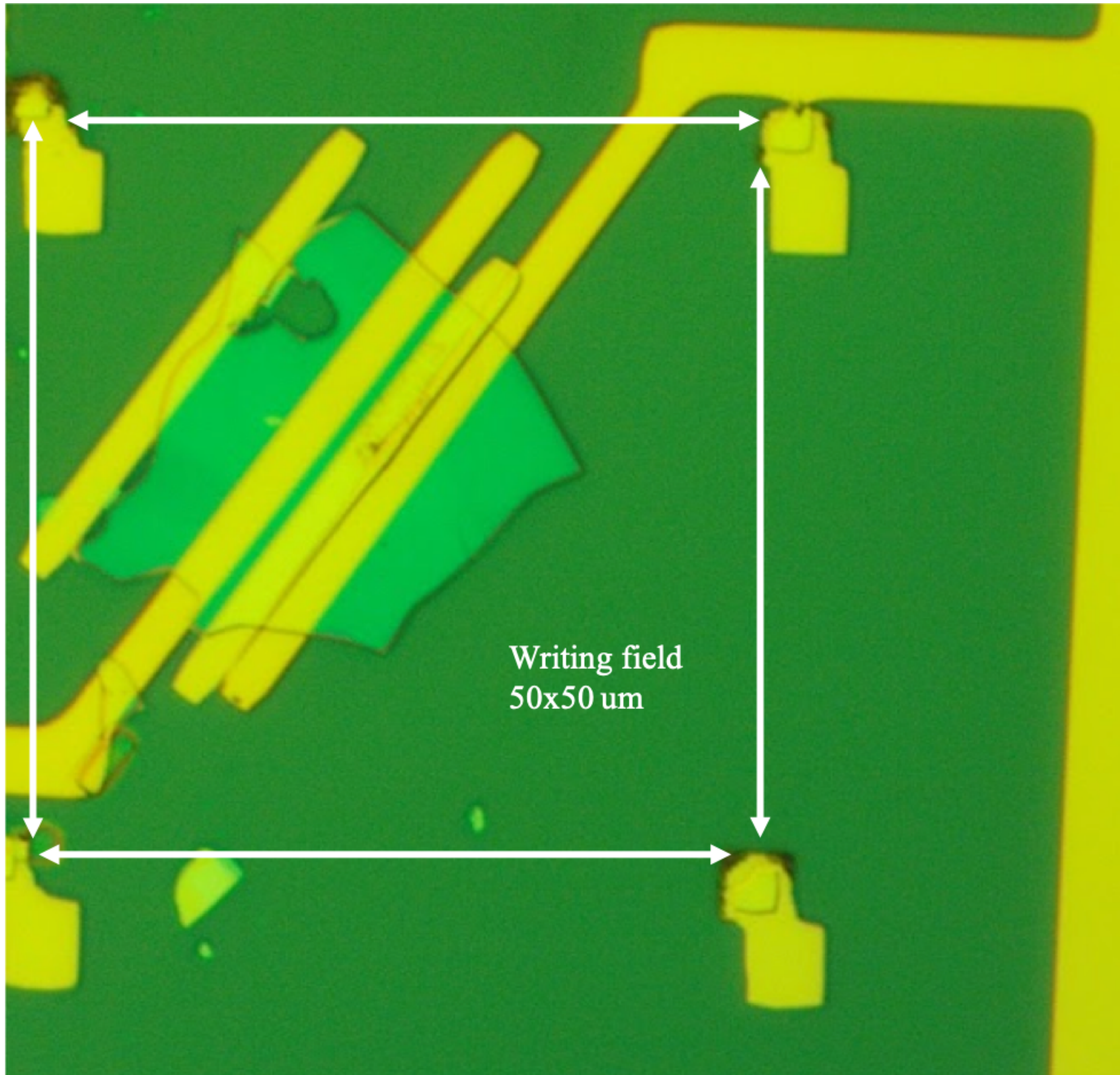


Figure 3.5-5 The crowded nature of the structure and the difficulty of stitching another smaller writing field, and hence lower accuracy levels.

3.6 Insuring minimal split gate gap with shadow deposition technique

The last section of the fabrication process is to form the split gate structure. In order to achieve a minimum split gate physical gap, we needed a different approach from using EBL. Considering

our writing field size and the distant markers, The EBL accuracy is ideally limited by 100 nm, which will increase the tunneling distance that charge carriers have to travel in order to form the tunneling current. Miao et al have fabricated a FET device with ultra-short channel of 20 nm using the shadow deposition technique and have acquired a record high on-current of 160 uA/um, figure 3.6-1[87].

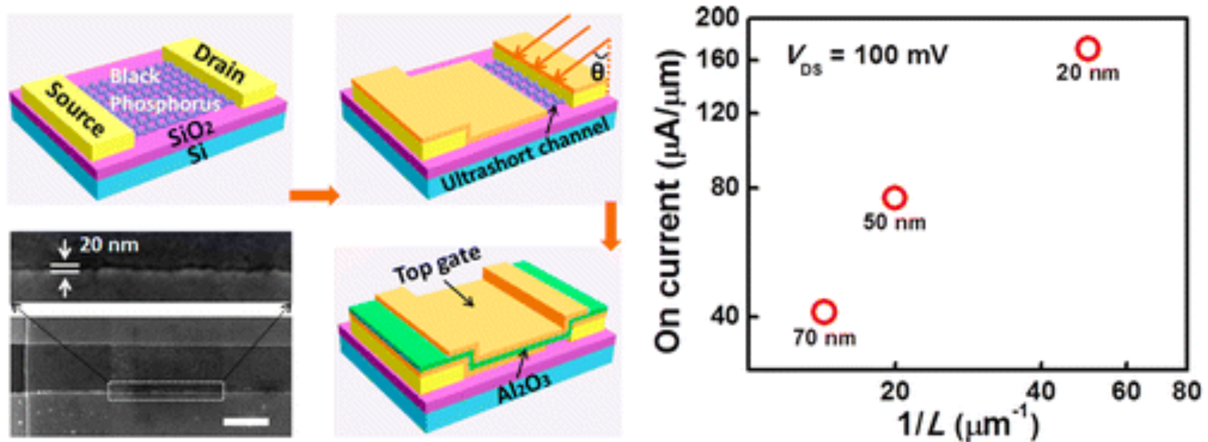
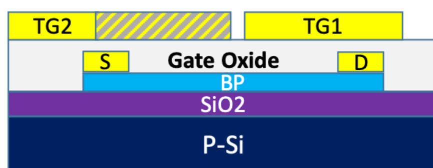


Figure 3.6-1 record on-current of 160 uA/um of ultra-short chanel using shadow deposition technique[87].

We have decided to use this technique to achieve our split gate structure. Figure 3.6-2 shows the schematic of the fabrication section. To proof our ability to perform the shadow deposition technique, we have firstly tried it on a dummy substrate where we deposited metal contacts and have inserted it in the e-beam metal deposition while shutting the turning function off. The e-beam metal deposition produces linear strings of evaporated metal. Tilting the substrate with a specific angle, a shadow is then naturally formed under the edge of the contact, and that shadow area is not exposed to the e-beam metal deposition string, figure 3.6-3.



Third Fabrication Section

- Angle resolved shadow deposition, gap < 100nm
- E-beam lithography, and E-beam metal deposition
- Encapsulation

Figure 3.6-2 Schematic of the device after the third fabrication section, the shadow deposition.

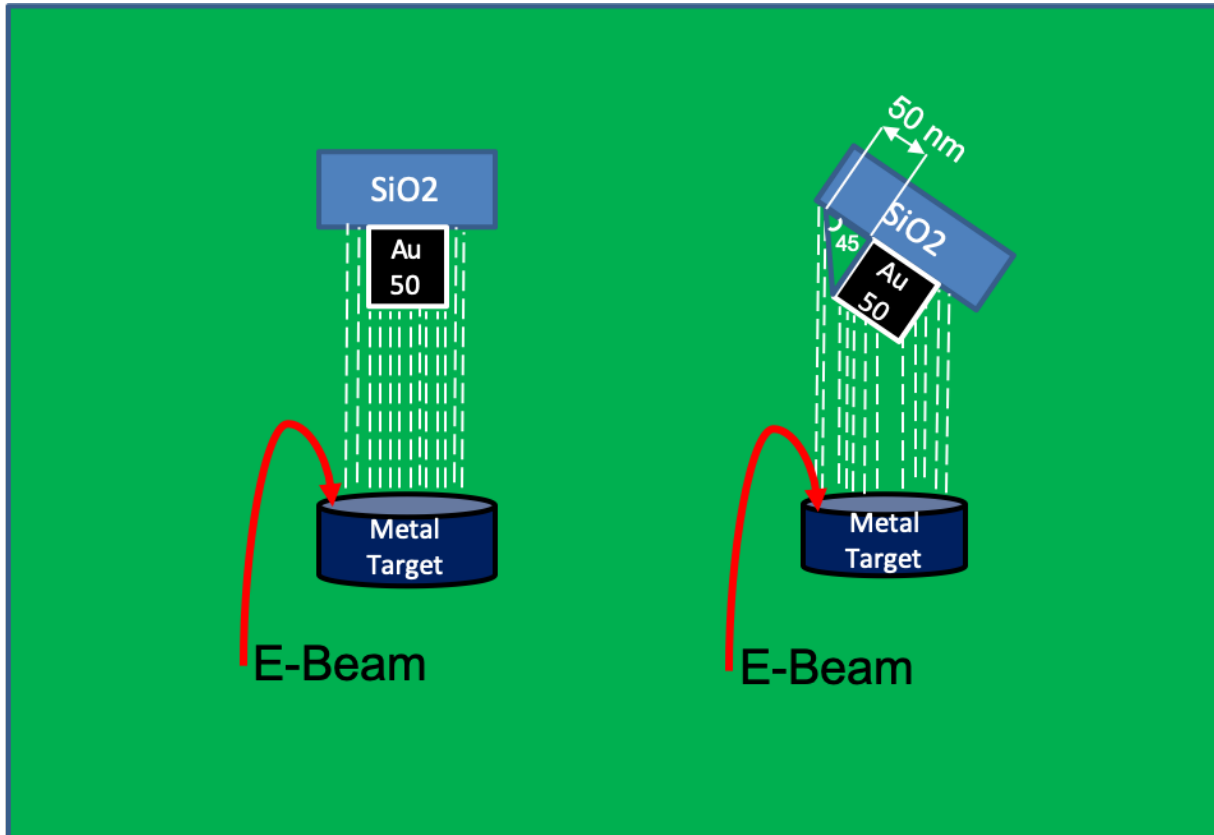
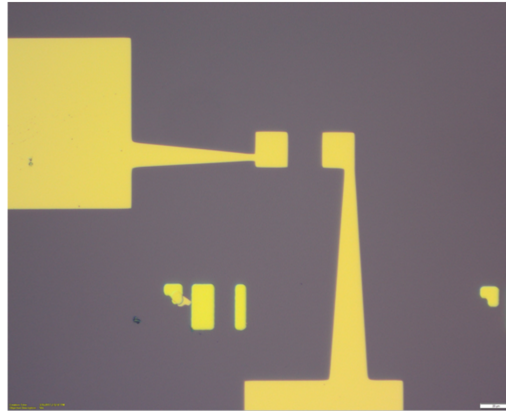
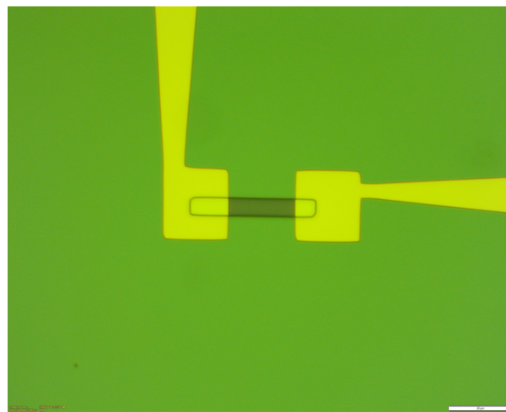


Figure 3.6-3 Cartoon of the shadow deposition process inside the e-beam metal deposition machine. The e-beam metal deposition produces linear strings of evaporated metal (lift). Tilting the substrate with a specific angle, a shadow is then naturally formed under the edge of the contact, and that shadow area is not exposed to the e-beam metal deposition string (right).

Figure 3.6-3 shows a dummy sample that underwent shadow deposition technique, the purpose is to optimize the angle of shadow deposition, and the thickness of the e-beam metal deposition material. First we fabricated regular contacts using e-beam lithography, and e-beam metal deposition, Figure 3.6-4 (a). We then spin coated that structure with photoresist and perform e-beam lithography to form an opening that will have the shadow deposition, figure3.6-4 (b). We then perform the shadow deposition technique on a 45 degrees angle using e-beam metal deposition using aluminum as the shadow deposition material, figure 3.6-4 (c).



(a)



(b)

(c)

Figure 3.6-4 Dummy sample to study and optemize the shadow deposition process. (a) Fabrication of 50 nm Au contacts using e-beam lithography, and e-beam metal deposition. (b) Spin coated that structure with photoresist and perform e-beam lithography to form an opening that will have the shadow deposition. (c) subjecting the e-beam deposition to the shadow deposition process of 10 nm Aluminum.

To characterize the success and functionality of the gap we either run a resistance measurement between the split gate contact, and for its success it must show no significant conductivity, figure

3.6-5, or run an SEM imaging analysis to see the gap distance, figure 3.6-6. We try to avoid SEM characterization since the e-beam generated could adversely affect the 2d sample. We have noticed that it is hard to achieve shadow deposition with higher tilting angle, since the probability of shorting between the contact increase, nor we can increase the thickness of the deposition, since also the shorting between the split gate will occur, figure 3.6-7 shows the relation between the angle of the shadow deposition and rate of success.

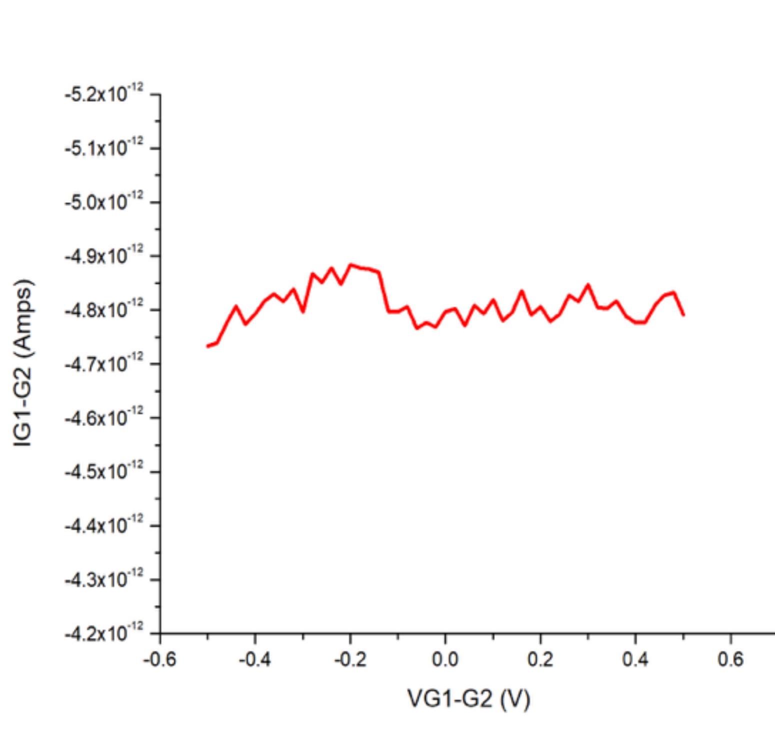


Figure 3.6-5 No conductivity between the split gates structure, which indicate no shortening, and a successful shadow deposition.

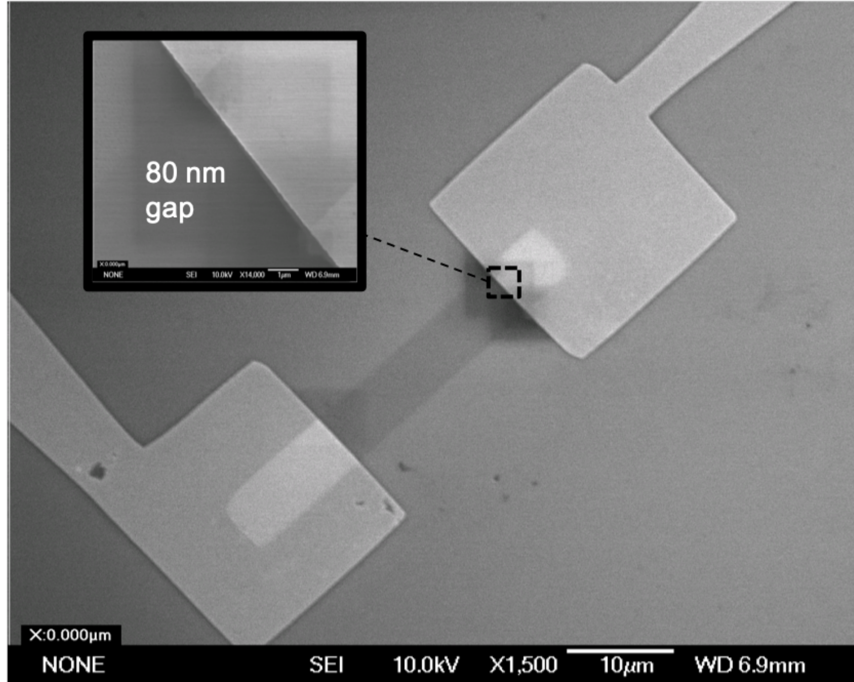


Figure 3.6-6 SEM imaging of the dummy sample, 70 nm gap between the split gates was formed.

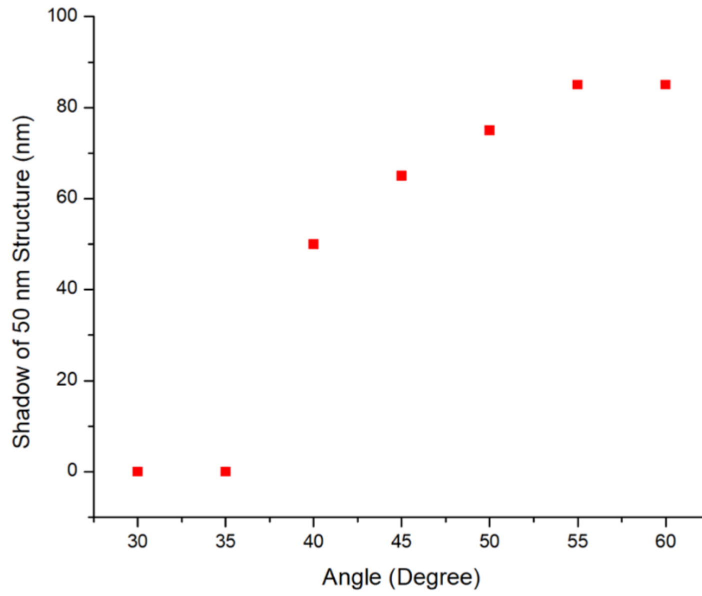


Figure 3.6-7 The relation between the angle of the shadow deposition and the size of the formed gap between the split gates.

3.7 T-FET device performance

TFETs have been put forward to be energy-efficient substitutes to the MOSFET that can reduce the supply voltage and satisfy the low power requirements[124,125]. Although TFETs theoretical foundation provide a steep switching needed to reduce power dissipation, nevertheless, the saturation current of TFETs is low[126,127]. which weakens their functioning speed and energy-delay figure of merit[128]. The band to band tunneling (BTBT) of carriers is the main mechanism of TFET to provide such current level. Therefore, the tunneling current is extremely sensitive to the effective mass and bandgap of the channel material. Although a reduced effective mass and bandgap improve the saturation current level and supply voltage reduction, in a similar manner this also worsen the OFF current and channel length scaling limitation[129]. To achieve the coinciding requirement of the semiconductor industry of both supply voltage and channel length scaling, materials with specific value of effective mass and bandgap, need too be either found, or carefully designed and prepared. It has been shown that the recently studied few-layer black phosphorus[92] offers the ideal electronic properties to attain extraordinary performance in TFETs while at the same time immune to the short channel effects. According to the following relation

$$\log I_{on} \propto \frac{-\sqrt{m^* E_g}}{F} \tag{3.7.1}$$

I_{on} is exponentially dependent on the effective mass (m^*), the band gap (E_g), and the electric field at the tunneling junction (F). Therefore, both of increasing the electric field or tailoring the perfect combination of effective mass and band gap could yield an enhanced I_{on}. Tight control of the channel band profile with strong electric field has been explored in 2d materials in the past, along with exploration of high-k and low-k materials, and internal polarization of Nitride[21,36,130–132]. In

addition to being of the two-dimensional material family, which is an atomically thin channel that improves electric field control on the channel profile, few-layer black phosphorus has the optimal combination of E_g and m^* necessary for high functioning TFET. Additionally, the bandgap of few-layer black phosphorus is direct, and whether the bandgap is of a single layer (2 eV) or of bulk regime (0.3 eV), it stays direct bandgap. As mentioned in Chapter 3.2, bP has a strong advantage over other 2D materials, such as graphene and TMDs. Graphene has no bandgap, which render it useless in the switching applications. Even if this bandgap is engineered, the transistor application is of great instability [133]. On the other hand, most single layer TMDCs have a bandgap greater than 1 eV. While the bandgap of few-layer TMDCs system could go below 1 eV, It is however indirect bandgaps, which means that the phonon assisted tunneling that was induced by momentum mismatch causes degraded ON current. Hence, and because of the atomic thickness nature of black phosphorus which means better electrostatic length and diminished short channel effects, and because of its suitable band gap in the few-layer system while being direct, and because of the low anisotropic effective mass value in both direction of arm chair and zigzag, we chose black phosphorus to be our active material of the TFET. After insuring to obtain excellent FET performance, excellent micro alignment accuracy, and minimum physical gap using shadow deposition, we thin move forward to combine all of this to fabricate a whole device in one diligent, sequenced, and extremely quick fabrication process that spans for 36 hours continues. Figure 3.7-1 shows the general steps of the TFET device fabrication, after exfoliating the black phosphorus crystal and encapsulate it with photoresist instantly the exfoliated flake, we then took it and run the first round of FET fabrication which consists of a round of e-beam lithography and e-beam metal deposition, along with writing the second set of markers to help us with microalignment (a), then we take that device and perform microalignment through e-beam lithography, and e-beam deposition of a top contact in the middle of the channel (b), and finally we perform the shadow

deposition on the top surface of the structure to induce the minimum physical gap of the split gate structure (c).

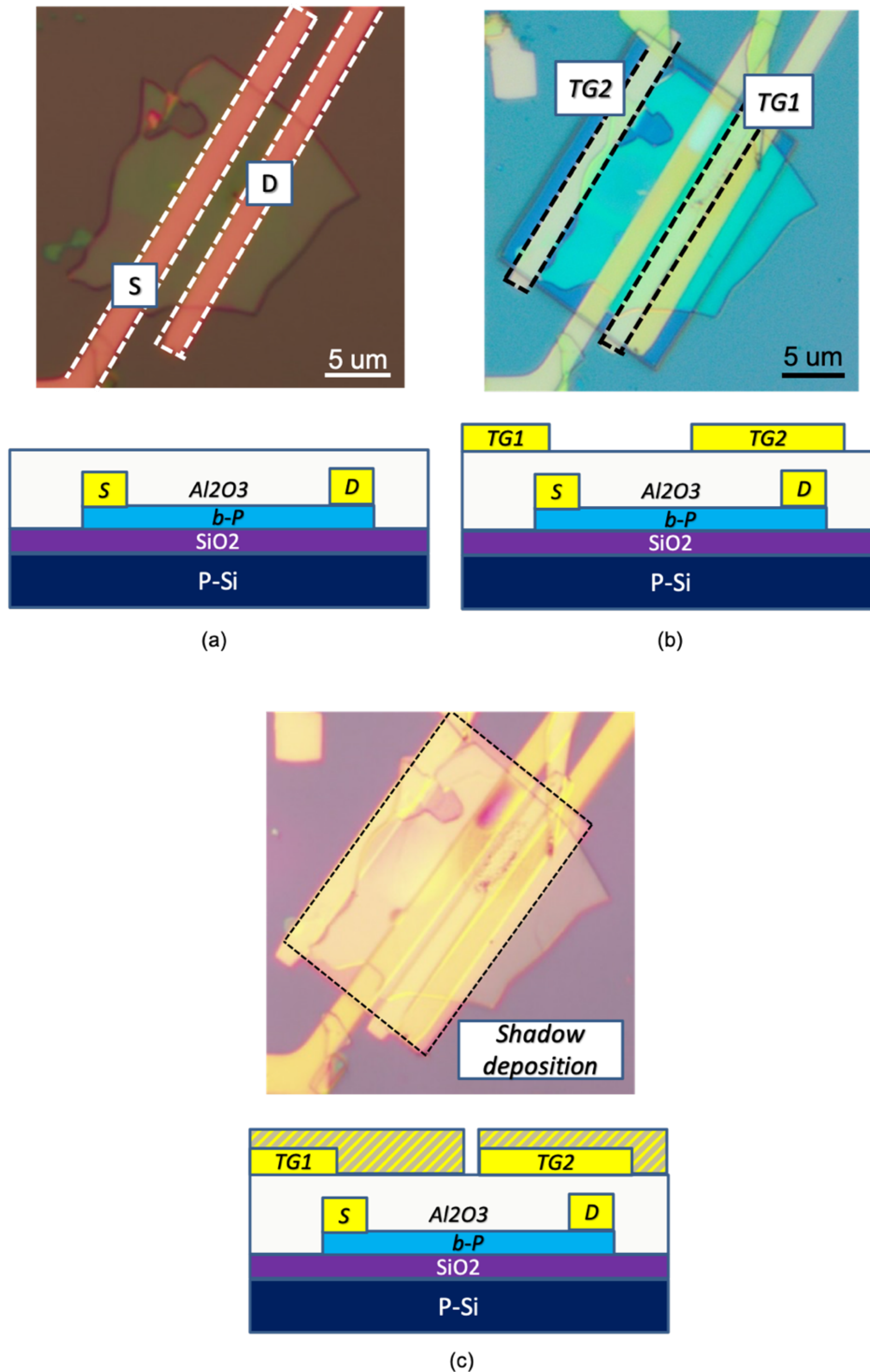


Figure 3.7-1 the general steps of the TFET device fabrication. (a) After the first round of FET fabrication which consists of a round of e-beam lithography and e-beam metal deposition, along with writing the second set of markers to help us with microalignment. (b) after performing microalignment through e-beam lithography, and e-beam deposition of a top contact in the middle of the channel. (c) after performing the shadow deposition on the top surface of the structure to induce the minimum physical gap of the split gate structure.

Figure 3.7-2 shows an SEM image of the structure. The structure of the shadow contact height is 50 nm and fixing the angle of the tilting stage in the metal e-beam deposition was set for 45 degrees, which should yield 50 nm gap. However, considering the primitive nature of the tilting stage that we made in the machine shop, it might not be accurately set at 45 degrees, it is important to mention that a small change in the angle could yield stronger change in the gap, this was mentioned in the shadow deposition fabrication section, so in other word the relation is not entirely linear beyond the 45 degree point. Nevertheless, 70 nm should be suitable to perform our measurement and expect a tunneling current.

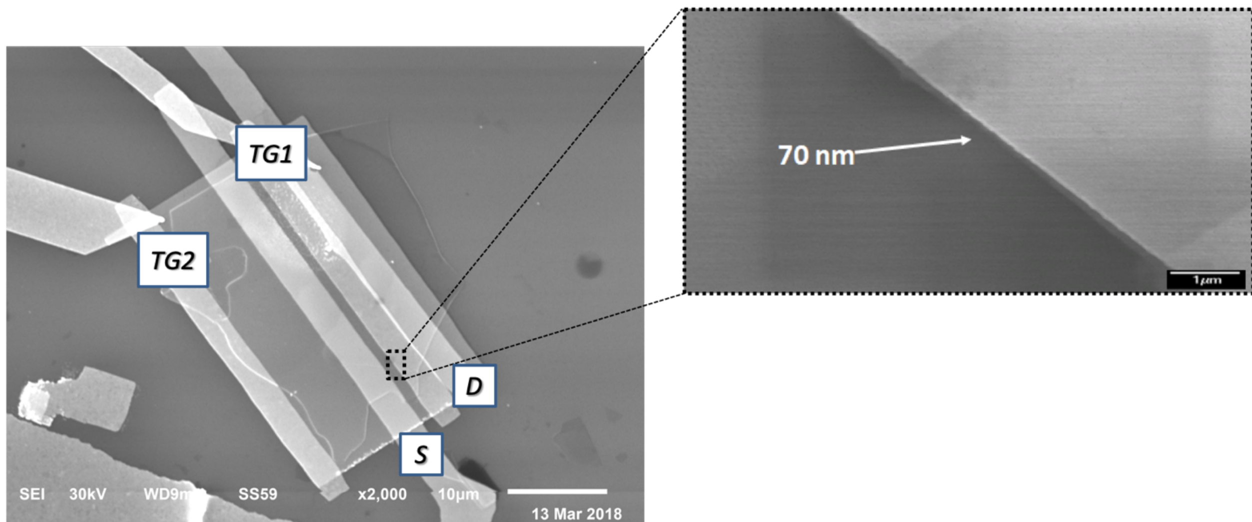


Figure 3.7-2 SEM image of the T-FET structure

The band diagram of the device shown in figure 3.7-3 shows the principle of the operation of our T-FET device. The device consists of two split gates contacts, we will mark them V_{TG-1} and V_{TG-2}. In our set up, we will electrostatically n dope V_{TG-2} to lower energies of 3 steps being 0, 1, 2 V. Simultaneously, we will sweep V_{TG-1} at each step from -3 V to 3V, which will range the doping of the region underneath that contact from p-type to n-type. This manipulation of V_{TG-1} and V_{TG-2} will yield two operation mechanism, the first will yield classical MOSFET operation, while the second manipulation arrangement will yield the TFET operation, figure 3.7-4 shows both arrangements with their corresponding band diagram.

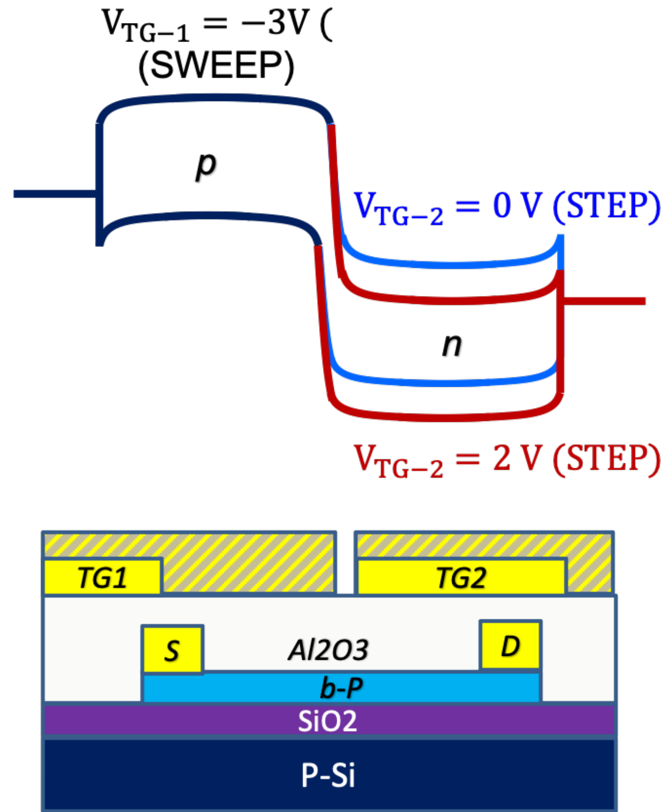


Figure 3.7-3 The band diagram of the device, sweeping the first gate contact while stepping the second gate contact to form favorable arrangement for either MOSFET operation or tunneling FET operation.

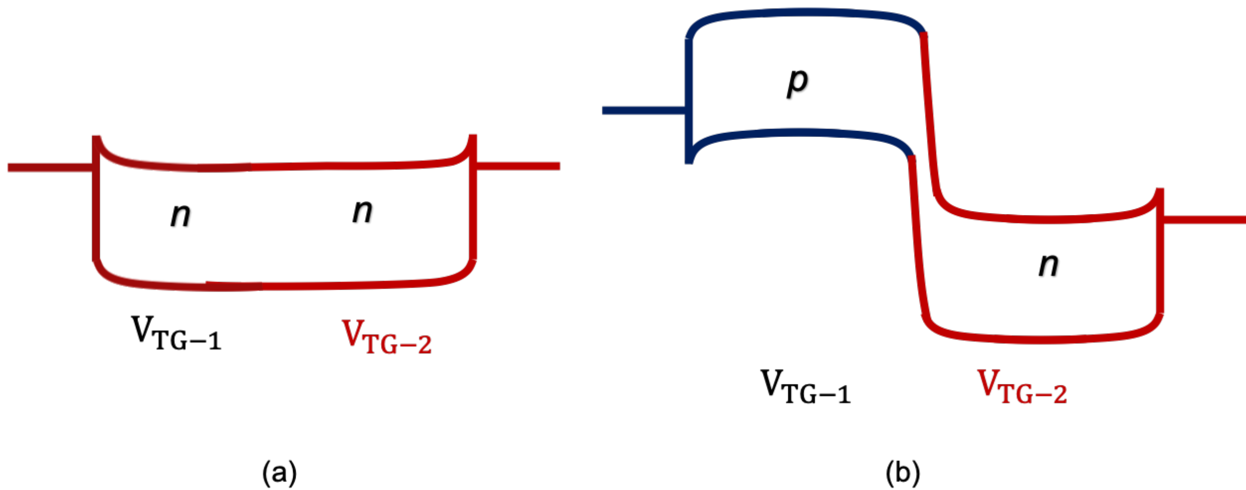


Figure 3.7-4 Both arrangements of band diagram through electrostatic doping (a) showing the MOSFET operation (it could be reversed to p-p arrangement). (b) tunneling FET operation (could be reversed to n-p arrangement).

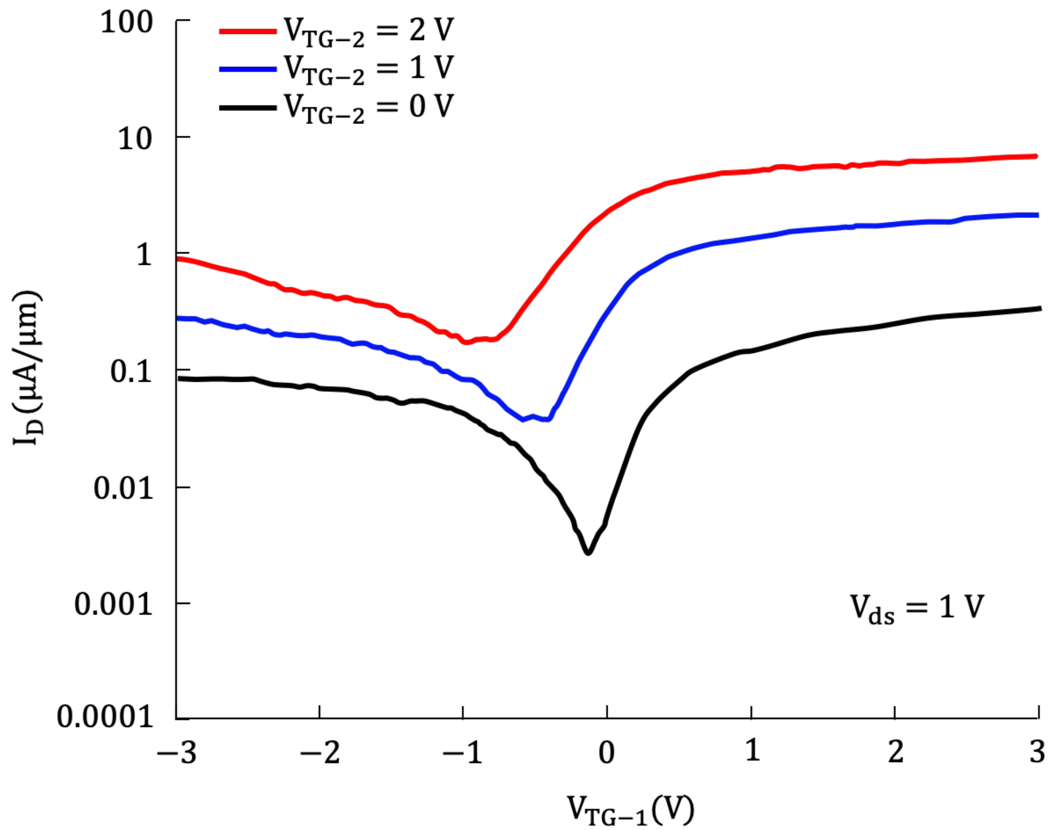


Figure 3.7-5 the transfer characteristics of our TFET device. It is shown that as we sweep V_{TG-1} the area underneath is electrostatically doped between +3 V (n) and -3 V (p) regions, and the device operation moves from regular N-MOSFET (right branch) to P-TFET (lift branch)

Figure 3.7-5 shows the transfer characteristics of our TFET device. It is shown that as we sweep V_{TG-1} the area underneath is electrostatically doped between +3 V (p) and -3 V (n) regions, and the device operation moves from regular N-MOSFET to P-TFET, figure 3.7-6. For example, when we set V_{TG-2} to 2V (red curve), and sweep V_{TG-1}, we can see that at around -1 V the device transition from n type MOSFET operation in the range from -1 V to +3 V to P-TFET operation in the range from -1 V to -3 V. We will call the branch of the FET operation the charge carrier injection branch, while we will call the branch on the lift, the tunneling current branch. The V_{ds} of the device is set at 1 V. Inspecting the tunneling branch of the device we can see that it has a high saturation current of 1 uA/um for -3 V of V_{TG-1} at 1V of V_{TG-2}. This high on tunneling current

shows the extreme suitability of black phosphorus to TFET application, if we compare this value with its closest contender of 2d materials, which is WSe_2, we can see that the record reported value of the saturation tunneling current is on the order of $10^{-5} uA/um$ [98].

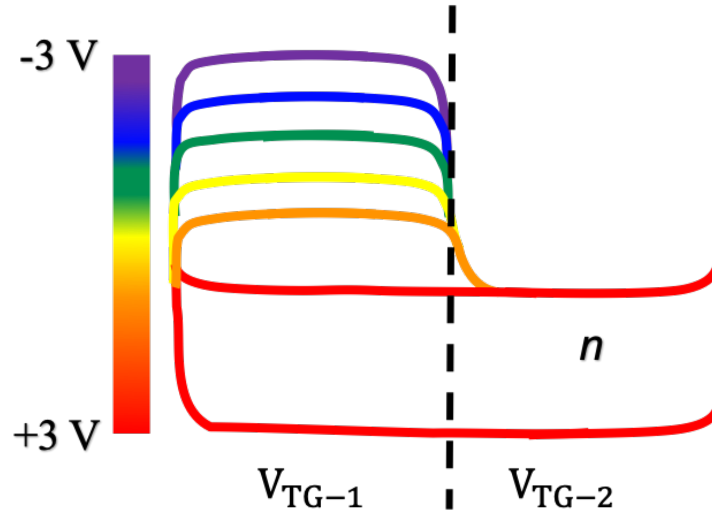


Figure 3.7-6 The modulation of the conduction band profile from p type (purple) to n type (red) by sweeping V_{TG-1} between -3 V and +3 V

Theoretical prediction of black phosphorus T-FET have shown that the ON current value of bp TFET could reach as high as 100 uA/um with aggressive channel scaling and thickness optimization [92]. The increase of current in both branch upon stepping up V_{TG-2} id due to the fact that the device is being doped with more charge carriers upon applying more gate potential. The other metrics have poor values, such as the ON/OFF ratio of the device is on the order of 100, and the subthreshold swing of the device is on the order of 800 mv/dec in the case of lower doping values of V_{TG-1} and fixing V_{TG-2} at 0 V. A major point of this transfer characteristic that it does not rule out the holes injection as being a possible reason for the tunneling branch instead of band-to-band tunneling current. Temperature dependence measurement would answer the question of the conclusiveness of whether that tunneling branch is truly due to BTBT mechanism, or other non-tunneling mechanism. We therefore fabricated another patch of black phosphorous TFET device with three aims, 1) to have better device metrics, 2) answer the question of the origin of the

tunneling current through temperature dependence measurement, and 3) investigate the effect of crystal orientation of the black phosphorus on the device performance, in other word, would aligning the TFET device along the armchair direction or zigzag direction will yield any significant differences. Figure 3.7-7 shows the optical microscopic image of the new TFET device. In order to insure normalized crystallinity study, we have fabricated both devices on the same black phosphorus flake.

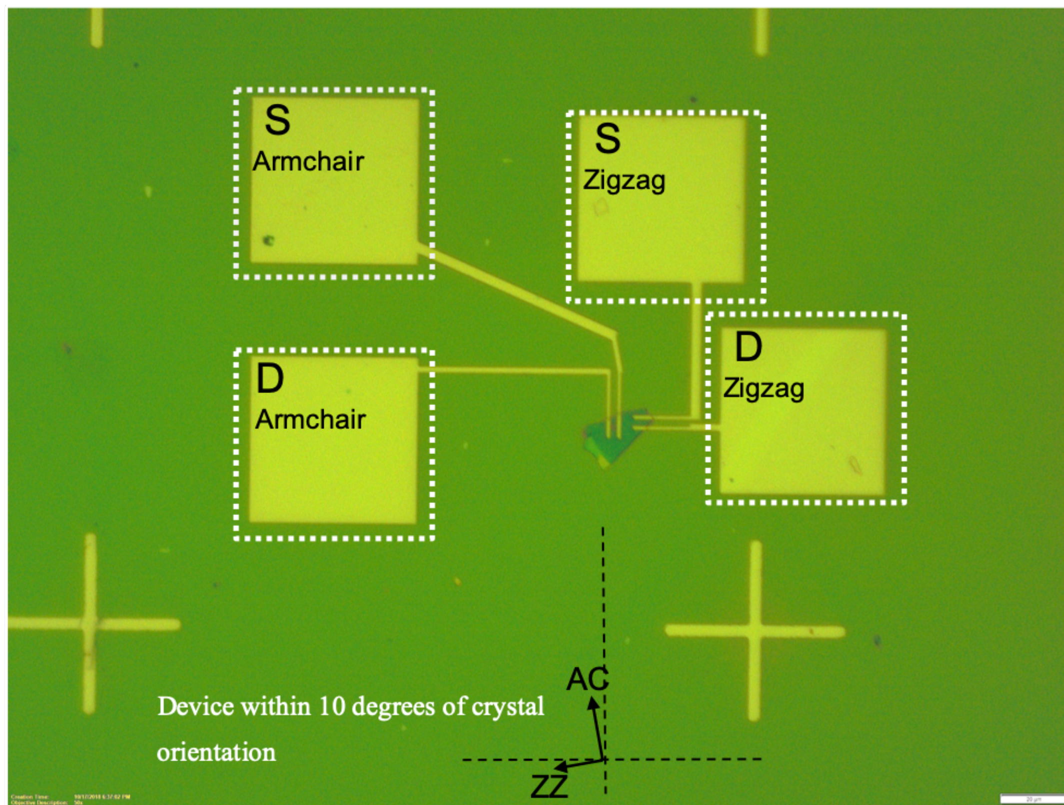


Figure 3.7-7 The optical microscopic image of the crystal-oriented TFET device between armchair and zigzag direction, the error of direction is 10 degrees,

The crystallinity direction was determined by a polarized Raman measurement, we have determined to 10 degrees error the direction of the crystal between armchair and zigzag, the armchair and zigzag direction are normal to each other, figure 3.7-8 shows the angle resolved Raman spectra of the A_{2g} peak with respect to the silicon. Followingly, we perform the microalignment of the device to place the contact in the middle of the channel area, figure 3.7-9

shows the structure with the microaligned contacts in the middle of both the armchair and zigzag direction.

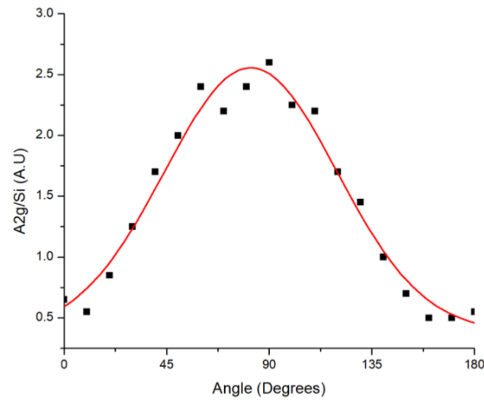


Figure 3.7-8 the angle resolved Raman spectra of the A_{2g} peak with respect to the silicon to detect the orientation of the crystal.

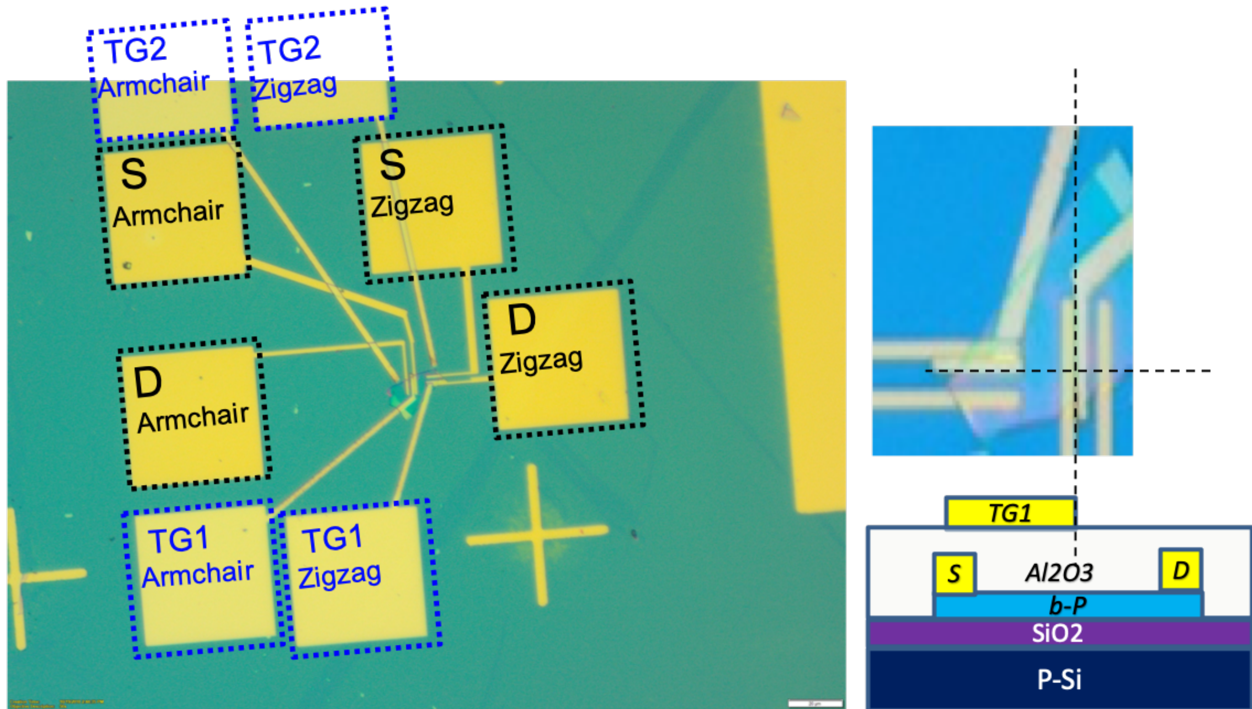


Figure 3.7-9 The structure with the microaligned middle top contacts in the middle of both the armchair and zigzag direction

As we did with our previous device, we finalize with a shadow deposition process in order to form a gap for each of the device directions, we had to perform the process of each of the devices on a separate fabrication process since it would be difficult to control the shadow deposition on both directions at the same time, however other processes of the core FET fabrication, and microalignment of the middle contact was done simultaneously. We then encapsulate the whole structure with 50 nm of Al2O3, and then processed the regions on top of the contact with hydrofluoric acid to insure best conductivity with our probe station probes. Figure 3.7-10 shows the final structure of our crystal-dependent few-layer black phosphorus FET.

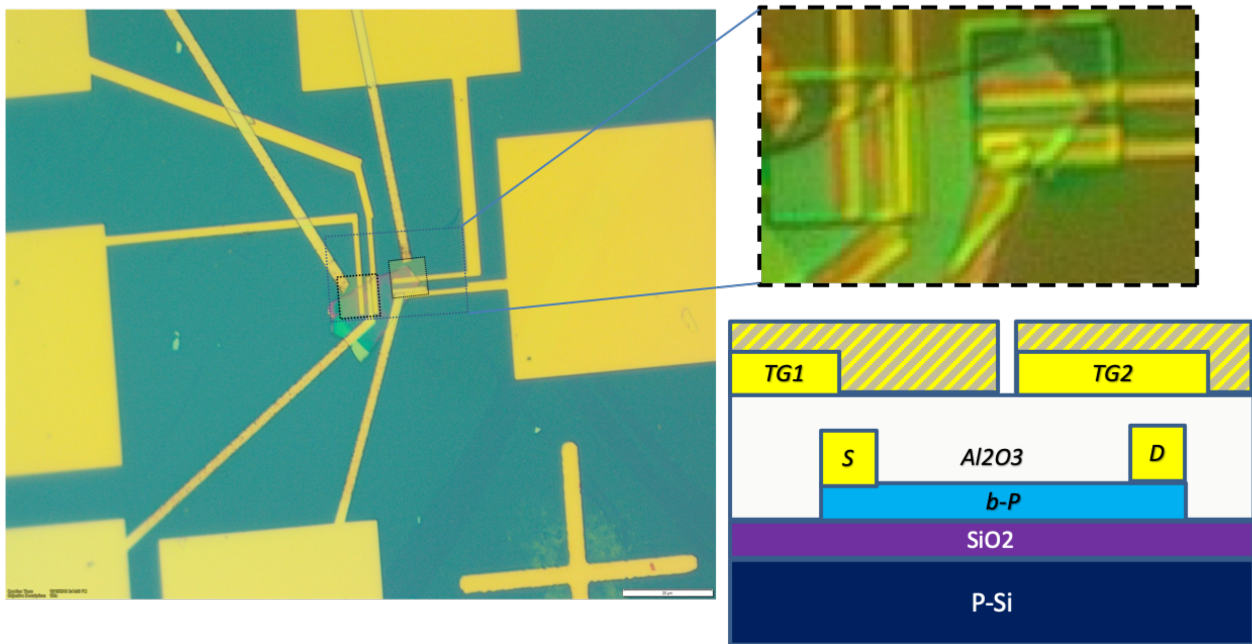


Figure 3.7-10 the final structure of our crystal-dependent few-layer black phosphorus FET after performing the shadow deposition

The fabrication process is essentially similar to what was prescribed in previous sections, however, a modification to the top oxide layer was performed, we have replaced our previous recipe with a lower temperature (90°C) ALD deposition, this temperature reduction was important to protect the black phosphorus from degradation due to the high temperature process, which was magnified due to the presence of water in the ALD process. This has insured a better interface between the top

oxide and the channel material, which was evident by the transport data we acquired from the device. Figure 3.7-11 shows the transfer characteristic of our TFET device on the armchair direction, while figure 3.7-12 shows the transfer characteristic of our TFET device on the zigzag direction, and figure 3.7-13 shows the combined data of armchair and zigzag direction.

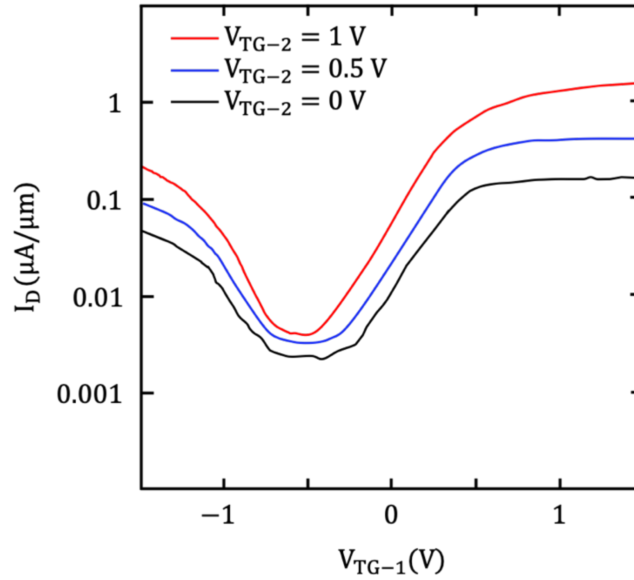


Figure 3.7-11 the transfer characteristic of our TFET device on the armchair direction showing the MOSFET branch from -0.5 V to 1.5V, and the tunneling branch from -0.5 V to -1.5 V

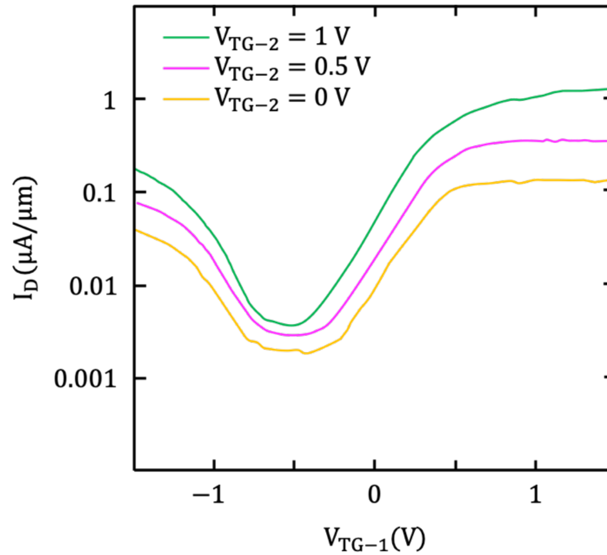


Figure 3.7-12 the transfer characteristic of our TFET device on the zigzag direction showing the MOSFET branch from -0.5 V to 1.5V, and the tunneling branch from -0.5 V to -1.5 V, the current levels are smaller by a factor of 2 when compared to the armchair direction.

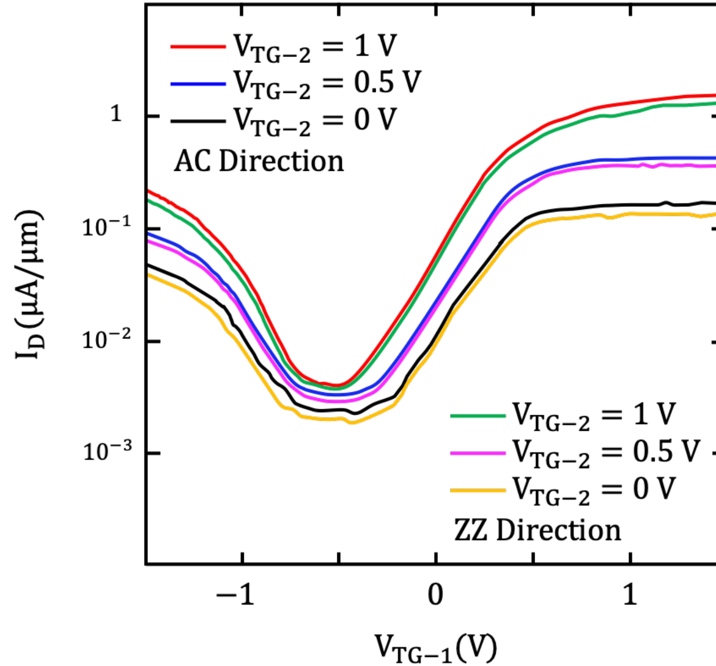


Figure 3.7-13 the combined transfer characteristic along armchair and zigzag direction

As figure 3.7-11 shows, the transfer characteristic of the armchair direction TFET device has also a similar behavior and principle of operation to our previous device, , when we set V_{TG-2} to 1 V (red curve), and sweep V_{TG-1}, we can see that at around -0.5 V the device transition from n type MOSFET operation in the range from -0.5 V to +1.5 V to P type TFET operation in the range from -0.5 V to -1.5 V. As we did with the previous device, we will call the branch of the FET operation the charge carrier injection branch, while we will call the branch on the lift, the tunneling current branch. The V_{ds} of the device is set at 1 V. Inspecting the tunneling branch of the device from -1.5 V to -0.5V, we can see that it has a saturation current of 0.5 uA/um, and an ON/OFF ratio of 2 orders of magnitude, the subthreshold swing is on the order of 180 mV/dec. In the charge carrier injection branch, in the range from – 0.5 V of V_{TG-1} to 1.5 V, we see a saturation current of 1 uA/um, an ON/OFF ratio of $10^3$and a subthreshold swing of the order 105 mV/dec. At every doping step of V_{TG-2}, the sweeping of V_{TG-1}yielded the same behavior. For the zigzag direction, we remarkably see a similar behavior to the armchair direction, with a reduced current level. The

reduction in current levels due to the anisotropic nature of black phosphorus structure. The effective mass anisotropy has a consequence on the current level, the reduction was in the factor of 2 for both branches, which is similar to reported studies about the transport anisotropy of black phosphorus[88,89]. The ON/OFF ratio was also similar to that of the armchair direction of 10^2 for the tunneling branch and 10^3 for the MOSFET branch. The subthreshold swing was in close proximity to that of the zigzag direction and it was in the order of 185 mV/dec for the tunneling branch, and 108 mV/dec for the MOSFET branch. Temperature dependence measurement was performed on the device to investigate the negative bias branch current origin. Figure 3.7-12 shows the temperature dependence data of the device at 300k, 200k, and 100k, respectively.

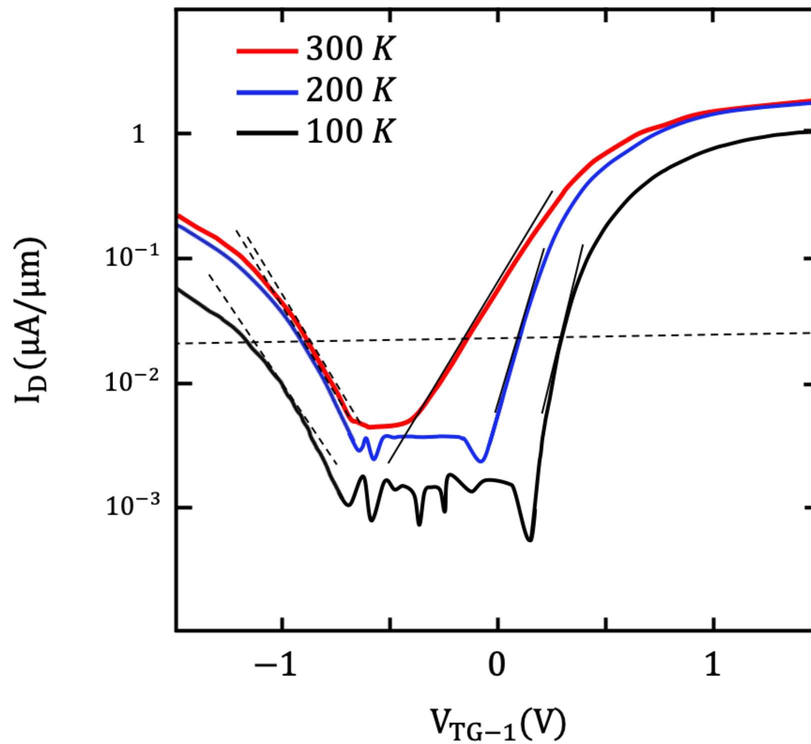


Figure 3.7-14 the temperature dependence data of the device at 300k, 200k, and 100k, respectively along the armchair direction. The MOSFET branch of the curve shows a strong temperature dependence, which is evident by the strong slope change. The tunneling branch shows very little temperature dependence which is evident by the fixed slope.

We can from the temperature dependence data that the device work on two different mechanism between the tunneling branch (TFET) and the thermionic branch (MOSFET). In the MOSFET branch the device is strongly dependent on temperature which is due to the fact that injected carriers are thermionically energized, the dependence appears strongly on the subthreshold swing value, which was reduced greatly as we increased the temperature. Contrary to that, the current in the tunneling branch has a weak dependence on temperature, which is evident by the very small change in subthreshold swing value, which prove that current is not thermionically energized, and that what controls the current is biasing field, figure 3.7-15 shows the SS extracted at constant current level values against temperature for both, the MOSFET operation and T-FET operation. It is important to note that the SS values in the graph does not contain the lowest SS we detected, since we measured all SS values at the same current values.

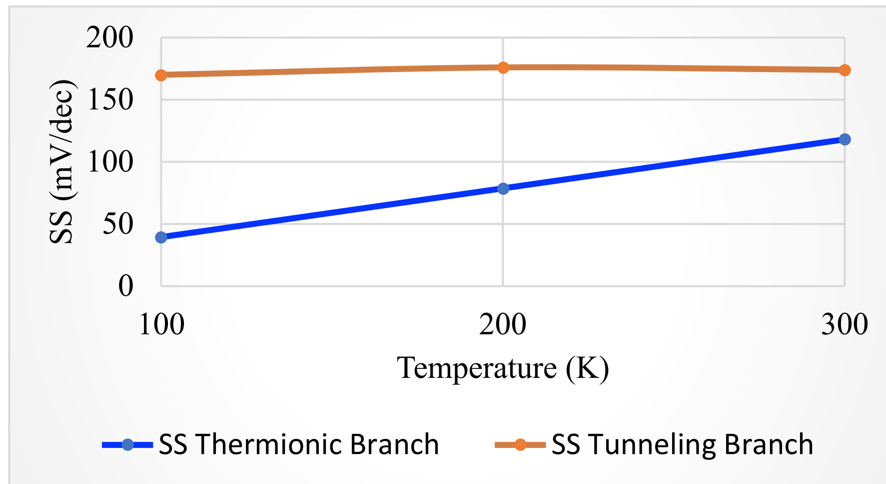


Figure 3.7-15 shows the subthreshold swing value extracted at constant current level values against temperature for both, the MOSFET operation and T-FET operation, with the MOSFET operation showing a strong temperature dependence, while the tunneling operation shows very little temperature dependence.

The temperature dependence transfer characteristic has also yielded another important point, which is the reduction of the off current due to the suppression of the thermionic injection from the drain, and also due to the subdual of trap-assisted transport. The off current in the temperature

dependence data could give us an insight about the activation energy of the device and therefore the bandgap of the channel, please note that at any point of the device fabrication there were no direct measurement of the channel thickness, it is a sacrifice that we took in order to keep the exposure level of the device as minimum as possible, and to always keep in an inert environment, it is rather difficult to estimate the bandgap of the flake without knowing the thickness, alternatively, we estimate the thickness depending on the color contrast of the flake from the optical microscope. However, activation energy measurement could supplement that information and could give us an insight about the bandgap, and possible thickness of the channel material form the off current temperature dependence measurement. Figure 3.7-16 shows a schematic of the activation energy in terms of the band gap of the device.

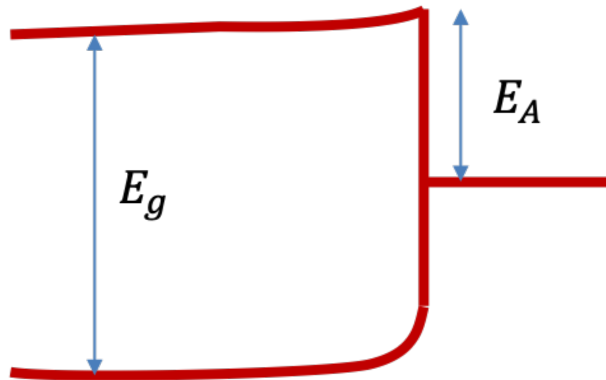


Figure 3.7-16 Schematic showing the relation of activation energy to the bandgap of the material.

The activation energy is the energy that is required to conduct the minimum current, in our transfer characteristic the minimum energy required for conduction takes place at the exact off current. The activation energy is double the bandgap

$$E_g = 2\,E_A \tag{3.7.2}$$

In other word, in order to achieve the minimum OFF current, the energy level should be exactly in the middle of the band gap to ensure the farthest distance either to electron to pass over the conduction band barrier, or holes to pass over the valance band barrier. The OFF current is related to the activation energy by the following Arrhenius relation

$$\ln \rho = \frac{-E_a}{2kT}\left(\frac{1}{T}\right) + \ln A \tag{3.7.3}$$

where ρ is the conductivity, T is the temperature, k is the Boltzmann constant, and E_a is the activation energy. The following figure 3.7-17 shows the Arrhenius relation of our device, if we fit the previous equation into that plot we can deduce E_a to be 0.13 eV, which means that the bandgap of our black phosphorus TFET is $E_g \approx 0.26\ eV$ which is equivalent to the reported black phosphorus bandgap of more than 5 layers.

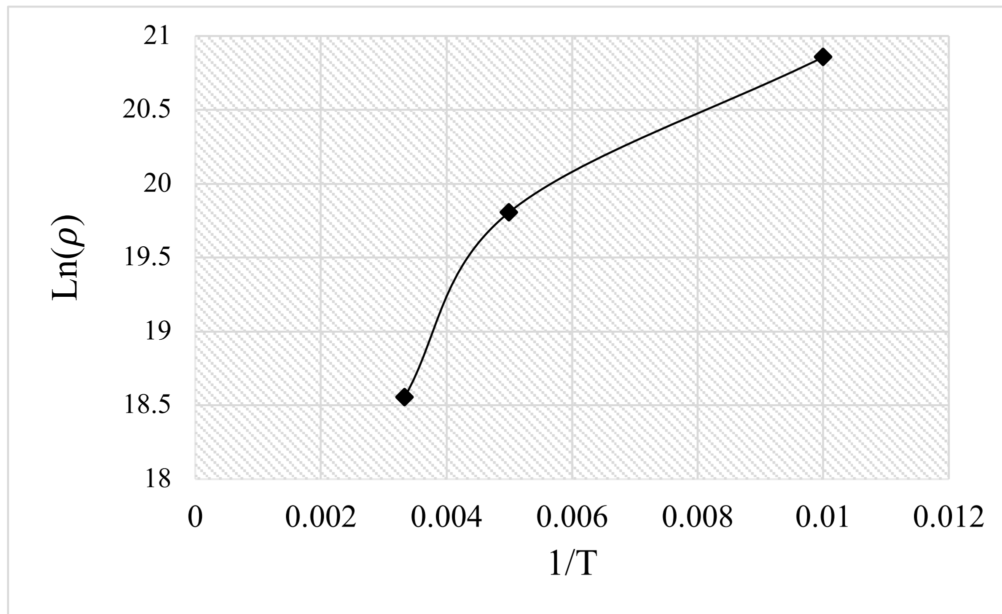


Figure 3.7-17 the Arrhenius relation of our T-FET device, the conductivity was extracted from the ohms law off-current with the corresponding voltage value, in the transfer characteristics, the activation energy fitting was done only on the lower temperature values.

Black phosphorus and 2D materials T-FET have been reported before with the majority having vertical structure rather than lateral structures that is similar to our device. Table 3.7-1 shows a survey of the current 2d and black phosphorus TFET devices. The type of structure can be categorized into 2 types, a vertical heterostructure type, and a lateral/planar TFET structure. The vertical structure yields the best saturation ON current, which is due to the atomic nature of the tunneling distance in the vertical structure, while in planar structures, the tunneling needs to travel more distance which compromise the current level. However, it is important to note, that in vertical structure, the pn junction is not clearly defined, and it would almost be represented as a sharp delta function, which means that what dictate the current movement is the probability of carriers being on either side of the junction. However, in lateral junction, the pn junction is clearly defined, and the electric field directly and evidently affect the tunneling of carriers at the pn junction. It is apparent that our SS is still above the thermionic limit, and our ON/OFF ratio still lags other reported studies. The reason for our tunneling device operating above the 60 mV/dec is due to the combination of oxide capacitance and drain capacitance not being in the ideal values. If we inspect the following equation

$$\mathrm{SS} = \left(\frac{\partial \log \mathrm{I_d}}{\partial \mathrm{V_{gs}}}\right)^{-1} = \ln 10 \left(\frac{\partial I_d}{\partial V_{gs}} \frac{1}{I_d}\right)^{-1} = \ln 10 \left(\frac{\partial I_d}{\partial \varphi_f} \frac{\partial \varphi_f}{\partial \varphi_g} \frac{\partial \varphi_g}{\partial V_g} \frac{1}{I_d}\right)^{-1}$$

With the chain rule parameters for the ideal case inside the bracket correspondent to

$$\frac{\partial I_d}{\partial \varphi_f} = \frac{-I_d}{KT} \quad , \quad \frac{\partial \varphi_f}{\partial \varphi_g} = 1 \quad , \quad \frac{\partial \varphi_g}{\partial V_g} = -e$$

The device is not operating in the ideal case since the effect the gate potential to the barrier potential is not ideal, specifically the term $\frac{\partial \varphi_f}{\partial \varphi_g}$ and losses along the oxide capacitance and drain capacitance are bound to take place. If we inspect the equation for the subthreshold swing with the capacitance terms included

$$SS = \frac{kT}{q}\ln(10)\,[1 + \frac{C_d}{C_{ox}}]$$

So in order to be around the 60 mV/dec, these 2 conditions must take place

$$C_d \rightarrow 0 \quad and \quad C_{ox} \rightarrow \infty$$

In other word, any parasitic capacitances or the deviation of the drain and oxide capacitances, should also deviate the SS from the 60 mV/dec limit. Possible degradation of the black phosphors surface, the imperfection of the oxide/black phosphorous interface, and the quality level of the oxide layer are the most important parts that has caused our device to operate above the thermal limit.

Table 3.7-1 survey of the current 2d and black phosphorus TFET devices

Structure Material	Saturation Current	ON/OFF Ratio	Subthreshold Swing(TFET)	Channel Thickness	Reference
Lateral bP	0.2 uA/um	100	600 mV/dec	> 40 nm	[134]
Lateral bP	0.6 uA/um	1000	170 mV/dec	7 nm	[135]
Vertical bP	15 uA/um	100	187 mV/dec	14 nm	[136]
Vertical bP/SnSe2	10 uA	-	-	N/A	[137]
Split gate lateral bP	0.5 uA/um	1000	170 mV/dec	12 nm (estimated)	This work

We believe, that with more scaling of the channel, and therefore scaling of the electrostatic length through manipulation of the oxide thickness and black phosphorus thickness we can decrease the tunneling distance. However, we have to bear in mind, that as we reduce the body thickness of black phosphorus, we are also going to different level of band gap, which might be out of the goldilocks zone of the TFET. Chen et al have calculated the optimum point of thickness and design and found that 3-layer black phosphorus will correspond to 0.5 eV, and when combined with lateral TFET structure it could yield to ON current of more than 1000 uA/um, ON/OFF ratio of 10000

and SS of 10 mV/dec[138]. It has been shown that negative deferential resistance appears in the TFET conduction mode to further solidify the evidence that a tunneling phenomenon is taking place[136] . However, in our device, we don't see any negative differential resistance due to the fact that NDR appears in the n-type mode operation of TFET under strong forward bias[136], whereas our device operate in the p-type TFET operation under moderate levels of gate sweep bias. The thickness of our bP could be extracted from DFT studies, and experimental studies that is studying the correlation between the black phosphorus thickness and the corresponding ON/OFF ratio, and subthreshold swing[113,139]. Hence, we could insert our values in those theoretical models to give us a good estimate about the thickness of our material. Figure 3.7-18 shows the theoretical model relation between the ON/OFF ratio and the material thickness, our value of 1000 for the ON/OFF ratio corresponds with 12 nm of black phosphorus, which is around 22 layers. This was also supported by figure 3.7-19 where it surveys the ON/OFF VS the bp channel thickness, and inserting our values in the graph, which shows an agreement of the estimated 12 nm of our material thickness.

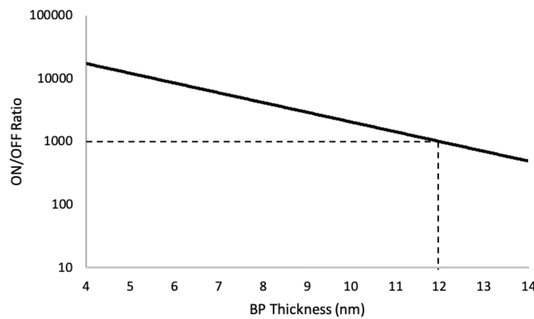


Figure 3.7-18 Theoretical models from (150, 151). Shows the relation between the ON/OFF ratio with the bp thickness, our device corresponds to 12 nm of thickness.

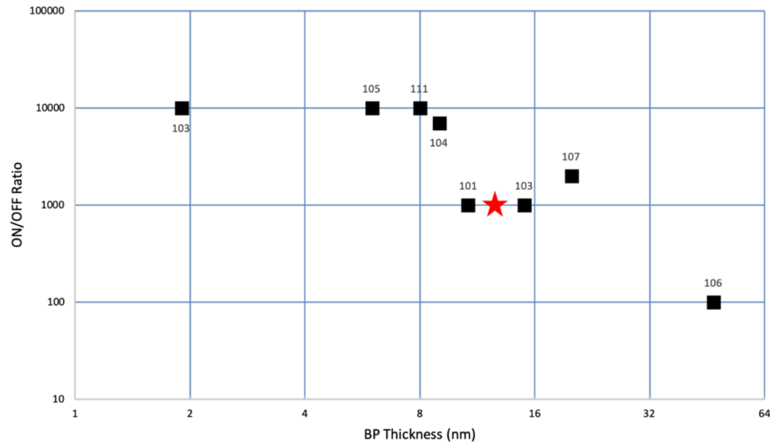


Figure 3.7-19 Survey of all bP top-gated devices that has both the information of the ON/OFF ratio, and the thickness of the channel, the red star is our work value which corresponds also to the bracket of thickness between (10 and 15 nm) which encloses with the theoretical estimate of 12nm from the previous graph.

We will also look at the relation between the subthreshold swing and the thickness of the material in a similar manner to what we did to the ON/OFF vs thickness. We will also apply the theoretical model to plot SS vs channel thickness, and we will insert our point of SS to see the correspondence to the material thickness, figure 3.7-20 shows that relation and the intersection point of our value with 12.4 nm, a remarkable agreement with the previous model. In figure 3.7-21, we show a survey plot of the all bp publication that published SS values and characterized the thickness at the same time, we can see that our device value of 181 mV/dec falls in the region around 12 nm of thickness.

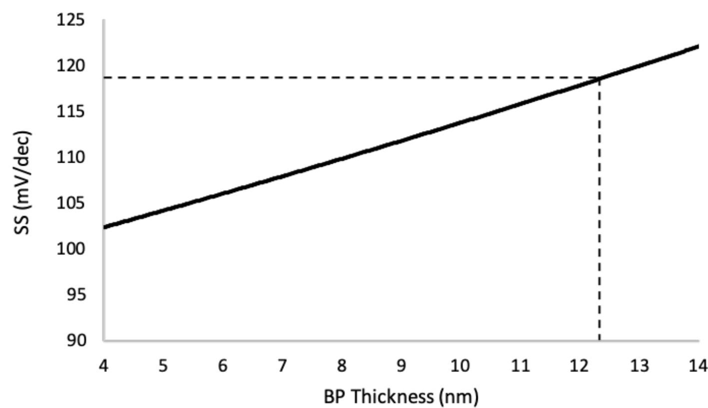


Figure 3.7-20 Theoretical models from (150, 151). Shows the relation between the SS with the bP thickness, our device corresponds to 12.4 nm of thickness.

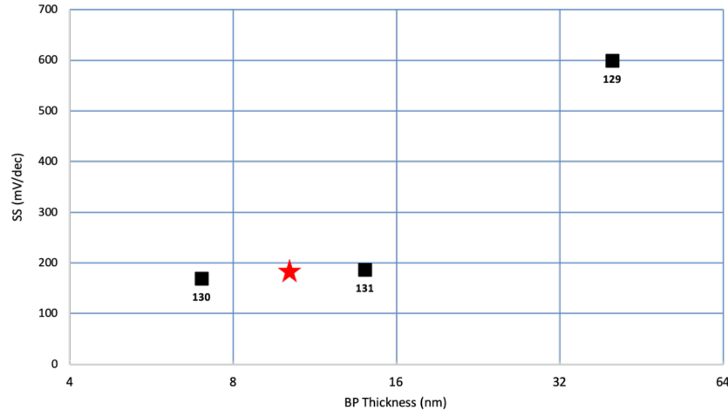


Figure 3.7-21 Survey of all bP top-gated devices that has both the information of the SS, and the thickness of the channel, the red star is our work value which corresponds also to the bracket of thickness between (7 and 15 nm) which encloses with the theoretical estimate of 12.4nm from the previous graph.

In terms of the bandgap, the black phosphorus bandgap as mentioned in previous section is highly modulated with the number of layers, especially in the first 5 layers, it is then believed that the bandgap modulation trend slows down exponentially toward the bulk value of 0.3 eV, so we can safely estimate that the bandgap of the material is between 0.3 and 0.4 eV. Figure 3.1-1 in section 3.1 shows a plot of the relation between the bandgap and the number of layers.

4 Conclusion

In this work, we have investigated the utilization of few-layer black phosphorus material as the channel material of a tunneling field effect transistor device. We reported experimental results on lateral tunnel field effect transistor device, with band to band tunneling transpiring at the electrostatically doped pn junction through a split gate structure. The split gate structure had a minimum physical gap to increase the probability of tunneling and transmission which was realized by the process of microalignment and shadow deposition. We demonstrated high ON current densities, and enhanced room-temperature subthreshold swing through an aggressive optimization of the foundational field effect transistor device. A temperature-dependence, along with crystal orientation dependence of the T-FET device was investigated. In the armchair direction, The MOSFET branch of the device demonstrate saturation current of up to 1 μA/μm and subthreshold swing of 128 mV/dec at room temperature for V_{ds} = 1 V, while the tunneling branch exhibited saturation current of up to 0.45 μA/μm and subthreshold swing of 185 mV/dec at room temperature for V_{ds} = 1 V. Our zigzag oriented device had a comparable result, the MOSFET branch of the device demonstrated saturation current of up to 1 μA/μm and subthreshold swing of 135 mV/dec at room temperature for V_{ds} = 1 V, while the tunneling branch exhibited saturation current of up to 0.45 μA/μm and subthreshold swing of 187 mV/dec at room temperature for V_{ds} = 1 V. Temperature-dependence measurement of the armchair direction device at 100, 200, and 300K have shown strong dependence of the MOSFET branch on temperature, while very little change of the subthreshold swing value took place when temperature was manipulated. Current densities of the order of 10^4 A/cm^2 have been realized in the tunneling branch of both crystal orientation. In this thesis, and after presenting the current state of micro- and Nano-electronics in the first part of thesis, we discussed the importance of scaling and power consumption. In the following 2 sections of the first chapter, we have discussed the short channel effect that arise from

the aggressive scaling of the channel length and slower switching which arise from the limitation of the thermal SS value of 60 mv/dec. We then discussed the applicability of 2D materials, which is inherently immune to short channel effect due to their short electrostatic length, in nanoelectronics from a material point of view. We also have discussed the applicability of tunnel field effect transistor design as oppose to the regular MOSFET design to get over the switching speed limitation of 60 mv/dec. We then proposed the idea of combining 2d materials, with the design structure of the tunnel field effect transistor. In Chapter 2, we discussed the electrophysical properties of two-dimensional materials in general, and two-dimensional semiconductors in particular such transition metal dichalcogenides (TMDCs) and elemental black phosphorus. A brief on the conventional and most recent approaches in controlled preparation and growth methods was presented. A discussion on the rule of two-dimensional semiconductors in the micro- and nanoelectronics applications will follow. Finally, A holistic view of the most persistent challenges that faces two-dimensional electronics such as electrical contacts, scattering of the charge carriers, and most-importantly, short channel effect in two-dimensional materials. In Chapter 3, we presented the work of tunnel field effect transistor based on few layer black phosphorus as a channel material. We presented our work in achieving excellent FET performance as a gateway for the ultimate goal in achieving excellent low energy consumption TFET performance, given the extremely unstable nature of the material during fabrication. We discussed the device design and the fabrication procedures. Followingly, we discussed the work done in terms of micro-alignment of the split gate structure, along with the shadow deposition process, in order to achieve minimal physical gap between the split gate structure. Finally, we presented the electronic characteristics of the device with a temperature dependence as well as crystal orientation dependence. Energy efficient tunneling device research is an important path that many famous research group around the world are pursuing, considering the issue of scaling, power

consumption, and switching speed, while at the same time considering the potential and variety of 2D materials and T-FET device structure, one could speculate that achieving energy-efficient, high-performance, high-storage, low-cost, flexible, and transparent devices are within reach of the technological industry.

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