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Design and Automation for High Fidelity Flexible Hybrid Electronics

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in

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by

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To my family for their love and support.

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Curriculum Vitæ

Leilai Shao

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Publications

[1] **Shao, L.**, Lei, T., Huang, T. - C., Bao, Z., and Cheng, K. - T., "Robust Design of Large Area Flexible Electronics via Compressed Sensing", in 57th Design Automation Conference (DAC), 2020.

[2] **Shao, L.**, Huang, T. - C., Lei, T., Chu, T.-Y., Bao, Z., Beausoleil, R., Wang, M. and Cheng, K. - T., "Compact Modeling of Thin Film Transistors for Flexible Hybrid IoT Design", in IEEE Design & Test, 2019.

[3] **Shao, L.**, Li, S., Lei, T., Huang, T. - C., Beausoleil, R., Bao, Z., and Cheng, K. - T., "Ultra-thin Skin Electronics for High Quality and Continuous Skin-Sensor-Silicon Interfacing", in 56th Design Automation Conference, 2019.

[4] Y. Wang, **Shao, L.**, Lastras-Montano, M. Angel, and Cheng, K. - T. Tim, "Taming Emerging Devices' Variation and Reliability Challenges with Architectural and System Solutions", in 32nd IEEE International Conference on Microelectronic Test Structures (Invited Paper), Kita-Kyushu City, Japan, 2019.

[5] T. - C. Jim Huang, Lei, T., **Shao, L.**, Sivapurapu, S., Swaminathan, M., Li, S., Bao, Z., Cheng, K. - T. Tim, and Beausoleil, R. G., "Process Design Kit and Design Automation for Flexible Hybrid Electronics", in Design Automation And Test in Europe (Invited Paper), Florence, Italy, 2019.

[6] Lei, T., **Shao, L. (Co-first)**, Zheng, Y., Pitner, G., Fang, G., Zhu, C., Li, S., Huang, Beausoleil, R., Wong, H. - S., Huang, T. - C., Cheng, K. - T., and Bao, Z. *"Low-voltage High-performance Flexible Digital and Analog Circuits based on Ultrahigh-purity Semiconducting Carbon Nanotubes"*, in **Nature Communication**, 2019.

[7] **Shao, L.**, Lei, T., Huang, T. - C., Beausoleil, R., Bao, Z., and Cheng, K. - T., "Compact Modeling of Carbon Nanotube Thin Film Transistors for Flexible Circuit Design", **Best Paper Awards Nomination**, in Design, Automation and Test in Europe (DATE), Dresden, Germany.

[8] **Shao, L.**, Lei, T., Huang, T. - C., Beausoleil, R., Bao, Z., and Cheng, K. - T., "Process Design Kit for Flexible Hybrid Electronics", (Invited paper) in in 23rd Asia and South Pacific Design Automation Conference (ASP-DAC).

[9] **Shao, L.**, Chu, T. - Y., Tao, Y., and Cheng, K. - T. Tim, "Fully Printed Organic Pseudo-CMOS Circuits for Sensing Applications", in 1st IEEE International Flexible Electronics Technology Conference (IFETC), Ottawa, Canada.

[10] Huang, T. - C., **Shao, L.**, Lei, T., Beausoleil, R. G., Bao, Z., and Cheng, K. - T. Tim, "Robust Design and Design Automation for Flexible Hybrid Electronics", in International Symposium on Circuits and Systems (ISCAS).

Abstract

Design and Automation for High Fidelity Flexible Hybrid Electronics

by

Leilai Shao

Flexible electronics is emerging as an alternative to conventional silicon electronics for applications such as wearable sensors, artificial skin, medical patches, bendable displays, foldable solar cells and disposable RFID tags. Combining FE with thinned silicon chips, known as flexible hybrid electronics (FHE), can take advantages of both low-cost printed electronics and high performance silicon chips. There exist several challenges before FHE can be broadly employed for next-generation wearable and IoT products. Due to material properties, TFTs are usually mono-type, either only p- or only n-type, devices. Existing CMOS design methodologies for silicon electronics, therefore, cannot be directly applied for designing flexible electronics. To address these challenges, a trustworthy TFT compact model and process design kit (PDK) is needed to facilitate simulations and design explorations.

In the first part, we developed the compact model for thin film transistors, which has been validated extensively with carbon nanotube (CNT), organic and indium gallium oxide (IGZO) devices. The developed model has been implemented in Verilog-A, which can perform co-simulations with silicon chips. With the developed model, we further built the FHE-PDK for flexible thin-film transistors (TFTs) and passive elements, including technology files for design rule checking (DRC), layout versus schematic (LVS) and layout parasitics extraction (LPE), as well as SPICE-compatible models. Wafer scale measurements are used to validate our SPICE models and design rules are derived accordingly to assure a satisfactory yield. With the developed FHE-PDK, we further built the robust Pseudo-CMOS cell library to address the

mono-type design challenges.

In the second part, we focused on addressing FHE system design issues. Specifically, motion noises in the flex-rigid interface and sensor defects in large area sensing system. We proposed the *"active electrode"* (with a thickness $\leq$2 um), which integrates the electrode with a thin-film transistor (TFT) based amplifier, to effectively suppress motion artifacts. The fabricated ultra-thin amplifier can achieve a gain of 32 dB at 20 kHz. The simulation results indicate that the active electrode can significantly improve the signal quality under motion noise (achieving $\geq$30 dB improvement in signal-to-noise ratio (SNR)) and boost classification accuracy by $\geq$19% for atrial fibrillation (AF) detection. We further study robustness issue of ultra-thin flexible electronics caused by inadequate device yield, reliability and stability which is inevitable due to the low temperature requirement for fabrication and the large-area nature of flexible sensing arrays. As signals sensed by body sensor arrays exhibit sparse statistical characteristics, we present a system design solution to leverage the sparse nature via compressed sensing (CS) which can ensure system robustness without relying on highly reliable devices. Specifically, we implement a flexible CS encoder together with the sensor array using carbon-nanotube-based flexible TFTs and decode the compressed signal in the silicon side. Our quantitative analysis, validated through two case studies: temperature imaging and tactile-sensor based object recognition, showed that the proposed robust sensing schema can accommodate up to 20% sparse defects (device defects or transient errors).

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Chapter 1

Introduction

Flexible Electronics (FE) is emerging for low-cost, light-weight wearable electronics, artificial skins and IoT nodes, benefiting from its low-cost fabrication and mechanical flexibility. Combining FE with thinned silicon chips, known as flexible hybrid electronics (FHE), can take advantages of both low cost printed electronics and high performance silicon chips, which brings together flexible form factors and IoT innovations. This chapter introduces background of flexbile hybrid electronics (FHE), motivations of the thesis work, and summary of some related work.

1.1 Status

Despite recent advances in the development of flexible materials, devices and integration [10, 1], it is still challenging to design a disruptive product using flexible hybrid electronics (FHE), as illustrated in Fig. 1.1, which involves multiple FHE vendors, silicon die-thinning and ad-

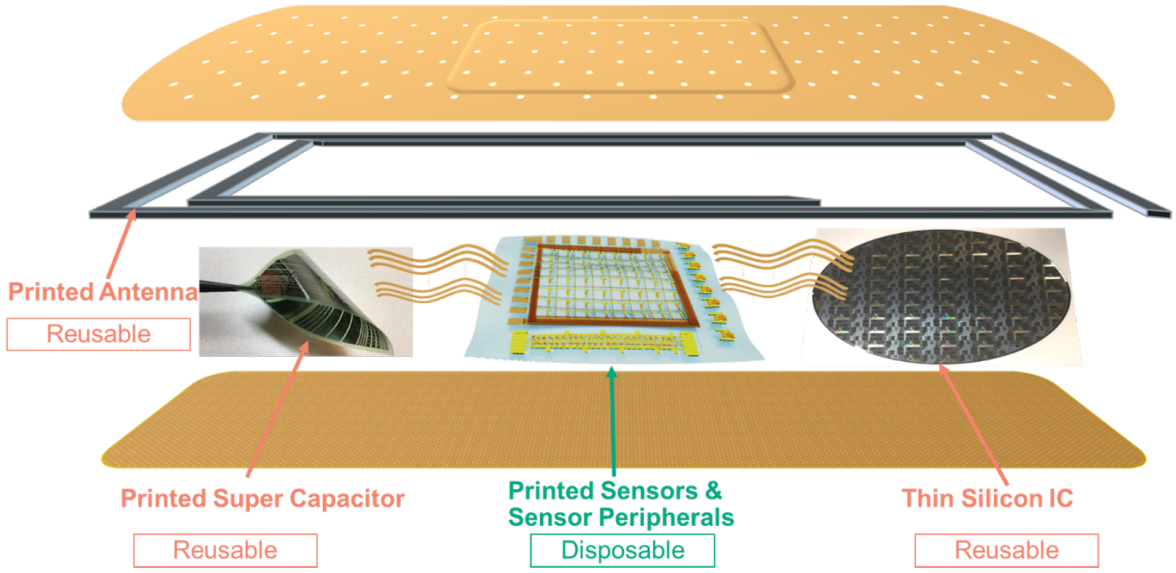


Figure 1.1: A conceptual diagram of an FHE patch that includes printed sensors, sensor peripheral circuits, printed super capacitors, printed antennas and thinned silicon chips, which offers greater comfort (wear-and-forget), enables continuous and non-invasive health monitoring, and could possibly be disposable once it reaches the economy of scale.

vanced packaging to achieve an ultra-flexible and highly-compact form factor and the required electrical specifications at the same time. Besides the large process variations and device defects due to the low cost and low temperature printing process, FHE applications will also involve bending, stretching and twisting scenarios, where the electrical characteristics and circuit performance has to been carefully characterized under different scenarios. To overcome the mentioned design challenges, it will need advanced design automation techniques to alleviate large process variations, mono-type circuit design challenges and heterogeneous integrations through accurate electrical models, robust circuit designs, automatic design rule checking, bending-aware place-and-route and multi-physics analysis.

1.2 Current and Future Challenges

One driving force for advancing the FHE technology is the strong need for thinner, cheaper, and large-area electronics to meet the requirements of flexible displays, healthcare patches, and low-cost internet of things (IoT). With the advances of FHE materials, printing processes, and FHE devices such as thin-film transistors (TFTs), an FHE sensor array, illustrated in Fig. 1.2, has become a reality for a wide range of applications. Among flexible substrates, plastic films such as polyimide (PI), polyethylene terephthalate (PET), or thermoplastic polyurethane (TPU) are popular choices due to their low cost and bendable form factor. However, the process temperature of FHE is thus limited by the melting temperature of the plastic films that is usually lower than 200^oC. The compatible TFT technologies such as organic, metal oxide, and carbon nanotube (CNT) generally suffer from inferior carrier mobility, only mono-type (p- or n-type only) device being available, and encountering large process variation, compared to conventional silicon electronics on silicon wafers. Additive manufacturing such as screen printing, ink-jet printing, or roll-to-roll imprinting, while contributing to lowering the manufacturing cost, limits the minimum feature sizes and the FHE circuit performance. The FHE circuit may also suffer from performance degradation due to continuous mechanical deformation such as bending or stretching. Under the aforementioned constraints and limitations, design optimization including multi-physics modelling and simulation is essential for meeting the performance target under the usage scenarios. The modelling, simulation, and design automation framework for FHE design have advanced enormously in the past few years while there still exists a significant gap between the needs and the current solutions, demanding more R&D efforts in design

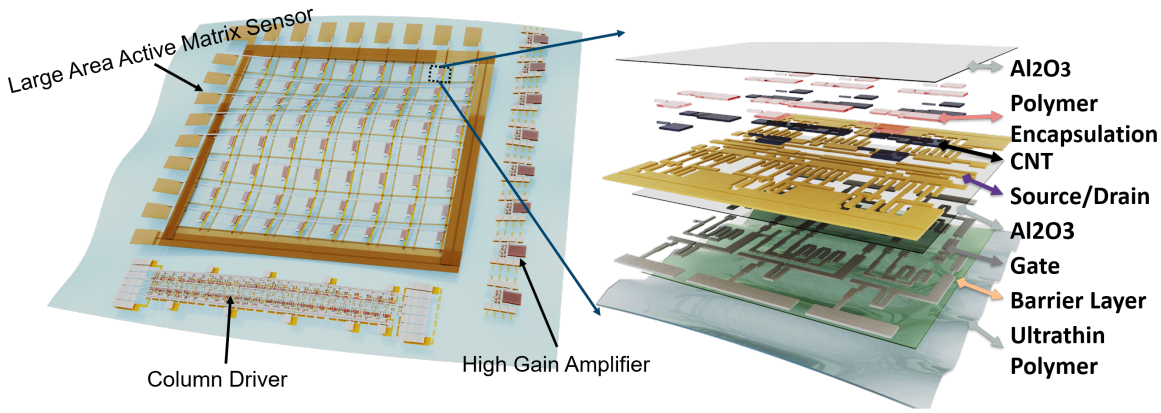


Figure 1.2: (Left) A conceptual drawing of an FHE sensor array that is composed of an array of FHE sensors, driving circuitry, and signal amplification on a thin and flexible substrate [1]. The thickness of the FHE sensor array is usually less than 10um, which enables a conformal form factor for such an array to be applied to non-planar surfaces such as human body. (Right) 3D view of a FHE circuitry that is usually composed of multiple layers of FHE devices such as transistors, resistors, capacitors, and inductors, as well as various sensors and antennas connected by the printed traces and laser or mechanical drilled through-layer vias. The process temperature of FHE is usually lower than 200^oC to accommodate low cost plastic substrates such as PET.

automation to close the gap.

1.3 Advances in Design and Automation to Meet Challenges

Among aforementioned FPE design challenges, addressing the broken link between FPE manufacturing processes and electronic design automation (EDA) tools is considered the most critical task. In silicon CMOS industry, a process design kit (PDK), together with a powerful suite of EDA tools, enables circuit designers to design sophisticated circuits manufacturable by CMOS foundries in large quantities. With a similar vision, a PDK for FPE and flexible

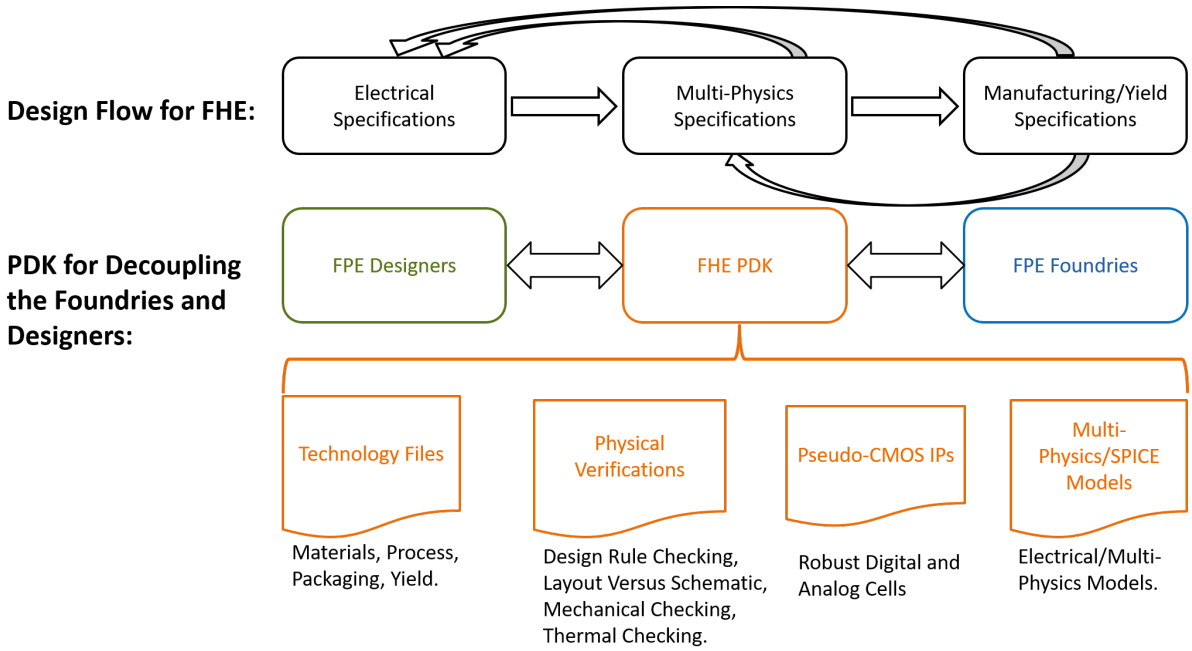


Figure 1.3: Design Ecosystem of Flexible Printed Electronics: The FHE design flow covers electrical designs, multi-physics specifications and manufacturing considerations, which will need multiple iterations to achieve the desired electrical performance, great mechanical flexibilities and a high yield. Process Design Kit (PDK) severs as the interface between foundries and designers, which is aimed to decouple the backend process and FHE designs and reduce the required design iterations and cost.

hybrid electronics (FHE) has been developed recently [11, 12]. FHE, which enhances FPE through introducing heterogeneous integration of thinned silicon chips (ex. $\leq$50um thick) with FPE elements on a flexible substrate, makes desirable features, such as near-sensor computing and wireless communication, feasible. The FHE ecosystem enabled by the PDK is illustrated in Fig. 1.3. The FHE designers can conduct various design simulations under target operating temperatures and bending radii and in turn produce manufacturable design database with the aid of EDA tools and PDK [12, 13]. The PDK could also include FHE process-validated design IP blocks such as Pseudo-CMOS design IP for digital, analog, and power circuits [14] which relieve the designers from tedious and repetitive tasks of handling device-level details. In addi-

tion to the FHE PDK, customized place-and-route (P&R) algorithms for physical design flow is also required in order to accommodate the bending use cases for TFT circuits. The study in [15] relied on a statistical timing analyzer (STA) to identify bending hotspots, and used the derived information together with TFT bending models [16] to generate a hotspot mapping for guiding circuit layout, followed by the cell placer's simulated annealing process for finding the optimized cell placement to minimize timing degradation under bending. The study in [17] further suggested inclusion of both mechanical strain and temperature drift's impacts on TFT circuit's performance in layout optimization. For bending or other use cases that require mechanical deformation or thermal cycles, FHE multi-physics models for electrical, mechanical, and thermal interactions must be comprehensive and accurate in order to derive useful information from multi-physics simulation. A recent study [18] investigated multi-physics 3D finite-element models (FEM) considering both mechanical and electrical aspects of Aerosol jet printed (AJP) and screen printed (SP) transmission lines and power inductors. The results showed strong correlation between FEM and measurement data of AJP transmission lines under flat cases and suggested insignificant changes for insertion loss S21 and return loss S11 under bending. However, there still exist larger discrepancy between FEM and measurement data as well as significant changes for S21 and S11 under bending for SP transmission lines and power inductors, which suggested that FHE multi-physics modelling and simulation methodology are still in the infancy and in need of further research.

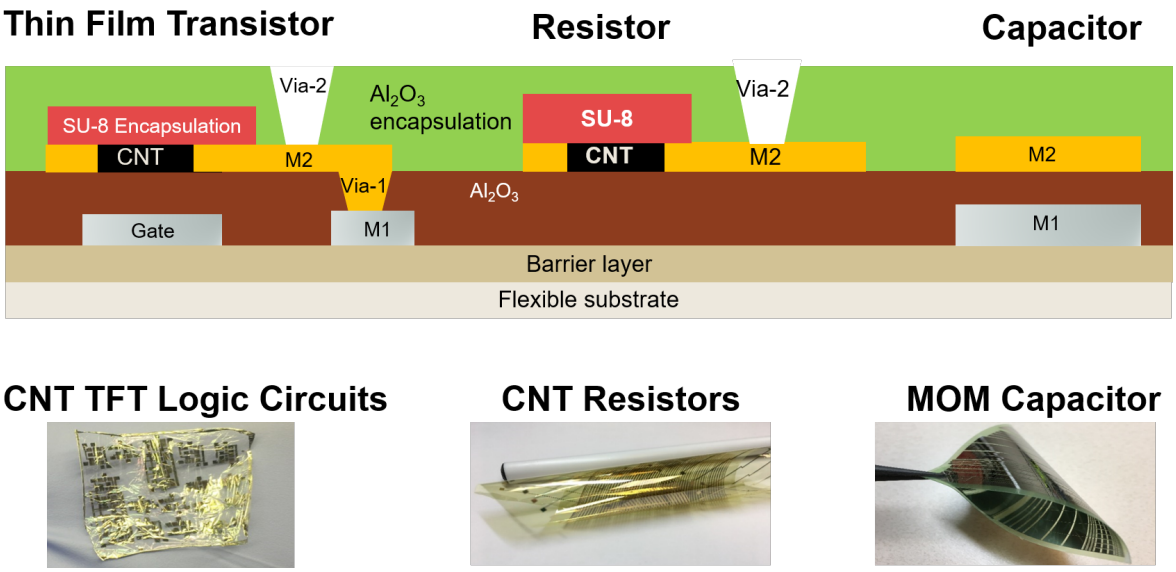


Figure 1.4: Carbon Nanotube based Flexible Electronics

1.4 Carbon Nanotube Based Flexible Electronics

Carbon nanotube (CNT) random network is promising for high-performance flexible thin film transistors (TFTs), as shown in Fig. 1.4, because of its high carrier mobility (25 cm^2/Vs), mechanical flexibility, and solution-compatible processes [19]. Recently developed CNT sorting methodologies in [20][21] enable high-purity semiconducting CNTs and dense CNT networks, which leads to a higher carrier mobility and lower operation voltages. Comparisons among different TFT technologies are shown in Table 1.5, which indicates that CNT-TFT is promising for high-performance low-power flexible applications [22][23][24]. In addition to merits of low-cost manufacturing such as low-temperature and solution-compatible processes, CNT-TFT is recently emerging as an ideal candidate for low-cost wearables and internet of things (IoT) nodes [25]. In Table 1.5, you may also notice that all four different TFT technologies have only either N- or P-type stable devices, which poses another challenge for flexible circuit

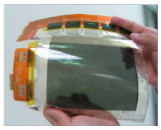
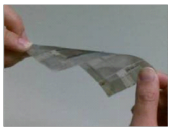
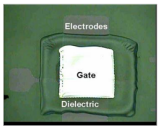
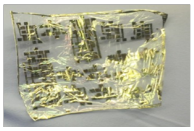
Transistor Technology	Amorphous Si TFT	Metal-Oxide TFT	Organic TFT	Carbon Nanotube TFT
Process Temperature	250 ℃	< 150 ℃	< 100 ℃	Room Temp.
Process Technology	Lithography	Lithography	Ink-Jet/ Shadow Mask	Lithography/ Shadow Mask
Feature Size	8 μm	5 μm	50 μm	2 μm
Substrate	Glass/plastics	Glass/plastics	Wafer/plastics	Wafer/plastics
*Stable Devices	N-type	N-type	P-type	P-type
Supply Voltage	20V	5V	20V	2V
Mobility (cm^2/Vs)	1	15	0.01/0.5 (N/P)	25
				

Figure 1.5: Comparisons of vairous TFT technologies.

design.

1.5 Key Contributions

This thesis mainly aims to address following challenges:

- The lack of accurate models and EDA supports for FHE design flow.
- Robust design of flexible circuits using mono-type devices.
- Improve signal fidelity for bio-signal sensing applications.

To close the existing gap of the FHE design flow, we collaborated closely with Stanford and Hewlett Packard Labs. Based on the CNT process developed by Stanford, we designed the masks for CNT-based flexible devices and circuits. Also, wafer level measurements are con-

ducted to extract key device parameters, process variations and build accurate models. With all these efforts, we successfully built the first Process Design Kit (PDK) for FHE design, including SPICE-compatible compact models for CNT-based flexible capacitors, flexible resistors and flexible CNT-TFTs. Furthermore, scripts are developed to automatic perform the physical verification, including design rule checking (DRC), layout versus schematic (LVS) and parasitic extraction (PEX), to greatly improve the design efficiency.

To address the mono-type circuit design issue, we adopted the Pseudo-CMOS circuit design style, which has been widely used in digital, analog and power circuits based on single type transistors. Also, with the developed PDK and physical verification scripts, we successfully designed high-speed and low-voltage flexible digital and analog cell library, which serves as the foundation of more complex flexible innovations. Based on CNT technology, we successfully pushed the boundary of the state-of-the-art flexible CNT circuit performance in respect of both the speed and circuit complexity.

To improve signal fidelity, we mainly focus on two scenarios: 1. motion noises in the skin-sensor-silicon (SSS) interfacing of wearable applications; 2. Sensor defects in large area sensing array. For motion noises, we propsed the ”Active Electrode”, which integrates the flexible amplifier with the electrode to pre-amplifier the critical signals before entering the flex-rigid interfacing. For device defects, motivated by the sparse nature of the body sensing signals, we adopted the compressed sensing technique and partitioned the sensing system into flex-encoder and rigid-decoder, which keeps the sensing in the flexible domain and pushes the high computation to the silicon domain.

1.6 Thesis Outline

This thesis mainly consists two parts: Chapter 2-4 presents our work on compact modeling, the development of FHE-PDK and Pseudo-CMOS digital and analog cells based on CNT flexible circuits. Chapter 5-6 discusses noises issues and device defects in FHE system design.

Chapter 2 presents compact models for various characteristics of TFTs and passive components. FHE-PDK for flexible thin-film transistors (TFTs) and passive elements, including technology files for design rule checking (DRC), layout versus schematic (LVS) and layout parasitics extraction (LPE), as well as SPICE-compatible models are summarized in Chapter 3. Chapter 4 demonstrates robust Pseudo-CMOS analog and digital cell library.

In Chapter 5, an *"active electrode"* design is proposed to reduce the motion noises in the skin-sensor-silicon interfacing. Chapter 6 the proposed encoder-decoder design for large area FHE sensing applications to alleviate the sensor defects challenge. Lastly, this thesis is concluded by Chapter 7.

Chapter 2

Compact Models for Flexible Electronics

2.1 Introduction

Carbon nanotube (CNT) random network is promising for high-performance flexible thin film transistors (TFTs), as shown in Fig. 5.1, because of its high carrier mobility (25 cm^2/Vs), mechanical flexibility, and solution-compatible processes [19]. Recently developed CNT sorting methodologies in [20][21] enable high-purity semiconducting CNTs and dense CNT networks, which leads to a higher carrier mobility and lower operation voltages. Comparisons among different TFT technologies are shown in Table 2.1, which indicates that CNT-TFT is promising for high-performance low-power flexible applications [22][23][24]. In addition to merits of low-cost manufacturing such as low-temperature and solution-compatible processes, CNT-TFT is recently emerging as an ideal candidate for low-cost wearables and internet of things (IoT) nodes [25].

While CNT-TFT is promising for a wide range of applications, an accurate and yet simple compact model for CNT-TFTs is still missing. Previously reported analysis for CNT-TFTs [19] only focuses on the linear region and does not reflect mobility dependency on the gate voltage and contact effect at source/drain terminals. For CNT random network, the charge transport characteristic is dominated by tube-tube junctions [19][26]. Due to the complexity of the CNT random network, it is infeasible to model all tube-tube junctions using Monte Carlo simulations [27]. In this work, we propose a compact model based on the measurement data and provide validation results of the model with fabricated CNT-TFT devices as well as Pseudo-CMOS logic circuits. The proposed model is implemented in the Verilog-A language, and is compatible with SPICE to explore the design space for Pseudo-CMOS circuit implementations [28][29]. We plan to release this model to allow designers to explore CNT-TFT based flexible circuits and evaluate their potentials.

The main contributions of this work are summarized as follows:

- Developing an accurate SPICE-compatible compact model for CNT-TFTs, which is thoroughly validated using transistor and circuit measurements
- Exploring the design space based on the developed model to analyze the noise margin (NM) and power-delay product (PDP) for flexible circuit design
- Proposing an optimization framework, which enables effective optimization of the NM and PDP for large-scale CNT-TFT flexible circuits

The rest of this work is organized as follows: Section 3.3.2 provides device details and model derivations for CNT-TFTs; Section 2.3 elaborates CNT-TFT model validation against

Table 2.1: Comparisons among different TFT technologies

Device Type (TFT)	Amorphous Si	Metal-Oxide	SAM Organic	Polymer Organic	Carbon Nanotube
Process Temperature	$\sim 250^{\circ}C$	$\sim 150^{\circ}C$	$\sim 100^{\circ}C$	Room temperature	Room temperature
Process Technology	Lithography	Lithography /Roll-to-roll	Shadow mask	Ink-jet	Solution
Feature Size (μm)	~ 8	$\sim$ 2-5	~ 50	~ 50	$\sim$ 2-5
Stable Device Type	N-type	N-type	P-type	P-type	P-type
Supply Voltage (V)	~ 20	~ 5	~ 2	~ 40	~ 2
Mobility (cm^2/Vs)	~ 1	~ 10	~ 0.5	~ 0.05	~ 25

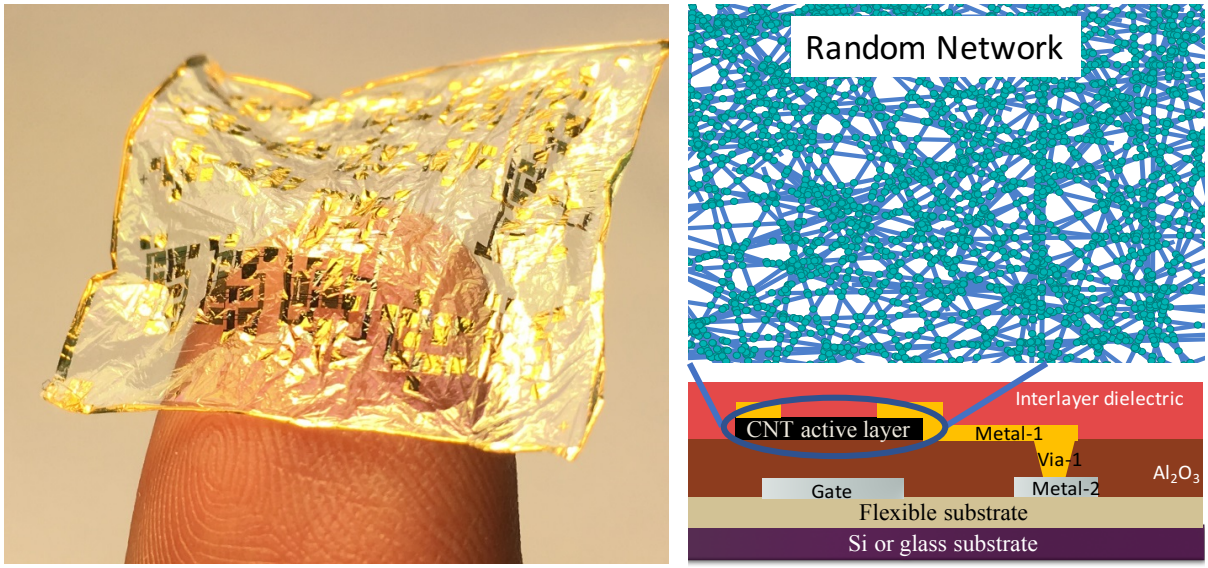


Figure 2.1: Flexible CNT TFT Circuits.

transistor and circuit measurements; Section 2.4 analyzes CNT-TFT circuits and explores the design spaces for NM and PDP optimization; Section 2.5 draws the conclusion.

2.2 Compact Modeling of CNT-TFT

2.2.1 CNT-TFT Properties

The cross section of the CNT-TFT is illustrated in Fig.5.1, where a bottom gate structure is used. The bottom gate structure enables a denser CNT network for better performance. For TFT technologies, there is only either N or P type of stable devices, as illustrated in Table 2.1.

CNT-TFTs usually exhibit P-type characteristics and the fabrication of stable N-type CNT-TFTs remains a longstanding challenge [30]. In our analysis, therefore, we focus on P-type CNT-TFTs and mono-type circuit design such as Pseudo-CMOS to accommodate material and device limitations of CNT-TFTs.

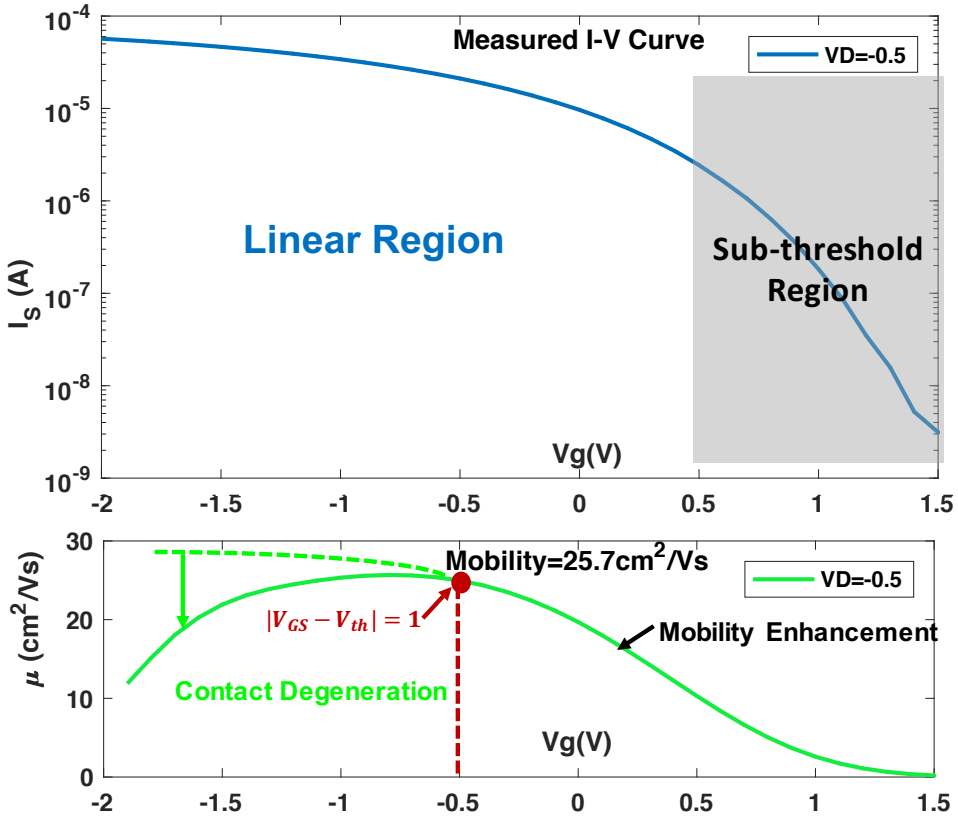


Figure 2.2: Measured CNT-TFT I-V curve and mobility dependency on gate voltages

2.2.2 Observations

To investigate the effective mobility of the CNT-TFT, a low source drain voltage ($V_S = 0V$ and $V_D = -0.5V$) is chosen to make sure that the device is in the linear region. The measured I-V curve is shown in the top part of Fig. 2.2. The bottom part of Fig. 2 shows the effective

mobility μ_{eff}, where the p-type MOSFET model is used to perform its derivation: $\mu_{eff} = g_m L/(WC_{ox}V_{SD})$ and $g_m = \partial I_{SD}/\partial V_{SG} = \mu_{eff}C_{ox}V_{SD}W/L$, where W is the gate width, L is the gate length, C_{ox} is the gate unit capacitance, V_{SG} is the source gate voltage and V_{SD} is the source drain voltage. Notice that the polarities of voltages and currents are opposite to those used in conventional N-type analysis. From Fig. 2.2, we observed that the effective mobility μ_{eff} is enhanced as the V_{SG} increases (with V_S fixed and V_G decreasing), when V_{SG} is relative small. However, as V_{SG} becomes larger, μ_{eff} starts to degrade.

2.2.3 Analysis and Assumptions

Similar mobility dependency phenomenon has been observed in OTFT and a-Si TFT [31], and the most accepted theories are based on charge drift in the presence of tail-distributed traps (TDTs) and variable range hopping (VRH) [26]. We therefore establish the CNT-TFT model based on TDTs and VRH theories which, to be shown in the following, can well capture the behaviors of CNT-TFTs.

Mobility Enhancement

Both theories indicate the field enhancement of the mobility :

$$\mu = \begin{cases} \mu_0(V_G - V_{th})^{\gamma}, & \text{N-type TFT} \\ \mu_0(V_{th} - V_G)^{\gamma}, & \text{P-type TFT} \end{cases} \tag{2.1}$$

, where V_{th} is the threshold voltage, γ is the field enhancement factor for mobility and μ_0 is defined as the effective mobility when $|V_G - V_{th}| = 1$, as illustrated in Fig. 2.2. This mobility enhancement assumption explains the increase of the effective mobility at a low V_{SG}.

Contact Effect

The degeneration of mobility at high V_{SG} can be explained by the contact resistances R_S and R_D at source/drain terminals, as shown in Fig. 3.8. These resistances result in effective source-gate voltage/source-drain voltage drops: $\tilde{V}_{SG} = V_{SG} - R_S\tilde{I}_{SD}$, $\tilde{V}_{SD} = V_{SD} - (R_S + R_D)\tilde{I}_{SD} = V_{SD} - R_C\tilde{I}_{SD}$, where $R_C = R_S + R_D$ and the current with contact effect is denoted as $\tilde{I}_{SD}$. The derivations are not presented here for simplicity and the contact effect can be illustrated as follows:

$$\tilde{I}_{SD} \approx \frac{WC_{ox}\mu}{L\{1 + kR_C(V_{th} + V_{SG})\}}\{(V_{th} + V_{SG}) - \frac{1}{2}V_{SD}\}V_{SD} \tag{2.2}$$

$$\frac{\tilde{I}_{SD}}{I_{SD}} \approx \frac{\tilde{\mu}}{\mu} = \frac{1}{1 + kR_C(V_{th} + V_{SG})};\ k = \frac{W}{L}C_{ox}\mu \tag{2.3}$$

From Eq. (2.3), we can conclude that contact resistances lead to a mobility reduction with a factor of $1/(1 + kR_C(V_{th} + V_{SG}))$ and it becomes more significant as V_{SG} increases, which explains the degeneration of the effective mobility with a high V_{SG} as shown in Fig. 2.2.

2.2.4 Model Derivations

We first establish the intrinsic current model based on the mobility enhancement assumption, then extend the model to capture parasitics and second order effects.

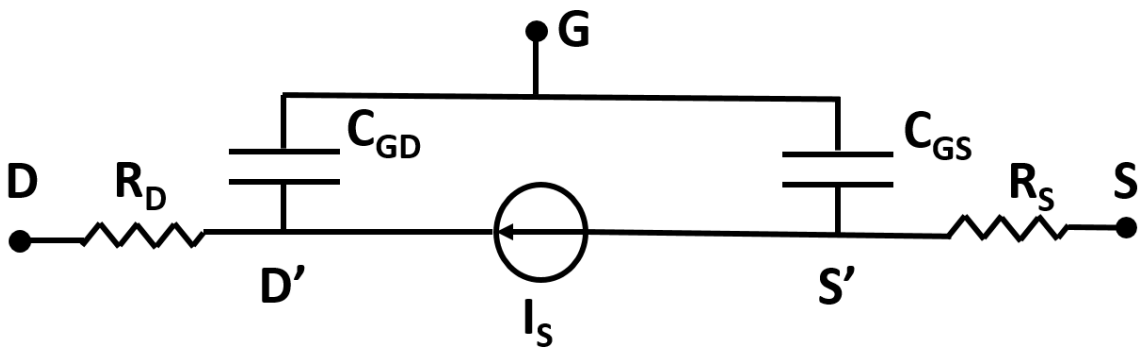


Figure 2.3: CNT-TFT intrinsic model with contact resistances

Intrinsic Current Model

We therefore integrate the mobility enhancement assumption Eq. (2.6) into the p type charge drift model Eqs. (2.4)-(2.5) to derive the intrinsic current model inspired by [31]:

$$I_{SD(x)} = Q_{CH}(x)v;\ v = u_{eff}\frac{\partial V(x)}{\partial x} \tag{2.4}$$

$$Q_{CH}(x) = WC_{ox}(V_{th} - V_G + V(x)) \tag{2.5}$$

$$u_{eff} = \mu_0(V_{th} - V_G + V(x))^{\gamma} \tag{2.6}$$

Since the current is constant in the channel [32], integrating along the channel $\int_{x=0}^{x=L} I_{SD}(x)dx$ yields:

$$I_{SD} = \frac{k}{(\gamma+2)}\{(V_{th} - V_{GS})^{\gamma+2} - (V_{th} - V_{GD})^{\gamma+2}\} \tag{2.7}$$

where k is defined as $\frac{WC_{ox}\mu_0}{L}$. Similar to MOSFET, we divide Eq. (2.7) into two regions: 1) linear region, and 2) saturation region. Applying the Taylor expansion and keep the first and

second order terms, we can then simplify the formula as:

$$I_{SD} \approx \begin{cases} k'\{(V_{th} - V_{GS}) - \frac{1+\gamma}{2} V_{SD}\} V_{SD}, \; V_{DS} > V_{GT} \\ \\ \frac{k'}{(\gamma+2)} (V_{th} - V_{GS})^2, \; V_{DS} \leq V_{GT} \end{cases} \tag{2.8}$$

$$k' = k(V_{th} - V_{GS})^{\gamma}; \; V_{GT} = V_{GS} - V_{th} \tag{2.9}$$

Notice that Eq. (2.8) becomes a conventional MOSFET model when $\gamma = 0$. This is because the main difference between the CNT-TFT intrinsic model, Eq. (2.7) and the MOSFET model is the mobility enhancement dependency on the gate voltage. This inherent connection between Eq. (2.7) and the MOSFET model leads to a major advantage: we can readily include second-order effects, such as channel length modulation, into Eq. (2.7) taking advantage of mature MOSFET theories.

Extending the Intrinsic Model

To further enrich the capability of the CNT-TFT intrinsic model, we incorporate the channel length modulation $1 + \lambda V_{SD}$ into Eq. (2.7) and the limiting function $f_{\text{lim}}(V_G, V)$ is added to provide smooth transitions between the sub-threhold region and the above-threshold region [32] :

$$I_{SD} = \frac{k}{\gamma + 2} (f(V_G, V_S)^{\gamma+2} - f(V_G, V_D)^{\gamma+2})(1 + \lambda V_{SD}) \tag{2.10}$$

$$f_{\text{lim}}(V_G, V) = SS \ln[1 + \exp(\frac{V_{th} - V_G + V}{SS})] \tag{2.11}$$

where λ is the channel length modulation factor and SS is related to the sub-threshold slope. We also summarize the simplified analytical model in Table 2.2, which can be used to analyze CNT-TFT based circuits and provide more design intuitions.

Table 2.2: Simplified Analytical Model for CNT-TFTs

	$V_{GS} \leq V_{th}$	$V_{GS} > V_{th}$
$V_{DS} \leq V_{GT}$	$\frac{k'}{(\gamma+2)}(V_{th} - V_{GS})^2$	$\frac{k}{(\gamma+2)}\{(SS\exp(\frac{V_{th}-V_{GS}}{SS}))^{\gamma+2}$ $-(SS\exp(\frac{V_{th}-V_{GD}}{SS}))^{\gamma+2}\}$
$V_{DS} > V_{GT}$	$k'\{(V_{th} - V_{GS})V_{SD}$ $-\frac{1+\gamma}{2}V_{SD}^2\}$	$-\frac{k'}{(\gamma+2)}(V_{th} - V_{GD})^2$

Contact Resistance and Gate Capacitance

We add two series resistances R_S and R_D to account for the contact effect as shown in Fig. 3.8. Two lumped capacitors C_{GS} and C_{GD} are added as well to characterize the transient behavior of the CNT-TFT circuits. Due to the large device sizes (hundreds of μm scale), two lumped capacitors are sufficient accurate to capture the transient responses of CNT-TFT circuits. Gate

source/drain parasitic capacitors C_{GSO} and C_{GDO} are also included to improve the accuracy.

$$C_{GS} = C_{GCS} + C_{GSO};\ C_{GD} = C_{GCD} + C_{GDO}; \tag{2.12}$$

$$C_{GSO} = C_{GDO} = C_{ox} W L_{ov}; \tag{2.13}$$

$$C_{GCD} = \partial Q_{CH}/\partial V_{GD} \approx \begin{cases} 1/2 C_{ox} W L \text{ Linear} \\ 0 \text{ Saturation/Cutoff} \end{cases} \tag{2.14}$$

$$C_{GCS} = \partial Q_{CH}/\partial V_{GS} \approx \begin{cases} 1/2 C_{ox} W L \text{ Linear} \\ 2/3 C_{ox} W L \text{ Saturation} \\ 0 \text{ Cutoff} \end{cases} \tag{2.15}$$

where L_{ov} is the gate source/drain overlap. C_{GCS} and C_{GCD} are implemented as voltage controlled capacitors in Verilog-A. The final equivalent circuit model is shown in Fig. 3.8 and all equations can be implemented in Verilog-A for the SPICE simulation.

2.3 Model Validation

In this section, we compare the SPICE CNT-TFT simulation results with measured source-drain current versus gate voltages (I-V) curves, Pseudo-CMOS inverters' voltage transfer curves (VTCs) and ring-oscillator's transient waveforms.

2.3.1 Device Validation

I-V Validation

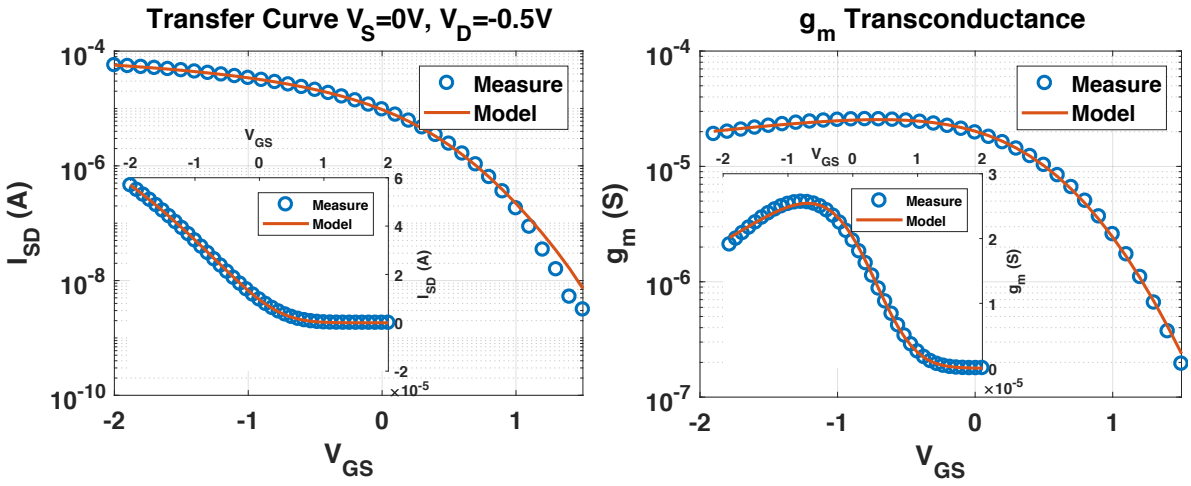


Figure 2.4: Model validation for $I-V$ and transconductance curves.

We first examined the proposed model with the measured I-V and transconductance curves. Both linear and logarithmic scales are shown in Fig. 2.4. The model prediction well matches the device measurement reflecting both the mobility enhancement and contact resistance caused degeneration as shown in the Fig. 2.4. A wide range of $V_{GS} \in [-2, 0]V$ and $V_{DS} \in [-4, 0]V$, covering sub-threshold, linear and saturation, are investigated, as illustrated in Fig. 3.9. To the best of our knowledge, this is the first ever reported SPICE CNT-TFT model to cover sub-threshold, linear and saturation regions. The excellent match between model predictions and measurement data further confirm the validity of the above-mentioned model derivations and assumptions.

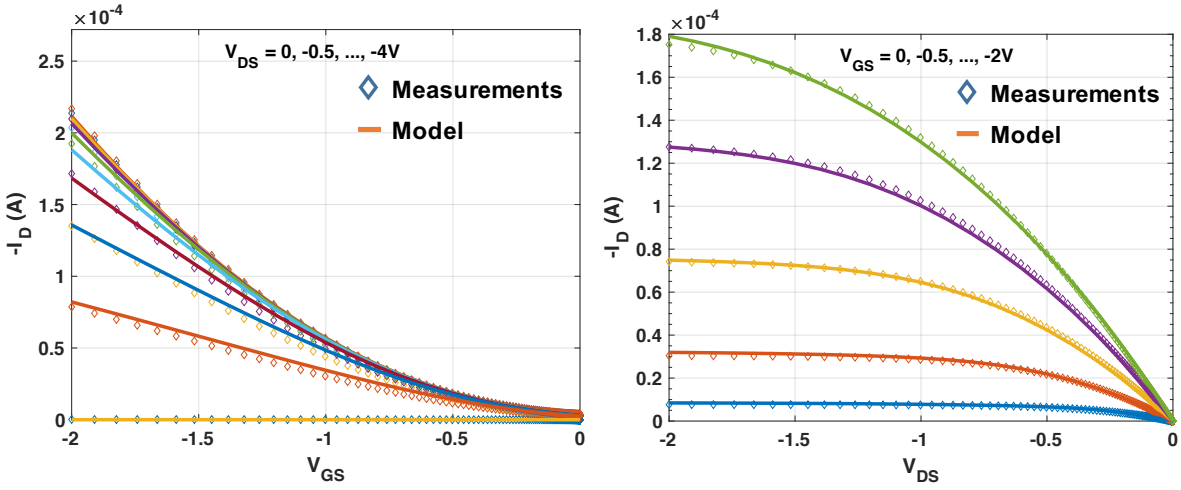


Figure 2.5: Model validation for $I - V$ curves

Parameter Extraction

We extract model parameters out of 52 fabricated CNT-TFTs, where a Gaussian distribution is assumed for process variations. All extracted parameters are summarized in Table 3.2, where the mean value μ and standard deviation σ are provided.

Table 2.3: Parameters extracted from 52 fabricated CNT-TFTs

Model Parameter	Notation	[μ, σ] Unit
Channel Length	L	[25, -] um
Channel Width	W	[125, -] um
Gate S/D Overlap	L_{ov}	[10, -] um
Gate Unit Capacitance	C_{ox}	[200, -] nF/cm^2
Threshold voltage	V_{th}	[0.5, 0.102] V
Sub-threshold Swing	SS	[0.28, 0.0388] V/dec
Effective Mobility	μ_0	[25.69, 0.19] cm^2/Vs
Contact Resistance	R_C	[1531, 291] Ω
Channel Length Modulation	λ	[0.064, 0.0185] V^{-1}
Factor of Gate Dependent mobility	γ	[0.20, 0.116] (-)

2.3.2 Circuits Validation

Beside single devices, the model must be able to predict the circuit level behaviors with a sufficient accuracy. We therefore compare the SPICE simulation results with the measured voltage transfer curves (VTC) and ring-oscillator's waveform.

Introduction to Pseudo-CMOS

Pseudo-CMOS is a design style proposed to address design challenges of mono-type TFT circuit design [28][29], which has been proven a robust design style and has been widely used for flexible digital, analog, and power circuits [33][34][35]. Compared to conventional mono-type digital design styles, such as the diode-load or resistive-load designs, Pseudo-CMOS offers better noise margin and provides post-fabrication tunability at the cost of an additional power rail V_{SS}. There are two topologies of Pseudo-CMOS: depletion (Pseudo-D) type and enhancement (Pseudo-E) type. We focus on the Pseudo-D type since it is more suitable for our depletion devices [29]. A Pseudo-D inverter consists of three power rails, V_{DD}, V_{SS} and GND, and four transistors M_{1-4}, as shown in Fig. 2.6.

VTC Validation

A typical voltage transfer curve (VTC) of an inverter is shown in Fig. 2.7 and here we focus on V_{SP}, $V_{I/OH}$ and $V_{I/OL}$, which determine the noise margin (NM) for digital circuits. In Fig. 2.8 (Left), we compare the SPICE simulated voltage transfer curves (VTCs) and small signal gain with actual measurements, where solid lines are SPICE simulations and dots are

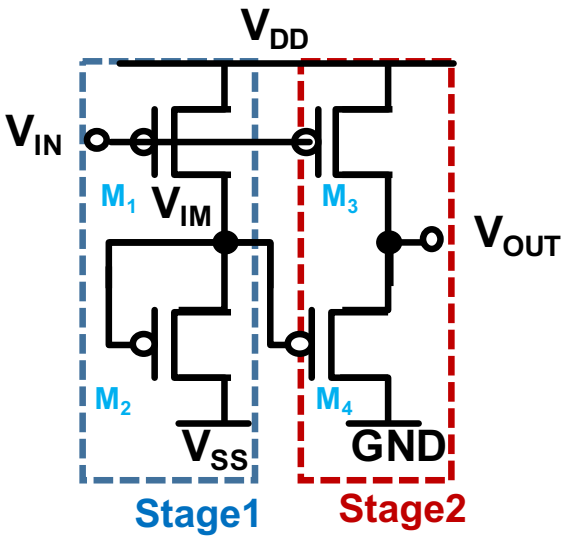


Figure 2.6: Pseudo-D inverter

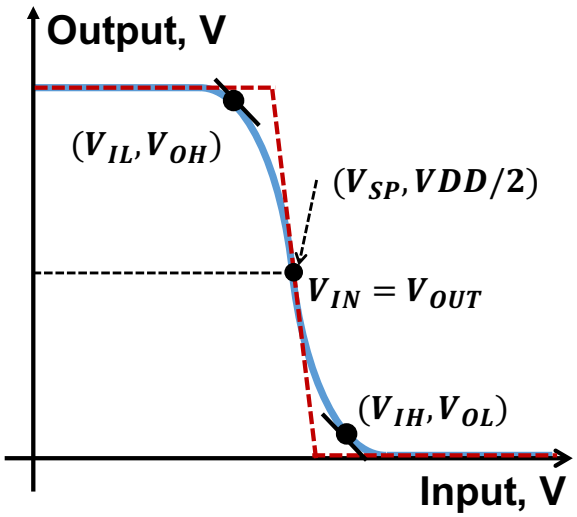


Figure 2.7: Typical VTC

measurements. Both VTC and small signal gain simulations match closely with the circuit measurements over a wide range of supply voltages V_{DD}, from 0.8V to 1.6V. Despite minor discrepancies in low supply voltages, the proposed model accurately predicts the V_{SP}, $V_{I/OH}$ and $V_{I/OL}$. Furthermore, Monte Carlo simulation is performed to illustrate various VTCs under process variations, based on extracted device parameters as shown in Table 3.2. From Fig. 2.8 (Right), we can see that the SPICE simulation can accurately predict the variation of the V_{SP} of the VTCs, where bold lines are simulation results using the mean values in Table 3.2.

Transient Validation

We validated our transient model using the Pseudo-D based five-stage ring-oscillator's measured waveform. As shown in Fig. (2.9), the SPICE simulation result well captures the oscillation frequency and the amplitude compared with the measurement data.

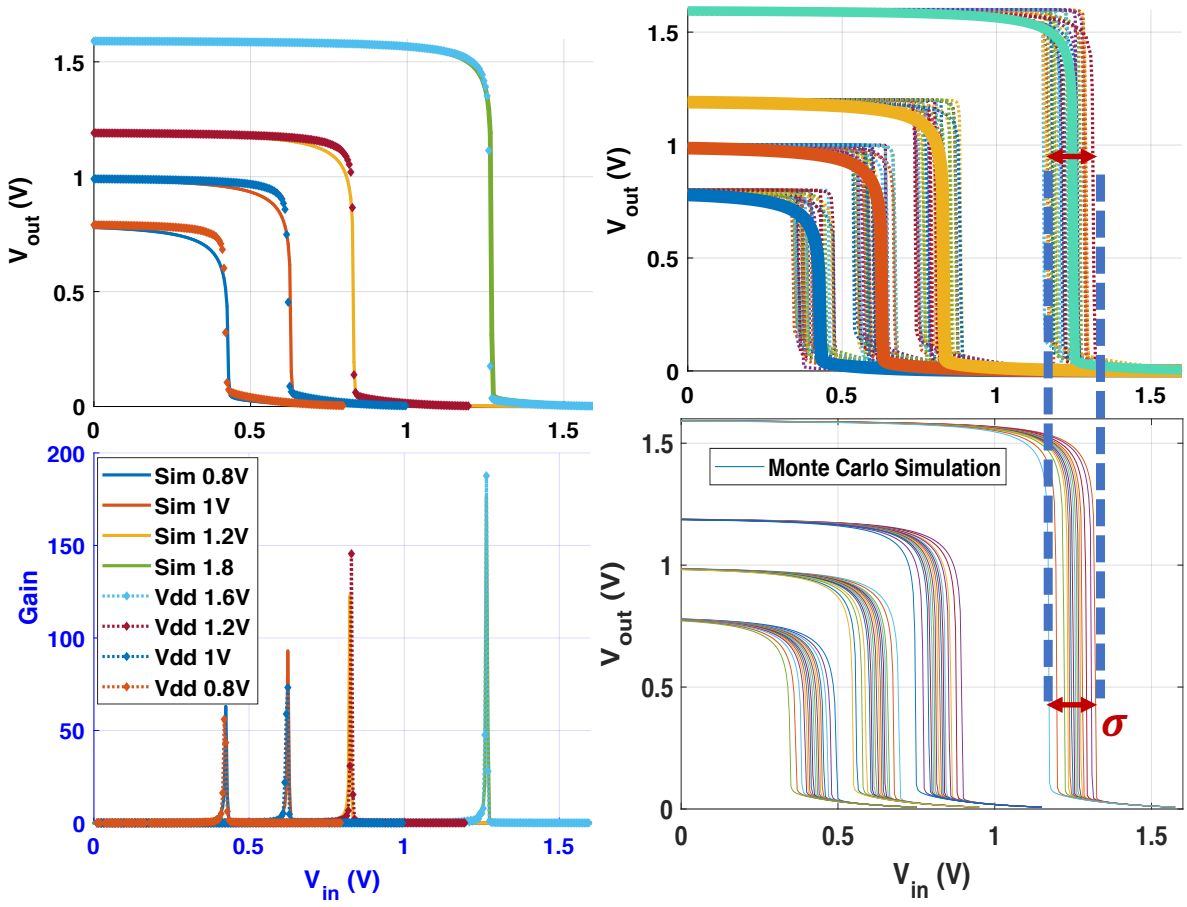


Figure 2.8: Left: Measured and simulated VTCs and small signal gains; Right: 26 measured VTCs and Monte Carlo simulation

In summary, the results of both DC and transient simulations indicate that the proposed SPICE CNT-TFT model can accurately predict both device and circuit level behaviors.

2.4 Noise Margin, Power-Delay Analysis and Design Exploration

To further enable large-scale flexible circuit design, we thoroughly analyze the key merits for digital circuits, including NM, power and delay, and develop a systematic design methodology

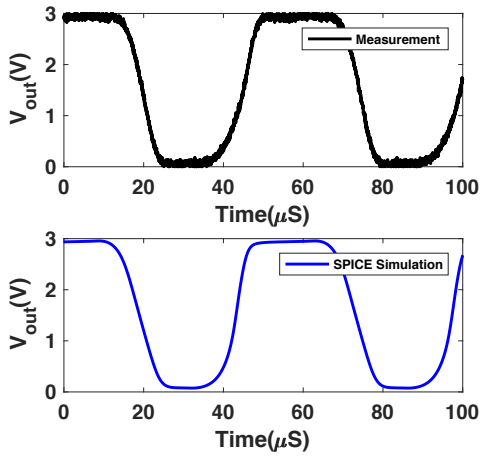


Figure 2.9: Ring-oscillator

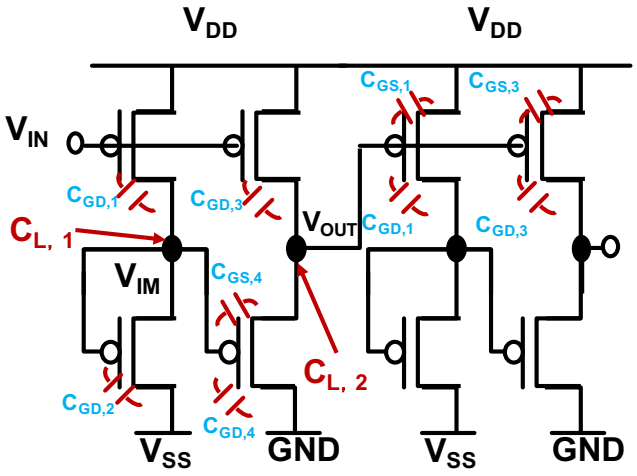


Figure 2.10: Load Capacitance

to facilitate design automation for CNT-TFT flexible circuits. In this section, we first analyze how device parameters, transistor sizes and supply voltages affect NM and PDP for Pseudo-D digital circuits. Based on insights derived from this analysis, we propose a design framework to optimize the NM and PDP.

2.4.1 Noise Margin Analysis

A Pseudo-D inverter consists of two stages, as illustrated in Fig. 2.6. Since the first stage dominates the overall inverter VTC, for simplicity our NM analysis focuses on the first stage.

Derivation A typical VTC of an inverter is shown in Fig. 2.7 and the NM is defined as $NM = \min(V_{OH} - V_{IH}, V_{IL} - V_{OL})$. We use the following approximations to simply the derivations: 1) $V_{OH} \approx V_{DD}$, $V_{OL} \approx GND$; 2) $V_{IH/L} \approx V_{SP} \pm \frac{V_{DD}}{2Gain} \approx V_{SP}$. Such simplifications are reasonable resulting in negligible errors. As shown in Fig. 2.8, the VTCs are almost rail to rail and the gains are very high (≥ 50) even with a V_{DD} at $0.8V$, which leads to

a negligible $\frac{V_{DD}}{2Gain}$. Therefor, the simplified analytical NM model can be expressed as:

$$\begin{aligned} NM &= \min(V_{OH} - V_{IH}, V_{IL} - V_{OL}) \\ &\approx \min(V_{DD} - V_{SP}, V_{SP}) \end{aligned} \tag{2.16}$$

$$V_{SP} = V_{DD} + V_{th}(1 - {}^{\gamma+2}\sqrt{\alpha}),\ \alpha = W_2/W_1. \tag{2.17}$$

$$(V_{DD} - V_{SS})/2 \geq {}^{\gamma+2}\sqrt{\alpha} V_{th}; \tag{2.18}$$

where $\alpha = W_2/W_1$ is the transistor size ratio of M_2/M_1 and V_{SP} is derived through the current equivalent at the switching point using the saturation model in Table 2.2. Eq. (2.18) ensures that $M_{1/2}$ are in the saturation region at V_{SP}. Compared to the mean value of 26 measured VTCs, the analytical NM model can predict the NM for Pseudo-D inverters within an error $\leq 6.25\% V_{DD}$ even at a low supply voltage $V_{DD} = 0.8V$.

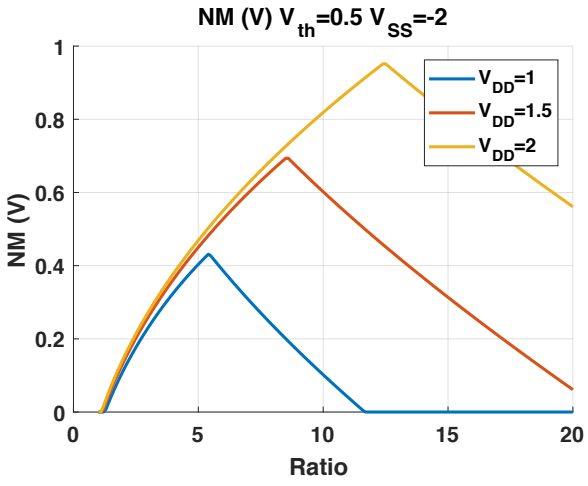


Figure 2.11: NM vs. Ratio α

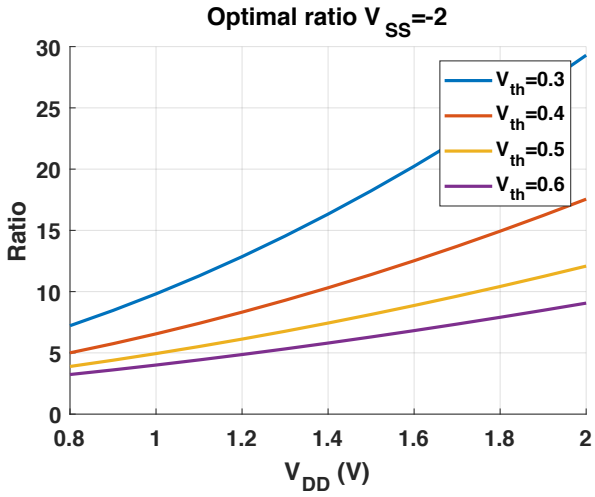


Figure 2.12: Optimal α.

Analysis In Figs. 2.11 and 2.12, we analyze the relationship among NM, transistor sizes, V_{th} and supply voltages. The simulation results show that: 1) properly adjusting transistor sizes can effectively improve the NM; 2) an optimal ratio α_{opt} to assure the maximum NM can be accurately predicted by Eq. (2.19) which is determined by the ratio of V_{DD}/V_{th}; 3) the maximum achievable NM is slightly less than $V_{DD}/2$ due to the imperfect $V_{OL/H}$. To ensure $V_{OL} \approx 0$ and $V_{OH} \approx V_{DD}$, the constraints for V_{DD} and V_{SS} are given in Eq. (2.20). Simulation results further confirm our analysis results, where $V_{DD} - V_{OH} \leq 0.05V$ and $V_{OL} \leq 0.05V$ with Eq. (2.20) being satisfied.

$$\alpha_{opt} = (1 + \frac{V_{DD}}{2V_{th}})^{\gamma+2} \tag{2.19}$$

$$\left.\begin{matrix} V_{DD}-V_{OH}\approx 0 \\ V_{OL}\approx 0 \end{matrix}\right\} \Leftrightarrow \left\{\begin{matrix} V_{DD}\geq 2V_{th} \\ -V_{SS}\geq 2V_{th} \end{matrix}\right. \tag{2.20}$$

2.4.2 Power and Delay (P&D) Analysis

In this section, we analyze the trade-offs among power, delay and NM for Pseudo-D circuits [36]. According to [29], we use the following default transistor sizes: $W_1 = W_{min} = 5\mu m$, $W_2 = W_3 = W_4 = 15\mu m$ in the analysis. And, we define t_{p0} as the propagation delay of a Pseudo-D inverter with these default sizes.

Power Analysis For the total power P_{tot}, it consists of two parts: static power P_{stat} and dynamic power P_{dyn}. We ignore the direct path power dissipation during switching P_{dp}, which

is negligible comparing to P_{stat} and P_{dyn}.

$$P_{tot} \approx P_{stat} + P_{dyn};\ k_i = \frac{W_i C_{ox} \mu_0}{L} \tag{2.21}$$

$$P_{stat} \approx \overbrace{\frac{D_H}{2} V_{th}^{\gamma+2} \{k_2(V_{DD} - V_{SS}) + k_4 V_{DD}\}}^{\text{Output High}} + \overbrace{\frac{D_L}{2} V_{th}^{\gamma+2} \{k_1(V_{DD} - V_{SS}) + k_3 V_{DD}\}}^{\text{Output Low}} \tag{2.22}$$

$$P_{dyn} \approx f\{\overbrace{C_{L,1}(V_{DD} - V_{SS})^2}^{Stage1} + \overbrace{C_{L,2}(V_{DD})^2}^{Stage2}\} \tag{2.23}$$

where f is the frequency, $D_{L/H} \in [0, 1]$ is the fraction of the duration when output is low/high in each period and $C_{L,1/2}$ is the equivalent load capacitance at node V_{IM}/V_{OUT}, as indicated in Fig. 2.10. To improve accuracy, Miller effects are incorporated as well:

$$C_{L,1} = \overbrace{2C_{GDO,1}}^{\text{Miller Effect}} + C_{GDO,2} + C_{GS,4} + C_{GD,4} \tag{2.24}$$

$$C_{L,2} = C_{GS,1} + C_{GD,1} + C_{GS,3} + C_{GD,3} + \overbrace{2C_{GDO,3}}^{\text{Miller Effect}} \tag{2.25}$$

The static power is dominantly determined by V_{th} because the leakage current $I_{leak} \propto V_{th}^{\gamma+2}$. The dynamic power is a function of the frequency, supply voltage and total capacitance.

Delay Analysis For the propagation delay t_p, we use the equivalent RC approximation [36]:

$$t_p = \frac{0.69}{2}\{\overbrace{C_{L,1}(R_{eq,1}+R_{eq,2})}^{Stage1}+\overbrace{C_{L,2}(R_{eq,3}+R_{eq,4})}^{Stage2}\} \tag{2.26}$$

$$R_{eq,2} \approx \frac{3}{4k_2}\frac{V_{DD}-V_{SS}}{V_{th}^{\gamma+2}};\ R_{eq,1} \approx \frac{3}{4k_1}\frac{V_{DD}-V_{SS}}{(V_{DD}+V_{th})^{2+\gamma}} \tag{2.27}$$

By setting the k_2 to $k_{3/4}$ and $V_{SS} = 0$ in $R_{eq,M1}$, we can get $R_{eq,M3/4}$. Notice that $R_{eq,M1/3/4}$ decreases as the supply voltage V_{DD} increases; however, $R_{eq,M2}$ behaves opposite. This is because zero-V_{gs} connection will limit the current to a small value ($I_{M,2} = k_2 V_{th}^{\gamma+2}$) during switching, leading to a large equivalent resistance. This also confirms the validity of ignoring P_{dp}.

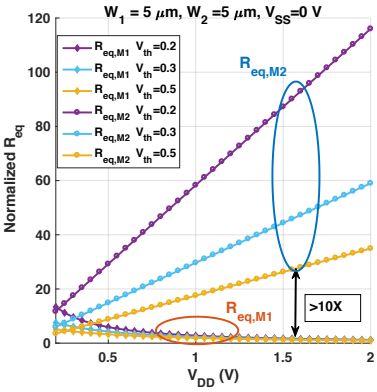


Figure 2.13: V_{DD} vs. R_{eq}

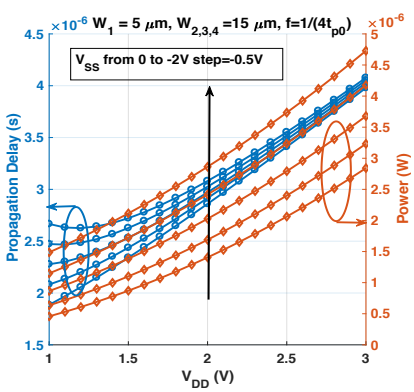


Figure 2.14: V_{DD} vs. P&D

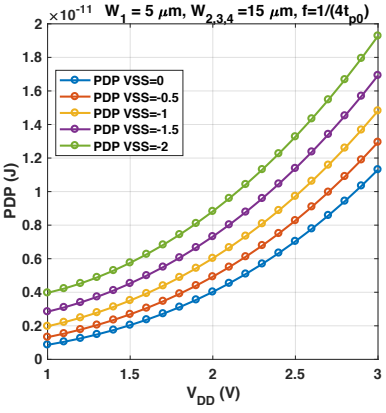


Figure 2.15: V_{DD} vs. PDP

Design Space Exploration First, we investigate how supply voltages affect the delay and power. We observed that simply increase the V_{DD} cannot improve the propagation delay as shown in Fig. 2.14, which is counter-intuitive to conventional wisdom. This is because $R_{eq,M2}$ increases as the supply voltage and $R_{eq,M2}$ is much larger ($\sim 10X$) than $R_{eq,M1/3/4}$, as shown in

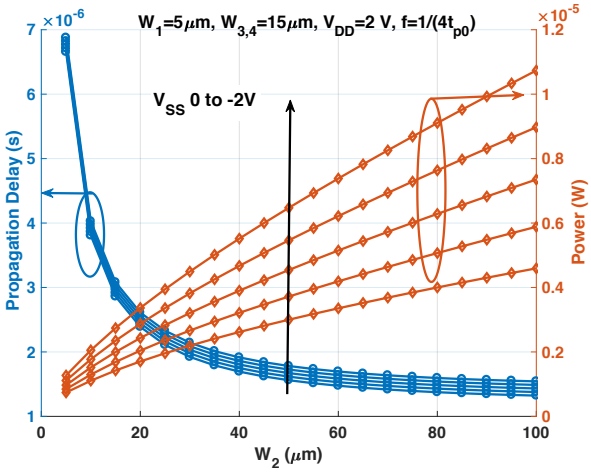


Figure 2.16: W_2 vs. P&D

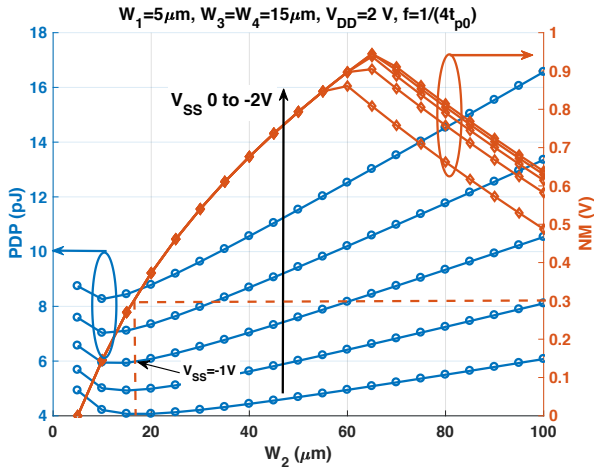


Figure 2.17: W_2 vs. PDP and NM

Fig. 2.13, preventing from further improving of the stage delay. As a result, the delay increases as V_{DD} becomes higher, due to the dominant $R_{eq,M2}$. This phenomenon indicates that Pseudo-D is more suitable for low voltage design, which can benefit from a better PDP, as shown in Fig. 2.15. For V_{SS}, a large negative V_{SS} will increase the delay and power; however, it leads to a better NM as illustrated in Fig. 2.17.

After identifying $R_{eq,M2}$ as a critical part for power and delay, we analyze the impact of W_2 on power, delay and NM. We observed that W_2 can be used to explore the trade-off between power and delay as show in in Fig. 2.16. A larger W_2 can lead to a smaller delay but higher power consumption. Furthermore, W_2 will also affect the NM, as shown in Fig. 2.17, and the optimal values of W_2 for NM and PDP are different. Thus, trade-off between NM and PDP should be evaluated during the circuit design stage.

2.4.3 NM and PDP Optimization

Based on the analysis in Section 2.4.2, we conclude that supply voltages and transistor sizes influence the PDP significantly for Pseudo-D circuits. Furthermore, to assure a good NM, transistor sizes and supply voltages have to satisfy certain constraints stated in Section 2.4.1. Hence, we can formulate a constrained optimization problem to optimize the PDP while meeting the NM requirement for Pseudo-D circuits:

$$
\begin{aligned}
&\text{minimize} && PDP(W_{1-4}, V_{SS}) \text{ given } NM_0, V_{th}, V_{DD} \\
&\text{subject to} && \min(V_{DD} - V_{SP}, V_{SP}) \geq NM_0 \Leftrightarrow \text{ Eq. (2.16)} \\
& && (V_{DD} - V_{SS})/2 \geq^{\gamma+2} \sqrt{\alpha} V_{th}; \quad \Leftrightarrow \text{ Eq. (2.18)} \\
& && V_{DD} - V_{OH} \leq \delta,\ V_{OL} \leq \delta; \qquad \Leftrightarrow \text{ Eq. (2.20)} \\
& && W_i \geq W_{min} = 5\ \mu m
\end{aligned}
$$

The above optimization determines transistor sizes and V_{SS} given specific NM_0, V_{th} and V_{DD}. Using Lagrange multipliers and gradient decent, we can solve the above constrained optimization and optimized results for different NM_0 are summarized in Table 2.4. Compared to the default design in Fig. 2.17, the optimized results show $\sim 3X$ improvement for PDP with the same $NM = 0.3\ V$ and supply voltages. Considering V_{th} and V_{DD} as design parameters, we can achieve $\sim 6X$ improvement with device and circuit co-optimization. Although our exemplar formulation above uses the PDP as the optimization target, it can be easily modified for power or delay optimization. In summary, this proposed design framework can effectively

optimize the PDP (or just power or delay) while satisfying the NM specification.

Table 2.4: Pseudo-D Optimization $V_{DD} = 2\ V$, $V_{th} = 0.5\ V$, $\delta = 0.05$

NM_0	W_1	W_2	W_3	W_4	V_{SS}	PDP
0.3V	5.0μm	18.5μm	5.0μm	5.0μm	-1.00V	2.14pJ
0.5V	5.0μm	27.4μm	5.0μm	5.0μm	-0.97V	2.24pJ
0.8V	6.9μm	62.4μm	7.0μm	5.1μm	-0.85V	3.39pJ

2.5 Summary

In this part, we present a SPICE-compatible CNT-TFT model to support CNT-TFT flexible circuit design. The model has been derived and validated based on 52 fabricated CNT-TFTs and 26 Pseudo-D inverters. Based on the proposed model, we further analyze how device parameters, supply voltages and transistor sizes affect the NM and PDP of Pseudo-D circuits. Finally, a constrained optimization procedure is proposed to optimize the PDP while meeting the NM specification. The proposed optimization methodology can be easily extended to more complicated logic gates and library cells, which can further enable greater automation of large-scale flexible circuit design based on CNT TFTs.

Chapter 3

Process Design Kit for Flexible Hybrid Electronics

This part, we will discuss the development of the process design kit (PDK) for flexible hybrid electronics (FHE) using CNT-based flexible electronics.

3.1 Introduction

Flexible electronics is emerging as an alternative to conventional silicon electronics for applications such as wearable sensors, medical patches, bendable displays, foldable solar cells and disposable RFID tags [2][33][35]. Fig. 3.1 shows a test sample of a recent Pseudo-CMOS logic circuit with carbon nanotube (CNT) TFTs on a 1-μm thick plastic foil [2]. Unlike conventional silicon electronics that needs sophisticated billion-dollar foundry for manufacturing, flexible electronic circuits can be fabricated on thin and conformable substrates such as plastic films,

Table 3.1: Comparison between different TFT technologies

Device Type (TFT)	Amorphous Si	Metal-Oxide	SAM Organic	Polymer Organic	Carbon Nanotube
Process Temperature	$\sim 250^{\circ}$C	$\sim 150^{\circ}$C	$\sim 100^{\circ}$C	Room temp.	Room temp.
Process Technology	Lithography	Roll-to-roll	Shadow mask	Ink-jet	Litho. & Shadow & R2R
Feature Size (μm)	8	5	50	50	25
Substrates	Glass/foil	Glass/foil	Foil	Foil	Foil
Device Type	N-type only	N-type only	Complementary	Complementary	Complementary
Supply Voltage (V)	20	10	2	40	2
Mobility (cm^2/Vs)	1	10	0.5	0.05	25

with low-cost, high-throughput manufacturing methods such as ink-jet printing and roll-to-roll imprinting. The time-to-market as well as manufacturing cost can therefore be significantly reduced. Its flexible form factor also enables innovative designs for consumer electronics and biomedical applications [37][20].

However, several design challenges of flexible electronics must be addressed before their broad deployment to their products for next-generation IoT and wearable products. Table 3.1 compares the key characteristics of thin-film transistors (TFTs). Compared with crystalline-silicon metal-oxide-field-effect-transistor (MOSFET), TFTs often have a significantly slower operating speed and are less reliable. Due to material properties, TFTs are usually mono-type, either only p- or only n-type devices [30][38]. Making air-stable complementary TFT circuits is quite challenging or often requires heterogeneous process integration of two different TFT technologies. Existing CMOS design methodologies for silicon electronics, therefore, cannot be directly applied for designing flexible electronics. Other factors such as high supply voltages, large process variations, and lack of trustworthy TFT compact models for simulation also make designing large-scale TFT circuits a significant challenge.

Design often involves multiple levels of abstraction for ensuring minimum product re-spins, for protecting intellectual property and for creating a seamless flow from application, manufacturing, to product realization. Process Design Kits (PDK) has been a key reason for the

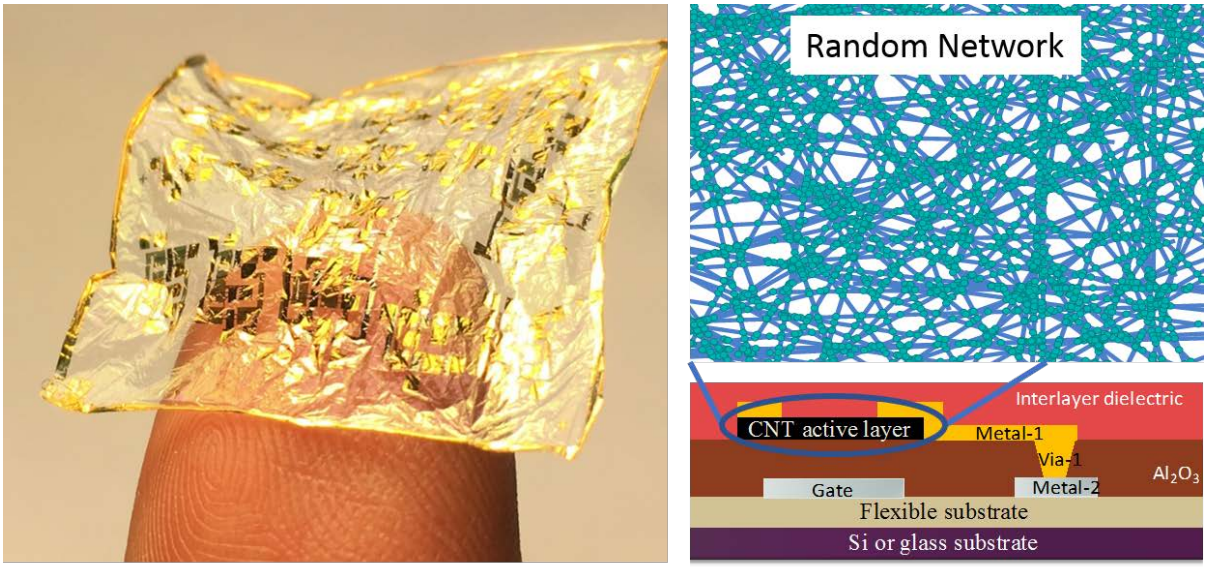


Figure 3.1: (Left) A CNT-TFT logic circuit on a 1-μm thick plastic foil. (Right) Side view of a CNT-TFT [2].

great success of CMOS technology in last several decades. To enable the design of large-scale, highly integrated Flexible Hybrid Electronics (FHE), PDKs will be very critical. In contrast to the semiconductor industry where a single foundry is responsible for the entire manufacturing process, the FHE industry is fragmented-multiple manufacturers provide processes that cater to subsystem, but not the entire system. Unlike a wafer fab with an investment of billions of dollars, a combination from multiple foundries, each with an investment only in the order of a few million dollars, is used to realize the FHE. In addition, different foundries could provide different substrates such as PEN, PET, DuPont^{TM} Kapton, glass or work to realize components such as resistors, inductors, capacitors, filters, antennas, sensors, batteries, etc. Such implementations will lead to greater deformation that any other systems today, and therefore addressing the associated mechanical, thermal, and electrical issues becomes critical. As technology evolves, new printing methods and materials will emerge with better proper-

ties. To enable seamless deployment of the FHE technologies, a framework is required where the design rules for each process can be captured, models can be developed and manufacturing details can be hidden, so that a designer can easily integrate various components into the system following a tool-assisted process. Needless to say, such a framework should be standardized and be compatible with commercial design environments using mainstream design tool suites. We currently collaborate with US Manufacturing Innovation Institute for Flexible Hybrid Electronics, *aka NextFlex*, to develop FHE-PDK to enable an open ecosystem for FHE design-manufacture-application. The main contributions of this work are summarized as follows:

- Developing an accurate SPICE-compatible design environment for FHE IoT applications, which is thoroughly validated using transistor and circuit measurements

- Lowering the design difficulties by providing a roust cell libraries

- Fully functional physical verification to guarantee design yield and circuit performance

In this work, we first introduce the key devices our FHE-PDK is targeting which includes flexible carbon-nanotube thin-film transistors (CNT-TFTs) and passive elements such as resistors. The following sections provide more details about compact modeling and technology files for these emerging devices to be used for design, simulation, and physical verifications.

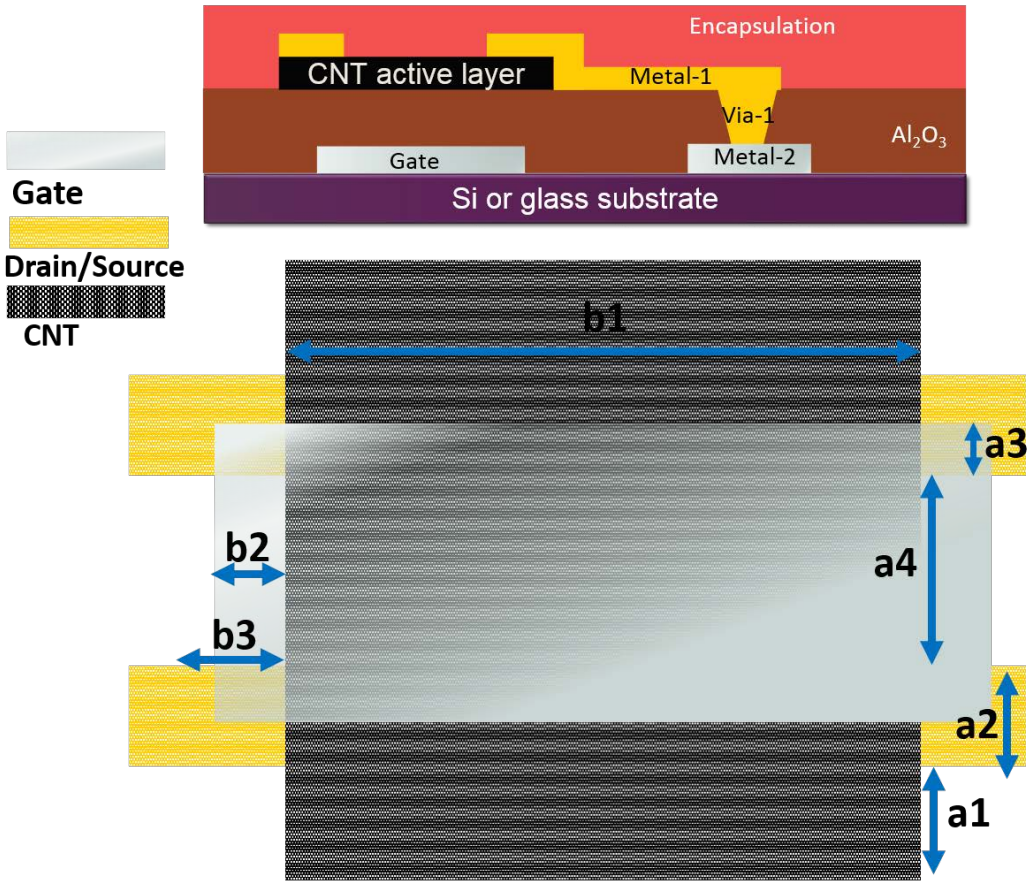


Figure 3.2: (Top) Side view of a carbon nanotube transistor (CNT-TFT). (Bottom) Top view of a CNT-TFT including physical dimensions for DRC.

3.2 Flexible Carbon-Nanotube Devices

3.2.1 CNT Thin-Film Transistor

The cross section of a CNT-TFT is illustrated in Fig. 3.2, where a bottom gate structure is used. The bottom gate structure enables a denser CNT network for a better performance. Multiple layers of metal are connected using vias as the case for CMOS silicon chips, and currently up to four layers of metal are supported to enable higher design complexity for CNT-TFT circuits. The physical dimensions for design rule checking (DRC) are also labeled in Fig. 3.2 and cur-

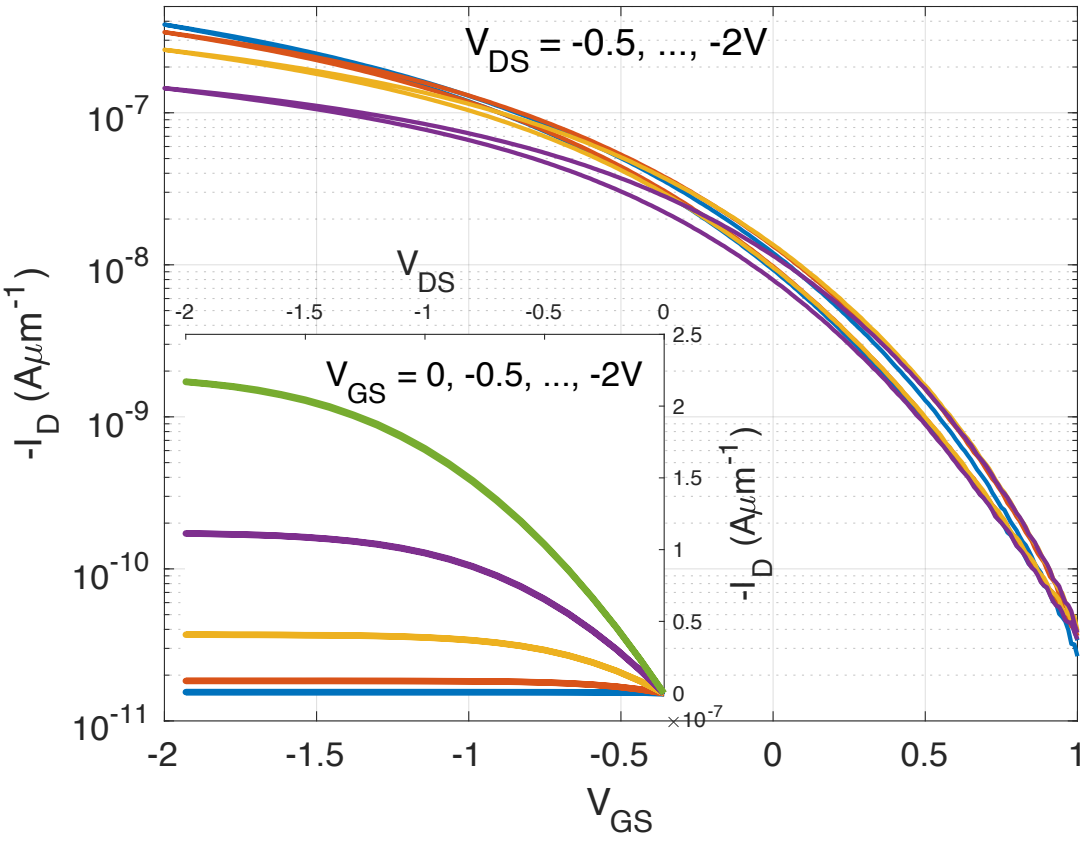


Figure 3.3: Drain current versus gate voltages for a CNT-TFT.

rently down to 2-μm channel length is feasible using manual alignment and photolithography masks to directly fabricate TFTs on thin flexible substrates. For TFT technologies, there is only either n- or p-type of stable devices, but not both, as illustrated in Table 3.1. CNT-TFT exhibits p-type characteristics and the fabrication of stable n-type CNT-TFTs remains a long-standing challenge. In this work, we use p-type CNT-TFTs as an exemplar driver for FHE-PDK development.

A typical transfer curve of the drain current (I_{DS}) versus the gate voltage (V_{GS}) for a p-type CNT-TFT is shown in Fig. 3.3. Thanks to the high dielectric constant (~ 8) of the thin gate dielectric layer of Al_2O_3, a low supply voltage of 2 V is feasible to drive a CNT-TFT with a

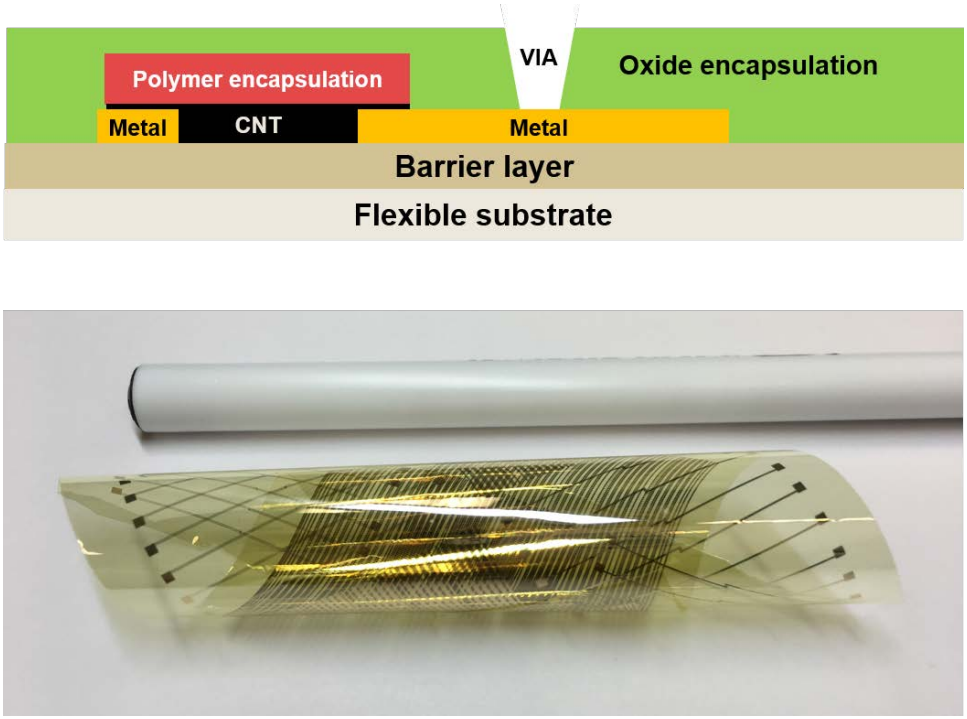


Figure 3.4: (Top) Side view of a CNT resistor. (Bottom) Device photo of the CNT resistor array on a 10-μm thick polyamide foil.

typical channel width of 125 μm and a length of 25 μm. A typical on-off current ratio is 10^5 to 10^6 for a CNT-TFT, and it often requires a positive gate voltage V_{GS} to turn off the device in the depletion mode.

3.2.2 CNT Resistor

Similar to a CNT-TFT, a CNT linear resistor is feasible by removing the gate terminal of a CNT-TFT to form a two-terminal CNT resistor on flexible substrates. A flexible CNT resistor array is shown in Fig. 3.4 including the side view of a CNT resistor. While the resistance values of a CNT linear resistor can be varied by width *W* and length *L* as indicated in Fig. 3.5, the sheet resistance is determined by the CNT material treatment. The current-voltage (I-V)

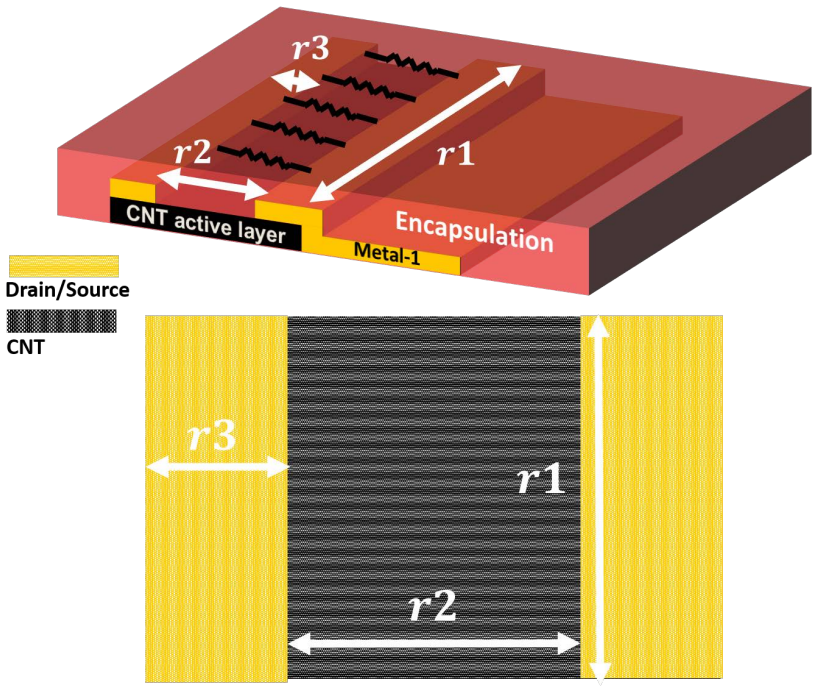


Figure 3.5: Device dimension of a CNT resistor. r1 represents the device width W and r2 represent the device length L. r3 is the metal enclosure distance.

relationship of the CNT resistor array is shown in Fig. 3.6, where the device width W is fixed at 40 μm and the device length L varies from 10 μm to 100 μm. These plots clearly indicate that CNT resistors have good linear relationship with 20-30% variations in their resistance values.

3.3 FHE-PDK Introduction and Compact Modeling

3.3.1 Introduction to the PDK

The PDK is a database for a specific technology, including devices properties and fabrication information, which can be stored in technology files and also expressed as SPICE/Verilog-A models. Illustrated in Fig. 3.7, the PDK provides all needed information for a typical circuit

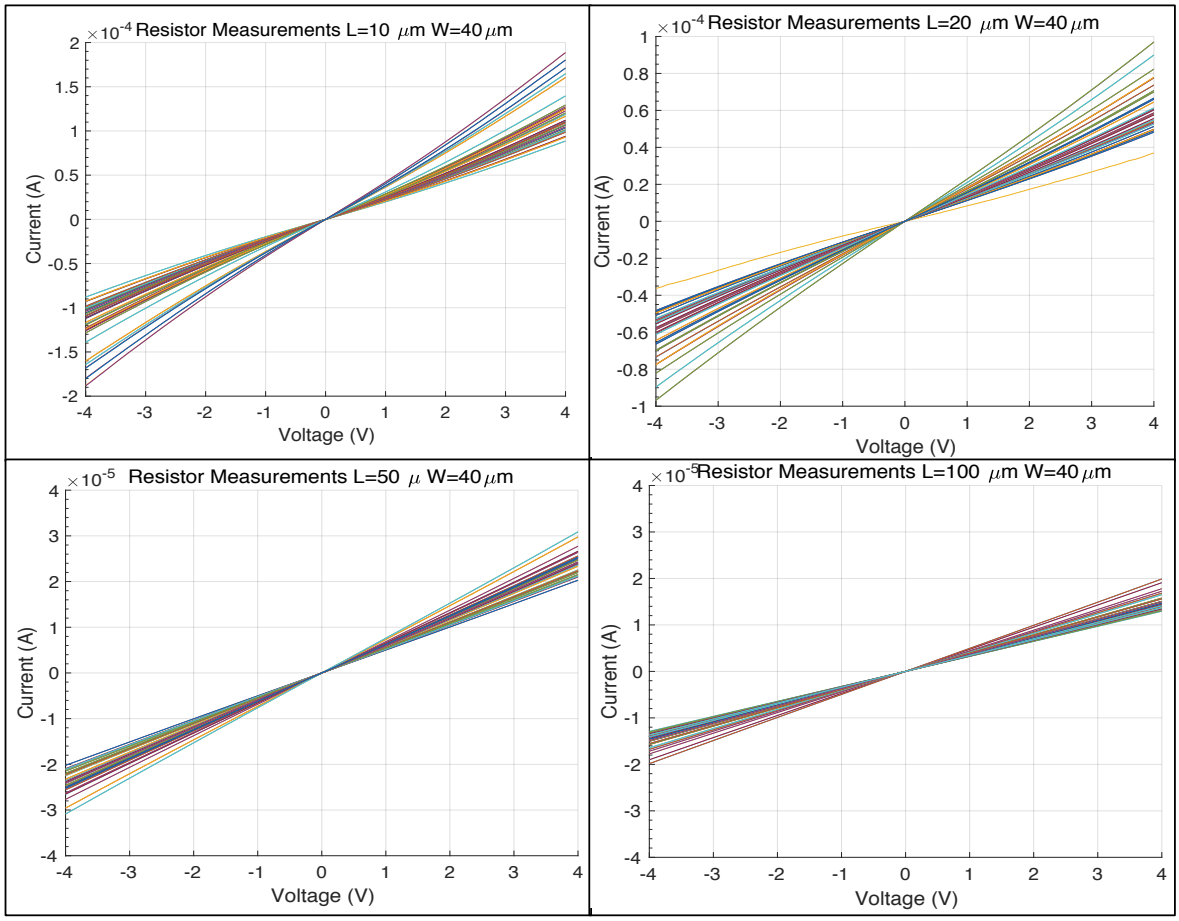


Figure 3.6: Measured I-V characteristics of flexible CNT resistor array. The width is 40-μm and the length varies from 10-μm to 100-μm.

design flow from schematic simulation and physical verification to post-layout simulation.

Accurate SPICE/Verilog-A models are necessary for circuit simulation and design space exploration. In the technology file, technology information is stored and electrical properties and fabrication rules are defined as well. Specifically, it contains layer definitions, device definitions and physical/electrical rules, which will be used for physical verification. Three procedures are required for verification: design rule checking (DRC), layout versus schematic (LVS) and layout parasitic extraction (LPE). DRC is used to verify whether the physical layout

obeys the design rules predefined in the technology files, such as minimum widths, spacings and overlaps. Thus, a DRC-cleared design promises a high manufacturing yield. LVS is used to verify whether the physical layout, created for manufacturing, is equivalent to the schematic design, which is used for simulation. Finally, LPE is used to extract the parasitic devices, such as parasitic capacitors and resistors, which should be included for post-layout simulation to ensure high simulation fidelity.

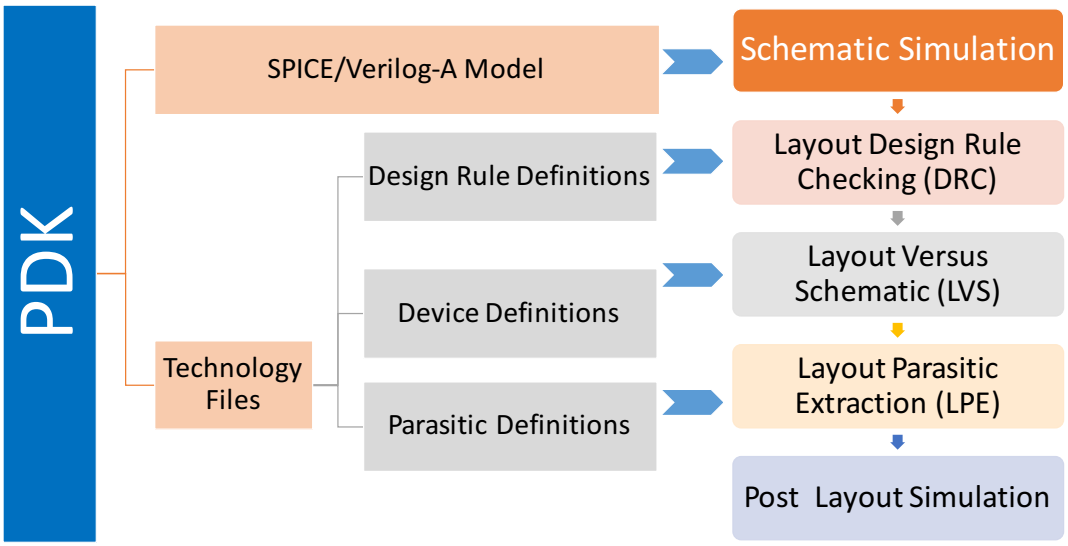


Figure 3.7: Process Design Kit (PDK) provides necessary information for the circuit design.

3.3.2 Modeling for Flexible CNT-TFTs

In this section, we first introduce the CNT-TFT compact model which takes into account the mobility dependency on the gate voltage [31]. The model also includes the contact effect which improves the accuracy for predicting the CNT-TFT behavior.

CNT-TFT Compact Model There are multiple theories for the electrical transport mechanisms of CNT-TFTs, and the most accepted theories are based on charge drift in the presence of tail-distributed traps (TDTs) and variable range hopping (VRH) [26][39]. Both theories indicate the mobility dependency on the gate voltage [31][40]: $\mu \propto (V_G - V_{th})^{\gamma},\ \gamma \geq 0$. V_{th} and γ are viewed as device parameters and complex deductions for V_{th} and γ are omitted in our analysis. The derived CNT-TFT compact model is shown in Eqs. (3.1)-(3.3), based on the well-established concept for charge drift (the deduction details can be found in [31][32]), where a limiting function $f_{\text{lim}}(x, A) = A\ln(1+\exp(\frac{x}{A}))$ is used to represent the transition from the sub-threshold region to the above-threshold region. Limiting functions have been widely used for compact modeling to provide smooth transition between different regions [32].

$$I_D = k(f(V_G, V_S)^{\gamma+2} - f(V_G, V_D)^{\gamma+2})(1 + \lambda V_{DS}) \tag{3.1}$$

$$f(V_G, V) = VSS\ln[1 + \exp(\frac{V_G - V_{th} - V))}{VSS}] \tag{3.2}$$

$$k = \frac{W\mu_0 C_{ox}}{L(\gamma + 2)} \tag{3.3}$$

Although the model is derived for n-type devices, we can easily get the p-type model by changing the polarities of voltages and currents. The model described by Eqs. (1)-(3) doesn't include the contact resistance R_C, which is caused by the current injection at the source and drain electrodes [31]. To take into account the effect of contact resistance, two series resistors are added to the CNT compact model, as shown in Fig. 3.8. With the contact resistance included, this model achieves sufficient accuracy matching the measured behavior of the CNT-TFT. The fitting results and measurements are shown in Fig. 3.9, which clearly indicates that

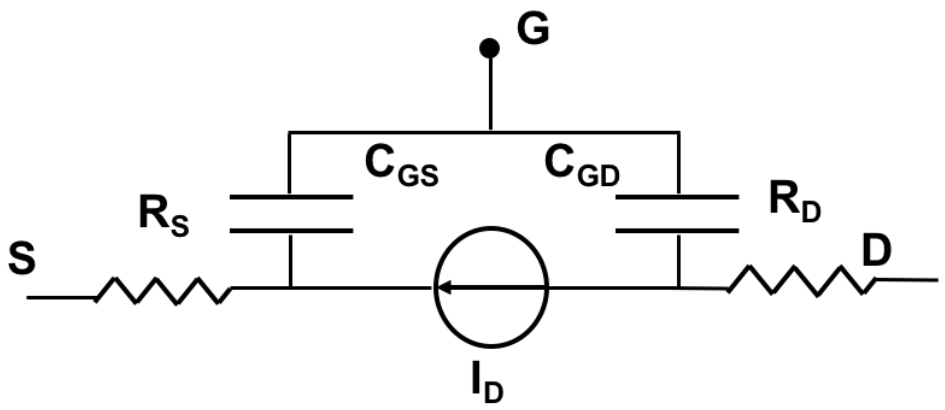


Figure 3.8: The CNT-TFT compact model.

the CNT compact model can accurately predict CNT-TFT behaviors.

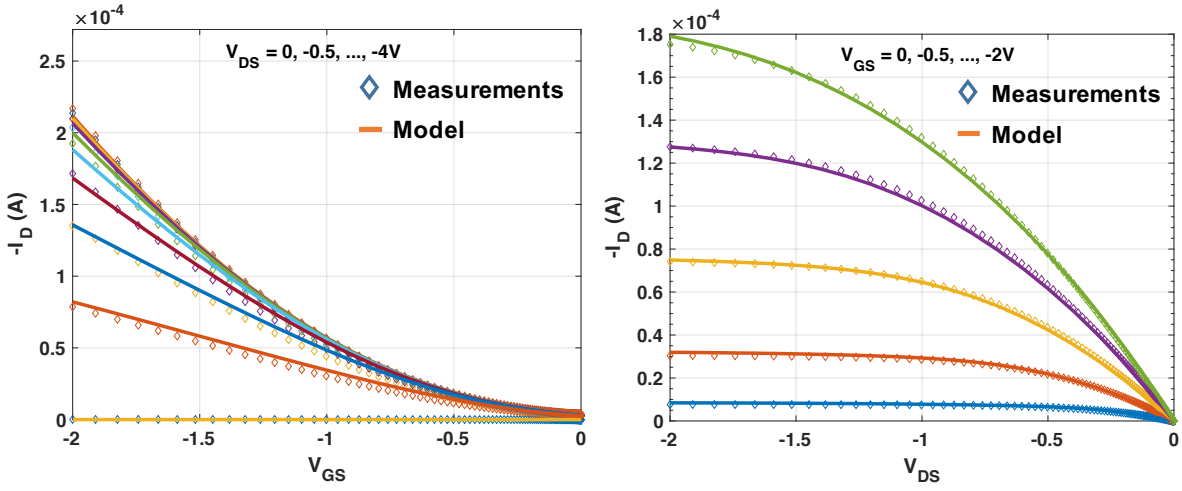


Figure 3.9: Model validation for $I-V$ curves.

Parameter Extraction To characterize the variations of CNT-TFTs, we perform nonlinear least-square optimization to automatically extract the parameters for 52 printed CNT-TFTs. Device parameters W, L and C_{ox} are directly obtained, and thus six parameters in the proposed model need to be extracted: $V_{th},\ \gamma,\ VSS,\ \mu,\ R_C$ and λ. The extraction process involves two

steps: 1) Derive an initial value for each of these parameters. For example: V_{th} is extracted as the x-axis intercept of the square root of the transfer characteristic in the saturation region and VSS is determined based on the slope in the sub-threshold region. For fitting parameters like γ and λ, an appropriated guess and lower/upper bounds would be derived. 2) Based on the extracted or guessed initial values, nonlinear least-square optimization is performed to minimize the defined error function for deriving the final values for these parameters. To achieve fitting results with greater accuracy, an error criteria including both current and conductance errors are used [32], as shown below:

$$E_I = \sum_{j=1}^{K} \{ w_{I_{D_j}} \left(\frac{\widehat{I_{D_j}} - I_{D_j}}{|\widehat{I_{D_j}}| + |I_{D_j}|} \right)^2 + w_{g_{o_j}} \left(\frac{\widehat{g_{o_j}} - g_{o_j}}{|\widehat{g_{o_j}}| + |g_{o_j}|} \right)^2 \} \tag{3.4}$$

$$g_o = \partial I_D / \partial V_D \tag{3.5}$$

Here, w_{I_D} and w_{g_o} represent the weights for current error and conductance error respectively and they are set to have the same value as the default. This error function is expressed in terms of percentage error and helps automatically reject noisy data at a low bias level.

We extracted all parameters for 52 fabricated CNT-TFTs which are summarized in Table 3.2. The table also includes the mean value μ and standard deviation σ, where a Gaussian distribution is assumed for device variations for each parameter.

Table 3.2: Parameters extracted from 52 fabricated CNT-TFTs

Model Parameter	Notation	[μ, σ] Unit
Channel Length	L	[25, -] um
Channel Width	W	[125, -] um
Gate Unit Capacitance	C_{ox}	[200, -] nF/cm^2
Threshold voltage	V_{th}	[0.5, 0.102] V
Sub-threshold Swing	SS	[0.28, 0.0388] V/dec
Effective Mobility	μ_0	[25.69, 0.19] cm^2/Vs
Contact Resistance	R_C	[1531, 291] Ω
Channel Length Modulation	λ	[0.064, 0.0185] V^{-1}
Factor of Gate Dependent mobility	γ	[0.20, 0.116] (-)

3.3.3 Modeling for Flexible Resistors

In addition to TFTs, the CNT film can also be used to produce resistors, whose fabrication process is compatible with that of CNT-TFT. With both passive components and active TFTs being available, circuits with a broader range of functionality can be built.

Flexible Resistor Modeling Modeling for the resistors is straightforward and a simple resistor model is used in our PDK, as shown in Fig. 3.10. For simplicity, the parasitic capacitor and inductor are ignored. The model contains an intrinsic part and an external part, where the external part is induced by the imperfect contact between the CNT film and the connection metal. Therefore, the total resistance R_{total} of the flexible resistor is composed of contact resistance $R_c = R_{cs} + R_{cd}$ and channel resistance R_{ch}. Here, R_{ch} is the sheet resistance of the channel and R_{sd} is the unit width contact resistance.

$$R_{toal} = \frac{R_c}{W} + \frac{R_{ch}L}{W} \tag{3.6}$$

Eq. (3.6) indicates that the R_{total} is a linear function of L if W is kept as a constant. $R_c/W = 4.78K\Omega$ is the intersection when $L = 0$, and $R_{ch}/W = 2.46K\Omega$ is the slope, as illustrated in Fig. 3.10.

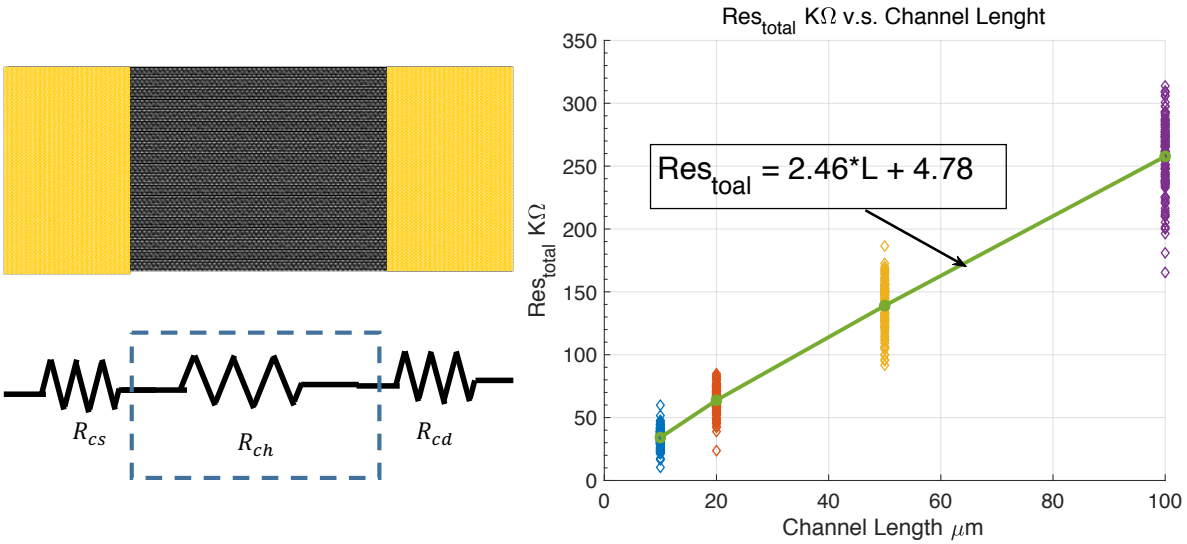


Figure 3.10: Flexible resistor analysis based on $\approx$ 500 fabricated devices with $L = 10,\ 20,\ 50,\ 100\ \mu m$ and $W = 40\ \mu m$.

3.4 Physical Verification Implementation

Physical verification is used to avoid fabricating incorrect masks and to insure a satisfactory manufacturing yield and performance [41]. Electronics Design Automation (EDA) tools have been developed and widely used for CMOS chips, which can handle extremely complex circuity with millions of transistors and more than 10 physical layers. The best approach for FE verification is to take advantage of available CMOS-centric EDA tools and focus on expressing the relevant information of our CNT technology into formats that can be directly recognized by commercial tools, as indicated in Fig. 3.11.

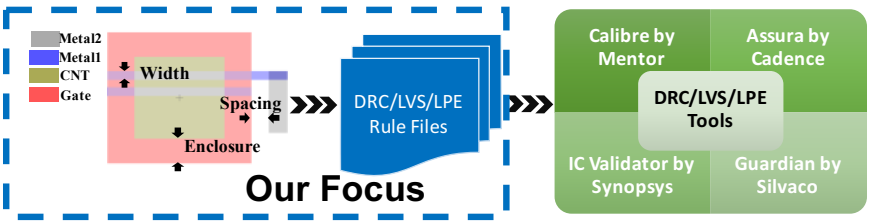


Figure 3.11: DRC, LVS and LPE Flow.

In the following, we introduce how the verification engine works and several key steps will be discussed in details. For illustration purposes, a typical physical verification rule structure is provided as below:

Physical Verification Rule Structure

Load Technology files: {
Layer Assignments;
Define Material Properties;
Define Physical Constraints}
DRC Statements : {
Local Layer Definitions;
Layer Derivations;
Rule Check Comments}
LVS Statements : {
Device Recognition;
Layout Netlist Generating;
Netlists Equivalent Checking}
LPE Statements: {
Parasitic Recognition;
Parasitic Netlist Generating}

3.4.1 Design Rule Checking (DRC)

DRC verifies whether the designed mask obeys the fabrication constraints, such as minimum widths, spacings and overlaps. According to their geometry representations, mainstream DRC approaches can be categorized as: polygon, raster (bitmap) and edge based methods

[42][43][44]. Despite the representation differences, the checking sequence is exactly the same: 1) local layer definition, 2) layer derivation, and 3) rule checking. The local layer definition is used to derive the critical regions in a layout. For layer derivation, it performs the boolean operation of basic layers, as shown in Fig. 3.12, and constructs useful regions. Thus, we can easily conduct rule checking using basic checking statements, as illustrated in Fig. 3.13.

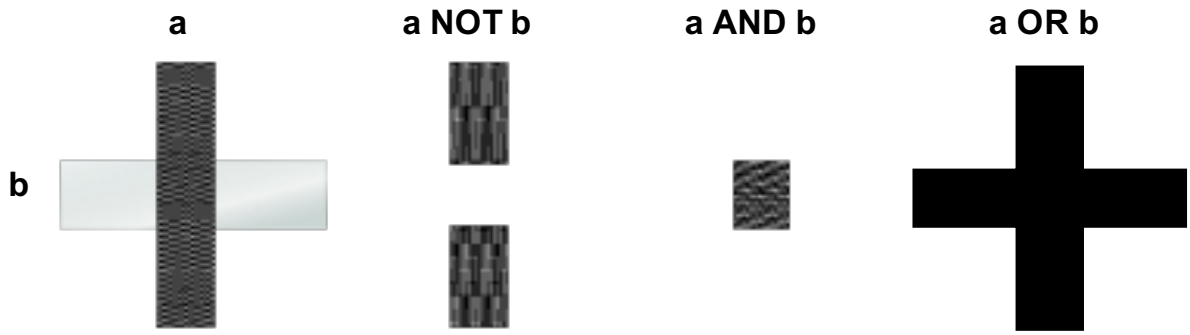


Figure 3.12: Common boolean operations of layer a and b. Boolean operations: NOT, AND and OR are demonstrated.

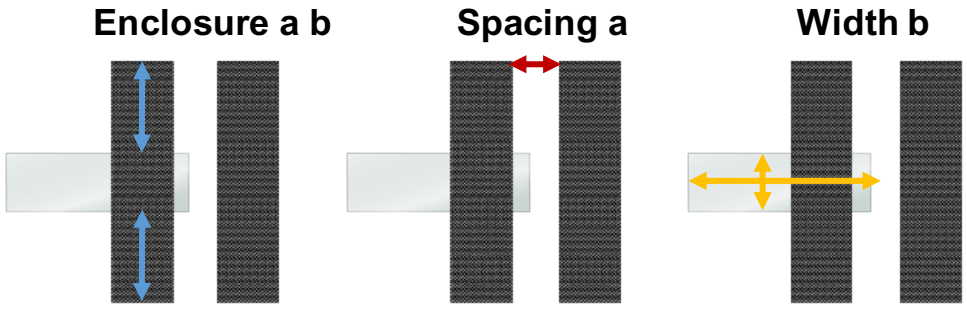


Figure 3.13: Common checking statements: enclosure, spacing and width.

The basic boolean operations of the polygon are shown in Fig. 3.12. For illustration purposes, only most common and useful operations are introduced. These operations find critical combinations of layers that comprise devices and connections. For example, the 'Source/Drain'

layer can be constructed as boolean AND of Metal and CNT layers. The combination of boolean operations (AND, NOT, OR, etc.) can generate all desired regions to facilitate the following rule checking task. Using CNT-TFT as an example, we illustrate how to use boolean combinations to derive critical regions of a CNT-TFT as below:

Exemplary Layer Derivation of CNT-TFTs				
Temp	=	CNT	AND	Gate
Channel	=	Temp	NOT	Metal
SD	=	Metal	AND	CNT
....				

Once critical regions are derived, it is straightforward to check the basic constraints: spacing, width and enclosure, as shown in Fig. 3.13.

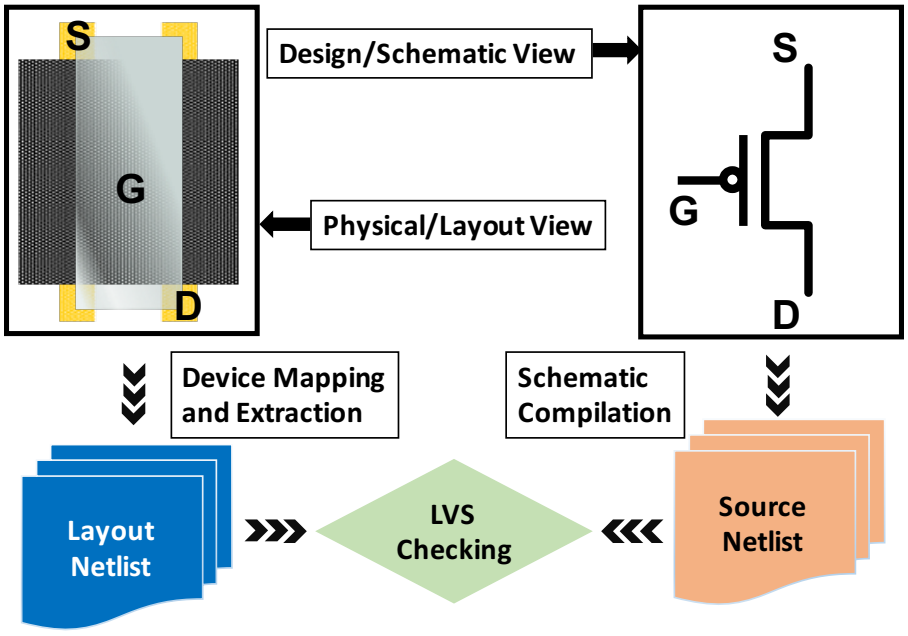


Figure 3.14: LVS principles and procedures.

3.4.2 Layout Verses Schematic (LVS)

LVS verifies the physical implementation by comparing a netlist extracted from a circuit layout to a schematic netlist that is assumed to be correct [45]. Basic procedures of the LVS are illustrated in Fig. 3.14, where netlists are extracted from both the schematic and the layout. Then, both netlists are converted into graphs and graph isomorphism is used to check their equivalence [46][47].

For the schematic view, it is straightforward to generate the netlist. However, for the layout view, we have to define the device recognition rules, which will be used to extract and generate the layout netlist. Also, device properties, such as a transistor's length and width, should be extracted as well. High level syntax of device recognition for CNT-TFTs is provided as below:

Device Recognition Example
CNT-TFT device recognition : Gate ⇔(G) SD ⇔(S) SD ⇔(D)
[**Property extraction:** L, W, AS, AD
W = Length(Channel)
L = Area(Channel)/W
AS = Area(SD)/2
AD = Area(SD)/2]

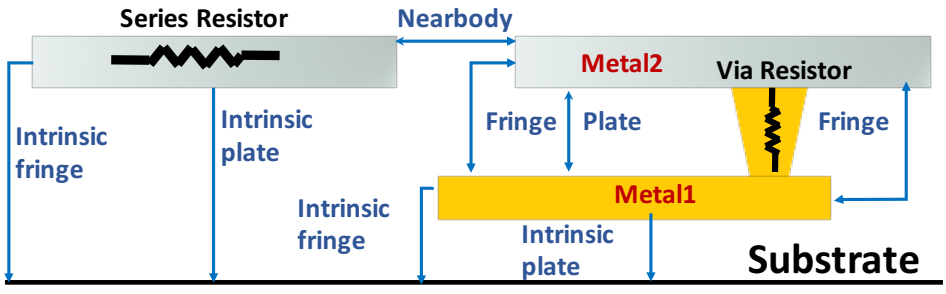


Figure 3.15: Different types of parasitic capacitors and resistors.

3.4.3 Layout Parasitic Extraction (LPE)

Parasitics in flexible electronics could be significant due to its low cost processes. Therefore, it is essential to extract the parasitic resistors and capacitors for inclusion in post-layout simulation. As shown in Fig. 3.15, the parasitic capacitors contain the intrinsic capacitors, formed between conducting layers and the substrate, and coupling capacitors, formed by nearby layers. Parasitic resistors exist in both the conduction layers and connection vias. After parasitic extraction and parasitic netlist generation, post-layout simulation can be performed for more accurate simulation results. Abstract description of parasitic recognition is provided as below:

Parasitic Recognition Example
Parasitic capacitor recognition : intrinsic or coupling
[**Property extraction:** C
C = C_{plate} * Area()+ C_{fringe} * Perimeter()]
Parasitic resistor recognition : conducting layers or vias
[**Property extraction:** R
R = R_{Sheet} * Length()/Width()]

3.5 Summary

In this part, we introduce CNT-based flexible electronics and illustrate how PDK can assist the design process of a FHE system involving schematic design, physical layout and post-layout simulation. We have developed compact models for both TFTs and resistors of our target CNT technology, which have been thoroughly validated based on measurement results of fabricated devices. Also, models and procedures for physical verification are included to enable the use of existing EDA tools for ensuring manufacturability. We believe this fully functional FHE-PDK

can facilitate innovative design of large-scale FHE systems and potentially trigger a fabless design business model for the FHE industry.

Chapter 4

Robust Flexible Circuit Design

In this part, we will discuss how we build the CNT-based robust flexible circuit with the developed models and FHE-PDK.

4.1 Introduction

Carbon nanotube (CNT) thin-film transistor (TFT) is a promising candidate for flexible and wearable electronics. However, it usually suffers from low semiconducting tube purity, low device yield, and the mismatch between p- and n-type TFTs. Here, we report low-voltage and high-performance digital and analog CNT TFT circuits based on high-yield (19.9%) and ultrahigh purity (99.997%) polymer-sorted semiconducting CNTs. Using high-uniformity deposition and pseudo-CMOS design, we demonstrated CNT TFTs with good uniformity and high performance at low operation voltage of 3 V. We tested forty-four 2-μm channel 5-stage ring oscillators on the same flexible substrate (1,056 TFTs). All worked as expected with gate

delays of 42.7 $\pm$ 13.1 ns. With these high-performance TFTs, we demonstrated 8-stage shift registers running at 50 kHz and the first tunable-gain amplifier with 1,000 gain at 20 kHz. These results show great potentials of using solution-processed CNT TFTs for large-scale flexible electronics.

High-performance flexible electronics are highly desirable for applications in wearables, healthcare, prosthetics and robotics [48, 49, 50, 51]. Carbon nanotube (CNT) thin-film transistor (TFT) is a promising candidate for high-performance flexible electronics because of its high carrier mobility, high mechanical flexibility/stretchability, and compatibility with low cost printing processes[52, 53, 54, 55, 56]. CNT TFT based circuits, such as flexible logic circuits[54, 57], and systems, such as flexible and stretchable sensors[58] and bio-medical devices[59], have been previously reported. However, to date, CNT TFT circuits were only implemented as simple ring oscillators running at low frequencies ($<$100 kHz)10 or small-scale logic circuits with a limited number of transistors ($<$50 transistors)[54]. The major obstacles include process complexity and low circuit yield due to the hybrid-integration of different types of TFT devices (ex. p-type CNT and n-type IGZO) as well as using slower and less reliable n-type CNT TFTs to realize the complementary logic. To enable large-scale flexible systems with low manufacturing costs, sensors, amplifiers and sensor interface circuits need to be integrated and fabricated on the same substrate with hundreds to thousands of transistors[60]. Flexible amplifiers and sensor interface circuits such as drivers and multiplexers are also essential for flexible/silicon hybrid systems[61]. However, a demonstrator of CNT TFT circuits with medium-to-large scale high-performance digital and analog circuits for sensor interface

and internet-of-things (IoT) applications is still missing [54, 62]. Even though much progresses have been made in CNT growth and sorting[63, 64, 65], the typical semiconducting purity of $<$99.9% of the solution purified CNTs is still insufficient for large-scale circuits. Furthermore, circuit operating speed is dependent on transistor channel length. Therefore, lack of high-purity and high-uniformity CNT network films are the current main obstacles for large-scale CNT flexible circuits with required speeds. In addition, in order to realize CMOS (complementary metal oxide semiconductor)-like CNT circuits[66, 67], unstable n-type dopants and low-work-function metals are often used, which inevitably increases the fabrication complexity and negatively impacts the device yield and uniformity. We have made many efforts on using n-type dopant for CMOS circuit fabrication. Although small-scale logics were successfully achieved in our previous work[67], large-scale integration turned out to be very challenging due to the large device-to-device variations (up to 50% for mobility) of n-type TFTs. In this work, we first report a polymer-sorting technique that achieves an ultra-high selectivity of 99.997% and a high sorting yield of 19.9%, much higher than previous reported methods (usually selectivity $<$99.9% and yield $<$5%)[68, 69]. Next, we increase the uniformity and bias stability of the flexible circuits by introducing a new type of self-assembly monolayer (SAM) for CNT absorption, adding additional barrier layers for long-time bias stability, and using bottom-contact device configuration. Benefiting from significant improvements of device uniformity and bias stability and an accurate simulation model[70], we are now able to design, simulate and fabricate large-scale CNT TFT based circuits with the pseudo-CMOS design style[71]. Our simulation results suggest that large CNT TFT device variations (e.g.

δ>20%μ) could result in a drop of noise margins $\sim$50% and an increasing circuit failure rate up to 15/500. Therefore, large-scale circuits require more emphasis on uniformity and reproducibility of device performance. Pseudo-CMOS is adopted as an alternative logic style to complementary logic, where only mono-type (ex. n- or p-type only) TFTs are needed and it can be used for either enhancement-mode or depletion-mode devices by changing the source-to-gate configurations[71]. We demonstrated high-performance 5-stage pseudo-CMOS based ring oscillators running at 3.5 MHz using only 2-μm p-type CNT TFTs. The benefits of using only high-performance p-type CNT TFTs are prominent in the circuit implementations of an 8-stage shift register consisting of 456 CNT TFTs operating at 50 kHz clock rate, as well as a tunable-gain amplifier with 1,000 voltage gain at 20 kHz. These circuits are foundational building blocks for implementing flexible sensor arrays and flexible displays. The higher speed these circuits can achieve, the more applications these circuits can be used for. Our results show that bottom-contact device configuration and p-type only pseudo-CMOS design provide an alternative device-circuit solution to realize comparable or even higher circuit speed than complementary design, in addition to simpler process complexity to enable large-scale flexible circuits.

4.2 Flexible Device Optimizations

s-SWNT TFTs were fabricated on a 4-inch carrier wafer using the device structure shown in Fig. 4.1a. A flexible substrate, either a 10 μm polyimide or a 1 μm parylene, was deposited on a carrier wafer. A thin SiNx layer (50 nm) was subsequently deposited to prevent moisture

diffusion through the polymer substrate. After lithographic patterning and deposition of the gate electrodes (Cr 35 nm, Metal Layer 1), 25 nm Al2O3 and 3 nm SiO2 were deposited as the dielectric layer using atomic layer deposition (ALD) and patterned with photolithography and wet etching. After Pd drain/source contact electrode patterning and deposition (Metal Layer 2), the SiO2 layer was functionalized with 11-(2-methoxyethoxy) undecyltrimethoxysilane to form a self-assembly monolayer (SAM). Then, the high-purity CNTs were deposited by soaking the wafer in the purified CNT solution, followed by removing the polymer residues and thermal annealing to increase the CNT adhesion (detailed procedures are provided in Methods). We found that repeating the above deposition once can increase the uniformity of the CNT networks and thus the device performance uniformity. The deposited CNTs have diameters of 1.3 1.5 nm[72] and lengths of 0.5 2 μm, and the CNT line density is about 35 40 CNTs/μm. Note that the wrapping polymers were almost completely removed after acid rinsing, which can further improve the CNT device performance and device uniformity. A negative photoresist was spin-coated on top of the CNT layer for both CNT patterning and encapsulation. Finally, a 40-nm Al2O3 encapsulation layer was coated by ALD to encapsulate all the devices. The flexible devices are subsequently characterized before and after peeling off (Fig. 4.1b). The SAM molecule design is novel. It has a hydrophobic base to reduce electrical hysteresis and a hydrophilic tail to help CNT absorption. It has been shown previously that hydrophobic surfaces help reduce interfacial traps on the dielectric surface[73]. The methyl ethylene glycol hydrophilic part is designed to enhance the CNT absorption, because we found that pure hydrophobic SAMs significantly decrease the CNT density. By combining the SAM

modification with polymer/Al2O3 encapsulation, the electrical hysteresis can be significantly reduced (Fig. 4.1c). In addition, the encapsulation was found necessary to provide a much better bias stability of the CNT TFTs (Fig. 4.1d and 4.1e). Before encapsulation, the CNT transistors showed very large on-current and off-current increase within 15s of biasing the devices. In contrast, after encapsulation, the device became much more stable over time upon gate and drain biasing. Only slightly on-current decrease and off-current increase were observed. We found that relying only on polymer encapsulation is not sufficient because moisture and oxygen can still diffuse through. Similarly, we also found that it was necessary to include a barrier layer above the plastic substrate to ensure low hysteresis and stable operation. These results indicate that the bias instability is largely due to oxygen and water doping, and proper encapsulation is important for practical applications of CNT TFTs. For the device structure, we choose the bottom-contact configuration, where source/drain electrodes are deposited below CNT networks as shown in Fig. 4.1s. Because top-contact configuration needs photolithography on CNTs, which will cause significant CNT loss during the lift-off process, and finally resulting in lower device uniformity and yield. Although bottom-contact configuration tends to show slightly lower performance than top-contact due to larger contact resistance, however, after systematic optimization and using pseudo-CMOS design, we achieved comparable or even better performance than other top-contact and CMOS-design circuits[54, 57]. We employ a photoresist layer for CNT TFT encapsulation. Since the photoresist contains a small amount of acid, the CNT TFT are slightly p-doped. However, decreasing the acid amount or using other polymer encapsulation layers can control the threshold voltages (VTh). Similarly, using

base or n-type dopant could also control the VTh. Thus, the VTh of our CNT TFTs can be controlled by different chemical dopants or different types of polymer encapsulation layers.

To obtain the electrical performance statistics, over 50 transistors were measured across a 4-inch wafer (Fig. 4.1f). We found that our fabrication method provided very high uniformity cross the 4-inch wafer with an average mobility of 23.4 $cm^2V^{-1}s^{-1}$, high on/off ratios of $>$105 and a small standard deviation of less than 10% (Fig. 4.1g). To the best of our knowledge, these values are among the highest performance and the best uniformity for wafer-scale fabricated flexible CNT TFTs. The performance and uniformity of our CNT TFTs are already comparable and even better than some oxide-based TFTs used for display applications. Note that higher mobilities up to 49 $cm^2V^{-1}s^{-1}$ has been achieved by increasing the CNT density, however, higher CNT density leads to significant larger device variations over 30%, and finally resulting lower circuits yield. Thus, we choose to use lower CNT densities for better uniformity. To test the flexibility of our CNT TFTs, the peeled-off devices were attached to a flexible polymer substrate (50 μm thickness) as the thin layer was too thin to support itself and bended to 5 mm radius (Fig. 4.1h). Only slight current changes were observed after many times repeated bending, suggesting the good flexibility of our devices.

4.3 Robust Pseudo-CMOS Digital and Analog Circuits

In addition to low electronic purity of semiconducting CNTs, another obstacle to realizing a large-scale CNT TFT circuit is the lack of air-stable and high-performance n-type CNT TFTs. The instability of the n-dopant, low-work-function metals and increased complexity of the fab-

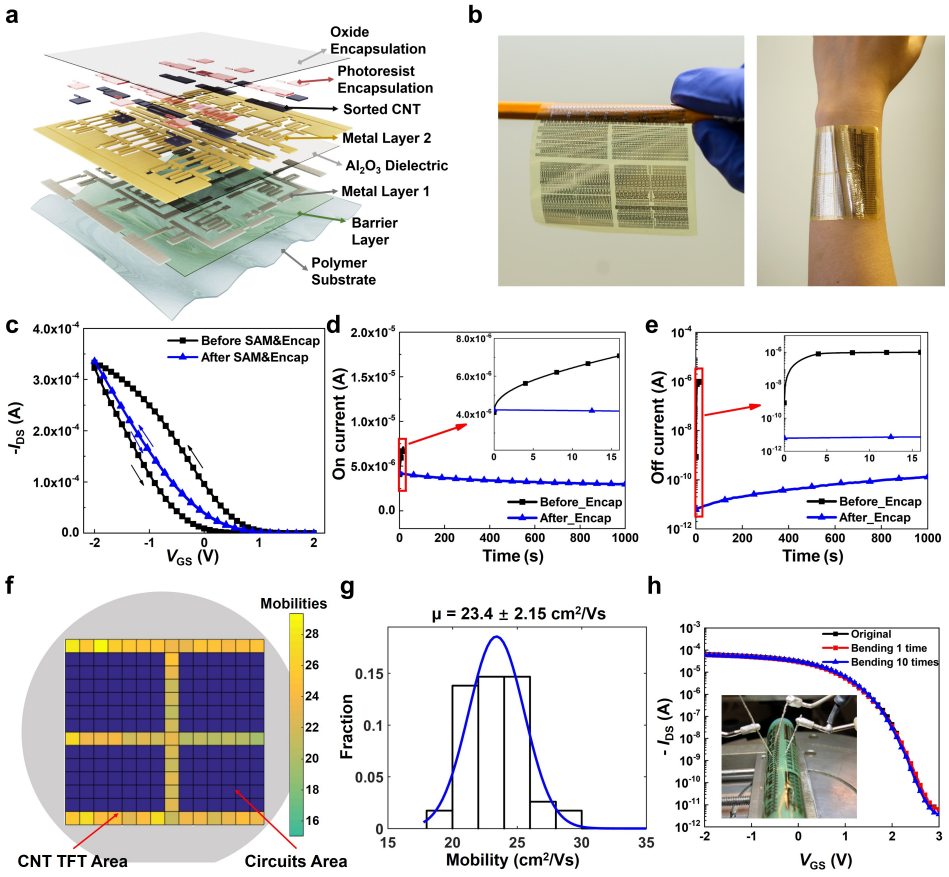


Figure 4.1: **Device layer structures and electrical characterizations of CNT TFTs on a plastic substrate.** a, Layer structures of the CNT TFT device. b, Photos of CNT TFT devices fabricated on a 10-um flexible polyimide substrate. The thin flexible devices show good conformal attachment to human skin. c, Transfer characterizations of CNT TFTs before and after SAM layer modification and Al2O3 encapsulation (VDS = -1 V). d, On-current bias stability of a CNT TFT before and after Al2O3 encapsulation. Inset shows the enlarged area (0-16s) of the bias stability test. e, Off-current bias stability of a CNT TFT before and after Al2O3 encapsulation. Inset shows the enlarged area (0-16 s). f-g, Mobility statistics from 56 CNT TFTs tested on a 4-inch wafer. The 56 CNT TFTs are distributed on the yellow areas. The colored scale bar indicates the mobility values. Dark blue areas are circuit areas and were not tested. The average mobility of CNT TFTs is 23.4 $cm^2V^{-1}s^{-1}$ with a standard deviation of 2.15 $cm^2V^{-1}s^{-1}$. h, Bending test of a flexible TFT with a bending radius of 5 mm. Only slight current changes ($<10\%$) were observed after 10 times of repeated bending. Inset shows the bending and testing setup image.

rication steps make the fabrication of n-type CNT TFTs much more challenging than their p-type counterparts[66, 67], leading to low circuit yields of complementary CNT circuits. To

address this challenge, we employ the pseudo-CMOS design style which uses only mono-type of semiconductors, either n- or p-type, while can achieve performance comparable to complementary-type logic circuits[71, 74, 75]. This alternative logic style does not only alleviate the reliance on n-type CNT TFTs, but also significantly improves the circuit speed as well as the noise margin particularly under low supply voltages[71]. Furthermore, high uniformity and stability of our CNT TFTs enable us to build an accurate device model for circuit simulation and optimization for designing large-scale high-performance pseudo-CMOS circuits using 2-μm p-type CNT TFTs. Based on these results, we show here the successful design and demonstration of several large-scale CNT-based pseudo-CMOS circuits, both analog and digital, on 4-inch flexible substrates, which include both combinational and sequential digital circuits as well as high-gain tunable amplifiers (Figs. 4.2 and 4.3).

We first built basic logic gates, including inverters, NAND and XOR logic gates, based on which any combinational circuit can be implemented. Twelve pseudo-CMOS inverters were tested whose voltage transfer characteristics showed insignificant (0.2V) hysteresis and the inverter's post-fabrication tunability through adjustment of the VSS voltage Ḟig. 4.2a shows an example of the transfer characteristics of a pseudo-CMOS inverter whose small signal gain is close to 300. The static noise margin is >0.9 V (>90% of 1/2VDD), which is a key merit of pseudo-CMOS design for enabling large-scale CNT-based flexible circuits. We further investigated the transient behaviors of the fabricated pseudo-CMOS inverter, NAND and XOR gates, as shown in Figs. 4.2b-d, respectively. The measured waveforms show correct Boolean functions and rail-to-rail characteristics with 10 20 kHz inputs. Here, voltages VDD = 3 V

and VGND = 0 V represent logic ‘1’ and ‘0’ respectively. As shown in Fig. 4.2e, 5-stage pseudo-CMOS ring oscillators with one output buffer stage were also designed, simulated, and fabricated. The 5-stage ring oscillator showed an oscillation frequency of 3.5 MHz with a stage delay of 28ns. We also evaluated tuning of the oscillation frequency based on the VSS voltage as shown in Fig. 4.2f. As VSS was varied from 0 V to 6 V with fixed VDD=3 V, there exists a quasi-linear relationship between the VSS voltage and the oscillation frequency, which is valid for different TFT channel lengths. These results indicate that the pseudo-CMOS ring oscillators can be used as voltage-controlled oscillators (VCOs) for various sensing, clocking, or communication applications. Furthermore, measured timing data for a total of forty-four fabricated 5-stage ring oscillators show an average stage delay of 42.7 ± 13.1 ns and the statistics is summarized in Fig. 4.2g. The 1056 CNT TFTs (with a 2-μm channel length) in these forty-four 5-stage ring oscillators fabricated on the same plastic substrate were all operating correctly, implying a greater than 99.9% transistor yield. Compared with the recent publication7, the performance achieved is among the best for CNT-based flexible circuits especially for low supply voltages. We believe the achievement of such a high yield and the state-of-the-art performance is due to the combined effects of high CNT purity, TFT uniformity and robust pseudo-CMOS design.

For CNT-based flexible circuits, while basic logic gates and sensors have been demonstrated previously[52, 53, 54, 58, 59], sensor interface circuits, such as shift registers, scan drivers, multiplexers, and high-gain amplifiers, were still missing. Figs. 4.3a-4.3b shows the circuit schematic and the die photo of a positive edge triggered D flip-flop (DFF), the key build-

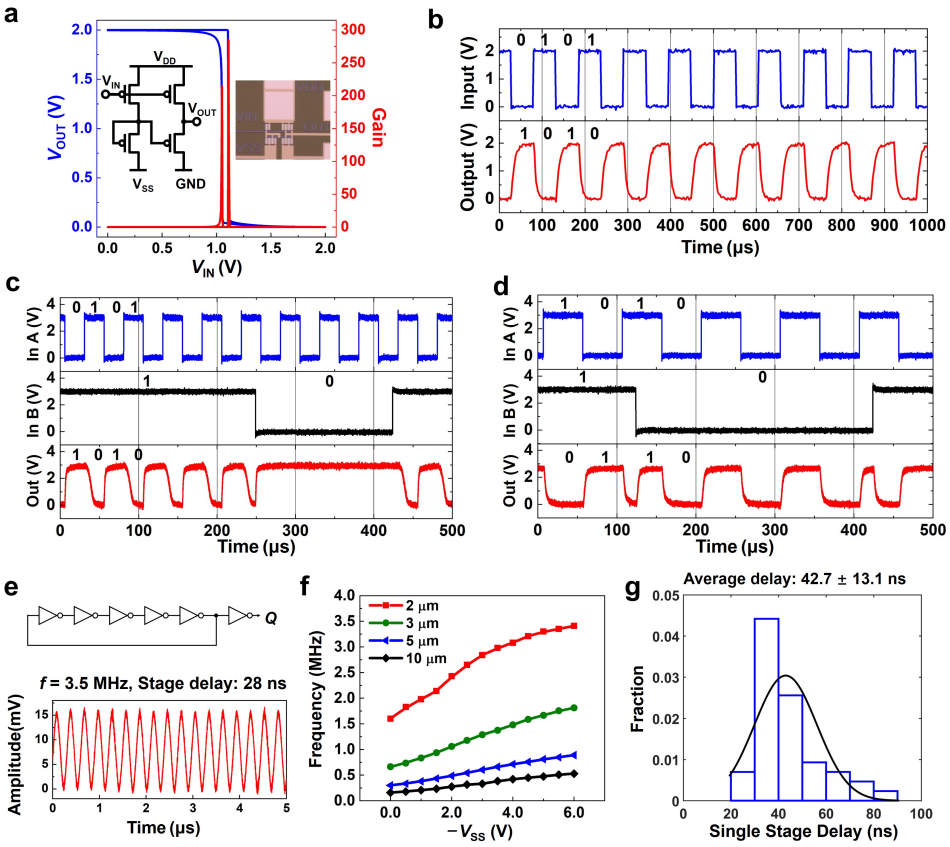


Figure 4.2: **Flexible pseudo-CMOS combinational logic gates and ring oscillators.** a, Circuit diagram of using depletion-mode TFTs, die photo, input-output characteristics and small signal gain of a pseudo-CMOS inverter. Channel length (L) = 10 um, VDD = 2 V, VSS = -3 V. b, Measured waveforms of a pseudo-CMOS inverter running at 10 kHz. L = 10 um, VDD = 2 V, VSS = -3 V c, Measured waveforms of a pseudo-CMOS NAND gate running at 20 kHz. L = 10 um, VDD = 3 V, VSS = -3 V. d, Measured waveforms of a pseudo-CMOS XOR gate running at 10 kHz. L = 10 um, VDD = 3 V, VSS = -3 V. e, Circuit diagram and output characteristics of a 5-stage ring oscillator. The ring oscillator shows an oscillation frequency of 3.5 MHz with a stage delay of 28 ns. L = 2 um, VDD = 3 V, VSS = -3 V. f, Frequency responses of the 5-stage ring oscillators under various VSS voltages and with different channel lengths. VDD = 3 V. g, Stage delay statistics of a total of forty-four 5-stage ring oscillators with VDD = 3 V, VSS = -3 V. The 5-stage ring oscillators show average stage delays of 42.7 $\pm$ 13.1 ns, comparable to current state-of-the-art CMOS-type CNT circuits.7 Note: Results of 2 um ring oscillators in e and f are from different devices and they are slightly different in performance due to process variations as shown in g. For measurement data in e, due to a large loading effect (measured to be $\sim$125 pF), the measured waveform only has $\sim$10mV scale, which is also consistent with our simulation results.

ing block of SRs. The measured waveforms of the DFF is presented in Fig. 4.3c, where the output Q samples the logic value of the input data at the rising edge of the CLK and holds the data until the next rising edge. An 8-stage serial-in, parallel-out shift-register (SR) based on such DFFs, as shown in Figs. 4.3d-4.3e, consists of a total of 456 CNT TFTs with a logic depth of 32. Fig. 4.3f shows the measured waveforms of the SR at 50 kHz clock rate and 10 kHz data rate. The challenges of realizing fast SR at 3 V are sufficient noise as well as setup/hold time margins when operating at fast clock rates, which set the foundation of using pseudo-CMOS CNT TFT circuits toward high-speed low-voltage flexible electronics in wearable or IoT applications. Figs. 4.3g-4.3h demonstrate a CNT TFT based voltage tunable-gain amplifier. In addition to fast and medium-complexity digital circuits, we also show the potentials of using CNT TFT for high-gain compact-sized amplifiers. We first developed an accurate CNT TFT device model, which was used for simulation and optimization of the design of a tunable-gain pseudo-CMOS amplifier. The final fabricated amplifier achieved a 1,000 or 60dB voltage gain at 20 kHz as shown in Fig. 4.3i, with only 9 CNT TFTs and 1 flexible capacitor. To the best of our knowledge, the measured voltage gain at given frequency ranges of this pseudo-CMOS amplifier outperforms all other flexible TFT amplifiers reported to date[60, 74, 75, 76, 77, 78]. Also, this amplifier allows the users to fine-tune the signal gain and bandwidth by adjusting the VTUNE node as shown in Fig. 4.3g. The frequency responses of the amplifier corresponding to different voltage levels of VTUNE are summarized in Fig. 4.3j. The low-frequency attenuation is due to the DC-blocking input capacitor, as shown in Figure 4.3g, to avoid any DC current flowing into the input electrode and to isolate the DC bias from external sensors. In addition

to being the first demonstration of using a single voltage VTUNE to provide post-fabrication tunability for the gain and the bandwidth, the footprint of this pseudo-CMOS amplifier is also ultra-compact (350-μm^2 excluding pads). These characteristics make this amplifier ideal for integration with various flexible sensors as a pre-amplifier to increase the signal-to-noise ratio (SNR) as well as overall sensor system sensitivity. To the best of our knowledge, this is the first demonstration of CNT-based key building blocks for sensor and display interfaces, such as shift registers (SRs) and high gain amplifiers[61].

4.4 Comparisons

To illustrate the performance and the scalability advantages of our CNT TFTs and circuit solutions, we first compare our results with recent reported CNT TFT based flexible circuits and other TFT technologies including metal oxide, organic and nanocrystal TFTs in Fig. 4.4a [54, 57, 79, 80, 81, 82, 83]and Fig. 4.4b[75, 84, 85, 86, 87, 88], respectively. Fig. 4.4a clearly shows that, in terms of circuit performance and design complexity, our measured results are among the top of recent CNT TFT circuits[75]. Although more mature metal oxide TFT technologies (blue diamond shape in Fig. 4.4b) show superior results, our CNT semiconducting layer is solution-processed at low temperature, which can be readily used for other scalable and low-cost fabrication technologies, such as inkjet printing and roll-to-roll fabrication[55]. The good mechanical flexibility and stretchability of CNT semiconducting networks also allow us to fabricate stretchable electronics that cannot be easily achieved using other traditional semiconductors[53, 89]. Besides the demonstrated scalability and performance, our

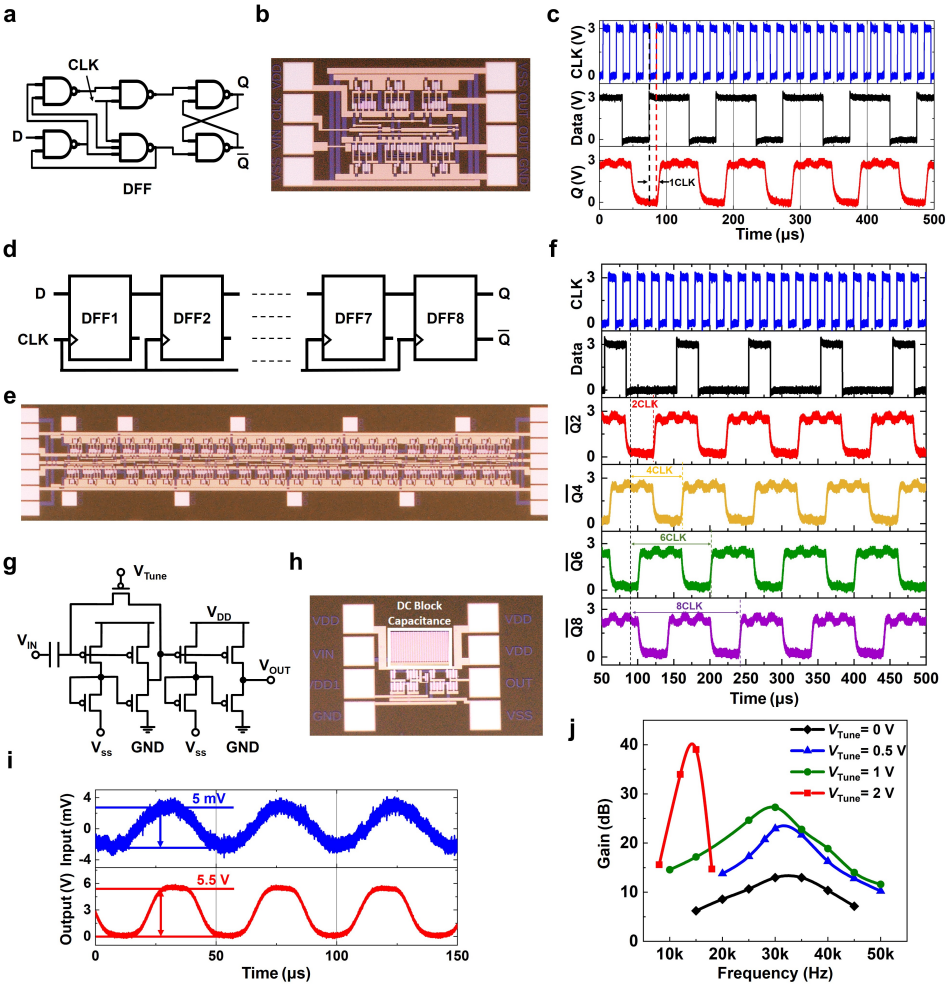


Figure 4.3: **Flexible pseudo-CMOS sequential circuits and self-biased tunable gain amplifier.** a-b, Circuit diagram and die photo of a positive edge triggered D flip-flop (DFF). c, Measured waveforms of a DFF with clock rate of 50 kHz and data rate of 10 kHz. L = 10 um, VDD = 3 V, VSS = -3 V. d-e, Circuit diagram and die photo of an 8-stage shift register consisting of 304 CNT TFTs. f, Measured waveforms of an 8-stage shift register with CLK running at 50 kHz and input data running at 10 kHz. L = 10 um, VDD = 3 V, VSS = -3 V. g-h, Circuit diagram and die photo of a self-biased tunable amplifier. i, Measured waveforms of a tunable-gain pseudo-CMOS amplifier with 5 mV input and ∼5.5 V output at ∼20 kHz and VTUNE = 3 V indicating a high gain >1,000 (60 dB). L = 10 um, VDD = 6 V, VSS = -6 V. j, Frequency responses of a tunable amplifier with VTUNE from 0 V to 2 V.

CNT based ring oscillators firstly achieved high performance (stage delay<100 ns) and low supply voltages (<5 V) at the same time, as indicated in the pink region of Fig. 4.4c, which

enables the sharing of the same supply voltage and easier integrations with silicon chips (no need for power conversions). In light of the high complexity and low device yield of the integration of n-type CNT TFTs, our pseudo-CMOS design provides an alternative device-to-circuit solution to realize comparable or even higher circuit speed than complementary design, though several limitations still exist, including higher power consumption, larger circuit area, and additional wiring.

4.5 Summary

In conclusion, we have developed a novel sorting method that can achieve high purity (99.997%) and high yield (19.9%) separation of semiconducting CNTs. Systematic device fabrication and optimization for CNT deposition, dielectric/semiconductor interface, device configuration, and encapsulations lead to high device yield, uniformity and much better bias stability. Using the developed transistor model and pseudo-CMOS design style, we have demonstrated the design, optimization, and fabrication of CNT-based circuits with superior performance and scale operating at low supply voltages. These advances can further enable new innovations in flexible CNT-based sensor acquisition systems.

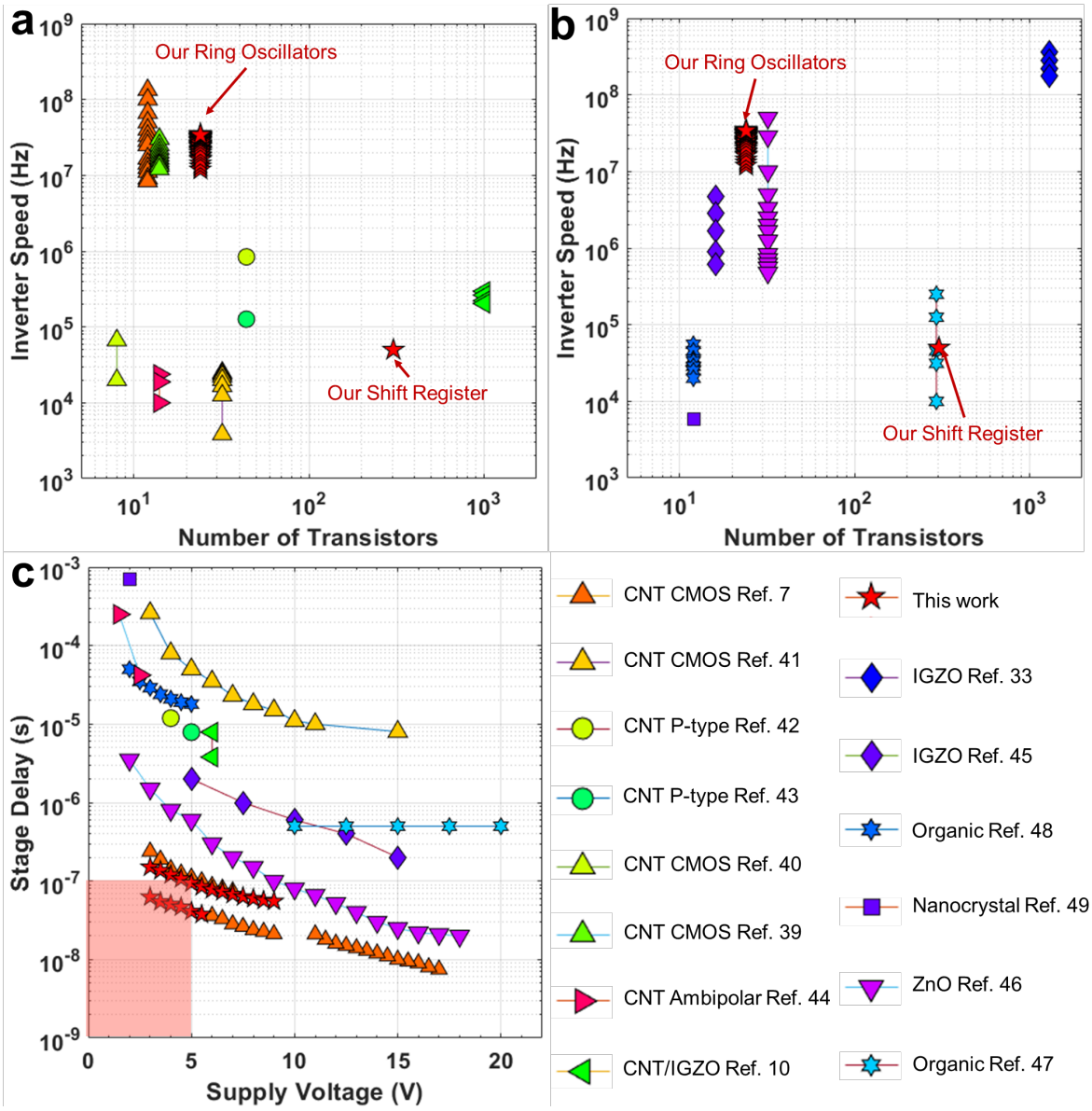


Figure 4.4: **Comparison of the circuit performance and complexity of various flexible TFT circuits.** a, Comparison of mono-type, complementary, ambipolar and hybrid CNT-based flexible circuits. The inverter speed is defined as 1/(stage delay) and the number of transistors represents the achieved circuit complexity; b, Comparison of state-of-the-art metal oxide, organic and nanocrystal based flexible circuits. c, Comparison of stage delay among representative flexible ring oscillators. To enable fair comparisons, we compared our flexible circuits with recent published results on flexible substrates not including those nanometer scale devices on rigid substrates.

Chapter 5

High Quality and Continuous Skin-Sensor-Silicon (SSS) Interfacing

In this part, we will discuss the proposed ”Active Electrode” and systematic analysis of the benefits in signal quality boosting.

5.1 Introduction

Emerging applications, from wearable, bio-medical therapy, disease prevention to electronic-skin, require flexible electronics to provide continuous, long-term and high quality human-machine interfaces with great comfortness and wearability for the users. Among flexible electronic materials, the polymers, carbon nanotubes, nano-wires and nano-crystal show great potentialsfor skin-inspired electronics [90, 91, 92] . Skin electronics, which involves flexible materials and device integration to enable skin-like properties, has enabled many desirable fea-

tures for wearable applications such as ultra-thin form factor, mechanical flexibility, stretchability and conformable adhesion to the human body [4, 5]. Among various emerging flexible materials, carbon nanotube (CNT) shows great potentials for high-performance skin electronics due to its high carrier mobility, mechanical flexibility, and low-cost manufacturing [20]. In Fig. 5.1a-b, we designed and fabricated ultra-thin ($<2\mu m$) CNT circuits along with 3D illustration of the device's layer structure, where CNT thin-film transistor (TFT) circuits are fabricated on a 1 μm polymer substrate. As shown in Fig. 5.1b, electrodes, interconnects, barrier, CNT and encapsulation layers are deposited in the illustrated order. In Fig. 5.1c, the scanning electron microscope (SEM) of various electrode on artificial skin shows that a conformable contact can be achieved with the ultra-thin circuits (<5 μm) [4]. Such a conformable contact brings not only better wearability but also effective suppression of motion induced artifacts for bio-signals detection [5]. As illustrated in Fig. 5.1d, both normal and ultra-thin electrodes are placed on the same place to record the ECG signal, when the subject moves, indicated by the red arrow, a significant motion artifact appears for a traditional electrode while an ultra-thin conformable contact electrode effectively suppresses the motion noise. Therefore ultra-thin ($<2\mu m$) CNT-TFT circuits are highly desirable for the high quality and long-term skin-sensor-silicon (SSS) interfacing for continuous health-monitoring applications.

Previous studies of skin electronics mainly focus on material and device level innovations [93, 94]. In this work, we demonstrate a skin-sensor-silicon interfacing as illustrated in Fig. 5.3 and offer systematic and quantitative analysis for the demonstration. The main focus of the SSS interface is on detecting and improving signal quality for wearable applications.

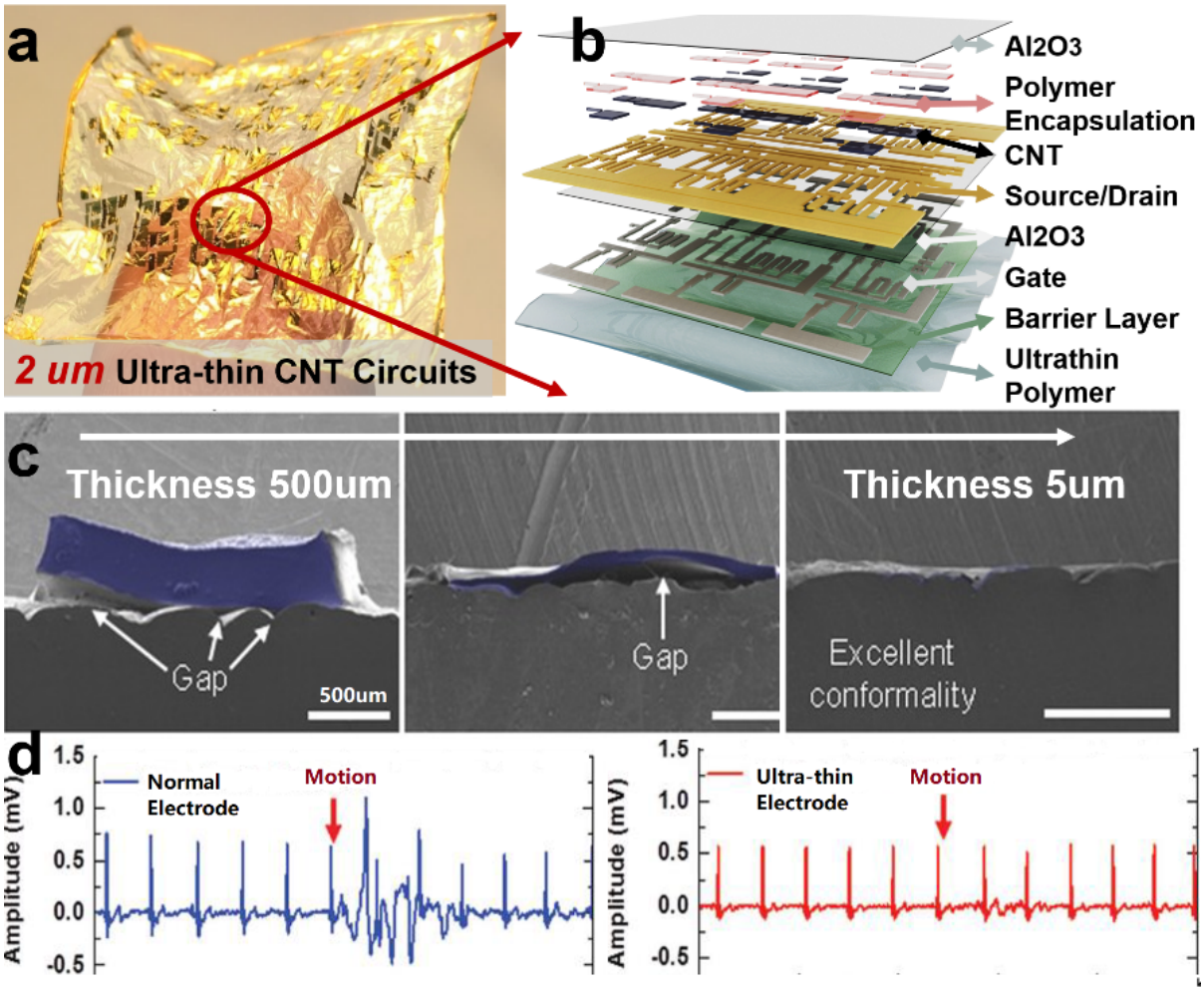


Figure 5.1: a&b. Ultra-thin flexible CNT TFT circuits [3] ; c. ultra-thin electronics enabled conformable contacts; d. motion suppression with ultra-thin electrodes. Reproduced with permission [4, 5]. Copyright 2013, 2014, Wiley .

We first demonstrate how an ultra-thin electrode can effectively reduce the motion-induced noise and we use an electrocardiogram (ECG) recording system as the use case. After identifying the noise sources in an SSS link, we further propose the ultra-thin *active electrode*, which integrates an ultra-thin CNT-TFT amplifier with the sensor/electrode as shown in Fig. 5.3b. The ultra-thin amplifier provides low-noise signal amplification for the signal-of-interest (SOI), is fully integrated with the ultra-thin electrodes, and thus greatly boosts the signal in-

tegrity. The signal quality improvement cannot be achieved by the typical configuration consisting of thick electrodes and rigid silicon amplifier located in a thick silicon chip (far away from the sensor/electrode), where noises have already entangled with the SOI in the interconnects/interfacing as indicated in Fig. 5.3. Heavy signal processing methods have been proposed to improve the signal quality [95, 96]; however, high power consumption ($>$10 mW) makes them not suitable for continuous wearable applications. Customized ASIC can achieve $<$1mW power consumption [97], but its high cost (when in low volume production) and relatively long developing periods limit its broad adoption for a wide range of applications.

In this study, we designed and fabricated an ultra-thin *active electrode* with an integrated ultra-thin CNT-TFT amplifier, successfully achieving a voltage gain of 32dB running at $\sim$20 kHz, shown in Fig. 5.4. To quantify the improvement of signal quality achieved by the proposed *active electrode*, we develop an end-to-end simulation framework for an SSS link including the skin, the sensor, the amplifier, interconnects and a classifier for atrial fibrillation (AF) detection, shown in Fig. 5.5. The framework enables analysis of how front-end SSS design affects the overall system performance, such as the classification accuracy for AF detection. The main contributions of this work are summarized as follows:

- Proposed an ultra-thin *active electrode* which integrates an ultra-thin flexible amplifier with the electrode, opening a brand new design space for skin-sensor-silicon interfaces.

- Designed and prototyped an ultra-thin CNT-TFT amplifier with a gain as high as 32dB running at $\sim$20 kHz, which provides clear evidence of the feasibility of the proposed *active electrode* design.

- Developed an end-to-end simulation framework which takes into account all relevant elements including the skin-sensor-silicon interface and the machine learning classifier, enabling systematic exploration and analysis of the impacts of front-end SSS interface on the overall classification accuracy.

- Quantitatively evaluated how the proposed *active electrode* can improve the signal quality under motion noises (achieving >35dB signal-to-noise ratio (SNR) boost) and how the front-end SSS design affects the overall classification accuracy (boosted from 65.5% to 84.6%).

The rest of this work is organized as follows: Section 5.2 introduces the SSS interface and our prototyped *active electrode*. Section 5.3 elaborates the end-to-end simulation framework including skin, sensor, amplifier and a deep-learning based classifier. Quantitative experimental results are described in Section 5.4. Section 6.4.3 discusses possible directions for future improvements. Section 6.5 draws some conclusion.

5.2 Skin-Sensor-Silicon Interfacing

A high quality skin-sensor-silicon (SSS) interface is critical for acquiring high-quality biological signals, while traditional Ag/AgCl electrodes with wet conductive gels could not ensure comfortable user experience particularly for continuous monitoring. Dry electrodes are more comfort to wear, however, they are more vulnerable to motion artifacts and interconnects noise [98, 99]. In contrast, ultra-thin skin electronics provides a promising solution to high quality

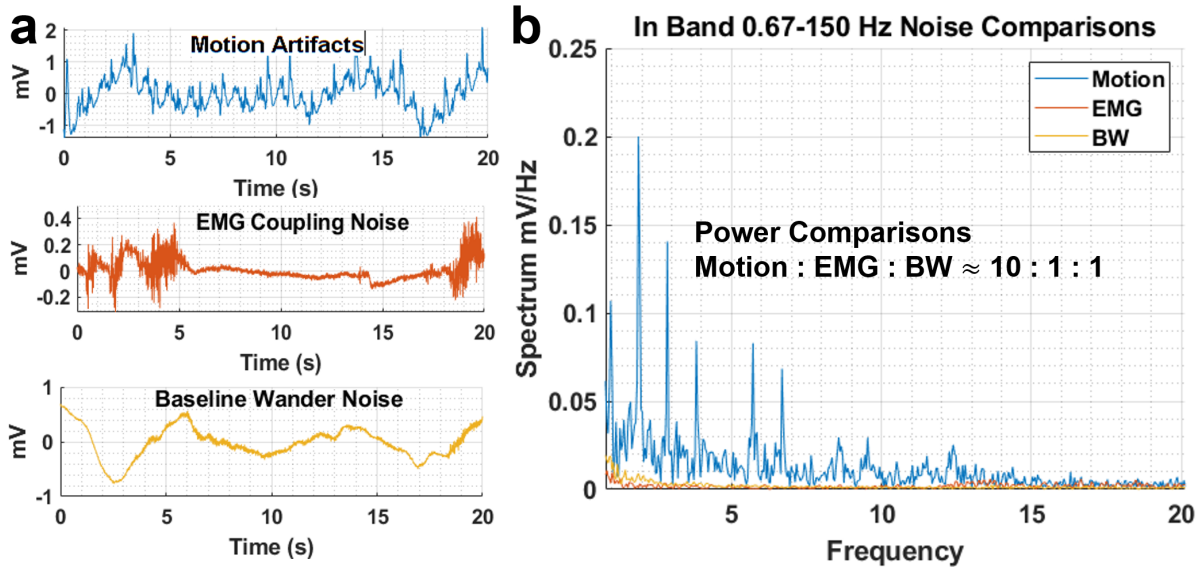


Figure 5.2: Three main noises for ECG recording system; a. waveforms of different noises; b. spectrum analysis (only 0-20 Hz is shown here) and power comparisons (integral over 0.67-150 Hz).

interfacing suitable for long-term monitoring.

5.2.1 Noise Suppression via Near Sensor Amplification

In an electrocardiogram (ECG) recording system, there are mainly three noise sources: baseline wander (BW), electromyography (EMG) and motion artifacts/interference [96]. The noise signals used in this study are from the PhysioNet MIT-BIH noise stress database [100]. Typical samples of these three noises, in both time and frequency domain, are shown in Fig. 5.2. As illustrated, the BW noise lies mainly in the low frequency domain (<0.5 Hz), which can be filtered out using a high pass filter. EMG and motion noises are relatively widespread over 0-500 Hz. Our driving application in this study is atrial fibrillation (AF) detection, whose useful information mainly lies within 0.67-150 Hz [101]. Thus, we compared these three noises'

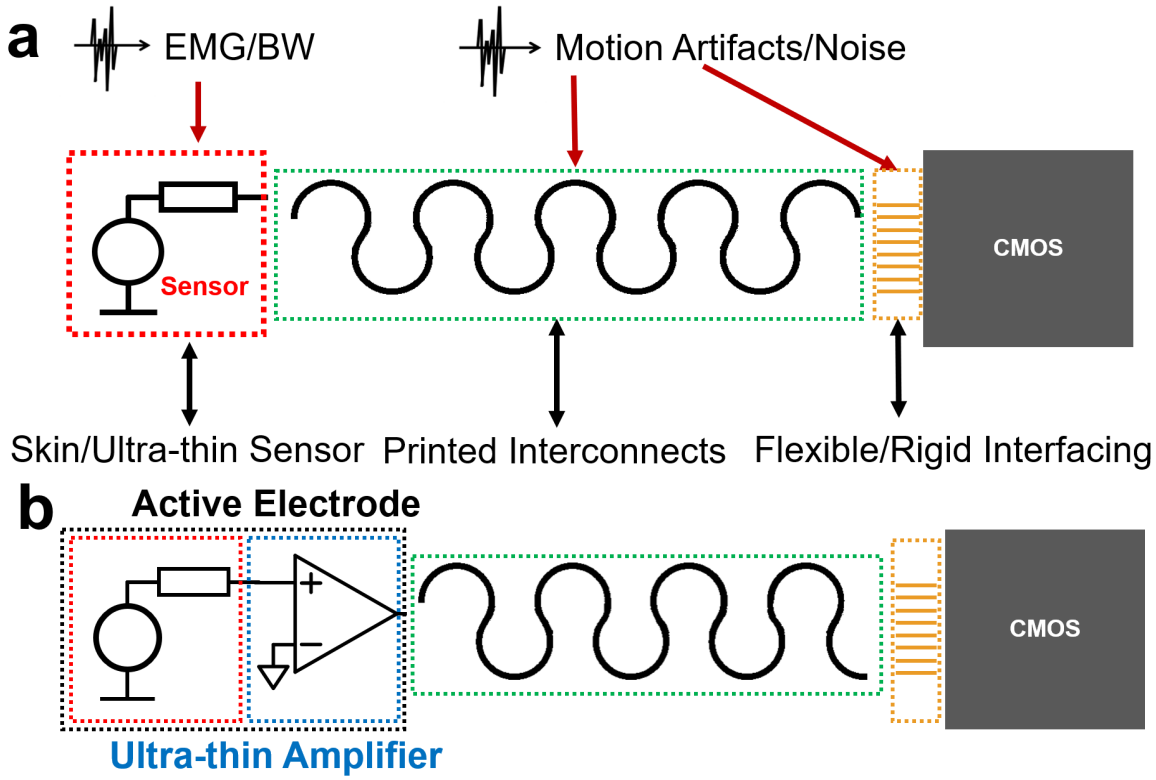


Figure 5.3: a. Illustration of a Skin-Sensor-Silicon interface; b. proposed ***active electrode*** by integrating ultra-thin amplifiers with the electrode.

power in the band of 0.67-150 Hz. The motion noise turns out to be the most significant noise source (Motion:EMG:BW≈10:1:1), for which an ultra-thin skin electronics could effectively overcome such motion artifacts.

As presented in Fig. 5.3a, the motion artifacts can be suppressed with an ultra-thin electrode which also offers conformable contacts with skin; however, the subsequent parts, such as interconnects and flexible/rigid interfacing, are still vulnerable to the motion noise. To further improve the signal quality for such an SSS interfacing, we propose a novel *active electrode* design, which integrates the electrode with an CNT-TFT ultra-thin amplifier to effectively suppress motion artifacts and interconnects' interference. This idea is demonstrated in Fig. 5.3b,

where signal-of-interest (SOI) is pre-amplified by the ultra-thin integrated amplifier. For study its feasibility, we designed and prototyped an ultra-thin CNT-TFT based amplifier, which will be elaborated in the following subsection.

5.2.2 *Active electrode* for the SSS Interfacing

Most previous reported TFT based amplifiers are thicker than 50 μm [102, 103, 104], which cannot meet the stringent requirement of conformability for seamless contacts. The organic TFT based amplifier reported in [102] achieves a thickness of less than 5μm; however, it's 3 dB bandwidth is less than 20 Hz, which cannot meet the performance requirement of most bio-signal applications.

Here, for the first time, we report an ultra-thin *active electrode* integrated with a CNT-TFT based amplifier, which achieves both an ultra-thin form factor and a bandwidth greater than 10 kHz running at 20 kHz. In contrast to [102], which required manual efforts to wire electrodes with the amplifier, we integrated everything in one ultra-thin substrate. Unlike silicon circuits, most flexible TFT circuits operate $\sim$1-100 kHz due to the limited temperature tolerance of the ultra-thin substrate [105, 3]. Thus, in comparison with the state-of-the-art flexible circuits [103, 104, 102], the performance of our fabricated CNT-TFT amplifier is highly competitive. Please note that $\sim$GHz performance has been reported for CNT based nanometer devices using high temperature silicon process on a rigid substrate, which is completely different from CNT-TFT devices fabricated on a flexible substrate.

The die photo and schematic of the fabricated *active electrode* is shown in Fig. 5.4a-b. The

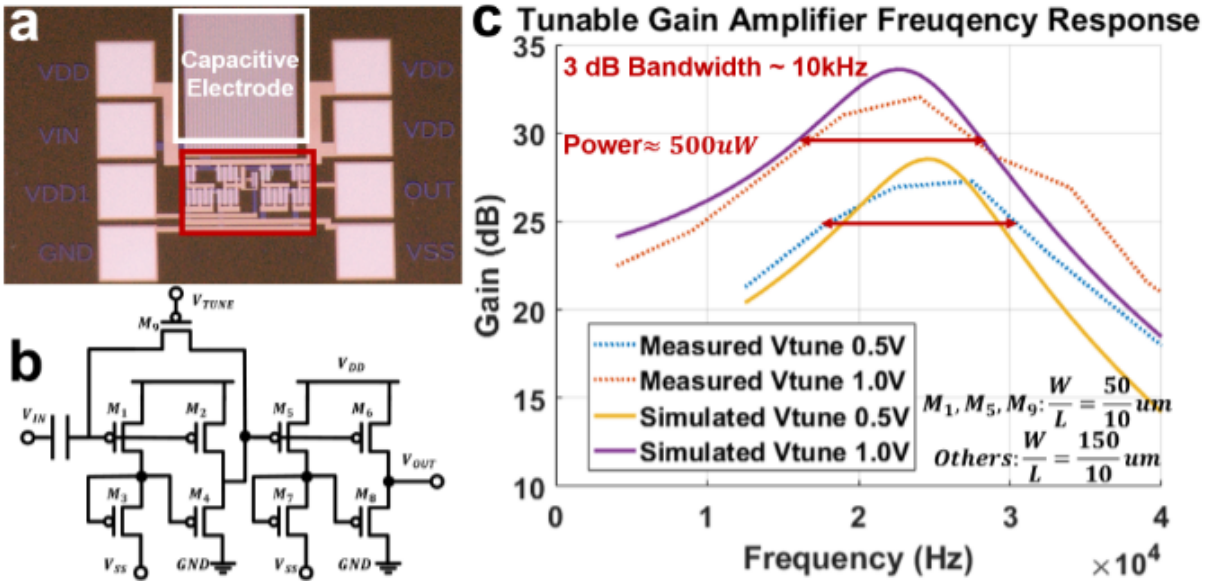


Figure 5.4: a&b. Die photo and schematic of the ultra-thin *active electrode* prototype; c. measured frequency responses of the amplifier and simulated results based on the device's compact model. $\mathbf{V_{DD} = 3V, V_{SS} = -3V}$.

total area of the *active electrode* is only (∼300x650 μm^2 excluding pads), where the white block is the electrode/sensor and the red block is the two-stage CNT-TFT based amplifier using only p-type devices. The fabrication of stable n-type CNT-TFTs remains a longstanding challenge and the performance is much worse than the p-type devices [30, 106], thus a mono-type design style, named Pseudo-CMOS [29], is used to design the two-stage amplifier ($M_1 - M_8$). One additional feedback transistor (M_9) is used to control the feedback path and to provide tunability for the frequency response.

As shown in Fig. 5.4c, adjusting V_{tune} can tune the frequency response, which offers greater flexibility and support broader application scenarios for the proposed *active electrode*. The low-frequency attenuation is determined by the effective capacitance value of the electrode. And, the overall frequency response can be optimized by properly sizing the transistors and

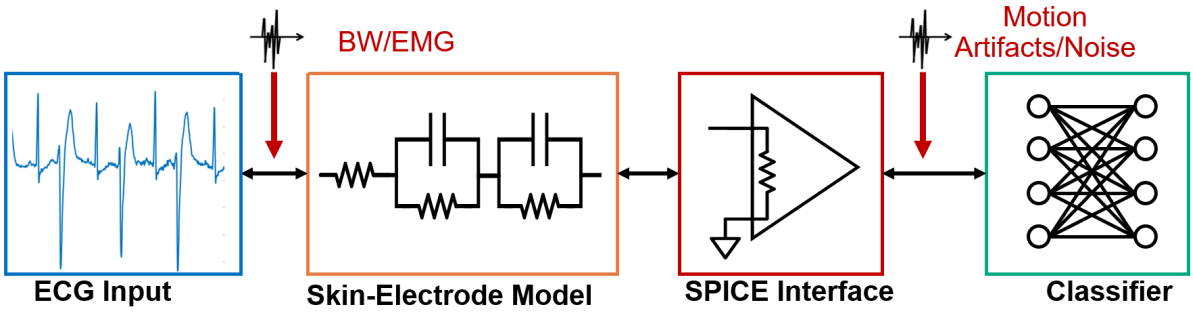


Figure 5.5: Developed end-to-end simulation framework, from emerging skin-sensor-silicon interface to machine learning classifier.

choosing a suitable dielectric material. In addition to achieving the state-of-the-art performance (∼32 dB gain and ∼10 kHz 3 dB bandwidth), the peak power consumption of the *active electrode* is ∼500 μW only at a supply voltage of 3V, which makes sharing of the power supply with silicon circuits without power conversion feasible. A designated *active electrode* for the ECG application will be described in Sec. 5.3.

The demonstrated performance, size, power consumption, and conformability of the proposed ultra-thin *active electrode* show its great potentials for bio-medical applications, such as ECG, EMG, electroencephalogram (EEG) and electrooculogram (EOG) (which usually require a bandwidth <2 kHz [107]). There are several directions for further improvement of the amplifier design, which will be discussed in Sec. 6.4.3.

5.3 End-to-end Simulation Framework

In this section, we introduce a simulation framework for systematic and quantitative analysis of an SSS link based on the *active electrode*. As shown in Fig. 5.5, the framework contains four main parts: the ECG inputs (including noise), the skin-electrode model, the SPICE model

for CNT-TFT based amplifiers and the deep learning-based classifier for atrial fibrillation (AF) detection. We built this framework in MATLAB with customized interfaces to the SPICE engine and the AF classifier. This framework, enabling us to systematically explore and analyze how front-end skin-sensor interface will affect the overall classification accuracy, will be open-sourced to enable further innovations on skin electronics based on active electrodes. In the following, we introduce the setup for each of the four parts.

5.3.1 ECG and Noise Database

Experiments in this study use ECG signals from the PhysioNet MIT-BIH database for performance analysis [101]. A typical waveform and spectrum of the MIT-BIH sample is shown in Fig. 5.6a-b. Later, we will use the AF detection for ECG as a driving application to evaluate the improvement achieved by the *active electrode*. Critical information for AF detection lies within 0.67-150 Hz, which is an important guideline the amplifier design [108, 109].

Noise injection: To simulate the noisy ECG signals, noises from the MIT-BIH noise stress database [100] are added to the clean ECG signal described as following:

$$Noisy\ ECG = Clean\ ECG + \alpha * Noise \tag{5.1}$$

$$SNR = 10log(S_{power}/(N_{power} * \alpha^2)) \tag{5.2}$$

where S_{power} and N_{power} stand for the signal power and the noise power respectively and α is a scale factor. Based on Eqs. (5.1)-(5.2), we can generate noisy ECG signals with various SNR levels.

Table 5.1: Equivalent Parallel RC Model

RC model	Skin	Electrode	Small Gap	Large Gap
R (Ω)	10K	1M	10M	100M
C (F)	N/A	10n	200p	20p

5.3.2 Skin-electrode Equivalent Model

The skin-electrode contact can be modeled as series of parallel RC circuits, where each coupling layer, such as the skin, the electrode dielectric and the air gap, can be modeled by a RC equivalent circuit and such a simple RC approximation turns out to be sufficiently accurate for analyzing low frequency bio-medical signals (<2 kHz) [99]. Typical RC values for the skin, the electrode dielectric and air gaps are summarized in Table 5.1.

5.3.3 Ultra-thin CNT-TFT Based Amplifier

We used the recently developed SPICE model for the CNT-TFT [105], which has been thoroughly validated with wafer level CNT-TFT devices and circuits, for simulation and optimization of the amplifier. We extracted all model parameters based on our CNT-TFT's measurements and validated the results with measurement from the fabricated amplifier as shown in Fig. 5.4c, where simulation results match well with the measured frequency responses. After confirming strong correlation between simulation and measurement results, the CNT-TFT model is used for design and optimization of the amplifier. Specifically, we follow the same topology described in Fig. 5.4b and optimize transistor sizes for AF detection from the ECG signals. Using long-channel ($100\mu m$) devices and optimized CNT-TFT ratios, the amplifier achieves great amplification (>30 dB when V_{tune}>$2V$) meanwhile no attenuation is introduced ($\sim 0^{\circ}$

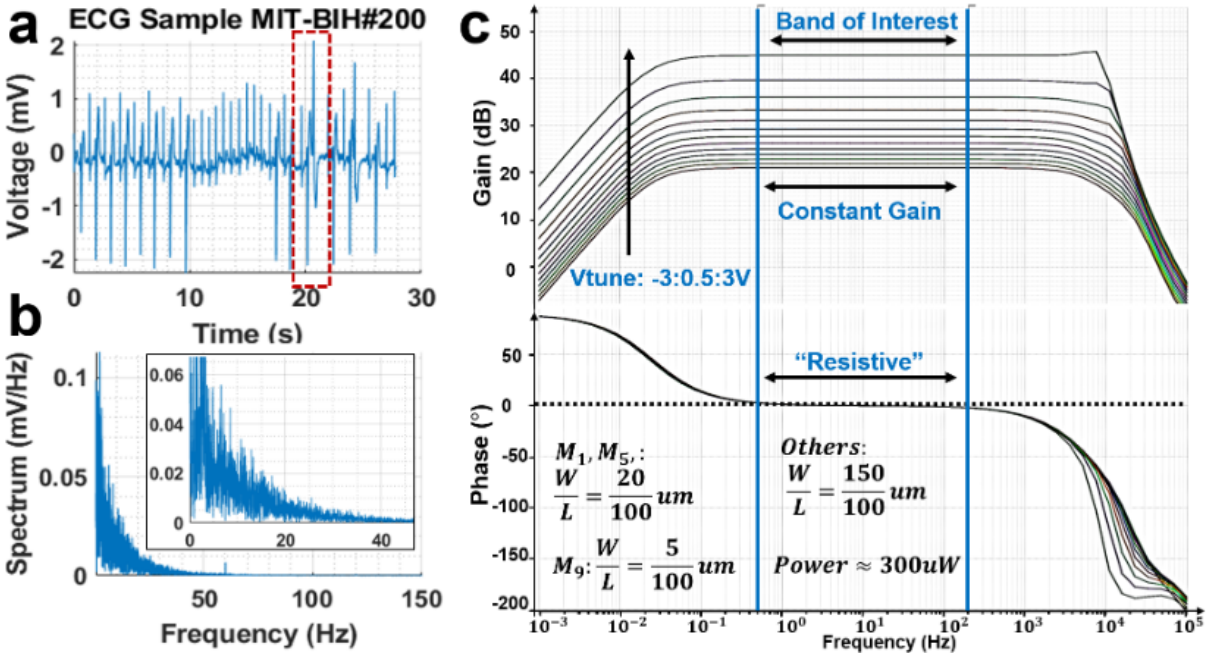


Figure 5.6: a&b. Recording of a MIT-BIH ECG signal; c. designed amplifier for ECG applications.

phase shift) in the band of 0.67-150 Hz, which is well-suited for ECG signals as shown in Fig. 5.6c.

5.3.4 Atrial Fibrillation Classifiers

Electrocardiogram (ECG) recording is an important clinical tool for detecting cardiac disorders. Among them, atrial fibrillation (AF) is the most prevalent cardiac arrhythmia and can occur in sustained or intermittent episodes [108]. We benchmarked a feature-based and a deep learning approach on single-lead ECG recordings for the task of AF detection. The feature-based approach extracts various hand-crafted features on time/frequency domain, including heart rate variability (HRV) and morphological characteristics [109], and then feed them to a random forest for classification. However, as shown in Fig. 5.10a the change of rhythm from

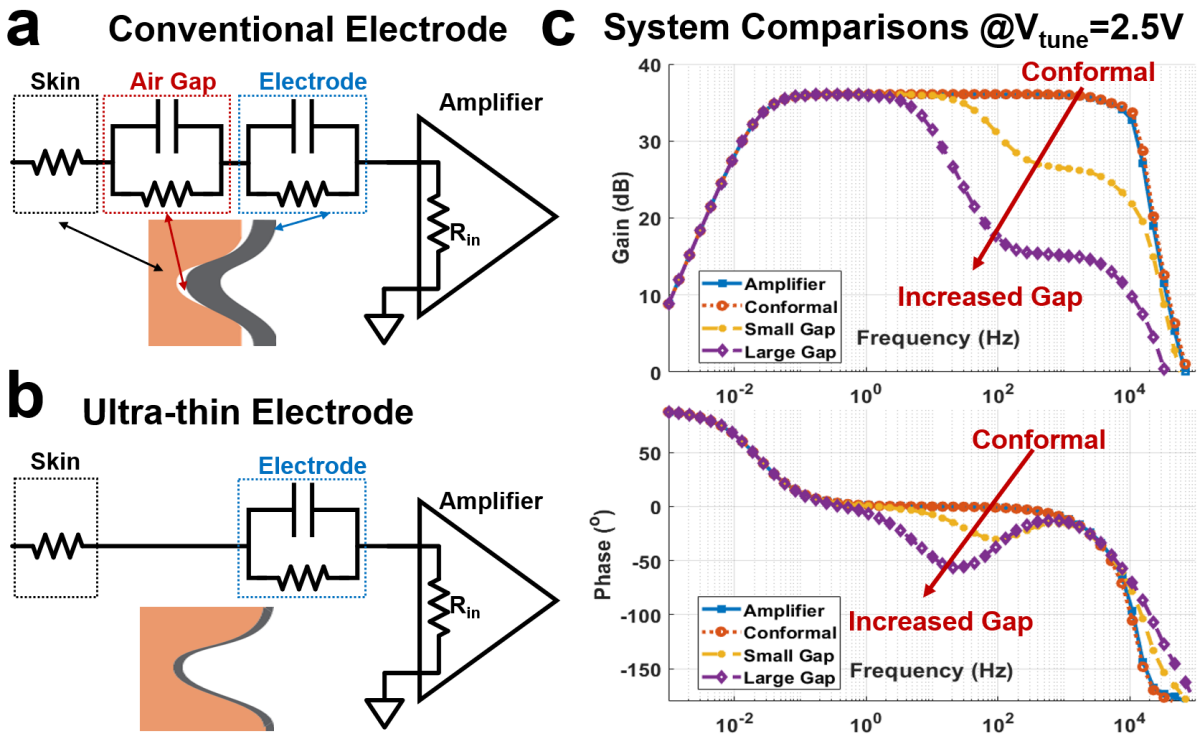


Figure 5.7: Attenuations in the frequency domain.

normal to AF ECGs has high variations, and such generic features may not be sufficient to fully represent the underlying characteristic of ECGs. Against this backdrop, we evaluated deep learning-based approach to automatically learn features at multiple levels of abstraction. Specifically, we deployed ResNet [110] as the network structure, of which the convolutional layer is the major feature learning component. The network takes fixed-length segments of 5 seconds each as input and produces a prediction for each segment. The overall classification for an entire ECG signal is the average of individual, segment-wise predictions. These two classifiers are used to quantify the impact of the front-end SSS design on the system level classification accuracy.

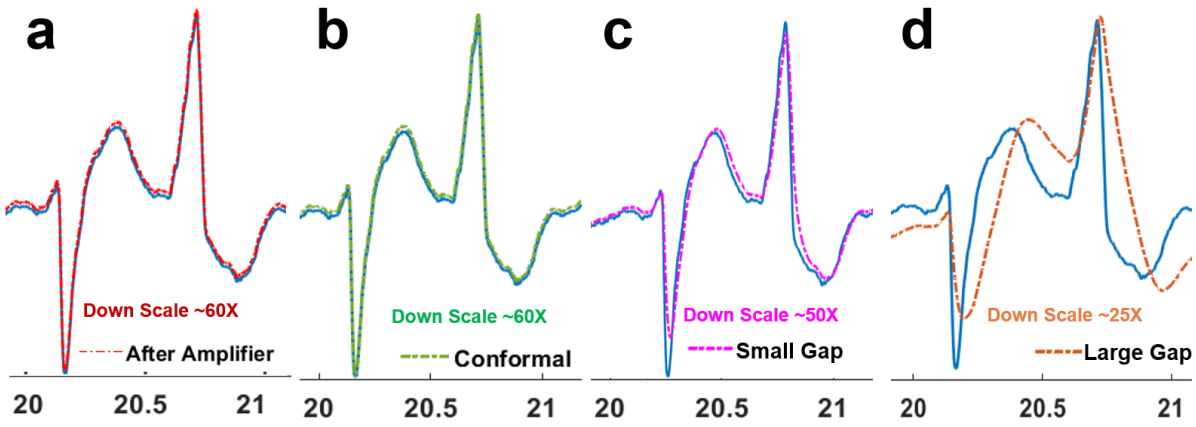


Figure 5.8: Attenuations in the time domain.

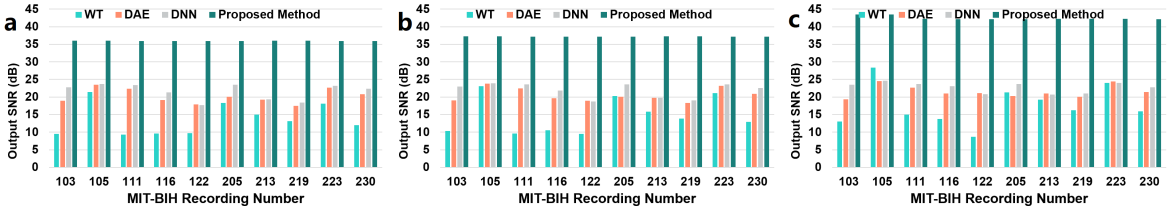


Figure 5.9: Simulated output signal's SNR under different motion noise levels: a. SNR=0 dB; b. SNR=1.25 dB; c. SNR=5 dB.

5.4 Simulation Results and Analysis

With our simulation framework, we conducted both frequency and time domain analysis, which provides comprehensive evaluation. First, we analyzed the benefits brought by the conformable contact, which essentially eliminates the attenuation caused by air gaps. We then examined the SNR boosts achieved by the *active electrode*. We also made comparisons with advanced signal processing methods. Finally, we investigated the impact of the input ECG's SNR on the

Table 5.2: Evaluations under BW and EMG noises.

BW Noise	MIT-BIH #	103	105	111	116	122	205	213	219	223	230	Average
Input SNR	0.00	2.66	2.68	2.64	2.56	2.55	2.57	2.67	2.65	2.63	2.61	2.616
	1.25	3.91	3.93	3.89	3.81	3.80	3.82	3.92	3.90	3.88	3.86	3.866
	5.00	7.66	7.68	7.64	7.56	7.55	7.57	7.67	7.65	7.63	7.61	7.616

EMG Noise	MIT-BIH #	103	105	111	116	122	205	213	219	223	230	Average
Input SNR	0.00	-3.05	-3.03	-3.06	-3.15	-3.15	-3.14	-3.04	-3.06	-3.08	-3.10	-3.086
	1.25	-1.80	-1.78	-1.81	-1.90	-1.90	-1.89	-1.79	-1.81	-1.83	-1.85	-1.836
	5.00	1.95	1.97	1.94	1.85	1.85	1.86	1.96	1.94	1.92	1.90	1.914

accuracy of the AF classification.

5.4.1 Ultra-thin Electrode Enabled Attenuation Reduction

The equivalent circuit diagrams of a traditional electrode and an ultra-thin electrode are shown in Fig. 5.7a-b, where the air gap is eliminated by a conformable contact of the ultra-thin electrode. Based on the RC parameters in Table 5.1, we simulated the frequency response of the skin-sensor-amplifier interfacing with a conformable contact, a small air gap and a big air gap respectively and summarized the responses in Fig. 5.7c. We can observe that the unavoidable air gap of a traditional electrode introduces attenuations in both gain and phase of the skin-electrode-amplifier link. For the time domain analysis, we chose an ECG segment with sharp dynamic behaviors, indicated by the red block in Fig. 5.6a, which has rich information in the frequency domain. For better visualization, we scale the amplitude of the output waveform and overlap it with the input waveform. As shown in Fig. 5.8, there are significant discrepancies and attenuations caused by the air gap while the conformable electrode shows great consistency between the input and output waveforms. For traditional electrodes, the air gap varies and the motion changes lead to unpredictable attenuations and noises, which pose significant challenges for AF detection. On the other hand, ultra-thin electrode minimizes the motion induced noises as the air gaps are eliminated.

5.4.2 *Active Electrode* Enabled SNR Boosts

In this following, we analyze the improvement to signal quality due to the *active electrode* under the motion artifacts, the BW noise and the EMG noise. Locations to inject these noises in an SSS link are indicated in the Fig. 5.5. Since the motion noises are suppressed for the ultra-thin *active electrode*, we assume that the motion noise mainly impacts the interconnects between flexible electrode and rigid silicon chip. EMG and BW noises, caused by body potential changes, are thus mixed with the ECG signal at the origin of the SSS link. In principle, the proposed method should be able to effectively overcome the motion noise while no significant difference would be observed for BW and EMG noises. We examine the SNR improvement under the motion noise first followed by evaluation with EMG and BW noises.

Comparison under the motion noise: We compared the SNR improvement achieved by our proposed method with those purely based on signal processing methods, such as wavelet transform (WT), denoising auto-encoder (DAE) and deep neural network (DNN) methods [95, 96]. For a fair comparison, the same 10 PhysioNet ECG recordings are chosen for the analysis and three different input SNR levels, 5 dB, 1.25 dB and 0 dB respectively, are generated based on Eqs. (5.1)-(5.2) for simulation. The simulation results are summarized in Fig. 5.9, where x-axis is the ECG recording index and y-axis is the output signal's SNR. The ultra-thin *active electrode* clearly outperforms all state-of-the-art signal processing methods for motion suppression under a wide range of noise levels. The peak power consumption of the *active electrode* is only about 300 μW, which shows significant energy saving compared to the heavy signal processing methods ($>$10 mW). Note that our method is a hardware-based solution which can

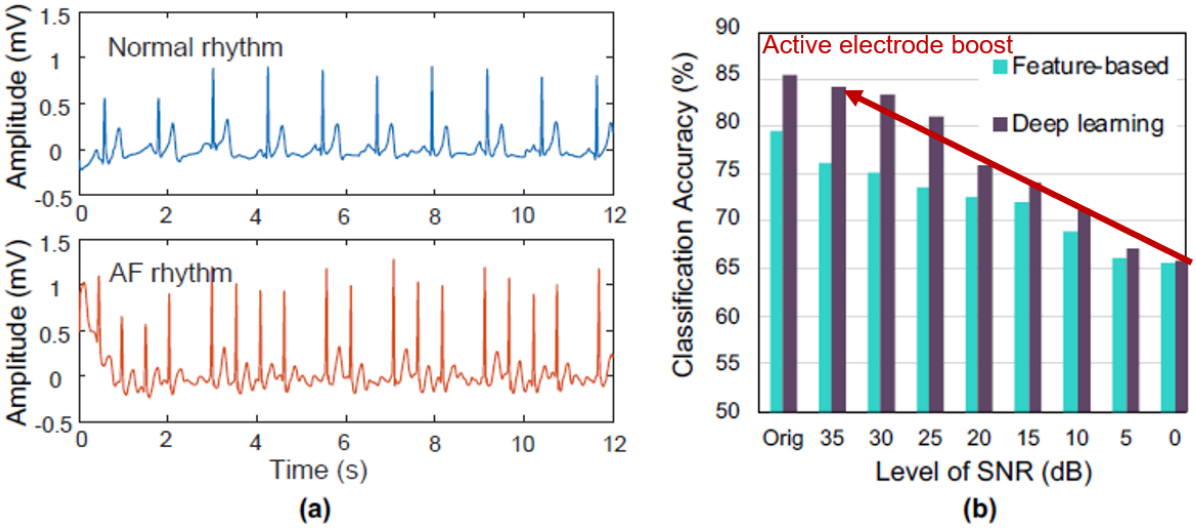


Figure 5.10: a. The comparison between normal and AF ECG recordings; b. classification accuracy improvement with increasing level of SNR on both of feature-based and deep learning-based approach.

be combined with advanced signal processing to further improve the system performance.

Evaluations under BW and EMG noises: Similarly, evaluation results of the *active electrode* under EMG and BW noises are summarized in Table 5.2, where the first row indicates the recording index and following rows correspond to the output SNR under different input noise level. Not surprisingly, the *active electrode* slightly suppresses the BW noise (mainly lies in $<$0.5 Hz) since the amplifier has a 3 dB corner $\sim$0.1 Hz as shown in Fig. 5.6c, which partially filters out the BW noise. For the EMG noise, the signal quality drops slightly ($\sim$ 3dB) since the widespread nature (over 0-500 Hz), which has a large overlap with the amplifier's high gain region. The slightly SNR drop is acceptable since the motion noise is the most significant noise source (Motion : EMG : BW $\approx$ $10:1:1$), as presented in Fig. 5.2b.

5.4.3 SNR vs. Classification Accuracy

To assess the impact of the front-end SSS interfacing on the system level accuracy of AF detection, we evaluated both feature-based and deep learning-based AF classifiers under various motion noise levels (SNR ranging from 0 dB to 35 dB) on publicly available PhysioNet data set, which contains 8,528 ECG recordings [107]. Five-fold cross-validation is applied to assess the two classifiers, and the classification accuracy is measured using the averaged true positive rates over normal and AF ECG recordings. The ResNet model is trained with error back-propagation using Adam optimizer and categorical cross-entropy as the loss function. During training, we reduce the learning rate by a factor of 10 until validation loss converges. The weights that achieve the best validation accuracy are selected for final evaluation. As shown in Fig. 5.10b, the accuracy of both the hand-crafted classifier and the deep neural network classifier increases as the SNR improves. Utilizing our front-end SSS design, we can boost the SNR from 0 dB to $>$35 dB, which in turn improves classification accuracy by $>$11% and $>$19% for the hand-crafted classifier and the deep-learning based classifier respectively. The ultra-thin SSS interface can alleviate signal attenuations and boost the signal quality under motion noises, which is critical to achieving high accuracy for AF classification.

5.5 Discussion and Future Work

One main challenge for the ultra-thin TFT circuits is that TFTs exhibit high 1/f noise, whose magnitude decreses as the freuency increses, shown in Fig. 5.11. From the measured 1/f noise over 0-100 kHz, we can see that the 1/f noise falls directly in the band of interest for ECG

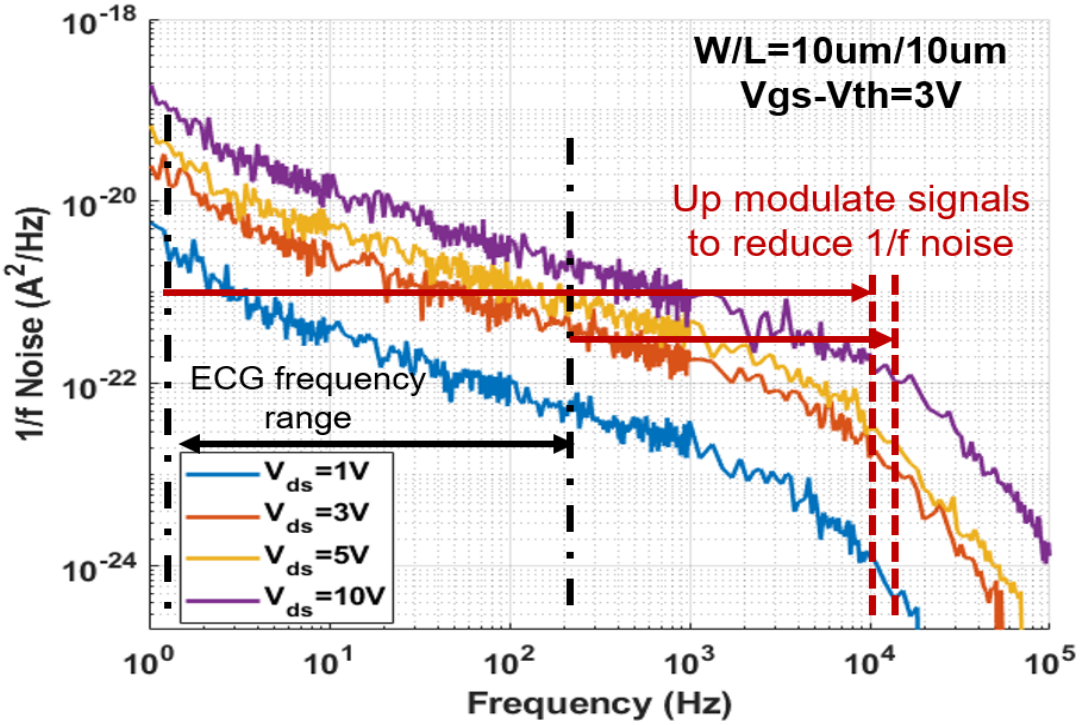


Figure 5.11: Measured 1/f Noise for a TFT transistor.

signals. The chopper stabilization technique can be used to effectively reduce the 1/f noise [111]. The key idea is using a carrier signal to up modulate the ECG signals to a relative high frequency range, where the 1/f noise is significantly lower ($\sim 10^4$X) than the low frequency range as illustrated in Fig. 5.11. Our fabricated CNT-TFT amplifier has already demonstrated an operation speed >20kHz, thus this technique can be readily applicable for reducing 1/f noise [111]. A single end topology is currently used for our prototyped amplifier; however, for better suppression of common mode noise, a differential topology should be considered. Other system aspects, such as hardware/software co-design and exploration of trade-offs between the silicon electronics and the skin electronics, could also be investigated.

5.6 Summary

In this part, we introduce an emerging paradigm for skin electronics, which shows great potential for high quality and long-term skin-sensor-silicon interfacing. Specifically, we propose an *active electrode* design and demonstrate a prototype of skin electronics based SSS interfacing. Besides measurement results, quantitative and systematic simulation results further confirm that the ultra-thin SSS interfacing can bring significant accuracy boosts for AF detection. In addition to the driving application (AF classification for ECG signals), the developed *active electrode* and simulation framework can be applied to other applications involving human-machine interfacing. Finally, promising future research directions are highlighted for further innovations on skin electronics.

Chapter 6

Robust Design of Large Area Flexible Sensing System

In this part, we will discuss the proposed encoder-decoder design, which combines FHE with compressed sensing to address the sensor defects issue in large area sensing applications.

6.1 Introduction

Large area flexible electronics, which brings ultra-thin form factor, mechanical flexibility, stretchability and conformable adhesion to the nonplanar surface [112, 5], has great potential for applications, such as structure health monitoring, wearable, bio-medical therapy, and electronic-skin [37, 113]. With recent advances in materials, device and integration, large area sensing for temperature, tactile and ultrasound has been demonstrated [7, 6]. Among various emerging flexible materials, carbon nanotube (CNT) shows great potentials for high-

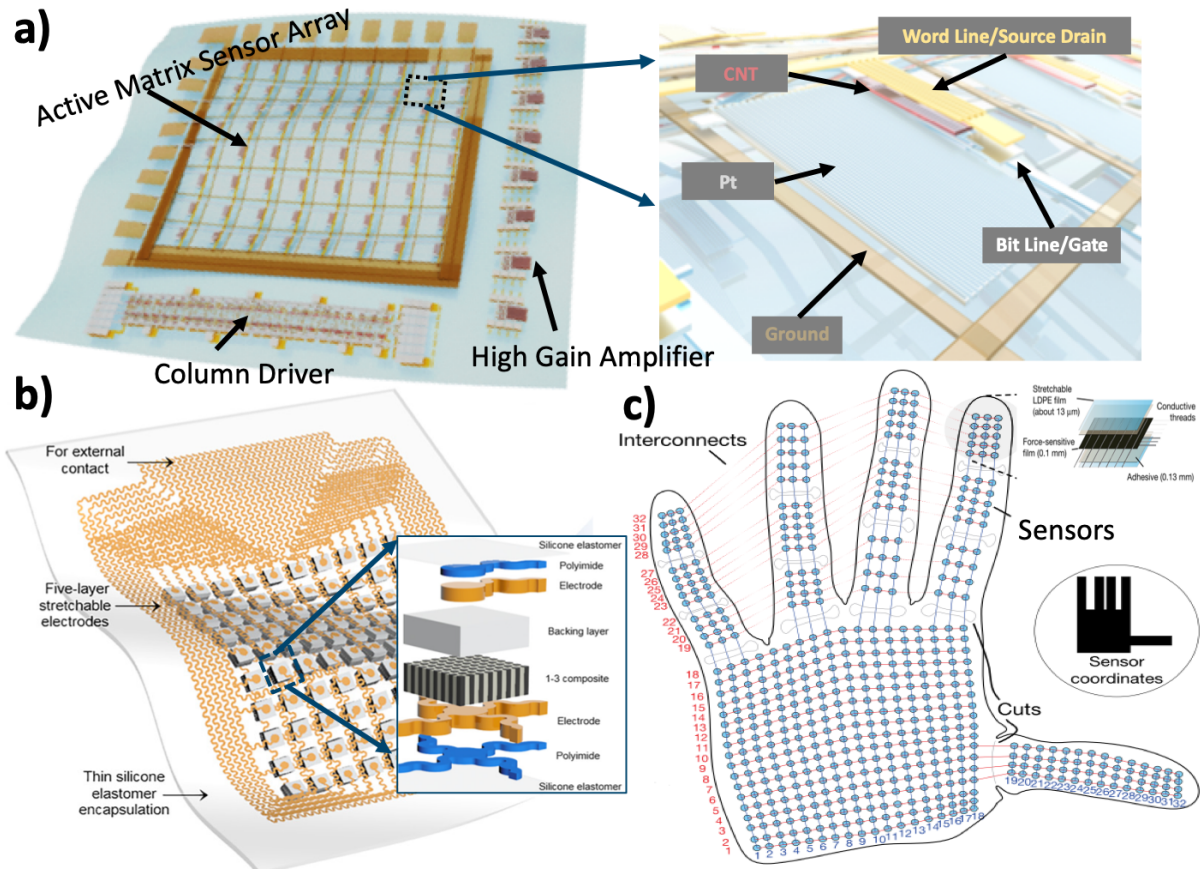


Figure 6.1: Examples of large area flexible sensing systems: a). Flexible temperature sensing array with column driver and amplifier on the flexible substrate; b). Ultrasonic transducer arrays for three-dimensional imaging [6]; c). Tactile glove for robotic object grasping [7]. Reproduced with permission. Copyright 2018, Science and Copyright 2019, Nature.

performance flexible electronics due to its high carrier mobility, mechanical flexibility, and low-cost manufacturing [20, 114, 115]. Fig. 6.1a) shows our design of a CNT-based temperature sensing array with column driver and amplifier on flexible substrates and Figs. 6.1b)-c) are recent published results for ultrasound and pressure sensing systems [6, 7].

Unlike conventional silicon electronics for which the manufacturing needs sophisticated billion-dollar foundry, flexible electronic circuits can be fabricated on thin and conformable substrates such as plastic films, with low-cost high-throughput manufacturing methods such as

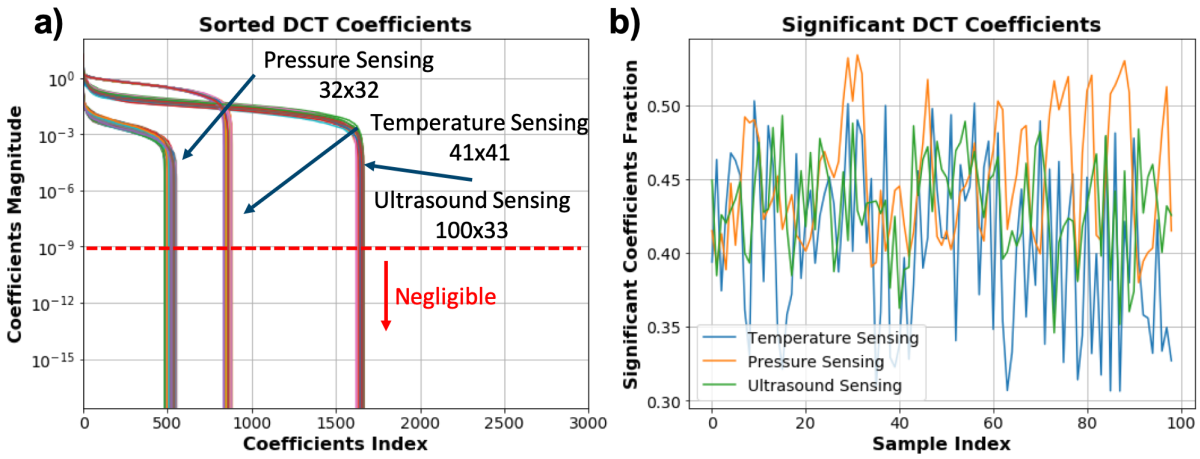


Figure 6.2: Statistical characteristics of temperature sensing, pressure sensing and ultra-sound sensing [8, 9, 7]. a). Sorted DCT coefficients of three sensing signals with different array size: 32x32, 41x41 and 100x33; b) Calculated significant DCT coefficients of 100 samples for three sensing signals. Here, significant coefficients are those coefficients $\geq \mathbf{1e^{-4}}$ max(coefficients).

ink-jet printing and roll-to-roll imprinting [3, 116]. The time-to-market as well as manufacturing cost can therefore be significantly reduced. However, the low-temperature requirement of the flexible substrate and the large-area nature of flexible sensors inevitably result in inadequate device yield, reliability and stability due to large device variation, device defects and transient errors, which pose great challenges for large area sensing applications [117, 118].

Previous studies addressing these challenges mainly focus on material- and device-level solutions to improve device reliability and stability [93, 94]. In this work, we propose solutions addressing system robustness for large area flexible sensing applications. We first investigated three public available datasets for typical human body sensing signals [7, 8, 9], covering temperature, pressure, and ultrasound. Applying discrete cosine transformation (DCT), these three natural body signals show similar sparse characteristics ($\sim 50\%$) in the frequency domain, as shown in Fig. 6.2, which implies the possibility of leveraging the sparsity to compensate for

device defects and transient errors. More details of the datasets can be found in Sec. 6.2. Based on this observation of inherent sparsity, we adopt the compressed sensing (CS) techniques to address system robustness for flexible large area sensing applications. The compressed sensing system consists of two parts: the encoder and the decoder. Since flexible electronics has limited operating speed and less reliability compared with silicon technology, it's desirable to implement the high complexity part in silicon and simplify the FE implementation as much as possible, as illustrated in Fig. 6.3. Fortunately, compressed sensing, unlike the conventional encoder-decoder schema, has a very simple universal encoder while a powerful decoder. Thus, through heterogeneous integration of flexible devices and silicon chips, we are able to implement the simple CS encoder using carbon-nanotube-based flexible electronics and process the sensor information in the high performance silicon chip. We have successfully designed and fabricated all key components of the flexible CS encoder: sensor array, column driver and amplifier to demonstrate the feasibility for a flexible encoder. In Sec. 6.3, we will provide implementation details for the compressed sensing encoder.

To quantify the improvement of system robustness achieved by the proposed sensing schema, we conducted two case studies: 2D temperature imaging and tactile sensor-based object recognition. The results show that the system can tolerate $\geq 20\%$ sparse errors (device defects or transient errors) while still being able to achieve very high level system robustness for practical applications. The main contributions of this work are summarized as follows:

- Propose a robust system solution for large area sensing applications through hardware/software co-design: specifically, implementing a CS encoder using CNT-based flexible electronics

and using powerful silicon chips for CS decoding.

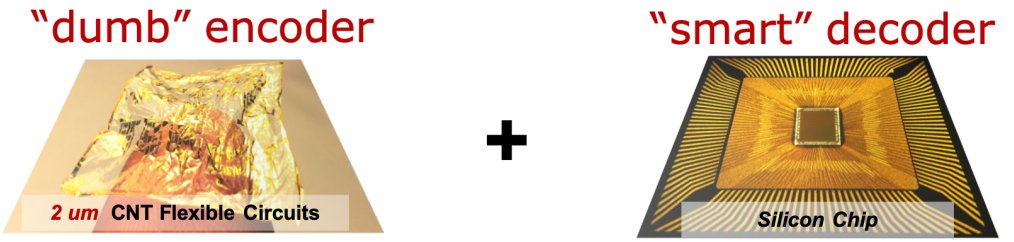
- Successfully designed and prototyped key components of the flexible CS encoder including a sensor array, a column driver and amplifiers, which demonstrates the feasibility of the proposed robust sensing design.

- Quantitatively evaluated how the proposed robust sensing schema can accommodate the sparse defects (device defects or transient errors). Under 10% sparse errors, it can reduce the RMSE from 0.20 to 0.05 for temperature sensing array and boost the classification accuracy by 19% (from 65% to 84%) for tactile-sensing based object recognition.

The rest of this work is organized as follows: Section 6.2 elaborates the statistical characteristics of sensed body signals. Section 6.3 introduces the compressed sensing and our prototyped building blocks for the encoder. Quantitative experimental results are described in Section 6.4. Section 6.5 draws the conclusion.

6.2 Statistics of Human Body Signals

As sensing of temperature, pressure, ultrasound sensing is essential functionality for emerging applications, such as e-skin, future robots and noninvasive structure monitoring, we analyzed three public datasets to characterize the signals in these datasets [8, 9, 7]. Many nature signals are sparse or compressible and can be expressed concisely in the proper basis [119]. For an illustration purpose, we simply applied the discrete cosine transform (DCT) to these datasets, while other suitable transformations, such as discrete Fourier transform and discrete wavelet



Flexible Electronics	Attributions	Si-Electronics
~2um	Thickness	~100um
+	Flexible	–
Low	Cost/Area	High
~um	Channel Length	~nm
Low	Performance	High
Large	Variation	Small

Figure 6.3: Compressed sensing schema: simple FE encoder and powerful silicon decoder [3].

transform, can be applied as well. As shown in Fig. 6.2a), the magnitude of the sorted DCT coefficients of all three type of sensed body signals decay rapidly. As summarized in Fig. 6.2b), all three types of sensed signals exhibit high sparsity ($\sim 50\%$) in the frequency domain after applying DCT. According to the compressed sensing theorem [119], the required measurements M can be estimated by:

$$M \approx K * log(N/K) \tag{6.1}$$

where K is the sparsity and N is the number of total sensors. From Fig. 6.2b), which indicates that, for typical human body signals, $K * log(N/K)$ ≈N/2, meaning only $N/2$ measurements are needed by utilizing compressed sensing for the large area sensing applications. In another

word, up to 50% sparse errors can potentially be compensated for and thus be tolerated. Of course, CS will inevitably introduce errors [119, 120]:

$$||x_{cs} - x^*||_2 \lesssim \overbrace{\sqrt{\frac{N}{M}}\epsilon}^{\text{measurement error}} + \overbrace{\frac{||x_{cs} - x_K||_{l1}}{\sqrt{K}}}^{\text{approximation error}} \tag{6.2}$$

where x_{cs} is reconstructed result, x^* is the original signal, x_K is the best K-term approximation of x^* and ϵ is the measurement noise. As shown in Eq. 6.2, the approximation error is determined by the sparsity (K) and the measurement error is determined by the measured portion (M/N) and measurements noise (ϵ). Although reconstruction errors are inevitable, we can still get significant RMSE reduction and classification accuracy boost under moderate sparse errors, which will be demonstrated in Sec. 6.4. In this study, we mainly focus on effects resulting from 0-20% sparse errors, which is the typical range of device defects/transient errors for FE reported in literature [118, 121, 122].

6.3 Flexible compressed sensing encoder

In this section, we first introduce the fundamentals of the compressed sensing and explain how to implement the CS encoder using CNT-based flexible circuitry. We will then give more details of the design and fabrication of our flexible circuitry.

6.3.1 Compressed Sensing Based on DCT

CS theory asserts that one can recover certain signals and images from far fewer samples or measurements than traditional methods need [119]. In the following, we mathematically formulate compressed sensing in sparse DCT representations.

Let $f(a, b)$ be a two-dimensional function of the performance of interest, where a and b represent the coordinate of a location within the two-dimensional plane. Here, $f(a, b)$ could be the pixel value of a temperature, pressure or ultrasound sensor array. For simplicity, we assume the coordinates a and b being integers $a \in$ [1,2,...,$\sqrt{N}$] and $b \in$ [1,2,...,$\sqrt{N}$] where N is the number of sensors in a square array. We can express the DCT transform in a matrix form [123]:

$$y = \Psi \cdot x \tag{6.3}$$

where $\{F(u, v); u, v \in [1, 2, ..., \sqrt{N}]\}$ is a set of DCT coefficients and Ψ is an NxN matrix,

and x and y are $Nx1$ vectors:

$$\Psi = \begin{bmatrix} \Psi_{1,1,1} & \Psi_{1,1,2} & \dots & \Psi_{1,\sqrt{N},\sqrt{N}} \\ \Psi_{2,1,1} & \Psi_{2,1,2} & \dots & \Psi_{2,\sqrt{N},\sqrt{N}} \\ \vdots & \vdots & \vdots & \vdots \\ \Psi_{N,1,1} & \Psi_{N,1,2} & \dots & \Psi_{N,\sqrt{N},\sqrt{N}} \end{bmatrix} \tag{6.4}$$

$$\Psi_{n,u,v} = \alpha_u \beta_v \cos(\frac{\pi(2x_n - 1)(u-1)}{2\sqrt{N}}) \cos(\frac{\pi(2y_n - 1)(v-1)}{2\sqrt{N}}) \tag{6.5}$$

$$x = [F(1,1) \dots F(\sqrt{N},\sqrt{N})]^T,\ y = [f(1,1) \dots f(a_{\sqrt{N}}, b_{\sqrt{N}})]^T \tag{6.6}$$

$$\alpha_u = \begin{cases} \sqrt{1/\sqrt{N}}\ (u=1) \\ \sqrt{2/\sqrt{N}}\ (2 \le u \le \sqrt{N}) \end{cases} \quad \beta_v = \begin{cases} \sqrt{1/\sqrt{N}}\ (v=1) \\ \sqrt{2/\sqrt{N}}\ (2 \le v \le \sqrt{N}) \end{cases} \tag{6.7}$$

In Eqs. (6.4)-(6.7), the DCT coefficients $F(u,v)$ are the problem unknowns. In other words, we need to determine $F(u,v)$ based on the measurement data $f(a,b)$. Once the DCT coefficients $F(u,v)$ are known, the function $f(a,b)$ can be easily calculated using IDCT [123]. Eq. (6.3) expresses the measurements y as a product of the new DCT basis Ψ and sparse coefficients x. According to the CS theorem [119], we can recover the N dimension sparse coefficients x with M measurements. To express this mathematically, we apply a sampling matrix Φ_M, which consists of M randomly sampled rows of the identify matrix. As a result, Eq. (6.3) becomes:

$$\underset{\text{Encoder: FE Side}}{\Phi_M \cdot y} = \underset{\text{Decoder: Silicon Side}}{\Phi_M \cdot \Psi \cdot x} \tag{6.8}$$

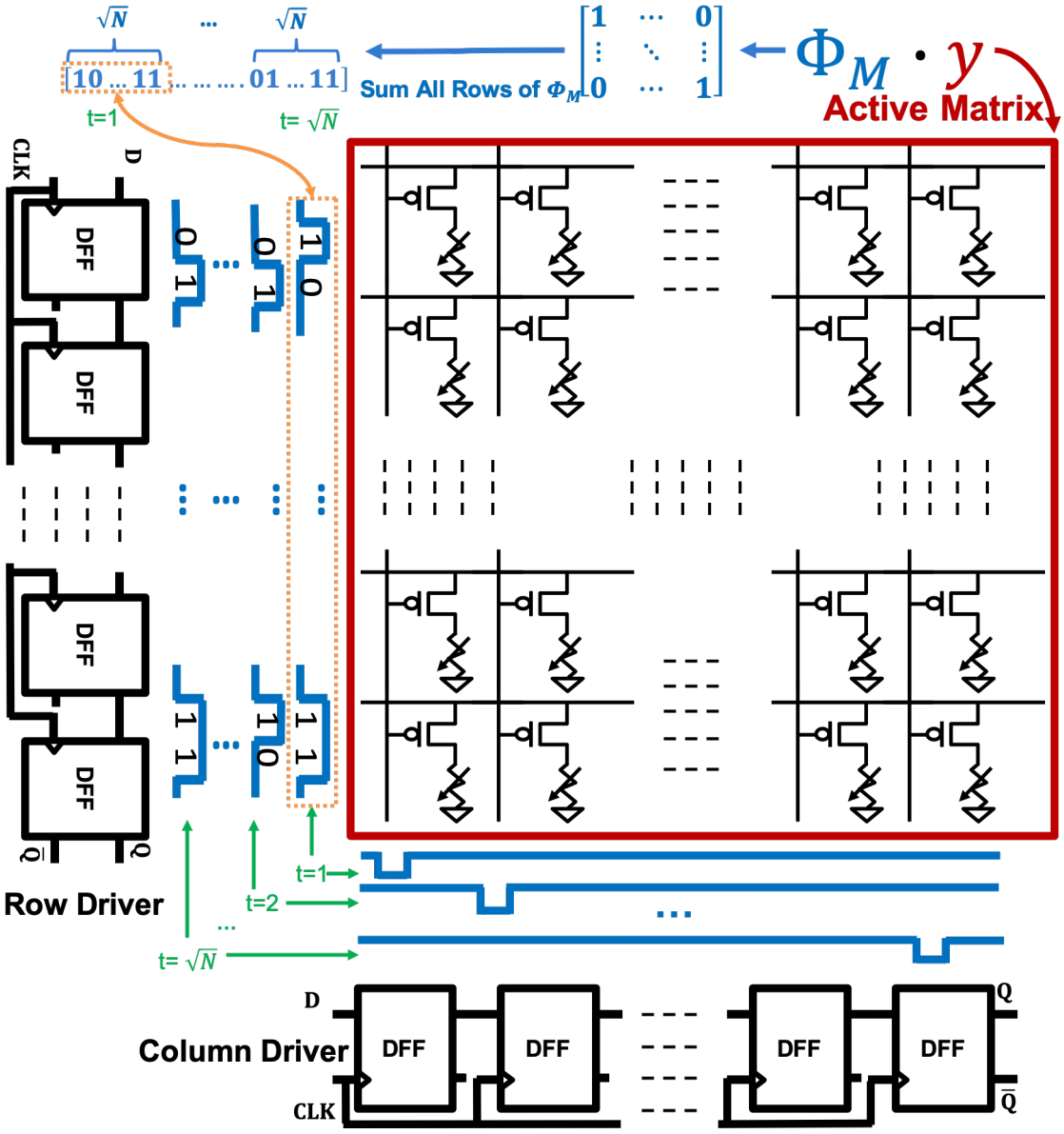


Figure 6.4: Circuit diagram for the implementation of the CS encoder. The sensor array $\mathbf{y}$ is implemented in an active matrix, where each pixel has a transistor to control the access. And, shift-registers are used for the column and row drivers to scan out sensor information based on the sensing matrix $\mathbf{\Phi}_\mathrm{M}$.

The left hand-side of Eq. (6.8) describes the encoding process: random sampling from the sensor array, which can be implemented effectively using an active matrix and shift-registers. As described in Fig. 6.4, the sensor array y is implemented in an active matrix and has control

of each pixel through row and column drivers with four interconnects: ground, row control, column control and readout. The active matrix design also provides good scalability as the array size grows in terms of interconnects, since the silicon chips have limited pins. Shift-registers are used for the column and row drivers to scan out sensor information based on the sensing matrix Φ_M. Since the Φ_M is randomly sampled rows of the identify matrix, each column has at most one '1'. After summing all rows, we have the $1xN$ vector, where it contains $\sqrt{N}$ blocks corresponding to control signals of each column of the active matrix as shown in Fig. 6.4. The silicon chip implementing the decoder will coordinate raw and column drivers to scan out sensor information based on Φ_M in $\sqrt{N}$ cycles as illustrated in Fig. 6.4. Note that we implemented the active matrix using CNT-based p-type transistors, thus the sensor array is low-enabled.

The right hand side of Eq. (6.8) describes the first part of the decoding process: representing the signal in a sparse basis. The remaining is a L_1-norm optimization:

$$\begin{aligned} &\underset{\text{x}}{\text{minimize}} \quad ||x||_1 \\ &\text{subject to:} \;\; \Phi_M \cdot y = \Phi_M \cdot \Psi \cdot x \end{aligned} \tag{6.9}$$

where $||x||_1$ denotes the L_1-norm of x and it will enforce the sparsity of the reconstructed x_{cs}. The L_1-norm problem can be solved through convex optimization or can be re-formulated as a linear programming problem and solved efficiently in the silicon side [124].

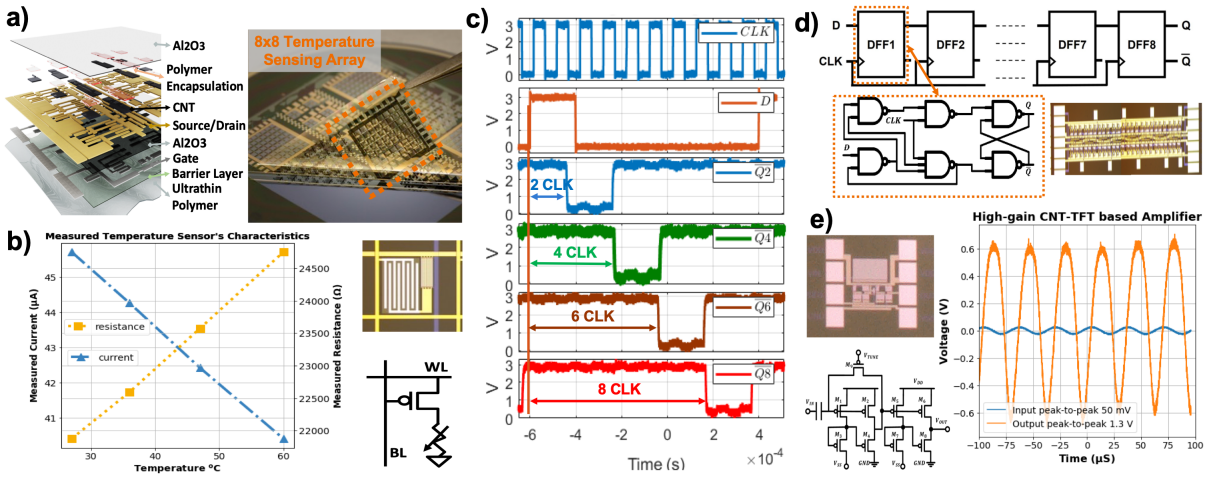


Figure 6.5: Building blocks of CNT-based flexible compressed sensing encoder. a) Device structure and die photo of the fabricated active matrix and peripheral circuits on a ultra-thin flexible substrate; b) Characteristics, die photo and schematic of a temperature sensor with $\mathbf{V_{WL} = 1\ V,\ V_{BL} = 0\ V}$; c)-d) Measured waveforms, schematic and die photo of a 8-stage shift-register with CLK running at 10 kHz and input data running at 1 kHz and VDD = 3 V; e) Die photo, schematic and measured waveforms of a self-biased high-gain amplifier with input = 50 mV, output = 1.3 V running at 30 kHz. L = 10 um, M1, M5, M9 = 50 um, Others = 150 um, C = 1 nF, Vtune = 1 V, VSS = -3 V and VDD = 3 V.

6.3.2 High-yield Carbon-nanotube Thin Film Transistors

To enable large scale CNT-based circuitry integrating with senors, scan drivers and amplifiers, we need high yield CNT TFTs and effective design methods to achieve the required complexity and robustness. One of the main obstacles is that the commonly grown CNTs contain both semiconducting (s-) and metallic (m-) types, where the m-CNT, deposited along with s-CNT in the channel region of a transistor, will bridge the source–drain electrodes resulting in the device failure. To achieve a purity of s-CNT >99.99%, we first use the polymer sorting method to separate s-CNT from m-CNT utilizing the aggregation behavior difference between s-CNT/polymer complex and m-CNT/polymer complex [125], then a second centrifugation is utilized to further remove the m-CNT after storing the polymer-sorted CNT in a fridge (4 ^oC)

for 24 hrs [115]. With this purification procedure, a ultra-high purity >99.997% of s-CNT and a high yield >99.9% of CNT TFTs can be achieved [115], which was validated thoroughly with wafer level fabrications and electrical measurements with >5000 CNT TFTs and 44 five-stage ring oscillators. As shown in Fig. 6.5a), CNT-based circuitry was fabricated on a ultra-thin flexible substrate, either a 10 um polyimide or a 1 um parylene, which is first deposited on a 4 inch carrier wafer. Electrodes, interconnects, barrier, CNT and encapsulation layers are deposited in the illustrated order. Another device-level challenge is the lack of air-stable n-type CNT TFTs leading to a low circuit yield of complementary CNT circuits [115, 125]. To address this challenge, we employ the pseudo-CMOS design style [28] which uses only mono-type TFTs, either n- type or p-type, while can achieve performance comparable to logic circuits based on complementary-type transistors [115, 35].

6.3.3 Design Methodology

In addition to the device-level challenges, the lack of industry standard SPICE model and support of design tools for CNT-TFT technology make the design of the CNT-based sensing system challenging. To address these challenges, a behavior model of CNT TFTs based on Verilog-A is developed [116], which was thoroughly validated with wafer level CNT-TFT devices and circuits. We first extracted all model parameters based on our CNT-TFT's measurement data, then simulation and optimization were performed for designing pseudo-CMOS digital cells, including inverters, NAND, and XOR logic gates, based on which 8-stage shift registers were successfully designed and implemented. Furthermore, pseudo-CMOS based self-biased ampli-

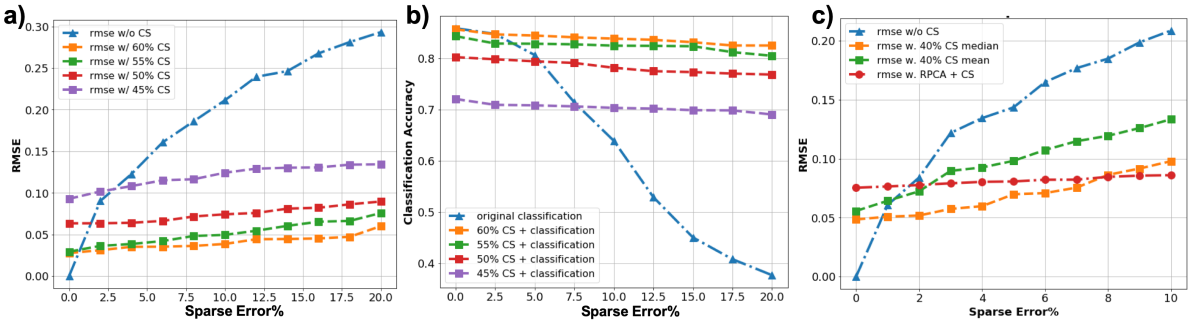


Figure 6.6: Compressed sensing enabled robustness for RMSE and classification accuracy. a) RMSE evaluation w/ or w/o compressed sensing under various sampling percentage; b) Classification accuracy w/ or w/o compressed sensing under various sampling percentage; c) RMSE evaluation of robust principle components analysis (RPCA) and mean/median from 10 rounds of resampling.

fiers were also designed and fabricated, which can boost sensor signals' quality via near sensor amplification. To maximize the manufacturing yield, we customized physical verification scripts to automatically perform the design rule checking (DRC) and layout versus schematic (LVS) based on fabrication processes of the CNT technology. Although the Verilog-A model and physical verification scripts are customized for CNT technology, the entire design flow is transferable and applicable for other flexible technologies.

6.3.4 Flexible Circuit Implementations

Fig. 6.5 shows the building blocks of the encoder design which was successfully fabricated and validated: a platinum (Pt) temperature sensor array, a shift-register and an amplifier. The die photo, schematic and typical sensor's characteristics are shown in Fig. 6.5b). To achieve a good linearity, we use a large CNT TFT (W/L = 500/25 μm) for each pixel which is biased in the linear region during the sensing process. The Pt sensor shows great linearity of the temper-

ature w.r.t. the sensed current, which allows us to map the current to temperature accurately. For touch, temperature, sweat and bio-medical sensing applications [126], the speed requirement ($\sim$kHz) is not critical while a low operation voltage ($<$5 V) is desirable due to safety considerations. To realize a fast shift-register (SR) at a low supply voltage, sufficient noise, and setup/hold time margins are required when operating at a fast clock rate. Figs. 6.5c)-d) show the schematic, die photo and measured waveforms of the 8-stage shift-register based on the pseudo-CMOS design style, which consists of 304 CNT TFTs. The SR functions properly with a clock rate of 10 kHz and a data rate of 1 kHz at a supply voltage of 3 V. To improve the signal quality and sensitivity of the sensing system, a high-gain self-biased amplifier is also prototyped which amplifies the sensor signal right at the output of the flexible sensor array, as shown in Fig. 6.5e), where a 28 dB gain has been achieved at 30 kHz. The self-biased amplifier is composed of two stages. The first stage is based on a pseudo-CMOS inverter (M1-M4) with a feedback CNT transistor (M9) biased in the linear region, as well as an input capacitor to block the DC current flowing from the the input terminal V_{IN}. The feedback CNT transistor biases the pseudo-CMOS inverter in the high-gain region around half-VDD, and also provides a resistive feedback path. The second stage (M5-M8) works as a common-source amplifier serving as a buffer to V_{OUT} with a fixed voltage gain.

It is the joint effort of high-yield CNT TFTs, robust pseudo-CMOS design and customized CAD tools that enables us to successfully design and fabricate the low-voltage high performance SR and high-gain amplifier, which serve as the foundation of the CS encoder. Unlike silicon circuits, most flexible TFT circuits contain ¡50 TFTs or operate at ¡10 kHz due to the

low device yield and the limited temperature tolerance of the ultra-thin substrate [125, 115]. Thus, in comparison with the state-of-the-art flexible circuits [115], our fabricated SR and amplifier are highly competitive in terms of both the speed and complexity. Please note that ∼GHz performance has been reported for CNT based nanometer devices using high temperature silicon process on a rigid substrate, which is completely different from CNT-TFT devices fabricated on a flexible substrate.

In summary, we formulate the large area sensing problem as a compressed sensing problem based on DCT and our implementation consists of two parts: an encoder and a decoder. We have successfully implemented the encoder in CNT-based flexible electronics achieving desirable performance.

6.4 Experiments setup and simulation results

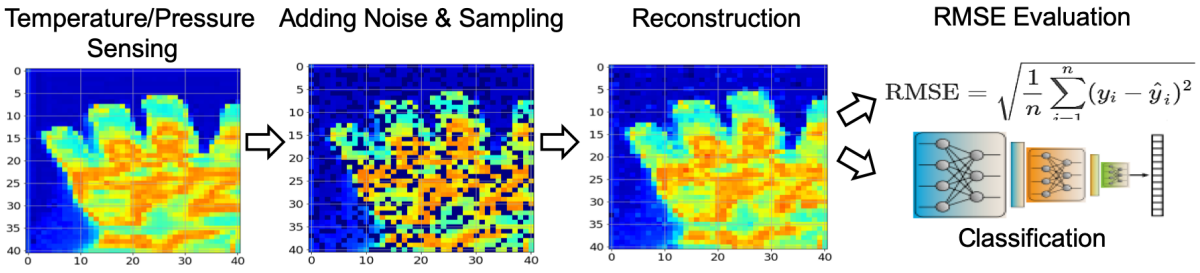


Figure 6.7: Experiments setup: Instead of directly using the noisy inputs, we perform the sampling and reconstruction before the RMSE evaluation and classification.

To evaluate the benefits of the proposed CS-based approach, we consider two metrics: 1) communication cost saving assuming no sparse error; 2) robustness boost in the presence of sparse errors in the sensor array.

6.4.1 Communication Cost Reduction

Under the assumption that all measurements contain no sparse errors (i.e. there is no device defects/transient errors), we can reconstruct the entire array's results with only, M, sensors' results by solving the L_1-norm optimization in Eq. (6.9). Based on the scheme shown in Fig. 6.4, we are able to scan all necessary M sensors' results in $\sqrt{n}$ cycles. Assuming that the silicon chip implementing the decoder has sample and hold circuitry followed by an Analog-to-Digital-Converter (ADC), storage and reconstruction of the results for the entire sensor array can be done in a straightforward manner. Thus, we can roughly reduce the communication cost to M/N ($\sim$0.5) of the original cost, since the A/D conversion usually is the bottle neck of sensing applications.

6.4.2 Improvement to System Robustness

This study evaluates system robustness in presence of device defects and transient errors in our measurement. For example, we have observed device defects/transient errors in the temperature sensor array, which usually show extreme results either very high or almost zero currents. Therefore, after testing to identify those defects, we can dramatically simplify the CS process by only sampling good pixels for reconstruction. Let's start with this simple case followed by discussion of more complicated scenarios.

To quantify the robustness, we choose two applications for evaluations each of which uses its corresponding metric for performance evaluation: root-mean-square-error (RMSE) for temperature array sensing and classification accuracy for tactile-sensor based object recognition.

Experimental setup and results for temperature array sensing: We use the temperature sensing dataset to conduct the experiments [8]. As shown the in Fig. 6.7 a), the experiment contains three steps: we first normalize the value of the dataset to the range of [0,1], then randomly choose a certain percentage of pixels to inject noises. We set those selected pixels to 0/1 to emulate the extreme values as observed in real measurements. Then, we exclude all 0/1s and perform random sampling. Based on sampled data, we reconstruct the data and evaluate the RMSE with respect to the origin data. The quantitative results are summarized in Fig. 6.6a), where we explored different sampling percentage with sparse errors varying from 0% to 20%. As sampling percentage increases from 45% to 60%, the RMSE decreases as expected and the RMSE is bounded by the measurements error as described by Eq. (6.2), which explains the slowdown of RMSE reduction as the sampling percentage increases. We also notice that as the sparse error goes up to 20%, the RMSE only increases slightly, which indicates the robustness benefited from the CS methods.

Experimental setup and results for tactile-sensor based object recognition: The tactile sensing dataset of 26 different objects is used for evaluating the accuracy for object classification [7]. We follow the same experiment steps as the temperature sensing experiment except the last step. Instead of directly calculating the RMSE, we evaluate the accuracy of the machine learning classifier. We used ResNet for identifying objects from the tactile data (32x32 arrays) [110], where 'Max pooling' and 'Dropout' are used for reducing dimensionality of the data and avoiding overfitting to the training data respectively. The ResNet model is trained with error backpropagation using Adam optimizer and categorical cross-entropy as the loss function.

During training, we reduce the learning rate by a factor of 10 until validation loss converges. The weights that achieve the best validation accuracy are selected for the final evaluation. The classification results are shown in Fig. 6.6b). Without CS, the classification accuracy drops dramatically as the sparse error increases. After applying CS, we can get a significant accuracy boost ($\sim$20%) under moderate spare errors ($\sim$10%). Also, the accuracy boost follows the same pattern as the RMSE, where accuracy improvement slows down as the sampling percentage reaches a relatively high level (60%).

6.4.3 Discussion for Sampling Strategy

In the previous subsection, we assume that the sparse errors can be detected through testing and thus can be eliminated from the sampling procedure, which might not be a valid assumption for certain application scenarios. Thus, in this section, we discuss some advanced sampling strategies, with which the proposed robust sensing scheme can be applied to broader application scenarios.

Resampling: We can perform multiple resampling and reconstructions, then the median value, as more robust to outliers, of each pixel from multiple reconstructions is used as the final result. Notice that the re-sampling and the reconstructions are executed in the silicon side after acquiring and storing the signals from the sensor array. As shown in Fig. 6.6c), we achieve a reasonably good ($\sim$50%) RMSE reduction with ten rounds of resampling and a moderate percentage (3-10%) of sparse errors.

Outlier Detection: We can also first detect and exclude outliers via robust principle com-

ponents analysis (RPCA) [127], then perform the random sampling and the reconstruction. From Fig. 6.6c), we notice that the RPCA method outperforms the resamping method under a relative high percentage ($>8\%$) of spare errors.

6.5 Summary

In this part, we introduce the use of CS to improve the system robustness for large area sensing applications, demonstrate the implementation and evaluate its benefits. Specifically, we first identify the sparse statistical characteristics of various sensing signals, then propose a robust sensing scheme based on a CS encoder implemented in FE right next to the sensor array and a much more complex decoder implemented in a silicon chip. Moreover, circuit measurements of our CNT-based implementation of the encoder confirm the feasisbility of the proposed FE encoder design. Simulation results further demonstrate that the robust sensing scheme can achieve significant RMSE reduction and classification accuracy boosts for temperature imaging and object identification respectively. In addition to temperature, pressure and ultra-sound sensing discussed in the work, the developed robust sensing method has broader applications for large area sensor array.

Chapter 7

Conclusions and Future Directions

This thesis is dedicated to the design and design automation of the high-fidelity flexible hybrid electronics. The key contributions and findings are as follows.

From the design automation aspect, we have developed the compact models for key flexible components , including flexible TFTs, capacitor, resistors. Also, the FHE-PDK has also been demonstrated with DRC, LVS and PEX to close the existing gaps of FHE system design flow.

From the circuit design aspect, using CNT devices, we have built the Pseudo-CMOS cell library to address the mono-type circuit design challenges and facilitate the large scale robust flexible circuit design. With the developed cell library and FHE-PDK, we successfully demonstrated CNT-based high-speed and large scale flexible circuits, which push the boundary of the state-of-the-art results regarding both the speed and complexity.

From the system robustness aspect, we proposed the ”active electrode” to alleviate the motions noises for wearable applications. Through the integration of flexible amplifier and

electrode, we can pre-amplifier the critical signals before sending them to interconnects and flex-rigid interfaces, where signals are easily contaminated by surrounding noise. System simulations show that the proposed "active electrode" can boost the SNR up to 30 dB.

Also, from the device yields and reliability aspect, we combined the encoder-decoder design with compressed sensing to alleviate sensor defects in large area sensing applications. Motivated by the sparsity of body-sensing signals and compressed sensing, we partitioned the FHE system into the flexible encoder and silicon decoder, which can push the complexity to the silicon meanwhile taking advantages of flexible sensing functionalities. Systematic analysis show that the encode-decoder design can compensate up to 20% sensor defects.

Although, numerous advances have been made from materials, devices, integration, design and design automation, innovations at the circuit-, architecture-, and system-levels are desirable in order to tackle large device variations, device defects and multi-physics considerations. Some potential future directions are listed as below:

- Noise modeling for flexible devices and sensors, such as TFTs, capacitors, resistors, various sensors and interconnects.

- Variation-aware system-level and architectural study of FHE system based developed compact models and process variations.

- Multi-physics modeling for bending, stretching and twisting impacts on electrical behaviors of the FHE system.

- More system-level and architectural study on improving the signal fidelity for critical

flex-rigid interfacing.

Bibliography

[1] Ting Lei, Lei-Lai Shao, Yu-Qing Zheng, Gregory Pitner, Guanhua Fang, Chenxin Zhu, Sicheng Li, Ray Beausoleil, H-S Philip Wong, Tsung-Ching Huang, et al. Low-voltage high-performance flexible digital and analog circuits based on ultrahigh-purity semiconducting carbon nanotubes. *Nature communications*, 10(1):1–10, 2019.

[2] Tsung-Ching Huang, Leilai Shao, Ting Lei, Raymond Beausoleil, Zhenan Bao, and Kwang-Ting Cheng. Robust design and design automation for flexible hybrid electronics. In *Circuits and Systems (ISCAS), 2017 IEEE International Symposium on*, pages 1–4. IEEE, 2017.

[3] Tsung-Ching Huang, Leilai Shao, Ting Lei, Raymond Beausoleil, Zhenan Bao, and Kwang-Ting Cheng. Robust design and design automation for flexible hybrid electronics. In *Circuits and Systems (ISCAS), 2017 IEEE International Symposium on*, pages 1–4. IEEE, 2017.

[4] Jae Woong Jeong, Woon Hong Yeo, Aadeel Akhtar, James J.S. Norton, Young Jin Kwack, Shuo Li, Sung Young Jung, Yewang Su, Woosik Lee, Jing Xia, Huanyu Cheng, Yonggang Huang, Woon Seop Choi, Timothy Bretl, and John A. Rogers. Materials and optimized designs for human-machine interfaces via epidermal electronics. *Advanced Materials*, 25(47):6839–6846, 2013.

[5] Jae Woong Jeong, Min Ku Kim, Huanyu Cheng, Woon Hong Yeo, Xian Huang, Yuhao Liu, Yihui Zhang, Yonggang Huang, and John A. Rogers. Capacitive epidermal electronics for electrically safe, long-term electrophysiological measurements. *Advanced Healthcare Materials*, 3(5):642–648, 2014.

[6] Hongjie Hu, Xuan Zhu, Chonghe Wang, Lin Zhang, Xiaoshi Li, Seunghyun Lee, Zhenlong Huang, Ruimin Chen, Zeyu Chen, Chunfeng Wang, et al. Stretchable ultrasonic transducer arrays for three-dimensional imaging on complex surfaces. *Science advances*, 4(3):eaar3979, 2018.

[7] Subramanian Sundaram, Petr Kellnhofer, Yunzhu Li, Jun-Yan Zhu, Antonio Torralba, and Wojciech Matusik. Learning the signatures of the human grasp using a scalable tactile glove. *Nature*, 569(7758):698, 2019.

[8] Xavier Font-Aragones, Marcos Faundez-Zanuy, and Jiri Mekyska. Thermal hand image segmentation for biometric recognition. *IEEE Aerospace and Electronic Systems Magazine*, 28(6):4–14, 2013.

[9] Michał Byra andAndrzej Nowicki Hanna Piotrzkowska-Wróblewska, Katarzyna Dobruch-Sobczak. Open access database of raw ultrasonic signals acquired from malignant and benign breast lesions.

[10] Takao Someya, Zhenan Bao, and George G Malliaras. The rise of plastic bioelectronics. *Nature*, 540(7633):379–385, 2016.

[11] Farhan Rasheed, Michael Hefenbrock, Rajendra Bishnoi, Michael BeigI, Jasmin Aghassi-Hagmann, and Mehdi B Tahoori. Predictive modeling and design automation of inorganic printed electronics. In *2019 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 30–35. IEEE, 2019.

[12] Leilai Shao, Tsung-Ching Huang, Ting Lei, Zhenan Bao, Raymond Beausoleil, and Kwang-Ting Cheng. Process design kit for flexible hybrid electronics. In *2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC)*, pages 651–657. IEEE, 2018.

[13] Leilai Shao, Sicheng Li, Ting Lei, Tsung-Ching Huang, Raymond Beausoleil, Zhenan Bao, and Kwang-Ting Cheng. Ultra-thin skin electronics for high quality and continuous skin-sensor-silicon interfacing. In *Proceedings of the 56th Annual Design Automation Conference 2019*, pages 1–6, 2019.

[14] Tsung-Ching Huang, Kenjiro Fukuda, Chun-Ming Lo, Yung-Hui Yeh, Tsuyoshi Sekitani, Takao Someya, and Kwang-Ting Cheng. Pseudo-cmos: A design style for low-cost and robust flexible electronics. *IEEE Transactions on Electron Devices*, 58(1):141–150, 2010.

[15] Chester Liu, En-Hua Ma, Wen-En Wei, James Li, I-Chun Cheng, and Yung-Hui Yeh. Placement optimization of flexible tft digital circuits. *IEEE Design & Test of Computers*, 28(6):24–31, 2011.

[16] H Gleskova, S Wagner, W Soboyejo, and Z Suo. Electrical response of amorphous silicon thin-film transistors under mechanical strain. *Journal of Applied Physics*, 92(10):6224–6229, 2002.

[17] Jiun-Li Lin, Po-Hsun Wu, and Tsung-Yi Ho. A novel cell placement algorithm for flexible tft circuit with mechanical strain and temperature consideration. In *2013 18th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pages 491–496. IEEE, 2013.

[18] Sridhar Sivapurapu, Rui Chen, Chirag Mehta, Yi Zhou, Mohamed LF Bellaredj, Xiaotong Jia, Paul A Kohl, Tsung-Ching Huang, Suresh K Sitaraman, and Madhavan Swaminathan. Multi-physics modeling and characterization of components on flexible substrates. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 9(9):1730–1740, 2019.

[19] Eiichi Sano and Tomo Tanaka. A simple drain current model for single-walled carbon nanotube network thin-film transistors. *Journal of Applied Physics*, 115(15):154507, 2014.

[20] Ting Lei, Xiyuan Chen, Gregory Pitner, H-S Philip Wong, and Zhenan Bao. Removable and recyclable conjugated polymers for highly selective and high-yield dispersion and release of low-cost carbon nanotubes. *Journal of the American Chemical Society*, 138(3):802–805, 2016.

[21] Ting Lei, Gregory Pitner, Xiyuan Chen, Guosong Hong, Steve Park, Pascal Hayoz, Ralf Thomas Weitz, Hon-Sum Philip Wong, and Zhenan Bao. Dispersion of high-purity semiconducting arc-discharged carbon nanotubes using backbone engineered diketopyrrolopyrrole (dpp)-based polymers. *Advanced Electronic Materials*, 2(1), 2016.

[22] Ali Javey, Qian Wang, Ant Ural, Yiming Li, and Hongjie Dai. Carbon nanotube transistor arrays for multistage complementary logic and ring oscillators. *Nano Letters*, 2(9):929–932, 2002.

[23] Mingjing Ha, Jung-Woo T Seo, Pradyumna L Prabhumirashi, Wei Zhang, Michael L Geier, Michael J Renn, Chris H Kim, Mark C Hersam, and C Daniel Frisbie. Aerosol jet printed, low voltage, electrolyte gated carbon nanotube ring oscillators with sub-5 μs stage delays. *Nano letters*, 13(3):954–960, 2013.

[24] Mingjing Ha, Yu Xia, Alexander A Green, Wei Zhang, Mike J Renn, Chris H Kim, Mark C Hersam, and C Daniel Frisbie. Printed, sub-3v digital circuits on plastic from aqueous carbon nanotube inks. *ACS nano*, 4(8):4388–4395, 2010.

[25] Ying Diao, Leo Shaw, Zhenan Bao, and Stefan CB Mannsfeld. Morphology control strategies for solution-processed organic semiconductor thin films. *Energy & Environmental Science*, 7(7):2145–2159, 2014.

[26] Kazuhiro Yanagi, Hiroki Udoguchi, Satoshi Sagitani, Yugo Oshima, Taishi Takenobu, Hiromichi Kataura, Takao Ishida, Kazuyuki Matsuda, and Yutaka Maniwa. Transport mechanisms in metallic and semiconducting single-wall carbon nanotube networks. *Acs Nano*, 4(7):4027–4032, 2010.

[27] S Kumar, JY Murthy, and MA Alam. Percolating conduction in finite nanotube networks. *Physical review letters*, 95(6):066802, 2005.

[28] Tsung-Ching Huang, Kenjiro Fukuda, Chun-Ming Lo, Yung-Hui Yeh, Tsuyoshi Sekitani, Takao Someya, and Kwang-Ting Cheng. Pseudo-cmos: A novel design style for flexible electronics. In *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2010*, pages 154–159. IEEE, 2010.

[29] Tsung-Ching Huang, Kenjiro Fukuda, Takao Someya, and Kwang-Ting Cheng. Pseudo-cmos: A design style for low-cost and robust flexible electronics. *IEEE Transactions on Electron Devices*, 58(1):141–150, 2011.

[30] Huiliang Wang, Peng Wei, Yaoxuan Li, Jeff Han, Hye Ryoung Lee, Benjamin D Naab, Nan Liu, Chenggong Wang, Eric Adijanto, Benjamin C-K Tee, et al. Tuning the threshold voltage of carbon nanotube transistors by n-type molecular doping for robust and flexible complementary circuits. *Proceedings of the National Academy of Sciences*, 111(13):4776–4781, 2014.

[31] Ognian Marinov, M Jamal Deen, Ute Zschieschang, and Hagen Klauk. Organic thin-film transistors: Part i—compact dc modeling. *IEEE Transactions on Electron Devices*, 56(12):2952–2961, 2009.

[32] Yannis Tsividis and Colin McAndrew. *Operation and Modeling of the MOS Transistor*. Oxford Univ. Press, 2011.

[33] Koichi Ishida, Tsung-Ching Huang, Kentaro Honda, Yasuhiro Shinozuka, Hiroshi Fuketa, Tomoyuki Yokota, Ute Zschieschang, Hagen Klauk, Gregory Tortissier, Tsuyoshi Sekitani, et al. Insole pedometer with piezoelectric energy harvester and 2 v organic circuits. *IEEE Journal of Solid-State Circuits*, 48(1):255–264, 2013.

[34] Kris Myny and Soeren Steudel. 16.6 flexible thin-film nfc transponder chip exhibiting data rates compatible to iso nfc standards using self-aligned metal-oxide tfts. In *Solid-State Circuits Conference (ISSCC), 2016 IEEE International*, pages 298–299. IEEE, 2016.

[35] Kris Myny, Yi-Cheng Lai, Nikolaos Papadopoulos, Florian De Roose, Marc Ameys, Myriam Willegems, Steve Smout, Soeren Steudel, Wim Dehaene, and Jan Genoe. 15.2 a flexible iso14443-a compliant 7.5 mw 128b metal-oxide nfc barcode tag with direct clock division circuit from 13.56 mhz carrier. In *Solid-State Circuits Conference (ISSCC), 2017 IEEE International*, pages 258–259. IEEE, 2017.

[36] Jan M Rabaey, Anantha P Chandrakasan, and Borivoje Nikolic. *Digital integrated circuits*, volume 2. Prentice hall Englewood Cliffs, 2002.

[37] Chuan Wang, David Hwang, Zhibin Yu, Kuniharu Takei, Junwoo Park, Teresa Chen, Biwu Ma, and Ali Javey. User-interactive electronic skin for instantaneous pressure visualization. *Nature materials*, 12(10):899–904, 2013.

[38] Luckshitha Suriyasena Liyanage, Hangwoo Lee, Nishant Patil, Steve Park, Subhasish Mitra, Zhenan Bao, and Hon-Sum Philip Wong. Wafer-scale fabrication and characterization of thin-film transistors with polythiophene-sorted semiconducting carbon nanotube networks. *ACS nano*, 6(1):451–458, 2011.

[39] Jia Gao and Yueh-Lin Lynn Loo. Temperature-dependent electrical transport in polymer-sorted semiconducting carbon nanotube networks. *Advanced Functional Materials*, 25(1):105–110, 2015.

[40] Jiaqing Zhao, Pengfei Yu, Shi Qiu, Qinghang Zhao, Linrun Feng, Simon Ogier, Wei Tang, Jiali Fan, Wenjiang Liu, Yongpan Liu, et al. Universal compact model for thin-film transistors and circuit simulation for low-cost flexible large area electronics. *IEEE Transactions on Electron Devices*, 2017.

[41] Michael H Arnold. Corner-based geometric layout rule checking for vlsi circuits. Technical report, California Univ Berkeley Dept of Electrical Engineering and Computer Science, 1985.

[42] Ulrich Lauther. An o (n log n) algorithm for boolean mask operations. In *Proceedings of the 18th Design Automation Conference*, pages 555–562. IEEE Press, 1981.

[43] Thomas G Szymanski and Christopher J Van Wyk. Goalie: A space efficient system for vlsi artwork analysis. *IEEE Design & Test of Computers*, 2(3):64–72, 1985.

[44] K-W Chiang, Surendra Nahar, and C-Y Lo. Time-efficient vlsi artwork analysis algorithms in goalie2. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 8(6):640–648, 1989.

[45] Carl Ebeling, Neil McKenzie, and Larry McMurchie. The gemini users guide. Technical report, Tech. Report, Department of Computer Science and Engineering, University of Washington, 1994.

[46] Miles Ohlrich, Carl Ebeling, Eka Ginting, and Lisa Sather. Subgemini: identifying subcircuits using a fast subgraph isomorphism algorithm. In *Proceedings of the 30th international Design Automation Conference*, pages 31–37. ACM, 1993.

[47] Carl Ebeling and Ofer Zajicek. Validating vlsi circuit layout by wirelist comparison. In *Proceedings of the International Conference on Computer-Aided Design*, pages 172–173, 1983.

[48] Dae-Hyeong Kim, Nanshu Lu, Rui Ma, Yun-Soung Kim, Rak-Hwan Kim, Shuodao Wang, Jian Wu, Sang Min Won, Hu Tao, Ahmad Islam, et al. Epidermal electronics. *science*, 333(6044):838–843, 2011.

[49] Takao Someya, Zhenan Bao, and George G Malliaras. The rise of plastic bioelectronics. *Nature*, 540(7633):379–385, 2016.

[50] Alex Chortos, Jia Liu, and Zhenan Bao. Pursuing prosthetic electronic skin. *Nature materials*, 15(9):937–950, 2016.

[51] Daniela Rus and Michael T Tolley. Design, fabrication and control of soft robots. *Nature*, 521(7553):467–475, 2015.

[52] Qing Cao, Hoon-sik Kim, Ninad Pimparkar, Jaydeep P Kulkarni, Congjun Wang, Moonsub Shim, Kaushik Roy, Muhammad A Alam, and John A Rogers. Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates. *Nature*, 454(7203):495–500, 2008.

[53] Chenxin Zhu, Alex Chortos, Yue Wang, Raphael Pfattner, Ting Lei, Allison Claire Hinckley, Igor Pochorovski, Xuzhou Yan, John W-F To, Jin Young Oh, et al. Stretchable temperature-sensing circuits with strain suppression based on carbon nanotube transistors. *Nature Electronics*, 1(3):183–190, 2018.

[54] Jianshi Tang, Qing Cao, George Tulevski, Keith A Jenkins, Luca Nela, Damon B Farmer, and Shu-Jen Han. Flexible cmos integrated circuits based on carbon nanotubes with sub-10 ns stage delays. *Nature Electronics*, 1(3):191–196, 2018.

[55] Daisuke Kiriya, Kevin Chen, Hiroki Ota, Yongjing Lin, Peida Zhao, Zhibin Yu, Tae-jun Ha, and Ali Javey. Design of surfactant–substrate interactions for roll-to-roll assembly of carbon nanotubes for thin-film transistors. *Journal of the American Chemical Society*, 136(31):11188–11194, 2014.

[56] Shu-Jen Han, Jianshi Tang, Bharat Kumar, Abram Falk, Damon Farmer, George Tulevski, Keith Jenkins, Ali Afzali, Satoshi Oida, John Ott, et al. High-speed logic integrated circuits with solution-processed self-assembled carbon nanotubes. *Nature nanotechnology*, 12(9):861–865, 2017.

[57] Haitian Chen, Yu Cao, Jialu Zhang, and Chongwu Zhou. Large-scale complementary macroelectronics using hybrid integration of carbon nanotubes and igzo thin-film transistors. *Nature communications*, 5(1):1–12, 2014.

[58] Chuan Wang, David Hwang, Zhibin Yu, Kuniharu Takei, Junwoo Park, Teresa Chen, Biwu Ma, and Ali Javey. User-interactive electronic skin for instantaneous pressure visualization. *Nature materials*, 12(10):899–904, 2013.

[59] Ja Hoon Koo, Seongjin Jeong, Hyung Joon Shim, Donghee Son, Jaemin Kim, Dong Chan Kim, Suji Choi, Jong-In Hong, and Dae-Hyeong Kim. Wearable electrocardiogram monitor using carbon nanotube electronics and color-tunable organic light-emitting diodes. *ACS nano*, 11(10):10032–10041, 2017.

[60] Luisa Petti, Florin Loghin, Giuseppe Cantarella, Christian Vogt, Niko Münzenrieder, Alaa Abdellah, Markus Becherer, Tobias Haeberle, Alwin Daus, Giovanni Salvatore, et al. Gain-tunable complementary common-source amplifier based on a flexible hybrid thin-film transistor technology. *IEEE Electron Device Letters*, 38(11):1536–1539, 2017.

[61] Yasser Khan, Mohit Garg, Qiong Gui, Mark Schadt, Abhinav Gaikwad, Donggeon Han, Natasha AD Yamamoto, Paul Hart, Robert Welte, William Wilson, et al. Flexible hybrid electronics: Direct interfacing of soft and hard electronics for wearable health monitoring. *Advanced Functional Materials*, 26(47):8764–8775, 2016.

[62] Li Xiang, Heng Zhang, Guodong Dong, Donglai Zhong, Jie Han, Xuelei Liang, Zhiyong Zhang, Lian-Mao Peng, and Youfan Hu. Low-power carbon nanotube-based integrated circuits that can be transferred to biological surfaces. *Nature Electronics*, 1(4):237–245, 2018.

[63] Suman Kalyan Samanta, Martin Fritsch, Ullrich Scherf, Widianta Gomulya, Satria Zulkarnaen Bisri, and Maria Antonietta Loi. Conjugated polymer-assisted dispersion of single-wall carbon nanotubes: the power of polymer wrapping. *Accounts of chemical research*, 47(8):2446–2456, 2014.

[64] Jacques Lefebvre, Jianfu Ding, Zhao Li, Paul Finnie, Gregory Lopinski, and Patrick RL Malenfant. High-purity semiconducting single-walled carbon nanotubes: a key enabling material in emerging electronics. *Accounts of chemical research*, 50(10):2479–2486, 2017.

[65] Ting Lei, Igor Pochorovski, and Zhenan Bao. Separation of semiconducting carbon nanotubes for flexible and stretchable electronics using polymer removable method. *Accounts of chemical research*, 50(4):1096–1104, 2017.

[66] Michael L Geier, Julian J McMorrow, Weichao Xu, Jian Zhu, Chris H Kim, Tobin J Marks, and Mark C Hersam. Solution-processed carbon nanotube thin-film complementary static random access memory. *Nature nanotechnology*, 10(11):944–948, 2015.

[67] Huiliang Wang, Peng Wei, Yaoxuan Li, Jeff Han, Hye Ryoung Lee, Benjamin D Naab, Nan Liu, Chenggong Wang, Eric Adijanto, Benjamin C-K Tee, et al. Tuning the threshold voltage of carbon nanotube transistors by n-type molecular doping for robust and flexible complementary circuits. *Proceedings of the National Academy of Sciences*, 111(13):4776–4781, 2014.

[68] Kevin S Mistry, Brian A Larsen, and Jeffrey L Blackburn. High-yield dispersions of large-diameter semiconducting single-walled carbon nanotubes with tunable narrow chirality distributions. *ACS nano*, 7(3):2231–2239, 2013.

[69] Gerald J Brady, Austin J Way, Nathaniel S Safron, Harold T Evensen, Padma Gopalan, and Michael S Arnold. Quasi-ballistic carbon nanotube array transistors with current density exceeding si and gaas. *Science advances*, 2(9):e1601240, 2016.

[70] Leilai Shao, Tsung-Ching Huang, Ting Lei, Zhenan Bao, Raymond Beausoleil, and Kwang-Ting Cheng. Compact modeling of carbon nanotube thin film transistors for flexible circuit design. In *2018 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 491–496. IEEE, 2018.

[71] Tsung-Ching Huang, Kenjiro Fukuda, Chun-Ming Lo, Yung-Hui Yeh, Tsuyoshi Sekitani, Takao Someya, and Kwang-Ting Cheng. Pseudo-cmos: A design style for low-cost and robust flexible electronics. *IEEE Transactions on Electron Devices*, 58(1):141–150, 2010.

[72] Ting Lei, Xiyuan Chen, Gregory Pitner, H-S Philip Wong, and Zhenan Bao. Removable and recyclable conjugated polymers for highly selective and high-yield dispersion and release of low-cost carbon nanotubes. *Journal of the American Chemical Society*, 138(3):802–805, 2016.

[73] Stephen A McGill, Saleem G Rao, Pradeep Manandhar, Peng Xiong, and Seunghun Hong. High-performance, hysteresis-free carbon nanotube field-effect transistors via directed assembly. *Applied physics letters*, 89(16):163123, 2006.

[74] Tsuyoshi Sekitani, Tomoyuki Yokota, Kazunori Kuribara, Martin Kaltenbrunner, Takanori Fukushima, Yusuke Inoue, Masaki Sekino, Takashi Isoyama, Yusuke Abe, Hiroshi Onodera, et al. Ultraflexible organic amplifier with biocompatible gel electrodes. *Nature communications*, 7(1):1–11, 2016.

[75] Kris Myny. The development of flexible integrated circuits based on thin-film transistors. *Nature electronics*, 1(1):30–39, 2018.

[76] Joseph Chang, Xi Zhang, Tong Ge, and Jia Zhou. Fully printed electronics on flexible substrates: High gain amplifiers and dac. *Organic Electronics*, 15(3):701–710, 2014.

[77] Koich Ishida, Reza Shabanpour, Bahman K Boroujeni, Tilo Meister, Corrado Carta, Frank Ellinger, Luisa Petti, Niko S Münzenrieder, Giovanni A Salvatore, and Gerhard Tröster. 22.5 db open-loop gain, 31 khz gbw pseudo-cmos based operational amplifier with a-igzo tfts on a flexible film. In *2014 Ieee Asian Solid-State Circuits Conference (a-Sscc)*, pages 313–316. IEEE, 2014.

[78] Tiffany Moy, Liechao Huang, Warren Rieutort-Louis, Can Wu, Paul Cuff, Sigurd Wagner, James C Sturm, and Naveen Verma. An eeg acquisition and biomarker-extraction system using low-noise-amplifier and compressive-sensing circuits based on flexible, thin-film electronics. *IEEE Journal of Solid-State Circuits*, 52(1):309–321, 2016.

[79] Heng Zhang, Li Xiang, Yingjun Yang, Mengmeng Xiao, Jie Han, Li Ding, Zhiyong Zhang, Youfan Hu, and Lian-Mao Peng. High-performance carbon nanotube complementary electronics and integrated sensor systems on ultrathin plastic foil. *ACS nano*, 12(3):2773–2779, 2018.

[80] Xiang Zhang, Jianwen Zhao, Junyan Dou, Masayoshi Tange, Weiwei Xu, Lixin Mo, Jianjun Xie, Wenya Xu, Changqi Ma, Toshiya Okazaki, et al. Flexible cmos-like circuits based on printed p-type and n-type carbon nanotube thin-film transistors. *Small*, 12(36):5066–5073, 2016.

[81] Yudan Zhao, Qunqing Li, Xiaoyang Xiao, Guanhong Li, Yuanhao Jin, Kaili Jiang, Jiaping Wang, and Shoushan Fan. Three-dimensional flexible complementary metal–oxide–semiconductor logic circuits based on two-layer stacks of single-walled carbon nanotube networks. *ACS nano*, 10(2):2193–2202, 2016.

[82] Dong-ming Sun, Marina Y Timmermans, Ying Tian, Albert G Nasibulin, Esko I Kauppinen, Shigeru Kishimoto, Takashi Mizutani, and Yutaka Ohno. Flexible high-performance carbon nanotube integrated circuits. *Nature nanotechnology*, 6(3):156–161, 2011.

[83] Dong-Ming Sun, Marina Y Timmermans, Antti Kaskela, Albert G Nasibulin, Shigeru Kishimoto, Takashi Mizutani, Esko I Kauppinen, and Yutaka Ohno. Mouldable all-carbon integrated circuits. *Nature communications*, 4:2302, 2013.

[84] Yong-Hoon Kim, Jae-Sang Heo, Tae-Hyeong Kim, Sungjun Park, Myung-Han Yoon, Jiwan Kim, Min Suk Oh, Gi-Ra Yi, Yong-Young Noh, and Sung Kyu Park. Flexible metal-oxide devices made by room-temperature photochemical activation of sol–gel films. *Nature*, 489(7414):128–132, 2012.

[85] Dalong Zhao, Devin A Mourey, and Thomas N Jackson. Fast flexible plastic substrate zno circuits. *IEEE Electron Device Letters*, 31(4):323–325, 2010.

[86] Kris Myny, Soeren Steudel, Steve Smout, Peter Vicca, Francois Furthner, Bas van der Putten, Ashutosh K Tripathi, Gerwin H Gelinck, Jan Genoe, Wim Dehaene, et al. Organic rfid transponder chip with data rate compatible with electronic product coding. *Organic Electronics*, 11(7):1176–1179, 2010.

[87] Ute Zschieschang, Frederik Ante, Tatsuya Yamamoto, Kazuo Takimiya, Hirokazu Kuwabara, Masaaki Ikeda, Tsuyoshi Sekitani, Takao Someya, Klaus Kern, and Hagen Klauk. Flexible low-voltage organic transistors and circuits based on a high-mobility organic semiconductor with good air stability. *Advanced Materials*, 22(9):982–985, 2010.

[88] David K Kim, Yuming Lai, Benjamin T Diroll, Christopher B Murray, and Cherie R Kagan. Flexible and low-voltage integrated circuits constructed from high-performance nanocrystal transistors. *Nature communications*, 3(1):1–6, 2012.

[89] Feng Xu, Meng-Yin Wu, Nathaniel S Safron, Susmit Singha Roy, Robert M Jacobberger, Dominick J Bindl, Jung-Hun Seo, Tzu-Hsuan Chang, Zhenqiang Ma, and Michael S Arnold. Highly stretchable carbon nanotube transistors with ion gel gate dielectrics. *Nano letters*, 14(2):682–686, 2014.

[90] Bryant Chu, William Burnett, Jong Won Chung, and Zhenan Bao. Bring on the bodynet. *Nature News*, 549(7672):328, 2017.

[91] Mallory L Hammock, Alex Chortos, Benjamin C-K Tee, Jeffrey B-H Tok, and Zhenan Bao. 25th anniversary article: the evolution of electronic skin (e-skin): a brief history,

design considerations, and recent progress. *Advanced materials*, 25(42):5997–6038, 2013.

[92] Takao Someya, Zhenan Bao, and George G Malliaras. The rise of plastic bioelectronics. *Nature*, 540(7633):379, 2016.

[93] Jin Young Oh, Simon Rondeau-Gagné, Yu-Cheng Chiu, Alex Chortos, Franziska Lissel, Ging-Ji Nathan Wang, Bob C Schroeder, Tadanori Kurosawa, Jeffrey Lopez, Toru Katsumata, et al. Intrinsically stretchable and healable semiconducting polymer for organic transistors. *Nature*, 539(7629):411, 2016.

[94] Alex Chortos, Ghada I Koleilat, Raphael Pfattner, Desheng Kong, Pei Lin, Roda Nur, Ting Lei, Huiliang Wang, Nan Liu, Ying-Chih Lai, et al. Mechanically durable and highly stretchable transistors employing carbon nanotube semiconductor and electrodes. *Advanced Materials*, 28(22):4441–4448, 2016.

[95] Manas Rakshit and Susmita Das. An efficient ECG denoising methodology using empirical mode decomposition and adaptive switching mean filter. *Biomedical Signal Processing and Control*, 40:140–148, feb 2018.

[96] Peng Xiong, Hongrui Wang, Ming Liu, Suiping Zhou, Zengguang Hou, and Xiuling Liu. ECG signal enhancement based on improved denoising auto-encoder. *Engineering Applications of Artificial Intelligence*, 52:194–202, 2016.

[97] Nick Van Helleputte, Sunyoung Kim, Hyejung Kim, Jong Pal Kim, Chris Van Hoof, and Refet Firat Yazicioglu. A 160μa biopotential acquisition asic with fully integrated ia and motion-artifact suppression. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, pages 118–120. IEEE, 2012.

[98] Martin J Burke and Denis T Gleeson. A micropower dry-electrode ecg preamplifier. *IEEE Transactions on Biomedical Engineering*, 47(2):155–162, 2000.

[99] Yu Mike Chi, Tzyy-Ping Jung, and Gert Cauwenberghs. Dry-contact and noncontact biopotential electrodes: Methodological review. *IEEE reviews in biomedical engineering*, 3:106–119, 2010.

[100] George B Moody, W Muldrow, and Roger G Mark. A noise stress test for arrhythmia detectors. *Computers in cardiology*, 11(3):381–384, 1984.

[101] George B Moody and Roger G Mark. The impact of the mit-bih arrhythmia database. *IEEE Engineering in Medicine and Biology Magazine*, 20(3):45–50, 2001.

[102] Tsuyoshi Sekitani, Tomoyuki Yokota, Kazunori Kuribara, Martin Kaltenbrunner, Takanori Fukushima, Yusuke Inoue, Masaki Sekino, Takashi Isoyama, Yusuke Abe, Hiroshi Onodera, and Takao Someya. Ultraflexible organic amplifier with biocompatible gel electrodes. *Nature Communications*, 7, 2016.

[103] Tiffany Moy, Liechao Huang, Warren Rieutort-Louis, Can Wu, Paul Cuff, Sigurd Wagner, James C. Sturm, and Naveen Verma. An EEG Acquisition and Biomarker-Extraction System Using Low-Noise-Amplifier and Compressive-Sensing Circuits Based on Flexible, Thin-Film Electronics. *IEEE Journal of Solid-State Circuits*, 52(1):309–321, 2017.

[104] Rei Shiwaku, Hiroyuki Matsui, Kuniaki Nagamine, Mayu Uematsu, Taisei Mano, Yuki Maruyama, Ayako Nomura, Kazuhiko Tsuchiya, Kazuma Hayasaka, Yasunori Takeda, Takashi Fukuda, Daisuke Kumaki, and Shizuo Tokito. A printed organic amplification system for wearable potentiometric electrochemical sensors. *Scientific Reports*, 8(1):1–8, 2018.

[105] Leilai Shao, Tsung-Ching Huang, Ting Lei, Zhenan Bao, Raymond Beausoleil, and Kwang-Ting Cheng. Compact modeling of carbon nanotube thin film transistors for flexible circuit design. In *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2018*, pages 491–496. IEEE, 2018.

[106] Le Cai and Chuan Wang. Carbon nanotube flexible and stretchable electronics. *Nanoscale research letters*, 10(1):1, 2015.

[107] Gari D Clifford, Chengyu Liu, Benjamin Moody, Li-wei H Lehman, Ikaro Silva, Qiao Li, AE Johnson, and Roger G Mark. Af classification from a short single lead ecg recording: The physionet computing in cardiology challenge 2017. *Proceedings of Computing in Cardiology*, 44:1, 2017.

[108] Fernando Andreotti, Oliver Carr, Marco AF Pimentel, Adam Mahdi, and Maarten De Vos. Comparing feature-based classifiers and convolutional neural networks to detect arrhythmia from short segments of ecg. *Computing*, 2017.

[109] Vykintas Maknickas, Algirdas Maknickas, and LLC Tesonet. Atrial fibrillation classification using qrs complex features and lstm. *Computing*, 2017.

[110] Kaiming He, Xiangyu Zhang, Shaoqing Ren, and Jian Sun. Deep residual learning for image recognition. In *Proceedings of the IEEE conference on computer vision and pattern recognition*, pages 770–778, 2016.

[111] Op-Amp Imperfections. Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization. *Proceedings of the IEEE*, 84(11), 1996.

[112] Leilai Shao, Sicheng Li, Ting Lei, Tsung-Ching Huang, Raymond Beausoleil, Zhenan Bao, and Kwang-Ting Cheng. Ultra-thin skin electronics for high quality and continuous skin-sensor-silicon interfacing. In *Proceedings of the 56th Annual Design Automation Conference 2019*, page 16. ACM, 2019.

[113] Ting Lei, Ming Guan, Jia Liu, Hung-Cheng Lin, Raphael Pfattner, Leo Shaw, Allister F McGuire, Tsung-Ching Huang, Leilai Shao, Kwang-Ting Cheng, et al. Biocompatible and totally disintegrable semiconducting polymer for ultrathin and ultralightweight transient electronics. *Proceedings of the National Academy of Sciences*, 114(20):5107–5112, 2017.

[114] Ting Lei, Igor Pochorovski, and Zhenan Bao. Separation of semiconducting carbon nanotubes for flexible and stretchable electronics using polymer removable method. *Accounts of chemical research*, 50(4):1096–1104, 2017.

[115] Ting Lei, Lei-Lai Shao, Yu-Qing Zheng, Gregory Pitner, Guanhua Fang, Chenxin Zhu, Sicheng Li, Ray Beausoleil, H-S Philip Wong, Tsung-Ching Huang, et al. Low-voltage high-performance flexible digital and analog circuits based on ultrahigh-purity semiconducting carbon nanotubes. *Nature communications*, 10(1):2161, 2019.

[116] Leilai Shao, Ting Lei, Tsung-Ching Huang, Sicheng Li, Ta-ya Chu, Man Wong, Raymond Beausoleil, Zhenan Bao, and Kwang-Ting Cheng. Compact modeling of thin film transistors for flexible hybrid iot design. *IEEE Design & Test*, 2019.

[117] Vitaly Podzorov, E Menard, A Borissov, Valery Kiryukhin, John A Rogers, and ME Gershenson. Intrinsic charge transport on the surface of organic semiconductors. *Physical review letters*, 93(8):086602, 2004.

[118] Veaceslav Coropceanu, Jérôme Cornil, Demetrio A da Silva Filho, Yoann Olivier, Robert Silbey, and Jean-Luc Brédas. Charge transport in organic semiconductors. *Chemical reviews*, 107(4):926–952, 2007.

[119] Emmanuel J Candès and Michael B Wakin. An introduction to compressive sampling [a sensing/sampling paradigm that goes against the common knowledge in data acquisition]. *IEEE signal processing magazine*, 25(2):21–30, 2008.

[120] Ery Arias-Castro and Yonina C Eldar. Noise folding in compressed sensing. *IEEE Signal Processing Letters*, 18(8):478–481, 2011.

[121] Mario Caironi, Enrico Gili, Tomo Sakanoue, Xiaoyang Cheng, and Henning Sirringhaus. High yield, single droplet electrode arrays for nanoscale printed electronics. *ACS nano*, 4(3):1451–1456, 2010.

[122] Xi Liu, Yun-Ze Long, Lei Liao, Xiangfeng Duan, and Zhiyong Fan. Large-scale integration of semiconductor nanowires for high-performance flexible electronics. *ACS nano*, 6(3):1888–1900, 2012.

[123] Rafael C Gonzalez, Richard E Woods, et al. Digital image processing, 2002.

[124] Hsiu-Ming Chang, Kwang-Ting Cheng, Wangyang Zhang, Xin Li, and Kenneth M Butler. Test cost reduction through performance prediction using virtual probe. In *2011 IEEE International Test Conference*, pages 1–9. IEEE, 2011.

[125] Ting Lei, Gregory Pitner, Xiyuan Chen, Guosong Hong, Steve Park, Pascal Hayoz, Ralf Thomas Weitz, Hon-Sum Philip Wong, and Zhenan Bao. Dispersion of high-purity semiconducting arc-discharged carbon nanotubes using backbone engineered diketopyrrolopyrrole (dpp)-based polymers. *Advanced Electronic Materials*, 2(1):1500299, 2016.

[126] Yeongin Kim, Alex Chortos, Wentao Xu, Yuxin Liu, Jin Young Oh, Donghee Son, Jiheong Kang, Amir M Foudeh, Chenxin Zhu, Yeongjun Lee, et al. A bioinspired flexible organic artificial afferent nerve. *Science*, 360(6392):998–1003, 2018.

[127] John Wright, Arvind Ganesh, Shankar Rao, Yigang Peng, and Yi Ma. Robust principal component analysis: Exact recovery of corrupted low-rank matrices via convex optimization. In *Advances in neural information processing systems*, pages 2080–2088, 2009.