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Asynchronous High Speed Serial Links Analysis using Integrated Charge for Event Detection

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ABSTRACT

We present a metric for event detection, targeted for the analysis of CMOS asynchronous serial data links. Our metric is used to analyze signaling strategies that allow for coincident or nearly coincident detection of both data and event timing. The metric predicts that the CMOS link signaling mechanism has substantial implicit dispersion and intersymbol interference [ISI] tolerance when compared to conventionally timed links. In fact, it predicts correct link operation in situations where eye-diagram techniques predict link failure. Practical operation margins and metrics are described and evaluated for PCB and cabling solutions suggesting 10+ Gb/s low-power asynchronous links could be implemented in CMOS 130nm technology.

1. INTRODUCTION

High speed serial links are commonly used in digital systems to move data between physically separated functional units. Serial links are attractive, because a single bit stream is easy to route and synchronize. High bit-rate links require low-jitter clocks and accurate clock-data recovery. Inevitably, the time base (clock) used to transmit the serial signal and the natural time base of the receiving circuit drift relative to each other. The circuits that compensate for this can be synchronous to, at most, one of the two time domains, giving rise to the use of asynchronous state-machines to handle the transition (phase alligners, FIFOs, bus arbiters, etc). Effectively, asynchronous machines are used in transmission regardless of whether the data is synchronous to a local clock. Thus, signaling methods that are naturally compatible with asynchronous logic become a promising subject of investigation. Asynchronous link design has been the subject of a number of recent studies [1], [2], [3]. Traditional asynchronous protocols are limited in speed due to the need to acknowledge data [2], [4]. In [5] asynchronous protocols share data lines, but performance depends on wire delays. In this work, we target (impolite) asynchronous links that do not use handshaking such as [6]. This subset of links lacks the feed-back bottle-neck allowing link time-of-flight to be longer than a bit transfer. The critical point of this model is that timing (arrival) of each bit must be unambiguous despite the unknown arrival time and the guarantee of this feature is designed into the system with margins. Signal integrity analysis is thus critical to determining if such a link has sufficient margins to meet the standards of unambiguous reception.

We introduce an integral charge model as a detection and analysis metric. The metric has the advantage that it mimics the behavior of CMOS transistors, which by nature accumulate charge and act when a threshold is reached. This metric is used to examine a variety of link signaling strategies and compare the suitability of the strategies in terms of noise, bandwidth, and practicality on realistic media models such as inexpensive coaxial cable and PCB transmission lines. For a signaling pulse, the critical measure becomes the integral of the pulse shape, rather than its amplitude or duration. Detection of edges, by contrast, is achieved by integrating a voltage level and subsequently integrating a new level leading to both *setup* and *hold* specifications for edge-detection. In that case, the integral is analogous to a slew measurement or RC delay model.

In Section 2 an integrated charge ($Q_{\int}$) metric is described. Section 3 presents an example application based on the integrated charge ($Q_{\int}$) metric. Section 4 defines metrics to analyze integrated charge ($Q_{\int}$) in a transmission media and describes transmission line effects on integrated Charge ($Q_{\int}$). Section 5 evaluates how to determine the data transfer rate of a practical link implementation. Section 6 presents results of datarate (Gb/s) for two different transmission media simulated over a range of lengths for edge and pulse based encoding.

2. INTEGRATED CHARGE METRIC

CMOS circuits, in general, have capacitive, voltage-sensitive, inputs. Digital logic, by design, provides well-defined, stable outputs between transitions. With a well-defined starting voltage, and a capacitive input one can define the amount of charge required to reach a given voltage as $Q_{\int}$, the integrated input charge. When $Q_{\int}$ reaches some value (Q_{crit}) the decision voltage (V_{trig}) is reached on the front-end, and the gate, from an event-driven perspective, is triggered. Timing critical asynchronous machines, such as synchronizers and phase detectors, have made use of integrated charge as early as some of the first CMOS based sawtooth phase de-

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tectors [7]. Equation 1 formalizes a $Q_\int$ metric which models a gate triggering condition.

$$\int g_m \cdot min(0, V_{in}(t) - V_{Imin}) \geq Q_{crit} = V_{trig} \cdot C_{eff} \quad (1)$$

This triggering condition signifies the minimum charge (Q_{crit}) to successfully recieve information. V_{Imin} represents the minimum voltage required to start integrating charge at the critical node (the noise rejection threshold). g_m represents the transconductance of the circuit averaged over the decision region. C_{eff} is the effective capacitance at the detection node. The validity of the $Q_\int$ measure is dependent on g_m being a valid representation of transconductance over a range of inputs between V_{Imin} and V_{trig}. Note that if the $Q_\int$ is below the V_{Imin} it should not affect the critical node at all. If the $Q_\int$ above V_{Imin} is less than $V_{DD}C_{crit}$ then the critical node should not be affected and no event must be detected. Lastly, two equal $Q_\int$ above V_{Imin} should have similar effects on the event detection.

3. EXAMPLE APPLICATION

To demonstrate the use of the $Q_\int$ concept we examine a circuit designed for data transmission, using self-resetting logic [6]. A receiver/pulse-shaper circuit from this family is shown in Figure 1. The critical values for Equation 1 are derived from the behavior of this pulse shaper: $Q_\int \geq Q_{crit}$ will cause a pulse on the output, while V_{Imin} is established by the noise suppressing keeper, the 10k resistor, and V_{trig} is set by the decision voltage of the inverter driving the output.

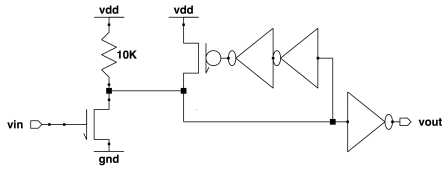

Figure 1: Logic circuit for detection of Integrated Charge ($Q_\int$) encoded as a pulse.

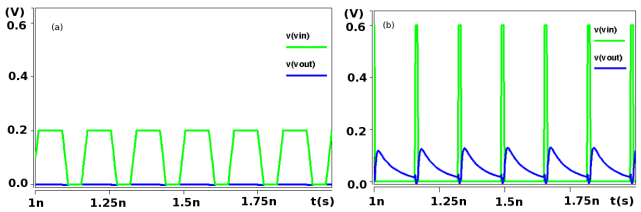

Figure 2: (a) Incoming pulse amplitude below V_{Imin} at critical node. (b) Incoming pulse amplitude above V_{Imin} at the critical node but $Q_\int$ is below Q_{crit}

Figure 2 shows circuit critical node behavior for two cases where $Q_\int < Q_{crit}$. In the first case (Figure 2(a)), Pulses don't cross above V_{Imin}, and no charge is accumulated. In the second case, (Figure 2(b)) Pulses cross V_{Imin} but V_{trig} is not reached and no pules result on the output. By contrast, Figure 3 demonstrates two cases of $Q_\int > Q_{crit}$. Here two pulse trains (dashed lines) at input both result as pulse trains a the output (solid lines). The relative difference in pulse shapes does not alter the one-pulse-in-one-pulse-out function. Thus, this simple model can be used to validate detection in this and similar signaling strategies.

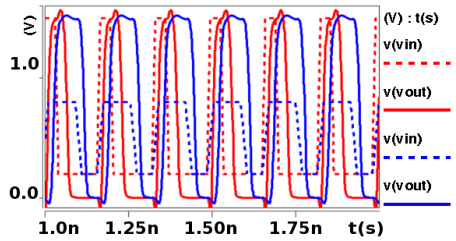

Figure 3: Different input pulses (dotted line) with same $Q_\int$ result in equivalent output.

4. INTEGRATED CHARGE AND SIGNAL INTEGRITY

$Q_\int$ has promise as an evaluation tool for signal integrity for asynchronous links, because it can describe the triggering conditions of asynchronous circuits. Classic measures of signal integrity for synchronous links, such as eye diagrams, focus on amplitude and timing uncertainty, while $Q_\int$ can better describe circuits where there is a trade-off between the two.

4.1 Timing variance & voltage noise

Variance in signal timing can be induced by loss in transmission media or from coupled noise. For example, Figure 4 shows strong loss applied to both edge, and pulse encoded signals. A lossy line induces a delay in the signal that is dependent on the previous, incomplete transmission.

To first order, $Q_\int$ can be viewed as the area in the signal above the defined threshold V_{Imin}. If this area is above Q_{crit} then the signal is successfully transmitted. $Q_\int$ here matches the human intuition that the signals in Figure 4 are interpretable if one were to set the levels correctly, even though neither of these curves would have an open eye. Hence $Q_\int - Q_{crit}$ serves as a noise margin allowing the selection of both V_{Imin} and Q_{crit}.

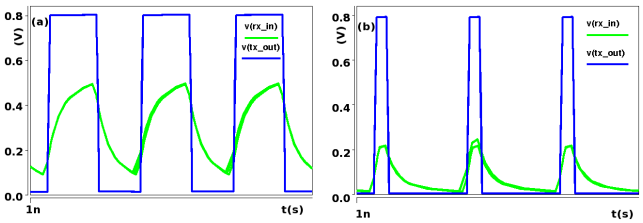

Figure 4: Jitter & attenuation for (a) Edge (b) Pulse

4.2 Inter Symbol Interference (ISI)

ISI, mainly caused by reflections, is a significant potential source of noise in a link. Such reflections are often due to impedance mismatches in the transmission media. Reflections can cause two effects, either interfere with the detection of an intended signal or inject a detectable unintended signal.

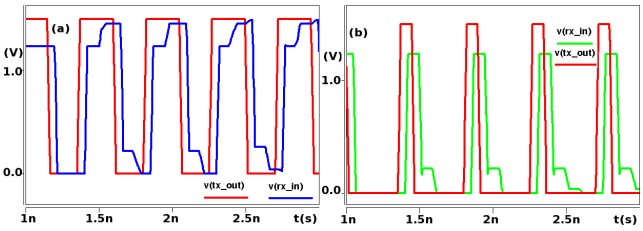

Figure 5: (a) Positive edge reflections have potential for double edge detection (b) Positive pulse reflections adding the charge where is does not exist and decreasing noise margin

Figure 5 shows the effect of positive reflections, due to under-termination, on both pulse and edge coded links. It can be seen that if the $Q_{\int}$ added because of positive reflection between the encoded information remains below noise margin, the information will be transmitted reliably. In case of negative reflections, if the $Q_{\int}$ remains above the noise margin the signal would be detected and the information will be successfully transmitted. It can be seen that it is advantageous to have positive reflections in the receiver as it adds to the signal, but it needs to be ensured that the noise created because of it remains below the noise margin.

4.3 Attenuation, Jitter and Dispersion

Attenuation is the result of losses in the transmission media, which are frequency dependent as higher frequencies are more susceptible to skin-effect, dielectric loss, and radiative loss. Attenuation is given by Equation 2 according to [8], where frequency dependent resistance and inductance are given by Equation 3 and Equation 4. If the information is represented as $Q_{\int}$, the effect of attenuation is decreased in the $Q_{\int}$ value as the signal passes through the transmission media.

$$atten = 20\ log_{10}[\exp(Re\sqrt{(R+j\omega L)(G+j\omega C)})] \quad (2)$$

$$R(f) = \omega\frac{\delta}{2}\frac{\partial L}{\partial n}; \delta = \sqrt{\frac{\rho}{\pi f \mu}} \quad (3)$$

$$L(f) = L_{external} + L_{internal} = L_{external} + \frac{\delta}{2}\frac{\partial L}{\partial n} \quad (4)$$

Dispersion is a spreading of signal energy in time. Dispersion is given by Equation 5 according to [8], where Equation 3 and Equation 4 are its frequency dependent resistance and inductance. Dispersion leads to phase variance in the transmitted information. Dispersion has a major effect in setting the data rate through the transmission media. The pulse encoding suffers from pulse widening and edge encoding from increase in rise and fall times. Jitter is the phase shift of the symbol resulting in external and internal noise in the system.

$$\beta(f) = Im[\sqrt{(R+j\omega L)(G+j\omega C)}] \quad (5)$$

Figure 4 shows the effect of attenuation, jitter and dispersion on the $Q_{\int}$ encoded as a pulse and an edge. Channel jitter also shows up as phase variance and can be similarly accounted for. Dispersion and jitter both result in phase variance and have been taken into account collectively as phase variance in this paper for analysis in the later sections. Successful reception requires that the $Q_{\int}$ after the attenuation and phase variance in the media remain above the noise margin.

4.4 Baseline Shift

For 2-wire transmission schemes, common mode (both wires changing in the same direction) content in the information sent over the transmission line shifts the reception baseline at the receiver. This results in a shift in the V_{Imin} value at the receiver as compared to that at the transmitter. For example baseline shift at the receiver event detector when constant pulses are sent down a meter of 50 ohms trace in a FR4 PCB can be about 300 mV. The offset is proportional to media length and can be mitigated by differential transmission or by chosing line codes with minimal common mode content.

5. DATA TRANSFER RATE

The maximum data rate of a link can be limited by the transmission media due to frequency dependent loss. Since loss and noise grow with distance, there is a trade off between data rate and link length. Data transmission over longer distances require that the $Q_{\int}$ remains above the noise margin after ISI, attenuation and jitter effects. Additionally, two adjacent symbols need to be kept from colliding due to jitter. A working link needs to maintain sufficient signal strength and temporal separation such that $Q_{\int}$ over the noise threshold represents an achievable Q_{crit} at the receiver.

For RZ pulse encoding, there is a minimum separation between pulses at the transmitter output to allow reliable detection at the end of the transmission line. The attenuation provides with different charge loss at different lengths of transmission media. Thus, the minimum charge needed by the detector to work reliably puts the limit on transmission line lengths. Phase variance allows determination of the minimum separation of pulses for different lengths of transmission media. This result is highly dependent on the jitter in the transmitter. The separation of effects determine the data rate depending on how many pulses can be accommodated in a given clock cycle. Hence if:

$$Q_{initial} - Q_{loss} \geq Q_{min\ detectable} \quad (6)$$

where $Q_{initial}$ is the charge in the minimum sized pulse. The minimum sized pulse generation is technology dependent. Then:

$$data\ rate = \left\lfloor \frac{T_{clock}/2}{T_{min\ pulse}} \right\rfloor \times \frac{2}{T_{clock}} \quad (7)$$

Else increase $Q_{initial}$ and calculate date rate according to new $T_{min\ pulse}$.

For edge based encoding, the minimum charge needed at the receiver directly helps in determining the minimum separation between the edges. T_{min} is the value of time it takes to reach the minimum detectable charge at the event detector. The value increases with length as the edge slope decreases with length. It is ensured that transmitter can transmit this minimum separation reliably. Thus, the data rate is determined by how many edges can be accommodated in a single clock cycle. Hence if:

$$T_{min\ edge} \geq T_{min}\ and\ T_{detector\ edge} \geq T_{min} \quad (8)$$

where $T_{min\ edge}$ is the minimum possible separation between the edges from the transmitter and $T_{detector\ edge}$ is the sep-

aration between the edges at the receiver or detector measured from V_{Imin}. then:

$$data\ rate = \left\lfloor \frac{T_{clock}/2}{T_{min\ edge}} \right\rfloor \times \frac{2}{T_{clock}} \quad (9)$$

Else increase $T_{min\ edge}$ and calculate the data rate again. Hence data rate in general is given by:

$$data\ rate = \left\lfloor \frac{T_{clock}/2}{T_{min\ symbol}} \right\rfloor \times \frac{2}{T_{clock}} \times N_{transition} \quad (10)$$

where $T_{min\ symbol}$ is the minimum possible separation between the symbols (edges or pulses) and $N_{transition}$ is the number of valid transitions possible after each transition.

6. RESULTS

The minimum detectable charge for the receiver based on circuit topology in Figure 1 is shown in Figure 6. The plots are done for 75ps pulse width at the transmitter and hence an initial charge of $44.25V.ps$. The minimum detectable

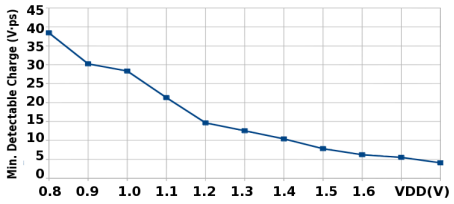

Figure 6: Minimum Detectable Charge

charge from Figure 6 has the value of 7.8 V.ps for 1.5V VDD. The minimum separation between the 75 ps pulses taking phase variance into account is 185ps. This value is highly dependent on jitter due to transmitter. This results in a 5.12 Gb/s data rate in the RZ encoded pulse link using Equation 10. The minimum time difference between the edges to take phase variance in the link and transmitter design constraints into account is 185ps, which is greater than T_{min}. This results in a data rate of 5.12 Gb/s using Equation 10 for 2 level edge based encoding. Figure 7 shows the increasing loss with length in the edge and pulse based links. This results in data rate as shown in Figure 8, which can be seen to be above 5Gb/s for about 5 feet in FR4 stripline. Data rates remain above 5Gb/s for RG-178 in lengths up to 6 feet.

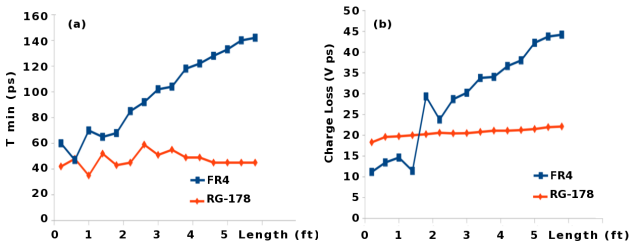

Figure 7: Loss vs Length in (a) Edge and (b) Pulse

The constraints on minimum separation of edges in two and three level encoding does not change but $N_{transition}$ has a value of two in three level encoding. Hence, data rate of the order of 10.24 Gb/s in the lengths in order of

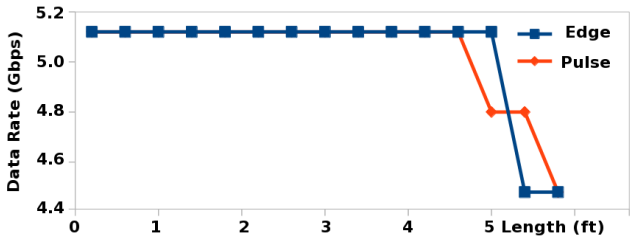

Figure 8: Data Rate vs Length

5 feet in PCB and coaxial cables is achievable with 130nm technology using Equation 10. The implementation must be fully differential to alleviate the baseline shift or line coding schemes must be used to reduce the integral common mode content in all these implementations. $Q_{\int}$ metric used in the presented results has an advantage over conventional eye diagram based metric as the effects mentioned in section 4 only become apparent at lengths greater than 5 ft in the analyzed media. Hence a substantially higher data rate is achievable at a given length with the use of $Q_{\int}$ metric.

7. CONCLUSIONS

A new methodology to alleviate the problems associated with conventional serial link designs was proposed. The proposed $Q_{\int}$ metric can help us make a jitter tolerant link, which can be self timed to get away from time of flight issues in handshaking and not have additional circuitry for synchronization and maintaining signal integrity. The link also has negligible idle state power consumption and can be used with conventional asynchronous techniques alongside the link. The margins for proper utilization of the metric were described and a design was proposed for implementation of a 10+ Gb/s link in 130nm.

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