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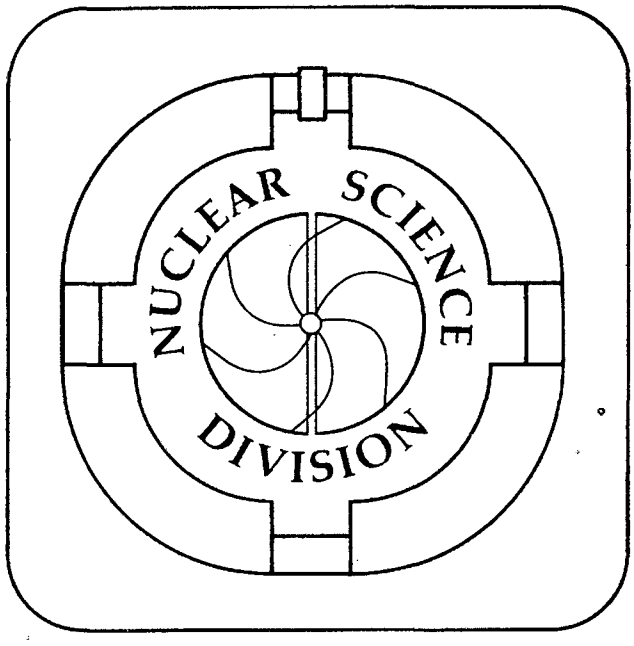

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DISCLAIMER

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ABSTRACT

We report on the design and performance of high speed data links and slower configuration control links used between the EOS TPC detector and the data processing electronics. Data rates of 5MBytes/s/link are maintained over 30m with optical isolation. Pedestal subtraction, hit detection , and data reordering are performed online.

I. INTRODUCTION

The Equation-of-State Time Projection Chamber (EOS TPC) being constructed at the U. C. Lawrence Berkeley Laboratory will be used by the Relativistic Nuclear Collisions group to study heavy-ion interactions at the Bevalac[1]. The TPC has 15,360 8mm x 12mm pads each instrumented with a low-noise preamplifier, shaper, and 256-cell analog storage device [2] which is loaded at 10MHz. Above the pad plane is an electric field cage forming the 1.5m x 1.0m x 0.8m active drift volume. All analog signal processing circuits including the ADCs which digitize the stored analog samples are mounted directly on the detector. The TPC will be located in the 2m diameter x 1m gap of the H.I.S.S. superconducting dipole magnet.

The data handling system for the EOS TPC is designed to do as much data correction, reorganization and compression as possible before writing to tape while keeping up with an event rate of 10 heavy (Au on Au) or 100 light (C on C) events/s. The custom-built data receiver modules contain Programmable Logic Cell Arrays and DSPs to perform this logic. Commercial VME modules using 68030 microprocessors are used to gather the data, build events in memory arrays, write the data onto 8mm tape casettes, and make data available to workstations for quick-look analysis.

II. THE DATA

The on-chamber electronics is organized as 128 boards each servicing 120 pads. For the maximum number of time-sequential samples = 256, each event produces 120pads x 128boards x 256samples x 2bytes = 7.86MBytes. At 100 events/second this implies a serial bitstream of 6.3GHz. By using one data link for each of the 128 boards, the required bandwidth is a modest 50MHz. In addition to the digitized pad data, housekeeping data (e.g. board ID#, event#, configuration, temperature, power supply voltages, etc.) must be included in each bit stream. The event number is a check of data synchronization between the boards. A 64KByte memory array on each board can be used to supply a complete pseudo-event data stream. By starting with a known data set, the data handling hardware and software can be tested. A typical data link channel is shown in Figure 1.

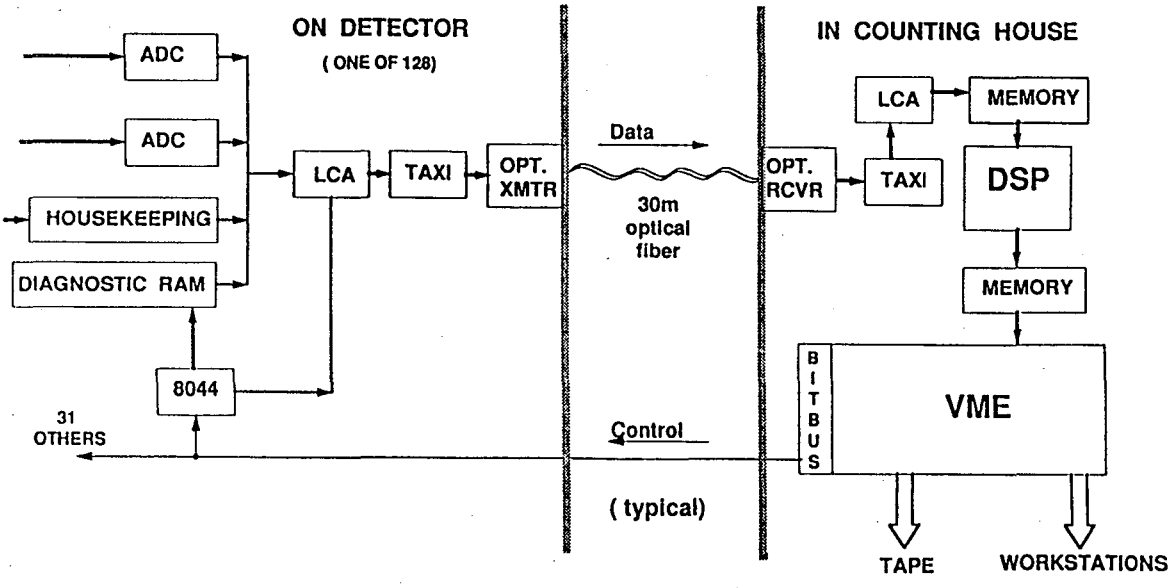

Figure 1. A typical data link from the TPC to the counting house

III. THE DOWN LINK

The data-handling hardware is the same on each of the 128 on-chamber boards: after the analog memories have been loaded, the interleaved outputs of two 1MHz ADCs plus housekeeping data (or a test event from diagnostic RAM) are presented, one byte at a time, to an AM7968 Transparent Asynchronous Xmitter-Receiver Interface (TAXI) chip [3] which applies 4 to 5 bit Manchester encoding and produces a serial NRZ bit stream. Transmission begins with a "command" word followed by all the pad data. A second command word precedes the housekeeping data. The event always ends with a third command word indicating a normal or a truncated transmission. This serial data is transmitted over 30m of 100μ optical fiber to receiver modules in the counting house. The use of optical coupling prevents ground loops from affecting the sensitive preamplifiers. Hewlett-Packard type HFBR2406 and HFBR1402 fiber optic transmitters and receivers provide an adequate signal to noise ratio of 30db @30m.

The TAXI receiver chip (AM7969) runs a phase-locked-loop to recover the clock and performs error detection on the incoming data. If there were significant noise in the received bit stream, various single- and multiple-bit errors could occur. An analysis of the error detection algorithm within the TAXI chip shows that all single bit errors are detected and flagged while a few 2 bit errors could be missed. Adding a parity bit to all the data bytes would not help this case and after measuring the error rate for our hardware to be less than 10^{-13} it was decided to forgo any additional error detection.

IV. THE DATA RECEIVER

Xilinx 3000-family Programmable Logic Cell Arrays (LCAs) are used throughout the data handling system to perform glue logic and state machine functions. The LCA that handles the data as it comes out of the TAXI receiver chip is one example. The sequence of operations is synchronized by decoding the beginning of event command word. Pairs of bytes are combined to form 16-bit words. A pedestal value taken from a local RAM is subtracted. Pedestal RAM has been loaded with (120pads x 256samples =) 30,720 appropriate values. The pedestal-corrected value is compared with a programmable digital threshold while it is being written into an output buffer. This comparison is used to update a hit-pattern array. The LCA also generates the addresses for the output buffer such that the data is reorganized into a logical sequence for subsequent processing by a DSP. The housekeeping data is also placed in a convenient area of memory. A counter in the LCA will flag the event as overrun if an end-of-event command word is not received over the TAXI link.

V. THE UP LINK

A reliable data path is required to load configuration tables and the diagnostic event RAM on each of the detector-mounted boards. The configuration tables include bits to control the test pulser built into each of the 120 preamplifiers, a field to set the number of time samples to record, and mode bits to force various event types such as diagnostic, pulser, or real data. The industry standard "Bitbus" offers a high degree of data integrity as an off-the-shelf product with internal firmware providing all protocol for network management and error detection and correction. An AMD type 8044BEM chip (and LCA) is located on each detector board; 4 networks of 32 nodes each are controlled by Bitbus Master VME modules. The data rate is a modest 20KBytes/s but this is quite sufficient to reconfigure the entire detector and load all diagnostic RAMs in under two minutes.

ACKNOWLEDGEMENTS

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[1] "A TPC Detector for the Study of High Multiplicity Heavy Ion Collisions", G. Rai, et.al., IEEE Trans. Nucl. Sci. Vol. 37, No.2, pp 56-64, April 1990

[2] "A 4096 Cell Switched Capacitor Analog Waveform Storage Integrated Circuit", S. A. Kleinfelder, IEEE Trans. Nucl. Sci.. Vol. 37, No.3, pp 1230-1236, June 1990

[3] AMD TAXI information package including data booklet #07370 and Technical Manual #12330C from AMD Literature Dept. (408) 732-2400

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