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IRVINE

Analog and Mixed-Signal Circuit Design for Internet of Things Applications

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Electrical Engineering

by

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Professor Guann-Pyng Li
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2018

DEDICATION

To my inspiring wife, my lovely family, and the memory of my father.

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ABSTRACT OF THE DISSERTATION

Analog and Mixed-Signal Circuit Design for Internet of Things Applications

By

Mohammad Radfar

Doctor of Philosophy in Electrical Engineering

University of California, Irvine, 2018

Professor Michael M. Green, Chair

Recent growth in applications related to the Internet of Things, has introduced new challenges to the design of integrated circuits. Accuracy of sensors, power consumption, speed, and sensitivity to internal and external noise sources are some of the challenges addressed in this dissertation.

A delta-sigma circuit architecture is designed to measure resistance with an accuracy of $\pm$ 1% over a range of four orders of magnitude. This performance is verified through both analog and mixed-signal simulation and chip measurement.

A novel compensation technique is developed and simulated to reduce the supply sensitivity of an LC oscillator. An improvement of 85% is verified based on simulations of jitter and frequency variation.

A new architecture is proposed for design of oscillators, based on a double-ladder periodic structure, whose behavior is less sensitive to the output termination resistance as compared to conventional oscillators. The advantages of the designed oscillator is verified compared to conventional LC and single-ladder structure oscillators. The design is optimized based on phase noise and power consumption.

Chapter 1

Introduction

With a market of nearly $157B in 2016 [1] for the Internet of Things (IoT), as well as with expected growth in the sensor and RFIC industries for related applications, there is an urgent need for new analog and mixed-mode circuit methodologies. Optimizing 31 billion devices operating in IoT systems in 2020 [2] certainly requires hardware design improvement to control the cost and the efficiency of these systems. Furthermore, IoT system expansions have required much more accurate and reliable sensing and communications circuits. In addition to the design complexity, power consumption plays an important role in IoT system scalability and maintenance costs. This issue has been researched at the system level [3] and [4], but any improvement at the circuit design level would directly affect the cost. In addition, fully monolothic implementations lead to less off-chip elements and hence, cost reduction. Removing elements such as off-chip capacitors, on the other hand, may increase the circuit sensitivity to the external interferences such as supply noise. Therefore, new techniques can render the device communications more reliable and sensors more accurate. Given this motivation, the work described in this dissertation describes novel techniques enabling measurement of the conductance of

materials using a second-order delta-sigma modulation system. The system design is followed by a stability analysis customized for the designed delta-sigma system. The circuit design implementation used new techniques to measure the conductance/resistance over a range of four orders of magnitude. The performance has been verified by the chip measurements. Furthermore, a novel compensation technique is proposed to reduce the LC oscillator's supply sensitivity. This method is shown to decrease the supply noise, resulting a reduction of jitter by 85-87% as compared to conventional designs. This has been achieved by studying the sensitivity of both the common-mode and the differential-mode aspects of the oscillation and then compensating both sensitivity mechanisms through an adaptive loop that adjusts the tail current appropriately. In the path to present new techniques to improve oscillator performance, a novel oscillator architecture is proposed using double-ladder Degenerate Band Edge periodic architectures (DBE). The oscillator is designed using conventional active elements; however, the DBE periodic structure is used as the resonator. The oscillator has proven to provide very small phase noise. A low-impedance termination can be driven directly with no required buffer, making this architecture more power efficient compare to conventional LC oscillators.

Chapter 2

Conductance Sensor Design Using Current Measurement Delta-Sigma Systems

Sensing circuits have a critical role in control systems, automobile and robotics. As Internet of Things networks are growing, more sensing applications are being introduced and new design techniques are needed to enhance the accuracy of the sensors, increasing the measurement range, and reducing the power consumption. In this chapter, a current measurement approach using a second-order delta-sigma system is introduced to sense conductance/resistance in a wide range from 1 nS to 10 μS (1 GΩ to 100 kΩ). The idea is analyzed at both the behavioral and transistor levels. The design is implemented in the XH035 XFAB 350nm process. The measurement results proves stability and less than $\pm$1% error after performing a two-point calibration.

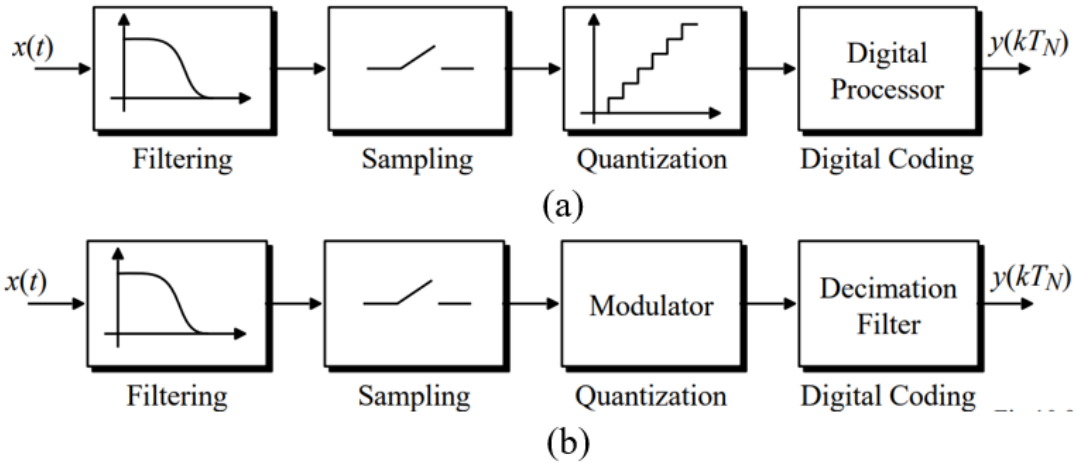


Figure 2.1: System block diagram of (a) Nyquist sampling and (b) over-sampling modulator [7].

2.1 Oversampling Systems Review

Analog-to-Digital Converters (ADCs) can be generally categorized as either Nyquist [5]-[6] or oversampling [7]-[8] data converters. As opposed to Nyquist-rate converters, oversampling uses a much higher sampling rate compared to the analog signal bandwidth. Nyquist sampling has the drawbacks of being vulnerable to noise and degradation of accuracy at higher resolutions. Among different types of oversampling converters architectures, Delta-Sigma ADCs are widely common in integrated circuit design. Fig. 2.1 compares the block diagrams of Nyquist and oversampling systems. Delta-sigma modulators are one of the oversampling data converters types with the ability to shape the noise spectrum due to the chain of integrators in their loops. Fig. 2.2 shows an Nth-order delta-sigma system, where N is the number of integrators in the modulator path.

As the output vs. the quantizer noise transfer function adds the factor of $(1\text{-}z^{-1})$ for integrator in the discrete-time domain, the noise transfer function of a delta-sigma modulator

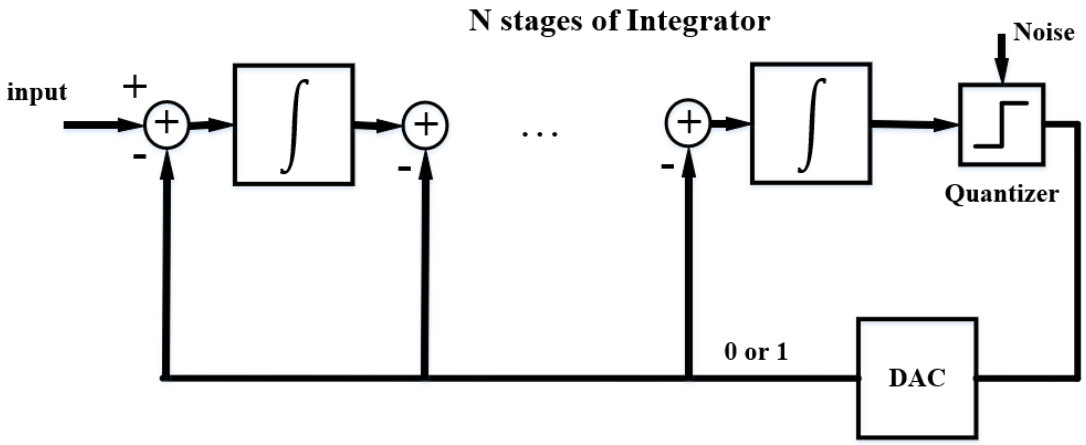


Figure 2.2: A general Nth order delta-sigma modulator.

Nth order can be written as [9]:

$$NTF(f) = (1 - z^{-1})^N \tag{2.1}$$

Therefore, the magnitude of the noise spectrum will be:

$$\mid NTF(f) \mid = \mid (1 - z^{-1})^N \mid = \mid (1 - e^{-j\omega/f_s})^N \mid = (2sin(\pi f/f_s))^N \tag{2.2}$$

where f_s is the sampling frequency, and $z = e^{j\omega/f_s}$. Fig. 2.3 shows this function for a first- and second-order delta-sigma with oversampling ratio f/f_s from 0 to $f_s/2$. The noise shaping at lower frequencies makes a delta-sigma system the proper choice for small resolution analog-to-digital converter applications. As described in detail in the next sections, the proposed system implements a second-order delta-sigma modulator to sample the charges accumulated as a result of electric current flow.

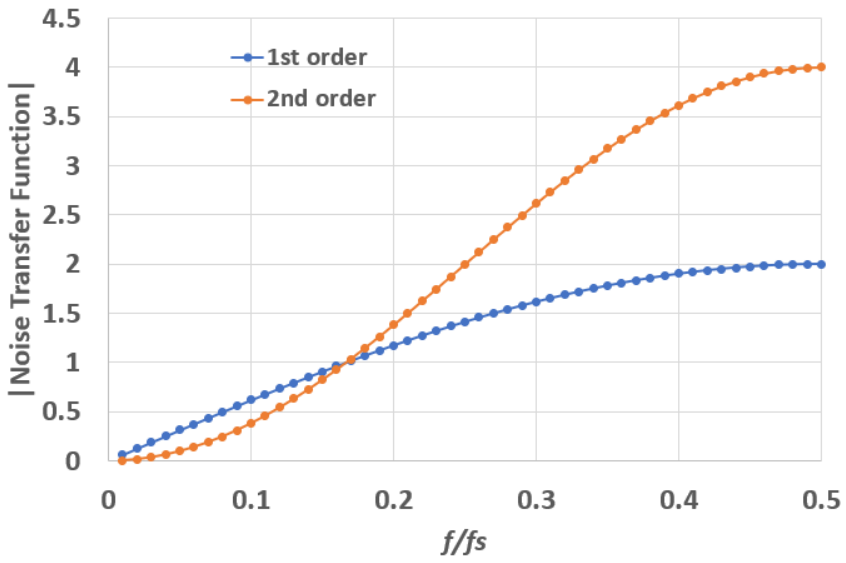


Figure 2.3: Quantization noise transfer function shaping in first- and second-order delta-sigma modulators.

2.2 Delta-Sigma Architecture for Current/Conductance Measurement

The idea of delta-sigma oversampling is applied in this project to precisely measure the average current. Using the proposed approach the conductance of certain materials can be measured. In this method, it is essential to draw current/charge from the material whose conductance, G_x is to be measured. This can be achieved by connecting one terminal to a known voltage source, V_s and the other terminal to a the delta-sigma feedback loop that keeps the terminal voltage close to the ground. This concept is illustrated in Fig. 2.4 where the generated current and charge can be written as:

$$I_x = V_s \cdot G_x \tag{2.3}$$

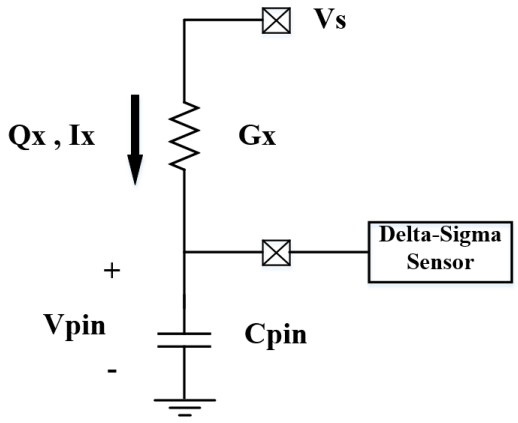


Figure 2.4: Generating current proportional to the conductance and a measure the current with a delta-sigma modulator.

$$Q_x = I_x \cdot T_{meas} = V_s \cdot G_x \cdot T_{meas} \tag{2.4}$$

where the T_{meas} is the measurement time and is a large number of clock period. With the delta-sigma closed-loop circuit keeping the average value of V_{pin} approximately 0 by discharging C_{pin} and calculating the total amount of charge drawn during the measurement, the total charge and current injected the pin and hence, the unknown conductance can be calculated.

Such a delta-sigma loop is modeled as a discrete-time system as shown in Fig. 2.5(a), where Q_x is the unknown input charge (flowing through the unknown resistance), out[n] is the output of the comparator at each clock cycle, Q_{ref} is the reference charge, and Q_{pin} = Q_x - out[n].Q_{ref}. This second-order system uses two integrators in the feedforward path together with the feedback mechanisms. The gain and feedback factor will be determined by design and described later.

The realization of Fig. 2.5(a) is shown in the Fig. 2.5(b) block diagram. The first integrator

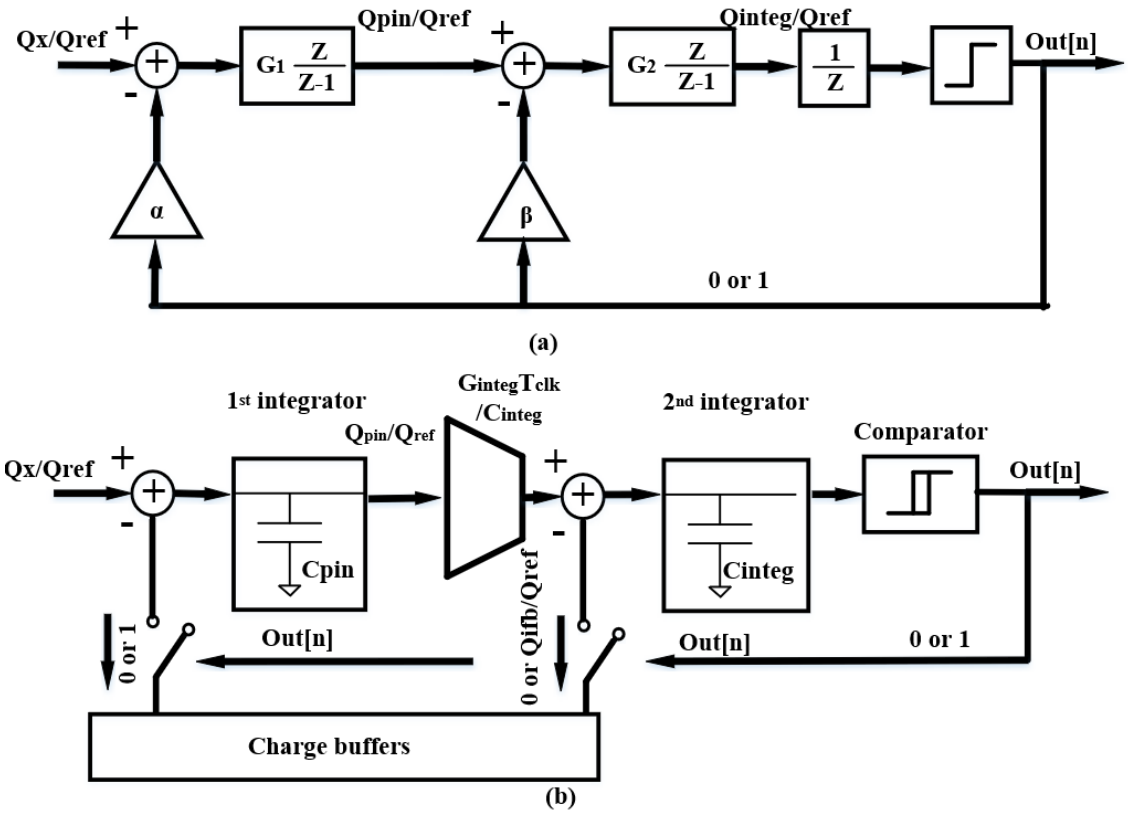


Figure 2.5: (a) Customized second-order delta-sigma system block diagram, (b) circuit implementation block diagram.

is implemented by the large off-chip capacitor C_{pin} to collect the charges proportional to the current that is conducted from the unknown material. The second integrator, implemented on chip is designed to integrate the voltage V_{pin} at the sensing pin. During each clock cycle, the integrator accumulates the charge of $G_{integ}T_{clk}V_{pin}$, where G_{integ} is the integrator transconductance gain, T_{clk} is the clock period. This charge will be seen across capacitance C_{integ}. Therefore the gains indicated in Fig. 2.5(a) can be written as G_1=$G_{integ}T_{clk}/C_{pin}$ and G_2=1. The output of the second integrator is digitized by a clocked comparator. Q_{ref} and Q_{ifb} are the amounts of charge drawn from C_{pin} and C_{integ} respectively when the comparator output Out[n] is 1. Thus feedback factor α and β in Fig. 2.5(a) are 1 and Q_{ifb}/Q_{ref}, respectively, as all the charges are normalized by the reference charge. If the delta-sigma loop is stable (which will be evaluated in the following sections) the average voltage V_{pin} will be close to 0 V in the steady state. By the end of the measurement, a total charge of NQ_{ref} discharged from C_{pin}, where Q_{ref} is the reference charge in the feedback loop and N is the number of times this amount of reference charge discharged during the measurement. Considering the fact that the average voltage (charge) is zero at the end of the measurement, NQ_{ref} should be equal to the total charge that is injected to the sensing pin's capacitor by the unknown current I_x. Since Q_{ref} is a known reference charge, the current and hence the conductance/resistance can be calculated through the following formulas:

$$Q_x = N \cdot Q_{ref} \tag{2.5}$$

$$I_x = \frac{N \cdot Q_{ref}}{T_{meas}} \tag{2.6}$$

$$G_x = \frac{N \cdot Q_{ref}}{T_{meas} \cdot V_s} \tag{2.7}$$

where T_{meas} is the measurement time and V_s is the voltage source used to generated fixed current through unknown conductance as shown in Fig. 2.4(b).

2.2.1 Circuit Blocks and Timing

To implement such a discrete-time system into the circuit design, a switched-capacitor system is presented in Fig. 2.6, which operates in two phases. During phase Φ_1, the charge-sharing part of the sensor is disconnected from the pin, while the reference capacitor (C_{ref}) is charged to $Q_{refhi} \equiv C_{ref} \cdot V_{refhi}$ where V_{refhi} is a voltage level that is defined as a fraction of the supply voltage. At the same time, the integrator is constantly accumulating the pin voltage at the output based on the integrator gain. When the integrator output becomes higher than the comparator input reference, the clocked comparator output goes high and hence the delta-sigma system invokes phase Φ_2. In this phase, the reference (charge) buffer charges up the reference capacitor to $Q_{reflo} = C_{ref} \cdot V_{reflo}$ (where $V_{reflo} < V_{refhi}$). This eventually leads to transferring $Q_{ref} = C_{ref} \cdot (V_{refhi} - V_{reflo})$ from C_{pin} to C_{ref}. V_{refhi} - V_{reflo} is designed to be adjusted from 100 mV to 600 mV. The digital controller once again invokes Φ_1 after half a clock cycle. At the end of measurement window, the total discharged charge from the pin (NQ_{ref}) will be equal to the total charge driven from and hence the unknown current and conductance can be determined from (2.5) to (2.7).

2.2.2 System Design Parameters

The measurement range determines the reference values and oversampling speed. In this current sensor design, 1 nS to 10 μS conductance (equivalent to 1 GΩ to 100 kΩ, respectively) is targeted as the desired conductance range. Assuming that a 35V external source is available, the current range can be calculated to be between 35nA to 350μA. With an off-chip capacitor C_{pin} at the pin acting as the integrator of the current, the maximum charge accumulation is 350 pC/μsec. Assuming a system clock rate of 8 MHz, this charge accumulation rate will be 43.7 pC/cycle. It is a necessary condition that Q_{ref} be larger than the maximum accumulated charge per cycle in order to keep the loop converged. For this purpose, the maximum values of V_{ref} and C_{ref} are selected to be 600 mV and 80 pF, respectively. This is enough to sense 48 pC/cycle, which is equivalent to 384 μA current conducted into the sensing pin. In the minimum current case, Q_{ref} should be much smaller than the total charge accumulated during the entire measurement time in order to provide enough resolution. In the 35nA case where the charge increasing rate is only 4.3 fC/cycle (i.e., 34.4 pC total charge in 1 ms measurement time), minimum values of 300 mV and 2.5 pF are chosen for V_{ref} and C_{ref}, respectively, to generate the reference charge of 750 fC. This proved the resolution on 750fC / 34.4 pC = 2.2% in the small current measurement. The reference buffer gain, integrator bandwidth, and inner feedback gain affect only the accuracy and the stability and will be discussed in the next sections.

2.2.3 MATLAB Model

A discrete-time model is developed for the proposed delta-sigma system to analyze the system behavior and the stability. Through two phases of the timing diagram, the sensing

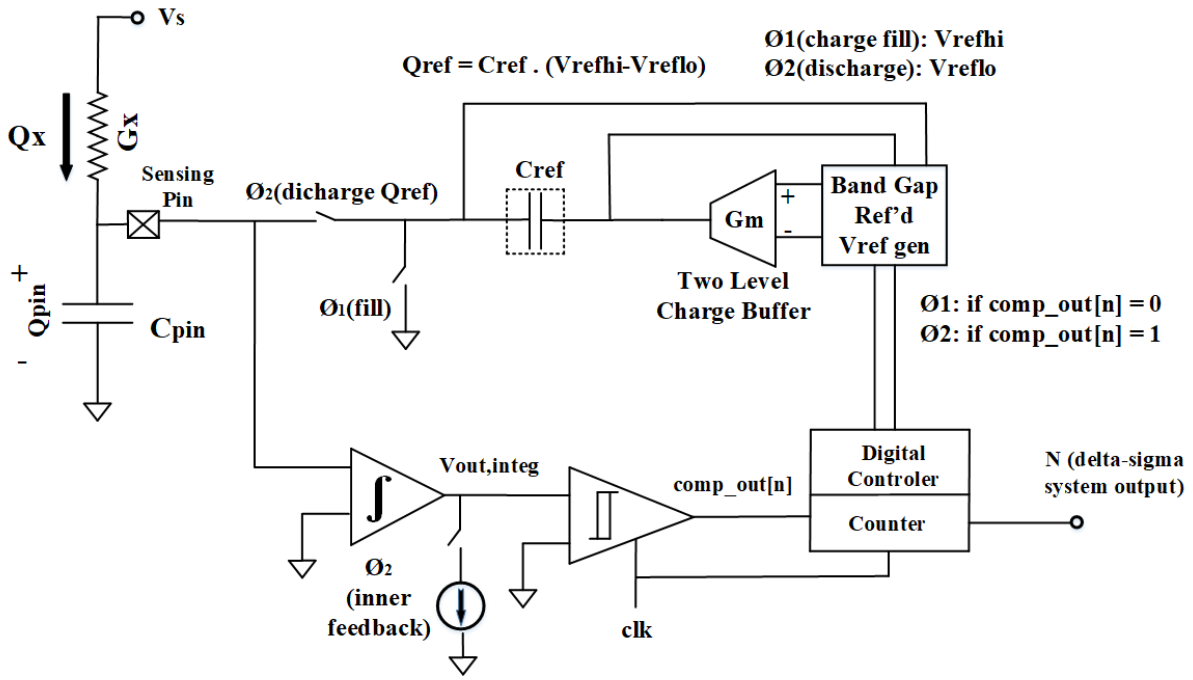


Figure 2.6: Switched cap delta-sigma system architecture.

pin charge $Q_{pin} = C_{pin}V_{pin}$ and integrator's output voltage $V_{out,integ}$ are updated twice each clock period. This MATLAB model includes the effects of constant leakage at the output pin together with the effect of parasitic capacitance in the circuit.

The transient waveforms of V_{pin}, $V_{out,integ}$, and $out[n]$ are presented in Fig. 2.7 for 35 nA measurement. The amount of charge transferred during phase Φ_2 of each clock period is equal to Q_{ref}. The inner feedback factor Q_{ifb}/Q_{ref} is also used to makes the loop stable as described in more details in the next section.

At the other end of the range, the 350 μA measurement case is also simulated through the system model. Fig. 2.8 indicates the stable delta-sigma loop signals at the sensing pin together with integrator output and comparator decision at each clock period.

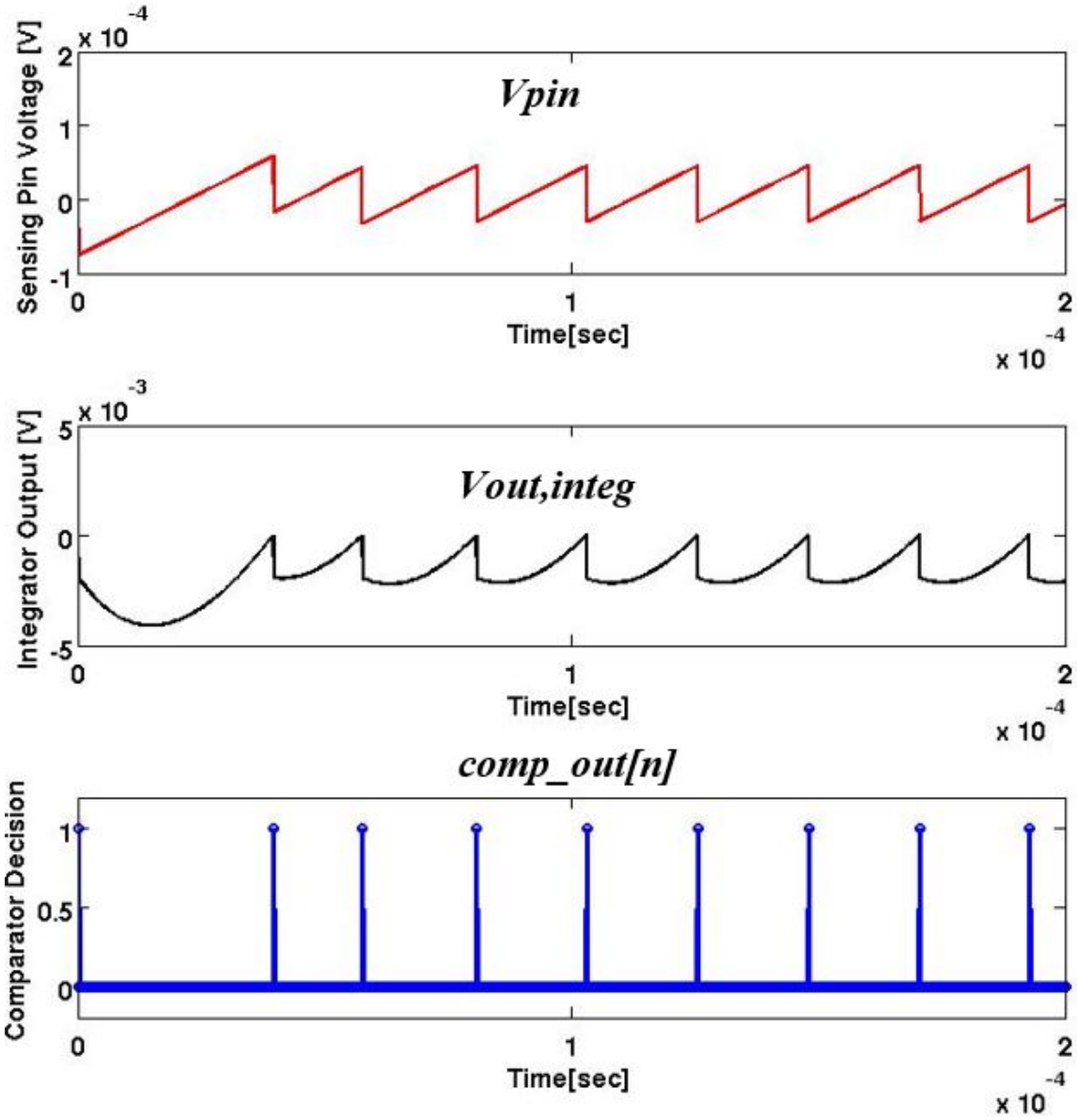


Figure 2.7: MATLAB model simulation delta-sigma loop signals during 200 μsec of 35 nA current measurement.

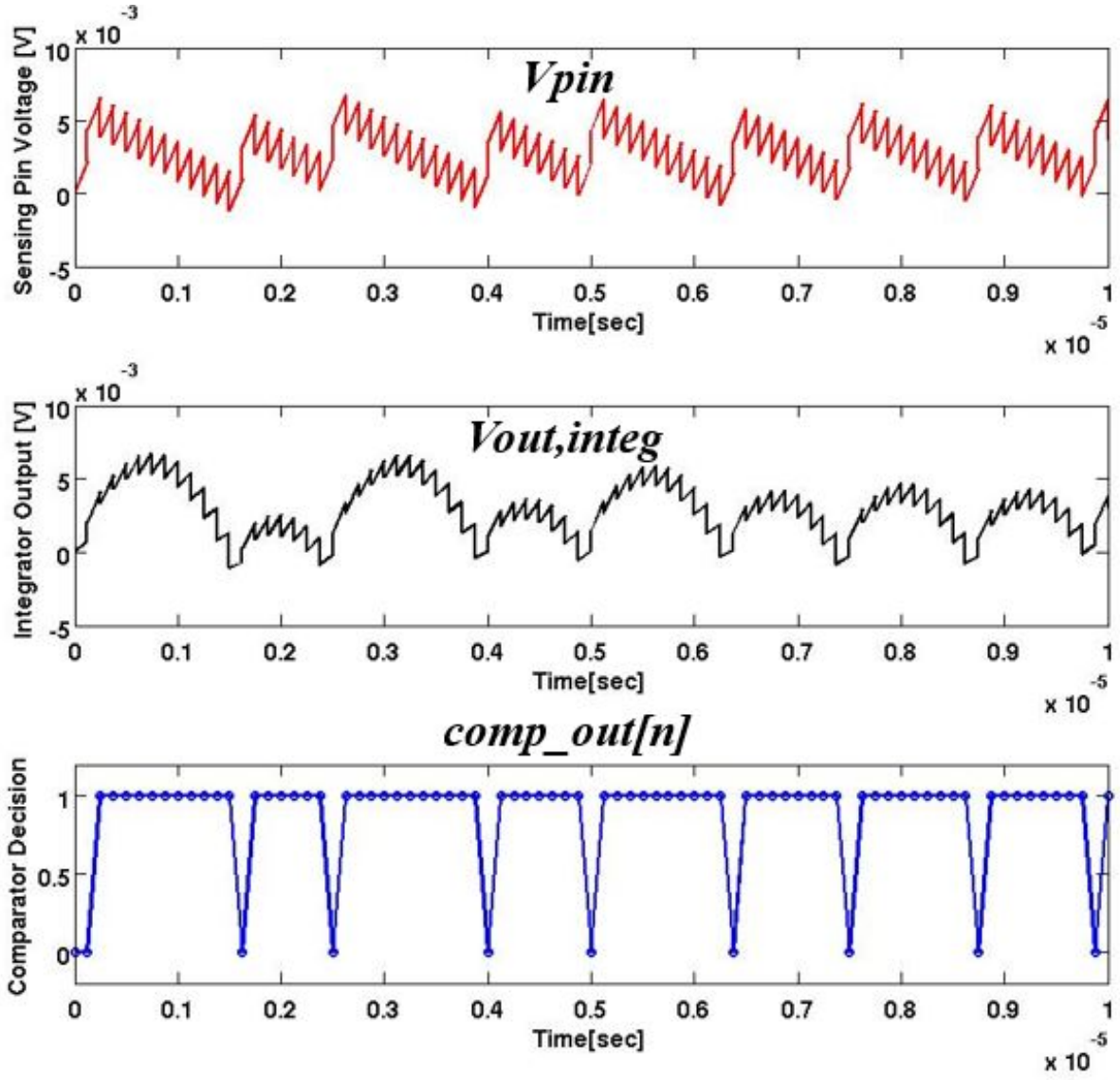


Figure 2.8: MATLAB model simulation delta-sigma loop signals during 10 μsec of 350μA current measurement.

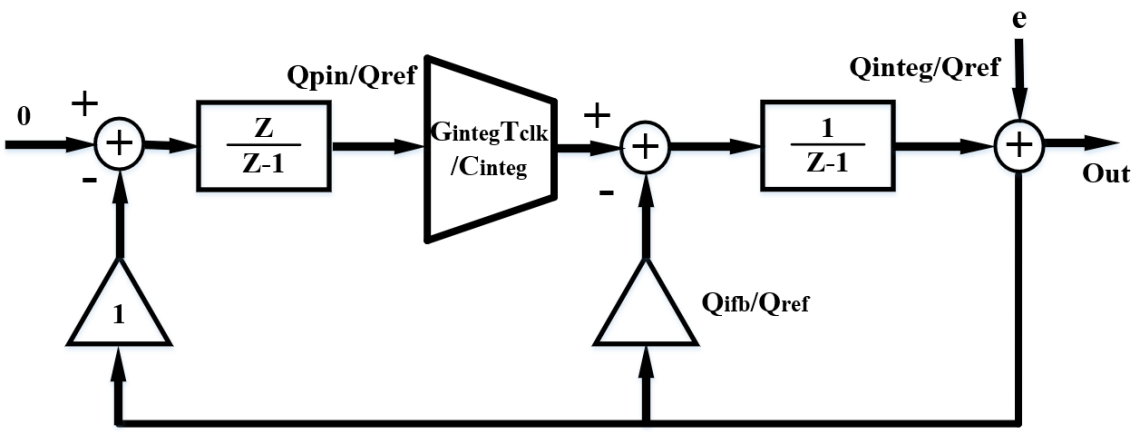


Figure 2.9: Noise transfer function block diagram model using describing function method [11].

2.2.4 Loop Stability

As pointed out in the previous sections the proposed second-order delta-sigma system has some stability considerations. Pole and zero formulation for such a modulator is non-trivial due to the nonlinearity of the quantizer (comparator) at the end of the feed-forward path of Fig. 2.5(a). However, using the describing function method proposed in [11], a noise transfer function can be developed applying the method, leading to a block diagram in Fig. 2.9 which is the same as system block diagram Fig. 2.5 except the noise source e is used to model the quantization noise from the comparator.

In the case where amount of charge drawn from the pin (outer-loop feedback) is the only feedback mechanism i.e., $Q_{ifb} = 0$, the loop can become unstable due the two integrators used in the feed forward path, 180° at any frequency. Analyzing the Fig. 2.9 block diagram, we have: .

$$Out(z) = e - \frac{z}{(z-1)^2}(G_{integ}T_{clk}/C_{pin})Out(z) \tag{2.8}$$

Thus the noise transfer function (NTF) [11, 8] can be written as:

$$H(z) = \frac{Out}{e} = \frac{(z-1)^2}{z^2 + (-2+k)z + 1} \tag{2.9}$$

where $k \equiv (G_{integ}T_{clk})$ / C_{pin}, which is known as the total loop gain. Plotting the pole magnitudes versus k as shown in Fig. 2.10(a) indicates that one of the poles always has magnitude greater than or equal to 1. Adding an inner-loop feedback mechanism by drawing charges from the comparator output shown in Fig. 2.5(a) will change the second-order noise transfer function to:

$$H(z) = \frac{(z-1)^2}{z^2 + (-2 + Q_{ifb}/Q_{ref} + k)z + (1 - Q_{ifb}/Q_{ref})} \tag{2.10}$$

where the ratio Q_{ifb}/Q_{ref} can be adjusted to render the poles in the stable region. This is used as the solution to solve the stability issue formulated in (2.9). Fig. 2.10(b) shows that the pole magnitudes corresponding to $G_{integ} = 80$ μS and $C_{integ} = 16$ pF, $C_{pin} = 10$ nF, $T_{clk} = 125$ ns, and $Q_{ref} = 40$ pC for different values of Q_{ifb}. Both pole magnitudes are moved below 1 for non zero values of Q_{ifb}.

Fig. 2.11 shows the instability in the time domain with the inner-loop feedback does not exist. As suggested in the original block diagram, inner loop feedback can be added by drawing charges at the integrator output. In the circuit design, the mentioned inner feedback is implemented using a switched current source steering circuit shown as a part of system architecture in Fig. 2.6. The transient behavior gets back to a stable situation with an appropriately designed inner-loop feedback as already presented in Fig. 2.7.

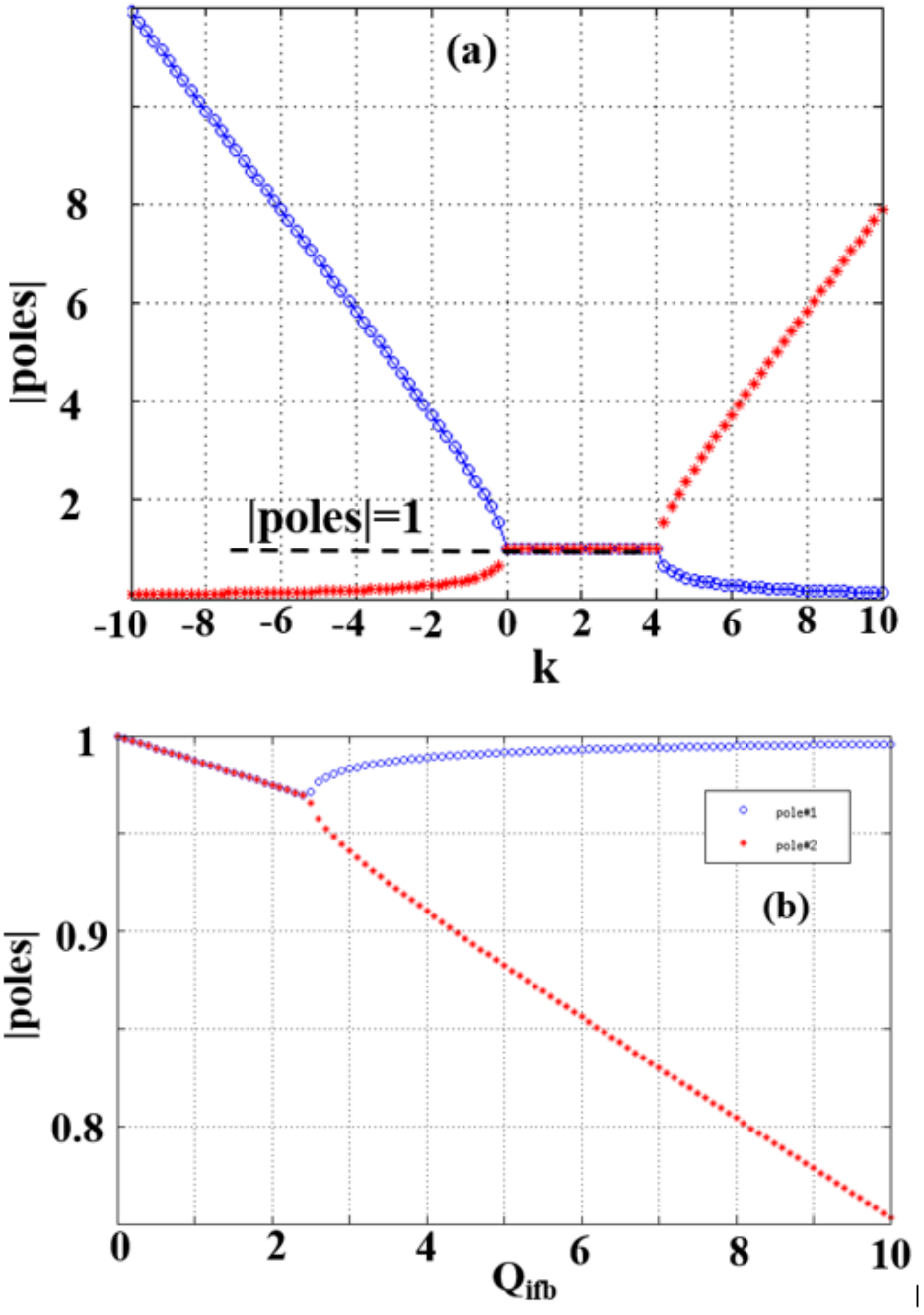


Figure 2.10: Pole magnitudes of the noise transfer function (a) without inner-loop feedback (b) with inner-loop feedback.

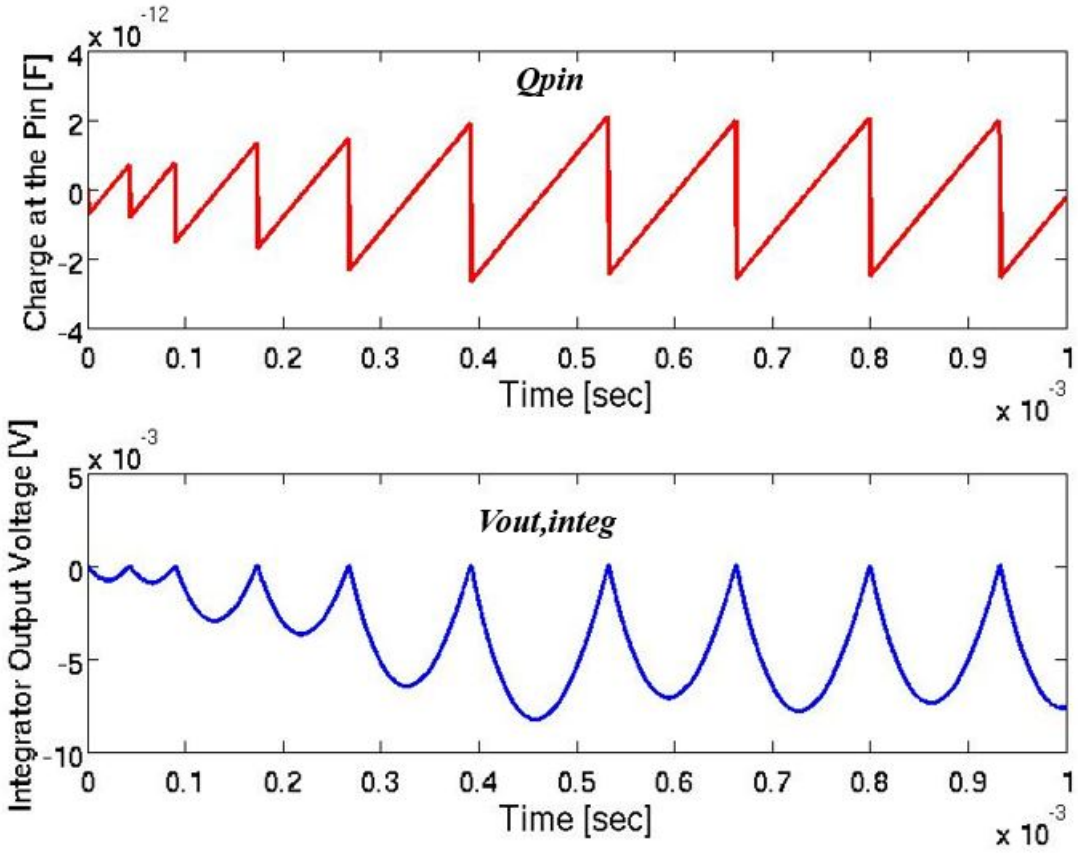


Figure 2.11: Instability issue without inner loop feedback in the system model.

2.2.5 Error and Accuracy Analysis

As described earlier, the total amount of charge is measured during a fixed amount of time, allowing evaluation of the total current and thus conductance value. Here are the analysis of error types that could affect the accuracy of this measurement.

Quantization Error / Resolution

The quantization error of this system will be the minimum unit reference charge that the buffer can draw from the sensing pin over the total measurement time. In other words, since the number of discharged reference charges is the output of the measurement, the ratio of unit charge to the measurement window time itself can be considered as the quantization error - i.e.:

$$\Delta I = \frac{C_{ref} \cdot V_{ref}}{T_{meas}} \tag{2.11}$$

Offset Error

Any leakage current or constant charge that is extracted from the sensing pin and not related to the measured current will contribute as an offset error. In this sensor problem, the offset is mainly created by the leakage in the ESD and/or off-chip elements. As the leakage becomes more significant compared to the lower currents, this value will limit the minimum measurable conductance.

Gain Error

Gain error can be one of the main sources of inaccuracy in the delta-sigma data converter. Referring to (2.7) any variation in the numerator and denominator parameters can contribute to the gain error, whose maximum value can be formulated as:

$$\text{Gain Error} = |\frac{\Delta G_x}{G_x}| = |\frac{\Delta C_{ref}}{C_{ref}}| + |\frac{\Delta V_{ref}}{V_{ref}}| + |\frac{\Delta T_{meas}}{T_{meas}}| + |\frac{\Delta V_s}{V_s}| \tag{2.12}$$

Among the four terms mentioned in (2.12), ΔV_{ref} can be minimized by using a bandgap-referenced current source and ΔT_{meas} can be minimized by generating the clock from a precise source such as a crystal oscillator. The error in V_s is relevant to the noise of external voltage source or buffer error, which is beyond the scope of this dissertation. The relative error of C_{ref} however, plays a significant role in the method's accuracy. The capacitance variations over the process corners are normally around $\pm 15\%$. This requires that each individual chip to have a two-point calibration to evaluate the value of C_{ref}. This can be done by simply measuring two different current values with the same setting and extract the gain and offset error. After the calibration, the remaining non-idealities will be mainly temperature variation and nonlinearity. Although temperature variation error is negligible in many applications, since the C_{ref} vs. T characteristic is monotonic and varies less than 0.6% as indicated in Fig. 2.12, this error can be reduced by an order of magnitude using a PTAT (Proportional To Absolute Temperature)-based temperature sensor results while the chip is operating.

Nonlinearity

The nonlinearity normally results from mismatch in the capacitor bank. In this type of delta-sigma system, the worst-case performance can be evaluated by comparing the

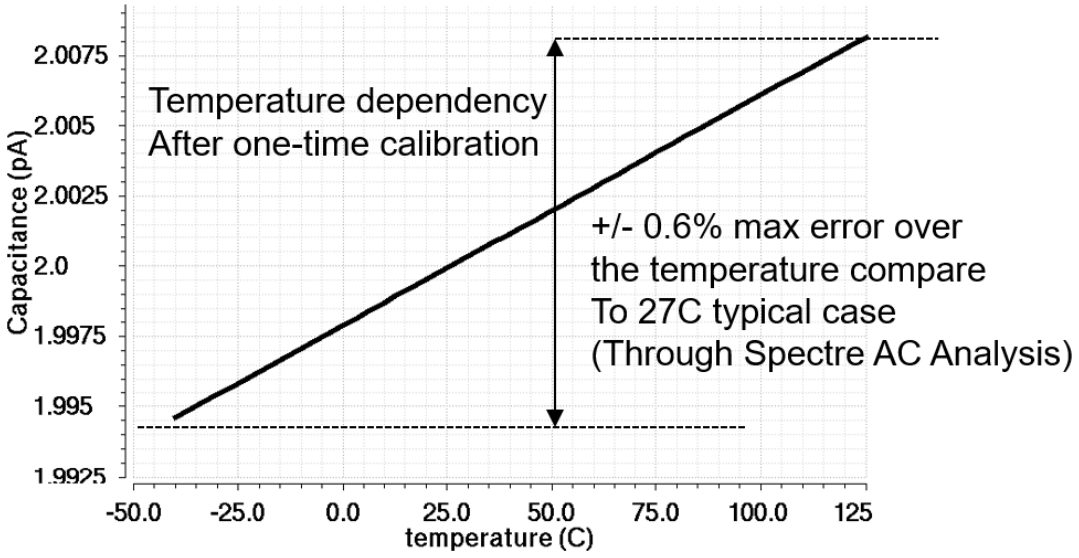


Figure 2.12: Reference CMIM capacitor dependency over temperature.

maximum capacitance mismatch relative to the minimum capacitor, which defines 1 LSB of C_{ref}. This way the standard deviation of each unit capacitance is $\sigma_{Cmax}=\frac{A}{\sqrt{W.L}}$, where W and L are the width and length of the unit capacitor and A is the mismatch factor per square root of capacitor area. In this case the worst-case mismatch for 64 unit cap of 1.25pF can be determined as $\sigma_{Cmax,total}= 64\ \sigma_{Cmax} \sim 80$ fF in this design. This variation is much less than the 1.25 pF unit cap, ruling out the effect of nonlinearity to dominate the quantization error.

2.2.6 Inner-loop feedback and Accuracy Trade-off

As described in the stability analysis, the inner-loop feedback is required for system stability. However, applying the feedback through drawing charges from the integrator output, introduces non-zero average voltage at the integrator input. This average voltage V_{ave} results in conductance measurement error. Assuming the delta-sigma system properly measures the input current I_x from the voltage source V_s in Fig. 2.4, the error can be

estimated as:

$$R_x - R_{calc} = \frac{V_s}{I_x} - \frac{V_s - V_{ave}}{I_x} = \frac{V_{ave}}{I_x} \tag{2.13}$$

In order to evaluate the average sensing pin average offset, first the average number of inner-loop feedback discharges, which is the same as the reference charge feedback, must be calculated. As the delta-sigma loop keeps the average charge at the sensing pin near zero, the amount of current integrated between each applied feedback is approximately equal to the reference charge $Q_{ref} = \int_{t_0}^{t_0+T_{fb}} I_x dt$. Therefore, the time in between each feedback discharge can be expressed as:

$$T_{fb} = \frac{Q_{ref}}{I_x} \tag{2.14}$$

Considering that the integrator input will reach an average offset to compensate for the average charge drawn from the integrator output, we can write:

$$\frac{Q_{ifb}}{T_{fb}} = G_{integ} V_{ave} \tag{2.15}$$

Combining (2.14) and (2.15) the non-zero average voltage at the sensing pin caused by

the inner-loop feedback mechanism can be formulated as:

$$V_{ave} = \frac{Q_{ifb} I_x}{G_{integ} Q_{ref}} \tag{2.16}$$

Fig. 2.13(a) shows how the circuit converges to different average pin voltages for different values of Q_{ifb} in 350 μA measurement using the MATLAB system model (assuming other system parameters are constant). The average voltage calculated from (2.16) is also verified with the system model simulation results. Applying (2.13)-(2.16) to the system design parameters, the resulting relative error is plotted vs. Q_{ifb} and G_x in Fig. 2.13(b), indicating that the value of Q_{ifb} can limit the accuracy improvement for high conductance (low resistance) measurement applications.

2.3 Circuit Implementation

each block has been realized following the system-level characterization. The details of each circuit architecture and performance characteristics are provided in the following sections. The feed-forward path contains the integrator and the comparator. The main feedback block includes the reference buffer and switched capacitor array together with a voltage-to-current reference generator. The inner-loop feedback is implemented using a current-steering technique.

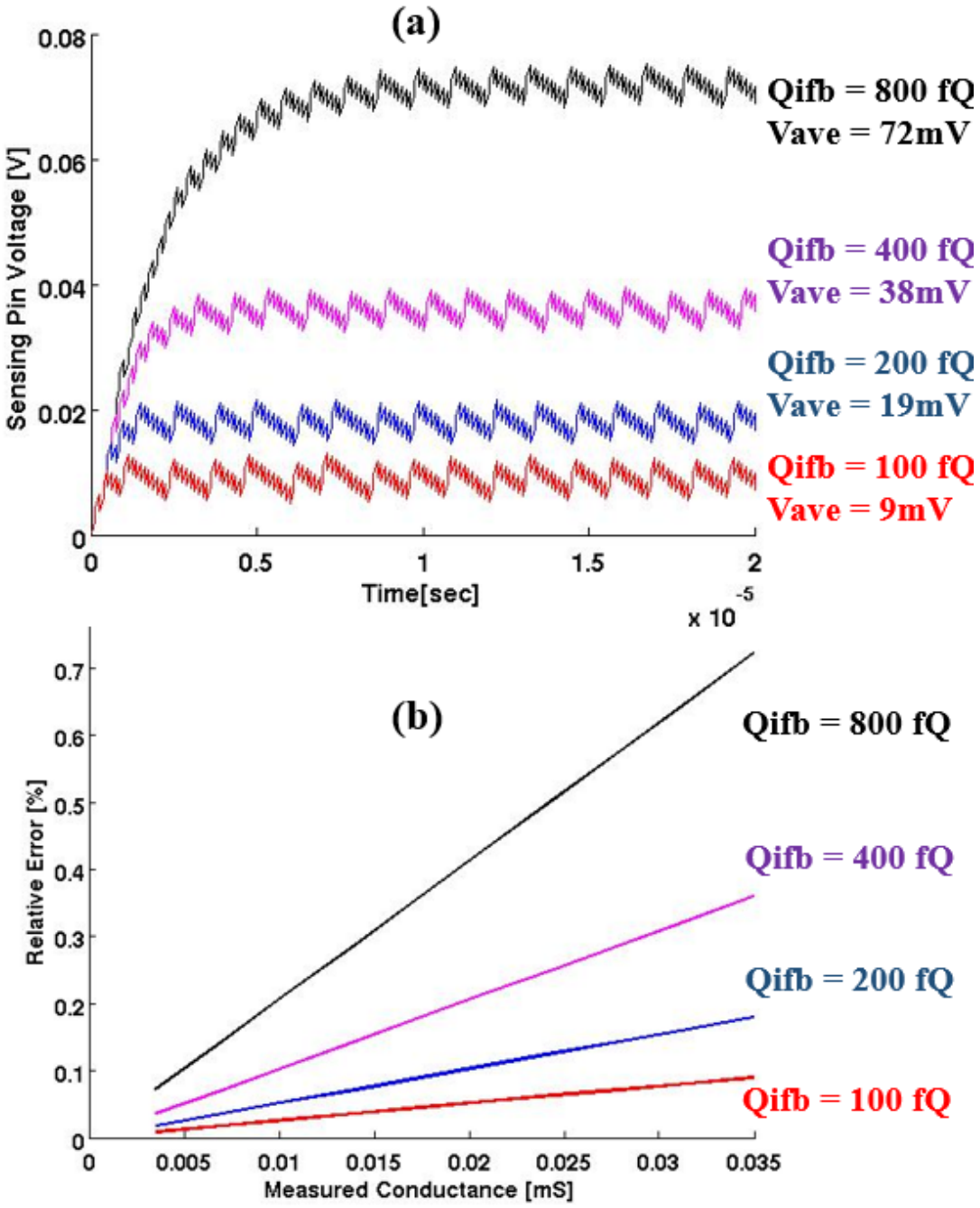


Figure 2.13: (a) Inner-loop feedback effect on sensing pin average voltage; (b) relative Error vs. inner-loop feedback and the measured conductance.

2.3.1 Reference Charge Buffer and Switched Capacitor

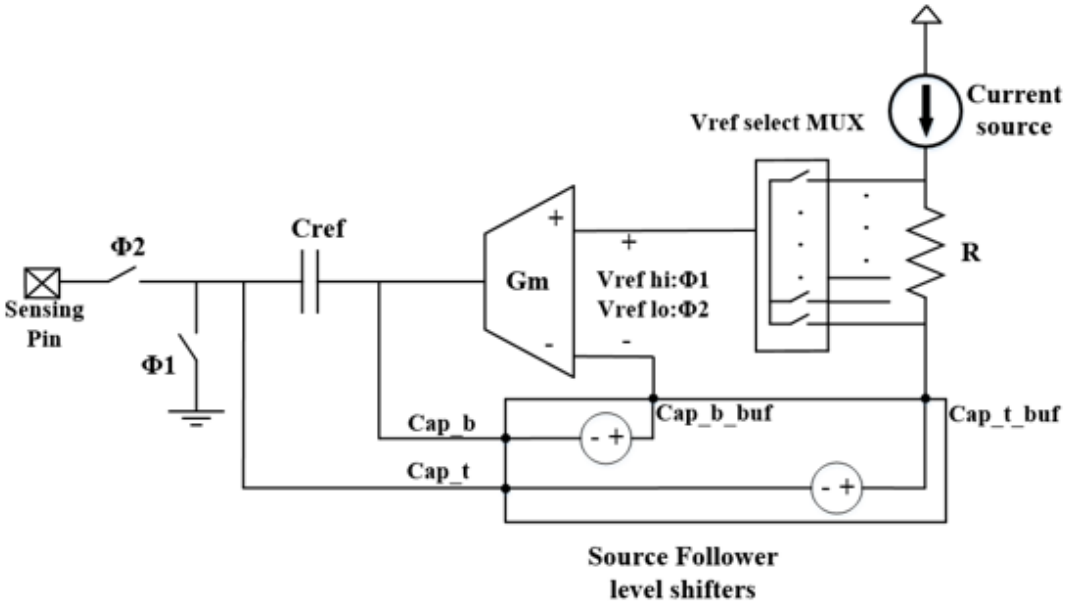
The reference charge buffer is the most critical block in the proposed delta-sigma system from the point of view of measurement accuracy and the feasible clock speed. The task of charging and discharging the reference capacitor bank between V_{refhi} and V_{reflo} should be completed within half of an 8 MHz clock cycle (62.5 ns). The reference buffer consists of a transconductance cell that provides a sufficiently linear transconductance over the desired input and output levels. The minimum required transconductance can be determined by $G_m/C_{ref} > n \cdot T_{clk}/2 = n{\cdot}62.5$ ns where the number of time constants, n, can be between 5 to 7 to provide a gain error of less than 1%. The phase margin of the reference buffer loop is also an important specification. Such a reference buffer topology is shown in Fig. 2.14(a). The reference voltage levels are generated by a voltage generation branch discussed in the next section. Two reference voltage levels V_{refhi} and V_{reflo} are selected using a multiplexer and applied to the transconductance at the beginning of in each phase. The difference V_{refhi} - V_{reflo} provides the V_{ref} for the reference charge Q_{ref}=$C_{ref}V_{ref}$. The transconductance is responsible for setting the required differential output voltage on the reference capacitor. As the top plate of the reference capacitor is connected to the sensing pin and required to be close to 0 V, voltage level shifting is required to provide input voltages within the transconductance input range as illustrated in Fig. 2.14(b). The transconductance is designed as shown in Fig. 2.15(a). It consists of an input transconductance stage followed by a second stage current-unlimited transconductance. The first stage itself is implemented using NMOS input pair folded cascode as shown in Fig. 2.15(b). This requires a common-mode input of higher than 1.2V. Switching between two input voltage levels, the differential output reference offset depends on the gain of the first stage G_m. Therefore, the output resistance of the current sources is maximized, allowing less than 1% offset error on V_{ref}. This is shown in Fig. 2.16 where the input offset is guaranteed for the V_{ref} range of 700 mV, slightly exceeding the

design target from the system-level analysis. This allows the input reference voltage to be switched between 1.7 V and 2.4 V during the two clock phases. The pole realized by the first-stage is at a relatively low frequency due to the high output resistance realized to reduce the input offset. All the other pole frequencies must be sufficiently high in order to meet the stability requirement. The current-unlimited second-stage architecture allows an increase of the transconductance in the output at the expense of increasing the channel width and current consumption, thereby increasing the frequency of the non-dominant pole corresponding to the output. Implementing this design approach, the AC loop analysis of the reference buffer is shown in Fig. 2.17. The dominant pole is at 50 kHz in the typical case, while the non-dominant poles are pushed to higher than 80 MHz. The design results in 58° phase margin in typical corner, varying between 50° to 67° over the process, temperature and voltage corners to guarantee the stability. The resulting gain bandwidth product (GBWP) of approximately 22 MHz meets the settling time requirement of 62.5 ns. The transient waveform of the reference buffer output shown in Fig. 2.18 shows an amplitude of V_{ref} = 600 mV, which ensures the complete transition in both delta-sigma phases.

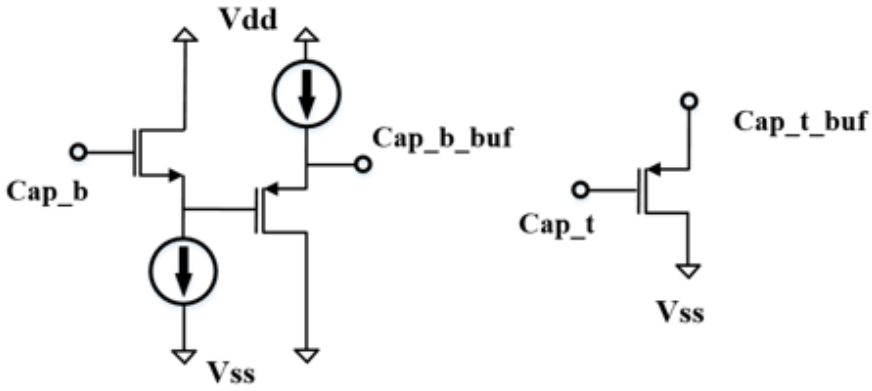
2.3.2 Referenced current source

In order to produce an accurate differential reference voltage with low variation over the process, temperature and supply voltage, a voltage-to-current (V2I) circuit is designed.

As shown in Fig. 2.19, the architecture contains a negative feedback transconductance cell loop to buffer the 1.2V input $V_{bandgap}$. This input voltage is conventionally implemented using a bandgap voltage circuit. Bandgap circuits often use well-defined quantities of bipolar junction transistors to provide positive and negative temperature coefficient [14]-[16]. A stable reference voltage is generated by canceling the various temperature coefficients.



(a)



(b)

Figure 2.14: Reference charge buffer architecture.

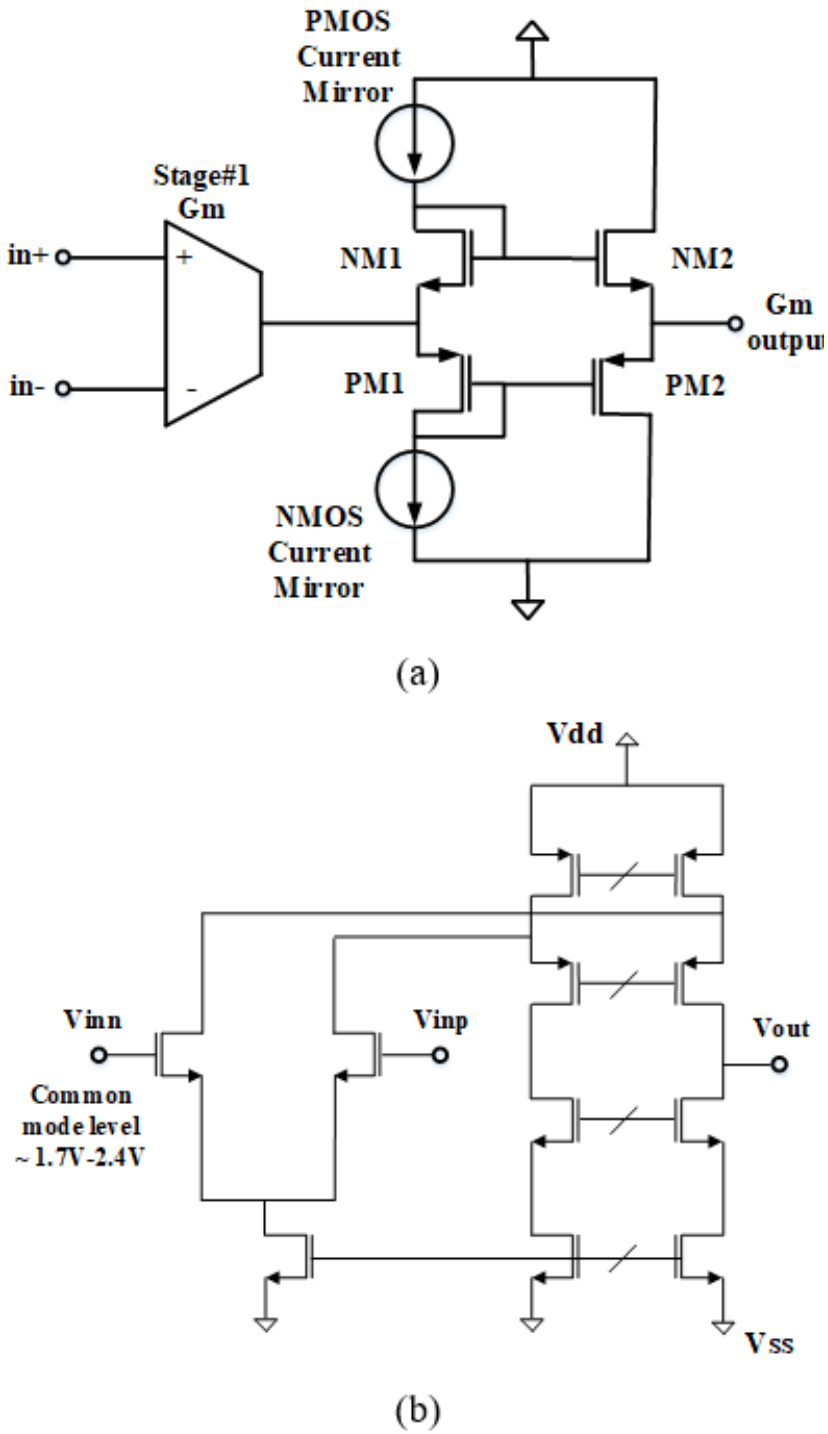


Figure 2.15: Reference charge buffer output transconductance architecture (a) the two-stage current-unlimited output (b) first-stage folded-cascode transconductor.

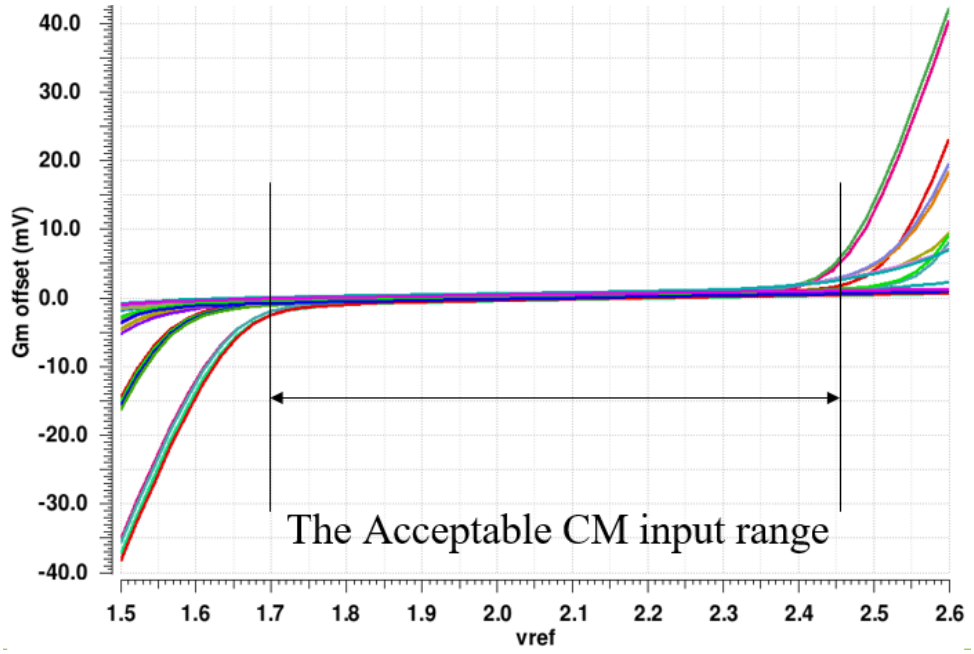


Figure 2.16: Reference charge buffer offset vs. the input reference voltage range.

The output I_{bias} is used to generate a current conducted into the reference resistor R_{ref}. This current can be mirrored by different branches to pass the expected current values to the same type of resistors that are matched with the reference. As temperature and process vary, the resistance value changes; however, since the input reference voltage is always kept at 1.2V, the reference voltage generated over the same type of the matched resistors will be constant. Using cascode current sources, 0.75% accuracy over PVT corners can be reached. The V2I circuit has to provide small variation over the mismatch as well to ensure the performance in the chip production. Using current source sizing and maximum V_{dsat} considering the available headroom, σ of the reference voltage variation is pushed to below 0.11% as verified by the Monte Carlo simulations indicated in Fig. 2.20.

The stability of the V2I loop needs to be assured as well. As adding more current mirrors decreases the Gm output pole frequency, the series resistor R_z as shown in Fig. 2.19 is employed to add a left half-plane zero to improve the stability. Considering that the gate capacitances of the current mirror transistors is around 20 pF, $R_z = 1.8$ kΩ was chosen

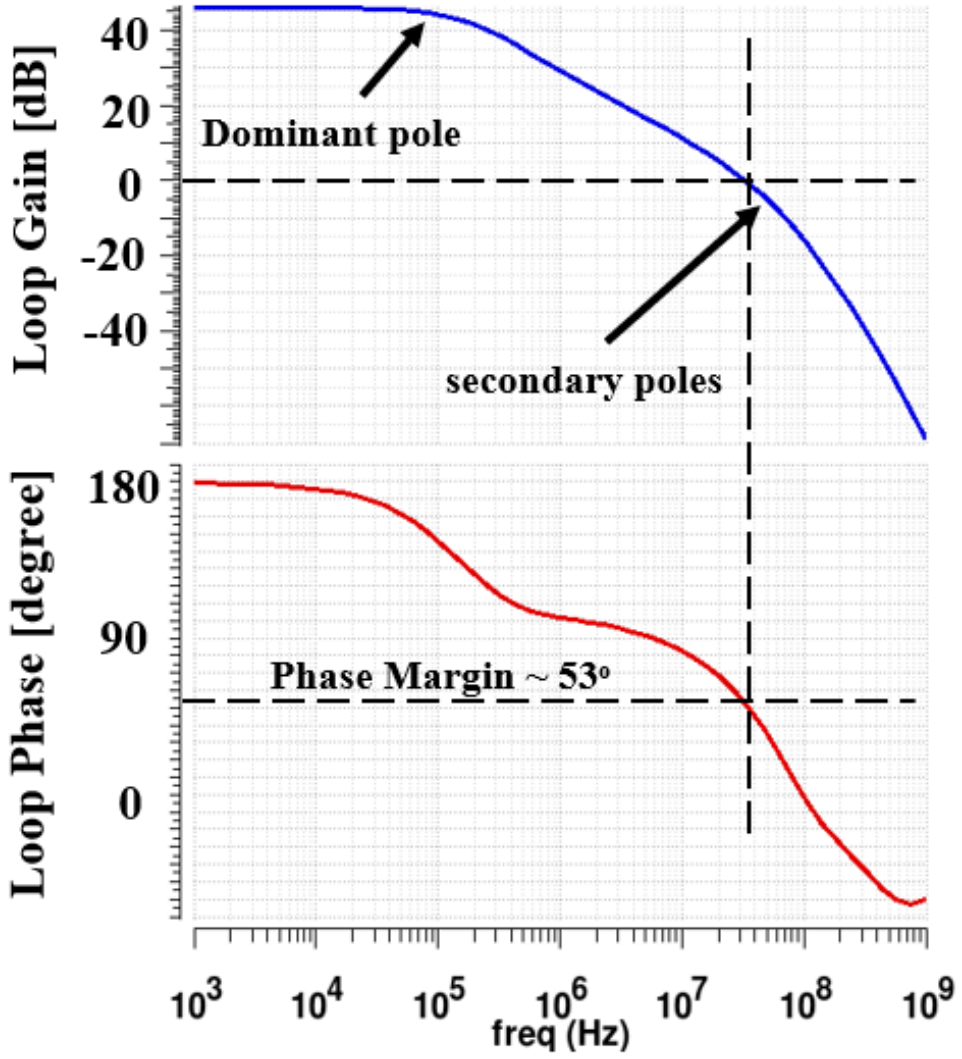


Figure 2.17: Reference charge buffer stability analysis.

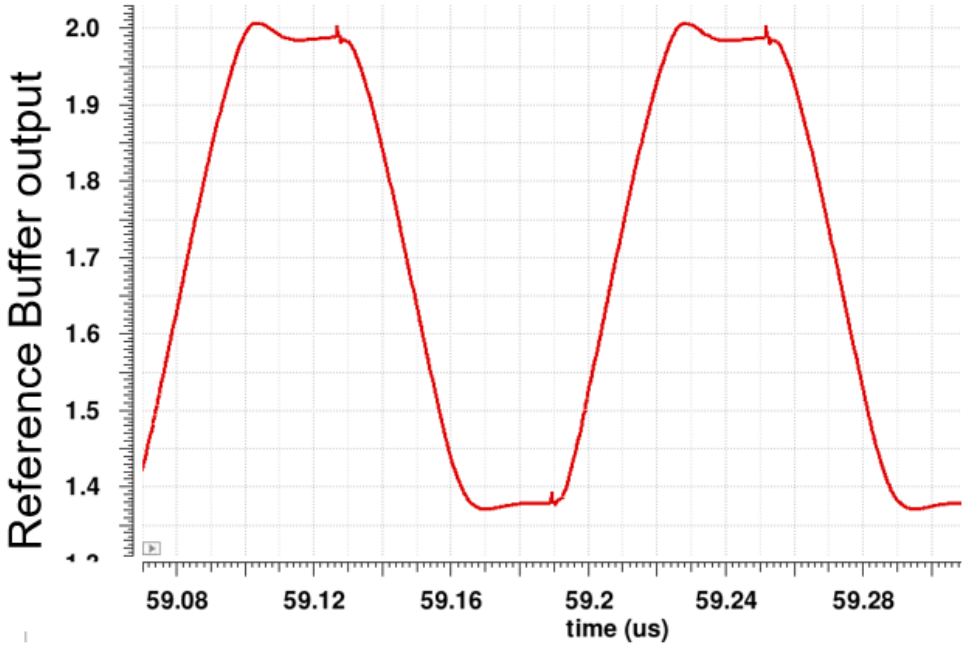


Figure 2.18: Transient settling in both delta-sigma phases.

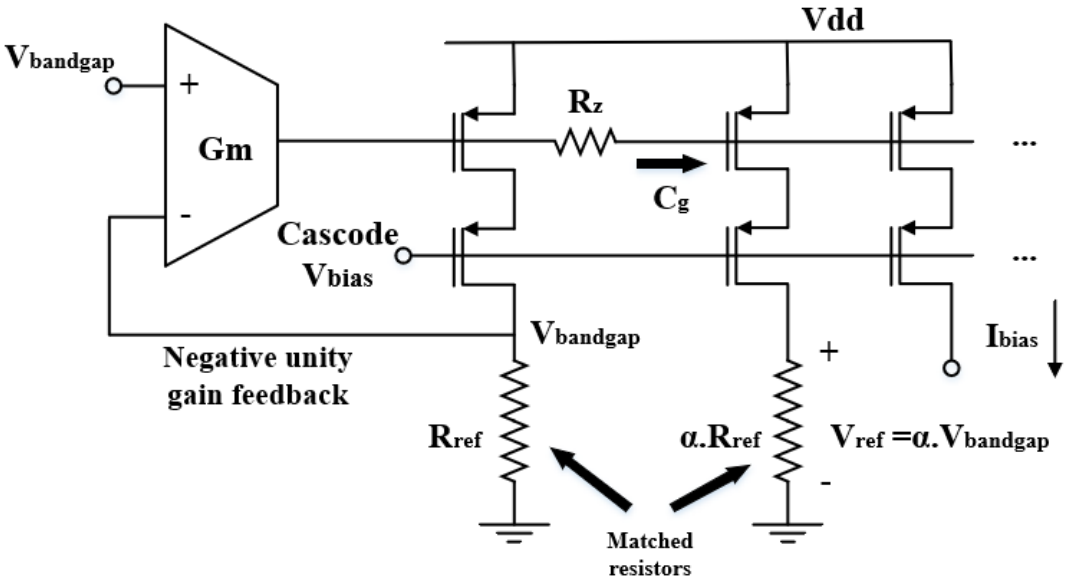


Figure 2.19: V2I architecture.

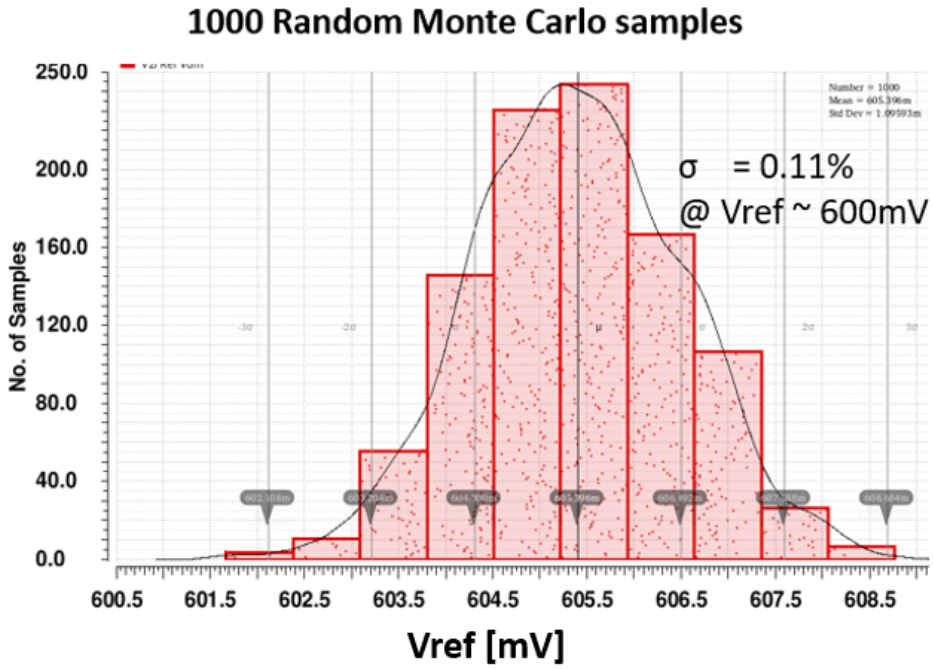


Figure 2.20: V2I mismatch analysis using Monte Carlo simulation.

to have set the zero near 3 MHz. This effect can be verified through stability analysis presented in Fig. 2.21, assuring phase margin of 85° or more over the corners, as illustrated in Fig. 2.22.

2.3.3 Clocked Comparator

An 8 MHz clocked comparator is designed using the Fig. 2.23 architecture. The pre-amplifing stage is implemented by a folded-cascode opamp with a small-signal gain of 30-40dB as shown in Fig. 2.24. The amplified analog signals are digitized by clocked comparator, realized by a the cross-coupled latch, in the next stage. The SR latch in the final stage maintains the comparator decision at the output at the end of each clock cycle. The timing diagram is indicated in Fig. 2.25. In the "load" phase, the analog input will be differentially amplified. The latch will take over during "compare" phase and a synchronous SR latch apply the decision to the output.

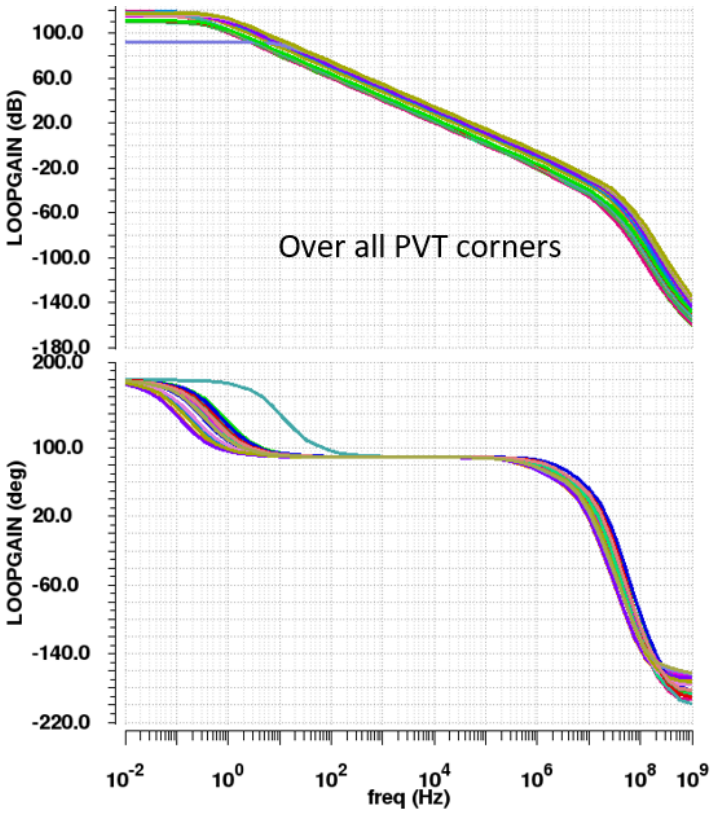


Figure 2.21: V2I loop gain and phase.

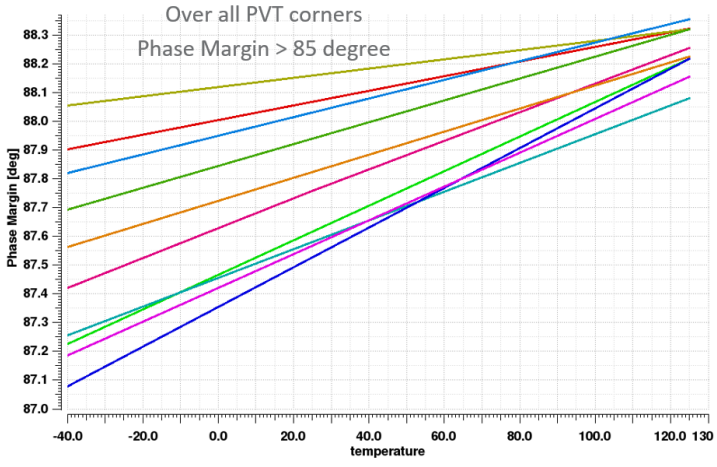


Figure 2.22: V2I loop's phase margin over PVT corner.

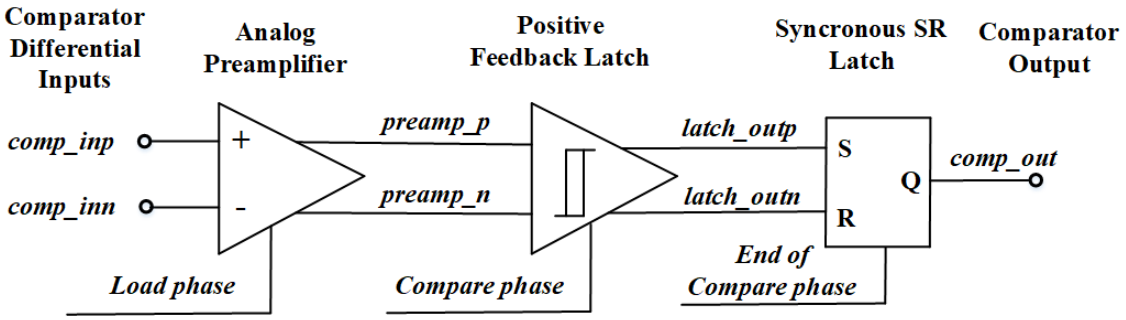


Figure 2.23: Clocked comparator architecture.

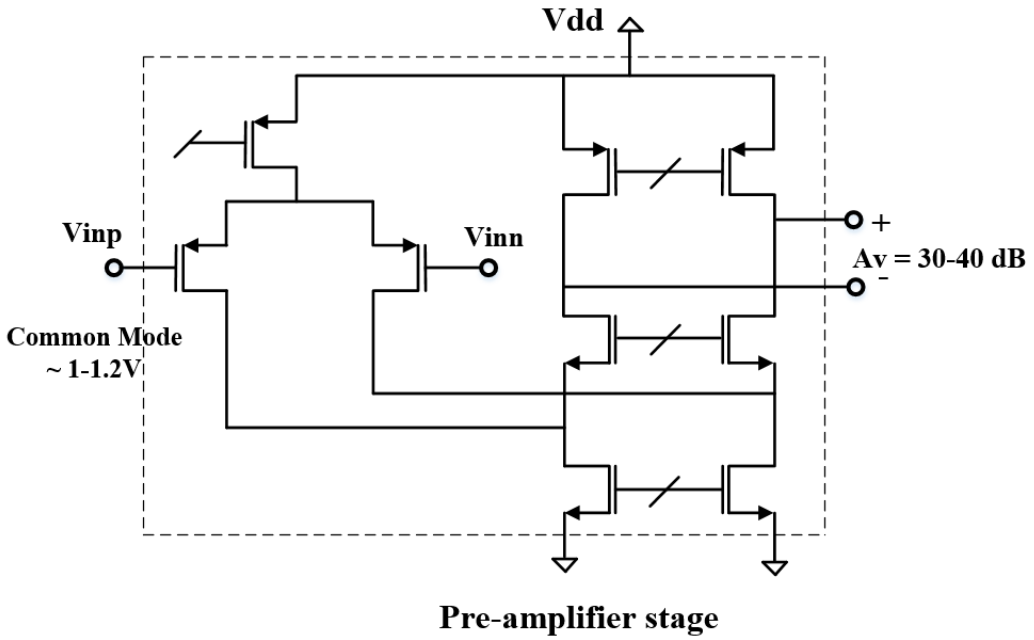


Figure 2.24: Comparator pre-amplifier topology.

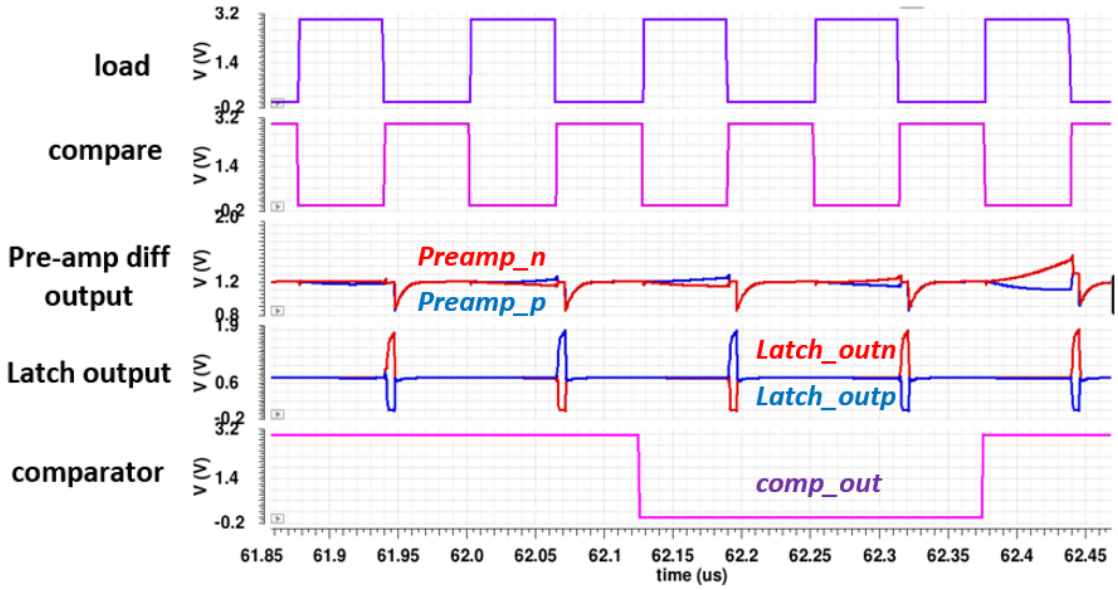


Figure 2.25: Clocked comparator timing diagram.

2.3.4 Integrator

In order to implement the integrator, the delta-sigma system uses a folded-cascode transconductance cell with a PMOS input pair to output a current proportional to the input voltage to the following capacitor as shown in Fig. 2.26. Since the inverting input of the Gm cell is connected to ground, the PMOS input pair is chosen in order to allow the transconductance to sense ground. The value of G_{integ}/C_{integ} is determined to allow at least tens of mV voltage swing at the input of the comparator in order to make sure the integrator noise and the comparator's input-referred noise do not dominate the integrator output. The maximum G_{integ}/C_{integ} is also determined by analyzing the stability analysis, since high gains in the feed-forward path can lead to instability. Based on MATLAB model analysis verified with the schematic simulations, the values of G_{integ}= 80 μS and C_{integ} = 16pF were used to satisfy this condition over the entire measuring range. The integrator frequency-domain transfer function is shown in Fig. 2.27, where a one-pole roll-off is observed over a wide range of frequency. The transconductance circuit's first non-dominant

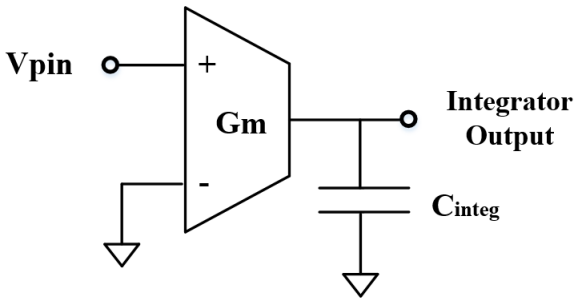


Figure 2.26: Integrator topology.

pole is at 35 MHz, which is much larger than the delta-sigma 8MHz clock speed.

The integrator output transient behavior is shown in Fig. 2.28. As illustrated in Fig. 2.26, the integrator positive input is connected to the sensing pin while the negative input is connected to the ground. At the output, the sensing pin voltage is integrated and applied to comparator input. The other comparator input is a DC voltage provided by a reference voltage generator. The comparator output will remain high as long as the sensing pin integrated voltage is higher than the reference.

2.3.5 Inner-Loop Feedback Current Steering

As discussed in the stability analysis, an inner-loop feedback is required to guarantee the stability over the entire measurement range. This feedback is implemented by discharging a certain amount of charge from the integrator output during every charge-drawing phase. As the clock frequency is constant in each measurement, drawing a certain amount of current can perform the desired discharging. In order to avoid unwanted charge sharing, a current-steering topology is implemented as shown in Fig. 2.29 where the buffer Gm architecture is presented in Fig. 2.30. The switching is controlled using non-overlapping signals generated by the SR latch. The control signals and output current drawn from the integrator output are presented in Fig. 2.31. The current-steering buffer loop stability

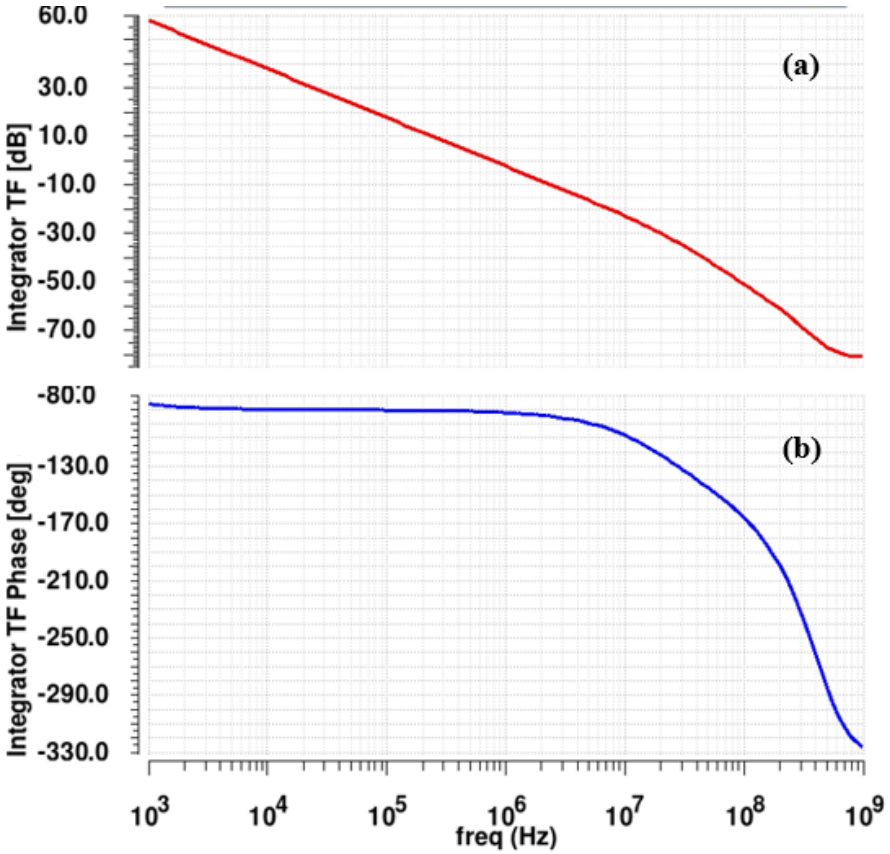


Figure 2.27: Integrator frequency domain transfer function; (a) magnitude; (b) phase.

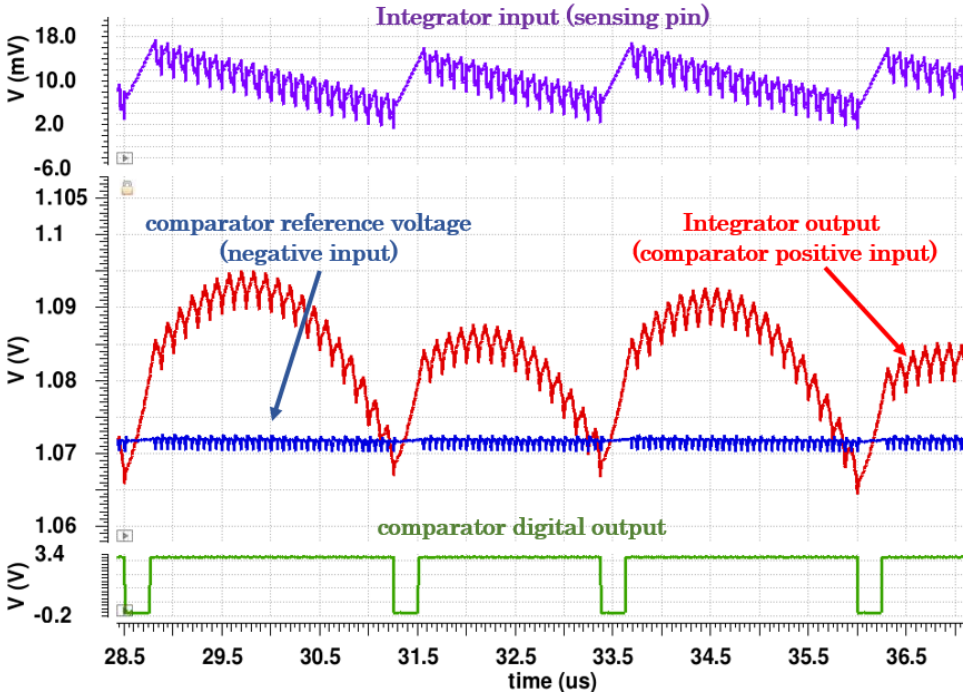


Figure 2.28: Integrator transient signals in the delta-sigma loop.

is also guaranteed by adjusting the gain and the poles in the Gm cell. The loop gain magnitude and phase values are verified over PVT corners together with the resulting phase margin in Fig. 2.32 and Fig. 2.33.

2.4 Delta-Sigma Loop Simulation Results

The delta-sigma closed-loop circuit is simulated using AMS (Analog Mixed Mode) simulations together with the digital controller. In order for the system to measure accurately, the loop has to be stable, and the main and inner-loop feedback transitions require a settling time of no more than a half clock period. In order to calculate the current value, the comparator output is measured by a counter. The counter's output i.e., the number of 1s at the comparator output, is the total number of reference charges that have been discharged from the sensing pin and plays the role of N in (2.6) and (2.7) to evaluate the

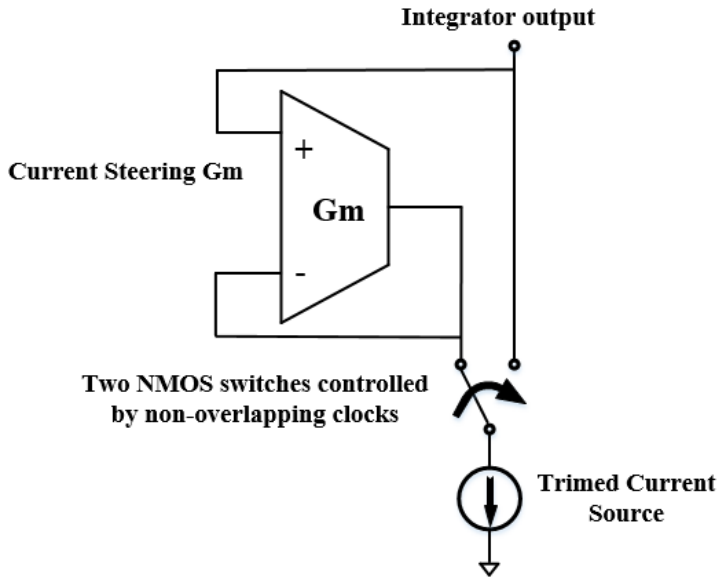


Figure 2.29: Current steering architecture for inner-loop feedback implementation.

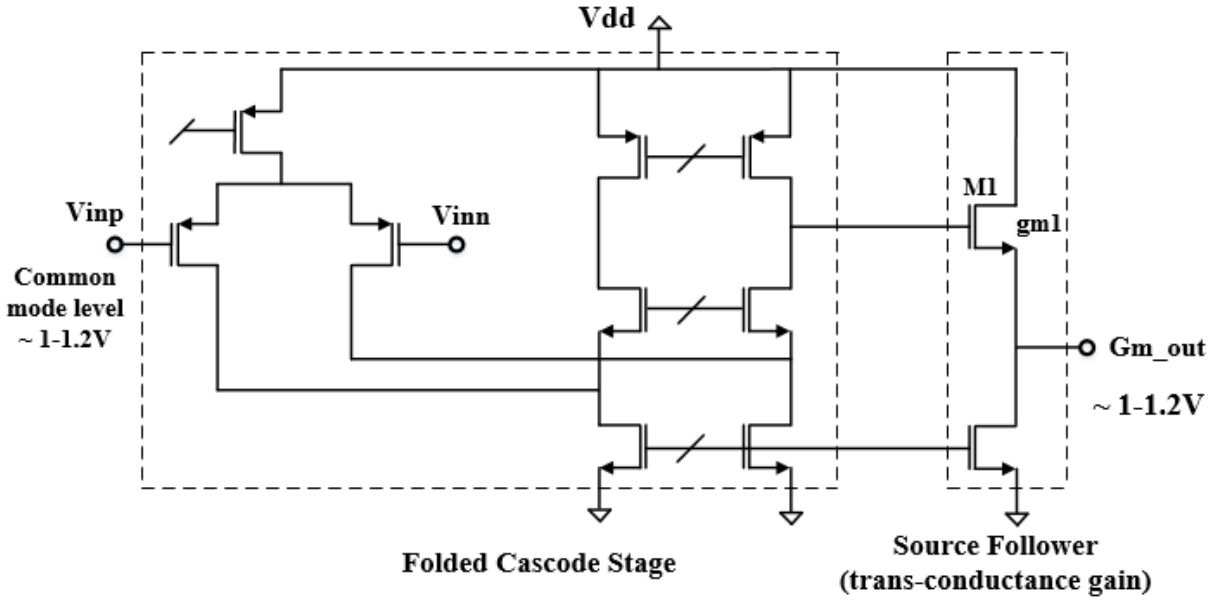


Figure 2.30: Current steering transconductance circuit.

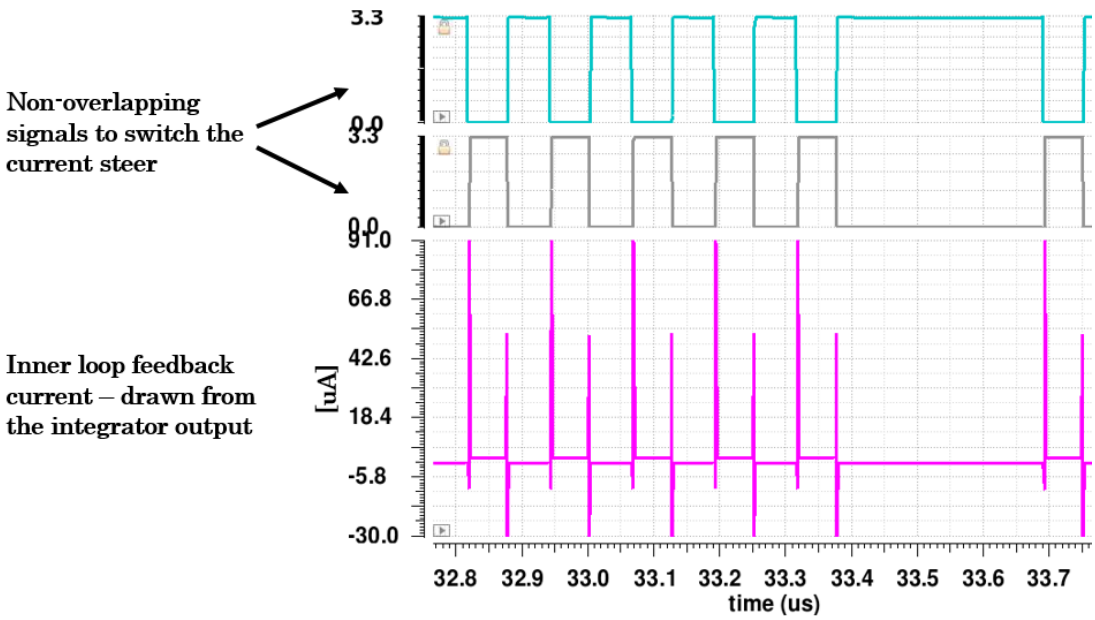


Figure 2.31: Current steering switches control signals and output current.

current or conductance.

The system is tested at both ends of the measurement range. Fig. 2.34 shows the system main waveforms while measuring 350 μA input current, where Q_{ref} = 48.7 pC (with V_{ref} = 0.6 V and C_{ref} = 81.4 pF). It shows the discharging through the reference capacitor and its effect on the sensing pin and integrator output. The phase 1 and 2 transitions are also indicated based on the comparator's decision. The number of reference charges that are discharged during the 100 μs measurement time counted as 714. Applied to (2.6), this corresponds to a measured current is I_{mease} = 714 x 48.7 pC / 100 μsec = 347.7 μA. This translates to 0.6% relative error compared to the input current of 350 μA.

For the other end of the range, 35 nA input current is sensed for 2 msec with Q_{ref} = 0.8 pC. N = 91 discharges were counted during the simulation. Using the same approach I_{mease} = 91 x 0.8 pC / 22 msec = 34.6 nA, resulting in approximately 1% relative error. The transient waveforms are shown in Fig. 2.35 for a simulation time of 60 μs.

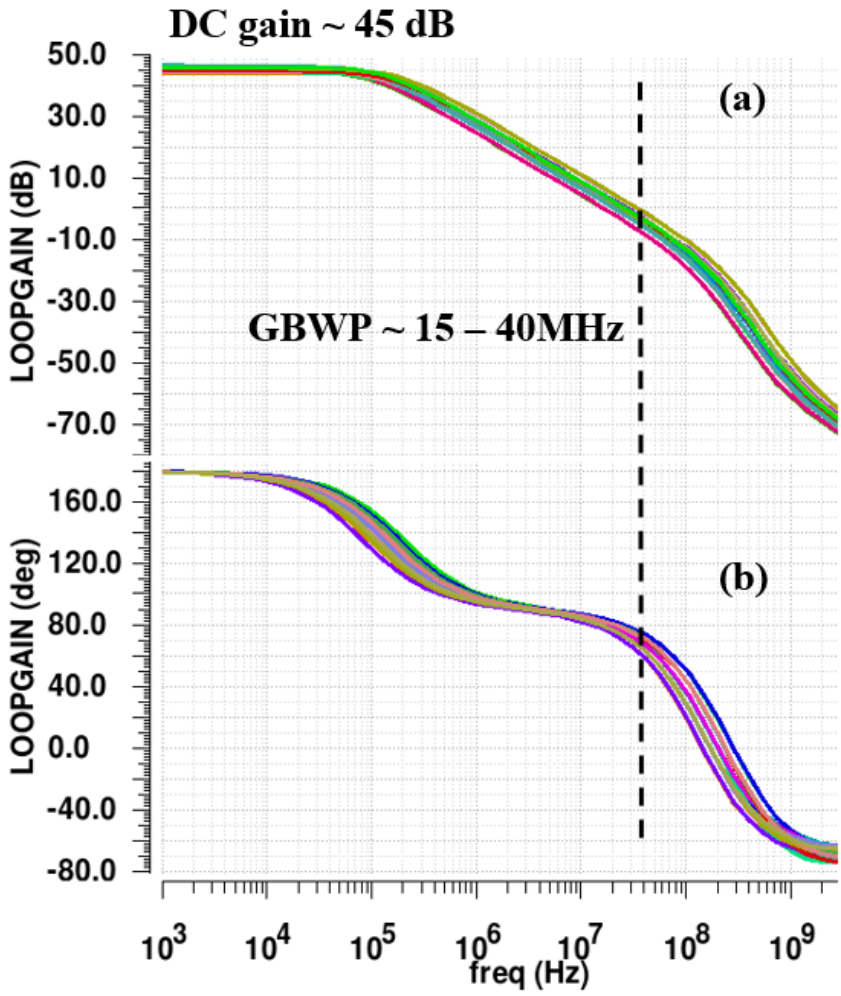


Figure 2.32: Current steering unity feedback Loop gain verification: (a) magnitude; (b) phase.

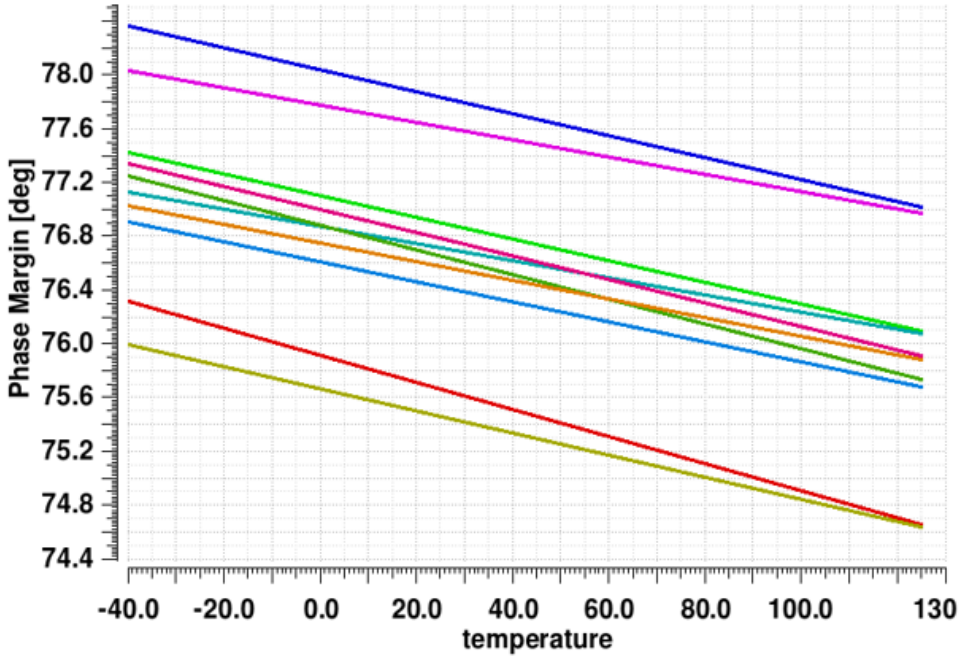


Figure 2.33: Current steering switches control signals and output current.

2.5 Layout

The designed delta-sigma system is sensitive to the layout and parasitic extractions. In the high-current values, the reference charge buffer layout is vulnerable to parasitic capacitance in the internal nodes of the transconductance cell. Such capacitance could both reduce the speed of the charge and discharge mechanisms while also increasing the overshoot by the changing the poles location, affecting the phase margin. In the lower current measurement, the sensitivity to the noise become significantly important. In order to minimize the noise, routing is done with appropriate shielding and ample spacing between metal lines.

Other general layout considerations are of the elements in the reference capacitor array and of the V2I components. In order to address them, the 64-unit capacitance of 1.25 pF is matched with symmetric routings. The capacitance array should be also located right next to the sensing pin to avoid any parasitic resistance which can slow down the

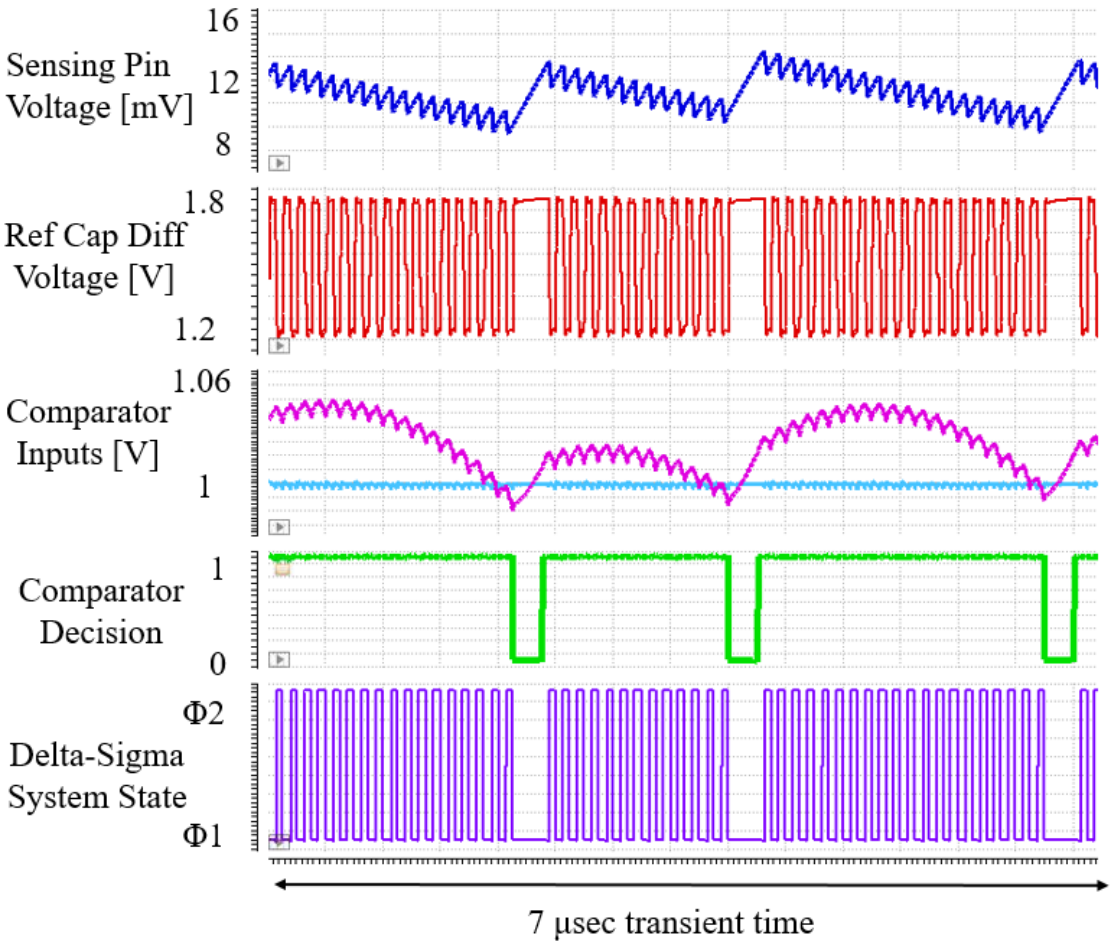


Figure 2.34: Closed-loop transient voltage waveforms for 350 μsec current measurement during a 7 μsec simulation time.

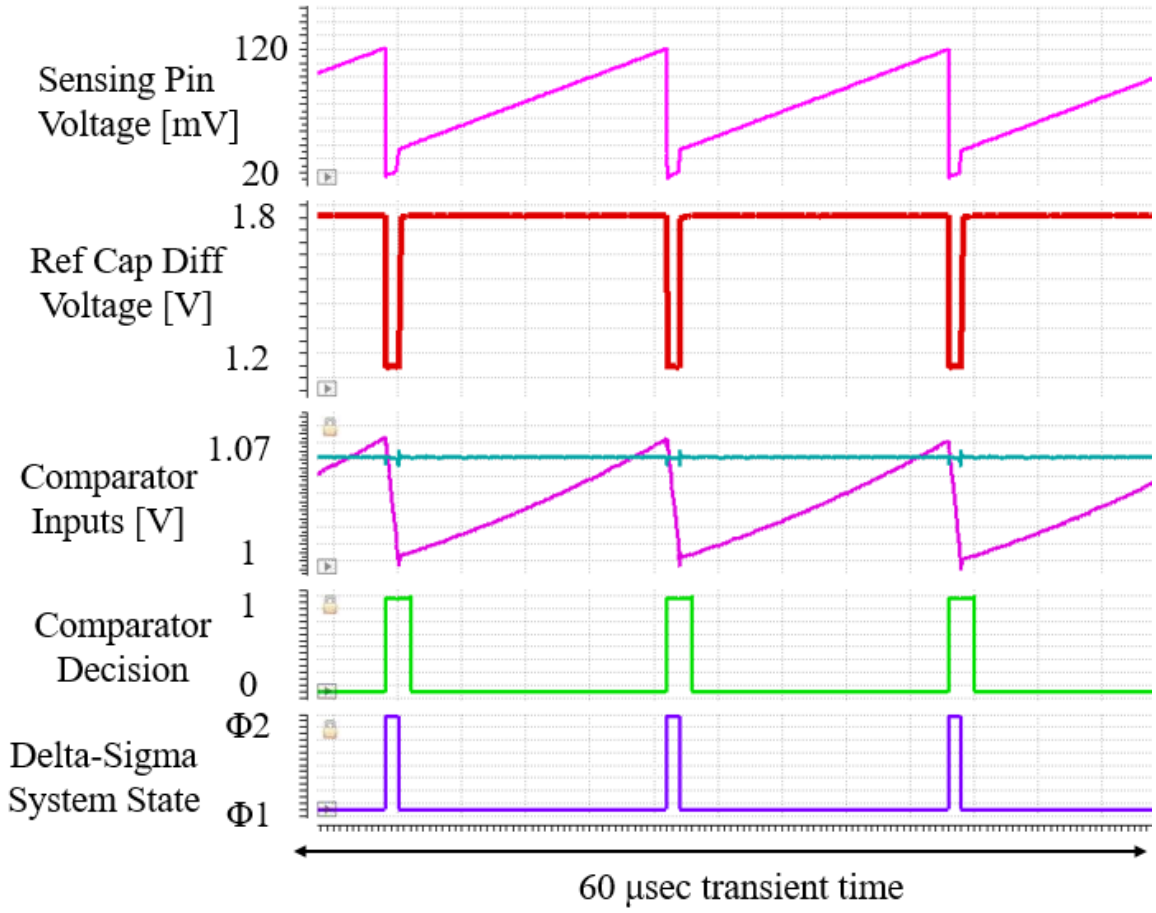


Figure 2.35: Closed-loop transient voltage waveforms for 35nA current measurement during a 60 μsec simulation time.

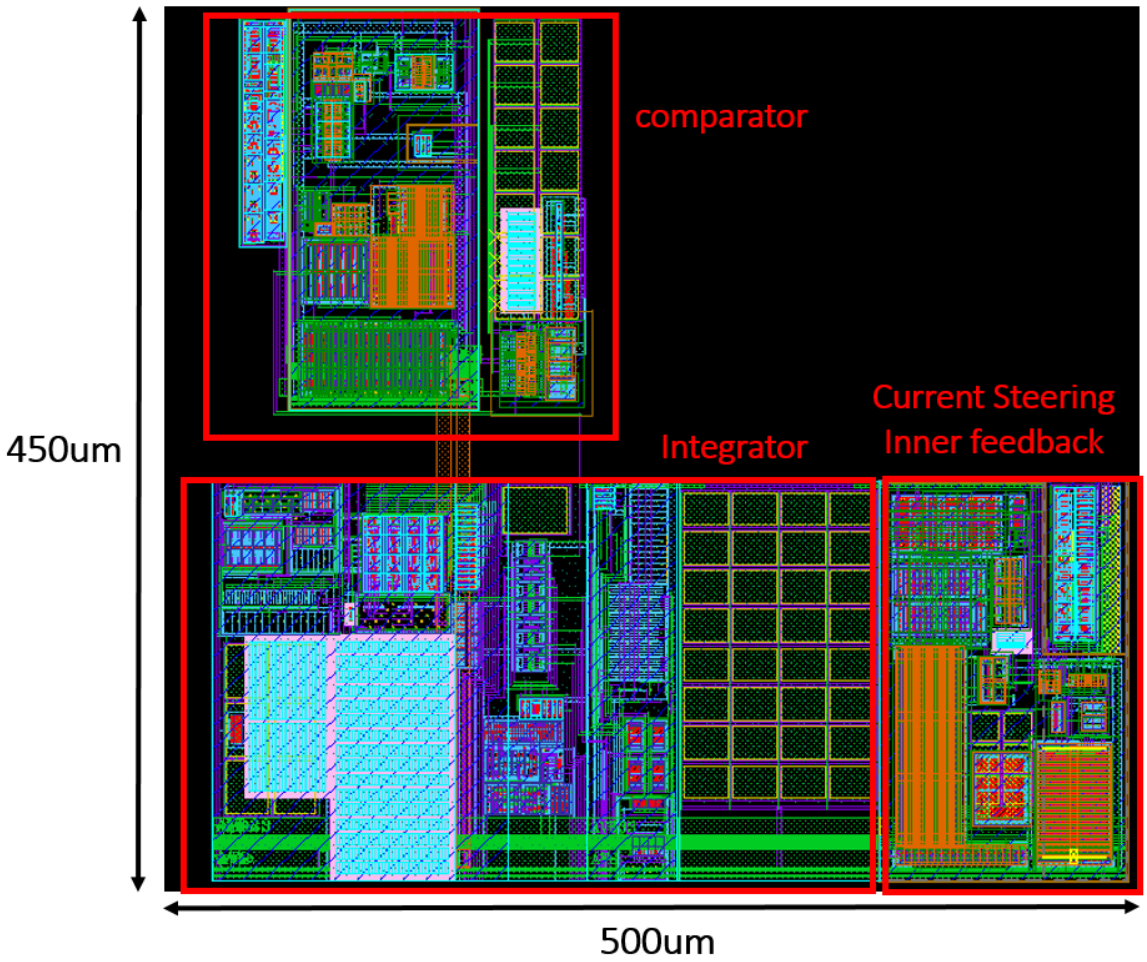


Figure 2.36: Layout for delta-sigma feed forward path and the inner loop feedback.

discharging settlement. In the V2I, all of the current sources, cascode devices, and the reference resistors are matched using a common-centroid layout.

The top level is laid out in two different islands. The first one is the feed-forward path of the integrator and comparator as shown in Fig. 2.36. The second island is the feedback discharging circuits including the V_{ref} generation block, reference buffer and capacitance array as shown in Fig. 2.37. The interface between these two islands is the sensing pin itself shielded through all the paths and the comparator decision output. The entire current sensor analog front-end, including the mentioned routing, is presented in Fig. 2.38.

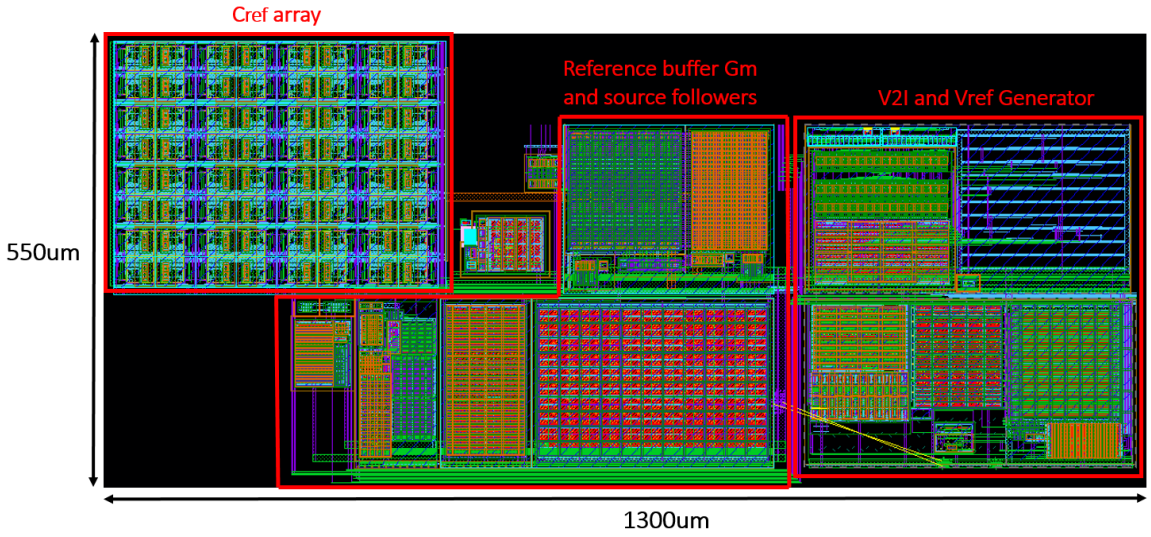


Figure 2.37: Layout for discharge and fill feedback path together with V_{ref} generator.

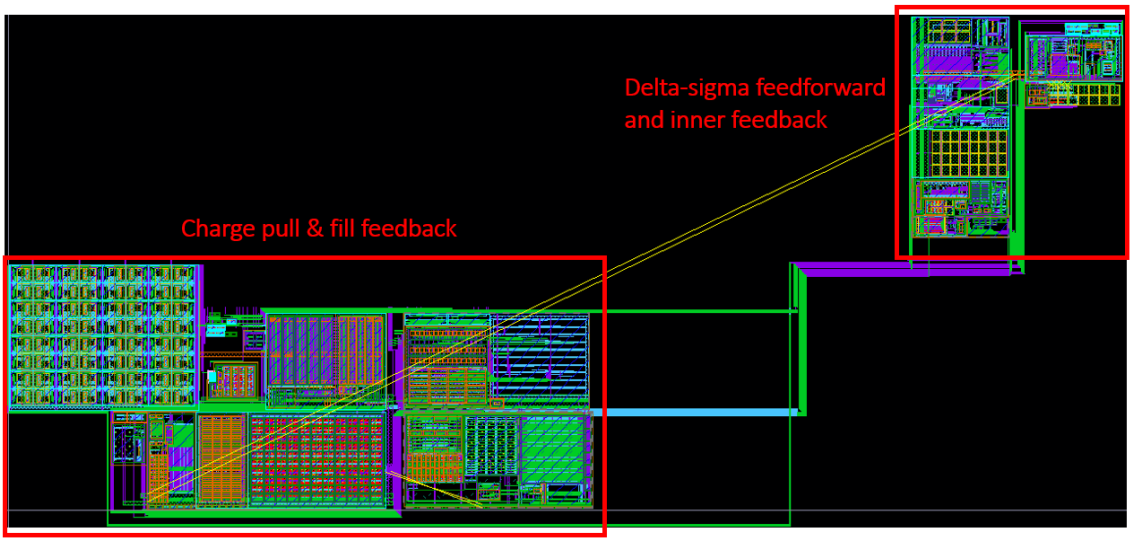


Figure 2.38: Layout for the current sensor's analog front end.

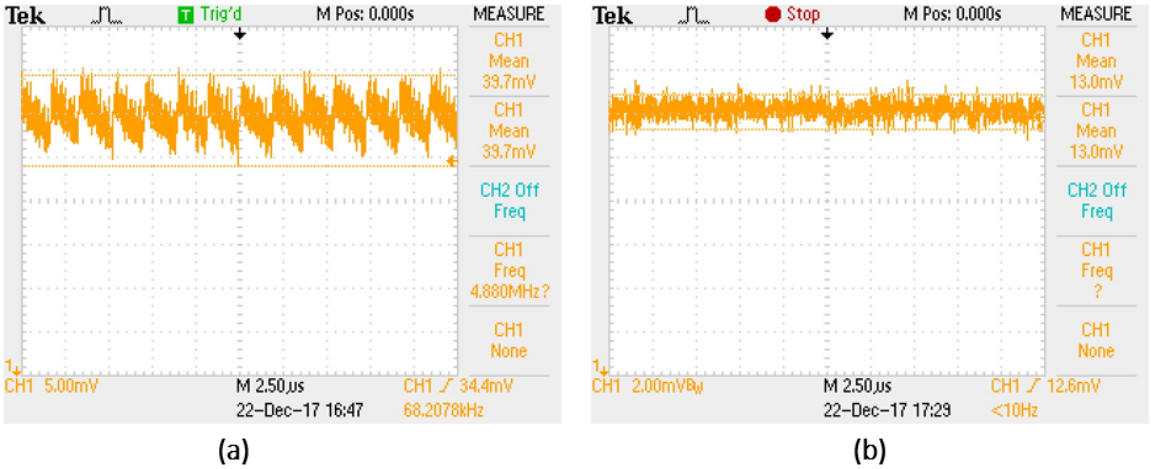


Figure 2.39: Measured Sensing pin voltage: (a) 350 μA and (b) 35 nA current measurement cases.

2.6 Measurement Results

The performance of the designed chip is verified through different current value measurements. The waveforms at the sensing pin are shown in Fig. 2.39, where the delta-sigma system is stable and functional over two extreme cases of 35 nA and 350 μA current sensing.

The accuracy is also verified by the sweeping current and repeating the measurement. The results are calculated based on N in (2.7) as the output of delta-sigma system. Since typical values for the coefficient in the same formula are known, the 2-point calibration mentioned earlier can fix any gain and offset variation. This calibration is done by measuring two known conductances. Comparing the calculated and known conductance measurements, the gain and offset error can be evaluated and canceled using a new fit line. Fig. 2.40 shows the measurements of the four samples measurement versus the fit line derived from the calibration. The relative error is also evaluated against the calibrated fit line. As indicated in Fig. 2.41 the error is within $\pm 1\%$.

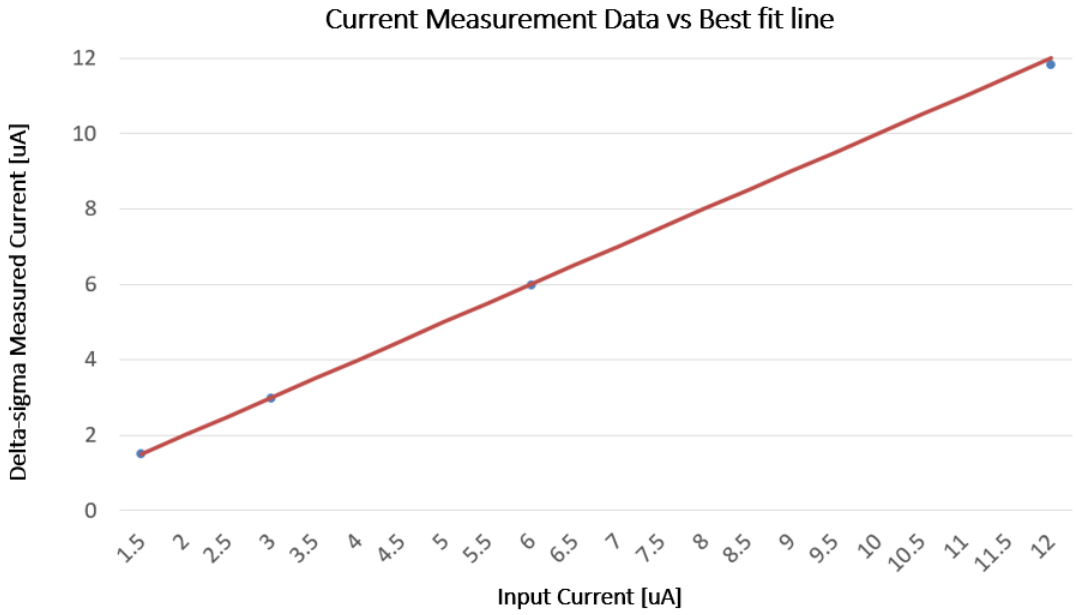


Figure 2.40: The measurement results vs. 2-point calibration fit line.

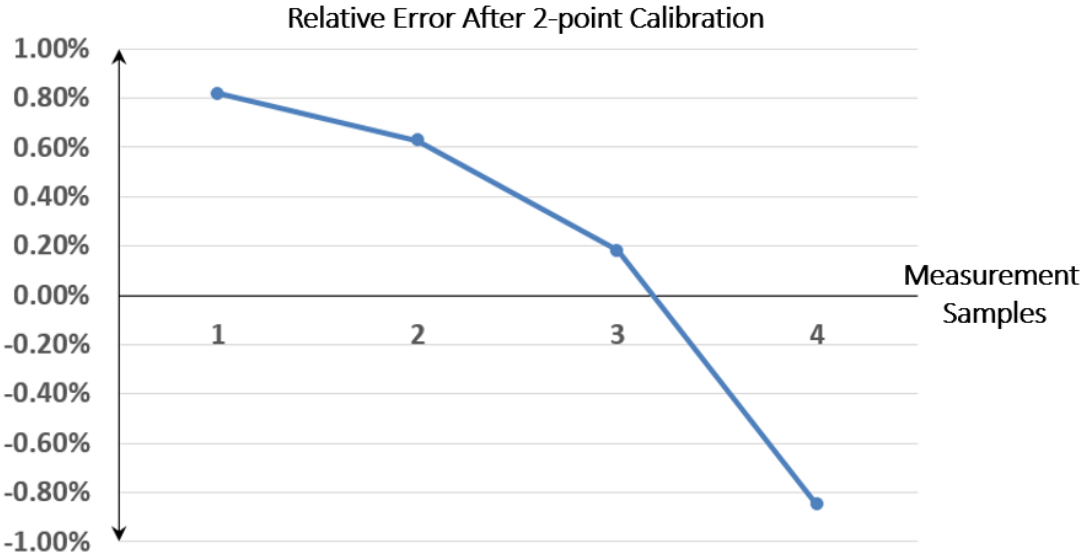


Figure 2.41: Measurement results vs. 2-point calibration fit line.

Chapter 3

Degenerate Band Edge Oscillator Design

3.1 Oscillator Architectures

Oscillators are essential blocks of all mixed mode or RF systems. The theory of oscillators is developed by generating a positive feedback loop based on Barkhausen criteria [14]. This criteria is described in Fig. 3.1 where negative feedback applied to an amplifier can give rise to oscillation if the transfer function magnitude is higher than 1 at the frequency where the phase shift exceeds 180°.

$$|H(j\omega)| = 1 \tag{3.1}$$

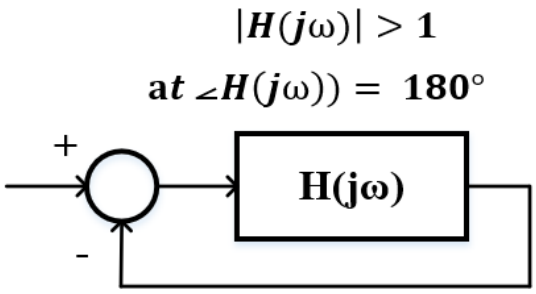


Figure 3.1: Barkhausen criteria to create an oscillator.

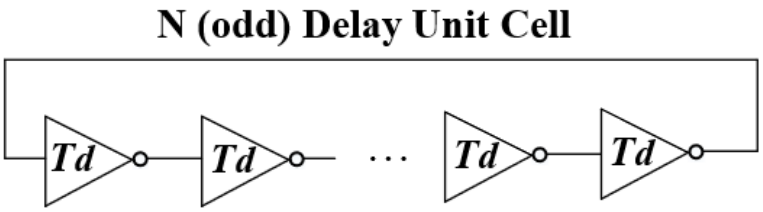


Figure 3.2: A general ring oscillator architecture.

$$\angle H(j\omega) = 180° \tag{3.2}$$

Oscillators can be divided into in three general categories: ring, RC relaxation, and LC resonator oscillators. Ring oscillators [21]-[23] are implemented using an odd number of inverting delay cells loop to create a 180° phase shift at a certain period as shown in Fig. 3.2.

Conventional RC oscillators [24]-[26] consist of a single or differential RC branch that is switched and reset triggered by a comparator shown in Fig. 3.3. The oscillator period for such an architecture is the total delay of the RC branch and the comparator path.

However, the most common architecture to synthesize RF frequencies is implemented using LC tank resonators [17]-[20]. These resonators can be used as parallel or series topology (Fig. 3.4). Series resonators are widely used in crystal oscillators to provide

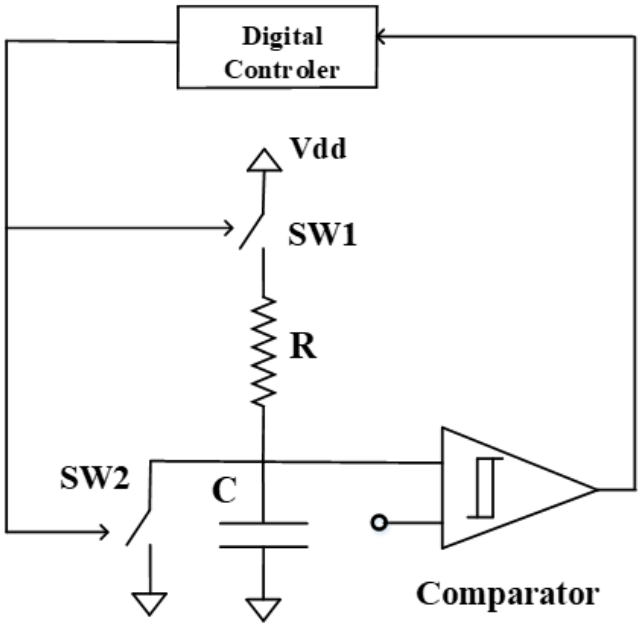


Figure 3.3: Conventional RC relaxation oscillator architecture.

accurate reference clock for the chips. Parallel LC tanks on the other hand are the main resonator in RF integrated circuits. The tank's resistor models the loss of the non-ideal resonator elements. The Q-factor of each element quantifies the amount of loss and is defined for the capacitor and the inductor as:

$$Q_L = \frac{L\omega}{R_L} \tag{3.3}$$

$$Q_C = \frac{1}{R_C C\omega} \tag{3.4}$$

where R_C and R_L are series resistors of the capacitance and the inductance and ω is the angular frequency.

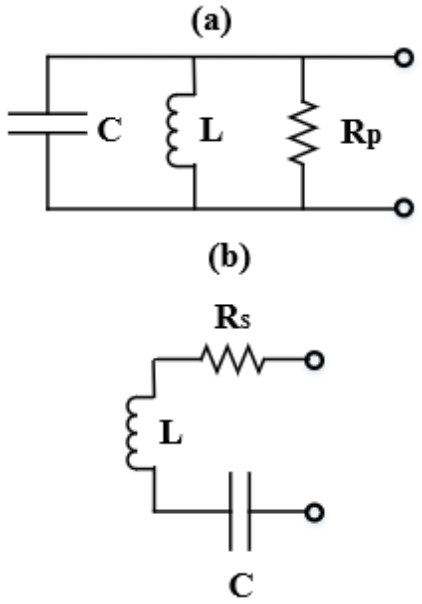


Figure 3.4: LC resonator (a) parallel and (b) series configuration.

In order to realize an oscillator using an LC resonator with loss, an active circuit is required to generate a negative conductance or resistance. That provides the 180° phase shift or, equivalently, positive feedback at the desired oscillation frequency. Cross-coupled pairs, Pierce, and Colpitts architectures are the most common active circuits to achieve this. The higher the Q-factor the less loss in the resonator elements and hence, the less negative conductance/resistance is required to create an oscillation.

Designing oscillators with a high Q-factor is an important challenge as phase noise is always a main concern in mixed-mode and RF circuits. Distributed oscillators [27] and substrate integrated waveguide (SIW) or microwave structures oscillators [28]-[32] are examples of achieving such high-Q oscillators.

The concept of realizing a degenerate band edge (DBE) [33]-[34] periodic structure, has been shown to have the potential of achieving a higher Q-factor, which in turn could result in a low phase noise profile. In this chapter, the DBE architecture and unit cells are discussed. Then, the frequency-domain admittance of such a periodic structure is studied

to identify the Barkhausen criteria. In addition, the oscillator design is performed using a cross-coupled pair that realizes a negative conductance implementation. The phase noise and power consumptions are simulated in the end to show the advantages of employing DBE architecture in oscillator design.

3.2 Degenerate Band Edge (DBE) Structures

As described earlier, single-ladder periodic structures are used to create oscillator architectures in order to achieve higher Q factors. The unit cell of such a structure is shown in Fig. 3.5(a). On the other hand, as DBE periodic structures can realize higher Q factors in their frequency characteristics, we explore the details of implementing an oscillator architecture in this chapter. A symmetrical DBE unit cell is presented in Fig. 3.5(b) with the same L and C, where the inductor and the capacitor can be either lumped elements or extracted from periodic microstrip lines. The DBE structure is a double-ladder unit cell with a series of inductors coupled together through the capacitance in addition to capacitors to ground.

Fig. 3.6(a) shows a periodic architecture using nine DBE unit cells connected in tandem. In order to create oscillation from this passive structure and meet the Barkhausen criteria, an active circuit should be added. The following section describes how to design an oscillator from the indicated DBE periodic structure.

3.2.1 DBE Architecture Admittance

Due to the loss of the DBE double-ladder components, the oscillator needs an active circuit to realize a negative conductance that can overcome the total loss. Such loss at

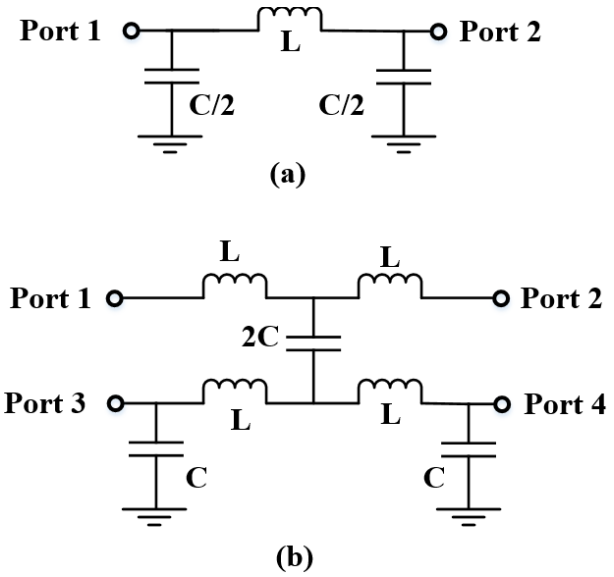


Figure 3.5: (a) Symmetrical single-ladder Unit cell; (b) symmetrical Degenerate Band Edge Unit Cell.

the resonant frequency can be represented by the real part of the driving-point admittance where the imaginary part crosses zero. In the DBE periodic structure the only port to observe symmetric finite DBE architecture is the middle cell, assuming that there is an odd number of cells as suggested in Fig. 3.6(b). The symmetry in the oscillator architecture also makes a convenient fully differential configuration, which is desirable in integrated circuits. The DBE structure is modeled using unit cell parameters of L = 45 nH and C= 56 pF, with series resistance of R_L = 180 mΩ and R_C = 30 mΩ corresponding to Q_L = 150 and Q_C = 500, respectively. These components are selected from available off-chip lumped elements [35]-[36]. The DBE resonant frequency $f_{res} \approx 1/(2\pi\sqrt{LC})$ = 100 MHz. A sweep of the driving-point admittance over frequency is shown in Fig. 3.7(a). The real part of the admittance around 100 MHz (corresponding to the circuit's resonant frequency) indicates the minimum required negative conductance that will be required to meet the oscillation criteria. Using the same unit cell parameters mentioned in the previous section, 660 μS is the minimum negative conductance between the two nodes to meet the Barkhausen criteria. This is less than half of what would be required for the

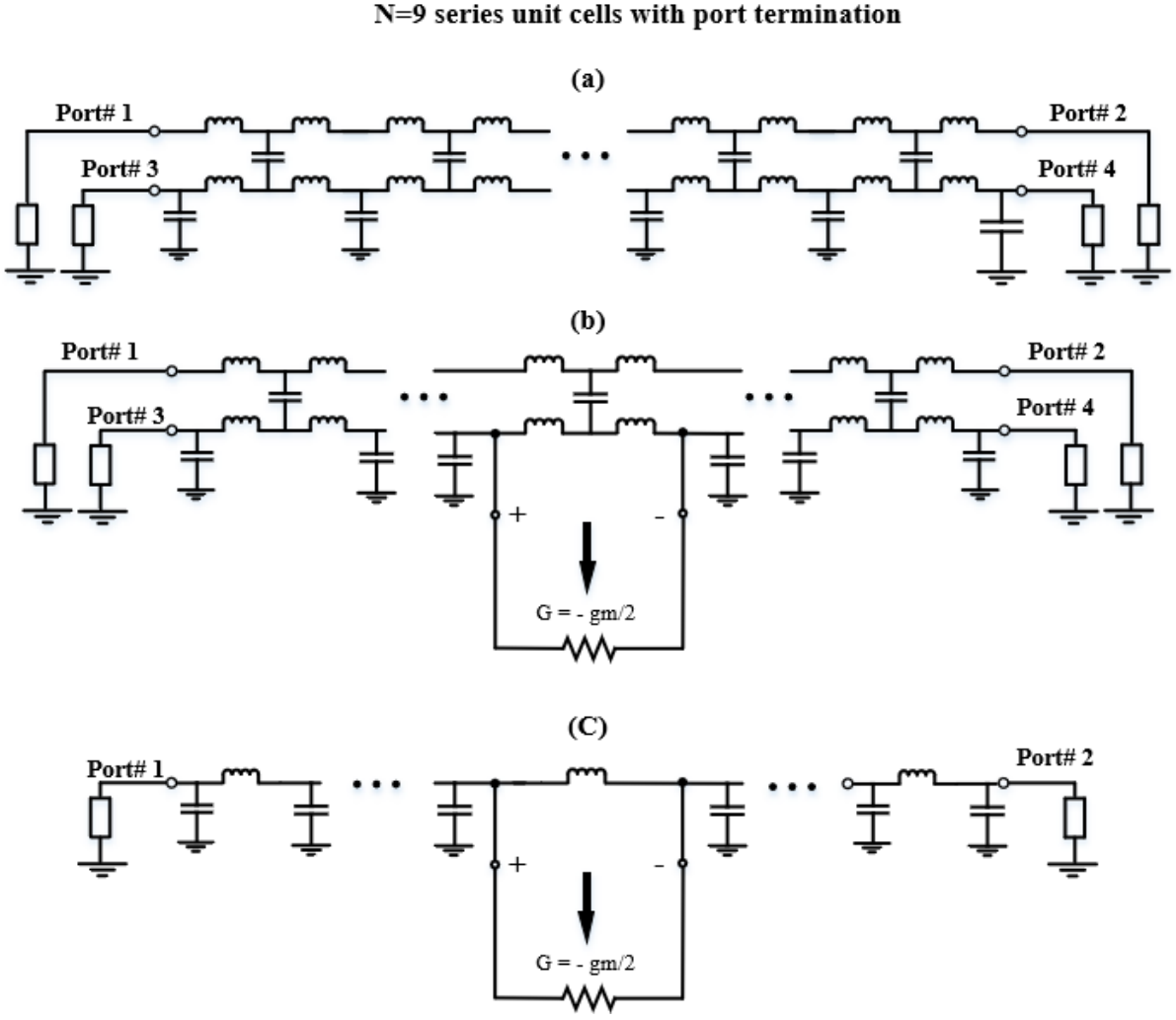


Figure 3.6: (a) DBE periodic structure model (b) DBE oscillator architecture (c) Single-ladder oscillator architecture.

equivalent single-ladder oscillator in Fig. 3.6(c) using the same parameters. As illustrated in Fig. 3.7(b), the real part of the admittance at the resonance frequency is 1.6 mS. The periodic structure's middle point not only provides the symmetry for the differential implementation, but also has the lowest required negative admittance for the oscillation. Fig. 3.8 shows the the driving-point admittance at the resonant frequency corresponding to each portion of the structure. That is why the oscillator implementation shown in Fig. 3.6(b) is the most efficient approach.

3.2.2 Nonlinear Negative Conductance

Negative conductance architectures are normally implemented using a positive feedback internally realized by active devices. Among different topologies, a conventional NMOS cross-coupled pair shown in Fig. 3.9 is a straightforward approach. The tail current source provides the biasing for the cross-coupled pair to realize the small-signal differential transconductance of -$g_m/2$, where g_m is the transconductance of each transistor at the bias point. In large-signal operation, the negative conductance degrades as the one of the transistors enters the triode region. Finally, when the differential signal is very large, one the devices switch off. In this region, the cross-coupled pair behaves like a small-signal open circuit. Such behavior is shown in the simulated dc sweep shown in Fig. 3.10 where the active circuit is implemented using TowerJazz sbc18h BiCMOS N-channel devices with 1.8 V and 700 μA supply voltage and bias current, respectively. Near the origin the I-V characteristics exhibit a negative slope. The dependency of the negative conductance slope on the cross-coupled pair bias current is presented in Fig. 3.11.

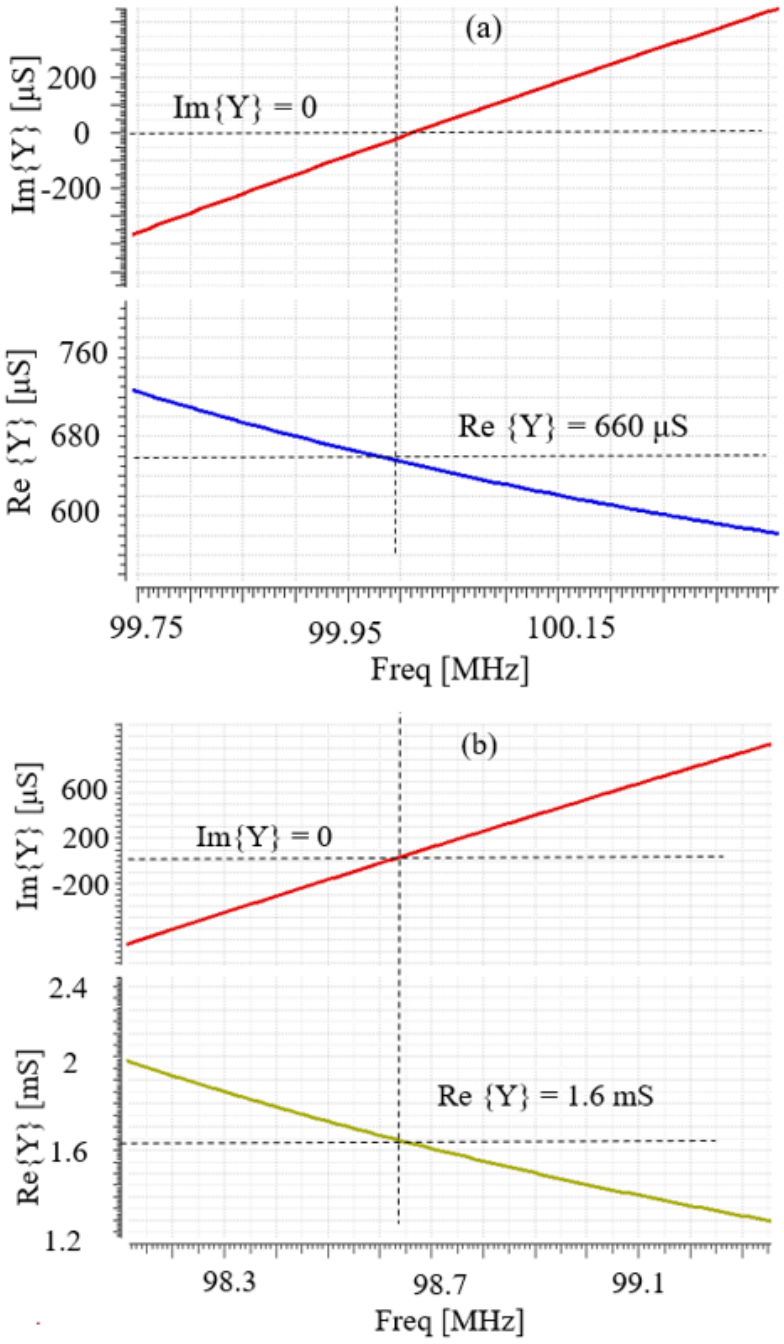


Figure 3.7: Real and imaginary parts of port admittances to determine the required negative conductance: (a) DBE architecture; (b) equivalent single-ladder.

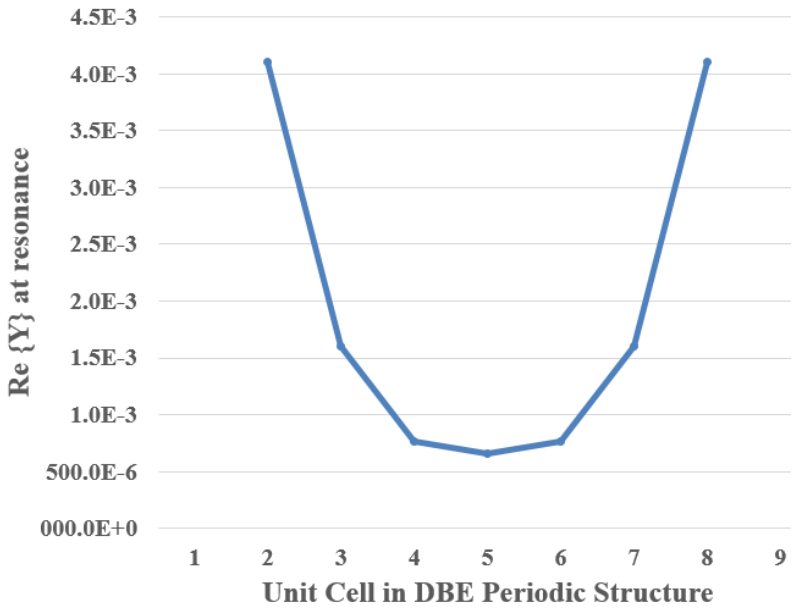


Figure 3.8: Admittance real part at resonance for different unit cells in the Fig. 3.7(a) DBE architecture.

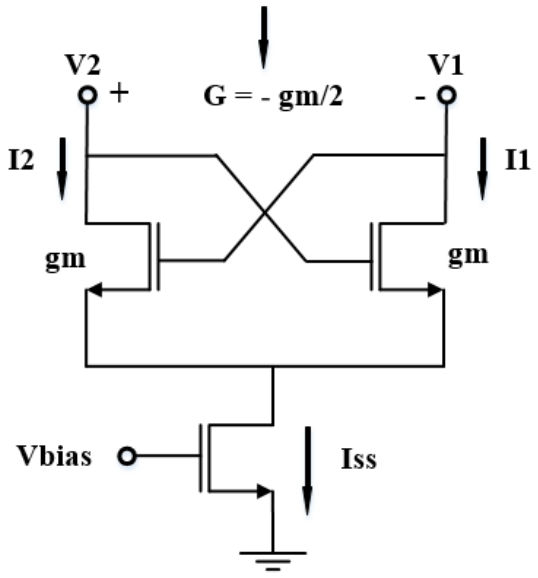


Figure 3.9: Nonlinear negative conductance implementation using cross-coupled pair.

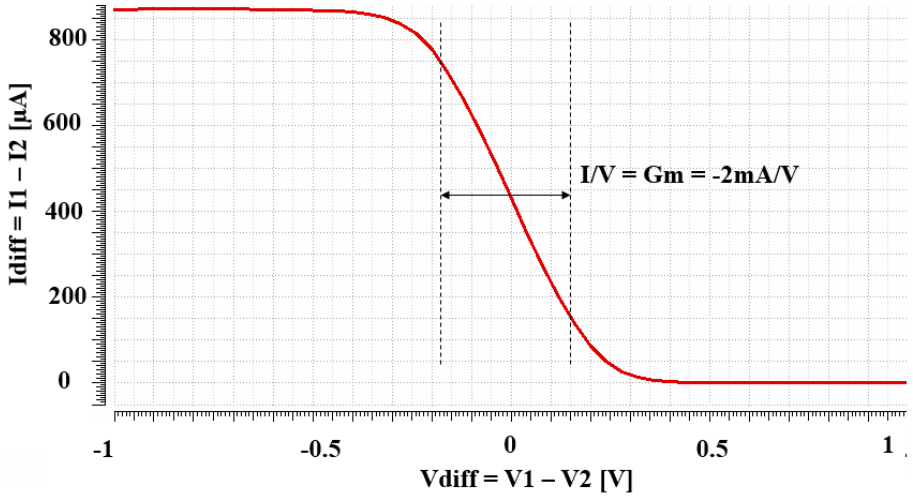


Figure 3.10: Nonlinear negative conductance from cross-coupled pair differential I-V Curve.

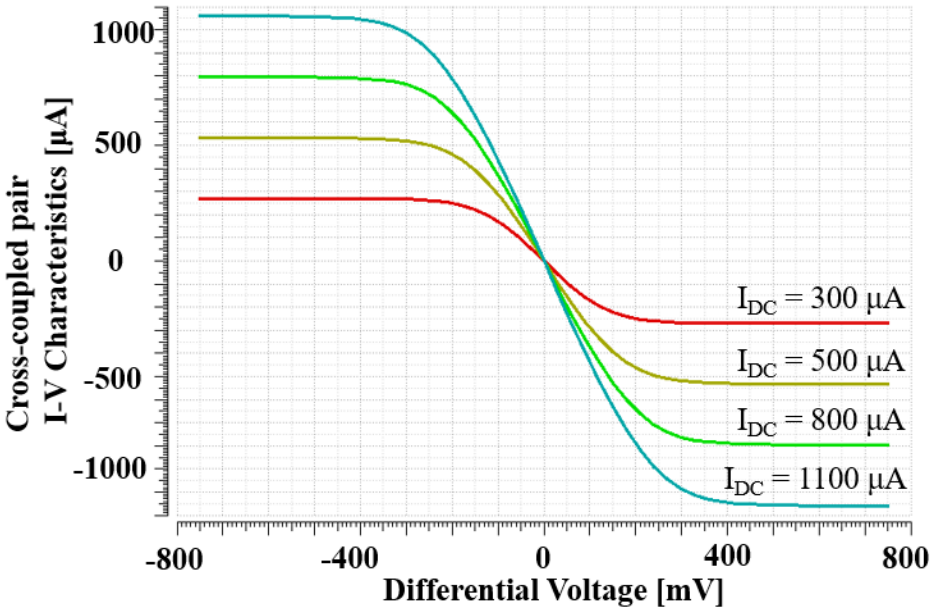


Figure 3.11: Nonlinear negative conductance from cross-coupled pair differential I-V Curve for different bias current.

3.3 Degenerate Band Edge Oscillator Architecture

3.3.1 Circuit Implementation

As discussed in the previous section, in order to realize a symmetric admittance, the middle DBE unit cell is chosen to be connected to the negative conductance cell. Such an oscillator architecture in shown Fig. 3.6(b) where the negative conductance is implemented using the circuit shown in Fig. 3.12. The off-chip chokes are employed to DC bias the cross-coupled pair. In addition, the off-chip coupling capacitors of 100 nF, used to decouple the DC biasing from the periodic structure, have a negligible high-frequency impedance to connect the active circuit to the DBE structure. The simulated oscillation startup is shown in Fig. 3.13 using transient simulation. The steady-state sinusoidal oscillation signals at the DBE structure terminals and cross-coupled output nodes are shown in Fig. 3.14 for three different termination loads at ports 1 and 2 – open circuit, short circuit, and 50 Ω. Ports 3 and 4 are terminated with an open circuit. As expected, the internal oscillation amplitude is not highly dependent on termination load resistance. On the other hand, the single-ladder terminated load, whose waveforms are shown in Fig. 3.15, exhibits reduced oscillation amplitude with lower terminal impedance.

3.3.2 Advantages of DBE Oscillators

Advantages of using the proposed DBE architectures as an oscillator include lower phase noise and no additional power consumption required to drive an external load resistance. As DBE periodic structures show higher Q-factor compared to single-ladder structure with the same unit cell parameters, they present improved phase noise. This comparison is shown in the Fig. 3.16 where the phase noise of a DBE and a single-ladder oscillator

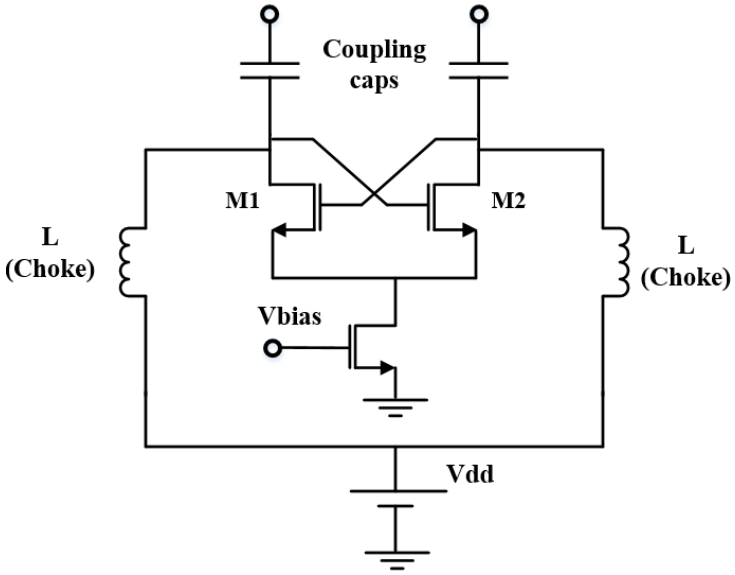


Figure 3.12: Nonlinear negative conductance implementation using cross-coupled Pair.

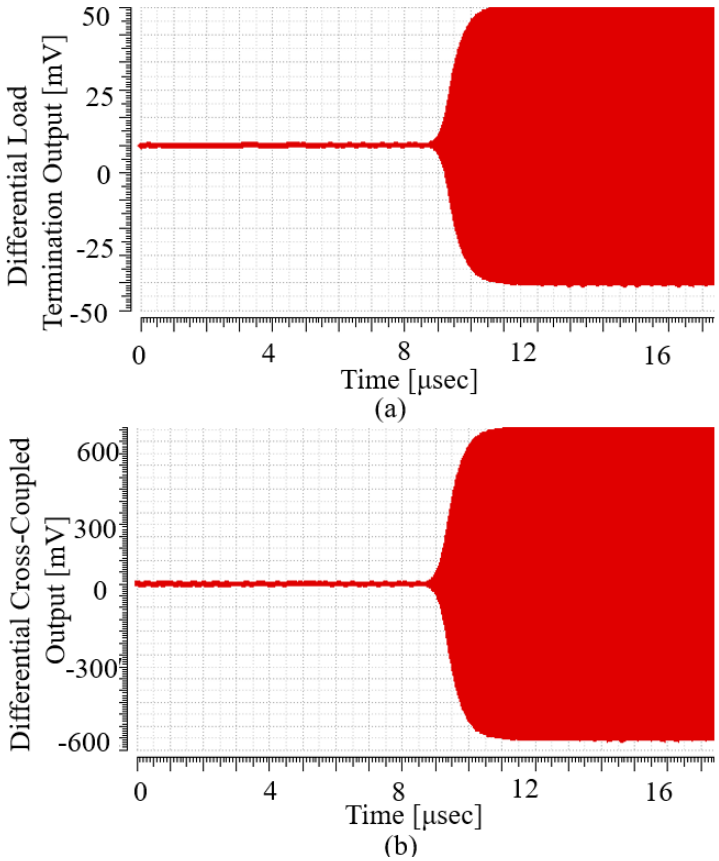


Figure 3.13: Oscillator startup in transient simulation.

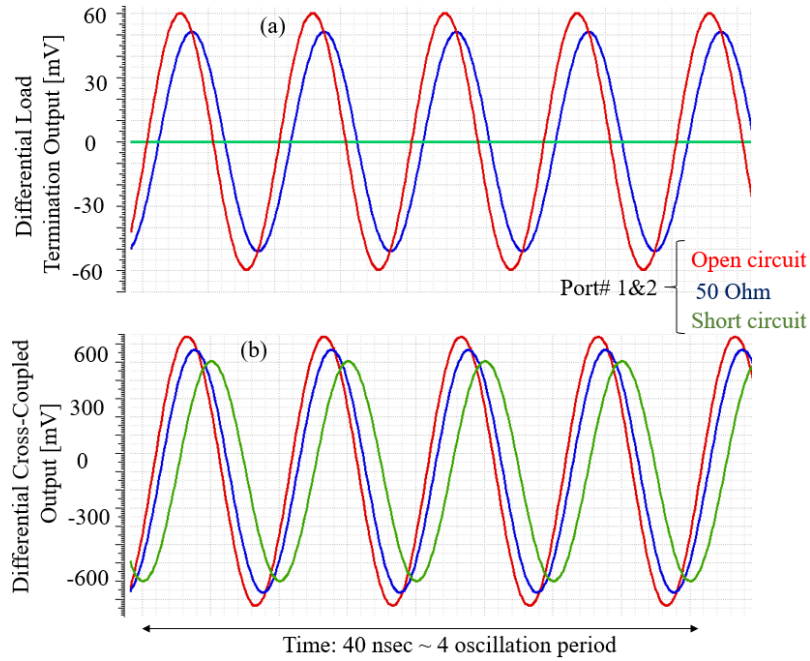


Figure 3.14: DBE oscillator terminal transient signal for different load impedance values while ports 3 and 4 terminated by open circuit.

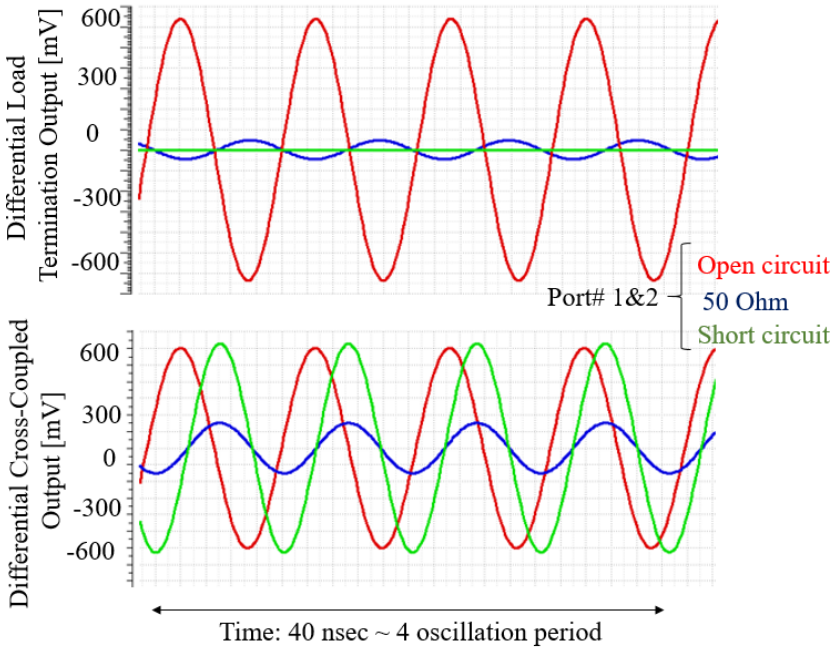


Figure 3.15: Single-ladder oscillator terminal transient signal for different load impedance values.

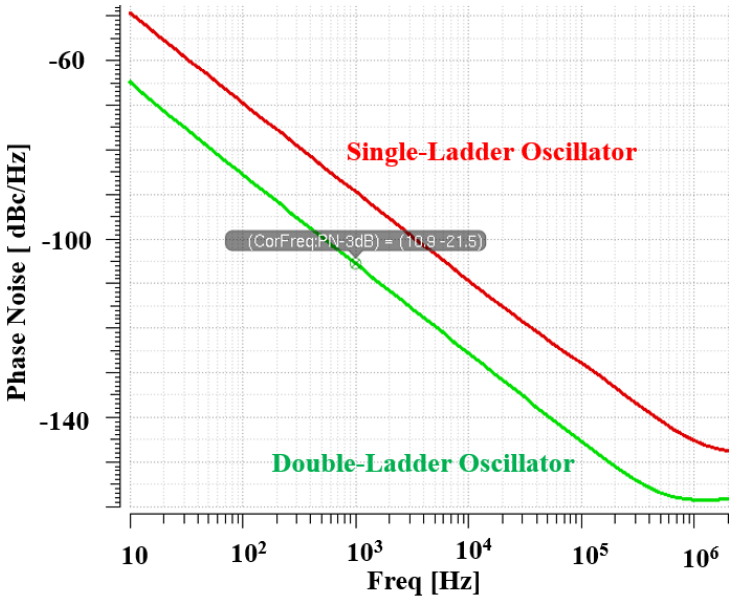


Figure 3.16: Phase noise comparison.

are evaluated at the output of the cross-coupled pair indicating nearly 15 dB phase noise improvement.

Another significant advantage of using the DBE architecture is that a power-hungry buffer is often not needed to drive the load resistance. In a conventional LC oscillator implementation, the differential signals must pass through one or more stages of buffers to be terminated to a 50 Ω. To achieve a 100 mV peak-to-peak oscillation amplitude at the load, a typical CML buffer chain with 50 Ω back termination resistance and an off-chip load needs at least 2 mA tail current at the latest stage as shown in Fig. 3.17. On the other hand, the DBE oscillator achieves the same oscillation amplitude with 700 μA current consumption and no extra buffer. The details of this comparison are presented in Table.3.1. The transient waveforms can be found in Fig. 3.18.

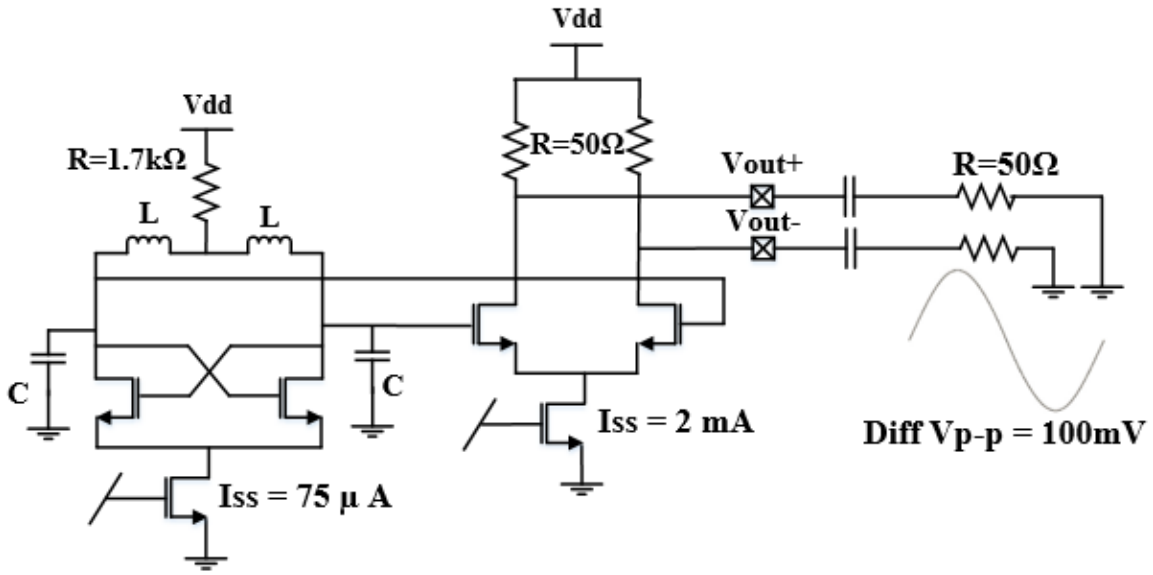


Figure 3.17: CML buffer load termination of conventional LC oscillator architecture.

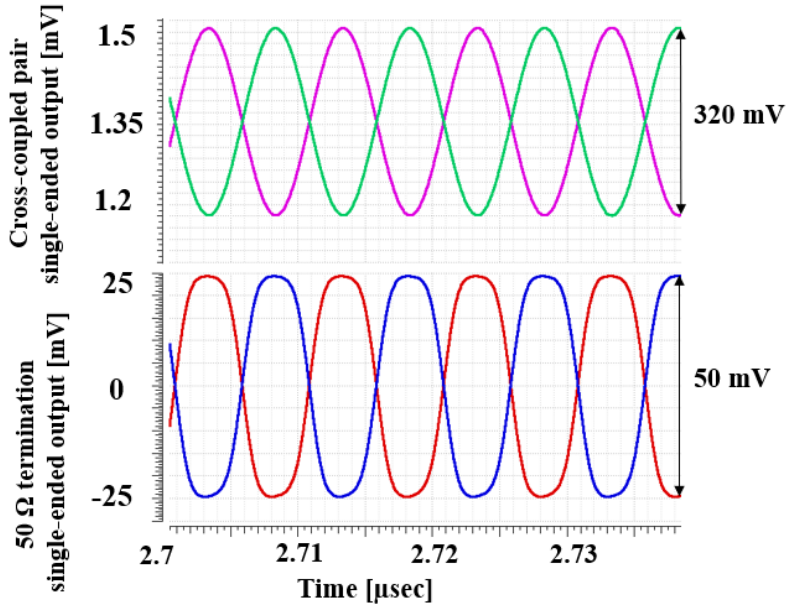


Figure 3.18: Conventional LC oscillator and CML buffers 50 Ω termination transient waveforms.

Oscillator Type	Negative Gm Current	Buffer Current	Total Current
DBE Osc	0.7 mA	0	0.7 mA
Single Ladder	0.74 mA	0	0.74 mA
Conventional LC	0.075 mA	2 mA	2.075 mA

Table 3.1: Oscillator current consumption details to reach differential 100 mVp-p oscillation amplitude at 50 Ω termination at 1.8 V supply voltage.

Chapter 4

LC Oscillator Design With Supply Sensitivity Compensation Method

A critical component of any broadband transceiver is the internal high-speed clock that generates the synchronization signal, generally a voltage-controlled oscillator (VCO). In order to maintain proper signal integrity it is imperative that the VCO output exhibit sufficiently low jitter. This jitter arises from both internal random noise generation and disturbances from outside the VCO circuitry, including power supply variation. Techniques for reducing the random jitter generated by the VCO itself are well known [39, 40]; however, predicting and guarding against external disturbances are more difficult to achieve. This is exacerbated by the trend to place more circuitry, on a single chip (particularly digital blocks), thereby coupling in significant switching noise. Although the effect of much of the noise coupling from the substrate can be reduced by appropriate layout techniques (e.g., guardbands or use of additional wells), it is more difficult to reduce the effect of noise coupled from the power supply. One of the most common ways to reduce LC VCO sensitivity to supply noise is making use of an on-chip low-dropout regulator

[42]. The quiescent additional LDO's current can be around 4% of the oscillator current consumption [45]. On the other hand, the technique developed in this chapter, dynamically compensates the supply noise effects. The method is first presented in [37] and [38]. It is also redesigned in TSMC 65nm process, achieving more than 85% improvement in frequency variation and periodic jitter.

In this chapter, an analysis of the supply sensitivity of a high-speed LC VCO is presented. The effect of supply variation on the operation of conventional LC oscillators is described first. Then, a compensation method to reduce this sensitivity is proposed along with simulation results, indicating sensitivity reduction.

4.1 LC Oscillators Supply Sensitivity

An LC oscillator topology with an NMOS cross-coupled pair is shown in Fig. 4.1. The LC tank capacitance consists of a pair of varactors C_{var} to fine tune the oscillation frequency as a VCO based on the control voltage V_{cont}, and the parallel capacitance C_p. This parallel capacitance includes parasitic capacitance C_{par}, load capacitance of the following stage C_L as well as the fixed output capacitances $C_{coarse-tune}$ for coarse tuning. C_{par} itself exists mainly due to the gate and drain capacitance of the cross-coupled pair transistors. Using the differential inductor L, the resonance frequency can be written as:

$$f_{res} = \frac{1}{2\pi\sqrt{L(C_p + C_{var})}} \tag{4.1}$$

where $C_p = C_{par} + C_L + C_{coarse-tune}$. In order to meet the oscillation criteria, a negative conductance is realized by the NMOS cross-coupled pair. The common-mode resistance

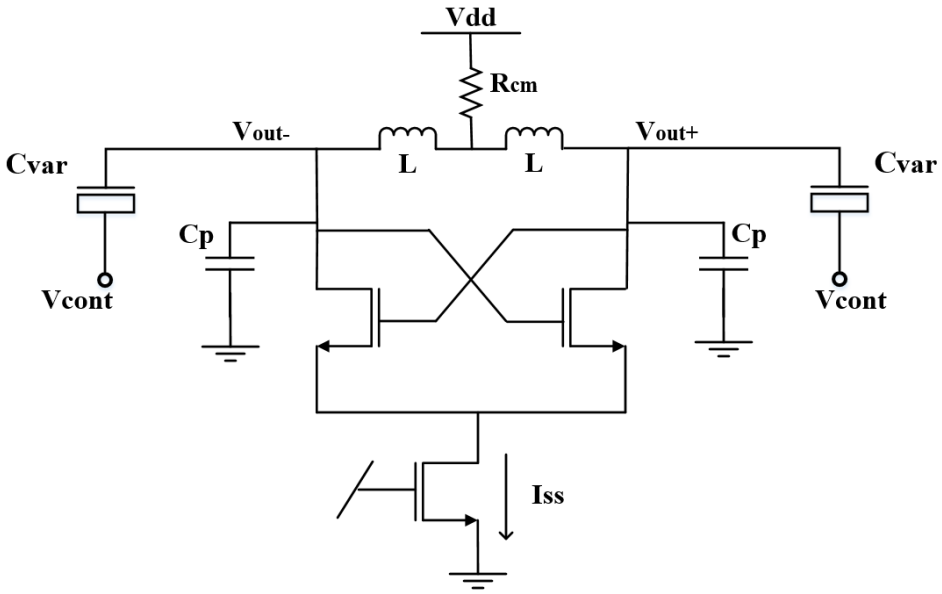


Figure 4.1: LC Oscillator architecture with NMOS cross-coupled pair as the negative conductance.

R_{CM} is used to shift the common-mode output voltage level V_{CM} lower than supply. The oscillation frequency is designed to be near 6.6 GHz, with $L = 0.5$ nH, $C_p \approx 400$ fF, and C_{var} varies between 22 and 44 fF.

$C_{coarse-tune}$ is normally designed using MIM or MOM capacitance providing a linear characteristics that is nearly independent of voltage. The parasitic capacitance is slightly nonlinear and varies as the output voltage or the control voltage changes. However, the varactor capacitance is sensitive to the output voltage. Fig. 4.2 shows the frequency vs. control voltage for the designed VCO. Near the center of the characteristic the slope K_{VCO} is approximately 300 MHz/V.

The varactor is implemented by NMOSCAP devices using the N+ doping in the NWELL. There is no threshold voltage on NMOSCAP, so the maximum capacitance variation occurs close to zero gate-bulk voltage. The capacitance vs. gate-bulk voltage is shown in Fig. 4.3. The NMOSCAP is sized to set the slope of C_{var} vs. differential voltage in order to adjust the target K_{vco}. The oscillator fixed capacitance can be also trimmed in order

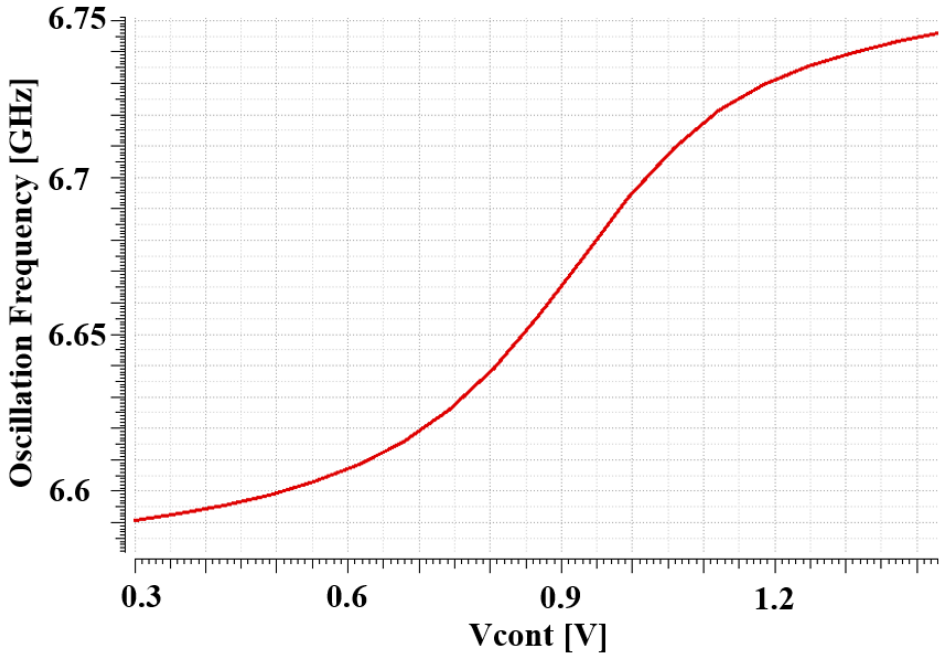


Figure 4.2: LC oscillator frequency vs. control voltage.

to create different frequency bands for the oscillator as shown in Fig. 4.4.

Although using varactor provides the possibility to control the oscillation frequency by a control voltage, it makes the oscillator more sensitive to the supply noise as any supply disturbance can change the voltage across the varactor.

In order to show the supply sensitivity, a sinusoidal disturbance with frequency 10 MHz and amplitude 50 mV peak-to-peak was superimposed onto the 1.2 V supply voltage. The 10 MHz frequency is chosen here because in a typical high-speed communication transceiver the PLL in which the VCO is embedded would typically have a jitter bandwidth on the order of 1MHz. Frequency components of the disturbances below this bandwidth would naturally be attenuated by the action of the PLL. On the other hand, since the periodic jitter is inversely proportional to the disturbance frequency (as derived in Appendix 1 in [22], frequency components much higher than the jitter bandwidth would have little effect on the output periodic jitter. For this reason, 10 MHz was chosen as the

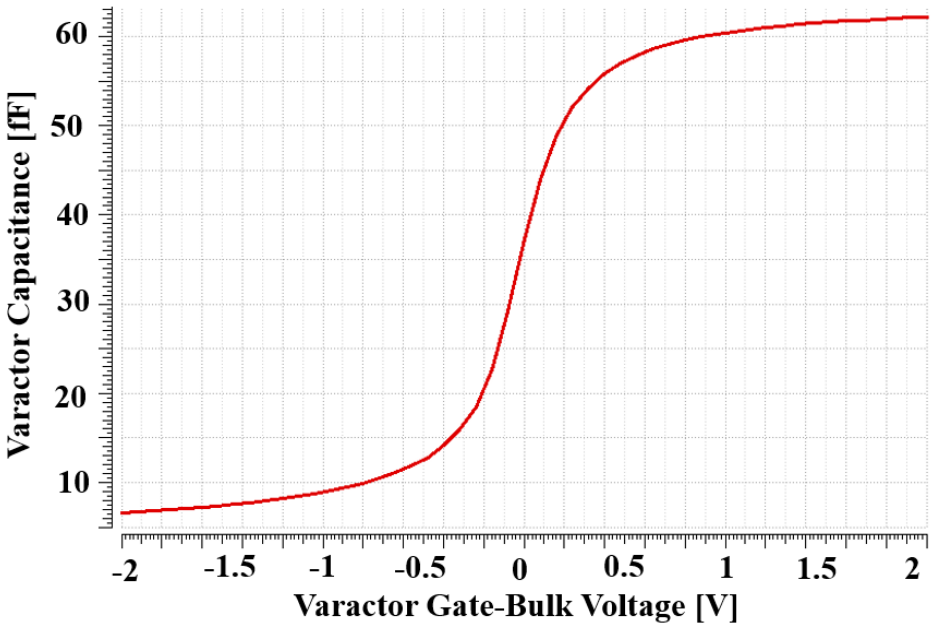


Figure 4.3: Varactor capacitance dependency on differential voltage.

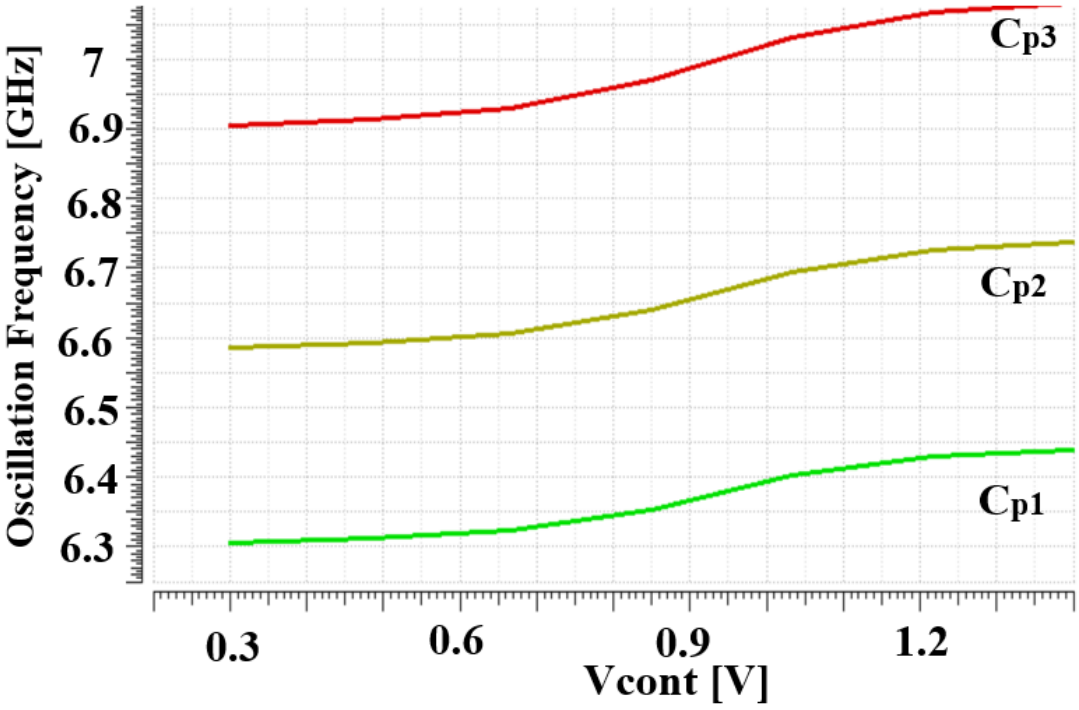


Figure 4.4: Coarse tuning of LC oscillators using the trimming load capacitance.

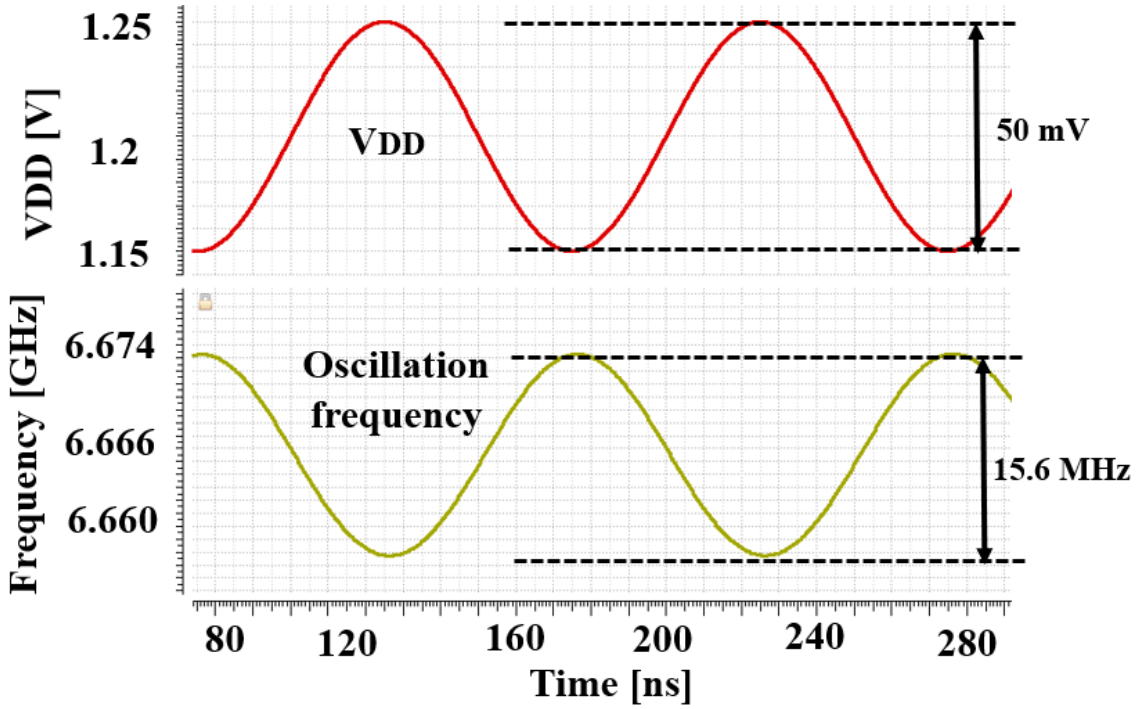


Figure 4.5: Oscillation frequency variation with supply disturbance.

disturbance frequency for the simulations presented here.

The oscillator frequency variation is shown in Fig. 4.5. A frequency variation of 15.6 MHz p-p can be observed as the result of the supply disturbance. The eye closure due to the supply noise-induced jitter is also shown in Fig. 4.6.

4.2 Sensitivity Mechanisms

In this section we investigate the two mechanisms that can lead to this sensitivity. They will be used to introduce a technique to cancel out the total sensitivity.

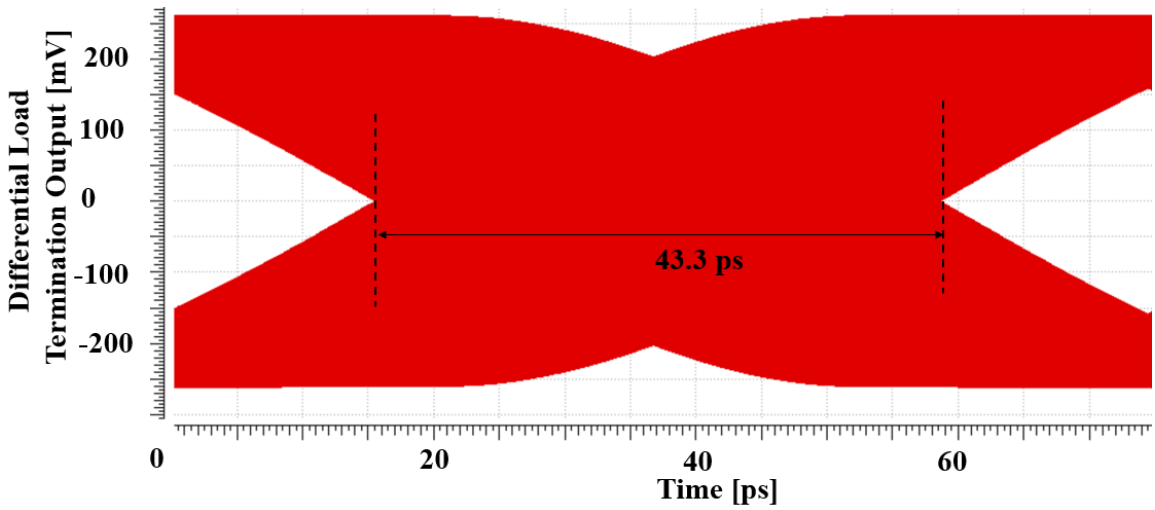


Figure 4.6: Oscillator output eye diagram.

4.2.1 Sensitivity on Common Mode Voltage

As described in the previous section, the voltage controlled capacitance (varactor) used in the VCO architecture is the primary cause of the sensitivity of the oscillation frequency to the supply voltage. Assuming the VCO control voltage is provided through the PLL's low-pass filter, V_{cont} will not be affected by the high frequency noise. However, the common-mode voltage at the LC tank can be directly affected from a disturbance on the supply. Fig. 4.7 shows the V_{CM} variation over V_{DD} variation under the condition that the tail current is biased independent of the supply voltage. The higher the K_{vco}, the higher the sensitivity to the supply and common-mode voltage.

4.2.2 Sensitivity to Oscillation Amplitude

Despite the fact that the LC tank resonant frequency is mainly shifted by the voltage across the varactor, oscillation amplitude variation (when V_{CM} is constant) also affects the oscillation frequency. To illustrate this fact, the oscillation frequency variation is plotted in Fig. 4.8 when a 10 MHz sinusoidal disturbance with 200 μAp-p amplitude is

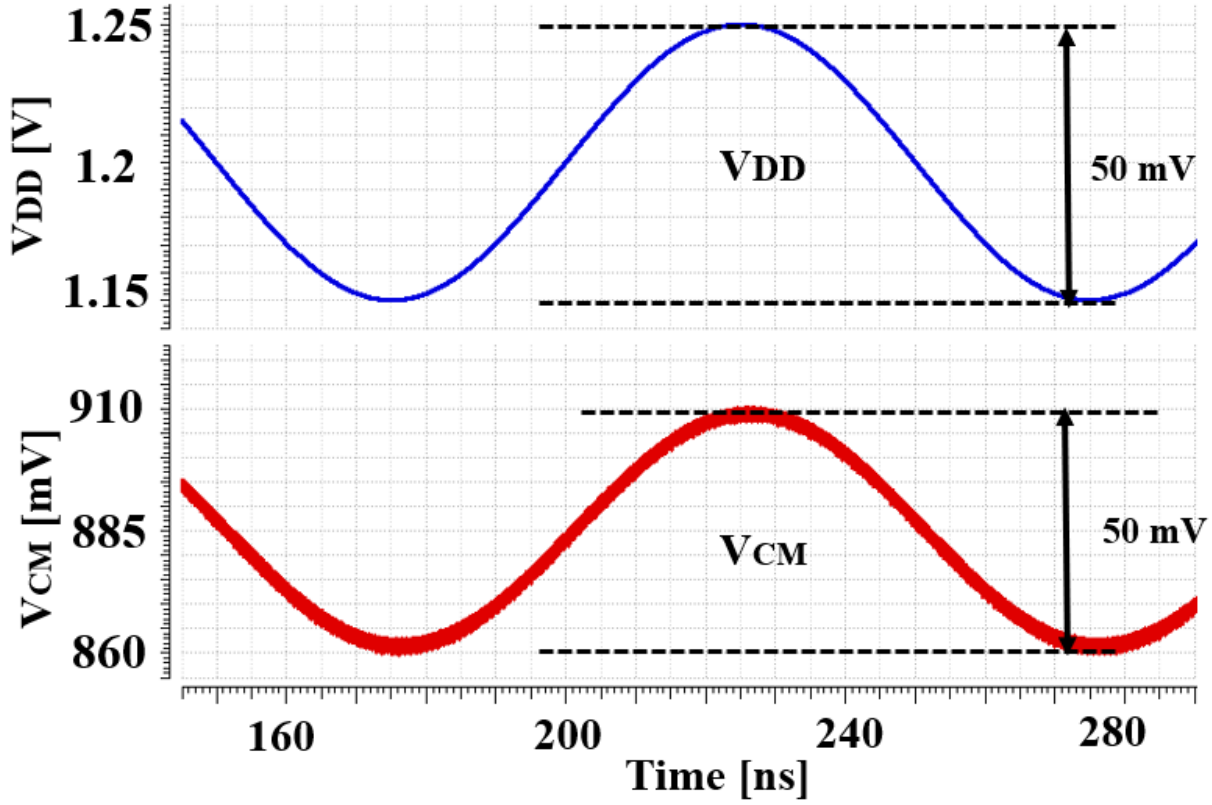


Figure 4.7: Oscillator output common-mode voltage vs. supply disturbance.

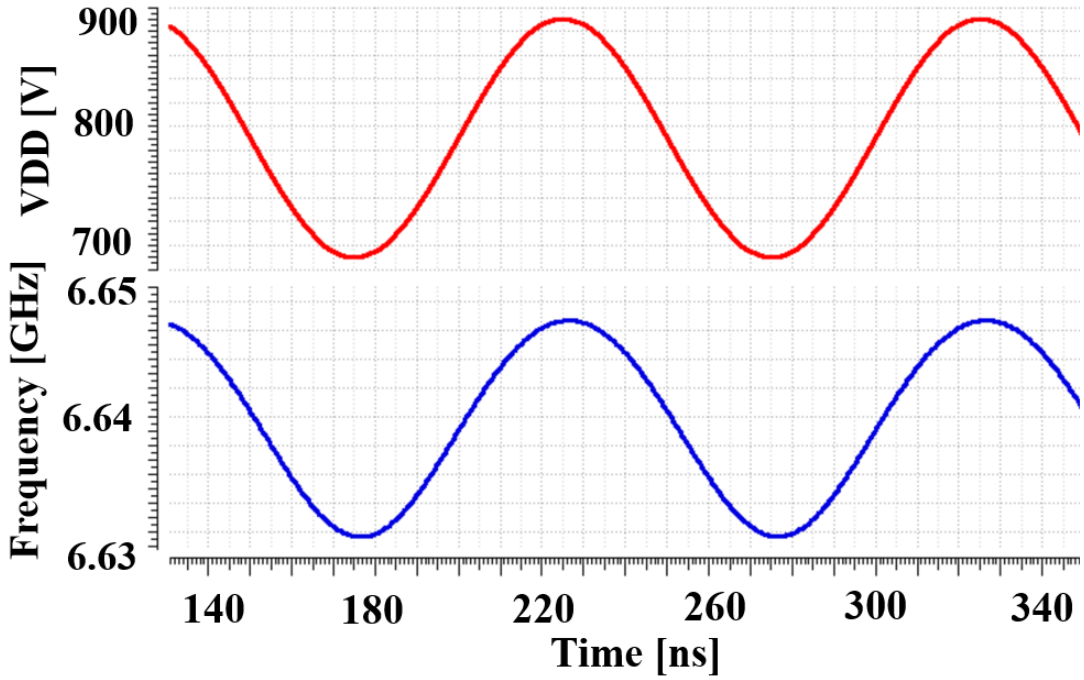


Figure 4.8: Oscillation frequency dependence on tail current while the supply is constant.

applied to the tail current while there is no noise on V_{DD} .

The main reason for this sensitivity is the nonlinear characteristic of C_{var} vs. voltage. When the oscillation amplitude varies due to variations in the tail current, the equivalent varactor capacitance might be slightly shifted, and hence, the oscillation frequency varies. This effect is described in Fig. 4.9.

4.2.3 Analysis of Sensitivity to Both Amplitude and Supply Variation

We have identified two sensitivity mechanisms that affect the oscillation frequency. The family of curves presented in Fig. 4.10 shows how the oscillation frequency varies with both the output common-mode level voltage and the tail current (oscillation amplitude).

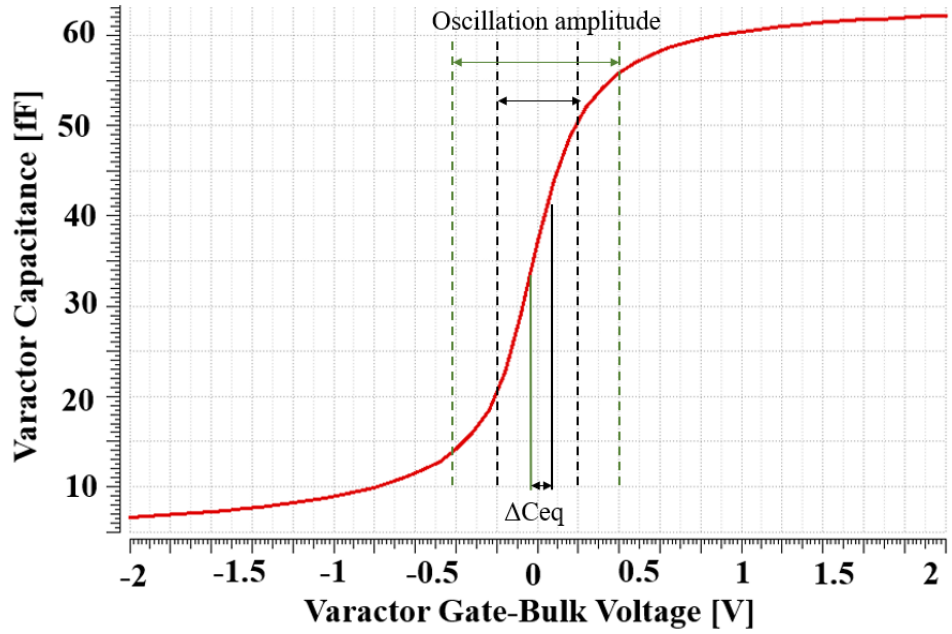


Figure 4.9: Nonlinear varactor capacitance vs. voltage characteristic.

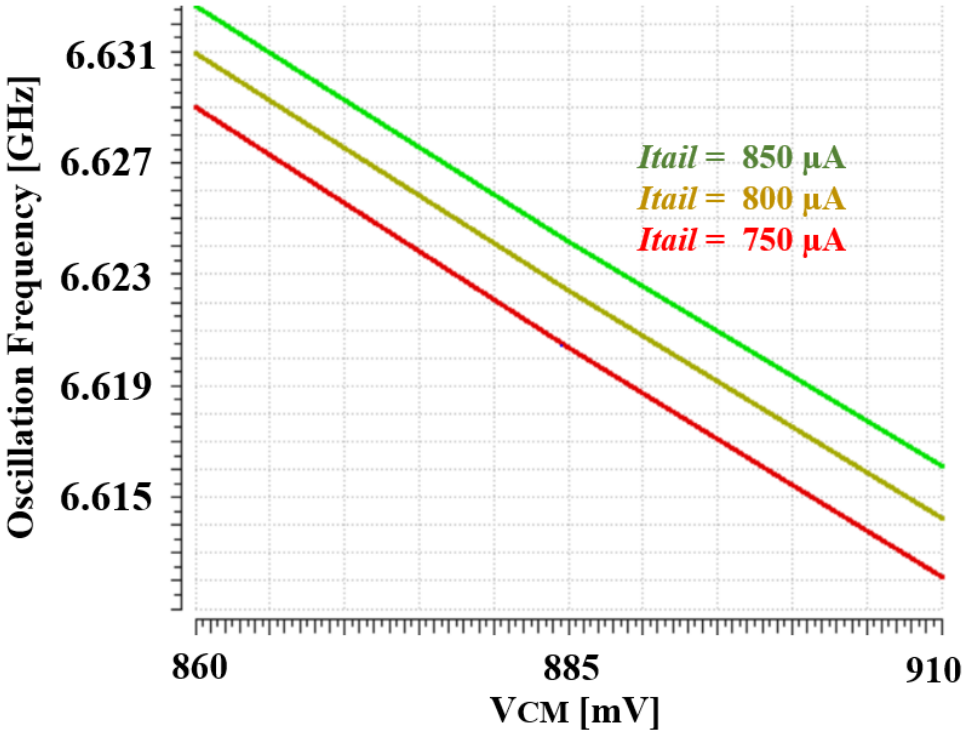


Figure 4.10: Family of curves indicating the oscillation frequency sensitivity to both common–mode voltage and tail current,

The sensitivity over V_{CM} is approximately -300 MHz/V which, as expected, is the negative of the Kvco. The oscillator also shows 44 GHz/A sensitivity due to variations in tail current, I_{SS}.

4.3 LC Oscillator Compensation Technique

In this section, we propose a compensation loop to reduce the overall sensitivity by compensating both sensitivity mechanisms.

4.3.1 Compensation Technique Formulation

The frequency sensitivity to the common-mode level and oscillation amplitude can be formalized as follows::

$$\frac{\Delta f_{osc}}{\Delta V_{DD}} = \frac{\Delta f_{osc}}{\Delta V_{CM}} \frac{\Delta V_{CM}}{\Delta V_{DD}} + \frac{\Delta f_{osc}}{\Delta I_{SS}} \frac{\Delta I_{SS}}{\Delta V_{DD}} \tag{4.2}$$

In a conventional oscillator architecture, a supply voltage disturbance normally has a rather small effect on the tail current due the channel length modulation effect. However, using a compensation circuit this effect can be exploited to reduce the overall sensitivity. The proposed circuit to achieve this is shown in Fig. 4.11 where a compensation loop modulates the tail current based on the V_{CM} disturbance. If we define G_{comp} as the total compensation loop transconductance, (4.2) can be expanded as:

$$\frac{\Delta f_{osc}}{\Delta V_{DD}} = \frac{\Delta f_{osc}}{\Delta V_{CM}} \frac{\Delta V_{CM}}{\Delta V_{DD}} + G_{comp} \frac{\Delta f_{osc}}{\Delta I_{SS}} \tag{4.3}$$

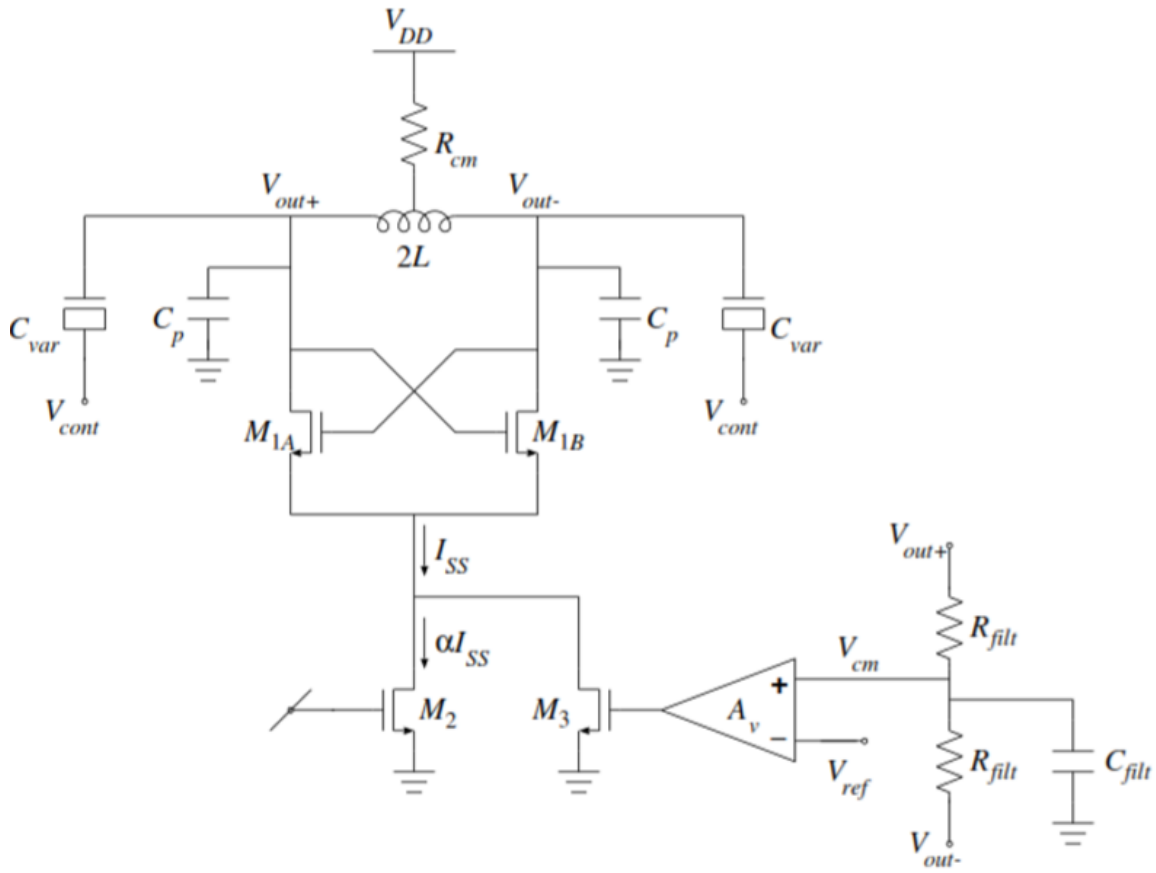


Figure 4.11: Proposed compensation loop architecture.

As shown before, Δf_{osc} / ΔV_{CM} = -K_{VCO} and ΔV_{CM} / ΔV_{DD} = 1. In order to minimize the supply sensitivity, we need to design G_{comp} as:

$$G_{comp} = \frac{K_{VCO}}{\frac{\Delta f_{osc}}{\Delta I_{SS}}} \tag{4.4}$$

For the designed VCO, $G_{comp} \approx 8$ mS can lead to the minimized supply sensitivity.

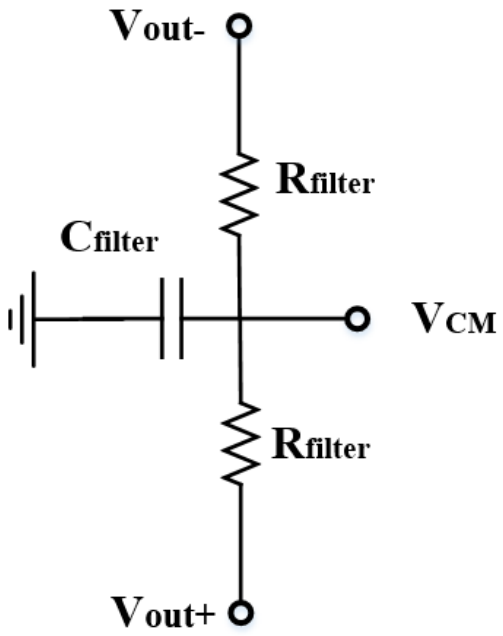


Figure 4.12: Compensation loop filter to extract the oscillator output common-mode voltage.

4.3.2 Loop Filter Characteristic

As proposed in the compensation technique, the oscillator differential outputs are fed back to the compensation path. However, in order to have access to V_{CM}, the the low-pass filtering circuit shown in Fig. 4.12 is used. The oscillation frequency tone is filtered but the supply disturbance should fully pass the filter providing common-mode variation based on only the noise frequency range.

4.3.3 Compensation Feedback Transconductance

In order to implement the transconductance feedback, a folded-cascode amplifier configuration shown in Fig. 4.13(a) can be used to keep the dc biasing constant as it provides a large gain of $g_m r_{out}$ at low frequencies. However, since a specific feedback gain G_{comp}

is needed, a series RC branch is implemented to control the gain in the higher frequency range as shown in Fig. 4.13(b). The RC branch moves the dominant pole to lower frequencies $1/(r_{out}C)$ while adding a zero at $1/(RC)$ to make the gain constant g_mR at higher frequencies. The ideal transfer function for this op-amp configuration is shown in Fig. 4.14(a). The added zero can cancel the phase delay, providing the feature to apply the amplitude change in-phase with the supply disturbance.

The optimal frequency compensation is achieved using $g_{m-opamp} = 600$ μS, $C = 20$ pF, and $R = 5$ kΩ for the op-amp, and $g_{m-tail} = 1.5$ mS , where g_{m-tail} is the compensation loop transconductance in the oscillator tail. Fig. 4.15 and Fig. 4.16 illustrate the frequency variation and eye closure with the same supply disturbance. An improvement of 87% can be seen in both frequency variation and jitter.

The op-amp magnitude and phase responses are analyzed in the frequency domain in Fig. 4.14(b). The secondary pole due to the current mirror should be pushed to higher frequencies. This will not only improve the compensation effectiveness, but also improves the stability of the loop which will be analyzed in the next section.

4.3.4 Compensation Loop Stability

In addition to the positive feedback implemented to create the oscillation, the added compensation loop creates a negative feedback loop, and hence stability analysis is required. The loop gain and phase, shown in Fig. 4.17, confirms 111° phase margin, which ensures the stability of the compensation loop.

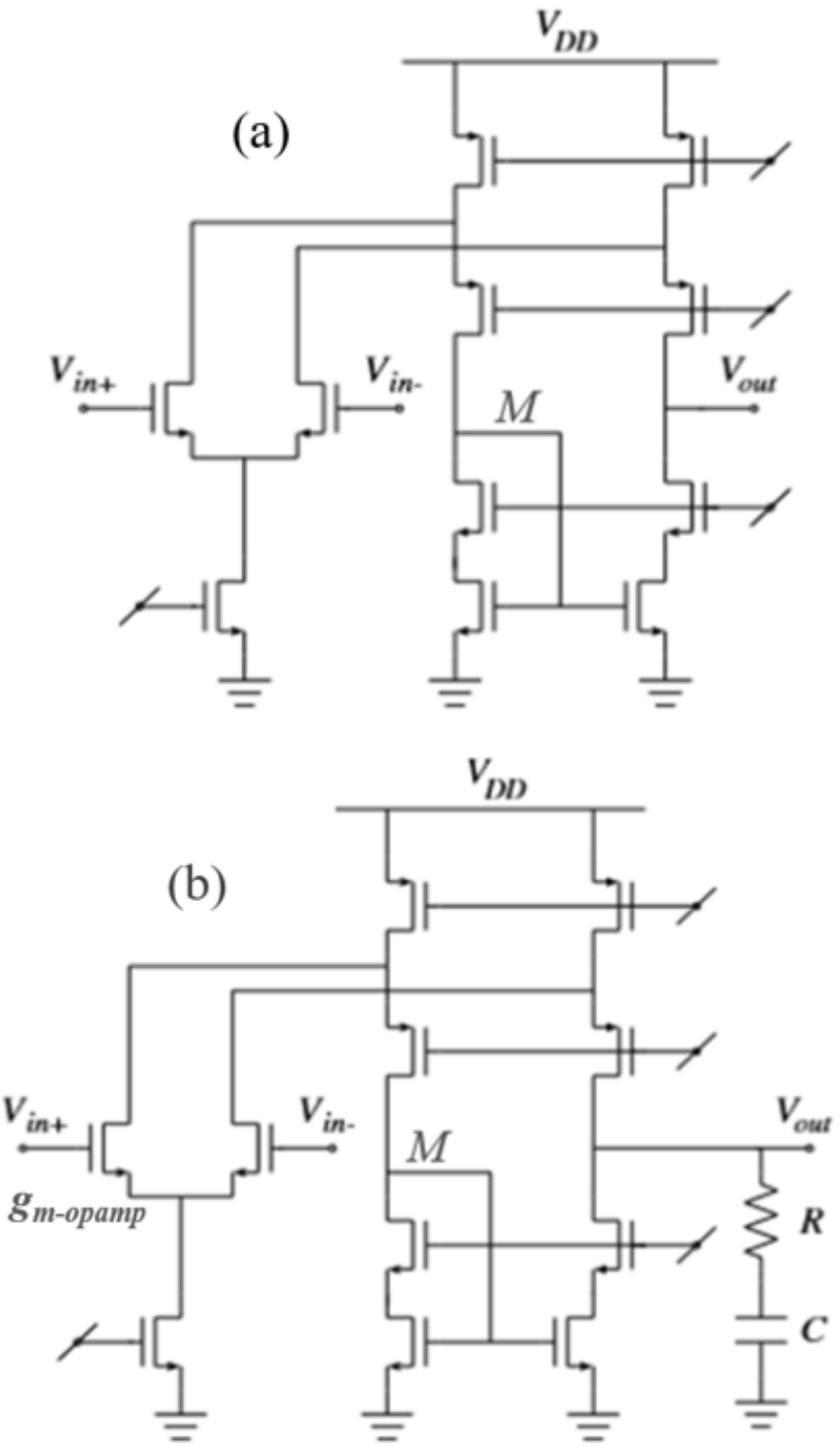


Figure 4.13: Proposed compensation loop op-amp architecture: (a) regular NMOS input pair folded-cascode op-amp; (b) folded-cascode op-amp with a zero added at the output node.

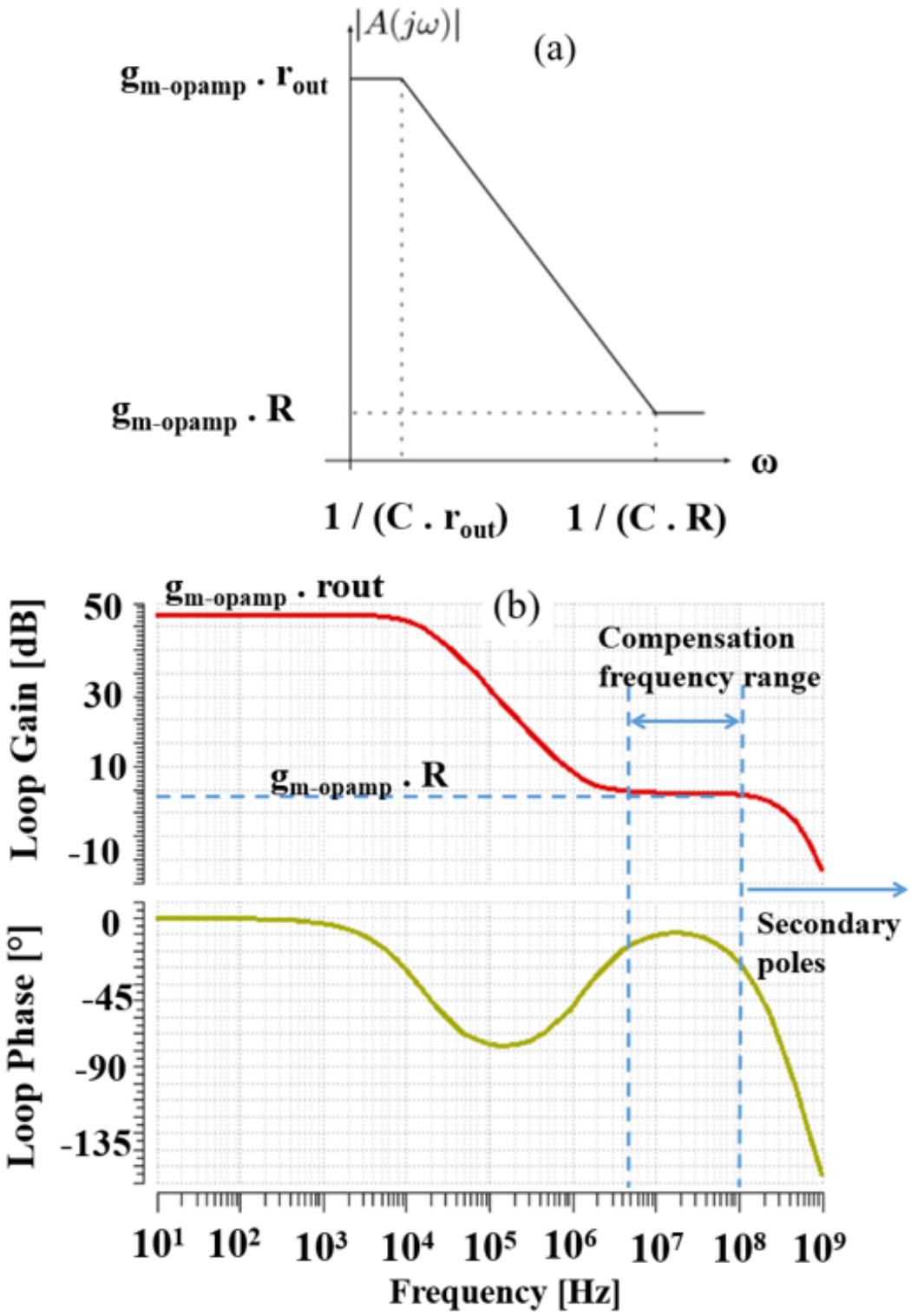


Figure 4.14: Compensation op-amp Bode plots: (a) ideal pole and zero effects (b) implemented op-amp.

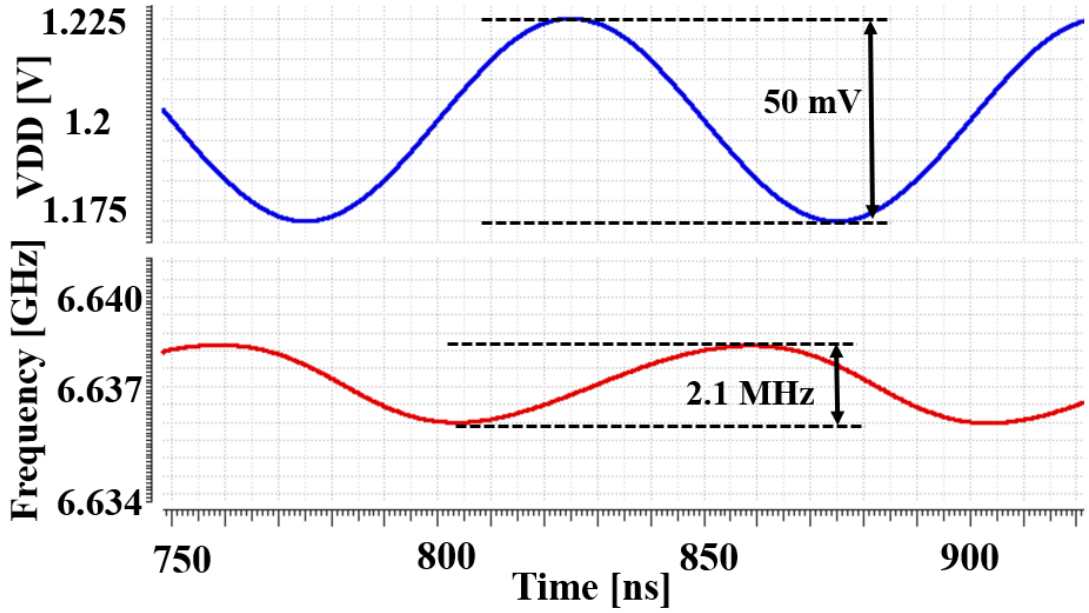


Figure 4.15: Frequency variation improvement using the proposed compensation loop.

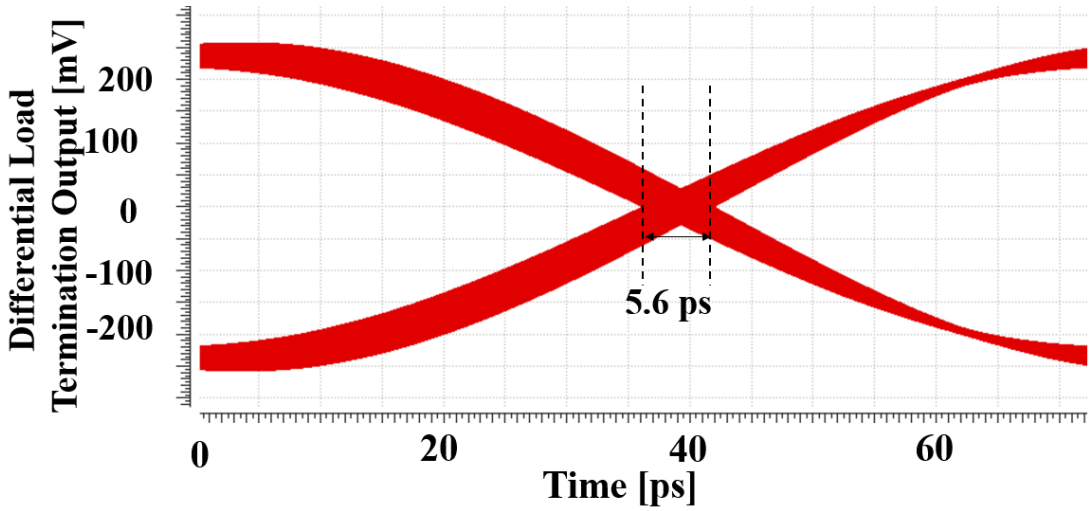


Figure 4.16: Eye diagram of compensated oscillator showing jitter improvement.

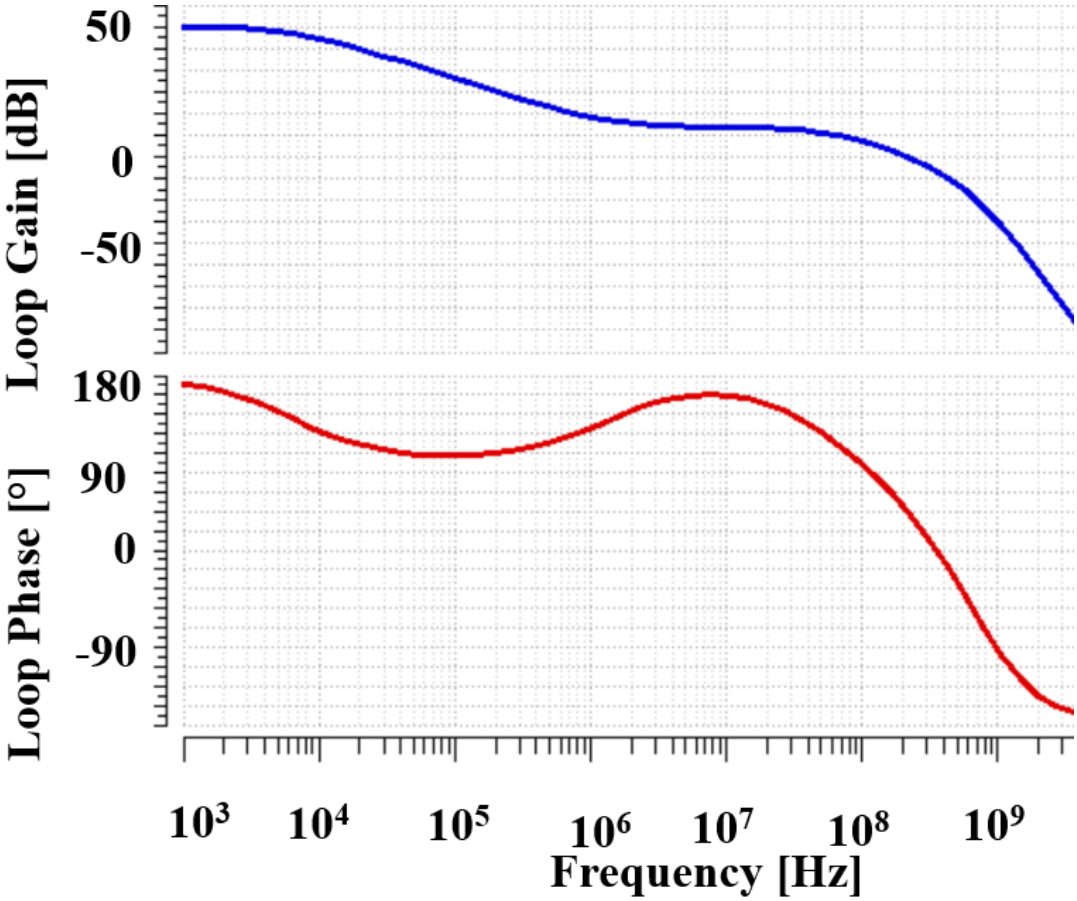


Figure 4.17: Loop gain and phase stability analysis

4.3.5 Additional Power Consumption

Despite the fact that compensation loop does not increase the tail dc bias of the core oscillator, the folded-cascode circuit design introduces 80 μA additional current consumption, which corresponds to 10% of the total current consumption. Compared to the voltage regulator, this compensation method consumes more current, however, as the voltage regulators pass the current from a higher voltage level, the compensation loop method can lead to less power consumption. In addition, it does not require an off-chip capacitor as is the case for the voltage regulator circuit.

4.3.6 Phase Noise

A drawback of adding the compensation loop is an increase in the number of noise-generating components. As shown in Fig. 4.18, the compensated oscillator exhibits 2 dB more phase noise compared to the uncompensated one at low offset frequencies. This phase noise degradation is negligible compared to 85-87% reduction of supply noise jitter, leading to more than 20 dB less overall phase noise.

4.3.7 One-time Calibration against Process Variation

As the process can vary, the designed oscillator sensitivity on tail current and common-mode voltage level can vary over the process corners. Therefore, a one-time calibration can be used to reach maximum compensation efficiency. This calibration could be done by trimming the op-amp gain using a programmable resistor ladder.

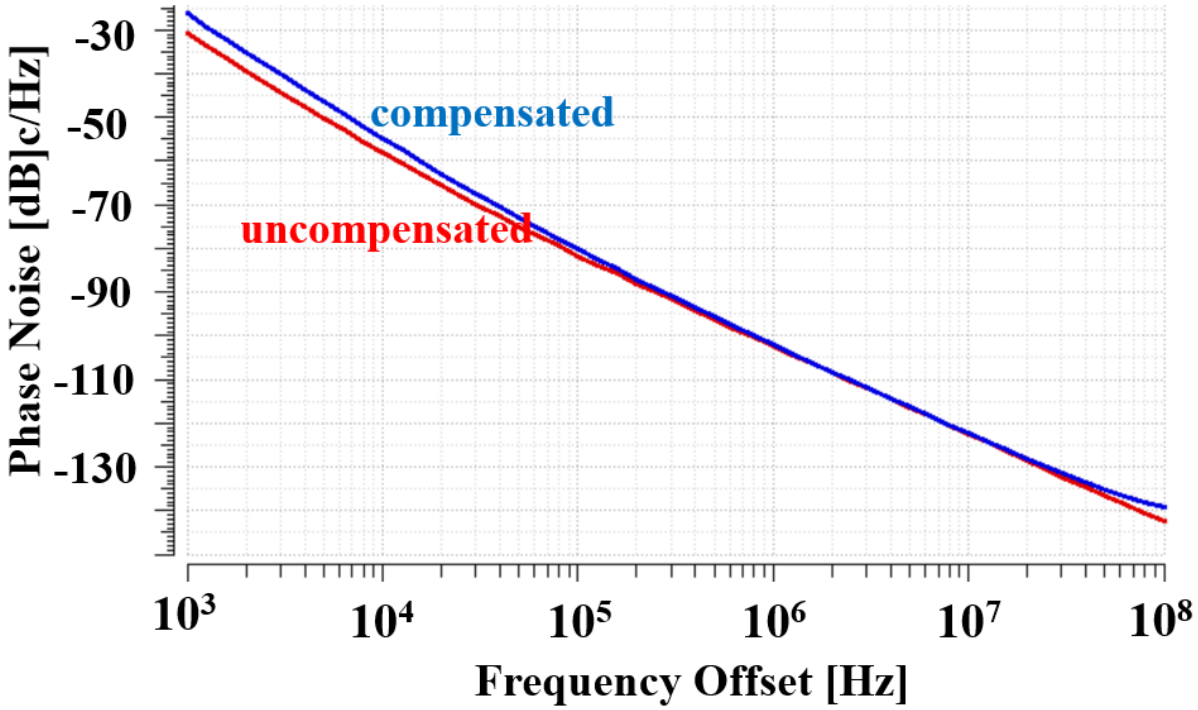


Figure 4.18: Uncompensated vs. compensated Phase Noise comparison.

4.3.8 Compensating the Complimentary (CMOS) Cross-Coupled Pair Architecture

The oscillator architecture discussed so far uses an NMOS cross-coupled pair only to generate the negative conductance in order to create the oscillation. Another commonly used architecture employs both an NMOS and a PMOS cross-coupled pair connected across the LC tank as shown in Fig. 4.19. This leads to a higher total negative conductance with the same amount of tail current. In order to verify the effectiveness of the proposed compensation technique, complimentary cross-coupled pair oscillator is designed to oscillate around 6.4 GHz with K_{vco} = 300 MHz/V respectively.

The compensation loop op-amp is redesigned to create a feedback factor required to compensate the sensitivity on the common-mode voltage and amplitude of oscillation. Using transient analysis with sinusoidal supply noise of 50 mVp-p at 10MHz, 86% improve-

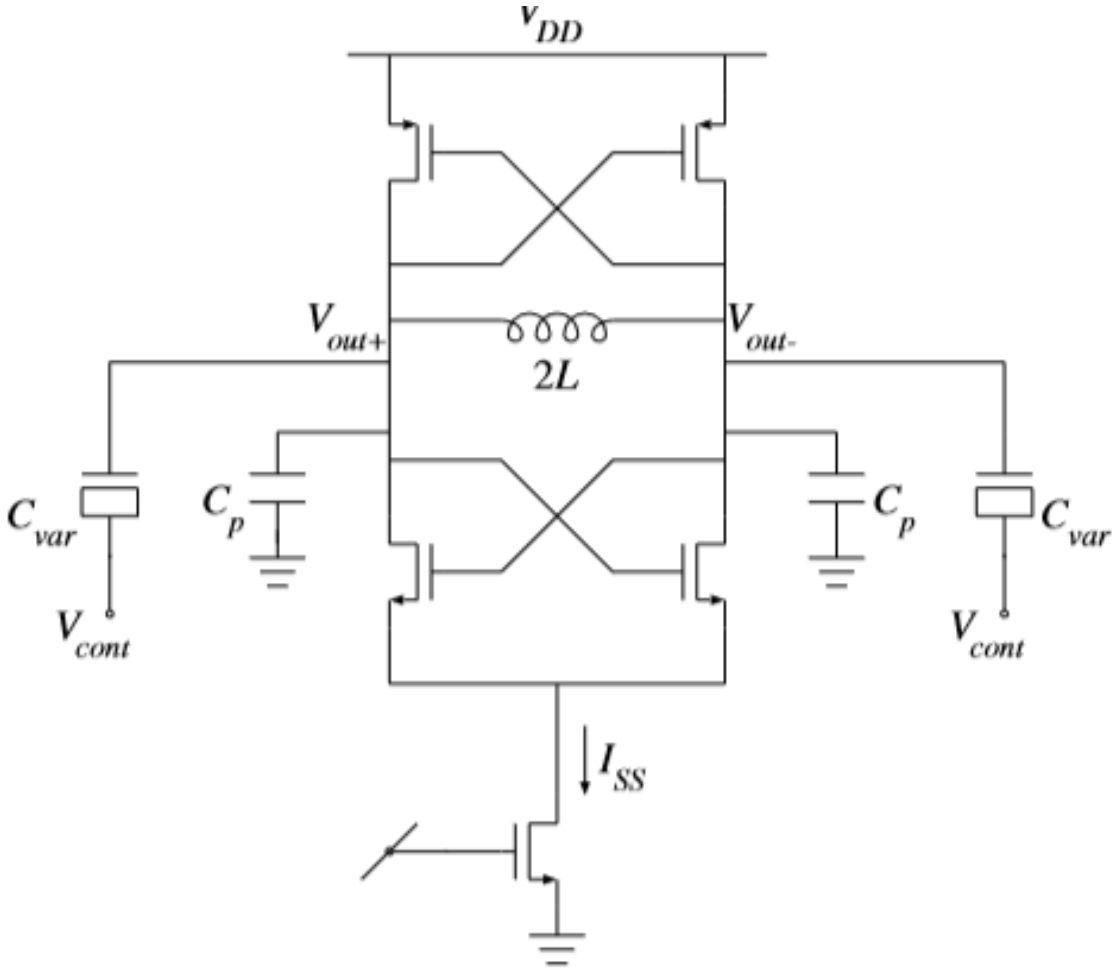


Figure 4.19: CMOS cross-coupled pair oscillator architecture

ment is achieved on both transient frequency as shown Fig. 4.20(a) vs. Fig. 4.20(b) as the frequency variation reduces from 16 MHz to 2.2 MHz after using the compensation method. Simulated jitter from the eye diagram leads to the same improvement as shown in Fig. 4.21(a) vs. Fig. 4.21(b). The compensated jitter is improved to 5.9 ps compared to 40.8 ps jitter in uncompensated oscillator. The LC resonance parameters are $L = 0.5$ nH, $C_p \approx 420$ fF (where C_{par} represents the parasitic capacitance and $C_{coarsetune}$ is the fixed capacitance at the output), while C_{var} varies between 36 and 60 fF. The tail current is set to 440 μA. The negative conductance generated by the NMOS and PMOS cross-coupled pair are 2.1 mS and 1.1 mS, respectively.

4.4 Conclusion

In this chapter, a compensation technique has been shown to reduce LC oscillators sensitivity to the supply noise. This method takes the advantage of dependency of the resonant frequency to both output common-mode voltage level and amplitude of oscillation to cancel out the sensitivity. This compensation loop amplifies the oscillation amplitude variation approximately in phase with the supply to compensate the variation due to the common-mode level. A reduction in jitter of 85-87% is verified with both the NMOS and CMOS cross-coupled pair architectures. The consideration of loop stability is analyzed together with the additional phase noise and current consumption.

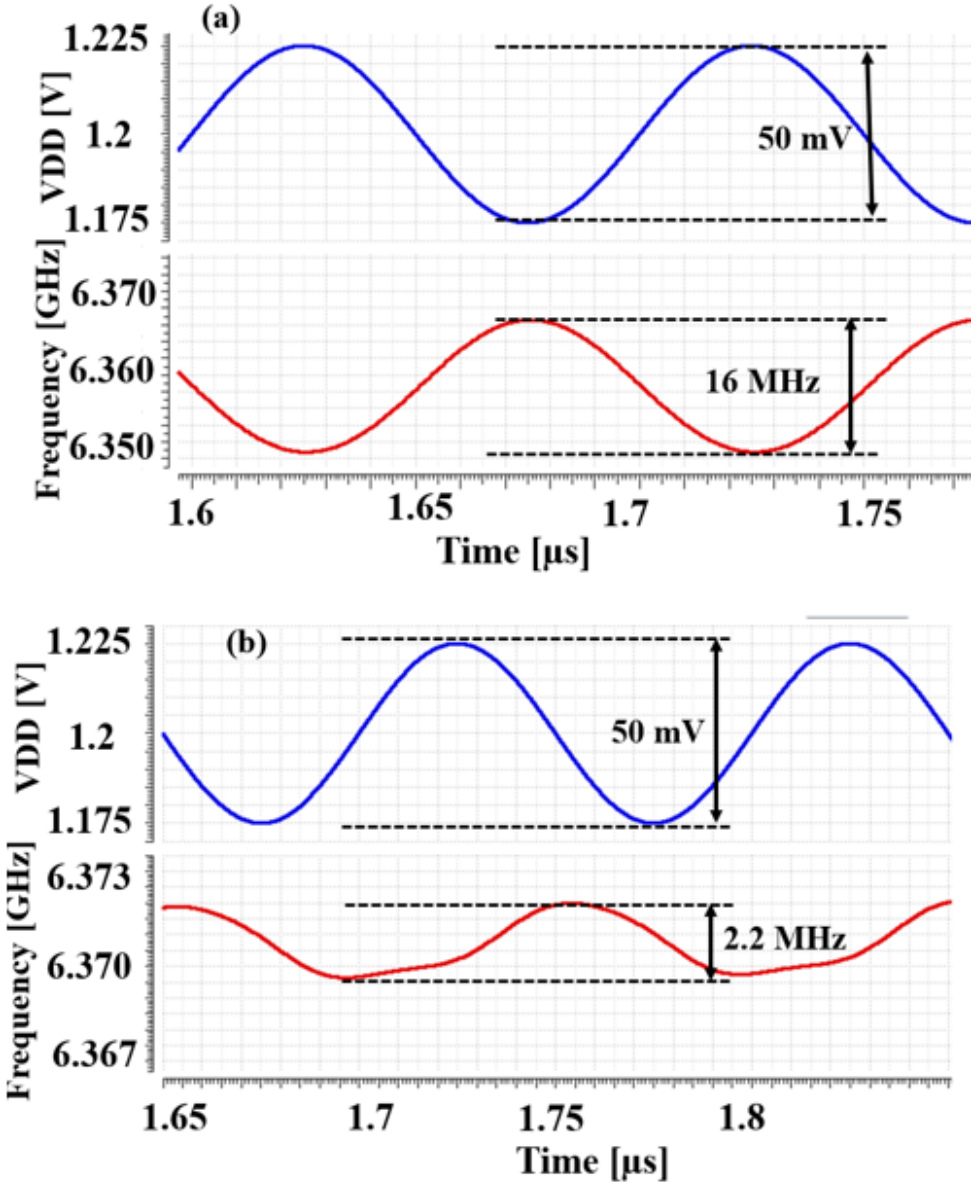


Figure 4.20: Cross-coupled pair oscillator sensitivity at 50 mVp-p sinusoid supply disturbance at 10 MHz: (a) uncompensated oscillator; (b) after applying the compensation technique.

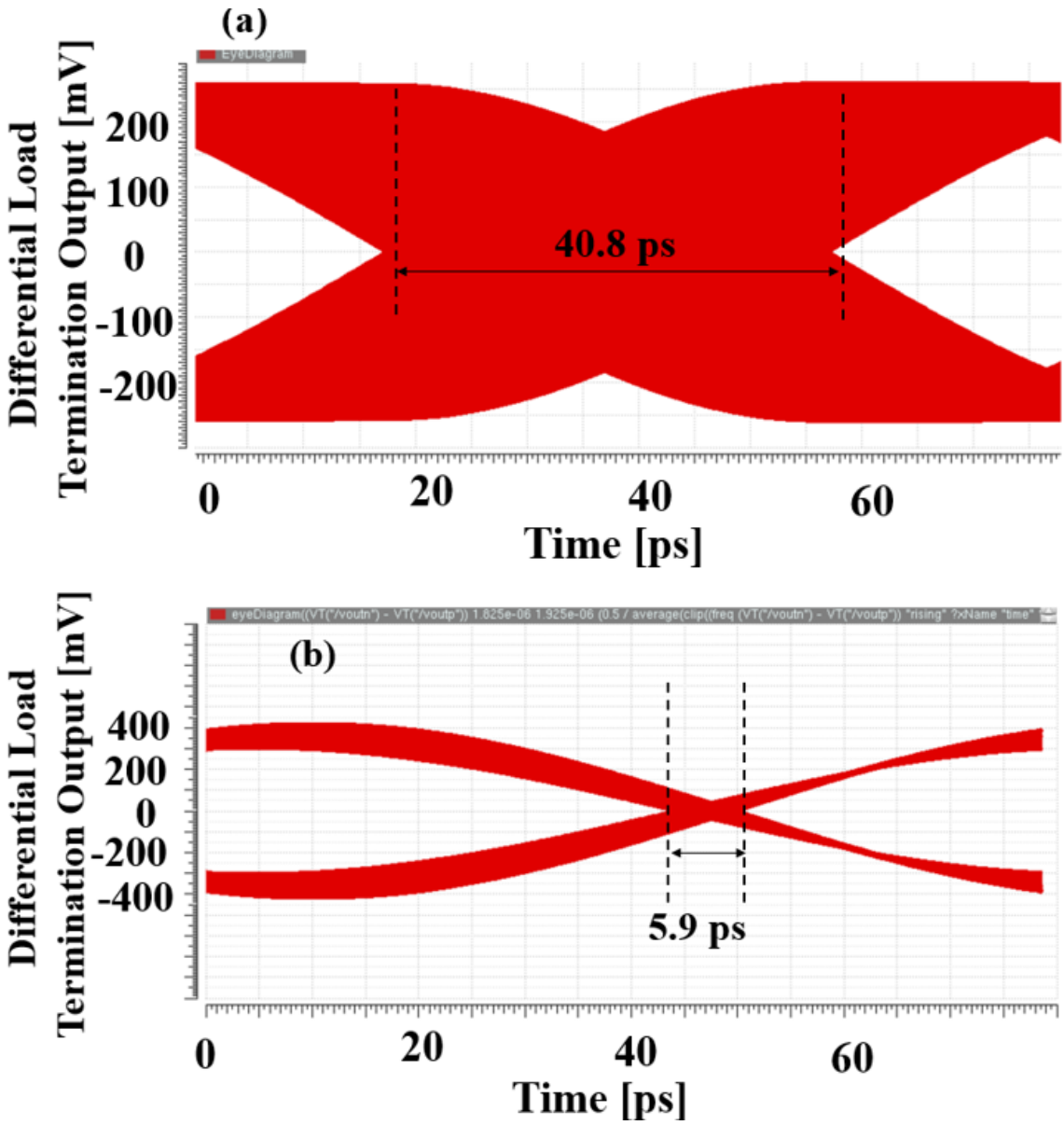


Figure 4.21: Cross-coupled pair oscillator eye diagram at 50 mVp-p sinusoid supply disturbance at 10 MHz: (a) uncompensated oscillator; (b) after applying the compensation technique.

Chapter 5

Conclusion

In this dissertation, circuit design techniques were developed to address new integrated circuit challenges introduced by the Internet of Things applications.

A delta-sigma system architecture was proposed and designed to measure the conductance over a range of four orders of magnitude. Its system model was developed in MATLAB to provide the behavioral performance and the operating range. The stability analysis was done both through the models and customizing noise transfer function method. The circuit design approach was presented in both block diagrams and transistor level. Each block was verified in separate test benches to ensure the performance. Eventually, $\pm 1\%$ accuracy was proven through chip measurement.

Next, a theoretical work introduced a new oscillator architecture based on DBE periodic structures. In this work, the fundamentals of LC resonator-based oscillators were reviewed. The DBE complex admittance was evaluated and the oscillator was created through designing a negative conductance active circuit. The oscillator shows low dependency on the termination load. Approximately 10 dB phase noise improvement was

verified through analog simulation. This architecture of oscillators does not need the additional buffer for the port termination. Hence, a reduction in the current consumption by a factor of 3 was proven compared to CML buffers. This dissertation covered the DBE oscillator design through lumped elements. Future works can use the waveguide implementation towards making these architectures more practical.

Finally, a new technique was developed to compensate the effect of supply noise on LC VCOs. The method was introduced by analyzing two different mechanisms of supply sensitivity in these oscillators, the output common-mode level and the oscillation amplitude. Then, a compensation loop was designed to use these two mechanisms to cancel each other. This technique was proven through analog simulations to reduce jitter and oscillation frequency variation by more than 85%.

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