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Modified Split-Phase Switching with Improved Fly Capacitor Utilization in a 48V-to-POL Dual Inductor Hybrid-Dickson Converter

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***Abstract*—This work demonstrates a modified split-phase switching scheme which maintains complete soft-charging operation when applied to a dual inductor hybrid-Dickson (DIH) switched-capacitor converter, while simultaneously greatly increasing the allowable fly capacitor voltage ripple and subsequent passive component utilization. Dissimilar to previous DIH split-phase demonstrations which sequentially introduce capacitive elements as a switching phase progresses, here all fly capacitors are inserted upon initialization of each phase, with select capacitors being disengaged before each phase's conclusion. As a result no switches experience a periodic reverse bias. This work includes analysis directing this insight along with a hardware prototype that achieves a peak efficiency of 93.8% (87.5%) at 750 kHz switching frequency, for 48V-to-3V(1V) conversion. Effective capacitor utilization and complete soft-charging is verified experimentally, and a power density of 54.4 kW/liter (892 W/inch^3) at 3 V output is recorded despite the use of stable Class I (C0G/NP0) dielectric capacitors and oversized inductors with minimal current ripple for simplified analysis.**

I. Introduction

With datacenter power consumption greatly increasing in recent years, there are strong incentives to adopt improved power delivery systems, with prominent server and cloud computing companies advocating for increased bus voltages beyond conventional 12V rails. This transition to 48V and higher bus architectures will be greatly facilitated through the development of DC-DC converters capable of highly effective voltage conversion at very large ratios. Attempting to fulfill this need, developments in the field of "hybridized switched-capacitor" converters (HSC) have yielded a number of topologies and converter techniques which demonstrate significant potential for improved power density, miniaturization, and associated cost reduction, with record-breaking performance metrics being reported in recent years (e.g. [1], [2]). One such topology, the dual inductor hybrid-Dickson (DIH) converter, discussed in [3]–[5] and depicted in Fig. 1, has received attention due to its minimal switch count, increased switch utilization, and convenient phase-shifted regulation capability. However, for even-order switched-capacitor networks of this type, a somewhat more complex switch clocking scheme, termed "split-phase switching" in [6], must be adopted to retain complete soft-charging of all fly capacitors [7]. This approach was successfully implemented in [4] and [5], however the manner in which split-phase clocking was applied resulted in fly capacitors experiencing a severe and systemic voltage ripple limitation, restricting ripple to an amplitude not greater than the switching devices reverse conduction threshold of ∼1V.

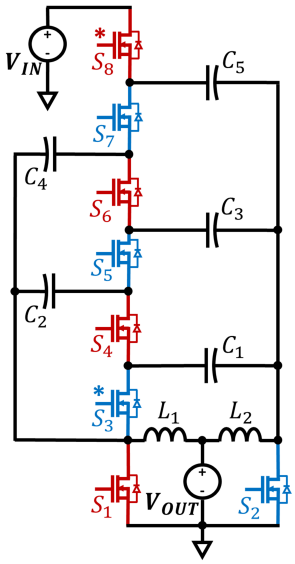


Fig. 1. Dual inductor hybrid-Dickson converter discussed in [3]–[5], here using a 6:1 HSC network. Switches requiring split-phase switching are marked with an asterisk (*), assuming all fly capacitors are equal in size.

In this work, we demonstrate an alternative split-phase clocking scheme applied to the same dual inductor hybrid-Dickson topology which does not exhibit the aforementioned voltage ripple limitation, allowing for significantly improved fly capacitor energy density utilization and subsequent improved power density.

II. Modified Split-Phase Switching

Previously demonstrated split-phase switching schemes have primarily focused on sequentially introducing capacitive elements throughout a phase upon realization of zero-voltage switching (ZVS) conditions ([1], [4]–[6], [8]). However, here we emphasize that in step-down HSC topologies it may often be preferable to perform this action in reverse: Instead, by controlling the time at which these elements are omitted, capacitor voltages may be directed such that all voltage loops are satisfied upon commencement of the subsequent switching phase, eliminating transient inrush currents and similarly enabling complete soft-charging. Importantly, as noted in [6] when considering a related fixed ratio converter, controlling switches in this way may remove the possibility of periodic reverse conduction in inactive switches: Subsequently, fly capacitor voltage ripple may be greatly increased for highly effective passive utilization, with all undesired reverse biasing constraints having been eliminated.

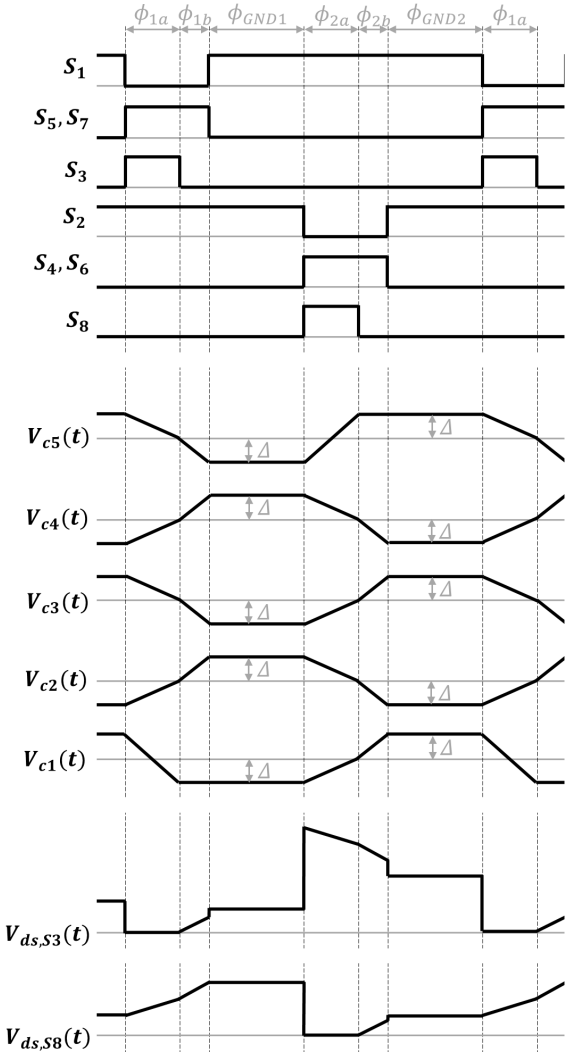
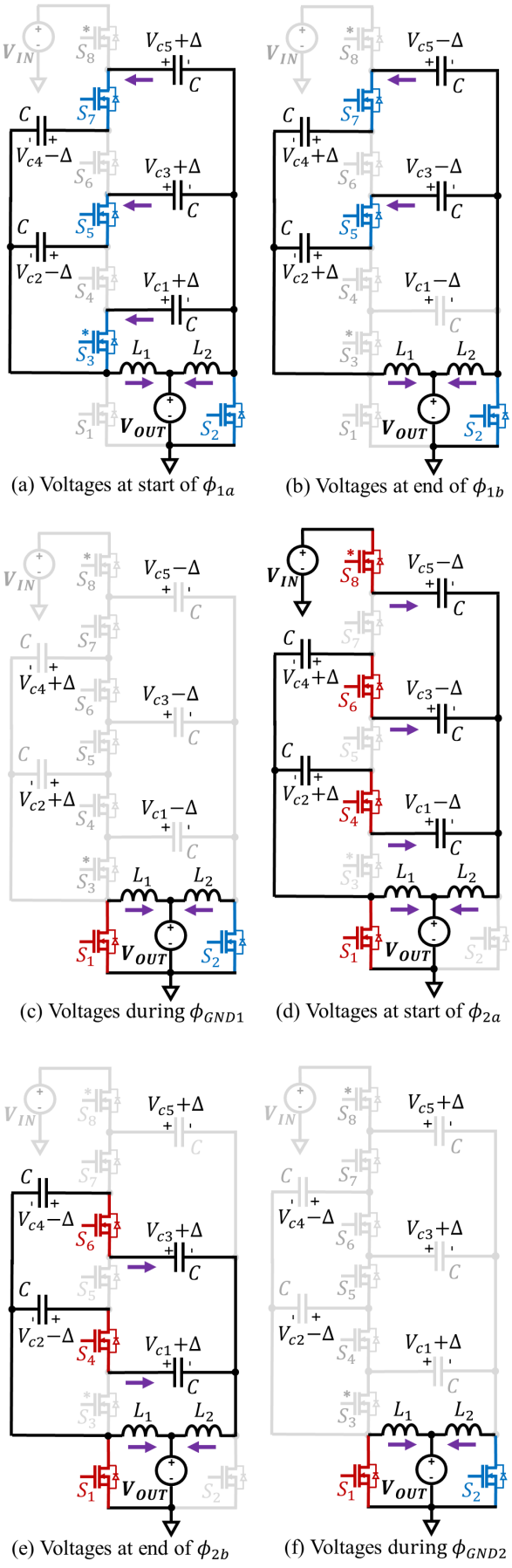


Fig. 2. Switch sequence and fly capacitor voltage waveforms of the proposed modified split-phase timing scheme.

Figures 2 and 3 depict the phase progression of the recommended modified split-phase switching scheme applied to a step-down DIH converter with an example 6:1 switched-capacitor network. Dissimilar to the clocking scheme demonstrated in [4] and [5] where select switches are turned *on*, here, switches S_3 and S_8 turn *off* part of the way through ϕ_1 and ϕ_2, thereby splitting these primary phases into sub-phases, $\{\phi_{1a}, \phi_{1b}\}$, and $\{\phi_{2a}, \phi_{2b}\}$ respectively. Doing so changes the slope of charge/discharge on fly capacitors C_{1-5} as the effective capacitance presented to inductors L_1 and L_2 is modified.

By applying the charge flow analysis described in [9] and [10], we can deduce that all fly capacitors must conduct equal quantities of charge per phase in steady-state. If we further choose to set all fly capacitors equal in size for simplicity, it follows that all capacitors experience identical voltage ripple, denoted here as $\pm\Delta$, albeit with opposite sign depending on the direction of charge flow. As such, Fig. 3 is also annotated with the fly capacitor voltages present at specified times, where V_{Cx} indicates the DC mid-range voltage present on capacitor C_x in steady-state operation and is a function of load [11].

To solve for all values of V_{Cx}, and subsequently derive load dependent switch stress, the techniques described in [6] and Chapter 5 of [11] may be extended to this topology, but is beyond the scope of this paper. Here, instead we assume



(a) Voltages at start of ϕ_{1a} (b) Voltages at end of ϕ_{1b}

(c) Voltages during ϕ_{GND1} (d) Voltages at start of ϕ_{2a}

(e) Voltages at end of ϕ_{2b} (f) Voltages during ϕ_{GND2}

Fig. 3. Phase progression of proposed modified split-phase timing scheme applied to a dual inductor hybrid-Dickson with a 6:1 HSC network. (a) Phase ϕ_{1a}, (b) ϕ_{1b}, (c) Phase ϕ_{GND1}, (d) Phase ϕ_{2a}, (e) Phase ϕ_{2b}, (f) Phase ϕ_{GND2}. Fly capacitor voltages at the times noted are annotated.

that inductor current ripple is small, as would be the case in deep continuous conduction, and focus on deriving the relative phase durations of ϕ_{xa} and ϕ_{xb} required to preserve complete soft-charging. Since only one inductor is interacting with the capacitor network at any given point in time, should this analysis wish to be revisited accounting for non-negligible inductor current ripple, only temporal relationships will be altered with the capability for complete soft-charging being retained[1]. Assuming $\Delta i_{Lx} \simeq 0\ A$, capacitor voltages change linearly as depicted in Fig. 2.

Regarding Fig. 3 (a) and (b), here we observe that during ϕ_1, L_1 must charge/discharge all fly capacitors by 2Δ. Since $\{C_2, C_3\}$ and $\{C_4, C_5\}$ are series connected pairs, we note that each of these series branches requires a net change of 4Δ. Since C_1 begins ϕ_{1a} wired in parallel with both of these branches, and yet only requires a 2Δ change, the necessity for split-phase switching is made obvious with C_1 needing to be removed from the charging path half-way through the total voltage swing. At this moment, S_3 turns off and C_1 is removed from the charging path, where it maintains $(V_{C1} - \Delta)$ until ϕ_{2a} (Fig. 3 (d)). That is, ϕ_{1a} ends, and ϕ_{1b} begins, at the exact moment C_1 reaches $(V_{C1} - \Delta)$. The two remaining branches complete their additional 2Δ voltage change over the course of ϕ_{1b}.

Although this 'split' occurs half-way through a 4Δ voltage swing, as observed by inductor L_1, this does not imply that both sub-phases are equal in duration: Once C_1 has been removed from the charging path, the effective capacitance seen by L_1 decreases, and so dv/dt increases, shortening the time required to complete the remaining 2Δ change.

In summary, assuming constant current in L_1 and equal fly capacitor values (C), the duration of ϕ_{1a} may be expressed as

$$t_{\phi 1a} = \frac{(C_{Eff,\phi 1a})(2\Delta)}{I_{L1}} = \frac{(2C)(2\Delta)}{I_{L1}}, \tag{1}$$

where $C_{Eff,\phi 1a}$ is the combined effective capacitance seen by L_1 during ϕ_{1a}.

Similarly,

$$t_{\phi 1b} = \frac{(C_{Eff,\phi 1b})(2\Delta)}{I_{L1}} = \frac{(C)(2\Delta)}{I_{L1}}, \tag{2}$$

where $C_{Eff,\phi 1b}$ is the remaining effective capacitance seen by L_1 during ϕ_{1b} after C_1 has been omitted.

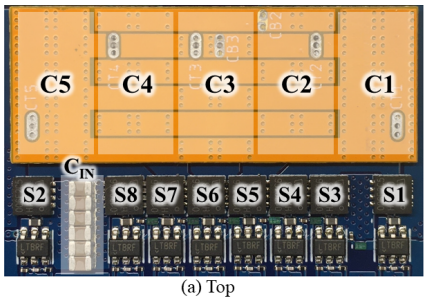
Note that as ϕ_{1b} progresses, the V_{DS} of switch S_3 increases from 0V (see Fig. 2), and as such there is no reverse conduction voltage threshold limitation, allowing fly capacitor voltage ripple to be very large in practice. Conversely, if the order of phases ϕ_{1a} and ϕ_{1b} were reversed, with C_1 instead observing its 2Δ swing during the latter half of ϕ_1, complete soft-charging would still be theoretically achievable, but in this case S_3 would witness a negative V_{DS} bias, restricting allowable voltage ripple to be less than the reverse conduction threshold of the switching devices (as was observed in [5]).

The same result is obtained for ϕ_2 where S_8 turns off early. Combining (1) and (2), we see that to achieve complete soft-charging in a 6:1 HSC network, assuming small inductor current ripple, both phases require a split-phase segmentation ratio of

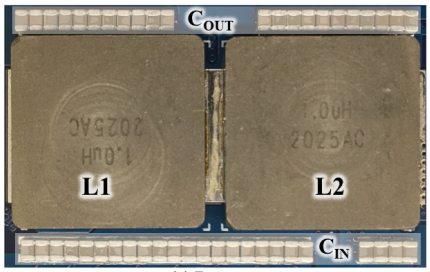
$$t_{\phi xa} \simeq 2t_{\phi xb}. \tag{3}$$

where this is the same result achieved in [5], but with reverse phase ordering.

[1]In [5], inductor current ripple was analysed, but the presented analysis instead assumed zero fly capacitor voltage ripple, although this assumption is largely justified given the aforementioned severe ripple limitations with this earlier clocking scheme. Should both inductor and capacitor ripple wish to be accounted for, the analysis becomes more involved.



(a) Top



(a) Bottom

Fig. 4. Photograph of the constructed prototype measuring 23.2mm × 35.5mm × 5.7mm.

III. Hardware Implementation and Results

To validate the performance of the proposed approach, a hardware prototype using discrete components was designed, fabricated, and tested. Figure 4 shows an annotated photograph of the prototype, which measures 0.286 inch^3 (4.687 cm^3) by the largest box that completely encompasses the converter. The total volume of the power stage components (fly capacitors, inductors, and switches) is 0.168 inch^3 (2.756 cm^3).

Each fly capacitor, comprised of 64×10 nF capacitors to better fit the overall converter box volume, was pre-assembled on a 0.2 mm thick FR4 daughter-board. Despite their reduced energy density relative to Class II dielectrics, Class I (C0G) fly capacitor dielectrics were used here for accurate component matching to better exemplify the proposed technique, with the added benefits of improved loss factor and stability with age, temperature and voltage [12], [13]. Moreover, as shown in [14], [15], the losses of Class II dielectrics under voltage bias and with large voltage ripple can be significantly higher than datasheet values. At $1\,\mu H$ each, inductors L_1 and L_2 were greatly oversized to approximate near zero-current ripple conditions and thus better match the calculated split-phase duration described by (3). As such, split-phase timing was controlled such that ϕ_{xa} and ϕ_{xb} maintained a 2:1 duration ratio. Silicon MOSFETs were used here given their comparable performance to Gallium Nitride within this voltage range. Each switching device was controlled by an independent level-shifting gate driver with power being delivered to all high-side switches using a conventional cascaded bootstrap, as shown in Fig. 5. Specific component details are listed in Table I, with a total volume breakdown depicted in Fig. 6.

With a fixed 48V input, maximum output powers of 150W, 120W, and 70W were recorded for output voltages of 3V, 2V,

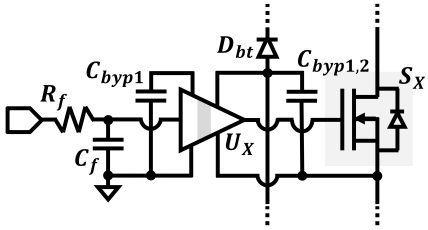


Fig. 5. Schematic of gate drive circuitry used for each switching device.

TABLE I
COMPONENT DETAILS

Components	Details	Part Number
$C_{1\text{-}5}$	64× 10 nF, 50V, C0G, 0603	GRM1885C1H103JA01D
$L_{1\text{-}2}$	1 μH, 1.86 mΩ, 41A	IHLP-6767DZ-11
$S_{1\text{-}2}$	0.65 mΩ, 25V, NMOS	IQE006NE2LM5CGATMA1
$S_{3\text{-}8}$	1.35 mΩ, 40V, NMOS	IQE013N04LM6CGATMA1
C_{IN}, C_{OUT}	30×, 22× 4.7 μF, 50V, X5R, 0805	CL21A475KBQNNNE
$U_{1\text{-}8}$	80V isolation, 1.5Ω, 2.4A	LTC4440
C_{byp1}	0.1 μF, 25V, X5R, 0201	C0603X5R1E104K030BB
C_{byp2}	2.2 μF, 16V, X5R, 0402	C1005X5R1V225K050BC
D_{bt}	Schottky, 0.5A, 30V, 0402	VSKY05301006
C_{f}	20 pF, 50V, C0G, 0201	GRM0335C1H200JA01D
R_{f}	100 Ω, 1%, 1/20W, 0201	RMCF0201FT100R

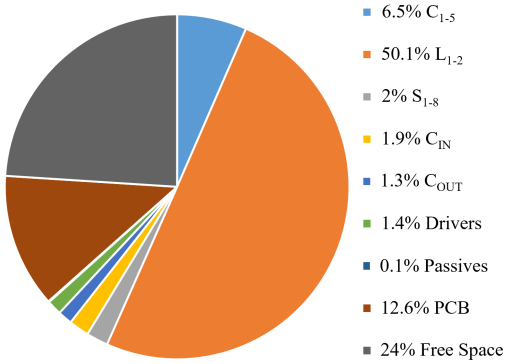


Fig. 6. Volume breakdown of a best-fit cuboid encompassing the constructed prototype. Oversized inductors consume half of the converter, with PCB and empty space consuming over 73% of the remaining volume.

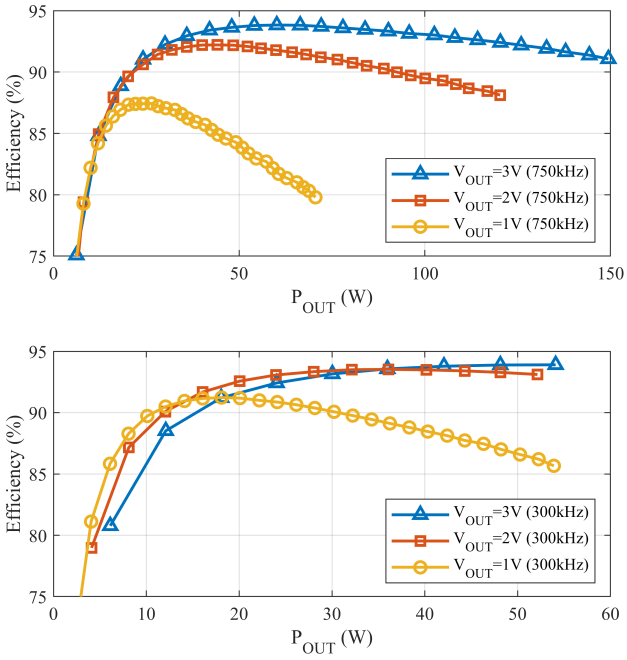
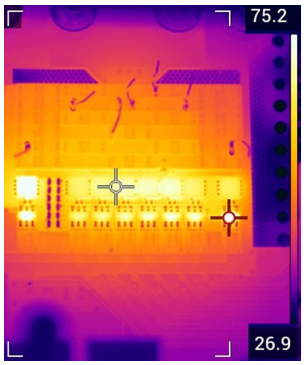


Fig. 7. Measured efficiency curves for $V_{IN} = 48V$ and switching frequencies of 750 kHz (top) and 300 kHz (bottom). At 750 kHz, the maximum output power is limited by the available load-bank, whereas at 300 kHz P_{OUT} is limited by the maximum allowable fly capacitor voltage swing being reached.



ESTIMATED LOSS BREAKDOWN

Loss Mechanism	%
Conduction & Overlap	76
Gating	13
C_{OSS}	11
Total Loss	**18.7W**

Fig. 8. Thermal image and estimated loss breakdown of the discrete prototype performing 48V-to-2V conversion at $f_{SW} = 750$ kHz and $I_{load} = 60$ A.

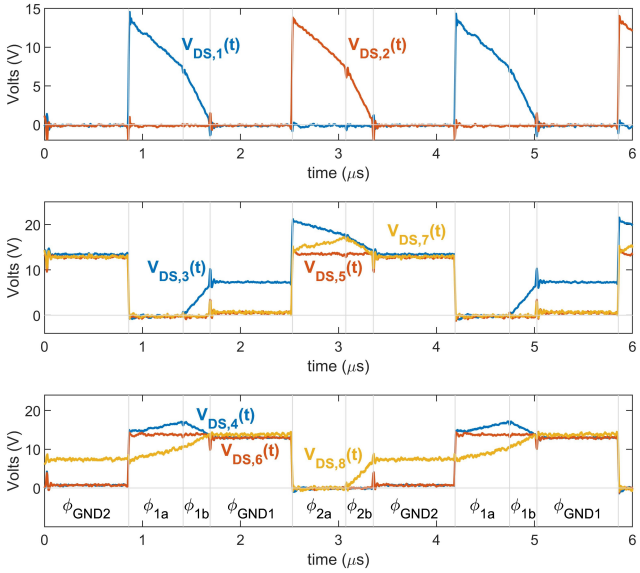


Fig. 9. Measured switch stress waveforms at the maximum allowable voltage ripple. All switches are positively biased when blocking, eliminating the operational dependency on reverse conduction voltage thresholds observed in [5]. $f_{SW} = 300$ kHz, $I_{load} = 26\ A$, and $V_{OUT} = 2V$.

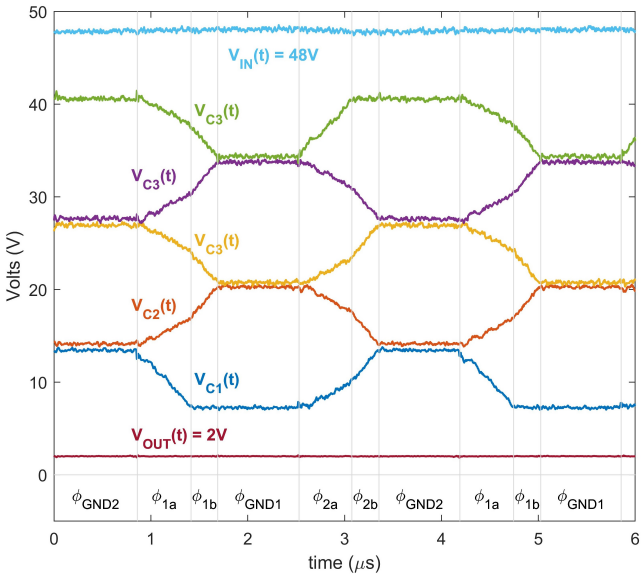


Fig. 10. Measured waveforms exhibiting large voltage ripple ($\sim 6\,V$) across all fly capacitors, implying effective passive utilization. The absence of any abrupt voltage transitions illustrates complete soft-charging operation. $f_{SW} = 300$ kHz, $I_{load} = 26\ A$, and $V_{OUT} = 2V$.

TABLE II
COMPARISON WITH PRIOR WORK

	APEC 2017 [16]	TIA 2019 [5]	COMPEL 2019 [17]	COMPEL 2020 [18]	**This work**
Conversion Ratio:	48V to 1V	48V to 1V-2V	54V to 1.5V	48V to 1V-2.5V	**48V to 1V-3V**
Topology:	Sigma (DCX + Buck)	DIH	LEGO-PoL	MLB-PoL	**DIH**
Switch Type:	GaN FET	GaN FET & Diode	MOSFET	MOSFET	**MOSFET**
f_{SW} :	600 kHz	300 kHz	500 kHz	250 kHz	**750 kHz**
Inductor:	36 μH & 190 nH	2 × 1.5 μH	12 × 1 μH	2 × 600 nH	**2 × 1 μH**
Peak Efficiency: (excl. Gating Loss)	93.5% @1V	95.02% @2V 93% @1V	93.1% @1.5V	95.6% @2.5V 95.1% @2V 93.1% @1V	**93.8% @3V** **92.2% @2V** **87.5% @1V**
$P_{OUT\text{-}MAX}$:	80 A @1V	10 A @2V 10 A @1V	300 A @1.5V	65 A @2.5V 65 A @2V 65 A @1V	**50 A @3V** **60 A @2V** **70 A @1V**
Efficiency @ $P_{OUT\text{-}MAX}$: (excl. Gating Loss)	92% @1V	94.5% @2V 92.3% @1V	78% @1.5V	92.1% @2.5V 91.3% @2V 86.8% @1V	**91.1% @3V** **88.1% @2V** **80% @1V**
Component volume[a]	-	1.436 cm^3	5.859 cm^3	1.842 cm^3	**2.756 cm^3**
Power Density[a]: (W/$inch^3$)	-	228 @2V 114 @1V	1,259 @1.5V	1,445 @2.5V 1,156 @2V 578 @1V	**892 @3V** **715 @2V** **422 @1V**
Power Density[b]: (W/$inch^3$)	420 @1V	-	152 @1.5V	494 @2.5V 395 @2V 198 @1V	**524 @3V** **419 @2V** **246 @1V**

[a]Considering power stage components only (fly capacitors, inductors, switches, and diodes).
[b]Best-fit cuboid encompassing entire converter solution.

and 1V respectively when switching at 750 kHz. Measured efficiency curves for operation at both 750 kHz and 300 kHz are depicted in Fig. 7 and do not include an additional gate-drive power consumption of 3.2 μW/Hz. While switching at 750 kHz, the maximum achievable output power was limited by the available load bank, with the operational temperature never exceeding 80°C (Fig. 8). Conversely, at 300 kHz the maximum output power was limited by fly capacitor voltage swing: Although the limitations on fly capacitor voltage ripple have been greatly relaxed with the presented modified split-phase switching scheme, as ripple increases further a subsequent ripple constraint is imposed by S_1 and S_2 whose V_{DS} tends towards 0 V at the ends of ϕ_{1b} and ϕ_{2b} respectively. If power through-put is to be increased further, capacitor sizes or switching frequency must be increased to reduce Δ such that S_1 and S_2 do not undergo a reverse bias. Figures 9 and 10 depict measured waveforms taken at this new relaxed bound, with V_{DS1} and V_{DS2} each reaching a minimum blocking voltage of 0V before transitioning to ϕ_{GND1} and ϕ_{GND2} respectively. Additionally, in Fig. 10 we observe a large maximum fly capacitor voltage ripple of $\sim$6 V, approximately an order of magnitude larger than that reported in [5], demonstrating greatly improved utilization of the energy stored on the fly capacitors. Moreover, the absence of any abrupt changes in capacitor voltage signifies complete soft-charging and highly efficient energy transfer. Lastly, Table II documents this prototype's results in contrast with several comparable works.

IV. CONCLUSION

In summary, here we have demonstrated a modified split-phase clocking scheme that alleviates reverse conduction limitations and greatly increases the allowable fly capacitor voltage ripple in step-down applications, subsequently resulting in improved passive component utilization. The described time-reversed implementation of split-phase switching, where fly capacitors are omitted as opposed to introduced during a switching phase, is expected to be the preferred approach in a number of step-down topologies requiring split-phase functionality for complete soft-charging operation.

A discrete state-of-the-art prototype provides measured waveforms that verify expected operation and yields a very satisfactory power density of 892 W/$inch^3$ at 750 kHz switching frequency and 3 V output despite the use of low density Class I dielectrics and excessive inductance for simplified analysis. As such, further improvement is expected in future revisions.

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