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25Gb/s hybrid silicon switch using a capacitively loaded traveling wave electrode

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Abstract: We demonstrate a hybrid silicon modulator and switch operating up to 25 Gb/s with over 10 dB extinction ratio. The modulator has voltage-length product of 2.4 V-mm while the switch has switch time less than 35 ps and crosstalk smaller than -12 dB.

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OCIS codes: (250.4410) Modulators; (250.5300) Photonic integrated circuits; (250.7360) Waveguide modulators.

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1. Introduction

The routing of data electronically within microprocessors is becoming increasingly challenging due to the large volumes of data being transferred. Optical interconnects on silicon are an attractive alternative to traditional electronic interconnects because they provide higher bandwidth and have the potential to be compatible with low cost, high volume, mature CMOS processing. One of the bottlenecks to exploit the tremendous capacity of an optical interconnect is the efficiency and the speed of the modulation device that impresses the electrical data onto the optical signal. In addition, a wide optical bandwidth is necessary if a wavelength division multiplexing (WDM) signal is used. Various optical modulators in silicon have been reported with differing tradeoffs. A Silicon ring resonator was first demonstrated as a modulator with the benefit of having an extremely small foot print [1]. However, it is hard to achieve operation over several Gb/s due to the limitation of carrier injection effect. A Mach-Zehnder modulator (MZM) utilizing carrier depletion effect can bring the modulation speed up to 40 Gb/s and usually has an optical bandwidth over 30 nm [2]. In addition to ring resonators and MZMs, electroabsorption modulators (EAM) are another candidate for realizing high speed operation with reasonable optical bandwidth

(usually $\sim 30\text{nm}$). Due to the well known limitations of silicon, materials such as Ge and III-V are used in conjunction with Si to get a more efficient electro-optic effect. SiGe EAMs were demonstrated to be very compact with drive voltages around 7 V and a 3 dB cutoff frequency of 1 GHz [3]. In order to achieve high speed operation within a small footprint while still maintaining CMOS compatibility, we utilize a hybrid approach: III-V (InP) material wafer-bonded to silicon at low temperature. The idea is to use effects inside the III-V materials for phase or amplitude change. We reported an EAM on this platform that had 10 dB extinction ratio (ER) at 10 Gb/s with 3.2 V swing, 16 GHz modulation bandwidth and 30 nm optical bandwidth [4]. Also, we demonstrated a hybrid MZM incorporating a traveling wave electrode (TWE) design [5]. Here, the dominant physical effect exploited for index change was carrier depletion inside the multiple quantum wells (MQW) [6]. This hybrid MZM had a 6 dB ER at 10 Gb/s with 3 V swing, 4 V-mm modulation efficiency and over 100 nm optical bandwidth [6]. In this paper, we present a new TWE design to achieve higher speed operation. We demonstrate large signal modulation up to 25 Gb/s with 10 dB ER. The 2x2 switches with this new design were characterized at 40 Gbit/s and have a switching time as fast as 35 ps. These silicon components with higher modulation bandwidth and wide optical bandwidth enable high speed interconnects for future optical communication.

2. Device design

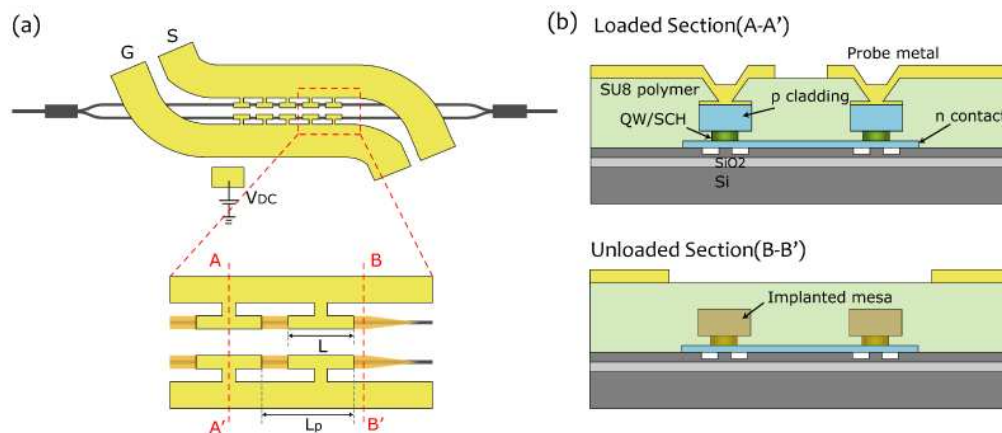


Fig. 1. (a) Top view of a device with a CL slotline electrode (b) Cross section of loaded (along A-A') and unloaded sections (along B-B') of the hybrid waveguide.

The MZM is fabricated on the hybrid silicon platform [7]. Our earlier MZM design incorporated a coplanar waveguide (CPW) electrode design with a voltage-length product of 2 V-mm and modulation bandwidth up to 8 GHz limited by the RC cutoff frequency [5,6]. In general, CPW is a very common TWE design to provide necessary electrical signal for modulation. However, for a CPW incorporating a pin diode, the structure is similar to a microstrip line rather than a simple CPW. In this case, the electrical fields propagate inside the depletion region of the diode instead of residing in between the gaps of signal and ground electrodes. Moreover, the electrical fields also penetrate into the top p cladding and bottom n contact layers depending on the skin depth. The skin depth of the doped epitaxial layers can be still around several μm at 40 GHz due to the small conductivity of the semiconductors so one would expect to see large propagation loss of the driven electrical signal. In order to reduce the propagation loss, it is important to ensure that the propagating electrical fields have minimal overlap with the doped semiconductor. One of the options that has been widely demonstrated for high speed operation is a capacitively loaded (CL) TWE [8]. As illustrated in Fig. 1(a), the small pads extending from the transmission line can provide the necessary electrical signal to drive the device while the TWE is kept away from the semiconductor. The loaded sections (small pads) are capacitive if the Bragg frequency of each periodic section

(L_p) is much larger than the highest frequency of interest. Furthermore, the phase velocity of the electrical signal can be adjusted by changing the distributed capacitance of the transmission line. This can help reduce velocity mismatch between the electrical and optical signal.

In this paper, a CL TWE based on a slotline architecture is preferred over a CPW because it can be implemented in a push-pull configuration for a MZM required reverse bias on both arms [9]. The electrical signal travels along the slotline and the bias voltage is applied using a probe pad connected to the n-contact layer. One important parameter of this design, the fill factor (F), is defined as L/L_p in Fig. 1(a), where L is the length of loaded section and L_p is the periodical length. The total modulation length ($L_t=L \times N$) is then the summation of each individual loaded section, where N is the number of loaded sections. One can also specify the total electrode length (L_t) as $L_p \times N$.

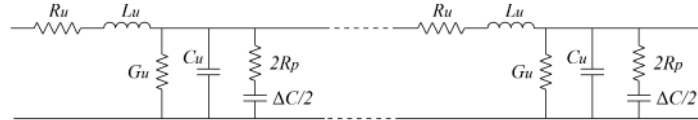


Fig. 2. The equivalent circuit model of the CL slotline design.

To have a further understanding of the design details, an electrical equivalent circuit schematic of the CL TWE is shown in Fig. 2, where L_u , R_u , C_u , and G_u are the inductance, resistance, capacitance and conductance per unit length of the unloaded transmission line while ΔC is the capacitance per unit length due to the loaded modulation section of one arm and R_p is the resistance from the stem. ΔC can also be written as follows:

$$\Delta C = \frac{\epsilon_{QW} w}{d} \cdot F \quad (1)$$

where ϵ_{QW} is the dielectric constant, w is the width, and d is the thickness of the QW, respectively. ΔC is divided by two in the circuit model because the capacitances from two arms are in series. Consequently, the characteristic impedance and phase velocity of the TWE can be expressed as in Eq. (2) because the inductance of the loaded section is almost identical to that of unloaded section [10].

$$Z_0 = \sqrt{\frac{L_u}{C_u + \Delta C / 2}} \quad v_{ph} = \sqrt{\frac{1}{L_u (C_u + \Delta C / 2)}} \quad (2)$$

Based on the above equations, a desired phase velocity of the electrical signal can be achieved, which indicates that the velocity mismatch can be eliminated by choosing the appropriate fill factor and impedance. In addition to velocity matching (Δv), the total length (L_t) of the electrode is also important to the modulation bandwidth since the total electrical loss is larger as the length increases. The small signal response as a function of velocity mismatch and total length is described in Eq. (3) where α is the loss coefficient.

$$H(f) = e^{-\frac{\alpha L_t}{2}} \left[\frac{\sin^2\left(\frac{\alpha L_t}{2}\right) + \sin^2\left(\frac{\omega \Delta v L_t}{2}\right)}{\left(\frac{\alpha L_t}{2}\right)^2 + \left(\frac{\omega \Delta v L_t}{2}\right)^2} \right]^{\frac{1}{2}} \quad (3)$$

Figure 3 illustrates the product of velocity mismatch and L_t as a function of fill factor for different characteristic impedances. The effective index is 3.45 for the hybrid structure and is used to calculate the optical group velocity. As can be seen, the product of $\Delta v L_t$ is positive for larger fill factors, where the optical signal travels faster than electrical signal due to large ΔC . Once the fill factor starts to decrease, the total device capacitance drops and the electrical

wave propagates faster. Eventually, it becomes greater than the optical signal. Ideally, the TWE will have the best small signal response if the impedance is set to $50\ \Omega$ without any velocity mismatch. A characteristic impedance other than $50\ \Omega$ will introduce reflections and oscillations (in the frequency domain) in the device (between two probes). However, to eliminate reflection and match the velocity between optical and electrical signal simultaneously, the fill factor has to be as low as 55% based on Fig. 3, which results in doubling the device length. This is not preferred due to the large footprint and possible increase in propagation loss. Hence, a characteristic impedance of $35\ \Omega$ and fill factor of 80% are chosen based on a conservative estimate of electrical propagation loss and as a tradeoff between device size and reflection.

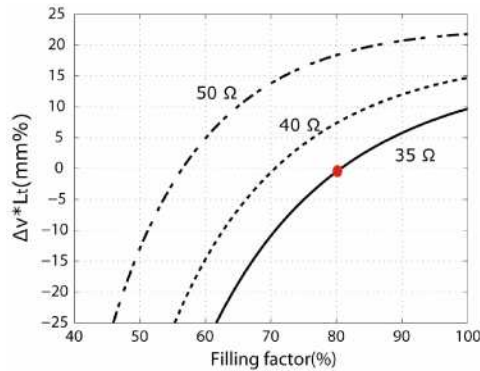


Fig. 3. The product of velocity mismatch and total length of the electrode as a function of fill factor for a MZM with $L_e = 500\ \mu\text{m}$. The red dot shows the device design implemented here.

In addition to the TWE design for improving the modulation bandwidth, some modifications were also made to the device structure to obtain better optical characteristics. Two adiabatic tapers, both in silicon waveguide and III-V mesa, as shown in Fig. 1(a), are added between passive and hybrid sections to minimize reflection and increase coupling efficiency. The cross section of the loaded region is depicted in Fig. 1(b). The signal and ground of the slotline are on top of each arm, respectively. The two arms have a common ground by connecting the n-contact layer together. The cladding mesa is $4\ \mu\text{m}$ wide, and the QW/SCH layers are intentionally under-cut to $2\ \mu\text{m}$ to reduce the device capacitance. The silicon waveguides have a height of $0.47\ \mu\text{m}$, a slab height of $0.2\ \mu\text{m}$, and a width of $1\ \mu\text{m}$. In order to have a better extinction ratio and reduce cross talk, the silicon waveguides are etched down to the buried oxide layer around each 2×2 MMI coupler to reduce undesired interference and improve the fabrication tolerance. The fabrication of the modulators is almost identical to our previous devices [5], except that an extra implantation step is added to create electrical isolation between the loaded sections. The metal and p-contact layer on top of the mesa are removed for the unloaded regions, and then proton implantation (Fig. 1(b)) is applied to damage the doping concentration of p-cladding layers such that modulation sections can be defined without disturbing the optical mode.

3. Device characteristics

The normalized transmission is similar to previous devices [5] since the III-V epitaxial layers are identical. The voltage-length product is $2.4\ \text{V}\cdot\text{mm}$ for a $500\ \mu\text{m}$ device with $3\ \text{dB}/\text{mm}$ propagation loss for the hybrid section and $1\sim 1.2\ \text{dB}$ loss per adiabatic taper. The ER of this MZM is $18.4\ \text{dB}$, which is better than published results due to the deep etch silicon waveguides mentioned in the previous section.

To characterize the electrode, a $500\ \mu\text{m}$ (L_e) MZM with $F = 80\%$ was measured using a Agilent 8164A network analyzer. To extract the device impedance, electrical propagation loss, phase velocity and other parameters, a full S matrix was first recorded and then converted to an ABCD matrix. Next, the ABCD matrix was inserted into the equations used

to calculate the corresponding impedance and loss. The comparison of impedance and propagation loss between previous CPW and current CL slotline design is shown in Fig. 4. As shown in Fig. 4(a), the characteristic impedance of the CL slotline with 80% fill factor is around 35Ω , which is consistent with the theoretical estimates in Fig. 3. This value is larger than the 20Ω impedance of conventional CPW design, and can help to reduce the reflection from the electrical source to the device. Moreover, the propagation loss also decreases from 7.5 dB/mm to 5.8 dB/mm at 20 GHz . The loss constant does improve, but not as much as desired. One of the possible sources for such a large loss for the CL slotline is the imperfect isolation between the loaded sections. As mentioned earlier, the proton implantation was used to create a large resistance between the modulation sections so that the electrical signal does not travel on top of the III-V mesa. However, the isolation might not be good enough and hence fringe fields penetrating into the semiconductor can cause excess loss. The loss can be further reduced by improving the isolation.

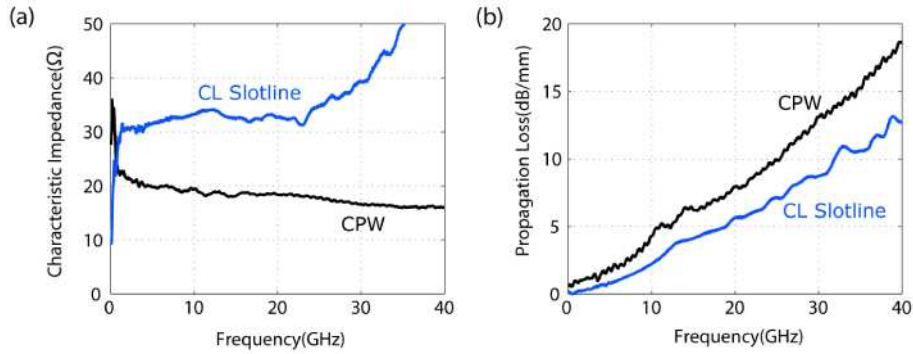


Fig. 4. (a) Impedance of CL slotline and CPW design for a MZM with $L_a = 500 \mu\text{m}$. (b) Propagation loss of CL slotline and CPW design for a MZM with $L_a = 500 \mu\text{m}$.

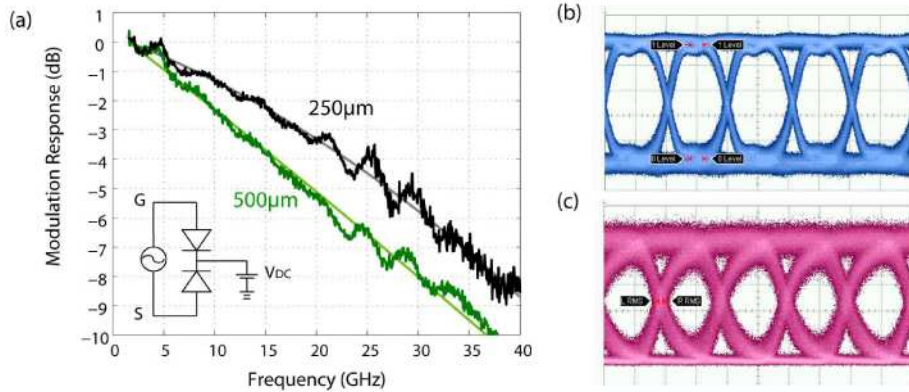


Fig. 5. (a) Experimental frequency responses for the MZMs. (b) The driven electrical signal out from the BERT at 25 Gb/s . (c) The modulated signal after the modulator for a $500 \mu\text{m}$ MZM.

Next, the modulation bandwidth of MZM was measured using an Agilent PNA network analyzer with a 45 GHz high speed photodetector (PD) attached to port 2 of the network analyzer. Calibration is done by directly connecting a cable from port 1 to port 2. The measured frequency response with a 50Ω termination is shown in Fig. 5(a) after subtracting the response of the PD, a RF probe and one extra cable, which are not in the calibration. The 3 dB cutoff frequencies of a $250 \mu\text{m}$ and a $500 \mu\text{m}$ device are about 18 GHz and 12.5 GHz , respectively. The measured bandwidths are mainly limited by RC cutoff frequency due to

imperfect isolation. The small resistance of the unloaded section not only increases the propagation loss, but also affects the capacitance of the loaded section and hence reduces the modulation bandwidth.

The large signal modulation was also characterized with a SHF 40G BERT system. A $2^{31}-1$ pseudorandom bit sequence (PRBS) at 25 Gb/s (Fig. 5(b)) is used to drive the device while a optical signal at 1550 nm is coupled to the chip. The 500 μm device is biased at -5 V with 4 Vpp swing while the bias of the AC signal is slightly adjusted to achieve best signal quality. As can be seen in Fig. 5(c), the modulated eye at 25 Gb/s is clearly open with 11 dB ER, which to the best of our knowledge is the best ER above 10 Gb/s for any silicon based modulator.

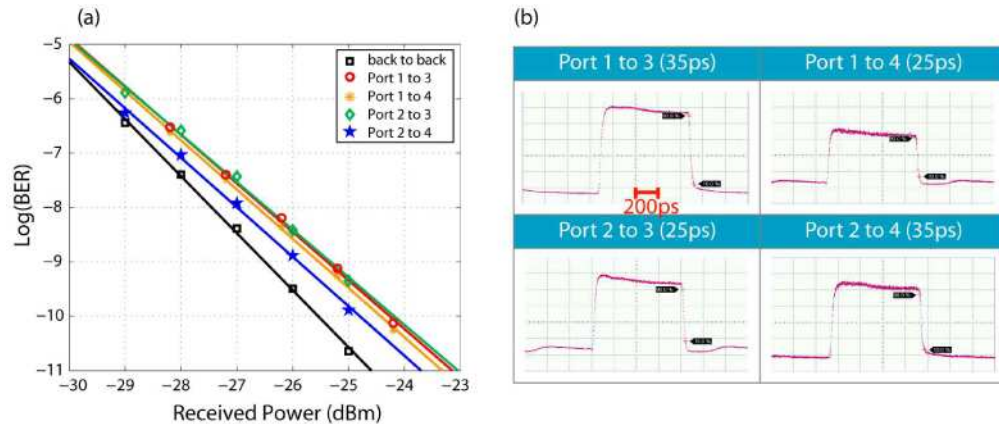


Fig. 6. (a) BER versus optical received power for all ports configurations at 40 Gb/s with $2^{31}-1$ NRZ PRBS. (b) The measured rise time from 10% to 90% for individual port.

A 40 Gb/s bit-error-rate (BER) measurement was also performed to explore the signal integrity for switching applications by replacing the 1x2 MMI with a 2x2 MMI coupler. As can be seen in Fig. 6(a), the power penalties for all ports are below 1.3 dB at 10^{-10} BER. Furthermore, the rise time of the switch, depicted in Fig. 6(b), is from 25~35 ps (4 V swing) with a driven signal of 17.4 ps rise time, which allows fast switching with low to zero latency for future high speed optical interconnects above 20 Gb/s. The energy consumption is 8 pJ to switch between two states. The ERs of these four ports are 19.0, 24.7, 14.4, and 25.2 dB with 4 V swing while the crosstalks are -24.3 , -19.2 , -27.6 and -11.9 dB.

4. Conclusion

A hybrid silicon MZM utilizing CL slotline design is demonstrated using 25 Gb/s large signal modulation. The new TWE design has resulted in improvements in impedance matching as well as reduction of propagation loss. Large ERs of 18 dB at DC and 10 dB at 25 Gb/s make it feasible to integrate these modulators with lasers to implement wide bandwidth transmitters. In addition, a switch based on these modulators was shown to have a capability of switching faster than 35ps with less than 1.5 dB power penalty for a 40 Gb/s data stream.

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