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A 62nW 0.6V CMOS Temperature Sensor Design

A Thesis submitted in partial satisfaction of the requirements
for the degree Master of Science

in

Electrical Engineering (Electronic Circuits & Systems)

by

Yuan Cao

Committee in charge:

Professor Patrick P. Mercier, Chair
Professor Peter M. Asbeck
Professor Bang-Sup Song

The Thesis of Yuan Cao is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

UNIVERSITY OF CALIFORNIA, SAN DIEGO

2015

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Most importantly, I would like to give my sincerest thanks to my mother and father, without whose sacrifice I will never have the opportunity to study here.

ABSTRACT OF THE THESIS

A 62nW 0.6V CMOS Temperature Sensor Design

by

Yuan Cao

Master of Science in Electrical Engineering (Electronic Circuits & Systems)

University of California, San Diego, 2015

Professor Patrick P. Mercier, Chair

The development of low power CMOS technology has enabled a higher level of integration for ultra-low power applications. Among the big variety of sensor systems, temperature sensor is one of the most important and commonly used subsystem.

In this thesis, a novel architecture of low power temperature sensor is proposed. In order to minimize power consumption, the temperature sensor is designed to work in subthreshold region, with a 0.5V-0.9V supply. With 62nW active power, 0.1°C resolution, and 0.55°C inaccuracy from 0 to 100°C, the proposed temperature sensor achieves low power consumption without degrading resolution and accuracy. The active power is

highly reduced by using a novel two-amplifier reference current generator. A 17nW 30-40kHz oscillator is designed as reference clock, 13ppm temperature coefficient is achieved with resistor calibration. The supply voltage sensitivity of oscillation frequency is 1.2%/V without using LDO or regulated current source. To demonstrate the proposed topology, a chip have been designed and submitted for fabrication in 180nm CMOS technology.

CHAPTER 1 Introduction

1.1 Background

Low power sensor network is obtaining more and more attention in the past few years. Researches on ultra-low power transceiver [1] and low power sensor platform [2] have brought the power budget down to scale of nano-Walt. Although the low power feature makes the sensor applications more convenient and powerful, it challenges the conventional design methodology.

Among the big variety of sensors, temperature sensor is one of the most important and commonly used subsystem. In virtue of the fast development of Wireless Body Area Network (WBAN), monitoring body temperature, blood pressure, heart rate and other signals on an integrated sensor platform is highly demanded. For example, [2] proposed a novel low power inner ear sensor platform that provide up to 2.6nW from cochlear potential. Known that human inner ear temperature has good sensitivity and isolation from outside air temperature, it is promising to integrate temperature sensor onto the inner ear sensor platform. In this case, how to minimize power consumption of temperature sensor is the core issue.

Recent works on low power temperature sensor have been proposed [3-6]. In [3], frequency-to-digital conversion is applied by counting the number of the clocks of the temperature dependent oscillator in a constant time interval. However the power consumption is relatively large. [4] proposed a 405nW temperature sensor based on time-to-digital conversion. It achieves sub-uW power consumption at the expense of lower

resolution. [5] gives a 220nW temperature sensor, it achieves good power feature but suffers from high inaccuracy due to the reference clock stability problem. In [6], a 71nW temperature sensor is proposed with a modified two-amplifier current generator that eases the difficulty of designing low reference voltage. But the measurement precision still suffers a lot from the reference clock temperature stability.

This thesis proposes a new architecture of a time-to-digital conversion based temperature sensor and a temperature independent oscillator. A total active power consumption of 62nW is achieved with 0.1°C resolution and 0.55°C inaccuracy (after two point calibration) from 0 to 100°C.

1.2 Thesis Organization

Chapter 2 introduces the design methodology and circuit topology. Detailed explanation of low power amplifier, temperature-to-pulse generator, and temperature independent oscillator design process are included. Chapter 3 contains the simulation results for the oscillator and the whole temperature sensor. The final Chapter gives conclusions from the research and expectations for future work.

CHAPTER 2 Design Principle and Circuits

2.1 Temperature Sensor Topology

It is known that previous works for low power temperature sensors suffer from comparatively large power consumption, high inaccuracy, and limited resolution. In this thesis, we present a novel low power temperature sensor topology for low power, low sampling frequency applications.

The block diagram of the proposed temperature sensor is shown in Figure 1. After “Start” signal turns from “0” to “1”, unlike topology that proposed in [7] which applies proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) current references, the proposed design first generates a reverse PTAT reference current and a reverse CTAT reference current from a set of reference current generators that apply subthreshold amplifiers and resistors. Then the reverse PTAT and CTAT current are feed into the current controlled delay generator and converted to CTAT and PTAT pulses at node A1 and A2 as input of XOR gate. The falling edge of XOR gate also drive the “READY” signal to “1”, indicating a sample period is completed and ready to read out data. In this way different temperature will result in pulse wave with different width, details of sensor design are introduced in Chapter 2.3. Then the pulse wave is further digitized by an on-chip oscillator, the frequency of this oscillator is temperature and supply voltage independent, details of oscillator are introduced in Chapter 2.4. A delay block is added to further reduce oscillator active power. After “Start” signal turns from “0” to “1”, the current-controlled-

delay generator first starts to operate, then when A1 and A2 are almost ready, the Delay block will power on the oscillator—by which 80% of oscillator active power will be saved.

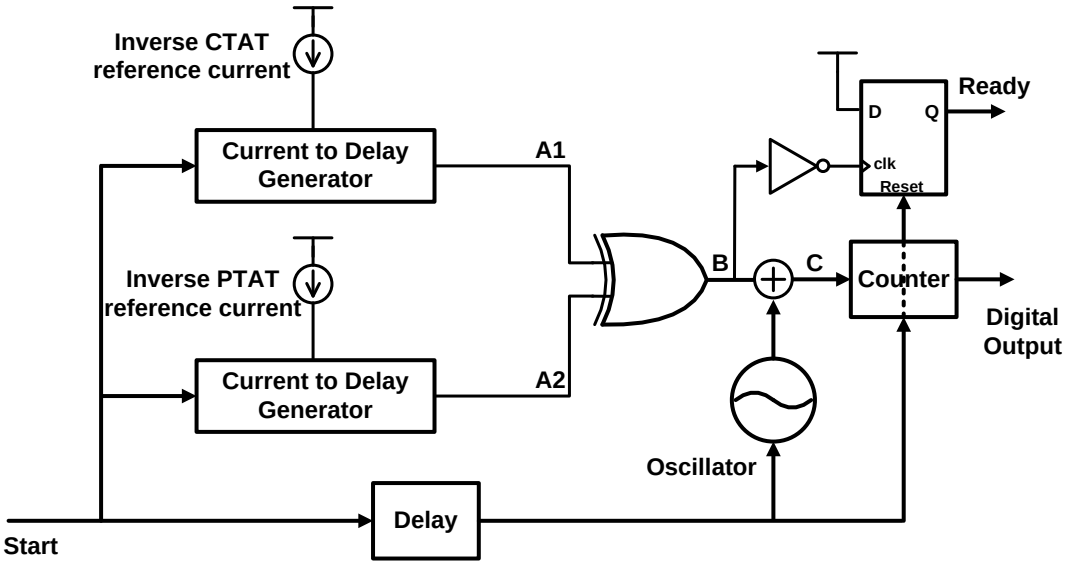


Figure 2.1.1. Block diagram of proposed Temperature

Key point of the current-to-delay generator part and oscillator part are current reference designing. Previous works tried to generate ultralow current reference by using bandgap, external oscillator, etc. However, those methods still suffered from relatively high power, external sources or clock, narrow operating temperature range, and supply dependency. In this design, we introduce a novel reference current generator (RCG), which is discussed in Chapter 2.2.

2.2 Reference Current Generator

2.2.1 Conventional Reference Current Generator

The conventional way to build RCG [7] is shown in Figure 2.2.1.1. Given a reference voltage V_{ref}, we obtain an output current $I_{ref} = \frac{V_{ref}}{R}$. This architecture is stable for conventional supply voltage and reference current purpose. However, in low power applications, we are facing low supply voltage (e.g. VDD=0.6V) and should avoid large current (>20nA). In this case, for a 0.6V supply voltage, it is very hard to achieve stable operating point in a wide temperature range, say, -20ºC to 120ºC. A circuit implementation of conventional RCG is shown in Figure 2.2.1.2, and Figure 2.2.1.3 shows the plot for V_{out} vs. V_{in} at 0ºC and 100ºC. It is hard for V_{out} to follow V_{ref} when V_{ref} is close to 0V or *VDD*, and this feature becomes more significant when temperature changes. Carefully designed amplifiers may suffer less from this phenomenon, but not able to eliminate it. We can briefly analyze how the operating point varies for the circuit in Figure 2.2.1.2. When temperature becomes higher, at certain bias current the drain-source voltage of transistor tend to decrease, $V_{DS,N1}$ tend to pull V_A down and $V_{DS,P1}$ tend to pull V_A up. If temperature goes out of certain range, e.g. 0ºC to 30ºC, it is hard for the amplifier to maintain proper operating point, and restricts this architecture to a limited usage.

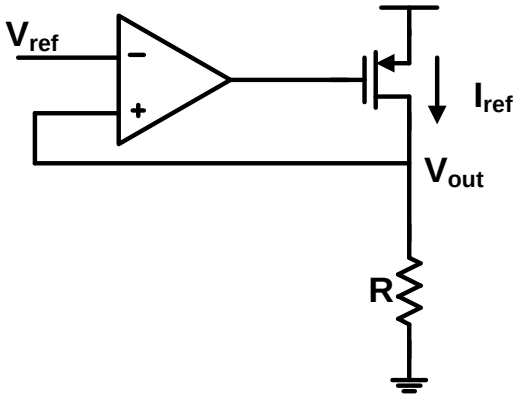


Figure 2.2.1.1 Block diagram of Conventional RCG.

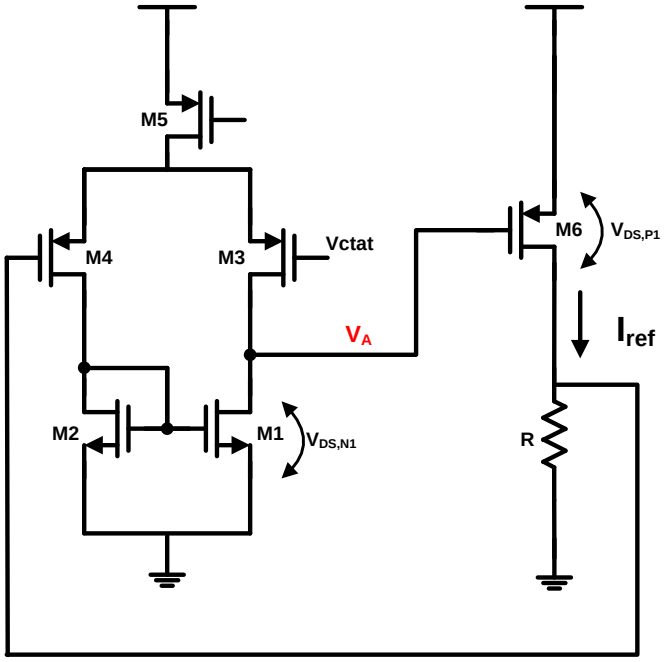


Figure 2.2.1.2 Schematic Conventional RCG.

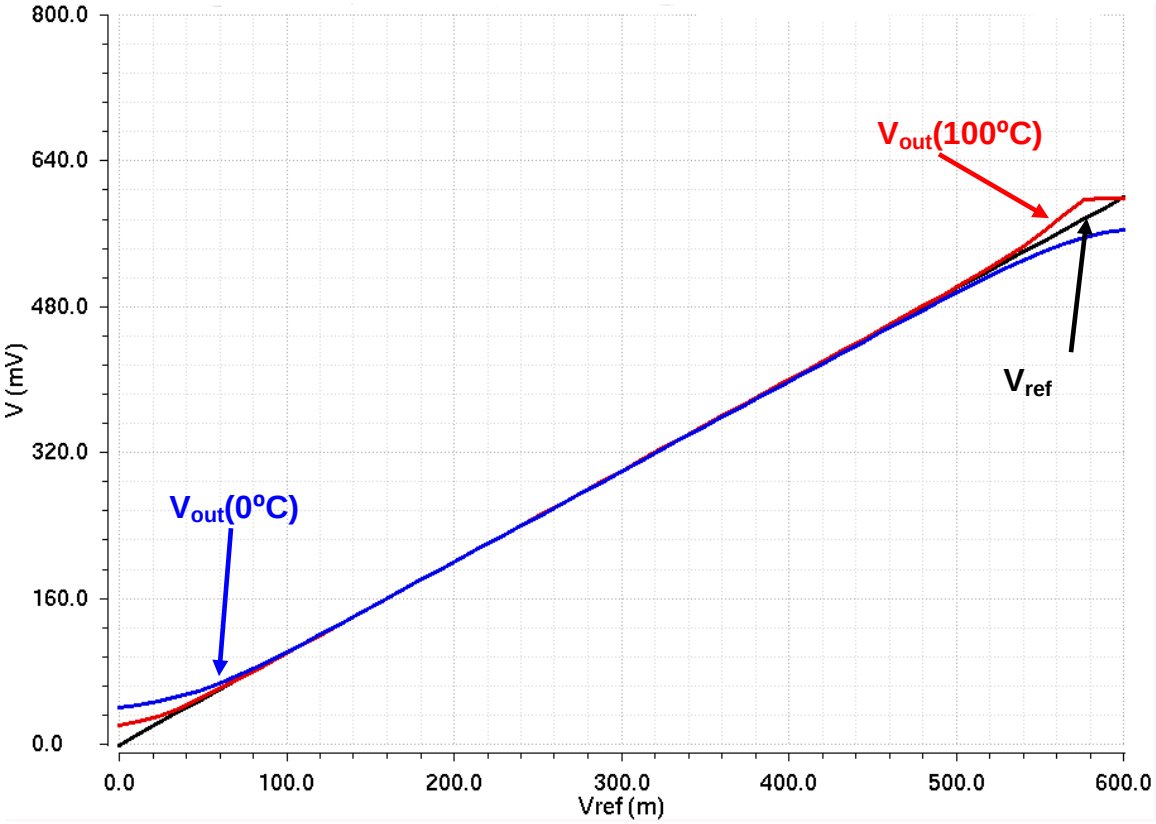


Figure 2.2.1.3. Conventional RCG V_{out} vs. V_{ref}.

In Fig 2.2.1.2, power consumption and chip area is a trade-off. For certain V_{ref} value, smaller I_{ref} current means large resistor. To achieve a 10nA reference current at V_{ref}=100mV, the resistor has to be 10MΩ. In order to obtain a lower current and minimize the area cost, lower reference voltage is preferred. However, according to previous discussions, in this topology is it difficult to maintain good operating point at very low reference voltage (e.g. 30mV), and it is also difficult to generate such low reference voltage. In the following chapter, we propose a novel double loop voltage controlled current reference generator.

2.2.2 Double Loop Voltage Controlled Current Reference Generator

To achieve wider operation range and stable operating point, a novel dual-amplifier reference current generator is proposed as shown in Figure 2.2.2.1, a similar architecture can be found in [6] with some differences. In this architecture, two amplifiers forms two feedback loops which give $V_1=V_{ref1}$ and $V_2=V_{ref2,}$ thus the reference current $I_{ref} = \frac{V_{ref1} - V_{ref2}}{R}$. This indicates that the reference current is no longer controlled by an absolute value. This is a useful property since we do not need to create a very low absolute voltage, but a low "relative voltage". Since a very low CTAT or PTAT voltage with relatively large temperature coefficient is hard to achieve [7-8]. In this design, the reference voltage can be set to accommodate amplifier operating point, e.g. V_{ref1}=230mV and V_{ref2}=200mV, which gives us more flexibility in amplifier design and achieving higher temperature stability.

By applying this architecture, we can use the NFET input device amplifier to drive the PFET transistor N1 and use the PFET input device amplifier to drive the NFET transistor P1, then the operating point of the amplifier's load transistors will move at same pace with relative output transistor, which helps the system to work properly in relatively large temperature range. It is also easy to bias the amplifier for this dual-amplifier architecture. In Figure 2.2.2.1, the bias voltage V_{bias_n} and V_{bias_p} are used to bias each other's tail transistor.

Figure 2.2.2.2 shows a 200 samples Monte-Carlo simulation for current I_{ref}. The simulation shows a good stability with a standard deviation of 0.13nA.

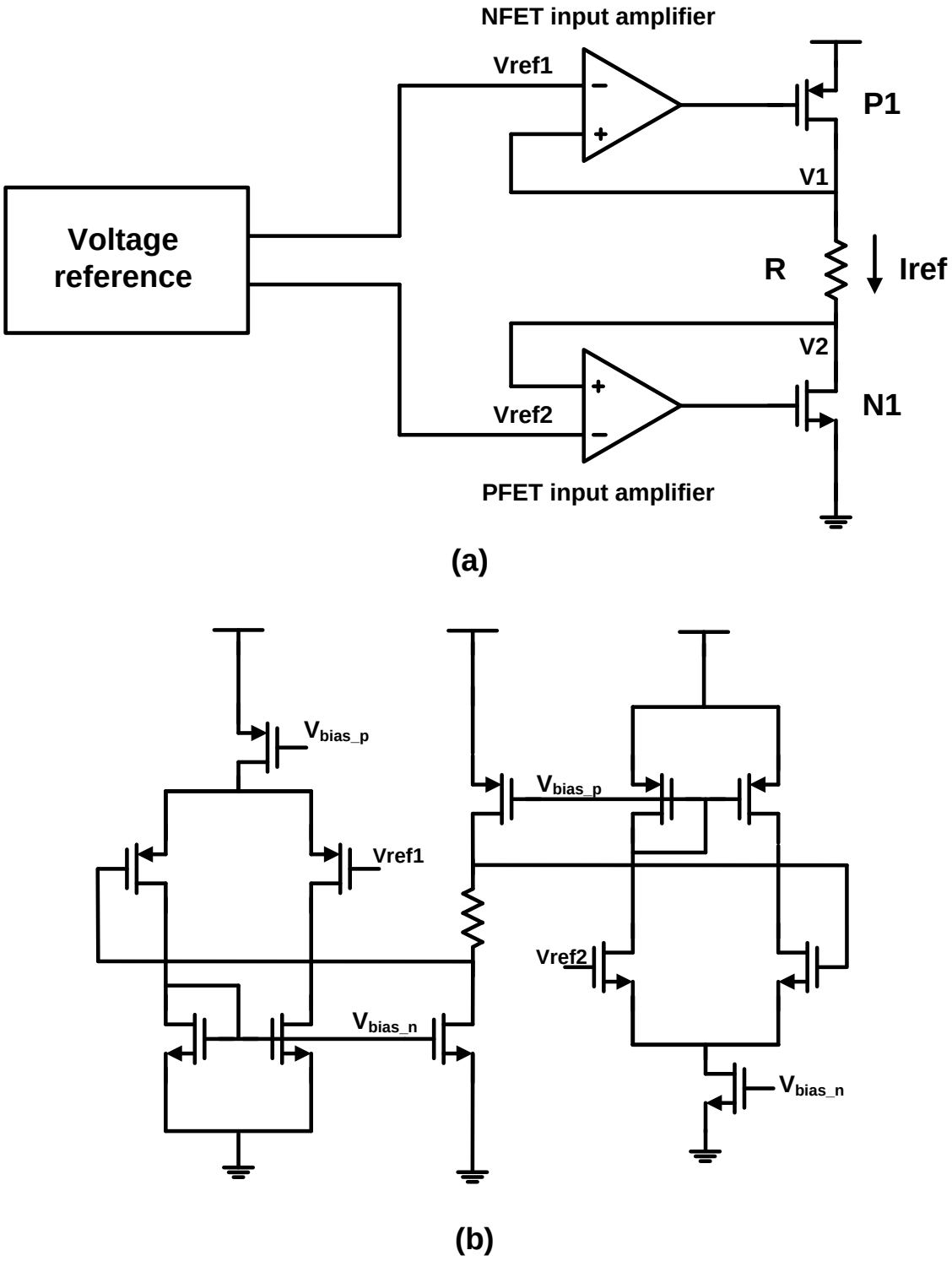


Figure 2.2.2.1. Dual-amplifier reference current generator (a) Block diagram (b) Schematic.

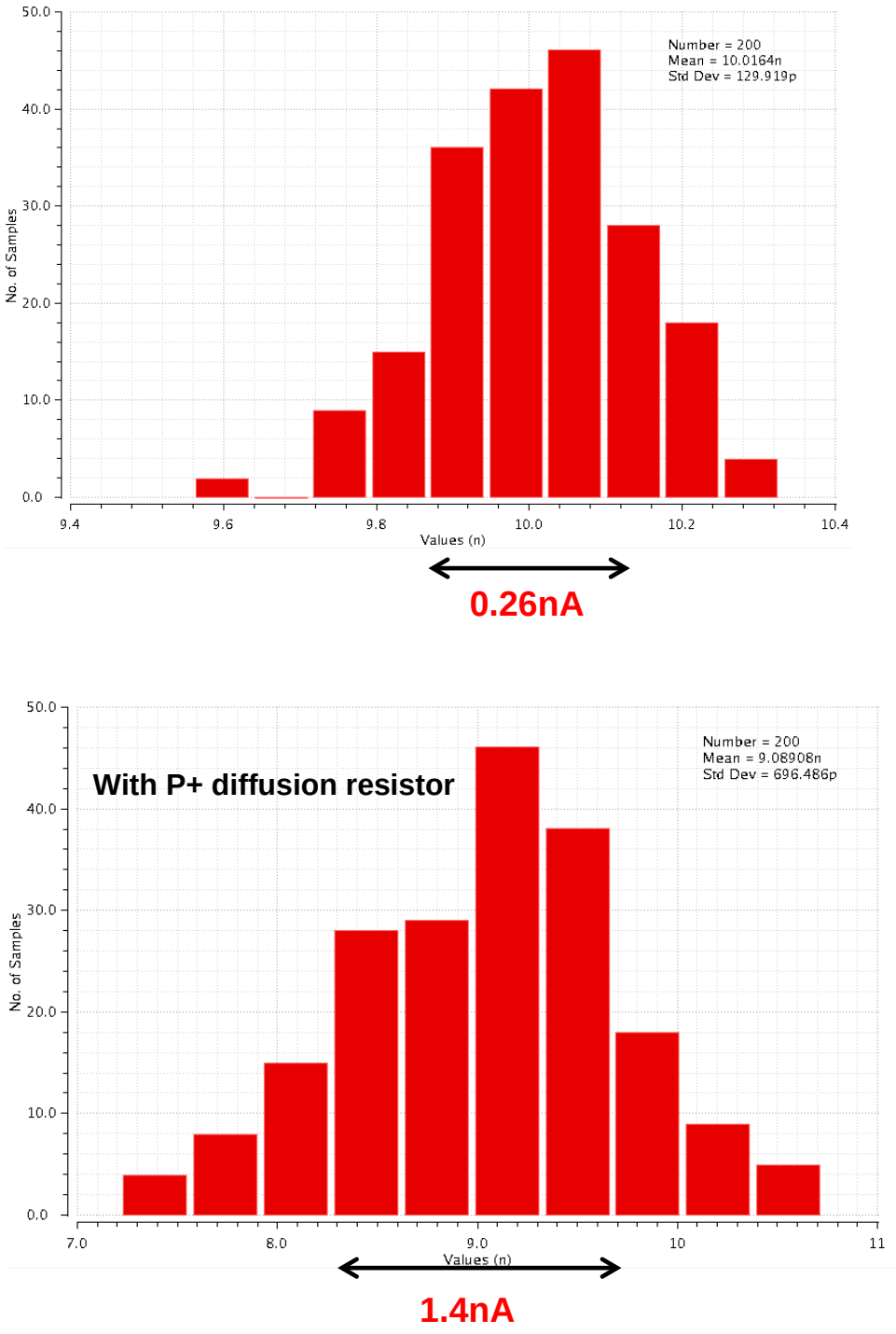


Figure 2.2.2.2. Monte-Carlo simulation for I_{ref}. (a) With ideal resistor model (b) With P+ diffusion resistor model.

2.2.3 Subthreshold Amplifier Design

This section introduces the design process of a low power subthreshold amplifier. In subthreshold region, drain current for MOSFETs is:

$$I_D = I_{ds,0} e^{\frac{Vgs-Vth}{n\phi_T}} (1 - e^{\frac{-Vds}{\phi_T}}) \quad (2.3.1)$$

By ignoring body effect, the threshold voltage for MOSFET is:

$$V_{th} = V_{th0} - \lambda_D V_{DS} \quad (2.3.2)$$

Where n is a technology dependent constant, V_T is thermal voltage, V_{gs} and V_{ds} are the gate-source voltage and drain-source voltage, $\phi_t = \frac{kT}{q}$ is the thermal voltage(k is the Boltzmann constant, T is the absolute temperature, and q the elementary charge). $I_{ds,0}$ is the drain-to-source current when gate-to-source voltage equals to threshold voltage, it depends on temperature, process parameter, and size of transistor. λ_D is the drain-induced-barrier-lowering(DIBL) effect coefficient. According to (2.2.1), if V_{DS} is large enough (>3ϕ_t), the transistor can be treated as a BJT-like device. We can derive important transistor parameters from the basic drain current formula of subthreshold transistor. Similar with above-Vt transistors, we can also define trans-conductance ($g_m = \frac{I_d}{n\phi_t}$), drain-to-source resistance ($r_d = \frac{n\phi_t}{\lambda_D I_d}$), intrinsic gain($A_{v0} = g_m r_d$), etc.

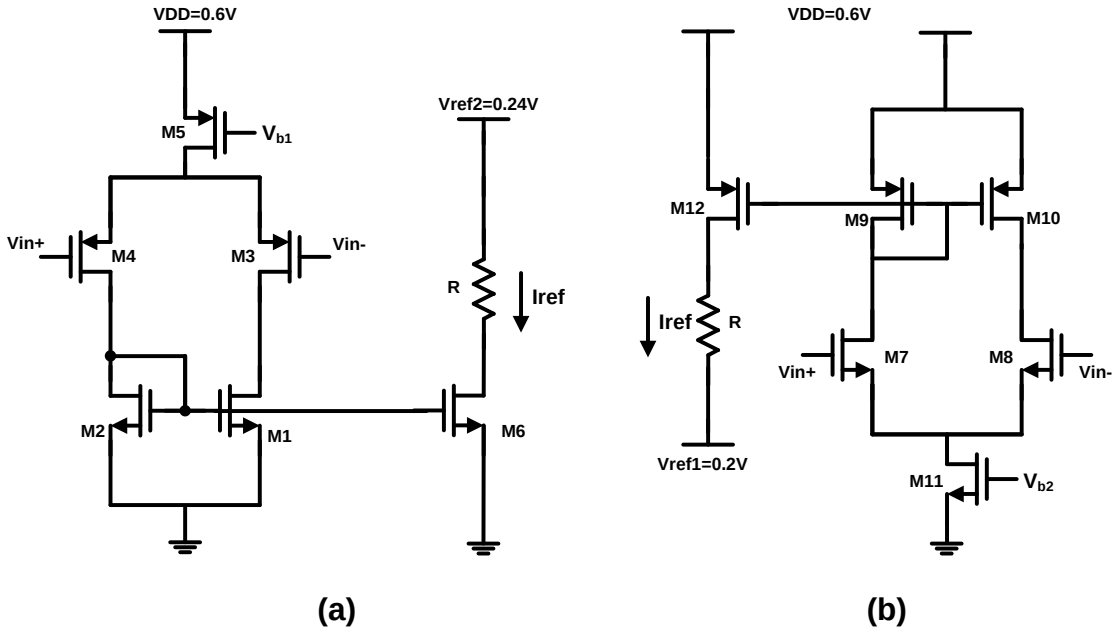


Figure 2.2.3.1. Schematic for designing dual-amplifier system.

For the dual-loop architecture, the two amplifiers are designed individually as shown in Figure 2.2.3.1. In this design, requirements for amplifiers that used in voltage-to-current generator are shown in Table.1:

Table.1. Amplifier design requirements.

First stage bias current	10nA
Second stage bias current	10nA
DC gain	60dB
Phase Margin	> 60 degree
Input common mode in (a)	240mV
Input common mode in (b)	200mV

The design procedure is mainly constrained by power consumption, because of the tight power budget. In order to guarantee low active power and enough SNR, a 10nA bias current for first stage and 10nA I_{ref} is chosen. Area is also an important aspect since we may use large resistors which may exceed a few mega-Ohm. So we prefer a lower value of $\Delta V = V_{ref2} - V_{ref1}$ which gives a smaller *R*. Considering proper operating point of the amplifier, we choose $V_{ref1} = 200mV$ and $V_{ref2} = 240mV$, then $R = 4M\Omega$. The DC gain is set to 60dB in order to force V_{out} follow V_{ref} closely.

The design procedure starts from DC gain. DC gain of the amplifier can be written as:

$$A_v = g_{m3}(r_{d1} \| r_{d3}) g_{m6} R \tag{2.3.3}$$

Rewrite A_v using DIBL coefficient:

$$A_v = \frac{g_{m6} R}{\lambda_{D1} + \lambda_{D3}} \tag{2.3.4}$$

Since the DIBL effect coefficient is directly related to the length of transistor, (2.3.4) will help us choose the minimum transistor length to achieve the gain requirement. Note that in order to keep good operating point in wide temperature range, transistor M_6 is set to be the same size as $M_{1,2}$. Since the drain current of M_6 and M_{12} will be mirrored to generate reference current, the length of transistors should be relevantly large.

The AC response of the circuit in Figure 2.2.3.1(a) is shown in Figure 2.2.3.2.

Table.2. Device sizes for amplifiers.

$M_{1,2}$	10u/20u=2*5u/20u
$M_{3,4}$	50u/10u=20*2.5u/10u
M_5	10u/10u=4*2.5u/10u
M_6	20u/20u=4*5u/20u
$M_{7,8}$	10u/20u=10*5u/20u
$M_{9,10}$	50u/10u=20*2.5u/10u
M_{11}	20u/20u=4*5u/20u
M_{12}	10u/10u=4*2.5u/10u

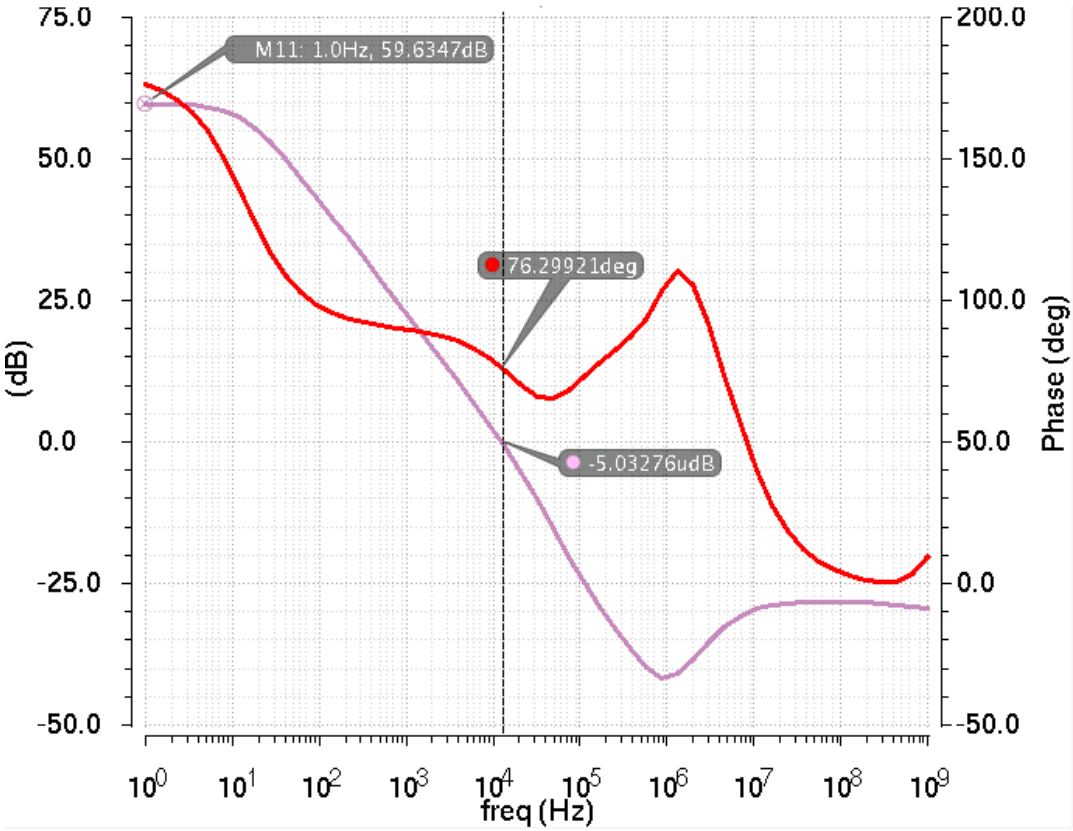


Figure 2.2.3.2. AC response of amplifier in Figure 2.2.3.1(a).

2.2.4 Stability and Compensation

The dual-amplifier circuit in Figure 2.2.2.1(b) is easy to achieve good gain (91dB), but tends to become unstable even at low frequency. In order to achieve good stability, compensation is required.

The dual-amplifier system becomes unstable when AC input signal at V_{ref1} and V_{ref2} have the same phase or 180° phase difference. Figure 2.2.4.1 shows the worst case AC response. At 5.1kHz, we find the worst phase margin of 8.6 degree with positive gain, thus the system is unstable. In order to achieve a phase margin larger than 60°, two 30pF capacitors are added across the gate and drain of the second stage transistors. The AC response after compensation is shown in Figure 2.2.4.2.

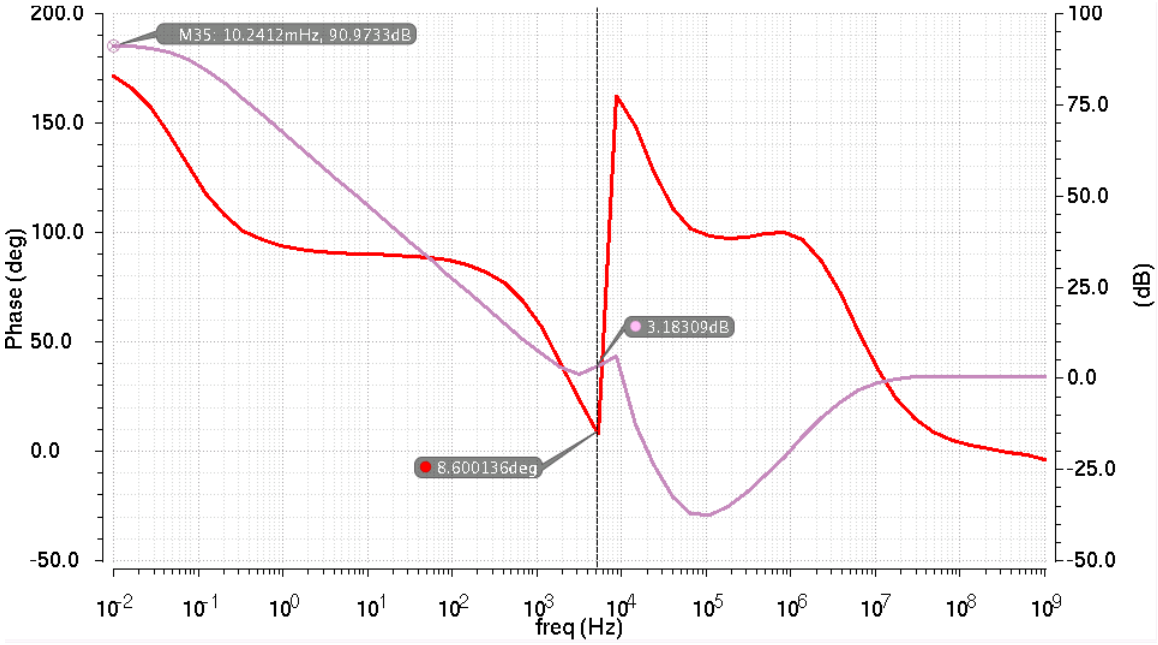


Figure 2.2.4.1. AC response of dual-amplifier system before compensation.

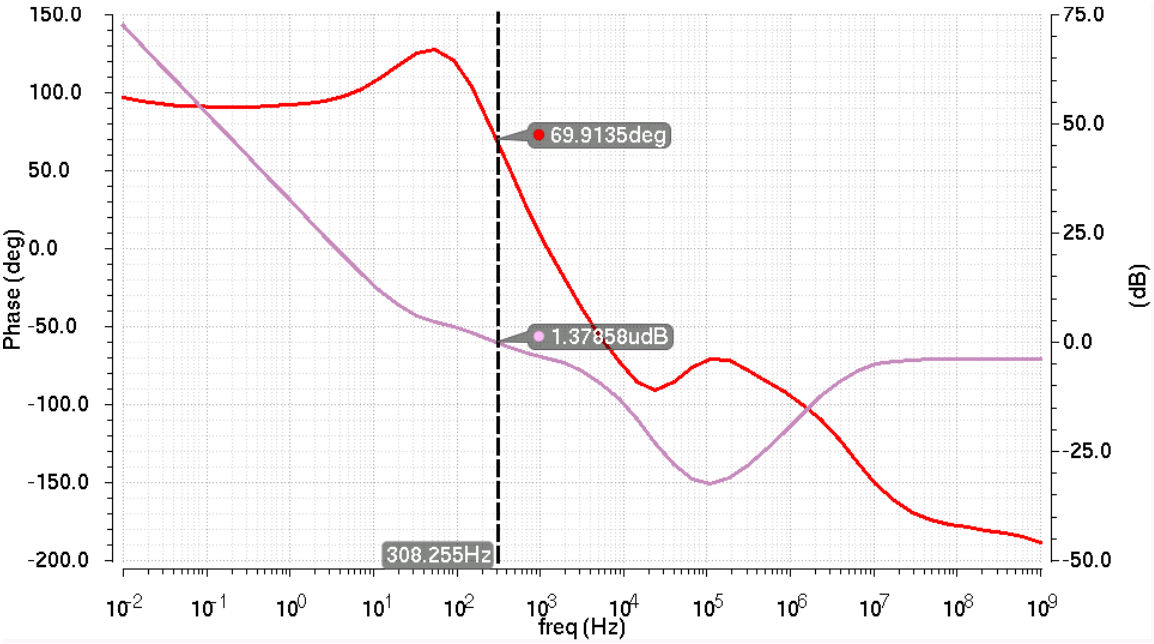


Figure 2.2.4.2. AC response of dual-amplifier system after compensation.

2.3 Temperature-to-Pulse Generator

In Chapter 2.1 we have introduced the block diagram of the temperature sensor in Figure 2.1.1. The sensor is composed of two main blocks: temperature-to-pulse generator and time-to-digital convertor. In this chapter, we mainly talk about the first part.

2.3.1 Current-to-Delay Generator

The current-to-delay generator is responsible for generating different voltage pulses at different temperature. In this design, the generated voltage pulse is proportional to absolute temperature, which means the pulse width will change linearly with temperature. The schematic of current-to-delay generator is shown in Figure 2.3.1.

Assuming I_{ref1} and I_{ref2} are two different reference currents, and the initial voltages of V_1 and V_2 are both 0V. When $t=0$, I_{ref1} and I_{ref2} start to charge node V_1 and V_2 , when the voltage of these two nodes reach the flip voltage of the first invertor, the invertor will flip and there will be a sharp rising edge at V_{out1} and V_{out2}. Since the arrival time of V_{out1} and V_{out2} are different, the XOR gate will generate a pulse Δt.

If the capacitance at node V_1 and V_2 are both C, and the flip voltage of the first stage invertor is V_{flip}, we can find the expression of Δt:

$$\Delta = \frac{CV_{flip}}{I_{ref\,2}} - \frac{CV_{flip}}{I_{ref\,1}} \tag{2.3.1}$$

Assuming V_{flip} is a temperature independent constant, then Δt is determined by I_{ref1} and I_{ref2}.

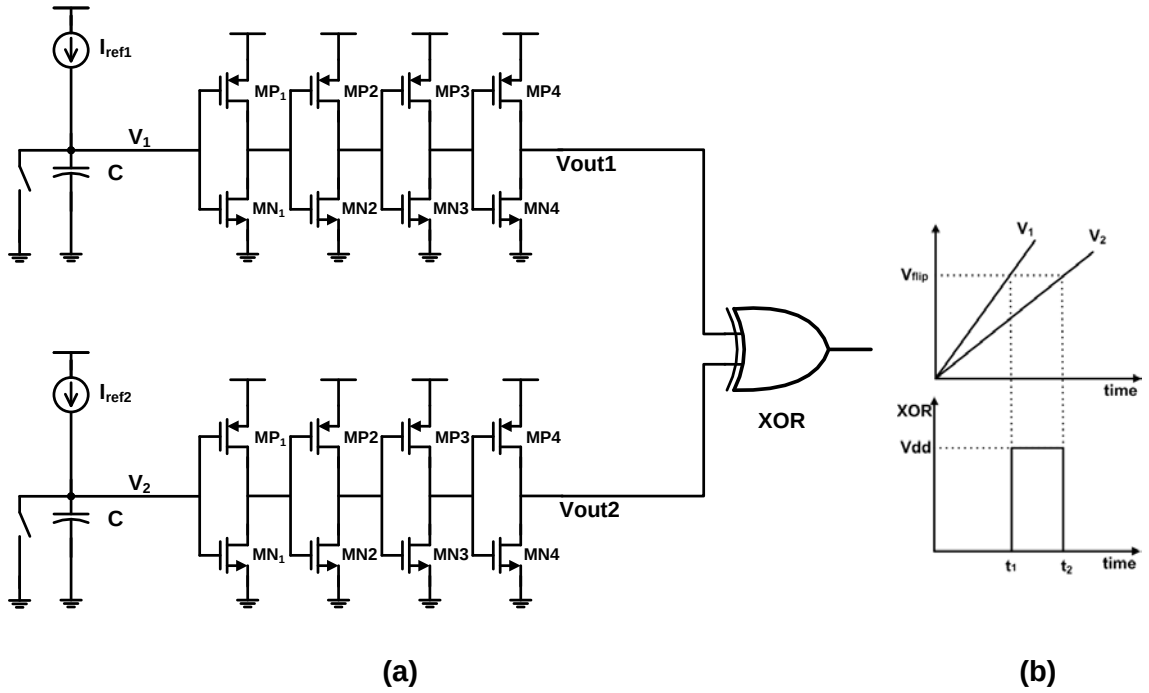


Figure 2.3.1. Schematic of current-to-delay generator

2.3.2 Temperature Dependent Reference Current Generation

In order to generate the pulse that increases linearly with temperature, the reference current I_{ref1} and I_{ref2} must have a proper temperature dependency.

Considering the expression of Δt, if I_{ref1} and I_{ref2} are designed to be reversely proportional to absolute temperature with opposite coefficients:

$$\begin{cases} I_{ref1} = \dfrac{k_1}{T} \\ I_{ref2} = \dfrac{k_2}{T} \end{cases}, \; k_1 < 0, k_2 > 0 \qquad (2.3.2)$$

The the pulse width Δt becomes:

$$\Delta = CV_{flip}(\frac{1}{k_2} - \frac{1}{k_1})T \qquad (2.3.3)$$

(2.3.3) indicates that the pulse width only varies with temperature, and increases linearly when temperature rises.

Since the resistors in CMOS technology usually perform different temperature dependency – either PTAT or CTAT (PTAT: proportional to absolute temperature; CTAT: complementary to absolute temperature), and for certain type of resistor the temperature dependency has a good linearity, this feature can be used to generate the demanded reference current. A circuit implementation is shown in Figure 2.3.2 using the dual-loop amplifier introduced in Chapter 2.2.2.

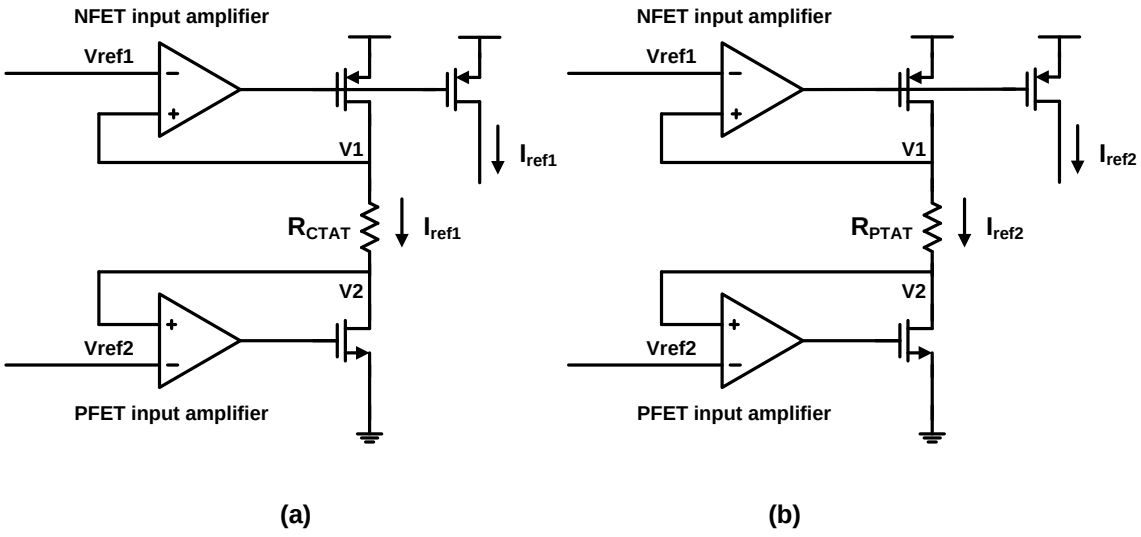


Figure 2.3.2.1. (a) CTAT current generator (b) PTAT current generator.

In Figure 2.3.2.1, V_{ref1} and V_{ref2} are reference voltage. R_{PTAT} and R_{CTAT} are resistors with opposite temperature coefficient:

$$\begin{cases} R_{CTAT} = R_{0,ctat}(T_0)\left(1+k_{ctat}T\right) \\ R_{PTAT} = R_{0,ptat}(T_0)\left(1+k_{ptat}T\right) \end{cases}, \; k_{ptat} > 0, k_{ctat} < 0 \tag{2.3.4}$$

where T is absolute temperature in Celsius degree, k_{ptat} and k_{ctat} are temperature coefficients of R_{PTAT} and R_{CTAT}. Then we can obtain the reverse-proportional-to-absolute-temperature reference current:

$$\begin{cases} I_{ref1} = \dfrac{V_{ref1} - V_{ref2}}{R_{0,ctat}(T_0)\left(1+k_{ctat}T\right)} \\ I_{ref2} = \dfrac{V_{ref1} - V_{ref2}}{R_{0,ptat}(T_0)\left(1+k_{ptat}T\right)} \end{cases} \tag{2.3.5}$$

where $R_{0,ptat}(T_0)$ and $R_{0,ctat}(T_0)$ are resistance for R_{PTAT} and R_{CTAT} at T_0 °C, ΔT is equal to T-T_0. And the pulse width can be expressed using the resistor expression:

$$\Delta t = \frac{CV_{flip}(R_{0,ptat}(T_0) - R_{0,ctat}(T_0) + (R_{0,ptat}(T_0)k_{ptat} - R_{0,ctat}(T_0)k_{ctat})\Delta T)}{V_{ref1} - V_{ref2}} \tag{2.3.6}$$

Here we assume the clock frequency is 30kHz, $R_{0,ctat}(-20^{\circ}C) = R_{0,ctat}(-20^{\circ}C) = 4M\Omega$, k_{ptat}=-k_{ctat}=1350ppm,. In order to achieve the 0.1°C resolution, we choose V_{ref1}-V_{ref2}=40mV, C=500pF. Simulated I_{ref1} and I_{ref2} are shown in Figure 2.3.2.2, simulated ΔT is shown in Figure 2.3.2.3.

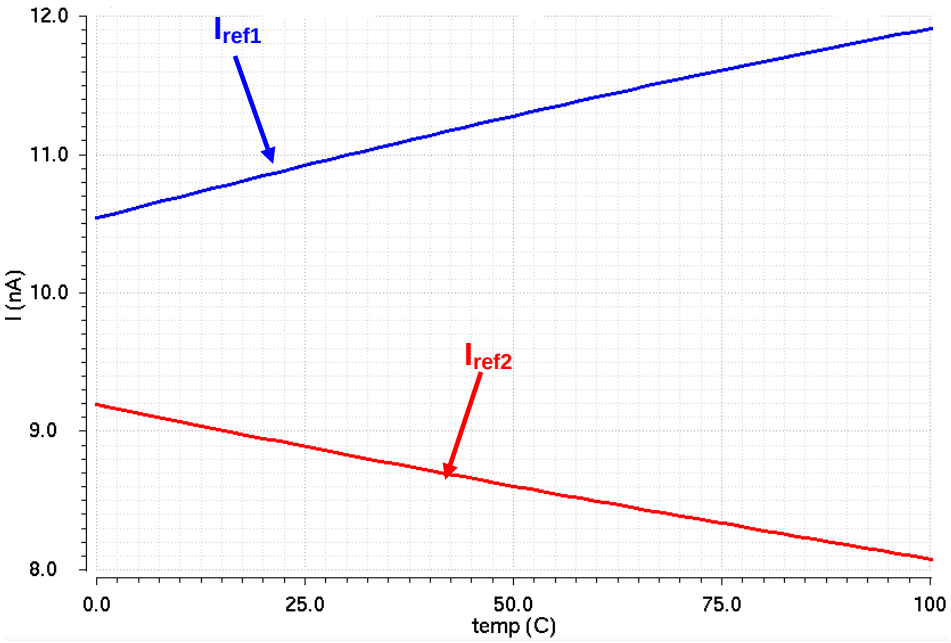


Figure 2.3.2.2. Simulation results for I_{ref1} and I_{ref2}.

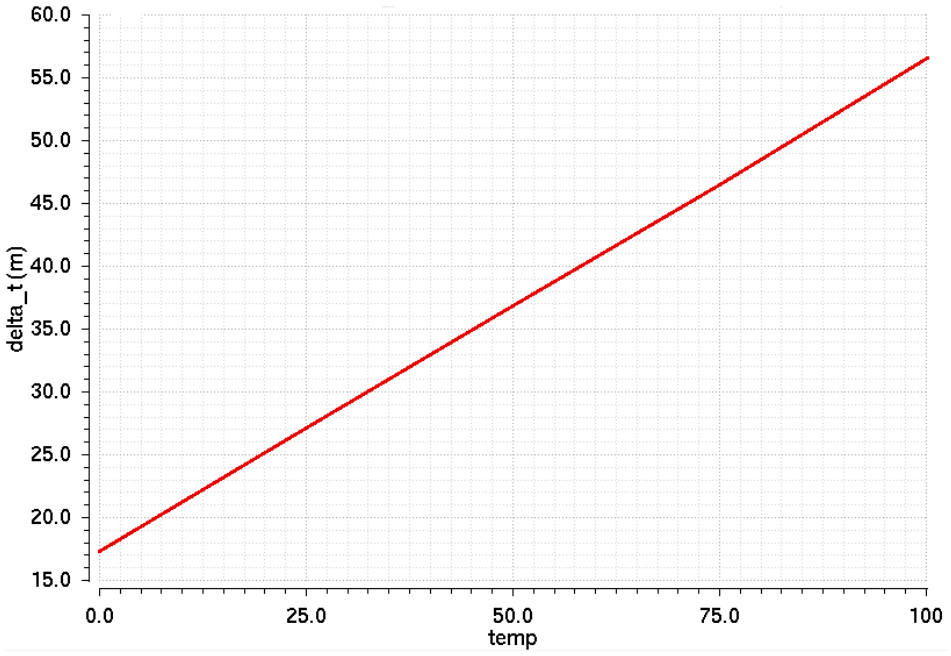


Figure 2.3.2.3. Simulation result for ΔT.

2.3.3 Switching Threshold of Invertor

In Chapter 2.3.2, we assume V_{flip} is a temperature independent constant. But in CMOS technology V_{flip} is determined by multiple factors such as process parameter, temperature, size of transistors, etc. In order to obtain a constant V_{flip}, it is necessary to derive its expression.

For MOSFETs in subthreshold region, the drain to source current can be expressed below. In Figure 2.3.3.1, assuming that for both NMOS and PMOS transistors the drain to source voltage V_{ds}>100mV, drain-induced-barrier-effect and channel-length-modulation can be ignored. If I_p and I_n are very small, we can assume that $V_{out} = \frac{VDD}{2}$ when $I_p = I_n$.

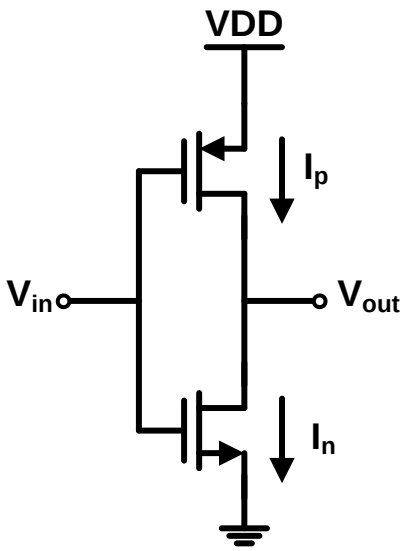


Figure 2.3.3.1 Schematic of invertor.

According to (2.3.1),

$$\begin{cases} I_n = I_{n,0} e^{\frac{(V_{in}-V_{th,n})}{n_n \phi_t}} \\ I_p = I_{p,0} e^{\frac{(VDD-V_{in}-V_{th,p})}{n_p \phi_t}} \end{cases} \tag{2.3.7}$$

Where $I_{n,0}$ is drain-to-source current of NMOS when the gate-to-source voltage equals to threshold voltage, and $I_{p,0}$ has a similar definition. $I_{n,0}$ and $I_{p,0}$ are dependent on process parameters, transistor size, and temperature:

$$\begin{cases} I_{n,0} \propto T^{\frac{3}{2}} \left(\frac{W}{L}\right)_{NMOS} \\ I_{p,0} \propto T^{\frac{3}{2}} \left(\frac{W}{L}\right)_{PMOS} \end{cases} \tag{2.3.8}$$

Let I_n=I_p, we have:

$$\ln\left(\frac{I_{p,0}}{I_{n,0}}\right) = \frac{(VDD - V_{in} - V_{th,p})}{n_p \phi_t} - \frac{(V_{in} - V_{th,n})}{n_n \phi_t} \tag{2.3.9}$$

Now the input voltage V_{in} is equal to the flip voltage V_{flip}. By carefully choosing the size of transistors, we can set $I_{p,0} = I_{n,0}$, then:

$$V_{flip} = V_{in} = \frac{VDD - V_{th,p} + \frac{n_p}{n_n} V_{th,n}}{1 + \frac{n_p}{n_n}} \tag{2.3.10}$$

Notice that $\frac{n_p}{n_n} V_{th,n} - V_{th,p} \approx 0$, we have:

$$V_{flip} = \frac{VDD}{1+\frac{n_p}{n_n}} \approx \frac{VDD}{2} \tag{2.3.11}$$

(2.3.11) indicates that V_{flip} is a proportional to supply voltage *VDD*. Simulation result of V_{flip} is shown in Figure 2.3.3.2.

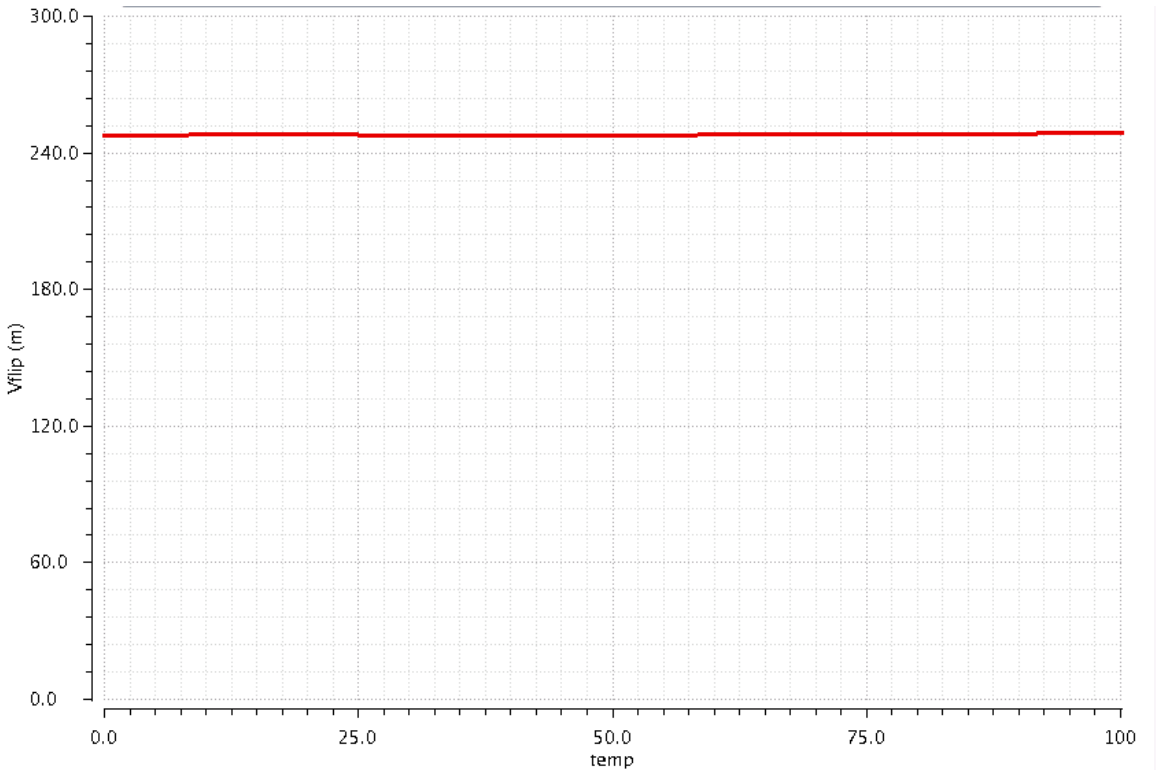


Figure 2.3.3.2 Simulation result of V_{flip}.

2.3.4 Time-to-Digital Convertor

Fig 2.3.4 shows the block diagram and details of the proposed time-to-digital convertor. In Figure 2.3.4(a), Signal "*A*" and "*B*" are the rising edge of the output of temperature-to-delay generator, "*clk*" is the clock generated by oscillator, "*Reset*" is the reset signal for the 13-bit counter. Figure 2.3.4(b) shows the XOR gate using transmission gate. Figure 2.3.4(c) shows the 13-bit counter using self-connected D flip-flops. Figure 2.3.4(d) shows the D flip-flop. Since the clock frequency is relatively low, latches are added at each internal floating node.

Since the flip-flops using standard NFET and PFET are power burning at low operating frequency, high threshold (HVT) transistors are used in flip-flops and latches. Note that the middle transistor of each stage still uses standard transistor, because a HVT transistor may result in insufficient pull-up or pull-down strength.

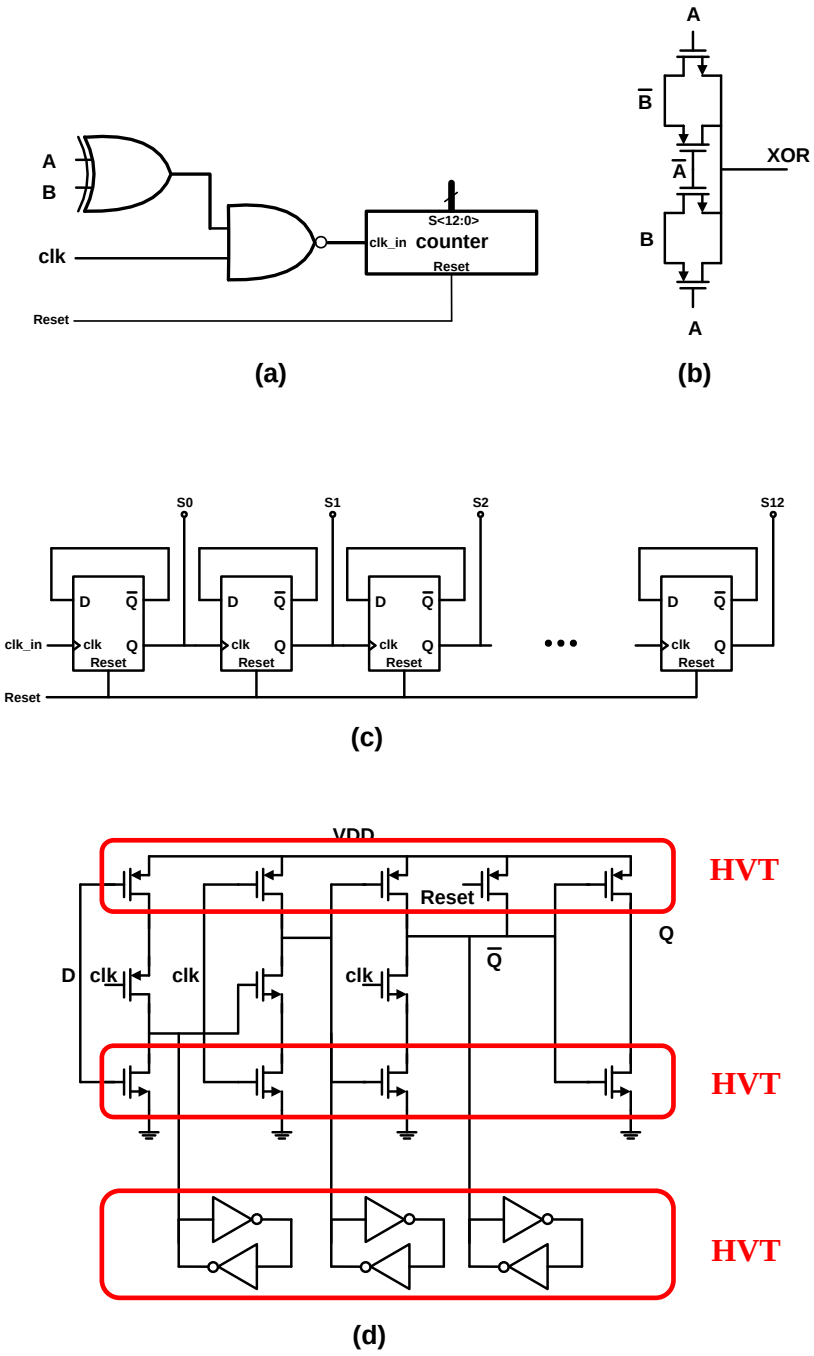


Figure 2.3.4 (a) Time to digital convertor (b)XOR gate (c) Counter (d) D flip-flop

2.3.5 Power Control Strategy

Since the output pulse of temperature-to-delay generator is ~20% of a sampling period, it is a waste of power for the oscillator to keep oscillating all the time. A delay block is proposed to partially power on the oscillator, which saves ~80% of the active power of oscillator.

From Chapter 2.4.3, the flip voltage of an inverter can be expressed as:

$$V_{flip} = \frac{n_n n_p}{n_n + n_p}\left(\frac{VDD - V_{th,p}}{n_p} + \frac{V_{th,n}}{n_n}\right) - \frac{n_n n_p}{n_n + n_p}\ln(\frac{I_{p,0}}{I_{n,0}})\phi_t \quad , \phi_t = \frac{kT}{q} \tag{2.3.12}$$

In the temperature-to-delay generator, the flip voltage is determined when $I_n = I_p$. If $I_n \neq I_p$, the flip voltage will become a temperature dependent variable. In Figure 2.3.5(a), we added another delay inverter which composed of MN_d and MP_d, and we choose the size of this inverter to be:

$$\left(\frac{I_{p,0}}{I_{n,0}}\right)_{delay} > 1 \tag{2.3.13}$$

Then the flip voltage of this delay inverter will be smaller than that of the original invertor with $\frac{I_{p,0}}{I_{n,0}} = 1$. In this way, as shown in Figure 2.3.5(b), the rising edge at "*Delay*" output will be earlier than that of V_{out1}. By properly choosing the size of the delay invertor, the "*Delay*" signal can be further used to power on the oscillator right before the pulse Δt is ready for digitization.

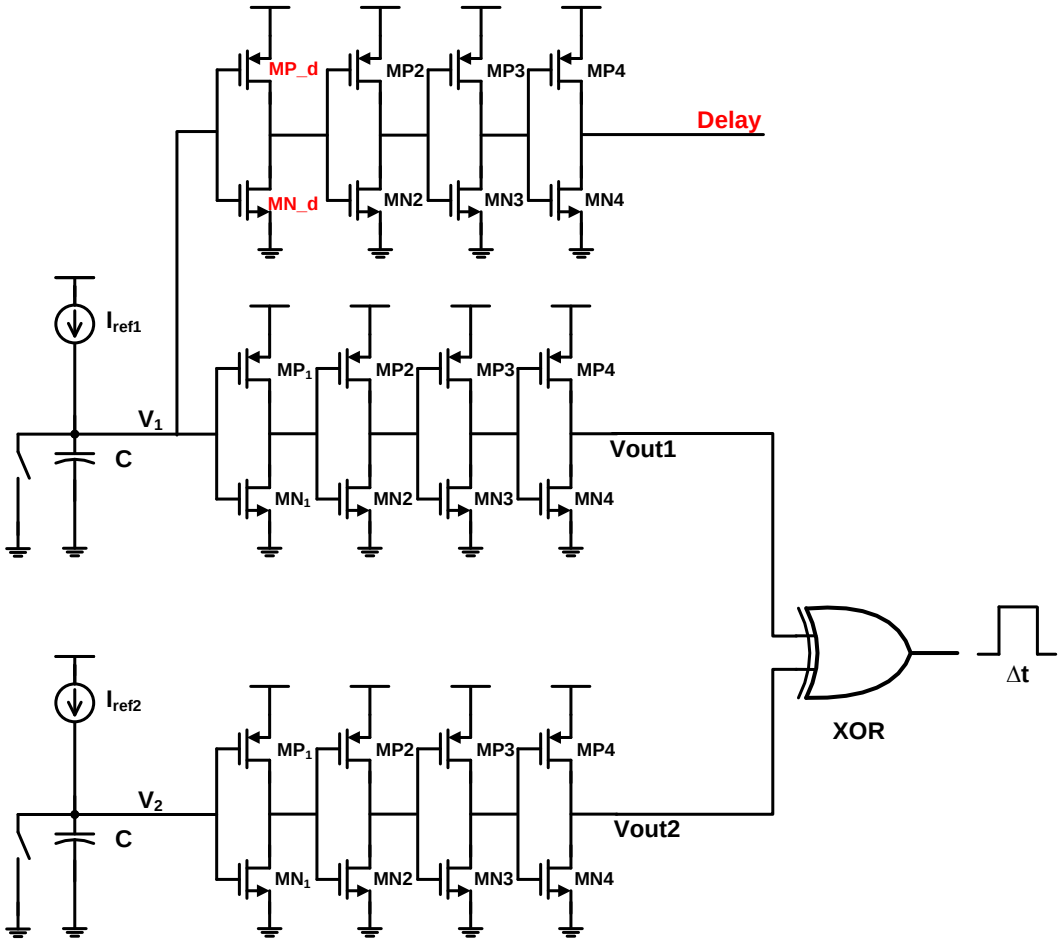


Figure 2.3.5 Oscillator power control circuit (a) Schematic (b) Waveform

2.4 Oscillator Design

2.4.1 Introduction

Oscillator with low frequency (kHz scale) has been widely discussed in recent years. It can be used to serve as a sleep-mode-controller [10] or a clock signal for low frequency application [6]. In those applications the oscillator is always actively working, so it is highly desired to minimize the power consumption. In biomedical and other low power area, operating frequency is limited to kHz scale because of subthreshold region operation. Especially, for temperature related applications, it is very important to develop oscillators at kHz scale with low power consumption and good temperature stability.

In recent years, several low power kHz level CMOS oscillators have been proposed in publications. Among these works, relaxation oscillator based and comparator based design are very popular. In [11], a relaxation oscillator is proposed with 280nW power consumption. A feed-forward period control block is applied to achieve good temperature independency. However, it still suffers from high supply voltage sensitivity, and multiple comparators also lead to higher power.

In [12], a 120nW relaxation oscillator is proposed with offset cancellation, which achieves low temperature coefficient. But this oscillator relies on a PTAT current reference which comes from a 1.5V-3.3V supply voltage, which is not preferred for low power design.

[10] also has the PTAT current reference problem. It proposed a relaxation oscillator that achieves 190nW power consumption and very good long term Allen deviation, but also depend on a 25nW PTAT current reference and lead to a higher supply voltage.

In [13], a 4.48uW 1.6V supply voltage oscillator with self-chopping is applied to achieve very good stability, but both power consumption and supply voltage are high.

On the other hand, gate leakage based timers that achieve very low power consumption (< 1nW) and good temperature stability have been introduced in [14-15]. However, the gate leakage based timers only operate at sub-Hz to a few Hz due to the limited amount of current that they can provide.

2.4.2 Oscillator Topology

Figure 2.4.2 shows the architecture of the proposed oscillator. I_{ref} is temperature independent of the current reference. We start to analyze from node A1, in the first half period, assuming A_1 = 0V when t = 0, I_{ref} starts to charg node A_1, voltage of A_1 then increases linearly until $A_1 = V_{flip}$, V_{flip} is the flip voltage of the invertor. Then B_1 turns from "0" to "1", consequently after a latch node C turns from "0" to "1", which closes switch S_2 and discharges node A_2. The invertors and latch will generate a delay, which is a nonlinear value that exponentially depending on temperature. The variation is controlled to be less than 0.1% of an oscillation period. In the second half period, when C turns to "1", switch S_2 opens and node A_2 start to discharge in the same pattern of A_1 as in the first

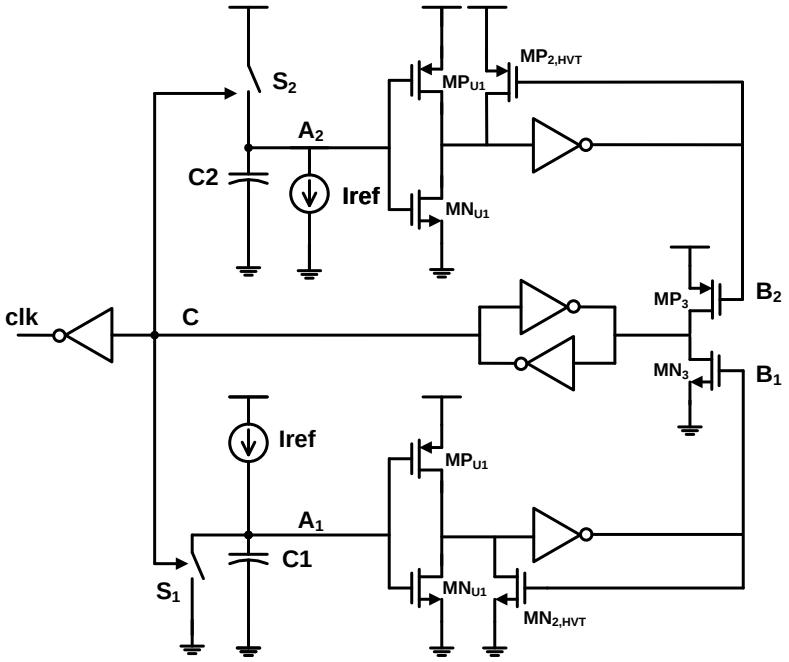
half period. Then B_2 drops from “1” to “0” and C behaves the same way, which repeats the first half period.

The delay time is harmful because it introduces a nonlinear time component to a oscillation period. $MP_{2,HVT}$ and $MN_{2,HVT}$ are added to reduce the delay time. This helps to reduce delay caused by the first and second stage invertors.

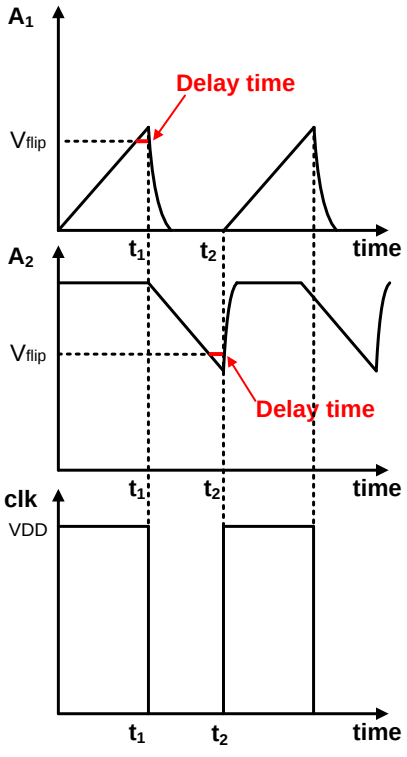
Then the period of oscillator can be derived as:

$$\begin{aligned} T_{period} &= \frac{CV_{flip}}{I_{ref}} + \frac{C(Vdd - V_{flip})}{I_{ref}} \\ &= \frac{CVdd}{I_{ref}} \end{aligned} \tag{2.4.1}$$

Since capacitance C is a fixed value, the oscillation period T_{period} only depend on supply voltage and reference current.



(a)



(b)

Figure 2.4.2 (a) Schematic of oscillator (b) Waveform of oscillator operation.

2.4.3 Reference Current Generation

According to (2.4.1), the oscillation period is determined by *VDD* and I_{ref}, and shows a strong supply voltage dependency. In order to achieve good supply voltage stability, a reference current generation circuit is proposed in Figure 2.4.3. From the tradeoff between power and area, we choose I_{ref} = 10nA, R=4MΩ. Then we have:

$$I_{ref} = \frac{\frac{2}{5}VDD - \frac{2}{6}VDD}{R} = \frac{1}{15}\frac{VDD}{R} \tag{2.4.2}$$

Substitute (2.4.2) into (2.4.1),

$$T_{period} = 15CR \tag{2.4.3}$$

Then (2.4.3) shows that the oscillation period has no supply voltage dependency.

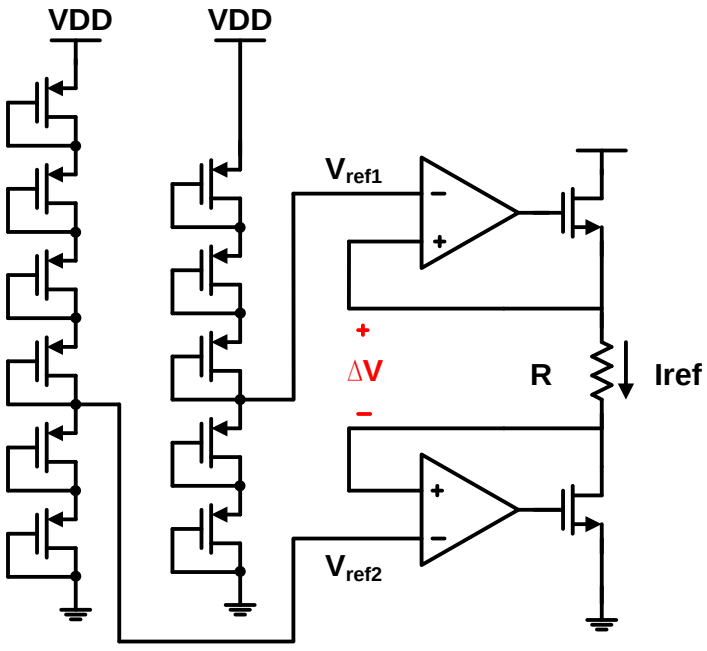


Figure 2.4.3 Oscillator reference current generator.

2.4.4 Resistor Calibration

In (2.4.3), the temperature coefficient of capacitor C is too small that to be considered. But resistors usually have non-ignorable temperature coefficient. One way to obtain temperature independent resistor is to combine two resistors with opposite temperature coefficient in series, as shown in Figure 2.4.4.1.

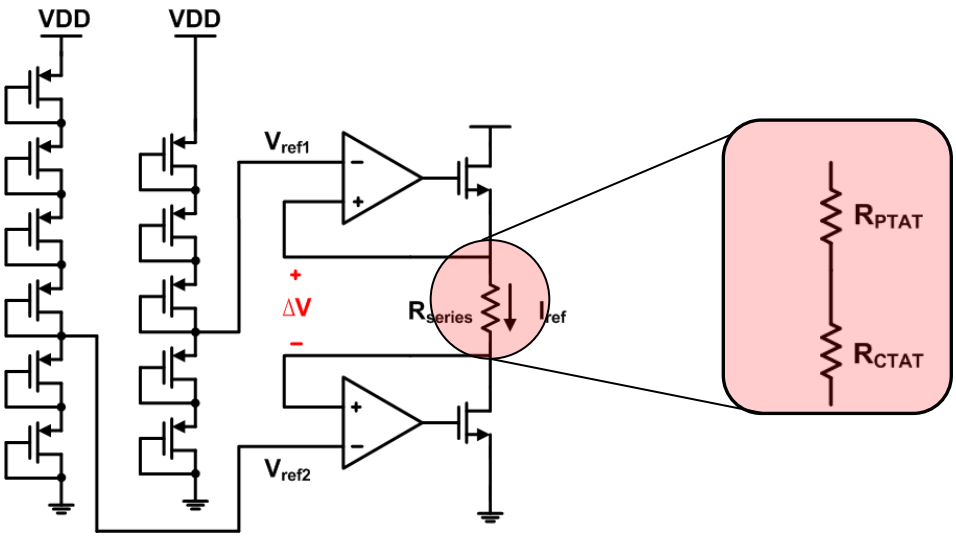


Figure 2.4.4.1 Oscillator reference current generator.

As discussed in Chapter 2.3.2, the resistance of a PTAT and CTAT resistor in series is:

$$R_{series} = R_{0,ctat}(T_0) + R_{0,ptat}(T_0) + \left(R_{0,ptat}(T_0)k_{ptat} + R_{0,ctat}(T_0)k_{ctat}\right)\Delta T \tag{2.4.4}$$

Since k_{ptat} is positive and k_{ctat} is negative, we can cancel the ΔT term by choosing the proper resistance of R_{PTAT} and R_{CTAT}.

Considering process variation may result in a 10~20% resistance variation, here we apply a binary-weighted resistor calibration as shown in Figure 2.4.4.2. R_{PTAT0} and R_{CTAT0} are dominant resistor, both are equal to 1MΩ. The minimum resistance step R_{PTAT} is 130kΩ and R_{CTAT} is 165kΩ.

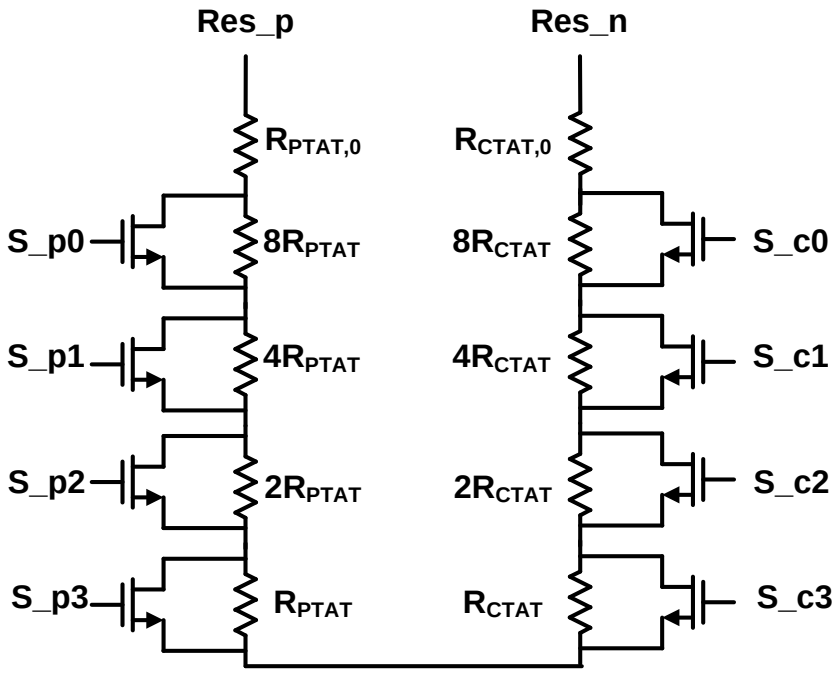


Figure 2.4.4.2 Resistor calibration.

2.5 Layout

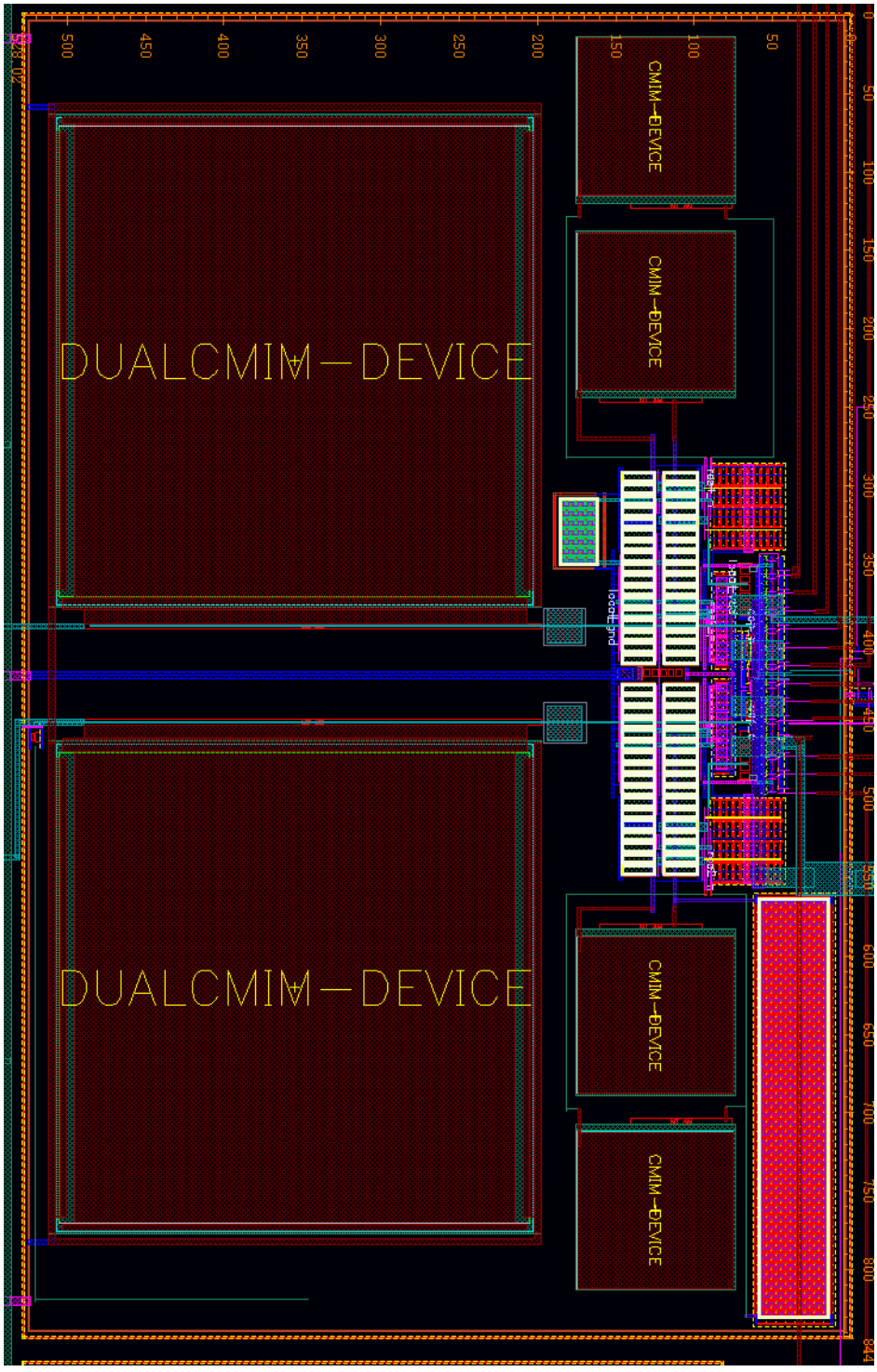


Figure 2.5.1. Temperature Sensor (530um*850um).

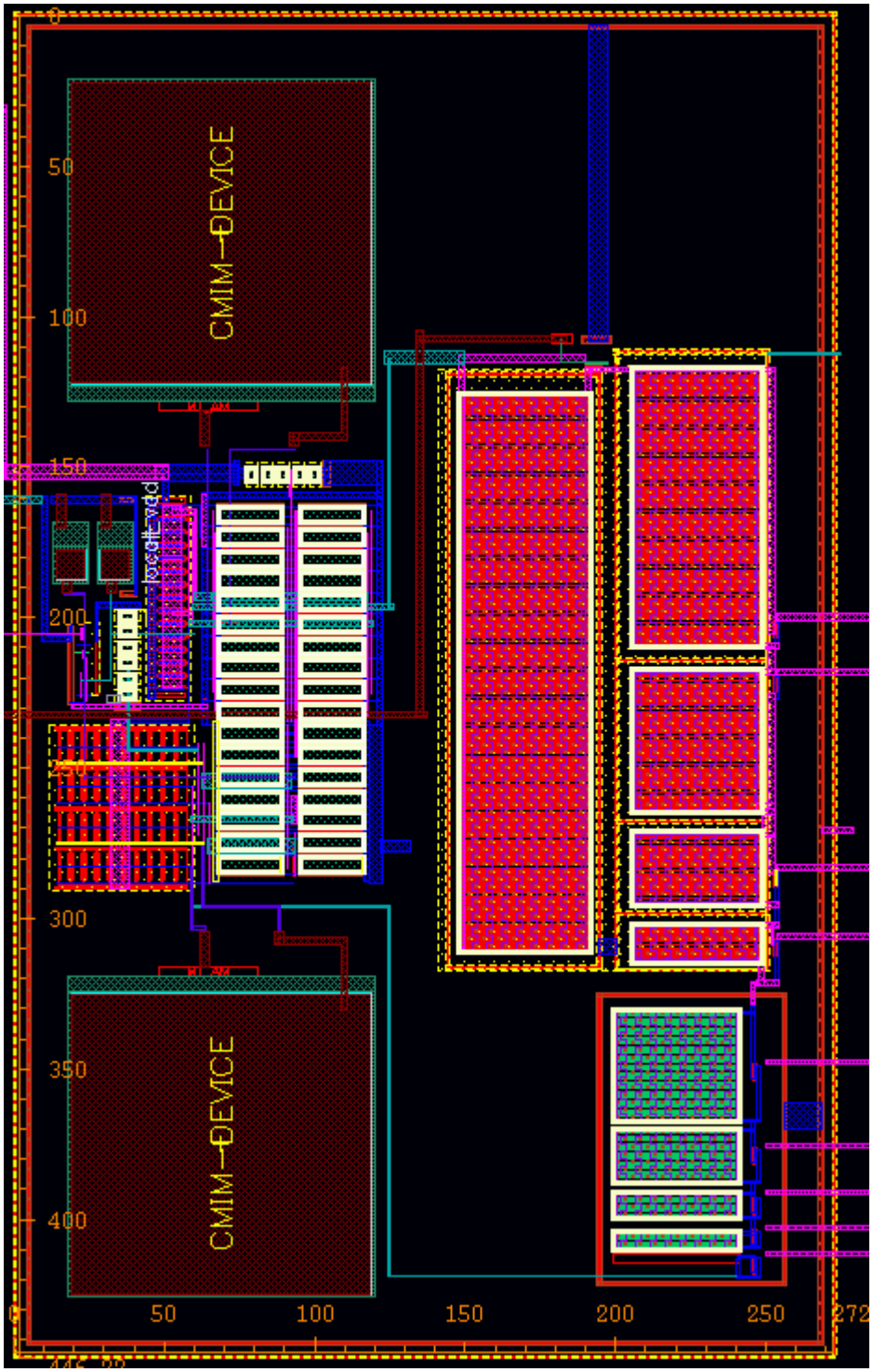


Figure 2.5.2. Oscillator (27um*450um).

CHAPTER 3 Simulation Results

3.1 Simulation Results for Oscillator

Figure 3.1.1 shows the supply voltage immunity of oscillator. With 0.6V center value, when supply voltage varies ±100mV, the output frequency performs a variation of 1.2%/V. This result is promising no LDO or specific external reference current.

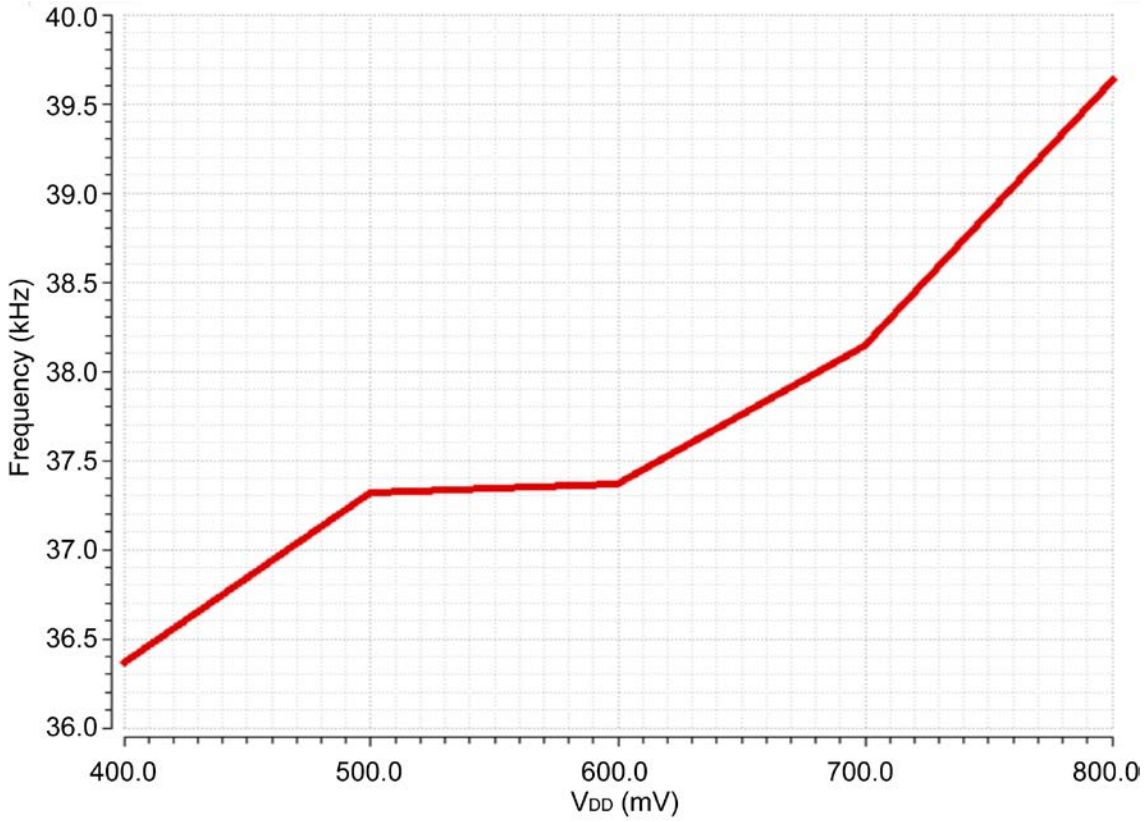


Figure 3.1.1 Oscillation frequency vs. supply voltage.

Figure 3.1.2 shows the plot for oscillation frequency vs. temperature. From 0°C to 100°C, the frequency changes ±0.13%, indicating 13ppm temperature coefficient. Compared with previous researches in Table.3, this work achieves good power consumption and temperature coefficient.

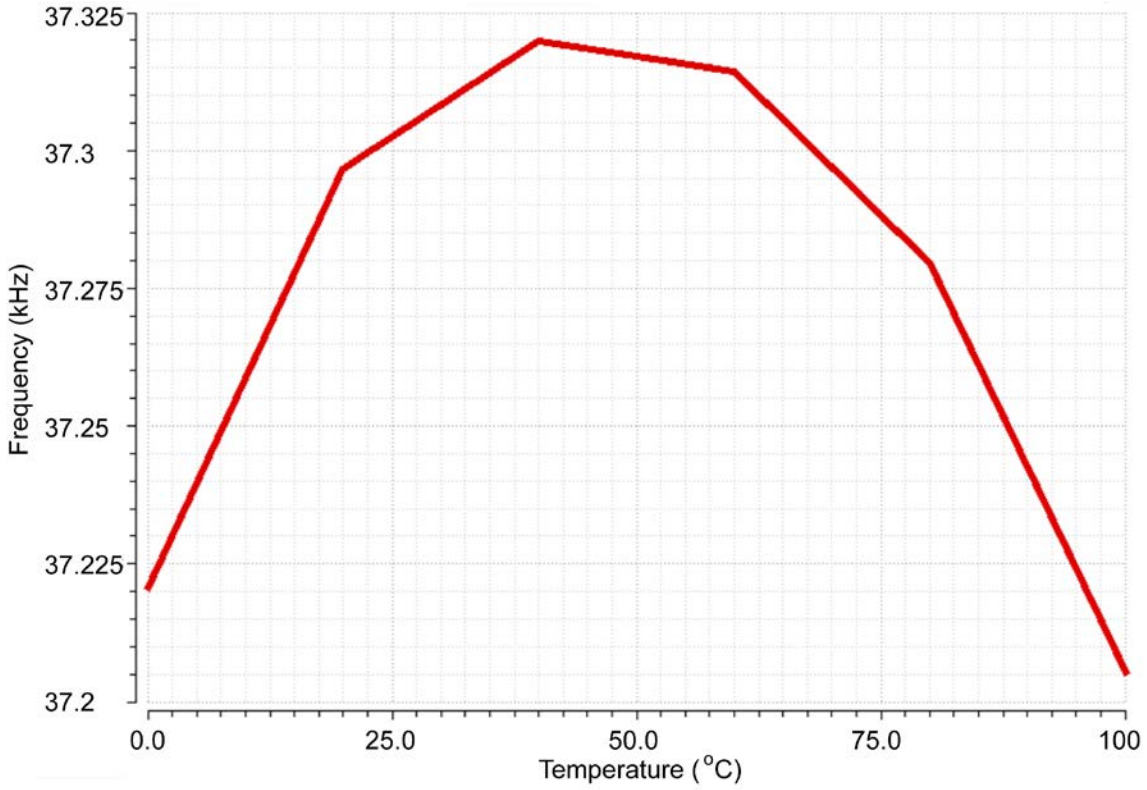


Figure 3.1.2 Oscillation frequency vs. temperature.

Table.3. Summary of the proposed oscillator and comparison with previous researches on low power oscillator.

	VLSI'12[11]	VLSI'12[13]	ISSCC'13[12]		JSSC'09[16]	ISSCC'14[10]	This work
Process	90nm	60nm	65nm		65nm	65nm	180nm
Area [mm2]	0.12	0.048	0.032		0.11	0.015	0.1
Freq (kHz)	100	32.768	18.5		100	33	30-40
Power	280nW	4.48uW	120nW		20.8uW	190nW	17nW
Temp Accuracy (%)	±0.68	±0.1	±0.25	±0.1	±1.1	±0.21	±0.13
Temp Range (°C)	-40 to 90	-20 to 100	-40 to 90	0 to 90	-22 to 85	-20 to 90	0 to 100
Voltage Accuracy (%/V)	9.4	0.06	1		0.37	0.09	1.2
Allan Deviation Floor	N/A	N/A	< 20ppm		~1000ppm	<4ppm	N/A

3.2 Simulation Results for Temperature Sensor

Table.4 records 5 samples of temperature sensor output from 0°C to 100°C. Data of samples are plot in Figure 3.2.1. In this temperature range, the temperature sensor and shows 0.55°C inaccuracy and 0.1°C resolution. Table.5 shows the performance summary of this work and comparison with previous researches on low power temperature sensor. The active power of this work is 62nW at 27°C.

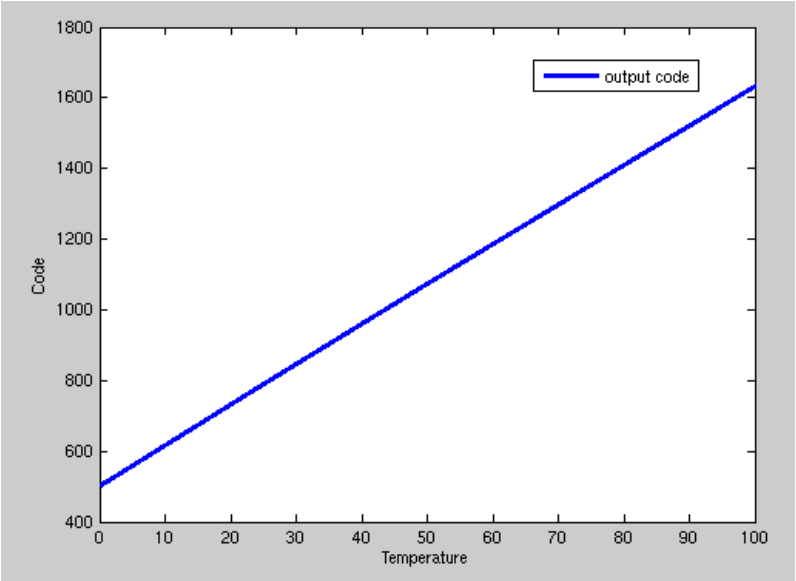


Figure 3.2.1 Output Code of Temperature Sensor.

Table.4. Output Code of Temperature Sensor.

Temperature	0	25	50	75	100
Code	505	792	1076	1353	1635

Table.5. Summary of the proposed temperature sensor and comparison with previous researches on low power temperature sensor.

	JSSC'14[6]	CICC'08[5]	ASSCC'07[**17**]	TCSII'12[4]	ISSCC'04[18]	This Work
Power	71nW	220nW	110nW	405nW	600nW	62nW
Resolution(^{0}C)	0.3	0.1	0.035	0.3	0.063	0.1
Supply(V)	1.2	1	1.4,2.1	1.2	0.85-1.2	0.6
Inaccuracy(^{0}C)	+1.5/-1.4	+3/-1.6	+0.1/-0.1	+1/-0.8	±0.4	±0.28

CHAPTER 4 Conclusions and Future Work

4.1 Conclusions

The design of a 62nW temperature sensor based on the time-to-digital conversion is proposed in this work. The temperature sensor was designed to achieve 0.1°C resolution, a 0.55°C inaccuracy, a 200mSec sampling period and a 0~100°C operation range. With 0.1°C resolution and 0.55°C inaccuracy, this work is suitable for precise temperature measurements such as human body temperature monitoring. With 62nW active power, this work is able to be integrated with low power sensor platforms subjected to the sub-uW power budget.

The dual-amplifier reference current generator was used in the oscillator to achieve better supply voltage stability and less inaccuracy. The improvement in oscillator highly reduced the accuracy of the whole temperature sensor. The reference voltage that proportional to the supply voltage is fed to the reference current generator to achieve good immunity to power supply. The oscillation setup time is one clock period, the short setup time makes the oscillator suitable for applications with low sampling frequency and power gating technique.

Reverse-to-absolute-temperature reference current is applied to temperature-to-pulse generator, which avoided any math approximations and maintains a good temperature coefficient linearity. To further reduce the oscillator power, the temperature-to-pulse generator will power on the oscillator right before the voltage pulse is ready for digitization.

4.2 Future Work

Although this work already achieves very low power consumption, good accuracy and resolution, several problems still exist. First, the resistors in oscillator need calibration which limits the easiness of use. It is highly desired to find out an architecture that has no or less requirement for calibration. Second, two reference current generators in temperature-to-pulse generator applied four amplifiers with each one consuming about 10nW, this is the main portion of overall power budget. By carefully utilizing supply voltage, it is possible to design the reference current generator with a single amplifier and further reduce power consumption.

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