Title
PEP- 4 INNER AND OUTER DRIFT CHAMBER SYSTEM

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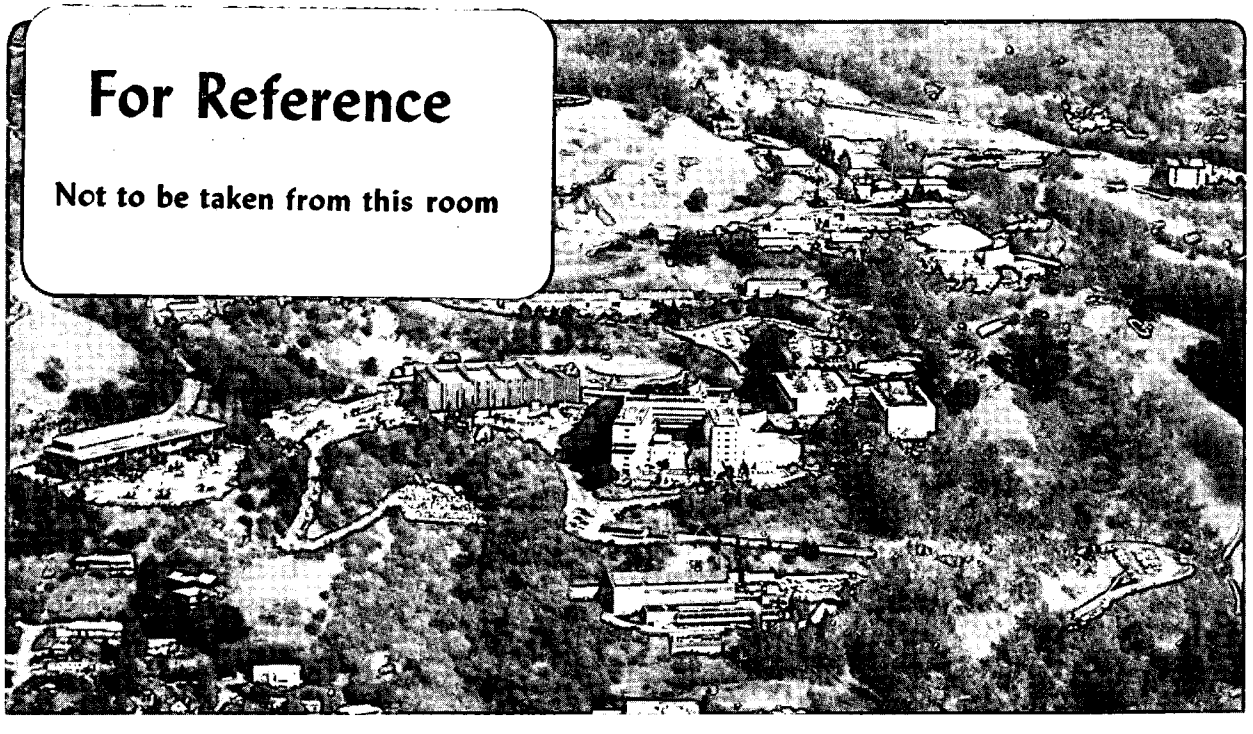

DISCLAIMER

Outer Drift Chamber

It is planned to use the same circuitry on the outer drift chamber as was described for the inner chamber since the electronic performance is more than sufficient, and it would cost more to develop and produce new circuits. The outer drift chamber differs in two ways from the inner. One is the distribution of test pulses and the other is the signal needed for the trigger circuitry.

The configuration of the single layer drift chamber is shown in Fig. 1b. The width of the cell is chosen so that the maximum drift time is less than 100 nsec which is required for the trigger system. The signal labeled to outer trigger on Fig. 2 is the fast "or" of all 8 channels and is within 100 nsec of the beam C/O.

The test pulses (36 total) are on every third wire for 30° arcs and offset by 15° with the segments in the TPC end caps.

Specifications of Inner and Outer Drift Chamber Systems

The following is a list of specifications for the system.

Mechanical

1. The inner drift chamber will contain 240 sense wires in four layers at 6° spacing.
2. The outer drift chamber will contain 600 ± 100 sense wires (not tightly defined yet).
3. There will be one preamplifier per wire.
4. Mounting of the inner drift chamber preamplifier will be between the TPC and the pole tip calorimeter at the inner radius on a ring motherboard.
5. Alternate rings of wires for the inner drift chamber will exit at alternate ends of the chamber.
6. Mounting of preamplifiers for the outer drift chamber will be just outside the drift chamber. (Possibly in the annular recess between the magnet and calorimeter which will be 2-3 cm wide.)

Electrical: Chamber Signals, Cable, Preamplifier, and Related Digitizer Requirements

1. Signals from the sense wires are to be near ground potential by appropriate application of high voltage (4 kV) to field wires, or else to sense wires with the use of blocking capacitors at the drift chambers.
2. Gain of chamber to be minimized (10^3-10^4).

SUBJECT
PEP-4 INNER AND OUTER DRIFT CHAMBER SYSTEM

NAME
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DATE
September 30, 1977

This note is to document the preliminary design criterion of the inner and outer drift chambers and will serve as a firm document to guide the development of the electronics system. The objectives of the design will be to provide the physics objectives at a minimun of cost with a reasonably simple and reliable electronic system.

Inner Drift Chamber

The inner drift chamber is composed of 240 cells each 6° wide in four layers as shown in Fig. 1. A fourteen-cell model that is 1.3 meters long is being supplied by John Layter to aid in the design of the preamplifier, signal shaping circuit, and discriminator. This circuitry must satisfy the objectives needed for triggering and momentum analysis.

The momentum analysis requires a resolution of 150 μm (rms) within a drift cell that is ~9000 μm wide. This corresponds to 2.12 nsec (rms) resolution of the electronic circuitry that subdivide the 140 nsec maximum drift time into 70 channels. The electronics will be designed to obtain 2 nsec (rms) with a stretcher that has a 8 bit (256 channel) output. There will be two time stretchers per channel.

The trigger requires that the tracks are radial within 4.75° (ΔT 28 nsec with drift velocity of 7 cm/μsec) and are within 25 nsec of the beam crossover (C/O) time. The time jitter requirements associated with this are easily met by the 2 nsec (rms) needed for the drift circuitry. In addition, the trigger will need to respond to multiple tracks within a drift cell; therefore, good pulse pair resolution will be needed. The design goal will be to obtain pulse pair resolution of less than 50 nsec.

Combining the above information with the system aspect of the PEP-4 electronics, yields the block diagram shown in Fig. 2. The preamplifiers, eight to a card, are mounted on a circular motherboard located between the Time Projection Chamber (TPC) and the end cap calorimeter. The motherboard distributes power and test pulses (six test pulses per end). There are 120 preamplifiers per end where the first and third radii of the drift chamber are on one end and the second and fourth on the other. Ribbon type coaxial cable is probably used to connect the preamplifiers to the digitizer card in the electronics house. (The cards are located in two bins on opposite sides of the house.) In operation, the circuitry has been reset before the beam C/O time. A linear signal that exceeds the computer controlled discriminator stops the time stretcher and causes a logic signal to be sent to the trigger system. The time stretcher continues to digitize the data and produce the 8 bit output. At 2 μsec after the beam C/O, the trigger circuits will make the decision whether it transmits a HOLD or RESET signal to the card. HOLD is generated if there is a pretrigger and RESET is generated if there is no pretrigger. HOLD will prevent any further triggering of the discriminator. After sufficient time (dependent on the clock frequency yet to be decided) for all time stretchers to finish digitization, the readout controller starts reading the drift times and addresses over the readout bus. When the data is completely readout, HOLD is released and the system is reset.

There will be provision for injecting test pulses on every wire input line at the preamplifier and a common test pulse to every digitizer card.

3. Signal rise time from chamber 10-30 nsec.

4. Positional accuracy required 150 μm (rms).

5. The preamplifiers must be capable of driving an appropriate terminated cable 100' in length.

6. Maximum crosstalk in the preamplifier/cable/receiver system will be determined later.

7. Jitter allowable due to electronics should be held at 2 to 4 nsec maximum.

8. Maximum drift time in inner chamber is 140 nsec. Outer chamber is 100 nsec.

9. The desired time/space resolution of the digitizer is 256 bins (8 bits).

10. Address generator needed on digitizer boards to locate wire.

11. Test points should be provided to allow examination of signals ahead of comparator on the digitizer boards without disturbing normal operation.

12. There are 30 cards of 8 channels each for the inner drift chamber.

13. There are 75 ± 12 cards for the outer drift chamber.

14. The digital signals used in communicating to and from the digitizer card are TTL negative-true levels.

15. The following definitions refer to the signals shown on Fig. 2.

TO OUTER TRIGGER $\triangleq$ true if any one of the 8 channels is within 100 nsec of the beam C/O.

TO INNER TRIGGER $\triangleq$ eight lines, each line is independent of the other lines and presents the discriminator output to the trigger system. The pulse pair resolution should be a minimum ($\leq$50 nsec).

TEST IN $\triangleq$ a common signal to all 8 channels that causes the discriminator to fire.

RESET $\triangleq$ reset all parts of the card except the discriminator level and shaper-width control registers.

HOLD $\triangleq$ prevents the discriminator from being triggered.

C/O $\triangleq$ a timing signal that specifies when there was a beam C/O.

READOUT BUS $\triangleq$ 21 bits total: 8 bits for time; T_0-T_7. Ten bits for address; A_0-A_9. Three bits for control; DATA PRESENT, ENABLE, ADVANCE.

The DATA PRESENT signal is active whenever there is any data in any of the digitizer card registers. It originates on the digitizer cards and is used in the controller.

The ENABLE signal is generated by the controller and is used on the digitizer cards to place one data word at a time onto the READOUT BUS. The signal progresses from digitizer cards with low addresses to those with higher addresses. It progresses on command from the controller, i.e., the ADVANCE pulse which the controller generates after it has latched the previous data word.

DISCRIMINATOR CONTROL BUS $\triangleq$ the discriminator control is accomplished by having a 4-bit register per channel that controls (via a D and A converter) the discriminator setting (base +40% in 16 steps). These bits, for all channels connected to the readout controller, form a long-shift register that can be shifted in or out from the computer via the controller by means of two control lines and one data line. There is also one four-bit register per channel (in the same register string) which will control (via another D to A converter) the width of the reshaping one-shots in a range of 20-40 nsec.

THRESH DIRECTION $\triangleq$ True to transfer from controller to register. Not true to transfer from register to controller.

THRESH SHIFT CLOCK $\triangleq$ True edge shifts data.

THRESH DATA $\triangleq$ True for 1. Not true for 0.

MASTER CLR $\triangleq$ clears all registers, counters, etc., on the digitizer board.

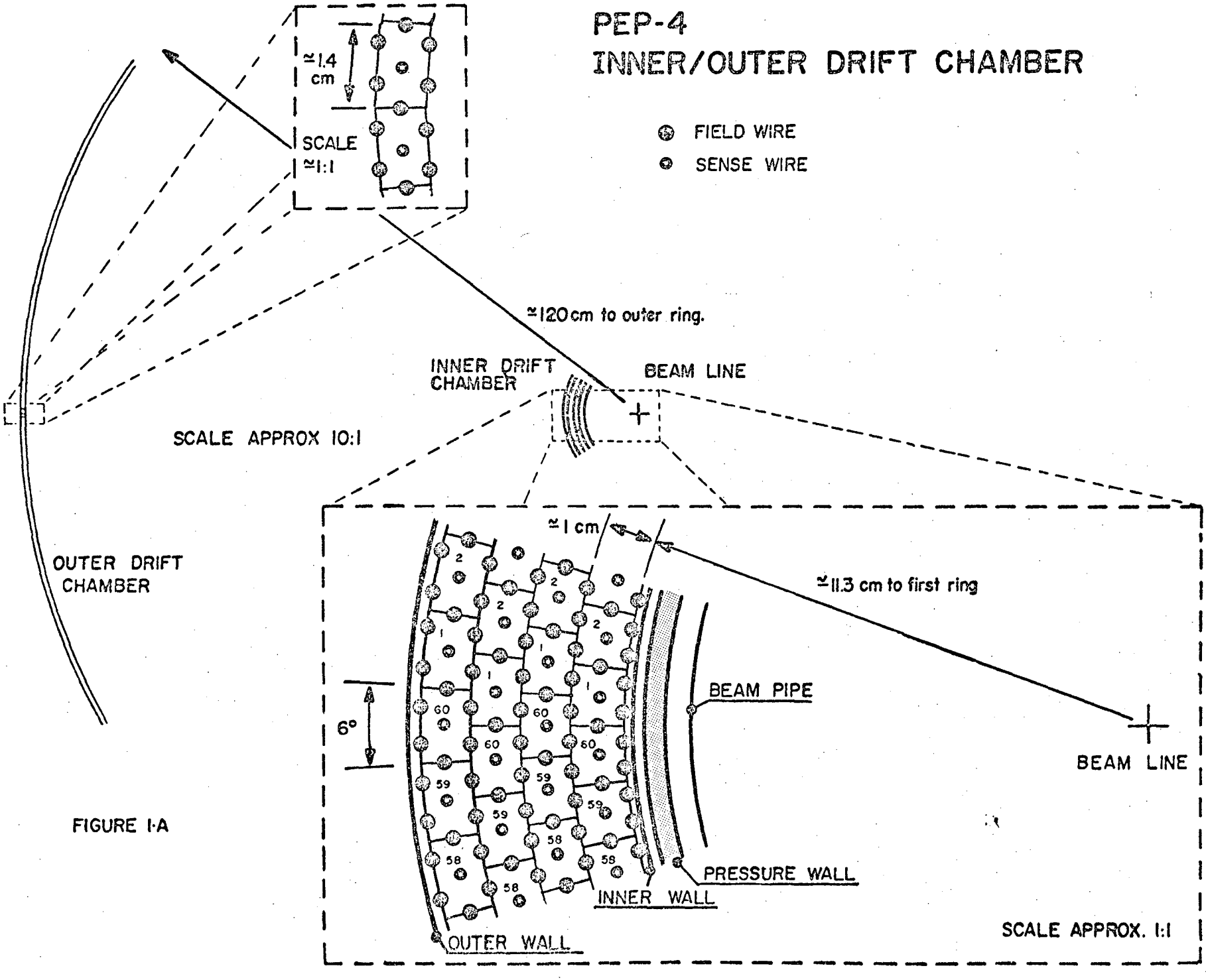
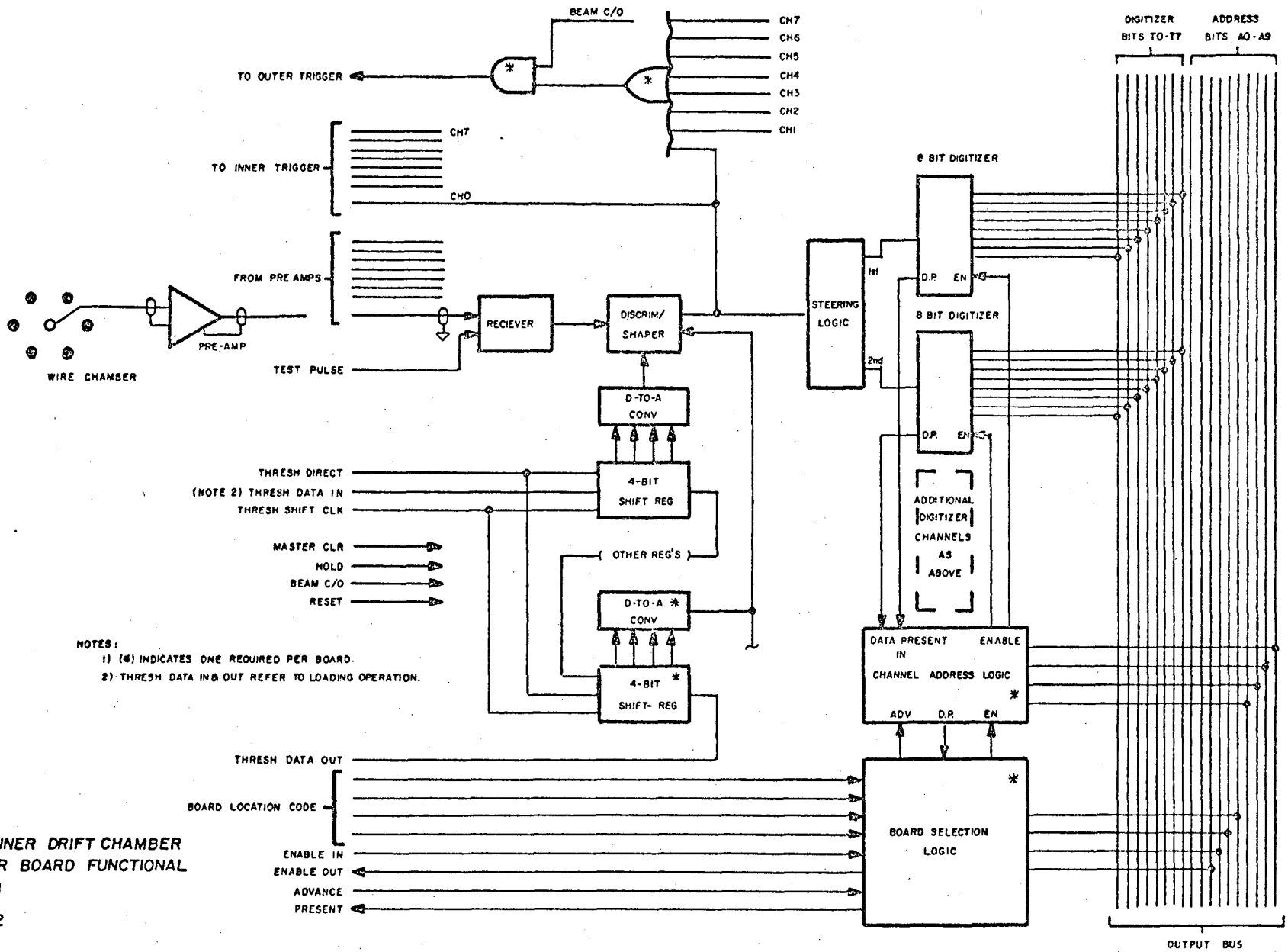

PEP-4
INNER/OUTER DRIFT CHAMBER
FIELD WIRE
SENSE WIRE
≃1.4 cm
SCALE ≃1:1
≃120 cm to outer ring.
INNER DRIFT CHAMBER
BEAM LINE
SCALE APPROX 10:1
OUTER DRIFT CHAMBER
≃1 cm
≃11.3 cm to first ring
6°
BEAM PIPE
BEAM LINE
PRESSURE WALL
INNER WALL
OUTER WALL
SCALE APPROX. 1:1

FIGURE 1-A



PEP-4 INNER DRIFT CHAMBER DIGITIZER BOARD FUNCTIONAL DIAGRAM

FIGURE 2

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