Title

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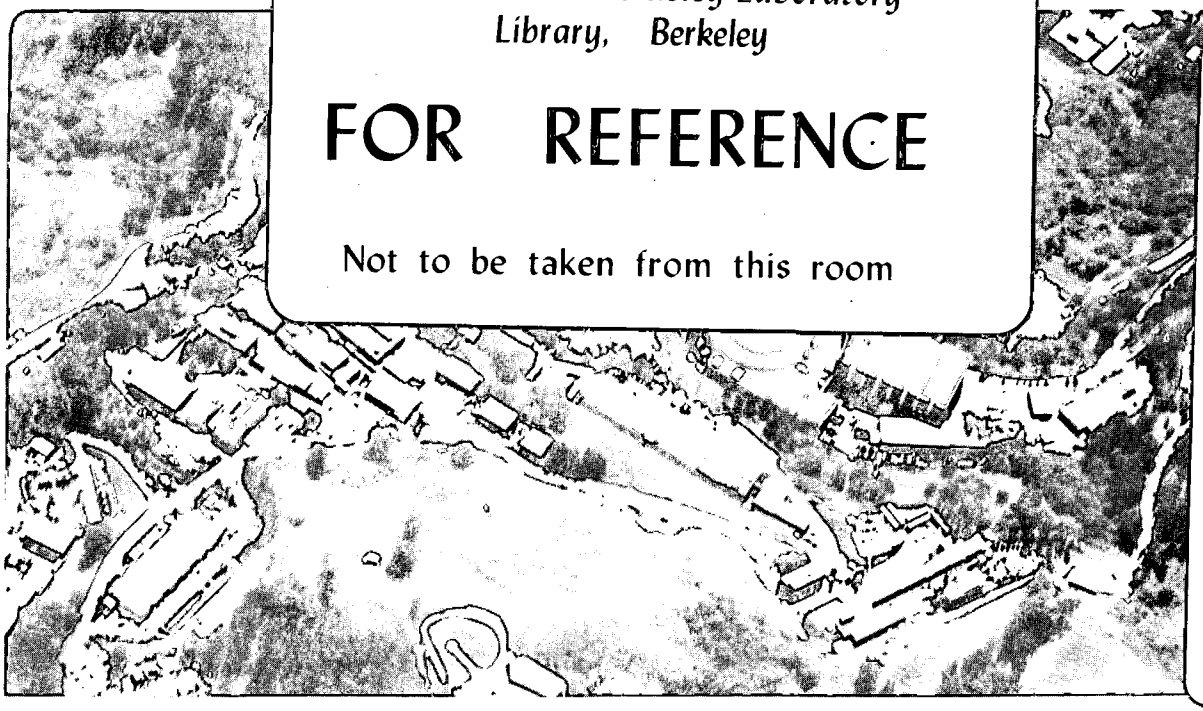

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Properties of CMOS Devices and Circuits Fabricated On High-Resistivity, Detector-Grade Silicon

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Abstract- A CMOS process that is compatible with silicon p-i-n radiation detectors has been developed and characterized. A total of twelve mask layers are used in the process. The NMOS device is formed in a retrograde well while the PMOS device is fabricated directly in the high-resistivity silicon. Isolation characteristics are similar to a standard foundary CMOS process. Circuit performance using 3 μm design rules has been evaluated. The measured propagation delay and power-delay product for a 51-stage ring oscillator was 1.5 ns and 43 fJ, respectively. Measurements on a simple cascode amplifier results in a gain-bandwidth product of 200 MHz at a bias current of 15 μA. The input-referred noise of the cascode amplifier is 20 nV/$\sqrt{\text{Hz}}$ at 1 MHz.

1. Introduction

The ability to monolithically integrate detectors and readout electronics on the same substrate offers new possibilities and challenges in the field of radiation detection. Advantages of on-chip readout electronics include minimization in the number of external connections, reduction of parasitic capacitance due to detector readout coupling, and improved reliability. We have previously described the monolithic integration of silicon p-i-n radiation detectors and PMOS circuitry on the same high-resistivity silicon substrate [1]. In that work a depletion-mode technology was used to realize charge-sensitive preamplifiers integrated with radiation detectors. Detection of the Am^{241} 60 keV gamma ray was demonstrated with a signal to noise ratio of 30 to 1 at a shaping time of 200 ns. The detector element was a 1.4 mm^2 p-i-n diode. Given this encouraging result we have focused our attention on improving the readout electronics technology. For this purpose we have begun the development of a CMOS technology that is compatible with silicon radiation detectors.

CMOS circuitry has several advantages when compared to what is possible in a depletion-mode technology. Depletion-mode logic circuits dissipate significant amounts of power in the quiescent state, and it is difficult to achieve large values of output resistance in analog circuits due to the inability to cascode the depletion load, unless positive feedback methods are used. As as result, a long-channel depletion load is required for high voltage gain and the resulting capacitance limits the achievable gain-bandwidth product. CMOS cascode amplifiers do not suffer from this limitation since both n-channel and p-channel devices at the amplifier output can use source degeneration to increase the output resistance. Hence the load devices can be small-area devices which reduces the output capacitance when compared to a long-channel depletion load. In addition, the PMOS devices have relatively poor transconductance in the strong inversion region due to the fact that the low-field hole mobility is much less than the electron mobility.

In this work we report the results of the development of a detector-compatible CMOS process. CMOS circuitry on high-resistivity silicon was first proposed in 1969 [2], and more recently in the context of compatibility with radiation detectors by Vanstraelen et al [3]. By employing an effective gettering process we are able to use standard CMOS fabrication techniques throughout the process. This is necessary to achieve acceptable packing density and device performance. In order to allow for detector-compatibility the substrate must be fully depleted during operation and hence the substrate bias voltage is much larger than in a standard CMOS process.

A CMOS test chip has been designed, fabricated and tested. The test chip contains NMOS and PMOS transistors of various geometries, test structures for isolation studies, and simple circuitry. This allows for the characterization of both the circuit performance and packing density (device isolation) possible with this technology. In the next section we describe the process with particular emphasis on the design and experimental results for the NMOS device. Circuit performance is presented in Section 3.

2. CMOS Process/NMOS Design

The CMOS fabrication process used in this work requires 12 masking layers and 8 ion implantation steps. The starting substrates are high-resistivity (≈ 8–10 kΩ-cm), detector-grade silicon substrates purified by float-zoned refining. The substrates are phosphorus-doped, n type. As in a conventional MOS process the crystalline orientation is <100>. The gate oxide thickness is 20 nm in order to minimize PMOS punchthrough and increase the transistor output resistance [1].

The p-channel devices are as described in the previous publications on the depletion-mode PMOS technology [1,4],

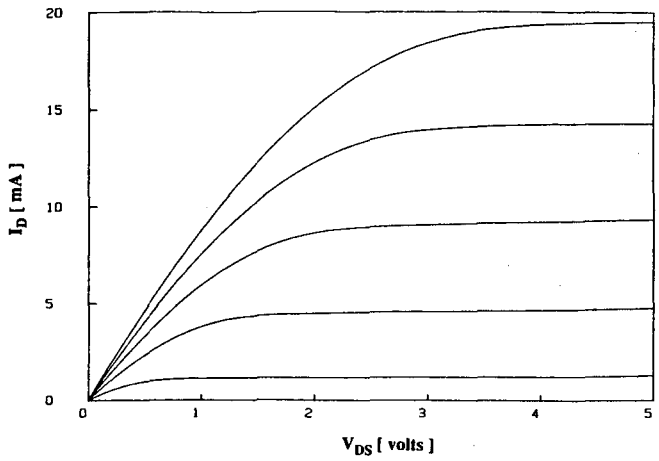
and are formed in the high-resistivity silicon without a well. The threshold voltage for the transistors is controlled by shallow implants through a sacrificial gate oxide. Enhancement, depletion, and unimplanted PMOS devices are available in this technology. The substrate bias used to deplete the p-i-n detector is also beneficial in terms of reducing the PMOS punchthrough [3]. Since the NMOS device is in a well it is unaffected by the substrate bias. For the circuits described in this work the p-channel punchthrough was acceptable although scaling of the technology to the 1 μm level will require substantial improvements in the PMOS device design.

A backside polysilicon gettering process maintains the detector reverse leakage current at approximately 1 nA/cm^2 [5], and allows for the use of conventional CMOS processing techniques throughout the fabrication process. There are no unusual restrictions on either the temperatures of the furnace steps or the use of plasma etching in the process. Both the nitride layer used to delineate the active transistor regions and the gate polysilicon layer are etched in a plasma chamber. Plasma etching of the contact and metal layers would have been preferred but was not possible due to the lack of suitable equipment.

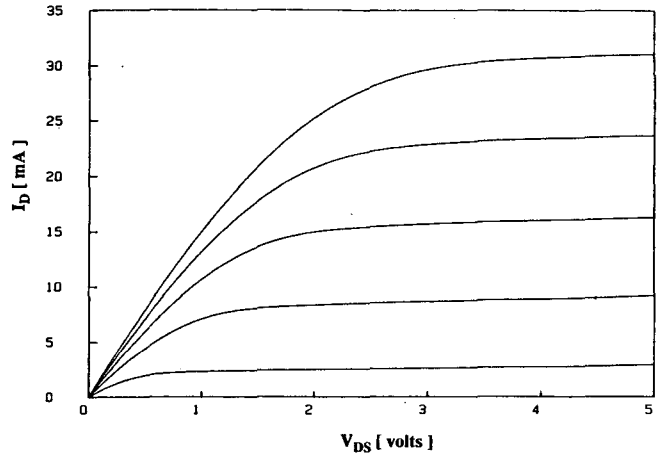
The most significant addition in the CMOS process with respect to the depletion-mode process is the NMOS device, and the design of this device will be discussed in some detail. The p well for the NMOS device is formed by a 400 keV ion implant of boron after the field oxidation step (actually doubly-ionized boron at 200 kV). This type of well is referred to as a retrograde well [6]. Because the well is formed after field oxidation, less redistribution of the implanted boron takes place during subsequent processing resulting in improvements in NMOS to PMOS device spacing, latchup susceptibility, and device isolation.

Figure 1 shows the output characteristics of NMOS devices with W/L of 100/3 and 100/2. The measurements were performed at a source to well voltage of 0V, and the substrate was biased at 25V as would be necessary for full depletion of a p-i-n radiation detector. The NMOS device is shielded from the relatively high substrate bias by the p-type well. For the 3 μm–length device, the saturation current at $V_{GS} = 5V$ is approximately 20 mA while the 2 μm device achieves a saturation current of approximately 30 mA. The 100/2 device has a transconductance at $V_{GS} = 5V$ of approximately 7 mA/V, or 70 ms/mm when normalized to the gate width. From measurements of threshold voltage versus source to well bias the body-effect coefficient γ for the NMOS device was determined to be 0.6 $\sqrt{V}$. The subthreshold slope was approximately 80 mV/decade for both.

For analog applications the product of output resistance and transconductance is of importance since this is the maximum voltage gain possible in a single-stage, common-source amplifier. Figure 2 shows the measured product of transconductance (g_m) and output resistance (r_o) for the 100/3 and 100/2 NMOS devices. Both devices maintain maximum gain at drain-to-source currents as low as 1 nA, and hence the devices have excellent punchthrough characteristics. The 100/3



a)



b)

Figure 1. Output characteristics of (a) 100/3 and (b) 100/2 NMOS devices. The substrate bias was 25V, and the source to well bias was 0V. The gate voltage was stepped from 0 to 5V in 1V increments.

device has a maximum $g_m r_o$ of approximately 1000 in the subthreshold region, while the 100/2 device $g_m r_o$ exceeds 100. The reduction in $g_m r_o$ for the 2 μm device results from the reduction in output resistance due to the shorter channel length. Figures 1 and 2 illustrate the excellent NMOS device performance realized with the retrograde well process.

As mentioned previously, the retrograde well process is also beneficial in terms of isolation for the NMOS device. We have measured the isolation characteristics of the retrograde well using test structures as described in [7] and [8]. A parasitic transistor is formed with the NMOS device n^+ junction as the source, the p-well under the field oxide as the channel, and the n-type substrate as the drain. This parasitic device limits the minimum spacing from the n^+ source/drain junction to the p-well edge and hence affects the packing density.

Since the well is implanted after field oxidation and at a relatively high energy, minimal thermal annealing (30 minutes at 1000C) is needed to drive the well to its desired depth in the silicon. After the well drive the anneal temperatures are lim-

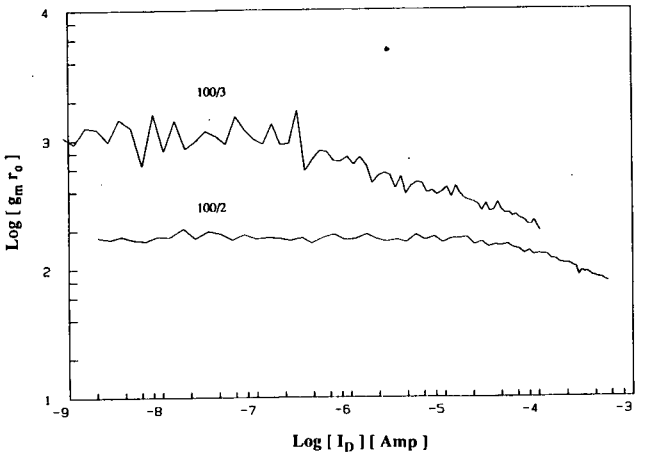


Figure 2. Measured product of transconductance (g_m) and output resistance (r_o) for 100/3 and 100/2 NMOS devices. Output resistance was measured at V_{DS} = 2V and the substrate bias was 25V.

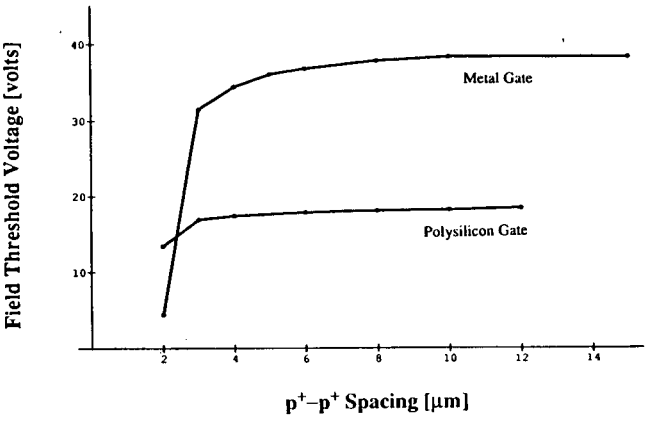


Figure 3. Field threshold voltage versus p^+–p^+ spacing. Field threshold is defined as the gate voltage at which the drain current is 1 nA/μm width of the parasitic field oxide transistor. V_{DS} = –5V and V_{sub} = 30V.

ited to 900C in order to maximize radiation hardness and minimize dopant redistribution. As a result a high doping concentration in the well under the field oxide (the parasitic field transistor channel) is maintained, thus resulting in the desired high field threshold voltage. The measured field threshold voltage at n^+ to p-well edge spacings down to 2 μm was 15V for a polysilicon gate device. Hence the retrograde well process results in excellent isolation for the NMOS device. In this work field threshold is defined as the gate voltage at which the drain current is 1 nA/μm width with a drain to source voltage of 5V.

Isolation characteristics of p^+–p^+ and p^+–p well parasitic devices were also measured and are shown in Figure 3. Device isolation for these parasitic devices is accomplished using the conventional local oxidation of silicon (LOCOS) process in conjunction with self-aligned field implants [7-8]. From Figure 3 it can be seen that a p^+–p^+ spacing of 3 μm is adequate for isolation at the 1 nA/μm width level. Additional measurements show that a 3 μm p^+–p well spacing is also adequate from a parasitic transistor point of view. However, this spacing will likely be determined by latchup considerations which is the subject of another investigation.

The above results are consistent with a conventional bulk CMOS process with minimum feature sizes of 2–3 μm in terms of transistor device characteristics and packing density (isolation characteristics). The main distinguishing feature of this process when compared to a conventional CMOS technology is the fact that the previous results are for a fully-depleted substrate. In the next section we describe the measured performance of circuits on a fully-depleted substrate with a minimum feature size of 3 μm.

3. Circuit performance

In order to assess the potential of this technology, simple circuits were fabricated and tested. Figure 4 shows the output voltage waveform for a 51-stage ring oscillator fabri-

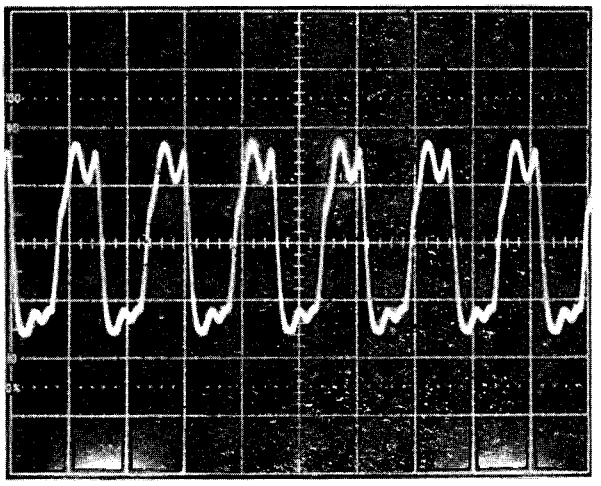


Figure 4. Output voltage waveform of a 51-stage ring oscillator. V_{DD} = 5V and V_{sub} = 25V. The W/L's were 3/3 and 6/3 for the NMOS and PMOS devices, respectively. 100 ns/div.

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cated in this technology. The device sizes are 6/3 and 3/3 for the PMOS and NMOS devices, respectively. The substrate bias was 25V and the ring oscillator power supply was 5V. The measured propagation delay is 1.5 ns per stage with a fanout of 1. The power dissipation is approximately 29 μwatts per stage yielding a power-delay product of 43 fJ. DC measurements on individual inverter stages yielded quiescent supply currents of less than 10 nA when the inverter input was at either 0V or 5V.

The simple cascode circuit shown in Figure 5 was used for analog measurements. External biasing including DC feedback was used to set the operating point of the amplifier. The DC feedback was filtered at the frequencies of interest to allow for the measurement of the amplifier open-loop properties. The NMOS input device size was 300/3, and the PMOS load was 100/20. Two types of amplifier were fabricated, the difference being the size of the cascode output devices M2

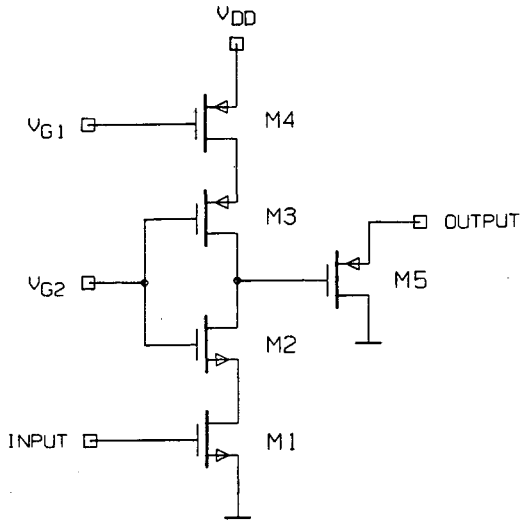

Figure 5. Schematic of the cascode amplifier considered in this work. The W/L's for M1, M4 and M5 were 300/3, 100/20, and 10/3 respectively. W/L for M2 and M3 was either both 25/3 or both 6/3.

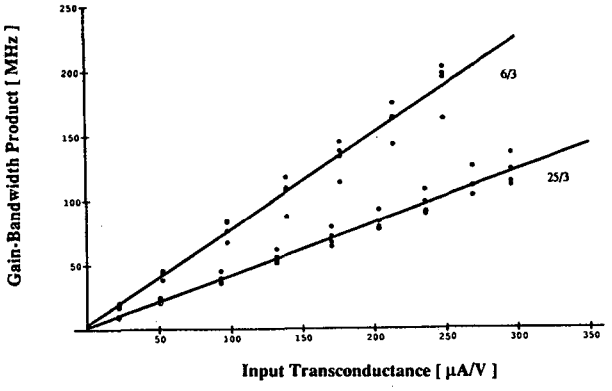

Figure 6. Gain-bandwidth product versus input transistor transconductance for the amplifiers whose schematic is shown in Figure 5. $V_{DD} = 5V$ and $V_{sub} = 25V$. The input bias current range varied from 1 to 15 μA for the amplifier with 6/3 output devices, and 1 to 20 μA for the amplifier with 25/3 output devices.

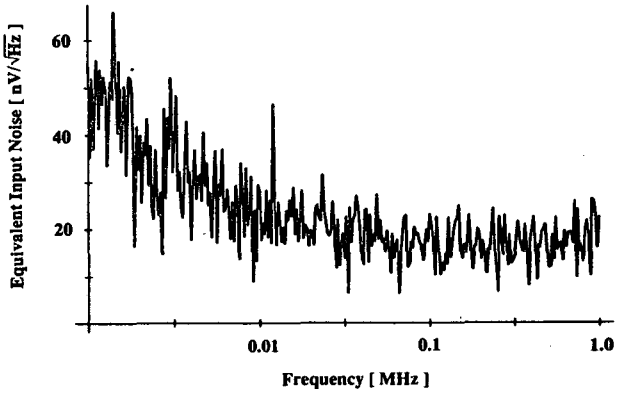

Figure 7. Input-referred noise for the cascode amplifier shown in Figure 5. The W/L for M2 and M3 was 6/3 and the bias current was 15 μA. $V_{DD} = 5V$ and $V_{sub} = 25V$.

and M3 which were 25/3 or 6/3.

Figure 6 shows the measured gain-bandwidth product for the two types of amplifiers versus the input device transconductance. The measurements shown in Figure 6 are open loop with no intentional frequency compensation. The gain-bandwidth product is defined here as the product of the low-frequency, open-loop gain and the frequency at which the gain has decreased by 3 dB. The bias currents ranged from 1–15 μA for the amplifiers with 6/3 output devices, and 1–20 μA for the amplifiers with 25/3 output devices. The typical open-loop voltage gain at the current levels corresponding to Figure 6 was 75 dB. As can be seen from Figure 6, gain-bandwidth products of approximately 200 MHz at a bias current of 15 μA are achieved with the amplifier containing 6/3 output devices. These values are considerably higher than that achieved with the depletion-mode PMOS technology [1].

Figure 7 shows the the input-referred noise at a bias current of 15 μA for the amplifier with 6/3 output devices. The input-referred noise at 1 MHz is on the order of 20 $nV/\sqrt{Hz}$. This value is larger than expected based on the input device transconductance and further investigation is required in order to determine the source of the discrepancy. Nonetheless, this value is only slightly worse than observed with the depletion-mode PMOS amplifiers which achieved a signal-to-noise ratio for minimum-ionizing particles of 30 to 1 at a 200 ns shaping time [1].

4. Summary

The results presented in the previous two sections illustrate the fact that radiation detectors and CMOS electronics can be fabricated on the same substrate using a conventional CMOS process. A key to this is the robust gettering which results from the backside phosphorus-doped polysilicon layer. The reverse leakage current for a fully-depleted detector in this 12-mask CMOS process is approximately 1 nA/cm^2 which is as good as that achieved in a simple, 3-mask detector process [5].

Analog and digital circuits at the 3 μm minimum feature size have been characterized, and their performance in terms of gain-bandwidth and power-delay product greatly exceeds that possible with the previous depletion-mode technology [1]. Device isolation is compatible with a 2–3 μm technology. In summary, the results are comparable to that expected from a foundary CMOS process and hence this technology can be used to realize radiation detectors monolithically integrated with high-performance analog and digital CMOS circuitry.

5. Acknowledgements

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