Stochastic thermodynamic bounds on logical circuit operation

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Using a thermodynamically consistent, mesoscopic model for modern complementary metal-oxide-semiconductor transistors, we study an array of logical circuits and explore how their function is constrained by recent thermodynamic uncertainty relations when operating near thermal energies. For a single NOT gate, we find operating direction-dependent dynamics and a trade-off between dissipated heat and operation time certainty. For a memory storage device, we find an exponential relationship between the memory retention time and energy required to sustain that memory state. For a clock, we find that the certainty in the cycle time is maximized at biasing voltages near thermal energy, as is the trade-off between this certainty and the heat dissipated per cycle. We identify a control mechanism that can increase the cycle time certainty without an offsetting increase in heat dissipation by working at a resonance condition for the clock. These results provide a framework for assessing the thermodynamic costs of realistic computing devices, allowing for circuits to be designed and controlled for thermodynamically optimal operation.

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I. INTRODUCTION

While semiconductor-based computational capacity [1,2] and efficiency [3–5] have exhibited sustained exponential growth over the past century, continued adherence to these trends is being disrupted as feature sizes approach atomic length scales and energetic scales near those of thermal noise [4–6]. At such small scales, computation has to reconcile with unavoidable noise [7,8]. This noisy limit has been termed *thermodynamic computing* [9,10] and requires the development of new principles to achieve robust and energy-efficient information processing [11–15]. In this paper, we explore fundamental limitations encountered when computing in this regime by showing how the function of realistic logical circuits is bounded by recent thermodynamic uncertainty relations [16,17].

Building upon equilibrium thermodynamics-based limits on computing operations, such as Landauer's limit on the cost of bit erasure [18], stochastic thermodynamics [19,20] provides a framework for exploring the inherent limits of logical circuit operations on small scales, far from equilibrium. Recent results like fluctuation theorems, thermodynamic uncertainty relations, and speed limits [21–30] can be used to strengthen bounds on computation within the thermodynamic computing regime, provided a physically consistent, stochastic model. Using a recently developed model for current complementary metal-oxide-semiconductor (CMOS) transistors [31], we study the interplay between accuracy, speed, and heat dissipation of an array of computations performed near thermal energies, locating optimal trade-offs between thermodynamic and operational costs.

This paper is organized as follows. In Sec. II, we describe the system discussed and the assumptions made. In Sec. III, we describe the behavior of a NOT gate and how the speed of its operation is weakly constrained by thermodynamics. In Sec. IV, we characterize a memory storage device and show it efficiently converted energy into memory preservation. In Sec. V, we extend the discussion to a clock, and in Sec. VI, we explore techniques for controlling it to enhance its accuracy without requiring excess energy consumption.

II. MODEL

Many conventional engineering approaches for characterizing the effects of noise on circuit operation rely on assumptions only valid near equilibrium or near specific operating conditions [32–35], guaranteeing neither thermodynamic consistency nor accuracy far from equilibrium [36]. To provide a more faithful description of stochastic circuits, we require models that obey local detailed balance and exhibit shot noise [37], while accurately reproducing known circuit characteristics. Recently, several stochastic models for CMOS devices have been proposed [31,38,39], enabling the study of noisy circuits and the associated thermodynamic costs when operating these devices near thermal energies [40–44]. Here, we employ one such model [31] to study systems of inverters, or logical NOT gates, built from single electron tunnel junctions operating within the classical limit [45] and using a capacitive charging model for the readout voltage. This model meets the three criteria emphasized above and in principle can be parameterized directly from microscopic calculations,

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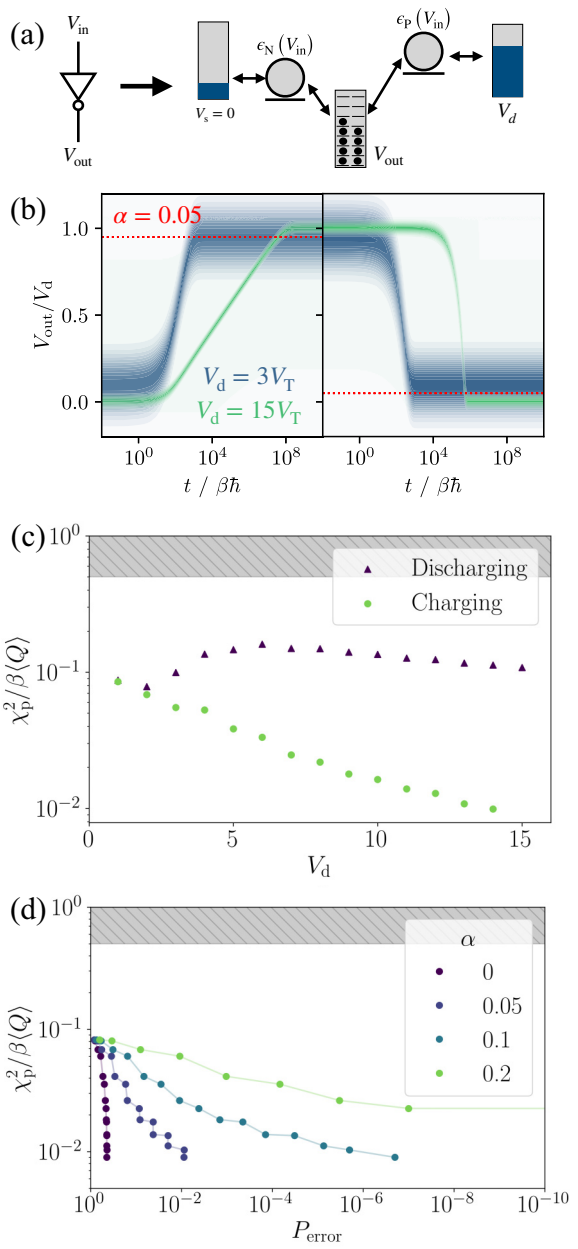

FIG. 1. Characterization of the NOT gate. (a) Illustration of the logical symbol and corresponding Markov model. (b) The probability of V_{out} with blue and green shading corresponding to different cross voltages. The left (right) panel illustrates the dynamics of charging (discharging) the inverter, with input voltages switched at $t = 0$. (c) Trade-off between first passage time certainty and heat dissipation for discharging and charging over a range of V_d with $\alpha = 0.05$, with the shaded region forbidden by the thermodynamic uncertainty relation. (d) The same trade-off as in (c) for the charging process shown as a function of the probability of a correct gate output in the steady state with varying accuracy thresholds $\alpha \in [0, 0.05, 0.1, 0.2]$.

providing a link between circuit performance and the underlying materials properties.

As shown in Fig. 1(a), each inverter contains an N-type and a P-type transistor, each modeled by the band energy of an electron in the transistor $\epsilon_N(V_{in})$ and $\epsilon_P(V_{in})$, respectively, with energy levels controlled by the inverter's input voltage V_{in}. This form of ϵ_i is valid in the limit of high gate capacitance. We set $\epsilon_P = qV_{in}$ and $\epsilon_N = \frac{3}{2}qV_d - qV_{in}$ to reproduce the characteristic voltage transfer curve of an inverter where q is the unit of charge [31]. The transistors are connected to three electron reservoirs: a source connected to the N-type transistor with reference voltage $V_s = 0$, a drain connected to the P-type transistor with voltage $V_d > 0$ resulting in a cross voltage, and an output gate connected to both transistors. While the source and drain are held fixed, the output gate voltage changes as electrons accumulate in the gate according to $dV_g/dt = -J_g(t)/C_g$, where J_g is the current of electrons into the gate and C_g is the gate capacitance. We use $C_g = 10q/V_T$ throughout, though we have verified nearly identical inverter performance at $C_g = 5q/V_T$ and $C_g = 15q/V_T$ [45].

The system evolves stochastically according to a Markovian master equation $\partial_t \mathbf{P}(t) = \mathbf{W}\mathbf{P}(t)$ where $\mathbf{P}$ is the configurational probability vector and $\mathbf{W}$ is the stochastic generator, with elements W_{ij} specifying the rate at which an electron transitions from state j to i and $P_i(t)$ being the probability of being in state i at time t. The ratio of forward and reverse rates satisfies local detailed balance, $W_{ij}/W_{ji} = e^{-\beta(E_i - E_j)}$, where E_i is the energy of a given configuration and $\beta = 1/k_B T$ is the inverse temperature defined with Boltzmann's constant k_B and temperature T. The rates are defined using the Fermi-Dirac distribution where the transition rate of an electron from an electrode j to a transistor i is $W_{ij} = \Gamma(e^{\beta(\epsilon_i - qV_j)} + 1)^{-1}$ and the reverse is $W_{ji} = \Gamma - \Gamma(e^{\beta(\epsilon_i - qV_j)} + 1)^{-1}$ where Γ specifies the timescale for transitions and is physically set by the resistance of the transistor-electrode interface. To ensure local detailed balance and to avoid the Brillouin paradox, we use the average of the gate voltage V_j before and after each transition [39,46].

We work in units of thermal voltages and times, $V_T = k_B T/q$ and $\beta\hbar$, respectively, and set $\Gamma^{-1} = 5\beta\hbar$ with $\hbar$ being Planck's constant. We set these constants to ensure the weak coupling limit, in which electron transitions can be treated as discrete hopping events [45]. For reference, at room temperature $V_T \approx 26$ mV and $\beta\hbar \approx 25$ fs. In these units, the model inverter is determined by a specification of the input voltage V_{in} and cross voltage V_d. While we first study the behavior of a single inverter, by supplying the output voltage of an inverter as the input voltage to another, more complex functionalities can be realized, such as the memory device and clock we subsequently consider.

III. NOT GATE

We start by considering the operation of a single inverter or NOT gate [Fig. 1(a)], which takes an input binary signal X and outputs its logical inverse Y according to the mapping

$$X = \begin{cases} 0, & V_{in} = 0 \\ 1, & V_{in} = V_d \end{cases}, \quad Y = \begin{cases} 0, & V_{out} \leqslant \alpha V_d \\ 1, & V_{out} \geqslant (1-\alpha)V_d \\ \emptyset, & \text{otherwise} \end{cases}. \quad (1)$$

In the deterministic limit, when the input is $X = 1$, current through the P-type transistor is inhibited, bringing the gate capacitor into effective contact with only the source reservoir with $Y = 0$. Conversely, when the input voltage is $X = 0$,

current is inhibited in the other transistor and the capacitor is connected to the drain reservoir, with $Y = 1$. All calculations performed for the single inverter are obtained using numerically exact time evolution, through a Padé approximation [47] with a truncated Hilbert space of $16C_g(V_d + 4)$, and verified using kinetic Monte Carlo simulations following the Gillespie algorithm [48]. For calculations where simulation times are not explicitly shown, we use time steps distributed logarithmically up to $10^{16}\beta\hbar$.

Figure 1(b) shows the time-dependent response of the inverter to an alternating input voltage, with the left and right panels corresponding to setting $X = 0$ and $X = 1$, respectively, at $t = 0$. Lower cross voltages V_d require less electron accumulation in the gate capacitor, and correspondingly fluctuations in the gate output are significantly larger for lower cross voltages. These small accumulations and large fluctuations lead to response times that are orders of magnitude faster at low cross voltages, highlighting a trade-off between output certainty and characteristic response time. While the steady-state statistics of the charged and discharged inverter are symmetric, we observe that the dynamics are not. As accentuated at larger V_d, the capacitor discharging happens rapidly, while charging occurs relatively slowly. This difference can be understood energetically. When discharging the capacitor, its occupation regulates the voltage in such a way that discharging becomes energetically more favorable as the gate empties. In the opposite direction, the accumulation of electrons becomes more energetically unfavorable as the gate charges, causing an exponential slowing of current into the gate as a function of time. Additionally, this leads to the circulation of electrons between the transistors and capacitor when charging, while electrons move directly from the capacitor out of the inverter when discharging. The functionally unnecessary transitions caused by this circulation cause slower operation times during the loading process.

To understand more precisely the interplay between the thermodynamic and operational costs for the inverter, we can employ a thermodynamic uncertainty relation [49]

$$\chi_p^2 = \frac{\langle \tau_p \rangle^2}{\langle \delta \tau_p^2 \rangle} \leqslant \frac{\langle Q \rangle}{2qV_T} + 1, \tag{2}$$

where brackets indicate a trajectory ensemble average, τ_p is the first passage time to an output voltage passing the accuracy threshold α, $\delta x = (x - \langle x \rangle)$, and Q is the the heat dissipated over a trajectory. Explicitly, τ_p is calculated from an initial state $X = 0$ (or $X = 1$), and the final absorbing boundary condition corresponds to the opposite output $Y = 1$ (or $Y = 0$) [50]. For a specific trajectory, the heat is given as

$$Q = \sum_{k=1}^{N} \ln \frac{W_{x_k x_{k-1}}}{W_{x_{k-1} x_k}}, \tag{3}$$

where the sum is over steps in the trajectory, and x_k is the state of the system at step k [51].

The thermodynamic uncertainty relation is a general result of stochastic thermodynamics, valid for any Markovian jump process. It states that the certainty in the first passage time, χ_p, is bounded from above by the heat dissipated over a trajectory, Q [52]. The bound relates the minimum thermodynamic cost for a given desired certainty in the first passage time. While the bound was originally formulated for a system in steady state, here we apply a finite-time version [49].

In practical terms, higher certainty in operation time allows for processing input bits at higher rates. For some acceptable probability of error, lower first passage time certainty χ_p requires waiting longer to be sure each operation has successfully completed. Conversely, higher first passage time certainty does not require such waiting time, which results in lower heat dissipation due to the shorter overall operation time.

Figure 1(c) shows how this bound depends on the cross voltage V_d for the accuracy threshold $\alpha = 0.05$. We observe that the bound is not saturated across all V_d and for both charging and discharging, which implies that the operation of the NOT gate may not be limited by thermodynamic constraints, but rather by its design. Theoretically, it should be possible to design a NOT gate that results in lower heat dissipation for the same level of first passage time certainty, possibly using a different architecture.

In Fig. 1(d), we vary the cross voltage and plot the trade-off between first passage time certainty and heat dissipation, as a function of the probability of an error in the output at long times $P_{error} = 1 - \langle Y \rangle_{X=0}$, where the ensemble average is over trajectories with the specified input. We additionally show multiple curves corresponding to differing values of the signal accuracy threshold α and observe that loosening α moves the curves significantly toward the bound by dissipating less heat. This trend suggests thermodynamically optimal operation at higher probabilities of correct outputs as α increases, with similar but less pronounced effects not shown for the discharging process.

IV. MEMORY DEVICE

Next, we consider a static random access memory (SRAM) device built by coupling two inverters, as shown in the inset of Fig. 2(a). This device operates using so-called flip-flop circuitry, meaning it exhibits a bistable steady state, which is a dynamical consequence of a pitchfork bifurcation. The inverter's state can be set by switching on V_{set}^1, employing feedback from V_{out}^1 to V_{in}^2. Here, we will focus on memory maintenance, which can be reliably achieved at sufficiently large cross voltages by switching both setting voltages off and both feedback loops on. To simulate the memory device, we perform an approximate evolution using a fourth-order Runge-Kutta scheme acting on a truncated Hilbert space using a time step of $\Delta t = \beta\hbar/10$ until a final time of $t_f \approx 10^6\beta\hbar$. We additionally evaluate the dynamics using kinetic Monte Carlo simulations.

Figure 2(a) shows the steady-state probability of observing an output voltage $V_{out} = V_I^{out}$. The requisite bistability for memory storage arises at $V_d/V_T \approx 2.5$ where the cross voltage overcomes the effects of thermal fluctuations. Notably, the bistability is a unique consequence of the nonequilibrium driving, which disappears in the absence of a finite cross voltage. At finite V_d, the degeneracy of the steady state manifests as a spontaneous switching of V_{out} as a function of time, illustrated in Fig. 2(a). For large V_d we observe V_{out}/V_d is localized near 0 or 1 for time scales much larger than individual inverter operation time scales $\langle \tau_p \rangle$, indicating persistent

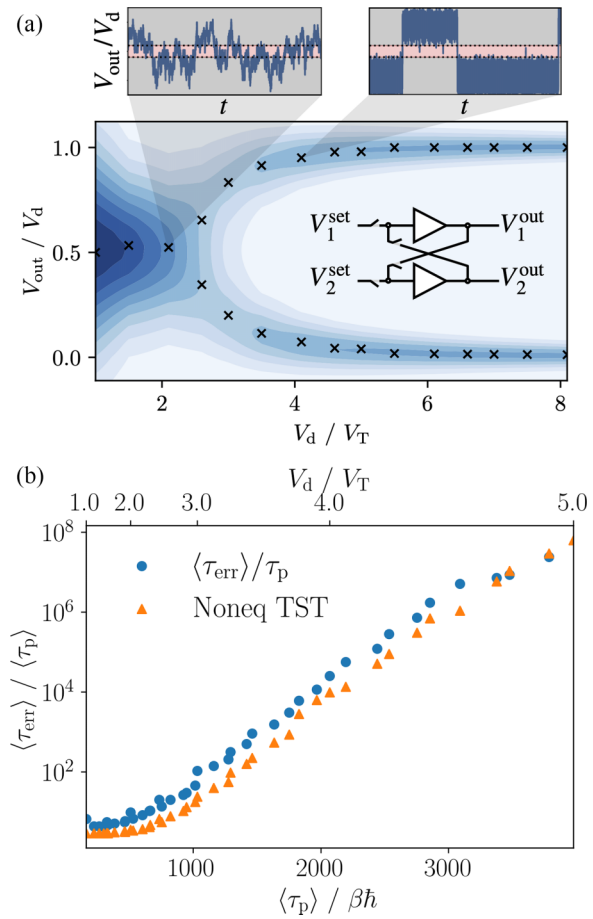

FIG. 2. Characterization of the memory device's behavior and adherence to thermodynamic speed limits. (a) Probability of V_{out} as a function of V_d, with crosses locating points of maximum probability at each V_d illustrating the onset of bistability. Example trajectories are shown for before and after the onset of bistability. (b) Mean time for a memory error as a function of the inverter relaxation time, controlled by increasing V_d, as indicated on the top x-axis label.

memory storage. At long times, however, the output voltage is stochastically inverted, corrupting the memory storage.

We define τ_{err} as the time required for a memory device, initialized in one of the bistable states, to experience a bit flip memory error. Figure 2(b) shows the average time required for a bit flip to occur $\langle\tau_{err}\rangle$ [53] as a function of the characteristic time of a single inverter. We observe that the rate of memory error occurrences decreases exponentially with respect to $\langle\tau_p\rangle$, thus increasing the average memory stability time by roughly five orders of magnitude, from about 100 ns to 20 ms for $V_d/V_T = 2$ to 5.

The efficiency of this memory device can be quantified using a nonequilibrium version of the transition state theory [26,54,55]. Transition state theory bounds the rate of a transition between two metastable states using the stationary distribution $P_{ss}(V_{out})$ and an uncorrelated estimate of the time to cross a dividing surface between the two states. Equivalent to Kramers' theory, the rate is estimated by the probability of a rare fluctuation, in this case, a fluctuation of the output voltage of one of the NOT gates of the memory storage device being equal to $V_d/2$. Taking the dividing surface to be $V_{out} = V_d/2$, and the typical time to relax from the top of the barrier as $\langle\tau_p\rangle$, a nonequilibrium transition state theory estimate for $\langle\tau_{err}\rangle$ is

$$\langle\tau_{err}\rangle \gtrsim \langle\tau_p\rangle \frac{P_{ss}(V_{out}/V_d \leqslant \alpha)}{P_{ss}(V_{out}/V_d = 1/2)}, \tag{4}$$

which is shown in Fig. 2(b). Here, the steady state has been evaluated numerically with $\alpha = 0.4$, but because the time scale for crossing the barrier is significantly larger than relaxation times within each well, the results are similar for $\alpha \in [0, 1/2]$. The nonequilibrium transition state theory provides a very accurate estimate of the memory time, reflecting the likelihood of observing a fluctuation of $V_{out} = 1/2$ as becoming exponentially unlikely with increasing V_d in accord with recent large deviation function analysis [40]. Since the transition state theory estimate corroborates the rate of transition between the two bistable states for the potential energy landscape at a given V_d, we conclude that the energy pumped into the SRAM device is efficiently directed into preserving the memory state, rather than spent on extraneous fluctuations which would result in more frequent bit flip errors.

V. CLOCK

An uneven number of inverters coupled sequentially in a ring creates a system with a frustrated steady state, because all inverters cannot simultaneously output the logical inverses of their inputs. This frustration causes cyclic oscillations, whose period is controlled by inverter operation times, making the device operate as a clock under deterministic conditions and providing an example of circuitry with nontrivial functionality. To simulate the dynamics of such a clock, we perform kinetic Monte Carlo simulations. We define the time for the clock to undergo a single cycle τ_c as the time for the output, Y, to cycle from $1-\alpha$ to α and back again to $1-\alpha$, using $\alpha = 0.4$. Example trajectories are shown in Fig. 3(a). All results are averaged over simulations containing at least 50000 clock cycles.

In Fig. 3(b), we show the output voltage autocorrelation function $C_{V_i,V_i}(t) = \langle\delta V_i(0)\delta V_i(t)\rangle$, as a function of time and cross voltage. At low cross voltages, the three output voltages evolve nearly independently, with $C_{V_i,V_i}(t)$ revealing exponential correlations. Above $V_d \approx 3V_T$ persistent oscillations emerge but are damped by the stochasticity of the evolution. We find a maximal persistence in the autocorrelation function oscillation at $V_d \approx 7V_T$, where the clock undergoes approximately 3.5 cycles. In this region, oscillations are persistent for long times and the fluctuations in τ_c are small relative to the mean cycle time. Above $V_d \approx 10V_T$, the autocorrelation exhibits oscillation for only half of a cycle because, while oscillations are persistent for long times, the fluctuations in τ_c are large relative to the mean cycle time as anticipated from Fig. 1(c) and the single NOT gate. In this regime, we find the cycle time to be inversely proportional to voltage output amplitude, which evolves stochastically.

We define the certainty in the cycle time as $\chi_c = \sqrt{\langle\tau_c\rangle^2/\langle\delta\tau_c^2\rangle}$, and plot this for $V_d \in [1V_T, 20V_T]$ in Fig. 3(c). The red dashed line indicates where the cycle time's fluctuations are equal to its mean, above which we find a narrow range of cross voltages where there is reliable cycling. The first passage time thermodynamic uncertainty relation

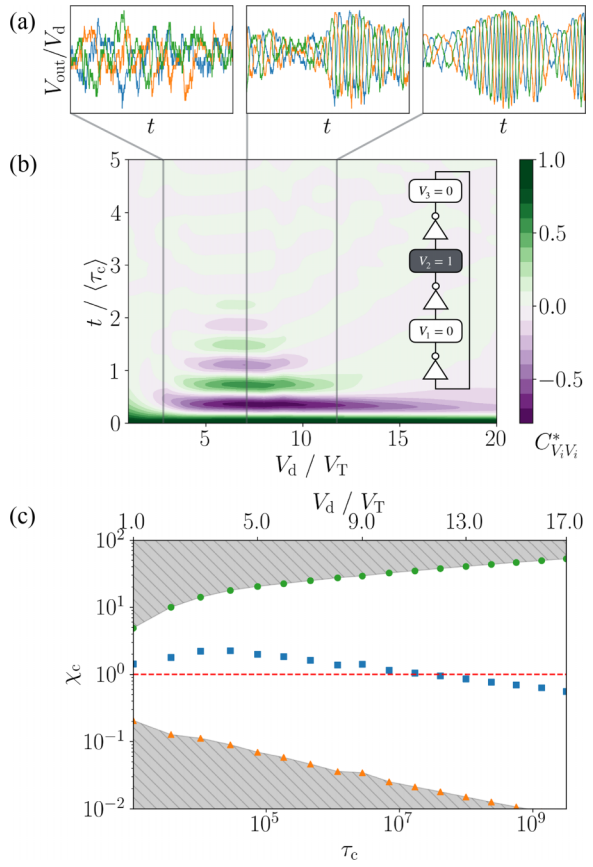

FIG. 3. Adherence to thermodynamic bounds of the logical clock. (a) Example trajectories at $V_d = [2V_T, 7V_T, 12V_T]$, with each curve representing how the output voltage of one of the inverters evolves. (b) Rescaled voltage autocorrelation function $C^*_{V_i,V_i}(t) = C_{V_i,V_i}(t)/C_{V_i,V_i}(0)$ as a function of applied cross voltage. (c) The certainty in clock operation time χ_c (blue squares) as a function of average clock cycle time $\langle\tau_c\rangle$ (bottom axis) and applied cross voltage (top axis), with the shaded regions indicating the forbidden regions from the uncertainty relations. The red dashed line indicates where $\langle\tau_c\rangle^2 = \langle\delta\tau_c^2\rangle$.

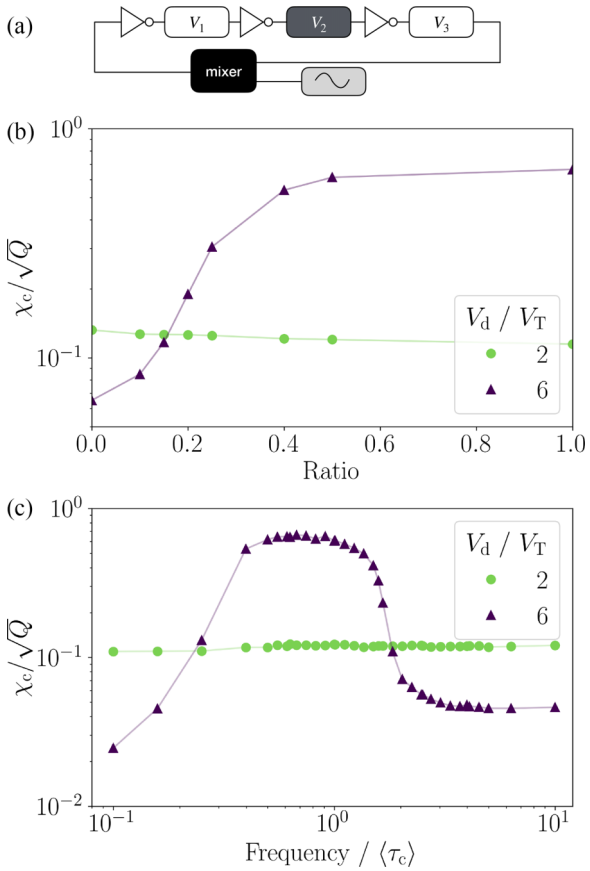

FIG. 4. Improvement in reliability of the logical clock cycle time with external control. (a) Control mechanism, where the input signal is mixed between the output of the rightmost NOT gate V_3 and the external sinusoidal controller. (b) Certainty in clock operation time χ_c as a function of mixing ratio of signal from V_3 or the external controller. (c) Certainty in clock operation time χ_c as a function of the frequency of the external controller.

expressed in Eq. (2) can be applied to give an upper bound on this quantity

$$\chi_c^2 = \frac{\langle\tau_c\rangle^2}{\langle\delta\tau_c^2\rangle} \leqslant \frac{\langle Q\rangle}{2qV_T}, \tag{5}$$

where $\langle Q\rangle$ is the average heat dissipated over a cycle. As in the single NOT gate, τ_c measures the time to reach a specific state of the gate capacitor.

Similarly, the dissipation-time uncertainty relation [24] relates the rate of heat dissipation with the mean time to complete a process. It can be applied to the clock cycle time to yield a lower bound,

$$\begin{aligned} \langle\tau_c\rangle &\geqslant (\beta\langle\dot{Q}\rangle)^{-1} \\ \chi_c^2 &\geqslant \frac{\langle\tau_c\rangle}{\beta\langle\dot{Q}\rangle\langle\delta\tau_c^2\rangle}, \end{aligned} \tag{6}$$

where $\langle\dot{Q}\rangle$ is the average rate of heat dissipation in the steady state.

Figure 3(c) exhibits the upper (green circles) and lower bounds (orange triangles) as shaded regions. The upper bound is best saturated when χ_c is maximized around $V_d \approx 3V_T$. This occurs for a large enough cross voltage that the coupled inverters exhibit bistability, but not so large that the fluctuations in the time to charge or discharge each gate are larger than the overall cycle time, preventing reliable cycle behavior.

VI. CLOCK CONTROL

To expand the range of reliable cycle times, we propose a simple control mechanism acting on the three-gate circuit. In Fig. 4(a), we show a schematic diagram: we insert a sinusoidal oscillator yielding a voltage

$$V_{ext} = \frac{V_d}{2}\sin\left(\frac{2\pi f}{\tau_c}t\right) + \frac{V_d}{2}, \tag{7}$$

whose frequency f we can control with respect to the clock cycle time τ_c. The signal into the leftmost inverter in the circuit is then given by a linear combination of the output of

the rightmost inverter V_3 and the external sinusoidal oscillator

$$V_{\text{in}} = rV_{\text{ext}} + (1 - r)V_3, \tag{8}$$

where $r \in [0, 1]$ denotes the mixing ratio. Here, $r = 0$ denotes an undriven system with $V_{\text{in}} = V_3$, and $r = 1$ denotes a fully driven system with signal completely from the sinusoidal oscillator, $V_{\text{in}} = V_{\text{ext}}$.

Although this controlled system does not satisfy a TUR because it is not time homogeneous, we can still use the cycle time precision χ_c defined previously as a metric for the efficiency of the clock. We find that this simple control mechanism can improve the reliability of the clock cycling in Fig. 4(b). At low driving voltage ($V_d = 2V_T$, green circles), the fluctuations in the signal are large enough that external control has little effect. With sufficiently high driving ($V_d = 6V_T$, purple triangles), however, we see that precision improves with increasing contribution from the oscillator from left to right. All data in this figure were generated with oscillator frequency equal to $1/\langle\tau_c\rangle$.

In Fig. 4(c), we vary the frequency of the oscillator relative to the average cycle time $\langle\tau_c\rangle$ of the uncontrolled circuit for a fixed ratio of $r = 0.5$. As before, the external controller has no effect at low driving voltage V_d. At higher driving, the clock precision is maximized when the oscillator frequency is slightly lower than $1/\langle\tau_c\rangle$, which we attribute to the oscillator acting roughly on resonance with the natural frequency of the circuit. The distribution of τ_c is asymmetric, so its average $\langle\tau_c\rangle$ is slightly higher than the peak of the distribution. Above and below the natural frequency $1/\langle\tau_c\rangle$, the external oscillations act functionally as noise, to which the system responds unfavorably.

VII. CONCLUSION

We have used a Markovian model for realistic logical inverters in the regime of thermodynamic computing to explore the interplay between operating characteristics, like accuracy and time, and thermodynamic properties, particularly heat dissipation. Our results demonstrate the theoretical limits of CMOS circuits using bounds derived from stochastic thermodynamics. As we have shown, this provides a framework for simultaneously exploring the fundamental behavior of noisy computational circuits, characterizing their optimality, and using the gained insight to propose more efficient operating procedures and circuits. We expect this work will provide a foundation for future work toward understanding and designing efficient thermodynamic computers. Current techniques should allow for the improvement of thermodynamic efficiencies by adapting principles from optimal control theory to operational control schemes [56–63] and by exploring the effects of circuit layout [14]. To extend this approach to larger circuits, more scalable simulation techniques, such as tensor network methods [64–68], can be adapted.

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DATA AVAILABILITY

The source code for the calculations done and all data presented in this work are openly available on Zenodo [69].

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