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Keywords

≪Converter circuit≫, ≪DC power supply≫, ≪Efficiency≫, ≪High power density systems≫

Abstract

Resonant switched-capacitor (SC) converters are becoming increasingly attractive for high performance applications due to their efficient utilization of switches and use of high energy density capacitors. Multi-phase SC converters can offer further improvements in performance, as they can achieve the same conversion ratio as traditional two-phase SC converters with fewer capacitors and switches, making them ideal for large conversion ratio applications. This paper presents theoretical analysis and experimental results for a resonant multi-phase SC converter comprising a cascaded series-parallel topology derived from the conventional 4-to-1 series-parallel converter. The proposed converter can achieve a 6-to-1 conversion ratio with the same number of switches and capacitors as the 4-to-1 series-parallel converter. A 48-to-8 V prototype designed for data center applications was built and tested with 40 A maximum output current. The prototype achieved 99.0% peak efficiency (98.5% including gate drive loss) and 2230 W/in^3 power density, demonstrating one of the best in-class performances.

Introduction

The power demands of data centers have grown rapidly due to the development of cloud computing, high-performance computing, and big data analysis. In 2014, data centers used more than 1.8% of all electricity in the US, and it is projected that they will use 10% by 2020 [1]. Therefore, much work has been done to increase the efficiency and reduce the physical footprint of data center power delivery networks. One of these efforts is to distribute power to servers at a higher voltage (e.g. 48 V) compared to the traditional 12 V bus to reduce resistive losses. One approach for converting the 48 V bus to a voltage that the server equipment can use is through a two-stage architecture. Here, the first stage converts the 48 V to an intermediate voltage (e.g. 5-12 V) and the second stage converts the intermediate voltage to the point-of-load (PoL) voltage. The intermediate bus voltage converter can be unregulated, as the second-stage buck converter can provide regulation. Recent research has indicated that using an

intermediate bus voltage lower than 12 V can result in better overall system efficiency once the efficiency of the second-stage buck is considered as well [2].

Due to their high efficiency and high power density, resonant switched-capacitor converters (ReSC) have received increased attention for use in data center applications. Resonant switched-capacitor circuits not only demonstrate an efficient utilization of switches [3] and the use of high energy density capacitors [4], but also allow for soft-switching and soft-charging operations [5–8]. Recent hardware demonstrations of ReSC converters have demonstrated excellent efficiency and power density, in applications ranging from high power discrete implementations [9–15] to CMOS integrated solutions [16, 17].

This work proposes and explores the performance of a new multi-resonant cascaded series-parallel 6-to-1 topology that can achieve very high efficiency and power density. Multi-phase switched-capacitor converters are especially attractive for data center applications, as they can achieve the same conversion ratio as traditional two-phase switched-capacitor circuits with fewer capacitors and switches, further improving efficiency and power density.

A 48-to-8 V, 40 A, fixed ratio (unregulated) converter prototype was designed and implemented. The prototype achieved 99.0% peak efficiency (98.5% with gate drive loss) and 2230 W/in^3 power density, both of which are among the highest of existing work.

Multi-Resonant Cascaded Series-Parallel Converter

Proposed topology and operating principle

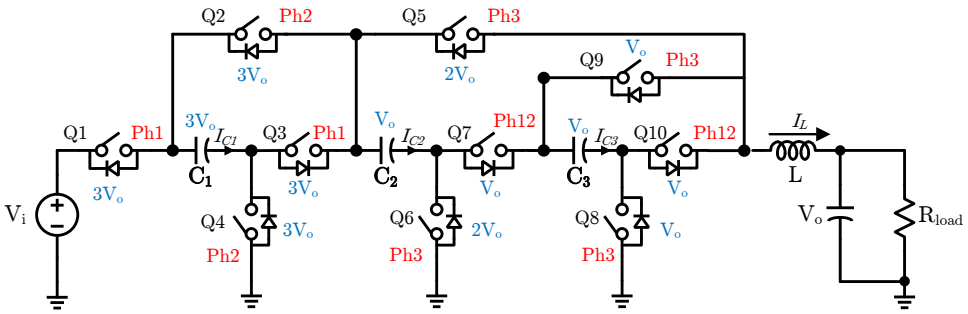

Fig. 1: Schematic of the proposed 6-to-1 cascaded series-parallel converter with device ratings labeled.

Fig. 1 shows the schematic for the proposed 6-to-1 cascaded series-parallel converter, with the output given by $V_{out} = \frac{V_{in}}{6}$. This circuit topology can be derived from the classic 4-to-1 series-parallel topology, by moving the source terminal of Q_2 in Fig. 1 from the left-side of the inductor to the positive-side of C_2 and adding an additional operating phase. The converter achieves a 2-to-1 step-down during the first $\frac{1}{3}$ of the switching period through a series-mode operation, followed by a 3-to-1 parallel-mode operation during the last $\frac{2}{3}$ of the switching period. This converter therefore can achieve a 6-to-1 conversion ratio for the same number of switches and capacitors as the 4-to-1 converter, although the device ratings on one switch and one capacitor are increased from V_o for the 4-to-1 converter to $3V_o$ for the 6-to-1 converter.

The current waveforms in the inductor and flying capacitors C_1-C_3, gating signals (matching switch labels in Fig. 1), and equivalent circuits for each phase are shown in Fig. 2. During the time 0 to $\frac{T}{3}$ (*Phase* 1 and *Phase* 2), the resonant frequency is determined by the series combination of C_1, C_2, C_3, and the inductor, L. Then, $f_{res,1} = f_{res,2} = \frac{1}{2\pi\sqrt{LC_{eq}}}$, where $\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$.

During the time $\frac{T}{3}$ to T (*Phase* 3), the resonant frequency is determined by the parallel combination of C_2 and C_3, so that $f_{res,3} = \frac{1}{2\pi\sqrt{L(C_2||C_3)}}$.

The time duration of each phase can then be derived from its respective resonant frequency. The duration of *Phase* 1 and *Phase* 2 can be written as:

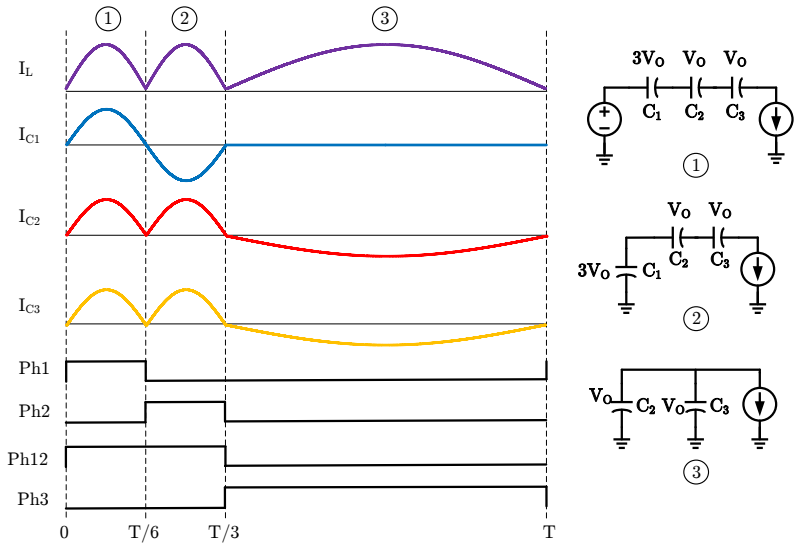

Fig. 2: Key current waveforms and control signals for the proposed converter. The converter state for each of the three phases is also shown.

$$T_1 = T_2 = \frac{T}{6} = \frac{1}{2} \cdot 2\pi \sqrt{L\left(\frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}}\right)} \tag{1}$$

where T is the switching period. T_1 has a factor of π rather than 2π at it represents a half cycle of the full resonant period.

The duration of *Phase* 3 can similarly be written:

$$T_3 = \frac{2T}{3} = \frac{1}{2} \cdot 2\pi \sqrt{L(C_2 + C_3)} \tag{2}$$

Due to the parallel operation mode, it is necessary that $C_2 = C_3 = C$. Substituting this into (1) and (2) and solving for $4 \cdot T_1 = T_3$ (as the duration of *Phase* 3 is $4\times$ that of *Phase* 1 or *Phase* 2), the minimum C_1 to achieve soft charging can be found to be $C_{1,\text{min}} = \frac{1}{6}C$. As can be seen from Fig. 1, C_1 sees $3V_o$ while C_2 and C_3 only see V_o, so the highest voltage rated capacitor is also the lowest valued capacitor. This can allow C_1 to take up a similar volume to C_2 and C_3 despite its higher voltage rating.

If operated at resonance, the converter can achieve zero-current switching (ZCS) as the current reaches zero at the switch transitions. The resonant frequency represents the minimum frequency to achieve soft-charging [7]. Here, the hardware prototype is operated above resonance to account for component non-idealities and reduce the output impedance and conduction loss. This also allows for the use of Class 2 ceramic capacitors, as the flying capacitors do not have to be precisely tuned to an exact ratio. In this operation mode, the converter can also achieve partial zero-voltage switching (ZVS) at switch turn-on.

Table I compares the component count and voltage ratings for several different switched-capacitor topologies that can be augmented with resonant inductor(s) and operated in a resonant mode. The proposed topology has the lowest number of components of all the 6-to-1 converters in Table I, and the same number of components as the lower conversion-ratio 5-to-1 Fibonacci converter. This is of note as the 5-to-1 Fibonacci converter demonstrates the maximum gain possible in a two-phase switched-capacitor converter, with 10 switches and 3 flying capacitors [18] [19]. The proposed topology also requires lower voltage capacitors compared to the FCML and Switched Tank (Dickson) converters.

Table I: Comparison of number and voltage rating of components for several resonant switched-capacitor converters

Topology	Conversion Ratio	Number of Switches	Switch Rating	Number of C_{fly}	C_{fly} Rating	Number of Inductors
Proposed Topology	6-to-1	10	$4\times3V_o$ $2\times2V_o$ $4\times V_o$	3	$1\times3V_o$ $2\times V_o$	1
Series-Parallel	6-to-1	16	$3\times5V_o$ $2\times4V_o$ $2\times3V_o$ $2\times2V_o$ $7\times V_o$	5	$5\times V_o$	1
Switched Tank (Dickson)	6-to-1	16	$2\times2V_o$ $14\times V_o$	5	$1\times5V_o$ $1\times4V_o$ $1\times3V_o$ $1\times2V_o$ $1\times V_o$	3
FCML	6-to-1	12	$12\times V_o$	5	$1\times 5V_o$ $1\times 4V_o$ $1\times 3V_o$ $1\times 2V_o$ $1\times 1V_o$	1
Fibonacci	5-to-1	10	$2\times3V_o$ $4\times2V_o$ $4\times V_o$	3	$1\times3V_o$ $1\times2V_o$ $1\times V_o$	1

Two useful metrics for comparing topologies are the switch stress (VA_{RMS}) rating and the total passive component volume. The switch stress relates to how much voltage the switches must block and how much current they must conduct, and is a good indication of the efficiency of the topology. The passive component volume is proportional to the amount of reactive energy that needs to be processed and stored in the converter, and reflects the power density of the topology. Fig. 3 plots the passive volume vs. the switch stress rating, using the method outlined in [20] assuming $\frac{\rho_C}{\rho_L} = 100$, where ρ_C is the energy density of the capacitor(s) and ρ_L is the energy density of the inductor(s). The switch stress and passive volume are normalized to the theoretical lowest possible value to allow for a comparison across topologies. In this plot, the ideal converter would be situated near the origin, and exhibit both low passive volume and low switch stress. The buck converter operating at a conversion ratio of 6-to-1 is also plotted to provide a benchmark for comparison with the presented hybrid converters.

Looking at Table I and Fig. 3, it can be seen that the proposed converter has much lower passive volume and therefore potentially higher power density compared to the Switched Tank (Dickson) converter, though it has higher switch stress. The proposed work has lower switch stress compared to the series-parallel topology, while its passive volume is only slightly higher. This is of note as the passive volume of the series-parallel topology is known to be at the theoretical lower limit [20]. This means that the proposed topology can achieve similar theoretical performance to the series-parallel converter even with a greatly reduced number of capacitors and switches (and their associated gate drive circuitry). Furthermore, as devices might not be able to be sized exactly to the theoretical VA rating due to limited availability of different voltage ratings, in a physical implementation topologies with different theoretical VA ratings may end up using the same device. This practical concern is most apparent in low-voltage Silicon power transistors, where discrete transistor products below 25 V are not readily available. In applications such as 48 V conversion, the series-parallel converter is very attractive despite its high theoretical switch stress, due to both the limited available switch voltage ratings in this application space as

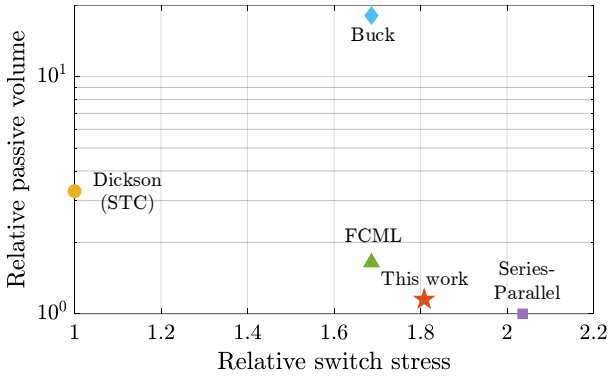

Fig. 3: Relative passive volume vs. normalized switch stress for several 6-to-1 converters.

well as the low output impedance exhibited by the converter due to its many parallel current paths [10]. The proposed topology operates in a similar manner to the series-parallel topology, and has the potential to exhibit very high performance in this application space compared to Dickson-based topologies due to its low passive volume and low number of components, as the disadvantage of switch utilization is relatively mild considering the actual switches available.

Hardware Implementation and Experimental Results

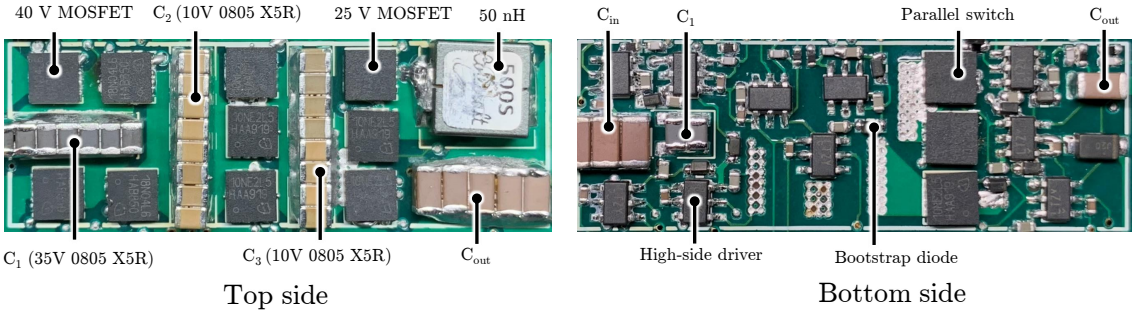

Fig. 4: Photograph of the converter. Dimensions: 1.38 × 0.46 × 0.22 inch (3.5 × 1.17 × 0.56 cm).

Table II: Components for Prototype Converters

Component	Description	Device	Value
Q1-Q4	40 V Si switches	Infineon BSZ018N04LS6	40 V, 40 A, 1.8 mΩ
Q5-Q10	25 V Si switches	Infineon BSZ010NE2LS5	25 V, 40 A, 1.0 mΩ
L	Resonant inductor	Coilcraft SLC7530S-500MLB	50 nH, 50 A I_{sat}, 0.123 mΩ
C1	Flying Capacitors	TDK C2012X5R1V226M125AC	16 × 22 μF* 35 V X5R 0805
C2	Flying Capacitors	Murata GRM21BR61A476ME15L	16 × 47 μF* 10 V X5R 0805
C3	Flying Capacitors	Murata GRM21BR61A476ME15L	16 × 47 μF* 10 V X5R 0805
	Gate driver	Analog Devices LTC4440-5	80 V, 1.1 A peak output current
	Bootstrap diode	ON Seminconductor NSR0340V2T1G	40V, 250 mA, Schottky
	Controller	TI TMS320F28069	

* The capacitance listed here is the nominal value before dc derating.

Fig. 4 shows an annotated photograph of the hardware prototype, with key components labeled. The PCB stack-up consists of 4 layers, with 4 oz copper on the outer layers (where the critical conduction path is) and 3 oz copper on the inner layers. As the maximum theoretical voltage a switch can see in this topology is $3V_o$, relatively low-voltage switches can be used (40 V and 25 V). Silicon devices are used for

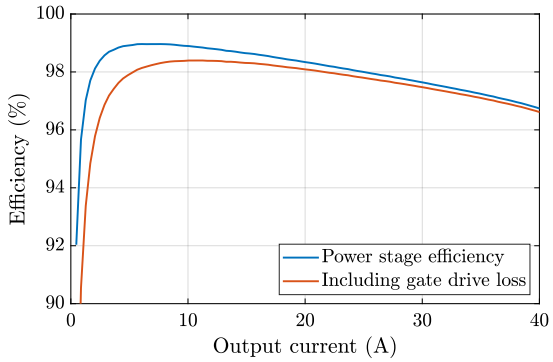

Fig. 5: Measured efficiency 40 to 6.7 V, f_{sw} = 65 kHz.

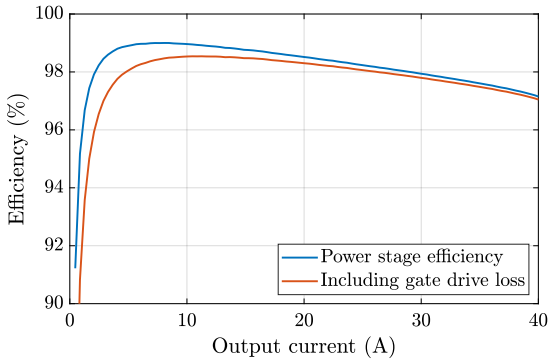

Fig. 6: Measured efficiency 48 to 8 V, f_{sw} = 68 kHz.

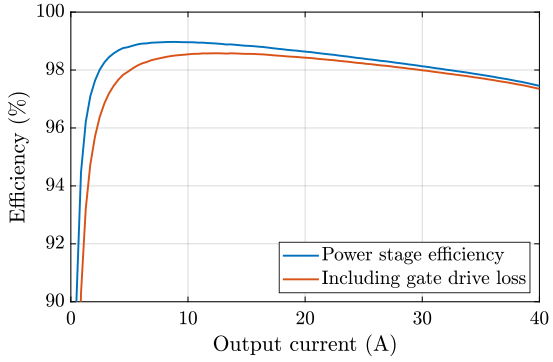

Fig. 7: Measured efficiency 54 to 9 V, f_{sw} = 75 kHz.

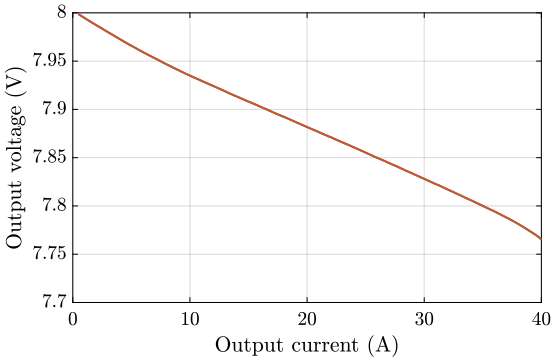

Fig. 8: Load regulation V_{in} = 48 V, V_{out} = 8 V.

this prototype, as at these low voltages the performance of Si can match that of GaN. The high-current path devices ($Q_8 - Q_{10}$) are paralleled to reduce conduction losses. Each floating switch is driven by a floating high-side gate driver powered using the cascaded bootstrap method [21], from a 9 V source. The total gate drive current was measured with a Yokogawa WT310 digital power meter, while the power stage voltage, current, and efficiency was measured with a Yokogawa WT3000E precision power meter for the most accurate results at the high efficiencies obtained. Table II lists the components used in the prototype.

Table III lists the operating conditions. The gate drive signals were programmed with a constant deadtime of 44 ns. The converter was tested up to 40 A output current, and achieved a peak efficiency of 99.0% and a full-load efficiency of 97.1% (98.5% and 97.0% with gate drive loss included, respectively) for a 48-to-8 V step-down conversion operating at 68 kHz. The power density at full-load was 2230 Win^3 with a box volume of 0.139 in^3 (2.29 cm^3). Efficiency curves for 48-to-8 V operation from 0 A to 40 A are given in Fig. 6. Efficiency curves were also taken for additional voltage levels within the expected

Table III: Converter Operating Conditions

Parameter	Value
Input Voltage	48 V (40 - 54 V)
Output Voltage	8 V (6.7 - 9 V)
Output Current	40 A
Power (Measured)	310 W (260 - 350 W)
Switching Frequency	68 kHz (65 - 75 kHz)
Dimensions	1.38 inch × 0.46 inch × 0.22 inch (3.5 cm × 1.17 cm × 0.56 cm)
Box Volume	0.139 in^3 (2.29 cm^3)

Table IV: Measured Converter Performance

Metric	V_{in} = 40 V f_{sw} = 65 kHz	V_{in} = 48 V f_{sw} = 68 kHz	V_{in} = 54 V f_{sw} = 75 kHz
Peak Efficiency	99.0% (98.4% with gate loss)	99.0% (98.5% with gate loss)	99.0% (98.5% with gate loss)
Full-Load Efficiency	96.7% (96.6% with gate loss)	97.1% (97.0% with gate loss)	97.4% (97.3% with gate loss)
Power Density	1840 W/in^3	2230 W/in^3	2510 W/in^3

range of a 48 V nominal intermediate bus for datacenter applications. Efficiency sweeps for 40-to-6.7 V and 54-to-9 V operation are shown in Fig. 5 and Fig. 7. Table IV lists the efficiency and power density of the converter for all tested input voltage and frequency conditions.

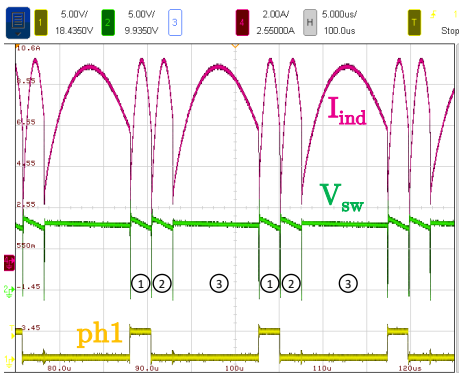

Fig. 9: Inductor current, switch node voltage, and ph1 gate signal waveforms for 48-to-8 V.

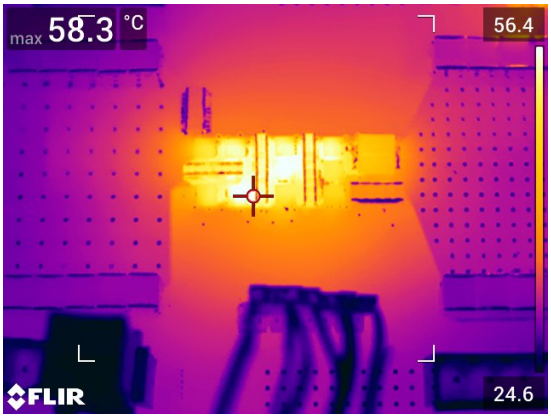

Fig. 10: Thermal image at full-load (40 A) for 48-to-8 V operation with fan cooling.

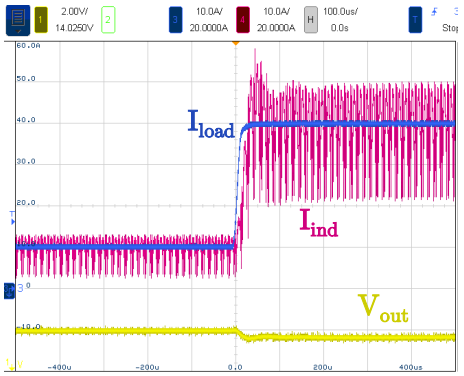

Fig. 11: Load-step from 10 A to 40 A for 48-to-8 V.

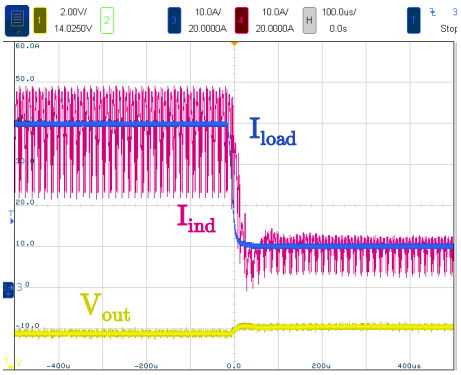

Fig. 12: Load-step from 40 A to 10 A for 48-to-8 V.

The high efficiency achieved by the converter decreases the impact of load regulation, as even though the converter operates in an open-loop fixed-ratio mode, it exhibits an output droop of only 234 mV (2.9% of V_{out}) at full-load as shown in Fig. 8.

Fig. 9 shows inductor current, I_L, switch node voltage, V_{sw}, and the ph1 gate drive signal for a 48 V input voltage. The three operating phases in Fig. 2 are labeled over two switching periods. As mentioned previously, the converter is operated above resonance to account for component tolerances and reduce conduction loss, as can be seen by the non-zero current at phase transitions. Partial ZVS at switch turn-on can be observed by noting that the switch node voltage goes below zero due to body diode conduction at the switch transitions. Future areas of research include optimizing the gate drive signals to improve the

ZVS performance of the converter.

Fig. 10 shows a thermal image of the converter operating at full-load at 48 V input. Even at 40 A output, the converter temperature did not exceed 59°C due to the low loss of the converter over its entire operating range. A bench-top fan was used to supply air cooling over the PCB.

Fig. 11 and Fig. 12 show the transient response of the converter for a step-up and step-down current load-step. Fig. 11 shows a transient from 10 A to 40 A at 48 V input. The inductor current stabilizes after approximately 200 μs after the initial ramp up in load current, while the voltage undershoot lasts less than 100 μs and then reaches its new steady state after approximately 160 μs.

Fig. 12 shows a transient from 40 A to 10 A at 48 V input. The inductor current stabilizes after approximately 120 μs after the initial ramp down in load current, while the voltage overshoot lasts less than 100 μs and then reaches its new steady state after approximately 200 μs.

Table V compares this work with some of the best existing works. The efficiencies given (including this work) include gate drive loss unless otherwise noted. The converter was tested at both 48-to-8 V and 54-to-9 V operating conditions to allow for a more equal comparison with prior work. The proposed topology has the highest power density of all the listed converters, and at 54-to-9 V operation the power density is almost 2$\times$ higher than the next most power dense converter (the EPC2905 buck [22]). The proposed topology's peak and full-load efficiencies are also higher than the EPC9205 buck converter, highlighting the potential efficiency advantages of the ReSC approach compared to more conventional approaches. The proposed topology also achieves a higher full-load efficiency compared to the Vicor VTM Current Multiplier [23], even at at higher full-load current. The power density and peak efficiency of the proposed converter are also higher as well, although the Vicor is a highly integrated product that may have more auxiliary circuitry compared to a prototype converter.

The proposed topology also has considerably higher power density and similar efficiencies compared to the 6-to-1 switched tank converter in [13]; however, [13] does not explicitly state whether their efficiencies include gate drive losses, which are often excluded in reported efficiencies for ReSC converters. Compared to the Google Switched Tank 4-to-1 converter [12], the proposed topology achieves roughly the same full and peak efficiencies for a larger conversion ratio (6-to-1 compared to 4-to-1).

Conclusion

In this paper, a multi-resonant cascaded series-parallel converter is proposed for 48 V to intermediate bus applications in datacenter power delivery architectures. The converter can achieve the same conversion ratio as traditional two-phase switched-capacitor converters with fewer capacitors and switches, allowing for very high power density and efficiency. A 48-to-8 V, 40 A converter prototype was built and tested, with 99.0% peak efficiency (98.5% with gate drive loss) and 2230 W/in^3 power density.

Table V: Comparison of this work and existing high step-down ratio bus converters

Reference	Topology	Voltage ratio	Output current (A)	Power density (W/in^3)	Efficiency	Notes
This Work	Multi-Resonant Cascaded Series-Parallel SCC	48-to-8 V	40	2230	full-load: 97.0%, peak: 98.5%	6-to-1 fixed-ratio, Si MOSFET
		54-to-9 V	40	2510	full-load: 97.3%, peak: 98.5%	
6-to-1 Switched Tank [13]	Resonant Dickson SCC	54-to-9 V	50	750	full-load: 97.18%*, peak: 98.55%*	6-to-1 fixed-ratio, GaN FET
EPC9205 [22]	Buck	48-to-8 V	14	1300	full-load: 93.2%, peak: 94.7%	GaN FET
Vicor VTM Current Multiplier [23]	Sine Amplitude Converter	48-to-8 V	30	∼900	full-load: 95.7%, peak: 95.8%	6-to-1 fixed-ratio
		55-to-9.2 V	30		full-load: 95.8%, peak: 95.9%	
Google 4-to-1 Switched Tank [12]	Resonant Dickson SCC	54-to-13.5 V	50	500	full-load: 97.41%, peak: 98.61%	4-to-1 fixed-ratio, Si MOSFET

* Not explicitly stated if efficiency number include gate drive loss

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