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Fabrication and Characterizations of Two-Dimensional Charge-Density-Wave Devices
Operating at Room Temperature

A Thesis submitted in partial satisfaction
of the requirements for the degree of

Master of Science

in

Electrical Engineering

by

Maedeh Taheri

September 2017

Thesis Committee:
    Dr. Alexander Balandin, Chairperson
    Dr. Roger Lake
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Committee Chairperson

University of California, Riverside

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Dedicated

To

My Parents

Farnoosh and Mahmood

ABSTRACT OF THE THESIS

Fabrication and Characterizations of Two-Dimensional Charge-Density-Wave Devices
Operating at Room Temperature

by

Maedeh Taheri

Master of Science, Graduate Program in Electrical Engineering
University of California, Riverside, September 2017
Dr. Alexander Balandin, Chairperson

The charge-density-wave (CDW) phase is a macroscopic quantum state consisting of a

periodic modulation of the electronic charge density which is accompanied by a periodic

distortion of the atomic lattice in quasi-one-dimensional (1D) or layered quasi-two-

dimensional (2D) metallic crystals. Several layered transition metal dichalcogenides

(TMDs) reveal the CDW phase transitions at rather high temperatures. These transitions

can be affected by environmental conditions, film thickness and applied electric bias.

This thesis, reports results of investigation focused on developing and optimizing

fabrication procedures for devices implemented with a specific TMD - 1T polytype of

TaS_2. This material undergoes the transition from a nearly commensurate CDW phase to

incommensurate CDW phase at 350 K. This phase transition is accompanied by a lattice

reconstruction, which results in strong modifications of the material's electrical

properties. The change in the electrical characteristics in the transition point can be used

for fabricating oscillator devices operating at room temperature. In this thesis, I briefly

outline CDW theoretical background and then, describe in details the fabrication steps

required for such devices. Specifically, I describe exfoliation of the 2D material, protection from oxidation, transfer process, spin coating, electron beam lithography, metal deposition and lift-off process. The current-voltage characteristics of the resulting devices show reproducibly an abrupt change in electrical current and a hysteresis loop. The hysteresis loop can be used for building a voltage-controlled oscillator. The low-frequency noise measurements have been conducted in a wide temperature range in order to elucidate the physical mechanism of the phase transition and electronic transport. The noise spectral density shows $1/f$ type spectrum with signature of the generation – recombination (G-R) bulges at some bias points (f is the frequency). The obtained results are important for developing the 2D electronic device technology based on the CDW effects.

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Chapter 1

Introduction to Charge-Density-Waves

1.1 Motivations

Since pursuing Moore's law still plays a significant role in electronic industry, scientists have put lots of efforts in designing electronic devices with new materials and novel geometries to tackle its scaling challenge [1]. By introducing two-dimensional (2D) materials such as graphene, transition metal dichalcogenides (TMDs), bismuth selenide (Bi_2Se_3) and bismuth telluride (Bi_2Te_3), the window opened toward maintaining transistors with thin channels, as well as the control over their thicknesses in the atomic scale [1]. TMDs are a family of materials with stacked layers of transition metal atoms (e.g. Mo, Ti, Zr, Ta, etc.), sandwiched between two layers of chalcogen atoms (e.g. S, Se, Te). The layers are bonded together with weak van der Waals forces and can be exfoliated into ultrathin layers. Number of TMDs members have been reported that maintain bandgap tunability, high mobility and high switching on/off ratios which make them promising for electronics and optoelectronic devices [2].

Among the TMDs family, multiple of its members such as 1T polytypes of TaS_2, $TaSe_2$ and $TiSe_2$ present an interesting quantum states known as charge-density-wave (CDW) phase, which is accompanied by periodic lattice distortions [3, 4]. The physic behind this phenomenon and its origin has grabbed lots of attentions. Recently several field-effect transistors (FET) and two-terminal devices, which implement the thin films of CDW materials have been fabricated to explore their properties [4-6]. Reports on the cost-effective voltage-controlled oscillator based on integrated tantalum disulfide-boron nitride-graphene devices, which operate at room temperature, and the prospects of 1T-TaS_2 as a possible memristive elements are among reasons that have motivated me to study the CDW behavior of tantalum disulfide devices [4, 7]. Also, lack of sufficient low-frequency noise measurements on these CDW materials is another intriguing region that needs to be explored. For satisfying these motivations and developing electronic devices based on CDW materials, a background knowledge on charge-density-waves theory is required, which would be followed in the next section.

1.2 Brief Concepts of Charge-Density-Waves Effects

From the Schrödinger equation defined for free electrons, in which the potential V=0, the dispersion relation is obtained as [8]:

$$\epsilon_k = \frac{\hbar^2 k^2}{2m}$$

(1.1)

Where, ϵ_k is the energy of electron at a wave vector k, $\hbar$ is the plank constant over 2π, k is the wave vector and m is the mass of a free electron here. The band structure of free

electrons is represented in Figure 1.1. Now consider a one-dimensional electron gas, the electron density defines the characteristic of electrons in this system. Then assume an external electrostatic potential is applied to this system. The electrons try to diminish the effects of this external potential which lead to redistribution of the carriers in the system and can be considered as an induced electron density. This induced electron density leads to the induced electrostatic potential. Such a characteristic is known as screening effects and would be considered as the following formula [9]:

$$\Phi^{tot}(r,\omega) = \Phi^{ext}(r,\omega) + \Phi^{ind}(r,\omega) \tag{1.2}$$

Where, $\Phi^{tot}(r,\omega)$, $\Phi^{ext}(r,\omega)$ and $\Phi^{ind}(r,\omega)$ are known as total, external and induced potentials, respectively. The charge density in this structure is defined as:

$$\rho^{tot}(r,\omega) = \rho(r,\omega) + \rho^{ind}(r,\omega) \tag{1.3}$$

Where $\rho^{tot}(r,\omega)$, $\rho(r,\omega)$ and $\rho^{ind}(r,\omega)$ are total charge distribution, charge density before exposing to the external potential and induced charge distribution, respectively. The relation between electron density and the potential leads to the famous Poisson equation [9-11].
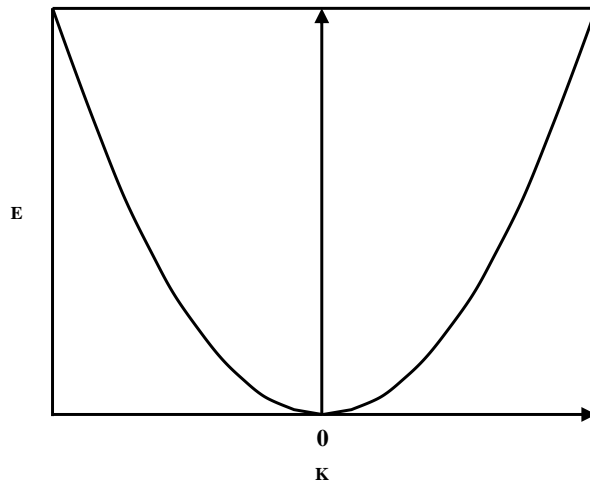

Figure 1.1: The band diagram of free electrons is plotted.

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Consider the situation that external potential is applied at the position r' which induces a change in the charge density at the position r. So, the relation between these two functions can be defined by the convolution between a function, defined as electron response function, and the potential. In another word, the convolution of these two functions is an integral expressed over the changes in the position of potential and leads to the definition of induced charge density. The following equation can represent such a relation between the potential and charge density for one-dimensional system.

$$\rho^{ind}(r,\omega) = e^2 \int dr'. \chi(r,r',\omega)\Phi^{tot}(r',\omega) \tag{1.4}$$

where e is an electron charge, ω is angular frequency and $\chi(r,r',\omega)$ is electron response function. Using random-phase approximation, a definition for $\chi(r,r',\omega)$ can be found which is known as electron response function in momentum space [9-11]:

$$\chi(q,q';\omega) = \lim_{\eta \to 0^+} \sum_{i,j} \frac{f_i - f_j}{\hbar(\omega - \omega_{ij}) - j\eta} \times \langle i|e^{jq.r'}|j\rangle \langle j|e^{-jq'.r''}|i\rangle \tag{1.5}$$

f_i is occupation function of the single-particle state and $\hbar\omega_{ij} = \varepsilon_i - \varepsilon_j$ is the difference between energy of the origin and the destination transition between two states. By considering the static case and using the notation $F(q) = -\chi(q, \omega = 0)$, the electron response function for one-dimensional electron gas would be reduced into [9-11]:

$$F(q) = \frac{N_1}{\epsilon_f} \frac{1}{2q} log \left| \frac{1 + \frac{q}{2}}{1 - \frac{q}{2}} \right| \tag{1.6}$$

Where, N_1 is the Fermi gas density and equal to $\frac{2k_f}{\pi}$. k_f and ϵ_f are the Fermi momentum and energy, respectively. Solving this equation leads to very interesting relationship

between external potential as perturbation and charge density, that is induced by that perturbation. The most interesting fact is that this function has singularity at the $q = 2k_f$ for 1D free electron gas. Such characteristics which exist inside electron response function may be interpreted as an instability inside the system. The Figure 1.2 represents static response function of 1D, 2D, 3D free electron gas at zero temperature [10, 11].
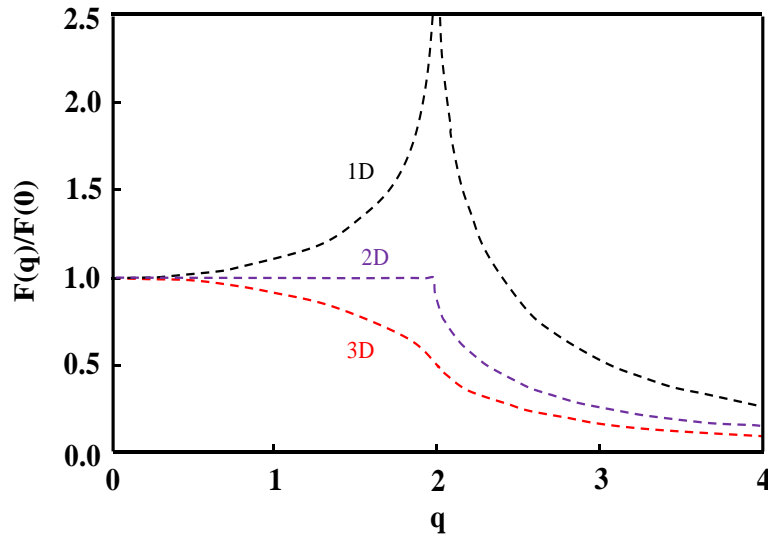
Figure 1.2: The plot shows the static response function F(q), of 1D, 2D and 3D free electron gas, based on wave vector q and at zero temperature. The horizontal axis is represented in the Fermi momentum units, k_f. For 1D system the divergence in response function occurs at $q = 2k_f$ [9, 11].

The system that is perturbed with q around $2k_f$ would be stable. However, this stability can turn into instability with small distortion from the environment. The divergence inside static electron response function is due to the topology of Fermi surface which is known as Fermi surface nesting [11]. The most important part of the response function is the correlation between the states i and j which one is empty and one is full

with momentum difference of $2k_f$. In one-dimensional free electron gas, the Fermi surface is determined by pair of states, one full and the other empty, with exact $2k_f$ difference and hence number of perfect nesting is high. While with the increase in dimensionality to two or three, the shape of Fermi surface changes to circle or sphere, respectively [11]. Figure 1.3 shows the Fermi surface for 1D and 2D free electron gas. Such shapes of circular or spherical Fermi surface in higher dimensions, reduce the possibility of successful perfect nesting and remove the singularity in the static response function. The one-dimensional materials are chains bound together and hence affect each other. These materials are known as quasi-one-dimensional materials. The Fermi surface for these materials is something between one and two-dimensional and can be modeled as Figure 1.4. As can be seen in the figure the high possibility of perfect nesting in quasi-one-dimensional electron gas is presented [11].
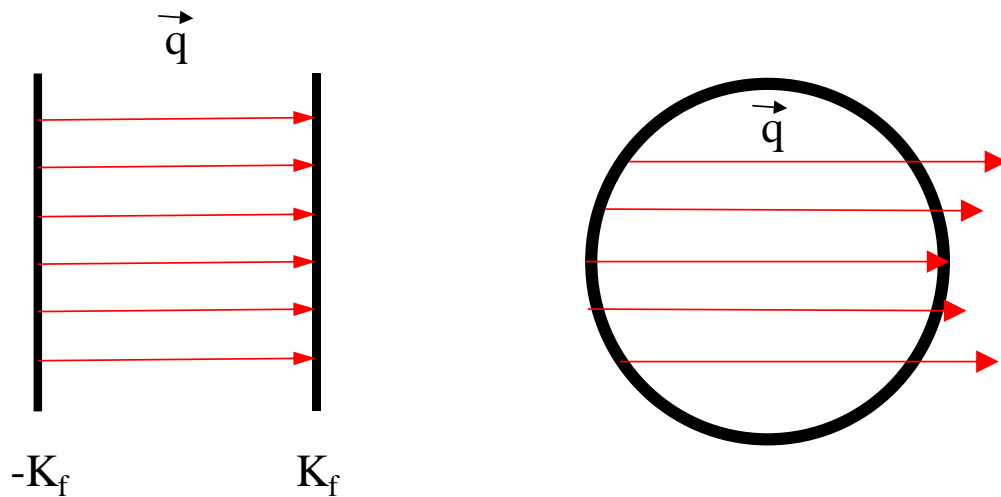
Figure 1.3: Images represent the topology of Fermi surface for 1D (left) and 2D (right) free electron gas. The arrows point to pairs of full and empty states.
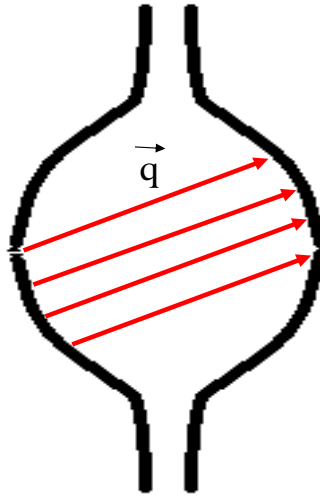
Figure 1.4: The Fermi surface is shown in the quasi-one-dimensional electron gas. The arrows demonstrate perfect nesting occurring in one direction, for some portion of states.

In a 1D free electron gas systems, which is coupled to the underlying ions via electron-phonon interaction, the coupled electron-phonon system is not stable [11]. Considering the point that static electron response function has logarithmic singularity at $q = 2k_f$, the reduction of phonon frequencies (based on phonon dispersion relation) would become more apparent at these wave vectors. If the temperature is decreased, the phonon frequencies at $q = 2k_f$ would go to zero at specific value of temperature, known as the transition temperature [11]. At these transition temperatures, the system may undergo a lattice distortions that would break the symmetry inside the crystal. Therefore, this instability in the coupled electron-phonon in 1D electron gas systems may lead to the modulation of charge density and change the energies of the related states [11]. Such changes in the energy may cause new band gap in the dispersion relation of quasi-one-

dimensional system. This gap can make a metal system to act as an insulator and result in a new state. This transition would be referred to as the Peierls transition [11]. The Figure 1.5 demonstrates the opening of a gap (represented with Δ) in the energy at the Fermi level (k_f) for a quasi-one-dimensional metallic system.

As the instability occurs, the energy of electron at the $q = \pm k_f$ is reduced and the total energy of the system is lowered. Therefore, the system will become stable. The change in the charge density may makes atoms see different potential and move to new stable positions. Such a new gap that is introduced by a previous unstable system is due to the modulation of the atomic positions. Inside the quasi-1D material the energy needed for such a modulation at low temperature is less than the gain in the conduction electron energy, so the new system is more favorable. These changes in atomic position and ρ lead to a periodic charge density with wavelength of $\lambda_c = \frac{\pi}{k_f}$ (in quasi-1D metal), which is known as charge-density-waves (CDW) [12]. While the main reason of CDW phase transition may be discussed as to be the high electron-phonon interaction, it is possible that electron-electron or electron-hole interactions lead to instability which may be known as excitonic insulator phase [13, 14]. Consider the case that density of carriers in the metal are dramatically reduced, then the number of carriers to form screening effect due to their columbic interaction is highly decreased. Such reduction will lead to bound states that make a gap in the metal and turn it into an insulator [14]. It should be noted that while the source of instability is different from ones that caused by electron-phonon coupling, the consequence of this instability is pretty much the same. For instance, such instability is seen in titanium diselenide (1T-TiSe$_2$) [14, 15].
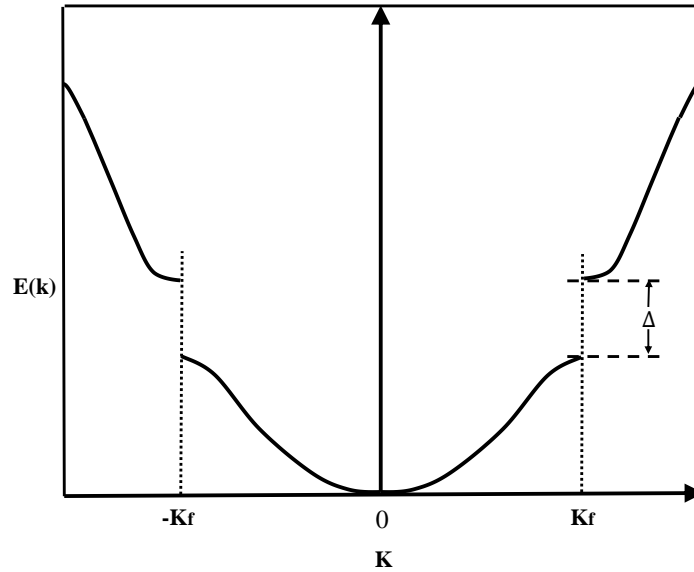
Figure 1.5: The band structure of quasi-one-dimensional metal in the effects of charge-density-waves. The band gap opening occurs at the Fermi level (k_f) and represented with Δ [11].

If the period of the CDW is in proportion with the underlying lattice period, then the CDW named as commensurate mode, while if it is not proportional then it will be called as incommensurate CDW phase. Considering these two defined states, it is possible to consider a phase between these two known as nearly commensurate mode. Considering these three conditions, the lattice inside 2D materials can change and form different periodic structures due to the CDW effects. Consider the bulk of 1T-TaS$_2$ as the richest candidate in phase diagram among the transition metal dichalcogenide family (which will be discussed in next chapter with details) [15]. Below 180 K the 1T-TaS$_2$ shows commensurate CDW characteristic [5]. The displacements inside the atoms are interesting in this phase and 12 Ta atoms approach the 13th Ta atom and form the Star-of-David shape as shown in Figure 1.6 left, labeled as CCDW (commensurate CDW) [7].

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The tantalum atoms displacements are in-plane while most of sulfur transitions are out-of-plane. In this phase the d orbital of Ta atoms regroup and form a pseudo-gap at the Fermi level which leads to semiconducting characteristic in this phase [15]. As temperature increases and settle into the range of 180 K to 350 K another phase can be seen which marked as nearly commensurate, NCCDW (nearly commensurate CDW) and is represented in the Figure 1.6, middle. At this phase the Star-of-David clusters form hexagonal-shape domains which are separated by incommensurate regions. If the temperature goes beyond 350 K to 550 K, stars are disappeared as shown and labeled with ICCDW (incommensurate CDW) in Figure 1.6, right [5, 7, 15].
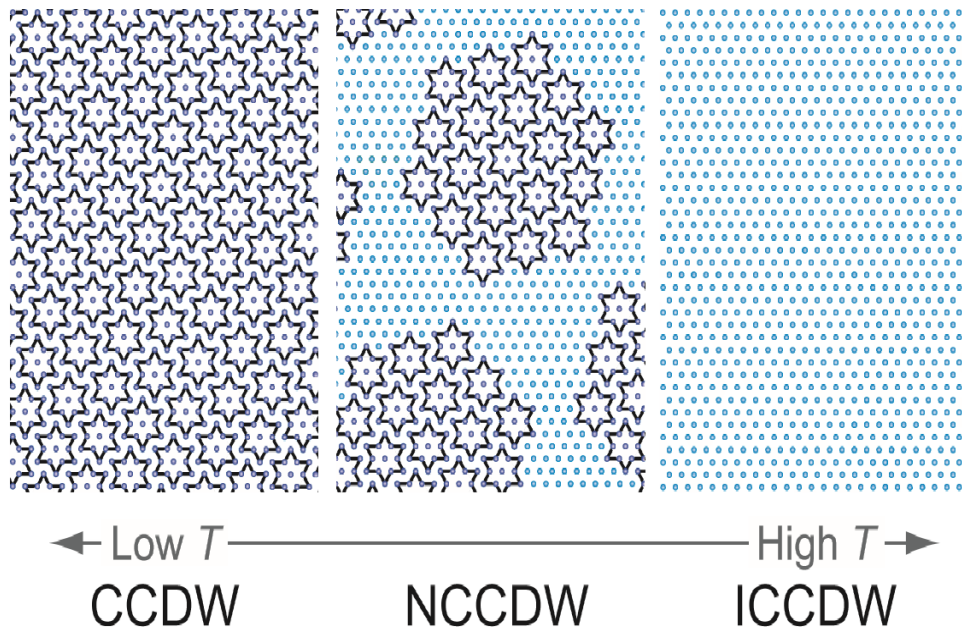
Figure 1.6: The rearrangement of atoms of 1T-TaS$_2$ crystals per different CDW phase transitions at different temperature ranges. At low temperature, the structure is in commensurate phase CCDW (left) and Ta atoms form a star-of-David shape. By increasing the temperature, it moves to nearly commensurate phase NCCDW (middle) and then afterwards shift to incommensurate phase ICCDW (right) at high temperature, where the stars-of-David domains disappear [7]. The Figure is reprinted from M. Yoshida, R. Suzuki, Y. Zhang, M. Nakano, Y. Iwasa, *Sci. Adv.*, 1 (9) (2015). This work is licensed under CC BY-NC (*http://creativecommons.org/licenses/by-nc/4.0/*).

By considering the gap inside the metallic band structure, one might assume that the transport of electrons in 1D materials can be diminished and this is almost a correct assumption. However, another kind of carrier transmission can replace the old metallic one which known as collective charge transport mode [12]. By applying electric field the Fermi level at the electrodes would be altered and the atoms move from their CDW positions that lead to change in the charge density. Such changes along the time can transfer charge from one point to the other that considered as collective charge density transport [12]. This is something like breathing mode in 1D materials. The charge is localized at the valley of the wave, by applying electric field the charge can overcome the barrier and moves to the next valley and continues these transfers till gets to the electrode with lower Fermi level. It may be concluded that a threshold voltage is required for charge to overcome the barrier and hence such characteristic can be seen in the current-voltage diagram as threshold voltage. This phenomenon is known as sliding or depinning of CDWs [12].

References:

[1] G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S. K. Banerjee and L. Colombo, *Nature Nanotechnology*, 9, 768-779 (2014).

[2] A. K. Geim, I. V. Grigorieva, *Nature*, 499, 419-425 (2013).

[3] R. Hovden, A. W. Tsen, P. Liu, B. H. Savitzky, I. Baggari, Y. Liu, W. Lu, Y. Sun, P. Kim, A. N. Pasupathy and L. F. Kourkoutis, *PNAS*, 113 (41), 11420-11424 (2016).

[4] G. Liu, B. Debnath, T. R. Pope, T. T. Salguero, R. K. Lake and A. A. Balandin, *Nature Nanotechnology*, 11, 845-851 (2016).

 [5] Y. Yu, F. Yang, X. F. Lu, Y. J. Yan, Y. Cho, L. Ma, X. Niu, S. Kim, Y. Son, D. Feng, S. Li, S. Cheong, X. H. Chen and Y. Zhang, *Nature Nanotechnology*, 10, 270-276 (2015).

[6] A. W. Tsen, R. Hovden, D. Wang, Y. D. Kim, J. Okamoto, K. A. Spoth, Y. Liu, W. Lu, Y. Sun, J. C. Hone, L. F. Kourkoutis, P. Kim and A. N. Pasupathy, *PNAS*, 112 (49), 15054-15059 (2015).

[7] M. Yoshida, R. Suzuki, Y. Zhang, M. Nakano, Y. Iwasa, *Sci. Adv.*, 1 (9) (2015).

[8] C. Kittel, *Introduction to Solid State Physics*, John Wiley & Sons, Inc. (2005).

[9] B. Mihaila, arXiv:1111.5337v1 (2011).

[10] K. Koumoto, T. Mori, *Thermoelectric Nanomaterials*, Springer, 182 (2013).

[11] G. Grüner, *Denisty Waves in Solids*, Perseus Publishing (1994).

[12] R. E. Thorne, *Physics Today*, 49 (5), 42-47 (1996).

[13] M. Imada, A. Fujimori, Y. Tokura, *Reviews of Modern Physics*, 70 (4), 1039-1263 (1998).

[14] H. Cercellier, C. Monney, F. Clerc, C. Battaglia, L. Despont, M. G. Garnier, H. Beck, P. Aebi, L. Patthey, H. Berger, L. Forró, *Physical Review Letters*, 99, 146403 (2007).

[15] K. Rossnagel, *J. Phys.: Condens. Matter*, 23 (21) (2011).

Chapter 2

Literature Review

This chapter is dedicated to the review of recent investigations on the charge-density-waves specifically in two-dimensional (2D) materials. First, briefly some 2D materials are introduced. Then I discuss recent studies on the charge-density-wave phenomenon observed in these materials.

2.1 The Overview on 2D Materials

One can say that the birth of 2D materials is back to 2004 by introducing graphene. Graphene, a monolayer of graphite, was introduced in 2004 as first 2D material [1]. This structure was first introduced theoretically by Wallace long before and considered to be unstable [2]. However, in 2004 this structure fabricated from graphite and showed remarkable electrical transport characteristics [1]. Since then, 2D materials have become promising research fields and grabbed lots of attentions.

Today lots of 2D materials with different properties are introduced and predicted to be more than 500 different 2D materials in nature [3]. Such a huge number of materials

open a new arena for technology to achieve new horizons. For such a promise, it is critical to know the most important characteristics of these materials in details. One of the most promising group of 2D materials that demonstrates different characteristic is known as transition metal dichalcogenides (TMD). TMDs are materials with general formula of MX_2 with M to be transition metals such as (Ti, Hf, Zr, V, Nb, Ta, Mo, W, Tc, Re, Pd and Pt) while X is S, Se or Te. One of the most explored member of this group is MoS_2 that shows direct semiconducting band gap in monolayer structure and good carrier mobility which is favorable for future field-effect transistors [4, 5]. One of the least explored member of this group is known as tantalum disulfide, TaS_2.

The bulk form of tantalum disulfide is the stack of TaS_2 layers which consist of tantalum atoms sandwiched between sulfur atoms in strong in-plane covalence bonds and weak out-of-plane van der Waals bonds that can be exfoliated to form monolayer. Previous investigations revealed that TMDs including TaS_2 may have two known phases, named as 2H and 1T [6]. In 2H phase, sulfur atoms are ordered around tantalum atoms in a trigonal prismatic configuration and sulfurs are rotated 60° with respect to the previous layer. But in the 1T phase, sulfurs atoms are set around tantalum atoms in an octahedron arrangement as the unit cell is illustrated in Figure 2.1 [7]. Figure 2.2 shows a crystal structure of two-dimensional tantalum disulfide in both 1T and 2H phases which are modeled using "3D Studio Max" software.
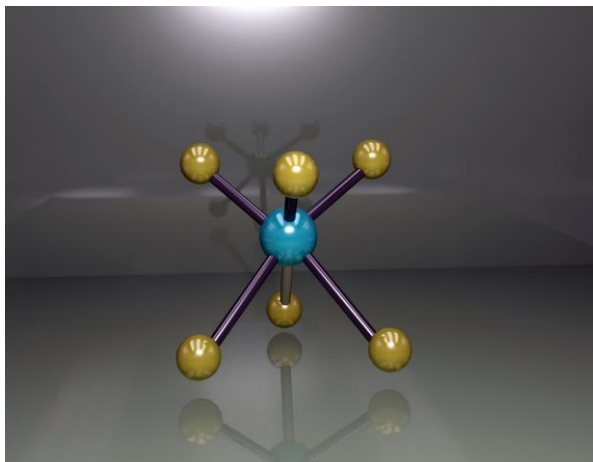
Figure 2.1: The unit cell of 1T polytype of TaS_2 is shown. Yellow atoms representing sulfur S, while blue ones illustrating tantalum Ta. In this crystal structure, sulfur atoms are ordered around Ta atom, on the corners of an octahedron.
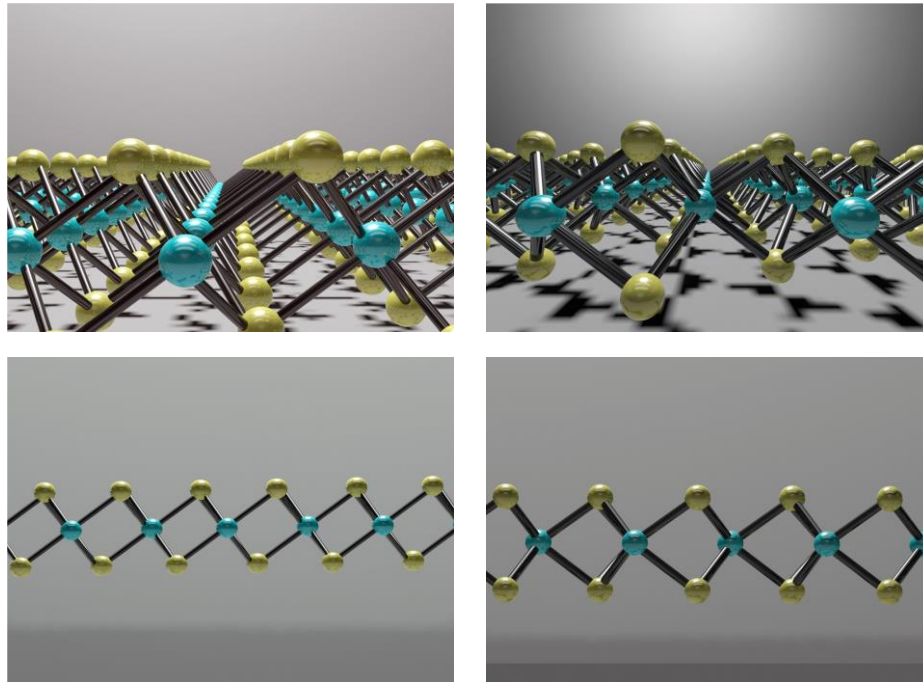
Figure 2.2: The left images (top and bottom) show one layer of octahedral polytype of TaS_2 known as 1T. The right images (top and bottom) represent monolayer of trigonal prismatic phase known as 2H. Yellow atoms depict sulfur S, and blue ones show tantalum atoms Ta, which are sandwiched between sulfur atoms.

2.2 CDW Effects in 2D Materials

Recently the charge-density-waves in few-layer $1T\text{-}TaS_2$ have grabbed lots of attentions just like its bulk form. One of the early theoretical studies in recent decade, revealed that monolayer TaS_2 (in 1T phase, not presented at that time in literature directly) exhibits metallic behavior with 2.47, 2.48 Å bond lengths [8] like its bulk form. In 2011, reports published on the origin of CDW in some layered TMD materials, as $1T\text{-}TaS_2$, $2H\text{-}TaSe_2$ and $1T\text{-}TiSe_2$ and from both experimental and theoretical perspectives. It pointed out that all those three compounds ($1T\text{-}TaS_2$, $2H\text{-}TaSe_2$, $1T\text{-}TiSe_2$) have high electrical resistivity above transition temperature (at 550 K for $1T\text{-}TaS_2$, at 300 K for $2H\text{-}TaSe_2$ and $1T\text{-}TiSe_2$) which is $\rho \geq 0.1$ mΩ cm and it is almost 50 times greater than that of copper at 373 K [6].   Another report showed theoretical calculation of $1T\text{-}TaS_2$ monolayer as a host surface of clusterization and detection of platinum [9].

The bulk of $1T\text{-}TaS_2$ demonstrates several CDW transitions as the temperature varies. When temperature comes down below 550 K, it enters metallic incommensurate CDW phase (ICCDW) and by reaching 350 K undergoes nearly commensurate CDW phase (NCCDW). As temperature falls to 180 K, bulk of $1T\text{-}TaS_2$ enters commensurate CDW phase (CCDW) [10]. In 2015, Yu et al. [10] observed CCDW-NCCDW and NCCDW-ICCDW phase transitions' dependencies on the films thicknesses. By reducing the film thickness and in cooling process, both of phase transitions move to lower values. Then under ~10 nm $1T\text{-}TaS_2$ film thickness, CCDW-NCCDW phase transition disappears and when the thickness gets down to ~3 nm the NCCDW-ICCDW phase transition disappears as well [10]. Therefore, film thickness is an important parameter for

attaining long-range charge ordering. Also, they made a FET device and performed lithium intercalation of 1T-TaS$_2$ via applying gate voltage [10]. In the same year, another paper published on the structures of CDW on the few-layer 1T-TaS$_2$. Tsen et al. [11] presented tantalum disulfide device encapsulated with hexagonal boron nitride. The device was maintained operating at low temperature around 200 K. They used transmission electron microscopy and electrical measurements to conclude that the conductance of 1T-TaS$_2$ device is dominated by incommensurate structure [11]. In an interesting application-based report, Balandin and coworkers [12] reported an oscillator device based on CDW at room temperature using thin film of 1T-TaS$_2$. Using chemical vapor transport method, they have grown uniform high quality bulk TaS$_2$ and then using exfoliation technique, a prototype device was fabricated. To protect the material from oxidation, the 1T-TaS$_2$ crystal has been capped using hexagonal boron-nitride. With the tantalum disulfide crystal specified to be <10 nm, they observed the disappearance of commensurate to nearly commensurate CDW phase transition at 180 K and the persistence of nearly commensurate to incommensurate CDW phase transition at 350 K. They also witnessed the insulator-to-metal (IMT) and MIT transition due to the applied electric field and at specific threshold voltages for various temperatures. Considering 1T-TaS$_2$ device switching between IMT and MIT states, proper oscillator device operating at the room temperature was achieved. Such an oscillator started to operate after passing a threshold voltage in which CDW would be depinned. In addition, by integrating top-gate graphene field-effect transistor with 1T-TaS$_2$ device they were able to tune the oscillator frequency via applying voltage. Such a device is highly desirable and has led to a

voltage-controlled oscillator (VCO) functional at room temperature [12]. In another report, Yoshida et al. [13] discussed the memristive phase switching in 2D crystals of 1T-TaS_2. They suggested a presence of some metastable metallic states and possibility of memristive function by switching between non-volatile metastable states. In 2016, Hovden et al. [14] studied the lattice disorder in CDW phase of thin layers of 1T-TaS_2. Using atomic resolution scanning transmission electron microscopy (at room and low temperatures) they were able to directly image the periodic lattice distortions of commensurate and nearly commensurate phases. Furthermore, crystallographic stacking domains and their boundaries in thin layer of 1T-TaS_2 were observed. They reported two stacking orders, one as trigonal array in which all Ta atoms lie on top of each other [14]. While in the other one, the hexagonal array, almost half of the layers have their Ta sites shifted about one bond length relative to the other layers [14]. They suggested that these stacking faults would produce fractional translation in the charge-density-waves and might lead to changes in the electronic properties, chiefly in thin films [14].

Till now, all reports have used exfoliated TaS_2 as the sample of their CDW-based devices, while Fu et al. [15] reported on the CDW of 1T-TaS_2 using chemical vapor deposition (CVD). Implementing the *in-situ* temperature-dependent Raman spectroscopy, they witnessed different CDW phase transitions for 16-nm-thick grown sample. Also, a comparison was made between the mechanically exfoliated 1T-TaS_2 samples and the CDV-grown ones. It appeared that the CVD-grown samples showed peaks with the broader widths which could be the result of introducing defects in the CVD process [15]. In 2017, Zhao et al. [16] investigated the effect of substrate on the CDW of ultrathin 1T-

TaS$_2$. They compared nearly commensurate to commensurate CDW phase transition of samples with same thicknesses on different substrates such as SiO$_2$/Si, sapphire, epitaxial graphene, vanadium oxide and strontium vanadium oxide. Surface roughness was concluded to be one of the influential factor in CDW transition temperature and hysteresis. While doping and charge transferring from the substrate has negligible impact on the CDW transition [16].

Tantalum disulfide is not the only 2D material that shows CDW in few-layer structures and there are other reports on such properties in other 2D Materials. One of the earliest report of this kind is in 2011, in which Balandin and coworkers [17] reported a behavior in a few-layer TiTe$_2$ material, similar to charge-density-waves characteristics. Using back-gate field-effect structure, they presented current-voltage characteristic of TiTe$_2$ showing strong non-linearity at room temperature. Xu et al. [18] in 2013 showed CDW behavior in the ultrathin sheet of VSe$_2$ due to strong electron coupling interaction between neighboring vanadium network. Using wet exfoliation, the proper thin film of VSe$_2$ achieved from the bulk and resistivity versus temperature curve exhibited CDW transition around 135 K [18]. Falmbigl et al. [19] studied a compound of $([SnSe]_{1.15})_m$ $(VSe_2)_n$ (for m, n = 1, 2, 3 and 4) to investigate the effects of VSe$_2$ dimensionality on its CDW state. By controlling m and n, they had good control over the films thicknesses and measured electrical resistivity versus temperature for different thicknesses of VSe$_2$ [19]. Samnakay et al. [20] studied bulk and few-layer 1T-TaSe$_2$ structure from Raman perspective. They showed that by reducing thicknesses from 150 to 35 nm, the

commensurate CDW phase transition temperature decreased from 473 K to 413 K due to the change in Raman peaks' positions [20].

In 2016, Sugawara et al. [21] presented CDW transition in monolayer of 1T-TiSe$_2$. The interesting point about their report is that by using angle-resolved photoemission spectroscopy they demonstrated that CDW in this monolayer happens without Fermi surface nesting [21]. They concluded that due to low electron-doped of their sample, the probability of nesting in Fermi surface is highly unlikely. They also proposed that because of positive band gap above CDW transition temperature the Jahn-Teller type lattice distortion might not be the reason behind CDW in this case [21]. Then, they investigated the excitonic condensate and suggested this condition as suitable reason behind CDW effect in monolayer 1T-TiSe$_2$ [21].

Wang et al. [22] used modified chemical vapor transport (CVT) method to grow sub-10 nm 1T-TiSe$_2$ films and investigated their charge-density-waves behavior. The CDW phase transition temperature of the as-grown crystal was observed via temperature-dependent resistance measurements of 1T-TiSe$_2$ device [22]. In one of the most recent investigation available on CDW properties within 2D materials, Kern and coworkers [23] systematically studied the Raman analysis for detecting CDW within bulk to few-layers 1T-TiSe$_2$. They presented that by monitoring changes in the peak position of Eg mode near 136 cm^{-1}, the charge-density-wave transitions can be observed [23]. Also, the Raman modes were suggested as a useful tool for determining the number of layers in thin films of 1T-TiSe$_2$. They introduced Raman spectroscopy-based method as an

effective way of inspecting CDW transition, however their accuracy could be influenced by surface oxidation, intrinsic defects and substrate effects [23].

References:

[1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, A. A. Firsov, *Science*, 306, 666-669 (2004).

[2] P. R. Wallace, *Physical Review*, 71 (9), 622-637 (1947).

[3] E. Gibney, *Nature*, 522, 274-276 (2015).

[4] K. Mak, C. Lee, J. Hone, J. Shan and T. F. Heniz, *Physical Review Letters*, 105, 136805 (2010).

[5] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti and A. Kis, *Nature Nanotechnology*, 6, 147-150 (2011).

[6] K. Rossnagel, *J. Phys.: Condens. Matter*, 23, 213001 (2011).

[7] A. H. Thompson, F. R. Gamble, J. F. Revelli, *Solid State Communications*, 9, 981-985 (1971).

[8] Y. Ding, Y. Wang, J. Ni, L. Shi, S. Shi, W. Tang, *Physica B*, 406, 2254-2260 (2011).

[9] H. D. Ozaydin, H. Sahin, R. T. Senger and F. M. Peeters, *Annalen der Physik*, 526 (9-10), 423-429 (2014).

[10] Y. Yu, F. Yang, X. F. Lu, Y. J. Yan, Y. Cho, L. Ma, X. Niu, S. Kim, Y. Son, D. Feng, S. Li, S. Cheong, X. H. Chen and Y. Zhang, *Nature Nanotechnology*, 10, 270-276 (2015).

[11] A. W. Tsen, R. Hovden, D. Wang, Y. D. Kim, J. Okamoto, K. A. Spoth, Y. Liu, W. Lu, Y. Sun, J. C. Hone, L. F. Kourkoutis, P. Kim and A. N. Pasupathy, *PNAS*, 112 (49), 15054-15059 (2015).

[12] G. Liu, B. Debnath, T. R. Pope, T. T. Salguero, R. K. Lake and A. A. Balandin, *Nature Nanotechnology*, 11, 845-851 (2016).

[13] M. Yoshida, R. Suzuki, Y. Zhang, M. Nakano, Y. Iwasa, *Sci. Adv.*, 1 (9) (2015).

[14] R. Hovden, A. W. Tsen, P. Liu, B. H. Savitzky, I. Baggari, Y. Liu, W. Lu, Y. Sun, P. Kim, A. N. Pasupathy and L. F. Kourkoutis, *PNAS*, 113 (41), 11420-11424 (2016).

[15] W. Fu, Y. Chen, J. Lin, X. Wang, Q. Zeng, J. Zhou, L. Zheng, H. Wang, Y. He, H. He, Q. Fu, K. Suenaga, T. Yu and Z. Liu, *Chem. Mater.*, 28, 7613-7618 (2016).

[16] R. Zhao, Y. Wang, D. Deng, X. Luo, W. J. Lu, Y. Sun, Z. Liu, L. Chen and J. Robinson, *Nano Lett.*, 17, 3471-3477 (2017).

[17] J. M. Khan, D. Teweldebrhan, C. M. Nolen and A. A. Balandin, *Mater. Res. Soc. Symp. Proc.*, 1344 (2011).

[18] K. Xu, P. Chen, X. Li, C. Wu, Y. Guo, J. Zhao, X. Wu and Y. Xie, *Angew. Chem.*, 125, 10671-10675 (2013).

[19] M. Falmbigl, A. Fiedler, R. E. Atkins, S. F. Fischer and D. Johnson, *Nano Lett.*, 15, 943-948 (2015).

[20] R. Samnakay, D. Wickramaratne, T. R. Pope, R. K. Lake, T. T. Salguero and A. A. Balandin, *Nano Lett.*, 15, 2965-2973 (2015).

[21] K. Sugawara, Y. Nakata, R. Shimizu, P. Han, T. Hitosugi, T. Sato and T. Takahashi, *ACS Nano*, 10, 1341-1345 (2016).

[22] J. Wang, H. Zheng, G. Xu, L. Sun, D. Hu, Z. Lu, L. Liu, J. Zheng, C. Tao and L. Jiao, *J. Am. Chem. Soc.*, 138, 16216-16219 (2016).

[23] D. L. Duong, G. Ryu, A. Hoyer, C. Lin, M. Burghard and K. Kern, *ACS Nano*, 11, 1034-1040 (2017).

Chapter 3

Fabrication Process

3.1 Introduction

In this chapter, I have explained the steps toward fabricating the two-dimensional charge-density-waves material (1T-TaS$_2$) devices. The steps for creating electronic circuits on top of substrates require special environment with reduced number of particles. Therefore, one can avoid contamination as much as possible and improve devices performance. In this work the fabrication has been done in the class 100/1000 cleanroom facility and the steps are described as follows.

3.2 Preparing Silicon Substrate

Before transferring a material on top of SiO$_2$/Si substrate (300 nm oxide layer), I need to make sure the surface of substrate is as clean as possible to avoid crystals detaching in further fabrication steps. To maintain this, first cut the silicon wafer into die and then spray them with acetone and rinse afterwards with isopropyl alcohol (IPA) and deionized water (DI) water and dry it with blowing nitrogen gas. After drying, the SiO$_2$/Si pieces are treated with oxygen plasma for 3-5 minutes with the power of 50 watts

using the inductively coupled plasma (ICP) etch machine. In this ICP system by implementing strong radio frequency (RF) electromagnetic field to the wafer platter, the plasma is produced. Thus, the positive ions drift to the wafer platter and collide with samples. This will help cleaning the substrates and increase the chance that crystals stick well to the surface in the following steps.

3.3 Exfoliation of Transition Metal Dichalcogenides

Transition metal dichalcogenides (TMDs) are a group of material in the form of MX_2, in which M is a transition metal atom and X is a chalcogen. In these crystals, the transition metal atoms are sandwiched between layers of chalcogen atoms and they form layered structures. Through van der Waals attraction the layers are bounded to each other. So, via mechanical exfoliation one can easily separate these layers and move from bulk crystals to the world of thin and only few-layer-thick of TMD materials.

In this work, the bulk of $1T\text{-}TaS_2$ is prepared through chemical vapor transport (CVT) method [1]. Then I exfoliate the crystal with simple scotch tape method as shown in Figure 3.1 (a). Few-layer $1T\text{-}TaS_2$ flakes which have almost purple color, with sub-12 nm thicknesses, have been selected for this work [1]. The Figure 3.1 (b) shows some of these few-layer crystals in purple color, while thick flakes of $1T\text{-}TaS_2$ are those in gold color. Figure 3.2 represents the atomic-force microscopy (AFM) image and Figure 3.3 demonstrates the AFM section analysis that verifies the thickness of ~11.9 nm for one of the selected $1T\text{-}TaS_2$ flake in a purple color.
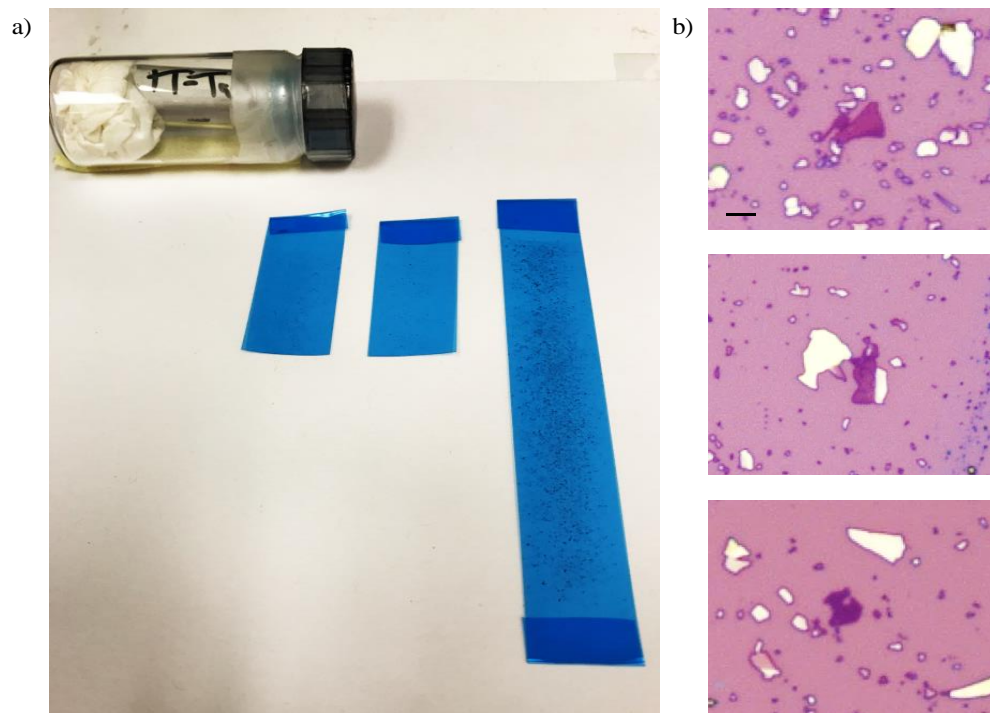
a)

b)

Figure 3.1: a) The image shows mechanical exfoliation of 1T-TaS$_2$ crystals. b) Some few-layered exfoliated 1T-TaS$_2$ crystals. The scale bar represents 3 μm.
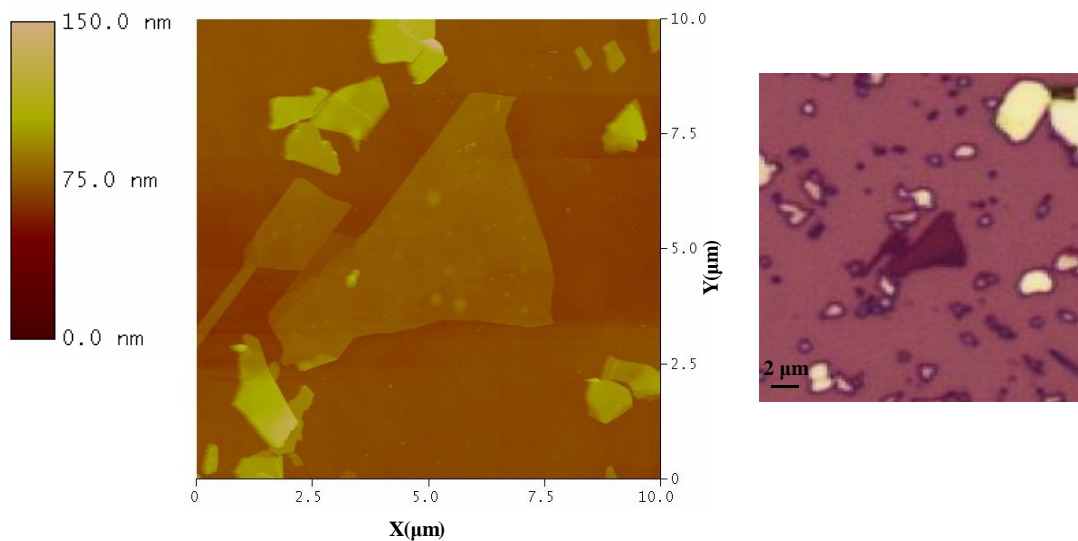
Figure 3.2: The AFM image (left) of selected 1T-TaS$_2$ crystal (right). As it is clear from the AFM image the gold flakes are thick, however the purple triangle-shaped flakes are much thinner.
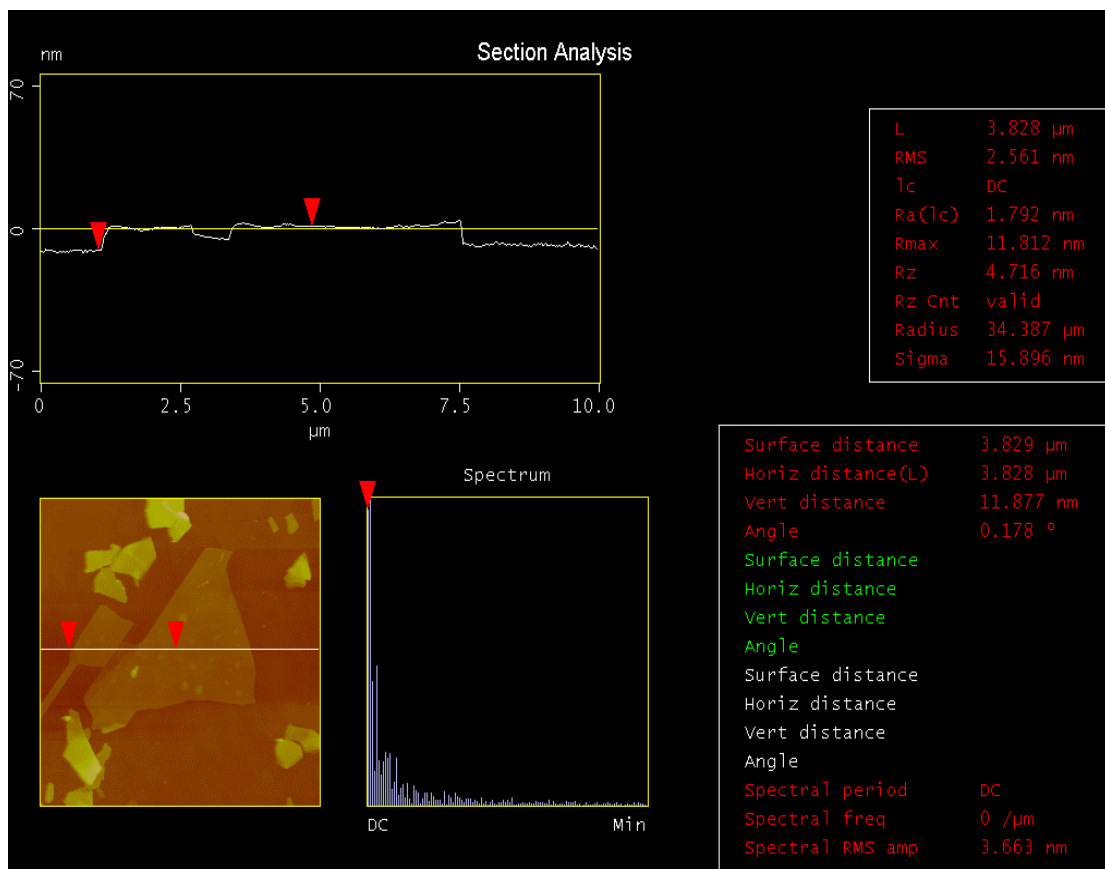
Figure 3.3: The AFM section analysis of the selected purple 1T-TaS$_2$ crystal (Figure 3.2, right). This analysis confirms the thickness of ~11.9 nm for the big triangle-shaped area, which is obtained from the difference in the vertical distances of two red cursors.

3.4 Protecting 1T-TaS$_2$ From Oxidation

Hexagonal boron nitride (h-BN) has a wide band gap which consists of boron and nitrogen atoms in a honeycomb form. It is among the 2D family in which layers of h-BN stick together with van der Waals force. In this work, hexagonal BN has been used as a protecting layer of 1T-TaS$_2$ to avoid oxidation and degradation of a device [1, 3].

Through mechanical exfoliation, thin film of h-BN is isolated which has a blue or greenish color and is transferred on top of the 1T-TaS$_2$ crystal. The transfer method is performed by all-dry viscoelastic stamping. The stamp is a polymer named as polydimethylsiloxane (PDMS) which acts as elastic solid in short timescale however, it will turn into viscous liquid at long flow times. A small piece of PDMS is cut and placed on a glass slide slowly to reduce the formation of wrinkle and bubbles [4]. Hexagonal BN is mechanically exfoliated and deposited on transparent PDMS layer. Figure 3.4 shows exfoliating h-BN and PDMS stamping layer.
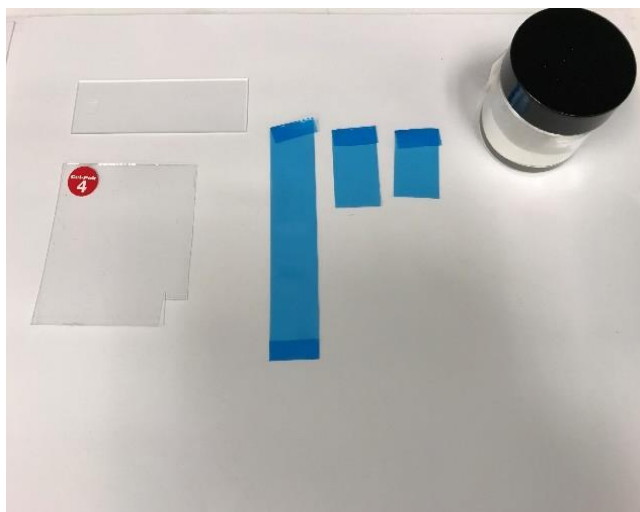

Figure 3.4: Image of PDMS stamping layer in the left and blue tapes that represent mechanically exfoliating white powder of hexagonal boron nitride.

3.4.1 Transfer Process

The dry transfer system, consists of two stages, is placed on the magnetic breadboard. The top stage with the PDMS layer is controlled by a micromanipulator and the sample is located on the bottom stage. The capping step should be performed right away after the exfoliation to avoid 1T-TaS$_2$ oxidation. The Figure 3.5 is representing the transfer system setup.
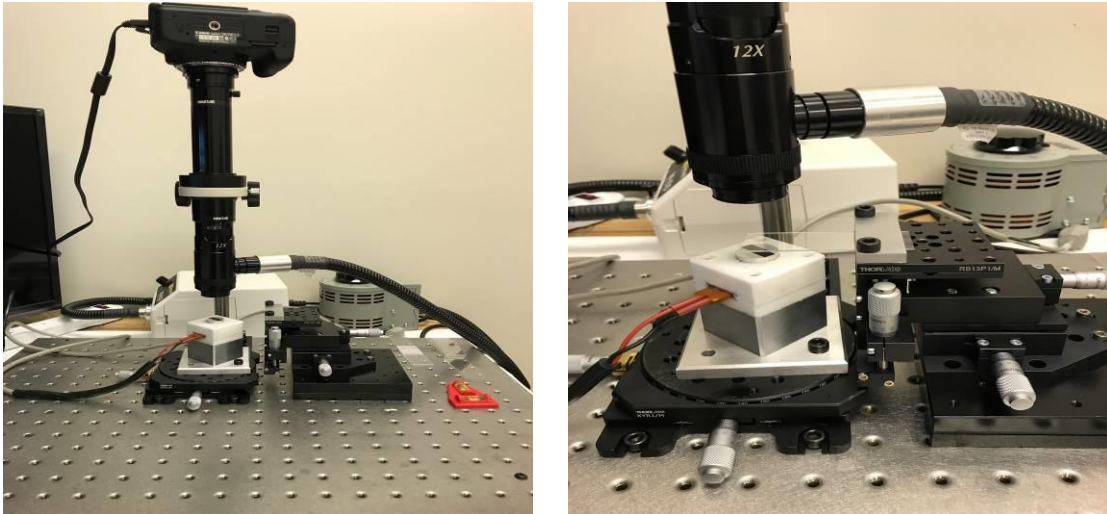
Figure 3.5: The transfer setup with two stages which controlled with micromanipulator, is located on the magnetic breadboard. The magnification and focusing are maintained via zoom lenses.

The 1T-TaS$_2$ flakes, on the SiO$_2$/Si substrate, have been placed on the bottom stage. By bringing it to the field of view of the zoom lens, I try to focus on the bottom layer and on a specific thin flake. Afterwards the PDMS layer which is sticking to the glass slide and carrying the exfoliated h-BN, is clamped to the top stage and roughly positioned on top of the sample. Then I focus on the top layer and on a specific h-BN

flake. After finding the desired flake on the PDMS layer, then focus back on the bottom layer and on the 1T-TaS$_2$ flake. Gradually bring the top layer down, using the micromanipulator, and adjust the stages each time to make sure the top and bottom flakes are aligned on top of each other. By moving the stage, notice when both layers are touching and then keep pressing slowly until the PDMS starts to flow through the surface. When this flow passes the desired flake, then reverse the process and move up the top layer very slowly. During this process, it is necessary to peel of the viscoelastic material gradually for providing a good and accurate transfer [4]. The Figure 3.6 is showing some steps of transferring h-BN on top of 1T-TaS$_2$. The top-left image is 1T-TaS$_2$ flake on SiO$_2$/Si substrate and the second one is h-BN on the top layer (PDMS). As the top stage moves closer, the h-BN flake become more apparent until they touch and the PDMS starts to flow. Then the process is reversed, the top stage is lifted up slowly and the capped 1T-TaS$_2$ can be seen in the final image.

Figure 3.6: Optical images of the steps, while transferring h-BN on 1T-TaS$_2$ crystal. The first image is showing a dark purple flake of 1T-TaS$_2$ and the last image shows the green layer of h-BN covered the 1T-TaS$_2$ crystal. The areas with almost yellow color in the second-row images, show the PDMS layer starting to flow through the substrate. The scale bar represents 39 μm.

3.5 Device Fabrication Steps

Now that 1T-TaS$_2$ crystal have been capped with h-BN, the sample is ready for device fabrication. One of the crucial step in the fabrication process is doing the alignment. Since patterns contain fine structures, accuracy in the location of writing is among the essential factors. After creating the alignment markers, I move to lithography steps for electrodes and pads. Considering the point that the sample has been capped with h-BN, another step would become necessary and that is etching h-BN. This step needs to be followed by metal deposition immediately. Finally, the ready device with 1T-TaS$_2$ channel and h-BN protecting layer will be presented at the last step.

3.5.1 Fabricating Alignment Markers

For creating alignment markers using the electron-beam lithography (EBL), first I need to coat the sample with e-beam resist layer and then continue with electron-beam writing step. Afterwards, deposit metal layers using electron-beam evaporator followed by lift-off process.

3.5.1.1 Spin Coating Resist Layer

In this step, I spin coat the sample with resist, using polymethyl methacrylate (PMMA). The PMMA is a polymeric material, commonly used as a positive resist. When it is exposed to the e-beam, its chemical structure changes and will become more soluble in contact to developer solution. However, in cases which PMMA is highly exposed to

the e-beam it will turn into negative-tone resist. By negative-tone, it means that the exposed areas become crosslinked and polymerized, thus they won't dissolve easily in a developer [5]. For achieving desired thickness of PMMA layer, one should pay attention to the dilution of PMMA and the spinning speed and time. Knowing its dilution, one can choose an appropriate spin speed by checking the curves of films thicknesses versus spin speeds based on the material's datasheet. The PMMA resist formulated in this work is 950PMMA A4. The final spinning speed is set to be 4000 rpm and duration time of 45 seconds. Based on the datasheet curves, this spin speed will provide almost 200 nm film thickness [5]. Then the spin coating is followed by a baking step. The substrate is placed on the hot plate and baked for 5 minutes at 150 °C and will be cooled down afterwards for 1 minute. For creating alignment makers, one layer of PMMA would be sufficient.

3.5.1.2 Designing Alignment Markers

The patterns which are supposed to be written on the sample need to be designed via computer-aided design (CAD) program. The Figure 3.7 shows the alignment markers design file. The area of 100 ×100 µm is enclosed by the markers. The EBL machine interprets the structures which are drawn with dashed lines, as the areas need to be exposed. While figures with solid lines would be behaved as lines to be exposed and not the areas. Alignment markers should be in a way to surround the desired capped-flake for further alignment steps.
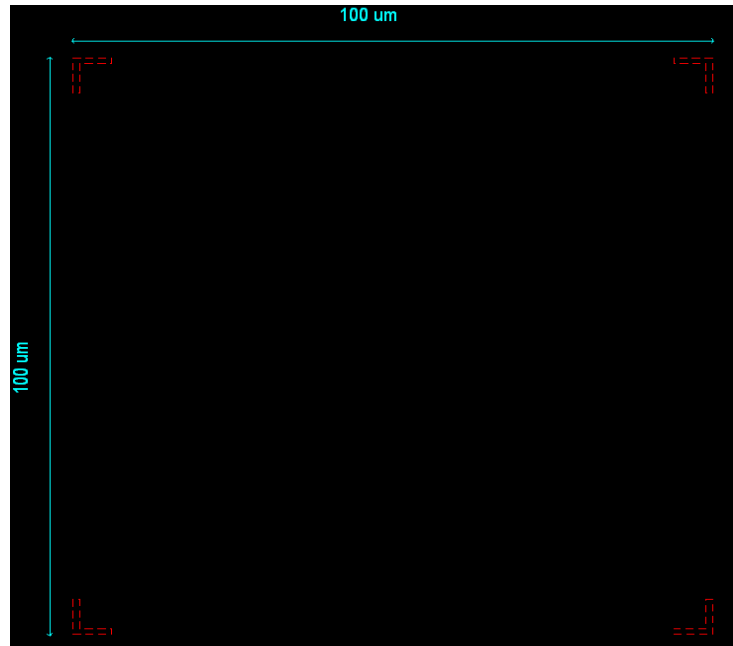
Figure 3.7: Designed CAD file of small alignment markers. The four red L-shaped markers are designed with dashed-lines, which then would be exposed by e-beam lithography. The markers enclosed an area of 100×100 μm.

3.5.1.3 E-Beam Lithography

Electron-beam lithography is a machine using electron-beam to draw patterns on the resist-coated samples. Performing lithography with electron source has the benefit of high diffraction-limited resolution. This will make it favorable when it comes to nanoscale pattern writing. In this EBL approach, the direct writing method is being applied, in which small portion of e-beam is separated and is directly written on resist-coated sample. This method will provide high resolution with no need of mask producing. However, the exposure would be one pixel at a time and this will make it time consuming process.

Figure 3.8: The e-beam lithography system (Zeiss Supra 55) in our clean room facility.

The Figure 3.8 is representing the EBL system (Zeiss Supra 55) in our clean room facility. The direct writing EBL, is constructed of some components that mainly I can name as source of electrons, a set of focusing optics, blanker for turning e-beam on and off, deflection system to move the beam and a sample holder stage [6]. In general, one can say that the EBL is a combination of scanning electron microscopy (SEM) and a system named as nanometer pattern generation system (NPGS) which provides an environment for designing and controlling the writing steps. In the SEM system, electrons are accelerated through the column with the voltage that usually can have a range from 0.5V to 30 kV. There are a set of lenses implemented through the column to

modify the beam diameter and do the focusing. Also, a series of apertures would be placed in the path of the beam which define the size of the hole that e-beam is passing through. In the bottom chamber, the specimen is located which would be brought to appropriate working distance (WD). When the e-beam interacts with the sample there would be some signals generated that need to be detected and processed to form the final image. Both the gun chamber and the specimen one, should be highly vacuumed. The pressure in the specimen chamber would be about 10^{-4} Pa [7].

In the EBL system, the first step is to focus on the substrate using the SEM. I place the prepared, resist-coated sample on a SEM specimen stub which is fixed with carbon tape. The rough position of the capped sample would be found via SEM and using the big alignment markers, previously made with photolithography. Since the surface is being scanned with e-beam, it is important not to increase magnification so high and avoid zooming on the specified crystal as this may damage it. There are some SEM parameters need to be adjusted for desired lithography results. I have set the acceleration voltage to be 20 kV and used 20-micron aperture size for writing the small alignment markers. The WD, the distance between the surface of the specimen and the lower part of the lens, is set to 6 mm to attain a good writing.

One can get a fine and reasonable lithography by becoming an expert in SEM setups and imaging. Therefore, it is crucial to make sure that I have a good and well-focused SEM image before starting writing the patterns. The aperture's centering is also an important factor in SEM setup. There is a "wobble" mode in most of SEMs, in which the focus is altered back and forth, when it is active. If the aperture is poorly centered, the

image will oscillate back and forth when the wobble mode is on. By changing the aperture knobs for X and Y direction, I should reduce this swinging behavior and optimize it by making it blinking rather than oscillating. After aligning the aperture, the wobble mode should be deactivated. Furthermore, another factor that needs special attention is astigmatism which is critical specially in writing fine features. The astigmatism should be minimized in the beam before writing patterns. If it is not adjusted properly then the quality of exposed lines would be different along various orientations. To fix the astigmatism, it would be recommended to focus on some part of a substrate, at least few blocks away from the specified crystal. Then I increase the magnification and change the stigmator knob along X direction and try to optimize it and refocus again. After finding the optimized focus and astigmatism along X, then repeat it for the Y direction [8]. By optimizing wobble and astigmatism the so-called "pen" is almost ready to write on the specimen.

The NPGS software has different menus. One would be DesignCAD which is a commercial CAD program and is specified for designing patterns. Another one is the Run File Editor, which is a menu style program itself, designed for setting the exposure parameters and steps. It has several entities and patterns would be written in the sequence in which the entities are ordered. At this step, for writing the alignment markers, three entities are inserted in sequence. First, it would be "Move Only" command in order to move the beam to the origin of the designed file. Second, can be the "Pattern" entity and the last one "Move Only" entity again, to move the beam to some blocks further away from the written pattern area. The "Pattern" entity gets the name of the designed file as

input and requires few more parameters such as "Magnification", "Center-to-Center" distance, "Line Spacing", "Measured Beam Current", "Dwell" and "Dose" of exposure [8].

"Magnification" in the Run File Editor, refers to the microscope magnification at which the pattern is written. However, in this setting the magnification has limits and its maximum would be in a way to make sure that the pattern is within the field of view [8]. "Center-to-Center" distance is the distance between neighbor exposure points while the beam is writing a line. The "Line Spacing" is the distance between adjacent lines when beam is filling an area [8]. "Measured Beam Current" is the parameter used to calculate exposure time or dose. "Dwell" is the exposure time per point and the "Dose" would be in the form of "Area Dose", "Line Dose" and "Point Dose" with the unit as $\mu C/cm^2$, nC/cm and fC, respectively. For example, the "Area Dose" is calculated in the form [8]:

$$Area\ Dose = \frac{(Beam\ Current) \times (Exposure\ Time)}{(Center-to-Center) \times (Line\ Spacing)} \qquad (3.1)$$

Dose is an important factor that not only depends on the sensitivity of the resists, but also on the beam energy, pattern's line width, pattern's density, etc. Therefore, it would be necessary to make a dose test first and find the optimum dose for pattern elements before writing on the original sample. If the dose is not set properly then one will see underexposed or overexposed areas appearing in the patterns. Sometimes poorly focused beam may result in underexposed areas and the solution to that is fixing the focus, not increasing the dose [8]. The Figure 3.9 is showing some examples of underexposed (left) and overexposed (right) patterns.
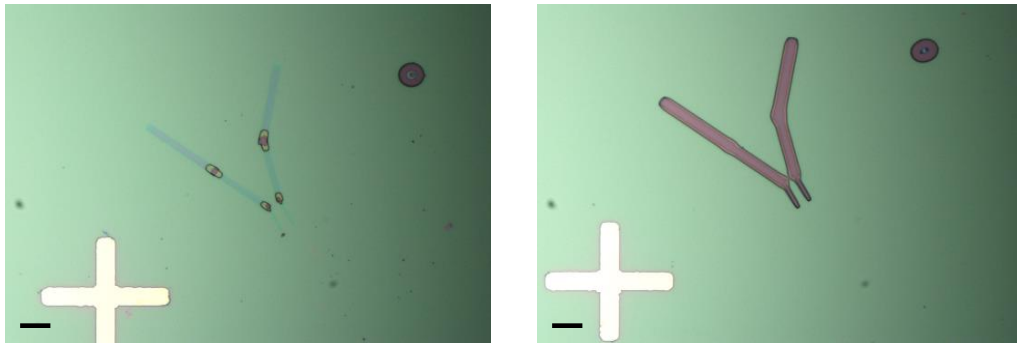
Figure 3.9: Optical images of underexposed (left) pattern and overexposed (right) pattern. The scale bars indicate 5 μm.

As these crucial parameters are set, the Run File Editor is ready. Adjust the working distance to 6 mm, which is suitable distance for writing purposes, and then run the program.

3.5.1.4 Developing PMMA Resist

Since I am using PMMA as a positive-tone resist, after the e-beam lithography the exposed areas become more soluble in a specific solution called as, developer. Here, I have used methyl isobutyl ketone (MIBK) as the developer. MIBK is an organic compound and strong solvent for PMMA. It would be diluted with IPA to make it less strong. Therefore, the 1:3 mixture of MIBK/IPA is applied for 70 seconds at room temperature and the sample is rinsed right after with IPA for almost 20 seconds and dried with blow of nitrogen gas [8, 9].

3.5.1.5 Metal Deposition

Now the beam-exposed-areas are open and ready for the metals to be deposited. The deposition has been done through electron-beam evaporator. Figure 3.10 is showing the e-beam evaporator (Temescal BJD) instrument. E-beam evaporation is among the most common method of physical vapor deposition of metals. In this method, several sources of materials such as titanium, nickel, aluminum, gold, etc. are located inside a chamber. The chamber needs to be evacuated and when it gets down to the pressure of 5×10^{-6} torr and under, I will start to power up and heat up the selected source material with a focused electron-beam. When the material is heated above its melting point the evaporation occurs. Then the shutter is opened, which previously was covering the source material, and the evaporated atoms travel in straight-line pathways and at high velocity [10]. Therefore, the evaporated metal atoms would be deposited on the surface of the sample. After reaching the specified thickness, I close the shutter to stop deposition, then powered the system down and turn off the gun. In this work, I deposited 5 nm titanium and 60 nm of gold for small alignment markers. The titanium acts as an adhesion layer, since without it the gold would easily fall from the surface.

Figure 3.10: The e-beam evaporator (Temescal BJD) instrument in our clean room facility.

3.5.1.6 Lift-Off Process

After metal deposition step, the whole surface of sample is covered with layers of metal. In order to peel off metal layers from areas on top of the PMMA, another step is required known as lift-off. However, to be able to evaluate the lithography and realize if the exposure has gone well or not, the patterns should be checked under microscope before continuing with the lift-off step. Once nice patterns are observed on the areas with developed resists, it would be a time to do the lift-off. While I have PMMA as my resist, a usual method of this process would be soaking the sample in the acetone. The acetone

attacks the PMMA resist layers and dissolve them [8]. As a result of that, the evaporated metal layers are peeled off except for pattern areas, since on those areas they were covering developed resist-surfaces. For thick layers of PMMA the lift-off would be easy and the sample can be left in acetone at room temperature for almost 20 minutes until wrinkles appear in the metal layers. By gently squirting acetone with pipette onto the surface of the sample, the metal would be detached. Then rinse the sample with IPA and blow nitrogen to dry it. The Figure 3.11 presenting some capped crystals of 1T-TaS$_2$ with small alignment markers. Based on the color contrast from optical microscopy images and the AFM results, the purple 1T-TaS$_2$ crystals thicknesses are approximated to be under 12 nm [1].
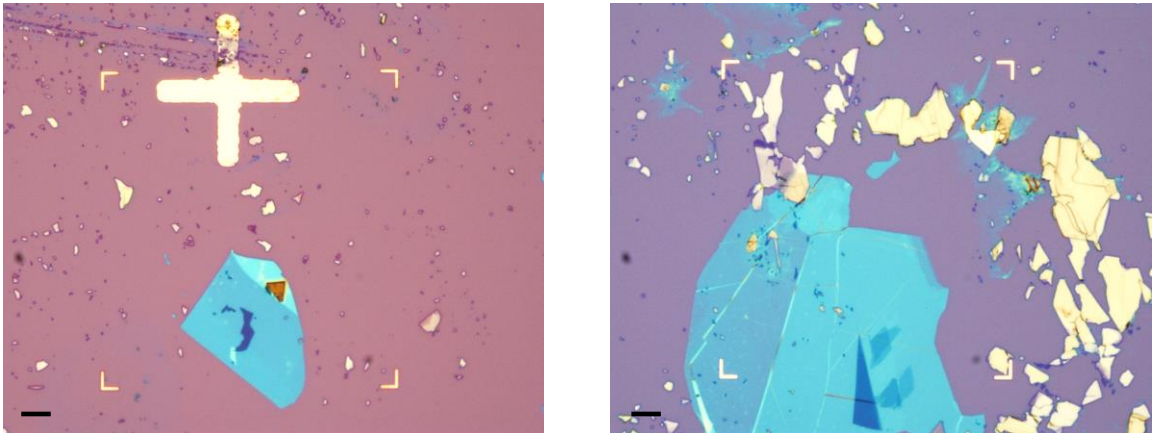

Figure 3.11: Optical images of h-BN-capped crystals of 1T-TaS$_2$ with written alignment maker patterns. 1T-TaS$_2$ thickness is less than 12 nm. The scale bar represents 9 μm.

3.5.2 Fabricating Electrodes and Pads

After creating the alignment markers, I move to the step of making device and fabricate electrodes and pads for the h-BN-capped crystal of 1T-TaS$_2$. I repeat the steps of spin coating, designing, lithography, developing, metal deposition and lift-off. However, this time another extra step is appeared after developing resist, which is dry etching to open a window in h-BN layer. Therefore, I can deposit metal in contact to 1T-TaS$_2$ crystal and have it as the channel material.

First, I spin coat the sample with two layers of PMMA. For each layer with the same recipe as 4000 rpm spinning speed and total time of 45 seconds. Then bake the first layer at 150 °C for 5 minutes. Now spin coat the second layer with the same recipe and do the baking afterwards at 150 °C for 5 minutes. Let the sample cool down for almost 1 minutes. At this point, the sample is coated with 2 layers of PMMA and with this recipe, I have achieved almost 400 nm thickness of resist layers. For fabricating electrodes and pads I have considered thicker resist layers since in the further steps, thicker metal layers are going to be deposited and there would be a need of straightforward lift-off process.

3.5.2.1 Designing Electrodes and Pads

To make sure that electrodes and pads would be written in right position and are aligned on top of the crystal, the alignment step is crucial. Figure 3.12 shows the alignment markers' design file. In general, each alignment pattern would consist of two parts. One is alignment pattern "window" and the other is "overlay". "Window" is the polygon with the dashed-lines, which EBL interprets it as the area to be exposed.

"Overlay" is the polygon with solid line that is defining the shape and position of the previously written alignment markers. "Window" will open an area in which I need to align the "overlay" with the registered alignment markers. Each pair of "window" and "overlay" should be assigned to be in a different drawing layer [8]. Figure 3.13 represents the electrodes' and pads' design files for the device. Electrodes are fine parts, while the pads would be the large features. Electrodes are drawn in red color, while pads are in blue. Layers with specified colors in the CAD file may be later assigned to a unique dwell and dose parameters in the run file. It is important to have one origin for all layers of the design file. Also in the design file, a green dot can be seen and that is called "Dump" point. In our EBL system, the beam blanker is set to zero and as a result of that, there is no blanker to set the beam on and off. Therefore, it is required to set a point in the design file as a dump location. This means that when the gun is not writing, it will go to the dump location. In the case that the blanker is off and I don't have this dump point, there might be some unwanted exposure in the pattern due to the traces of the beam [8].

3.5.2.2 Lithography for Electrodes and Pads

The process is continued with the EBL machine for doing lithography. Two Run File Editors have been created. One for running the electrodes layer and the other one consists of running steps for pads layer. The Run File Editor for electrodes starts with the "Alignment" entity. I set the alignment mode to be "Manual" which means the alignment overlay features and the registered alignment markers need to be matched and located by user. For each layer of alignment, one would be prompted with parameters like "Dwell",
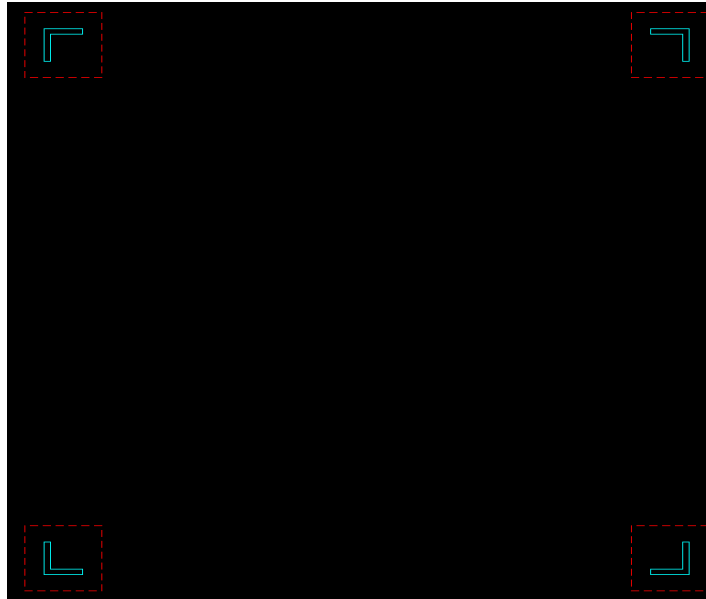
Figure 3.12: Alignment's design file. The dashed-line-square is the alignment "window", while the blue L-shape marker is the "overlay".
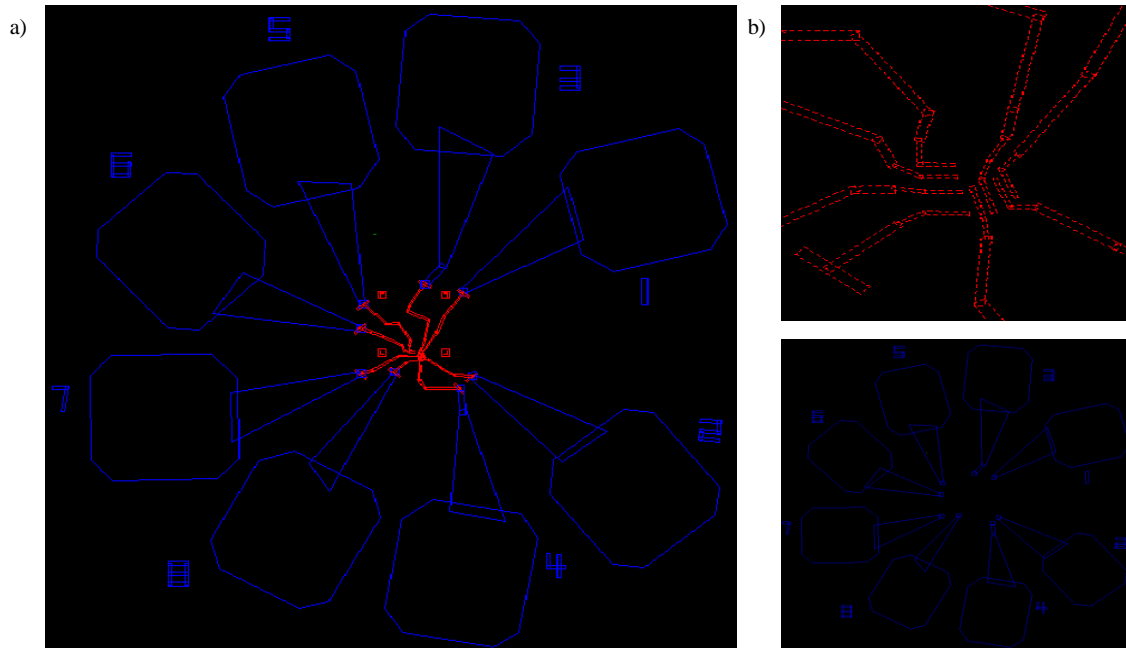

Figure 3.13: The design files of electrodes and pads. a) The integrated electrodes and pads layer. b) The top is a closer look on the designed electrode layer and the bottom is their corresponding pads.

"Magnification" and "Measured Beam Current". Within a group of windows, changing one parameter will change that one for other windows (layers) as well [8]. After aligning step, the next entity would be the "Pattern" that will get electrodes' design file as an input. For this design, I have set the "Magnification" to 1000, "Area Dose" to be 570 $\mu C/cm^2$, "Measured Beam Current" to be 100 pA, "Center-to-Center" and "Line Spacing" almost 20 Å (Limits may change due to the design file and magnification). "Dwell" parameter would be calculated automatically from Equation 3.1. It is worth saying that the dose values required for exposing fine parts are higher than that of for lager features such as pads.

The Run File Editor for the pads layer begin with "Pattern" entity that will take the pads' design file as an input. The parameters for the pads layer are set as 480 $\mu C/cm^2$ for "Area Dose", "Measured Beam Current" as 2400 pA and "Center-to-Center" and "Line Spacing" almost 37 Å. The upper limit of magnification would be set due to limitations of the design file. The "Pattern" entity is then followed by a "Move Only" entity. So, the beam is moved by almost 400 μm along (positive or negative) X and Y directions to get far from the writing areas. When the Run File Editors are ready, the first step before doing the lithography would be optimizing SEM parameters. Try to minimize wobbling and astigmatism and make sure the beam is well focused at WD of 6 mm. I have set the accelerating voltage to 20 kV and the aperture size to 20 μm for writing the electrodes. Then with low magnification, I move to the area with those small alignment markers and quickly position the beam on the center of area (origin) which is enclosed by alignment markers. The electrodes' Run File Editor would be processed then. After it is

completed and before starting the pads' run file, the aperture size is changed from 20 μm to 120 μm because writing the large features like pads with 20-micorn aperture, would take a very long time. Afterwards the pads' run file is processed and the writing is completed. The Figure 3.14 shows the optical images of patterns after e-beam lithography and before developing step. In the next step, the sample is developed in MIBK/IPA with 1:3 ratio at room temperature and for 70 seconds. Rinse afterwards with IPA for almost 20 seconds and blow nitrogen to dry it.
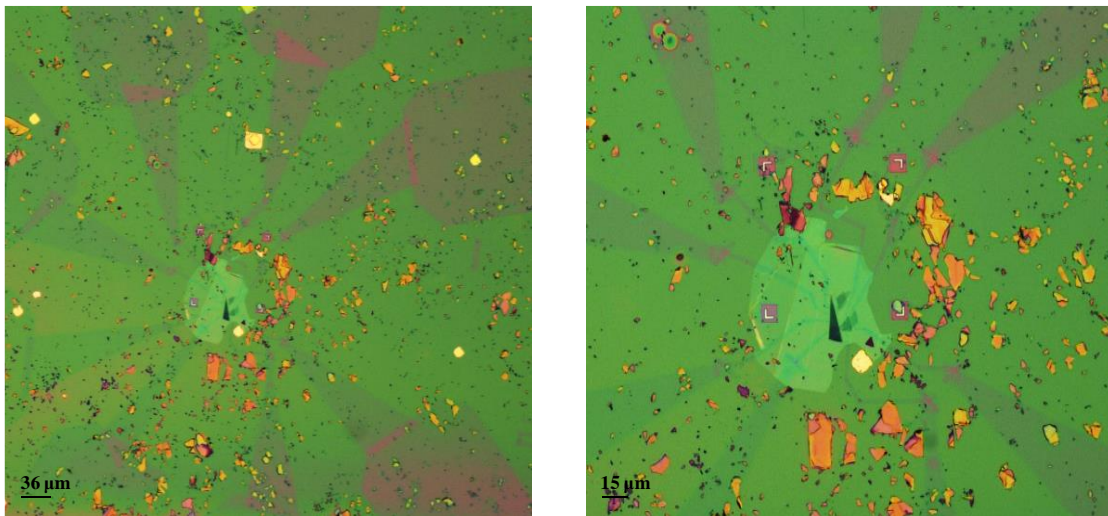

Figure 3.14: Optical images of patterns, after e-beam lithography and before developing. The exposed areas are in light purple color.

3.5.2.3 Etching h-BN

After developing, the exposed areas are open, while rest of them are coated with resists. At this step, the h-BN layers in the written electrodes areas should be etched, thus contacts with the 1T-TaS$_2$ crystals can be made. To maintain this, I have used inductively coupled plasma (ICP) etching system which is a dry etch method. Figure 3.15 demonstrates our ICP etch system (Oxford Instruments Plasmalab System 100).

Figure 3.15: The ICP etch system (Oxford Instruments Plasmalab System 100) located in our clean rom facility.

ICP technology uses an inductive element, which is typically in a helical or spiral form, for coupling the energy from a radio frequency (RF) power source to an ionized

gas. The RF current flows in the inductive element and produces an RF magnetic flux, which would vary by time since it is adjacent to the discharge region. This time, varying magnetic flux density induces an electric field that maintain the plasma [11]. The ion energies would be controlled by defining an RF power and plasma drifts toward the substrate. Etch gases need to be selected and then it will move through the chamber. The sample is placed on an anodized aluminum wafer carrier, which is cooled down by helium gas [12].

For blue or almost greenish color of h-BN, I have used sulfur hexafluoride (SF_6) as the etching gas. The rest of etching parameters in ICP system are set as follows: 40 sccm SF_6 gas flow, 20 mTorr pressure and 50 watts RF power. The etching time is first set to 8 seconds. After finishing this etch step, I will take out the sample and quickly observe under microscope to make sure there is no h-BN remaining on the developed-electrodes areas. After that, put the sample back in the ICP chamber and repeat the etching step for just 2 seconds. As this step is finished, it needs to be followed by metal deposition immediately. By etching h-BN layer the $1T$-TaS_2 crystal at the electrodes areas become exposed to the air. Therefore, it is crucial to deposit metal right after and minimize the time that sample is exposed to the air. When the etching step is completed, the sample would be placed in the e-beam evaporator chamber and pumped down quickly. I deposit 10 nm titanium as adhesion layers and then deposit 90 nm gold layers. Figure 3.16 is representing a device after metal deposition and before the lift-off step.
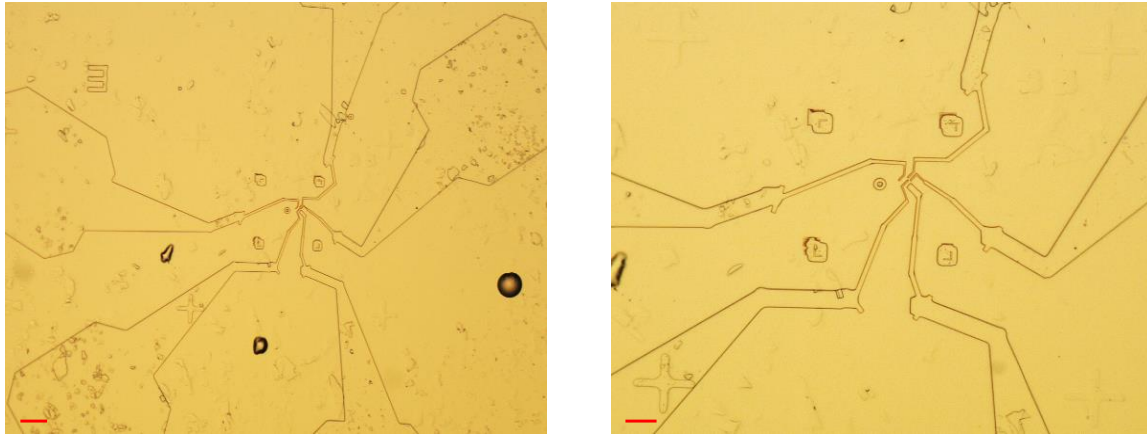
Figure 3.16: Optical images of a h-BN-capped 1T-TaS$_2$ device before lift-off process. The scale bars represent 33 μm and 21 μm for left and right images, respectively.
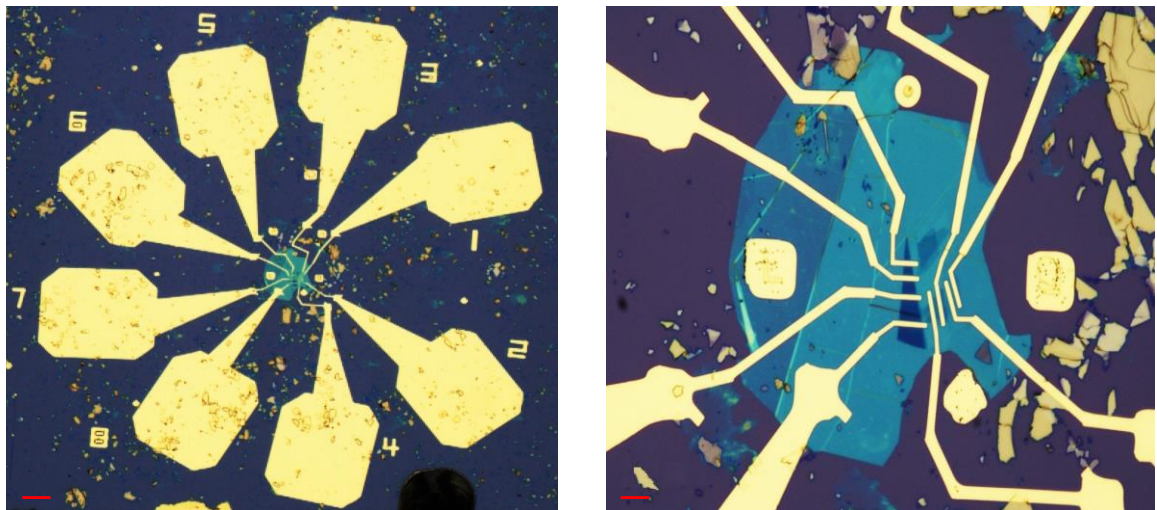

Figure 3.17: Optical images of 1T-TaS$_2$ devices with channels thicknesses of <12 nm, capped with h-BN protecting layer after lift-off process. Devices implemented at different channels lengths. Scale bars represent 50 μm and 5 μm for left and right images, respectively.

As the deposition is completed and the patterns look good, I may proceed to the lift-off process. The sample is soaked in the acetone at room temperature and left there for almost 20 minutes or until I will see wrinkles appearing in the surface of the sample. As the acetone attacks the PMMA layers and dissolve them, the metal on top of the resist layers starts to detach. Gently squirting acetone on the surface of substrate to complete peeling off the metal layers. Then rinse the sample with IPA and dry it with blow of nitrogen gas. Figure 3.17 shows 1T-TaS$_2$ devices with various channel lengths and thicknesses of less than 12 nm, capped with h-BN protecting layer.

References:

[1] G. Liu, B. Debnath, T. R. Pope, T. T. Salguero, R. K. Lake and A. A. Balandin, *Nature Nanotechnology*, 11, 845-851 (2016).

[2] W. Fu, Y. Chen, J. Lin, X. Wang, Q. Zeng, J. Zhou, L. Zheng, H. Wang, Y. He, H. He, Q. Fu, K. Suenaga, T. Yu and Z. Liu, *Chem. Mater.*, 28, 7613-7618 (2016).

[3] L. Song, L. Ci, H. Lu, P. B. Sorokin, C. Jin, J. Ni, A. G. Kvashnin, D. G. Kvashnin, J. Lou, B. I. Yakobson and P. M. Ajayan, *Nano Letter*, 10 (8), 3209-3215 (2010).

[4] A. Castellanos-Gomez, M. Buscema, R. Molenaar, V. Singh, L. Janssen, H. S. J. van der Zant and G. A. Steele, *2D Materials*,1 (1) (2014).

[5] MicroChem Corp., PMMA datasheet (2001).

[6] A. Tseng, K. Chen, C. Chen, K. Ma, *IEEE Transaction on Electronic Packaging Manufacturing*, 26 (2), 141-149 (2003).

[7] P. Hawkes, J. Spence, *Science of Microscopy*, 1, Springer (2007).

[8] J. C. Nabity, *Nanometer Pattern Generation System*, JC Nabity Lithography Systems (2006).

[9] M. J. Rooks, E. Kratschmer, R. Viswanathan, J. Katine, R. E. Fontana Jr. and S. A. MacDonald, *J. Vac. Sci. Technol. B*, 20 (6), 2937-2941 (2002).

[10] G. May, S. Sze, *Fundamentals of Semiconductor Fabrication*, John Wiley & Sons, Inc. (2004).

[11] J. Hopwood, *Plasma Sources Sci. Technol.*, 1 (2), 109-116 (1992).

[12] R. Shul, G. McClellan, S. Casalnuovo, D. Rieger, S. Pearton, C. Constantine, C. Barratt, R. Karlicek, C. Tran, M. Schurman, *Appl. Phys. Lett.*, 69 (8), 1119-1121 (1996).

Chapter 4

Characterizations

4.1 Introduction

In this chapter, I characterize the h-BN-capped 1T-TaS$_2$ devices by maintaining current-voltage (I-V) characterization and low-frequency noise measurements. The octahedral (1T) polytype of 1T-TaS$_2$ crystal is among transition metal dichalcogenides family members, which presents rich CDW phase transitions. At high temperatures above 545 K it has a metallic phase, but when it comes down to 545 K it would enter an incommensurate CDW phase (ICCDW) until 350 K. At 350 K 1T-TaS$_2$ undergoes a transition to nearly commensurate CDW phase (NCCDW) and at 180 K experiences a transition to a commensurate CDW (CCDW). However, when the thickness of 1T-TaS$_2$ film is less than 10 nm, the transition temperature at 180 K due to commensurate to nearly commensurate phase, would be vanished while the one at 350 K remains [1, 2]. There are several parameters that can affect and modify the CDW phase transitions such as doping, environmental pressure, film thickness and applied electric field [1, 3]. In this chapter, I have represented how the electrical conductivity changes as 1T-TaS$_2$ undergoes a nearly commensurate to incommensurate CDW phase transition at room temperature.

Then I have confirmed CDW phase transition with temperature-dependent resistance measurements of the device and witnessed the nonlinearity in the resistance after passing phase transition. Afterwards the low-frequency noise measurements have been discussed, which are implemented on the 1T-TaS$_2$ h-BN-capped device.

4.2 Electrical Characterizations of 1T-TaS$_2$

The model of 1T-TaS$_2$ device capped with h-BN is demonstrated in Figure 4.1. A few-layer tantalum disulfide (light blue Ta atoms and yellow S, in octahedral arrangement) is creating the channel. The channel is preserved with hexagonal BN (dark blue N and the pink B atoms) and located on SiO$_2$/Si substrate with Ti/Au contacts. First, I describe the setup for measuring the I-V characteristics of the device operating at room temperature (RT). Afterwards I discuss the characteristics and continue with the temperature-dependent resistance.

In order to measure the current-voltage characteristics I have used semiconductor device analyzer (Agilent Technologies B1500A) integrated with a probe station. Figure 4.2 demonstrates our probe station. The device is placed inside the chamber and the chamber is vacuumed. Then the probes are laid over the pads gently and could be controlled through the optical microscope. For the device of Figure 3.17, represented in previous chapter, I have selected the device between pads 6 and 7 and have laid the probes over them. Because of the symmetry, the order of contacts doesn't matter and one electrode is to be grounded, while the other changes over the voltage ranges. The channel
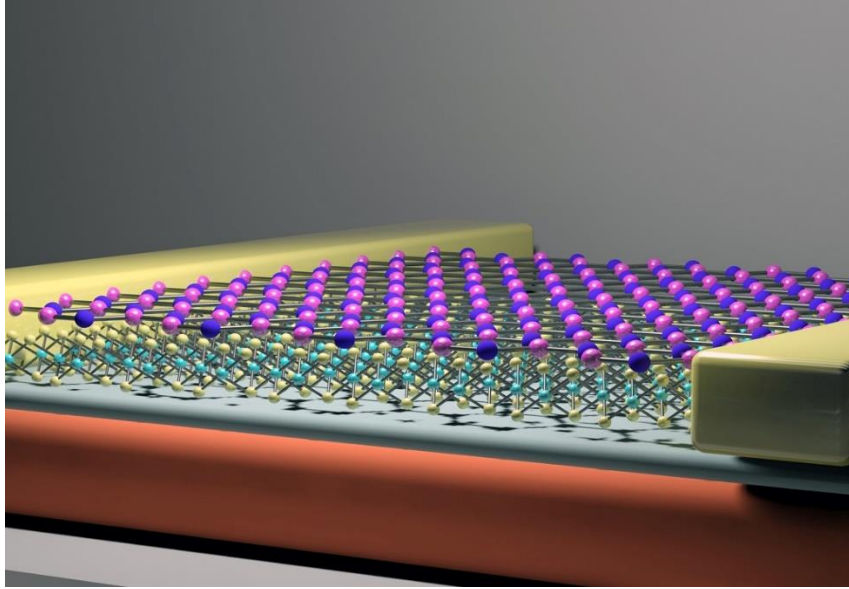
Figure 4.1: The model of 1T-TaS2 device, capped with h-BN located on SiO$_2$/Si substrate and with Ti/Au contacts. Light blue, yellow, dark blue and pink represent Ta, S, N, B atoms, respectively.
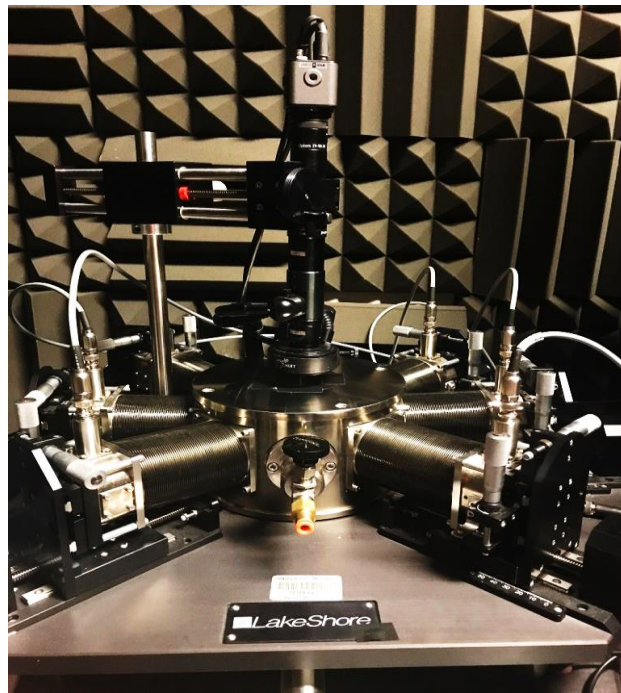

Figure 4.2: The probe station with six probes, integrated with optical microscope.

is 1T-TaS$_2$ material which is preserved by a h-BN protecting layer. The probes are then connected to a set of coaxial cables which would be efficient transmission lines. The cables will be directed to the source/measure unit (SMU) channels, designed at the back of the semiconductor device analyzer. The semiconductor device analyzer is an instrument for testing the performance of devices through current-voltage, capacitance measurements or capacitance-time or frequency measurements. This instrument has a high resolution of measuring I-V down to femto amperes (fA) current. Another interesting point in this equipment is implementing a measuring module, named as SMU, which provides both current/voltage sources and current/voltage meters in one single unit. Therefore, one can get higher accuracy and resolution as a result of close source and measuring circuitry [4].

As the probes are connected to two SMU channels, I set one of them to be ground and change the voltage of other probe in a small step size. At the room temperature, the voltage is gradually increased until I see an abrupt change in the current passing through the channel and afterward swept the voltage all the way back. Figure 4.3 is illustrating the I-V characteristics of 1T-TaS$_2$ device with channel length of about 4 μm and ~2.5 μm width. Due to the applied electric field the CDW phase transition is triggered. Since the device is operating at the room temperature (~295 K), I may claim that before threshold voltage the 1T-TaS$_2$ resides in NCCDW state [1, 2]. While after the sudden jump in the current, it would be electrically driven into the ICCDW. Also, the reason behind this abrupt change in the current level could be the loss of insulating states in some of the CDW domains, while the crystal still remains in the NCCDW state [1]. By extracting the

resistance from the slope of the I-V curve, one may realize that the resistance of the device starts from ~ 3.03 kΩ and by increasing voltage the resistance decreases gradually until passing the threshold voltage, which a sudden increase in the slope (lower resistance) is obtained. The threshold voltage depends on the temperature and as the temperature increases to the ones close the nearly commensurate to incommensurate CDW phase transition, the threshold switching becomes less apparent. By the time, it reaches the NCCDW-ICCDW phase transition temperature, the device will enter the incommensurate CDW phase and will follow a linear I-V curve [1]. From the Figure 4.3, it can be observed that below the threshold voltage, the characteristic is not following a complete linear trend. In the regions, far from the threshold voltage I have almost linear behavior, however when it almost gets close to the switching region, the characteristic represents some exponential dependency [1]. It is worth mentioning that, through the voltage sweep I realized that the triggering voltages in the increase and decrease cycle do not overlap and display a hysteresis behavior, called as hysteresis "window" [1]. A threshold voltage in the way of increasing steps is named as V_{UT} (Up-Threshold Voltage) and the one in the way of decreasing is named as V_{DT} (Down-Threshed Voltage). As can be seen from the Figure 4.3, V_{DT} is taking place at lower voltage value compare to the V_{UT}.
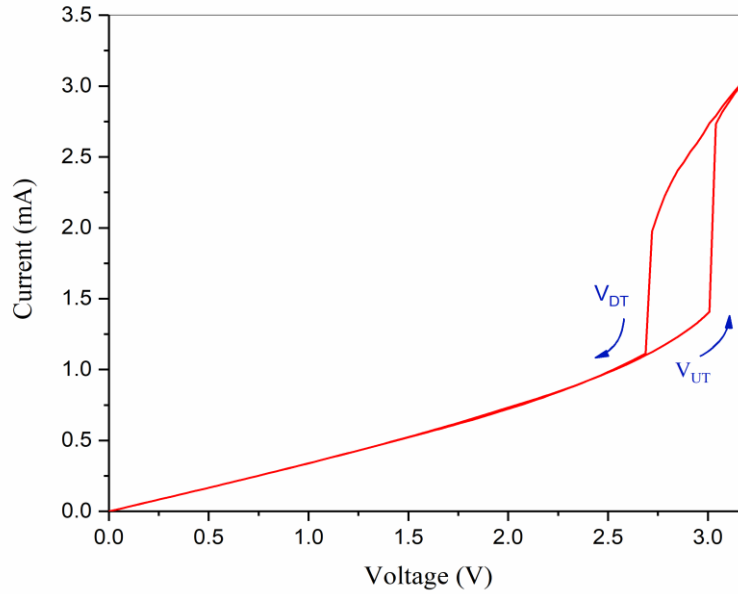
Figure 4.3: The plot of current-voltage characteristics of 1T-TaS$_2$ device with <12 nm channel thickness and ~4 μm channel length and ~2.5 μm width, capped with h-BN, at room temperature. As the voltage increases, there is an abrupt jump in the current value, due to the triggering of ICCDW phase. V_{UT} refers to the threshold voltage in the voltage-increasing cycle, while V_{DT} indicates the threshold voltage in the decreasing cycle. The hysteresis can be observed, as V_{UT} and V_{DT} do not overlap.
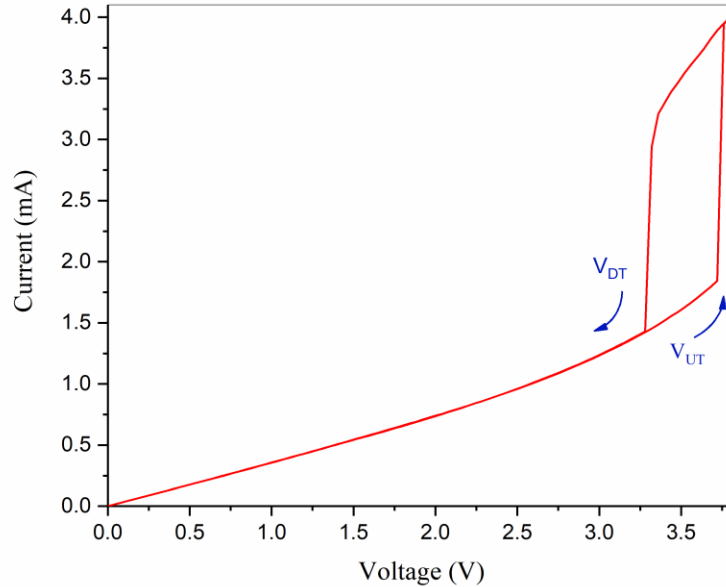

Figure 4.4: The I-V characteristic of 1T-TaS$_2$ h-BN-capped device, with ~6 μm channel length, ~3.5 μm width and <12 nm thickness is plotted at room temperature. As it is clear from the figure, the threshold voltages occur at higher voltage values compare to the previous device with smaller channel area size.

60

Furthermore, the I-V characteristics of 1T-TaS$_2$ device with pads 7 and 8 is measured. The channel length in this device is about 6 μm and ~3.5 μm width and with almost the same thickness of tantalum disulfide as the previous one. Figure 4.4 is showing its I-V characteristics. In this measurement, the current compliance is set at 4 mA to avoid burning of the device. Therefore, it is clear that the current is clamped at 4 mA. I have noticed that as the area size of the device increases, the threshold voltage shifts toward higher values. This means that as the size of channel area increases, it requires higher electric field to switch between nearly commensurate and incommensurate CDW phase, at the same temperature (here, room temperature).

4.2.1 Temperature-Dependent Measurements

I have performed temperature-dependent resistance measurements for the 1T-TaS$_2$ device with 4 μm channel length and <12 nm thickness. The temperature range is from 290 K to 370 K and the nearly commensurate to incommensurate CDW phase transition can be observed [1]. In order to implement the temperature-dependent measurements, the vacuumed chamber which contains the device is cooled down with liquid nitrogen. Then the temperature is controlled with a heater (Lake Shore 336 temperature controller). Although, in this experiment the measured temperature is mostly above the room temperature, to better control its swing, the presence of liquid nitrogen is required. I started measuring the 1T-TaS$_2$ device's resistance from 290 K temperature up to 370 K with the step of 5 K and at the voltage of 600 mV over the device. By observing the Figure 4.3 at voltages around 600 mV at RT, the I-V is still showing linear behavior.

During the measurements, I have kept voltage around the selected value of 600 mV and measure resistance as temperature varies. Figure 4.5 represents temperature-dependent resistance measurements. At 290 K, the resistance is around 3.2 kΩ and as the temperature increases till 360 K, the resistance decreases almost monotonically. Then at temperatures around 365 K there would be an abrupt change in the resistance that falls by almost ~850 Ω. The nonlinearity in the resistance happens at 365 K and it may be suggested to be an indication of NCCDW to ICCDW phase transition. Based on the previous reports on the CDW phase transition temperatures of 1T-TaS$_2$, NCCDW to ICCDW phase transition occurs at temperature around ~350 k [1, 2]. However, the phase transition temperature could be affected (shifted or disappeared) as a result of specific thicknesses. In this case, the effect of channel thickness on the shift of NCCDW-ICCDW phase transition at 365 K may be suggested as one of the possible factor [2].

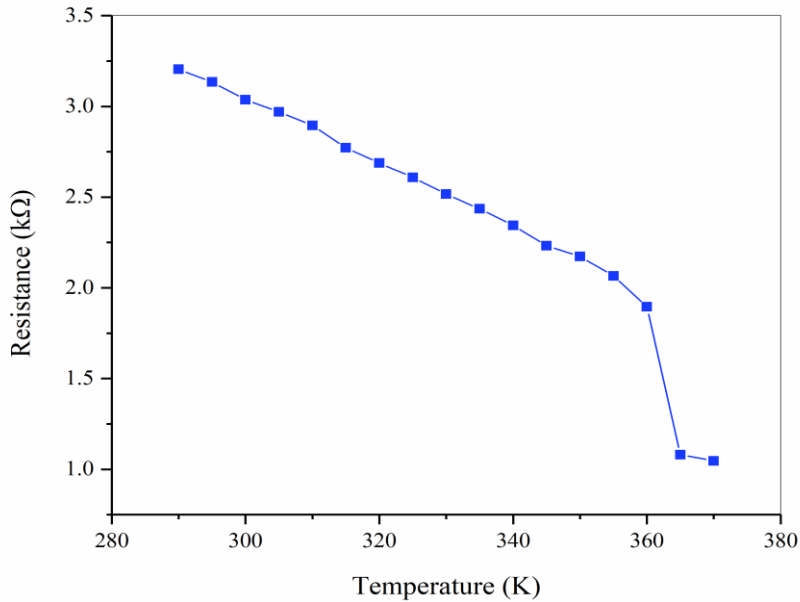**Figure 4.5**: The plot of temperature-dependent measurements for 1T-TaS$_2$ device with 4 μm channel length, ~2.5 μm width and thickness of <12 nm. The nearly commensurate to incommensurate CDW phase transition happens at almost 365 K in this device.

4.3 Introduction to Electronic Noise

The electronic noise, random fluctuations of electrical signal, has been a research topic for a long time. Lots of efforts have been made to optimize devices for reduced noise, however in some cases noises are unavoidable [5, 6]. Electronic noise can be divided into four categories as: (1) thermal noise, (2) shot noise, (3) generation-recombination noise, (4) flicker or $1/f$ noise (f is the frequency) [6]. They are generated from different physical phenomena. However, the origin of $1/f$ noise is still quite ambiguous and has brought many controversial arguments that whether it is the result of generation-recombination mechanism between conduction bands and traps states or due to some fluctuations in the lattice scattering [5]. I briefly describe different types of noise and then move to the low-frequency noise measurements of 1T-TaS$_2$ device and observe their behaviors at different temperatures.

Theorems describing the behavior of fluctuating variable over time, maintaining relations identifying autocorrelation functions and power spectral density for the noise. Autocorrelation function is a useful tool in providing a picture of the average time-dependence of the fluctuating variable. Considering time interval of repetition of a signal T long enough and expanding that randomly varying signal as a Fourier series, the power spectral density can be achieved which represents signals power distribution over frequency [7]. The power spectral density is represented with S_x, in which subscript x determines a variable such as voltage or current.

Thermal noise is a fluctuation of electric charges as a result of thermal motions and it would be expressed as follows [5]:

$$S_I = 4K_BTG \tag{4.1}$$

Where, S_I is spectral density for current, K_B is Boltzmann constant, T is temperature and G is a conductance.

Shot noise can be introduced as a result of grainy structure of electricity, considering each electron leaving the cathode as an independent current contributor. This would lead to electrical fluctuations with the spectral density as follows [7]:

$$S_I = 2q < I > \tag{4.2}$$

Where, q is a charge and $< I >$ is the average value of electric current. Both thermal noise and shot noise are named as white noise, since their spectral densities do not depend on the frequencies [6].

Generation-recombination noise would be due to the trap states forming in a semiconductor device. Because of the exchanging of electrons between trap states and conductions bands or valence bands, the number of free electrons would vary. This may lead to fluctuations that correspond to the following spectral density [5]:

$$S_I(f) = \frac{S_\circ}{[1 + (2\pi f\tau)^2]} \tag{4.3}$$

Where, f is the frequency, $S_\circ$ is a frequency-independent term perceived at frequency less than $(2\pi\tau)^{-1}$. Also, τ is a time constant due to the trapping states [6].

Knowing these intrinsic noises, it needs to be pointed out that the origination of $1/f$ noise is a quite different scenario. It could be generated as a result of fluctuations in number of charge carriers or mobility or both of them [6].

4.4 Low-Frequency Noise Setup and Measurements

Flicker or 1/f noise would happen in contacts, resistors, films and almost in all semiconductor devices [5]. The fluctuations in the conductance of my device (in its ohmic range) can be measured by conducting constant current and read the fluctuations in voltage or keeping the dropping voltage over the sample constant and then measure the fluctuations in current. As the relation below is valid for their spectral densities:

$$\frac{S_I(f)}{I^2} = \frac{S_V(f)}{V^2} \tag{4.4}$$

Where, I is the current passing through the sample and V is the voltage across the resistive sample [5].

In this work, I have implemented low-frequency noise measurements for 1T-TaS$_2$ device (capped with h-BN) with channel length of 4 μm and ~2.5 μm width, from the range of 1 Hz to 100 kHz and for temperature range from 290 K to 370 K. The measurements have been performed in two-electrodes arrangement, since the device has shown low contact resistances and it can be assumed, in a good approximation, that the most fluctuations in the conductance are coming from the sample (resistive tantalum disulfide channel) [1, 5]. In this configuration, I have applied a constant voltage, about 600 mV, to the device and measured fluctuations in the current passing through it. It is worth mentioning that the voltage source supplying the circuit is a 6 V battery (PS-640 Lead Acid Battery) to maintain a noiseless system as much as possible. The device is located inside the vacuumed chamber and two probes are laid over the Ti/Au pads. The probes are then connected to a resistive circuit via coaxial cables, where the resistive

circuit is connected to a voltage supply, voltmeters and spectrum analyzer. Figure 4.6

demonstrates the setup of the measurements and Figure 4.7 shows the schematic of the

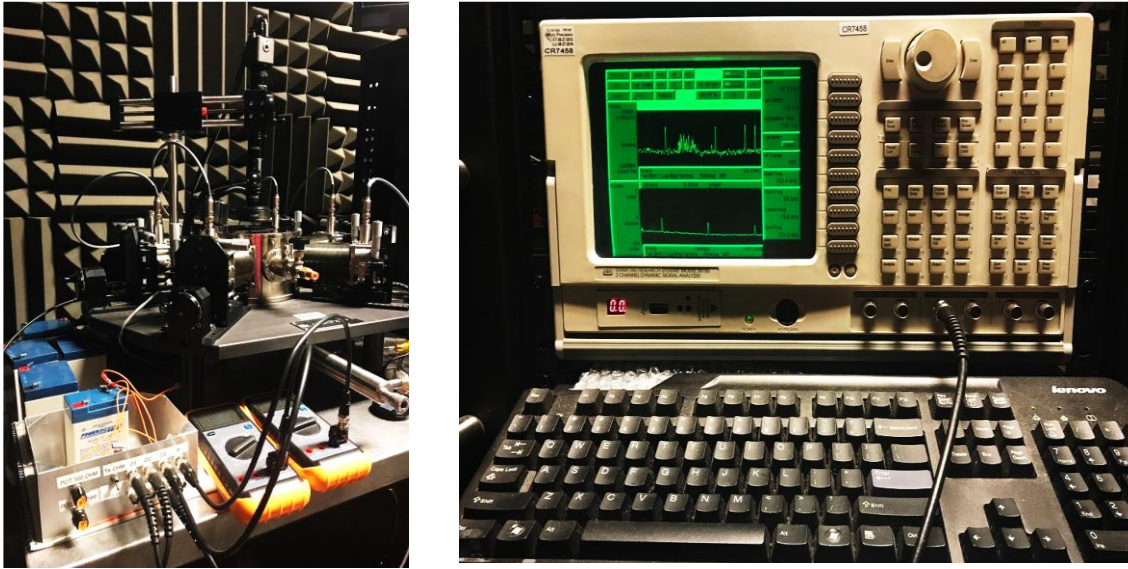circuit which is designed to measure noise of the device.

Figure 4.6: Images show the setup of noise measurements. Left, is the image of chamber and resistive box. Right, is the image of spectrum analyzer (Stanford Research System Model SR785)
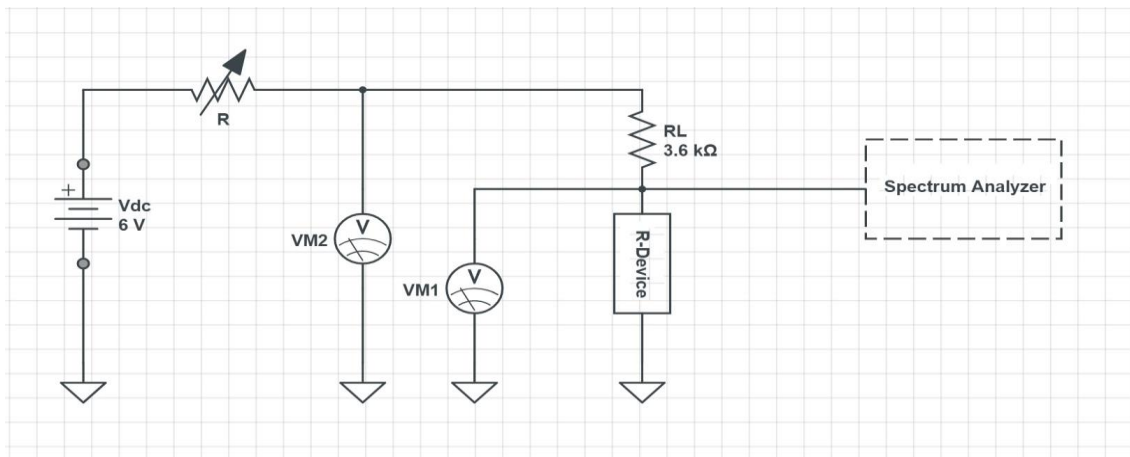

Figure 4.7: The schematic of a circuit, designed to maintain noise measurements. The two voltmeters are specified with VM1 and VM2. The R is a 100 Ω potentiometer and the dashed-box is representing the spectrum analyzer.

As it is clear from the schematic in Figure 4.7, the voltage from the 6 V battery would be divided between a potentiometer (100 Ω) and a 3.6 kΩ resistor (R_L) and the tantalum disulfide device (R-Device). R_L is selected to be a low-noise metal film resistor with the value in the same range of the device resistance. If R_L appears to be smaller, the noise spectrum could be dominated by the resistance of R_L instead of that of the device. I have set the voltage across the device to be around 600 mV, by reading from voltmeter 1 (VM1), and then read the total voltage drop across both R_L and the device, from voltmeter 2 (VM2). With these voltage values and considering the point that the current drain of spectrum analyzer is negligible, the device resistance can be calculated at each voltage reading step. The spectrum analyzer (Stanford Research System Model SR785, shown in right part of figure 4.6) measures spectral density for the voltage S_V, in this configuration. According to the Equation 4.4, the spectral density of the device for current S_I, can be derived.

Noise measurements have started with the temperature of 290 K and have increased till 370 K at the step of 5 K. During the steps of temperature increase, after each adjustment I wait till the temperature of the device becomes almost fixed and then start measuring. Since our spectrum analyzer does not provide us with a single full span from 1 Hz to 100 kHz, I may need to break the measuring frequencies into four bands (1 Hz~100 Hz, 100 Hz~3 kHz, 3 kHz~50 kHz, 50 kHz~100 kHz) and do the measurements in four sub-steps at each temperature level. Furthermore, in order to reduce the noise that is generated from the environment, I switch off optical microscope's light before starting each measurement.
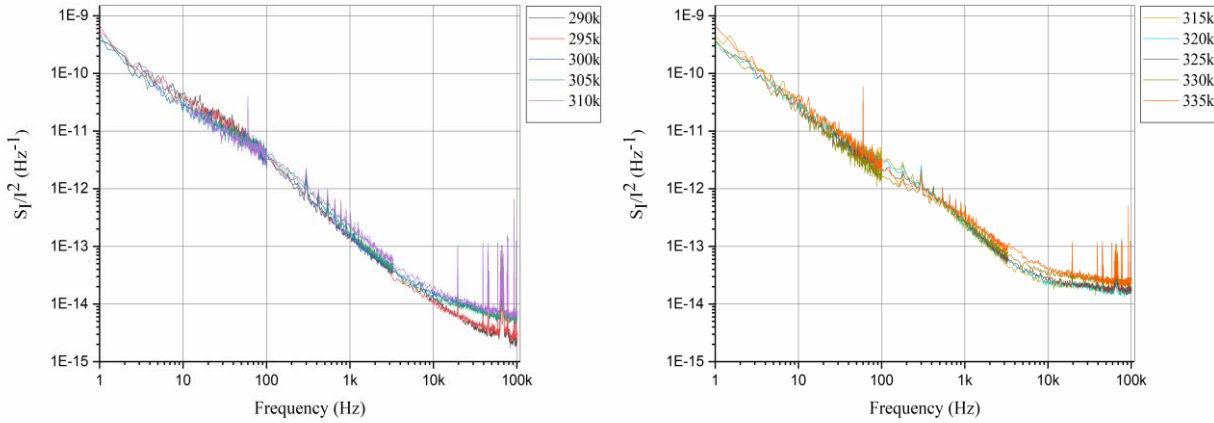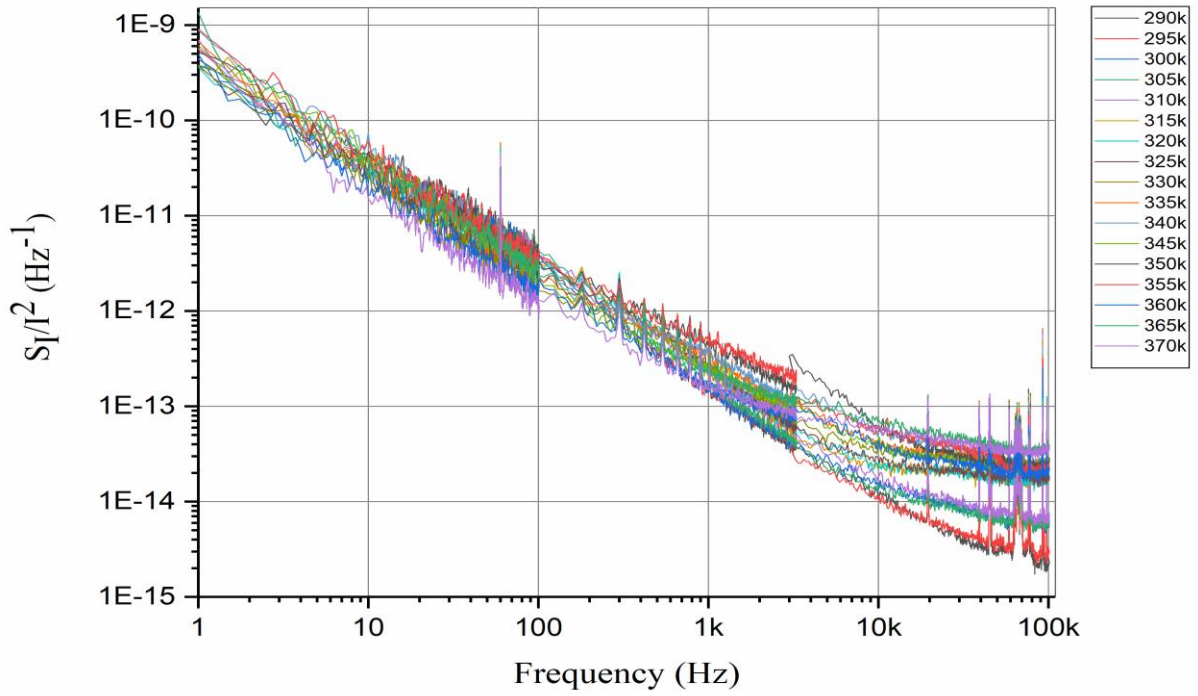
Figure 4.8: The log-log plots of spectral density versus frequency for 1T-TaS$_2$ device with less than 12 nm thickness and 4 μm channel length and ~2.5 μm width. The top plot represents the measurements for the frequency range of 1 Hz to 100 kHz and temperature range of 290 K to 370 K. The bottom-left plot is specified to just 290 K ~ 310 K temperatures for better sight on the bulges around 10 Hz ~ 100 Hz. The bottom-right plot is just drawn for the temperature range of 315 K ~ 335 K for better vision on the bulges around 100 Hz to 1 kHz.

When the measurements are completed I wait till the chamber is cooled down and then vent and take the sample out. Figure 4.8 represents the normalized spectral density of current, $S_I/_{I^2}$ versus frequency from 1 Hz to 100 kHz for h-BN-capped 1T-TaS$_2$ device with channel size of 4 μm × 2.5 μm and thickness of <12 nm. The measurements implemented for temperatures from 290 K to 370 K which include the temperature at which 1T-TaS$_2$ have nearly commensurate to incommensurate CDW phase transition (around 365 K here) and plotted in a log-log scale. As it can be seen from the plot, the low-frequency noise for different temperatures is not completely obeying 1/f behavior. For instance, for temperatures about 290 K ~ 310 K there are broad bulges appearing in the range of about 10 Hz to 100 Hz. While for temperature range of 315 K ~ 335 K the bulges form at frequencies around 100 Hz to 1 kHz. After 340 K temperature, the end of the noise spectrum become more flat that could be the combination of thermal noise and 1/f noise [5]. Since 1T-TaS$_2$ has a high electron density of about ~10^{22} cm^{-3}, it would be challenging to attribute these bulges to the trap states due to defects in the structure, similar to the CMOS (complementary metal-oxide-semiconductor) devices [6, 8].

Based on a recent report on the 1T-TaS$_2$ CCDW and NCCDW phases, beside the disorder in the periodic lattice distortion of the structure, they have revealed stacking disorders in the layers of exfoliated 1T polytype of tantalum disulfide [9]. The expected stacking for a perfect 1T phase would be a trigonal stacking arrangement, that all of Ta atoms are located on top of each other from planar vector perspective. However, they observed another arrangement known as hexagonal stacking, in which Ta atoms in some layers have almost one bond length shift with respect to other layers [9]. This fault in the

stacking order was reported to be repeating in several samples and not a rare phenomenon [9]. They suggested that a fractional translation in the CDW can occur as a result of these stacking disorders and it may influence the electronic properties of this material [9]. Therefore, it would be noteworthy to consider these faulty stacks' ordering in the 1T-TaS$_2$ layered structures and their effects on the electrical properties of thin films. Thus, it may be useful to investigate the influence of this factor in low-frequency noise characteristics. However, it is quite clear that further study and modeling are required to clarify the low-frequency noise behavior of 1T-TaS$_2$ devices.

References:

[1] G. Liu, B. Debnath, T. R. Pope, T. T. Salguero, R. K. Lake, and A. A. Balandin, *Nature Nanotechnology*, 11, 845-851 (2016).

[2] Y. Yu, F. Yang, X. F. Lu, Y. J. Yan, Y. Cho, L. Ma, X. Niu, S. Kim, Y. Son, D. Feng, S. Li, S. Cheong, X. H. Chen and Y. Zhang, *Nature Nanotechnology*, 10, 270-276 (2015).

[3] M. Hollander, Y. Liu, W. Lu, L. Li, Y. Sun, J. A. Robinson and S. Datta, *Nano letter*, 15, 1861-1866 (2015).

[4] Keysight Technologies, B1500A Semiconductor Device Analyzer datasheet (2017).

[5] F. N. Hooge, T. G. M. Kleinpenning and L. K. J. Vandamme, *Rep. Prog. Phys.*, 44, 480-532 (1981).

[6] A. A. Balandin, *Nature Nanotechnology*, 8, 549-555 (2013).

[7] D. K. C. MacDonald, *Noise and Fluctuations: an introduction*, John Wiley & Sons, Inc. (1962).

[8] A. H. Thompson, F. R. Gamble and J. F. Revelli, *Solid State Communications*, 9, 981-985 (1971).

[9] R. Hovden, A. W. Tsen, P. Liu, B. H. Savitzky, I. Baggari, Y. Liu, W. Lu, Y. Sun, P. Kim, A. N. Pasupathy and L. F. Kourkoutis, *PNAS*, 113 (41), 11420-11424 (2016).

Chapter 5

Conclusions

5.1 Summary and Conclusions

In this thesis, I explained the fabrication and characterizations of two-dimensional charge-density-waves devices. The CDW is a periodic spatial alteration of electronic charge density which comes along with periodic lattice displacements. The 1T polytype of tantalum disulfide, one of the members of TMDs family, is a rich candidate in the CDW phase transitions. I have implemented few-layer 1T-TaS$_2$ as my 2D channel material and Later, did electrical characterizations on the fabricated devices to investigate their interesting CDW behavior.

First I started with an introduction to the theory of charge-density-waves. The CDW effects in one-dimensional free electron gas was briefly described and discussed that due to a topology of the Fermi surface, the 1D metallic system has a high possibility of perfect nesting with a wave vector about $2k_f$ and this may lead to a logarithmic singularity in static response function at low temperatures [1]. The coupled electron-phonon in 1D system is not stable and considering the divergence in the electron response function at $q = 2k_f$, the reduction in phonon frequencies would become significant at

this wave vector. This instability in the coupled electron-phonon 1D systems leads to the definition of transition temperatures. This instability may cause a periodic lattice distortions and band gap opening at $q = \pm K_f$ [1]. Besides the quasi-1D systems, CDW could form in some of the two-dimensional structures. 1T-TaS$_2$ was selected as a rich candidate in CDW phase diagram and the three different phases of CDW, known as CCDW, NCCDW and ICCDW, which were accompanied by atoms repositioning, were explained.

In chapter 2, I reviewed some recent published reports on the charge-density-waves in 2D materials. Articles were discussed on the observation of CDW phase transitions between CCDW, NCCDW and ICCDW states and their reported dependencies on the films thicknesses. Since 1T-TaS$_2$ exhibits a hysteresis window in its I-V characteristics, application-based reports which were addressing this behavior were described. These reports with more focuses on the applications of CDW materials such as voltage-controlled oscillator based on integrated tantalum disulfide-boron nitride-graphene devices and one with memristive-function perspective, were summarized. Then continued by studying CDW effects, existing in other TMD materials such as few-layer TiTe$_2$, VSe2, 1T-TaSe$_2$ and 1T-TiSe$_2$ [2-10].

Afterwards, the steps toward fabricating 1T-TaS$_2$ devices were explained in chapter 3. The thin films of tantalum disulfides were mechanically exfoliated from the CVT-grown bulk of 1T-TaS$_2$. In order to protect the device from oxidation and preserving the crystal, it was capped with hexagonal boron nitride. The process continued with describing e-beam lithography steps for creating electrodes' patterns. Then the

hexagonal BN layers, which were covering the contacts areas, were etched and the steps followed by Ti/Au deposition immediately. The final 1T-TaS$_2$ devices with <12 nm channels thicknesses, various widths and h-BN capping layer presented at last.

Chapter 4, was continued by electrical characterizations and low-frequency noise measurements of the fabricated 1T-TaS$_2$ devices with less than 12 nm channels thicknesses. The setup of the experiment was explained and followed by current-voltage characteristics' measurements at room temperature. The presence of an abrupt jump, in the current passing through the channel, was expressed to be an indication of electrically induced NCCDW to ICCDW phase transition or it could be resulted from losing insulating states in CDW domains due to high electric field, while the crystal was still in the NCCDW state [2]. This threshold voltage was shown to vary for devices with different channel area sizes. The I-V curves were measured in both sweeping the voltage upward and downward and showed a hysteresis behavior, in which the threshold voltage in the decreasing cycle happened at lower voltage value compare to the increasing cycle. Afterwards, a temperature-dependent resistance measurements were implemented. I went through a temperature range from 290 K to 370 K and observed a nonlinearity behavior in the resistance values. As the temperature increased from 290 K to 360 K, the resistance of 1T-TaS$_2$ device decreased almost monotonically, but at 365 K it dropped abruptly and set to new low value. I witnessed the NCCDW to ICCDW phase transition occurring at 365 K for the device. Based on the previous reports, I may suggest the film thickness as one possible factor that can affect the CDW transition temperatures [11].

Furthermore, various types of electronic noise were described and a low-frequency noise measurements for 1T-TaS$_2$ device in the range of 1 Hz to 100 kHz and for temperatures from 290 K to 370 K, were performed. The low-frequency noise behavior showed 1/f dependency to some extent, however at some specific temperatures there were some bulges appearing that could be attributed to the generation-recombination noise. Also at the frequencies, around 10 kHz to 100 kHz the noises started to follow some diverse flat behavior for different temperatures, that may be the combination of thermal noise and 1/f noise [12]. This controversial behavior of 1/f noise characteristics for 1T polytype of tantalum disulfide device may be related to the domains sizes and their defects and periodicities in the NCCDW phase of 1T-TaS$_2$ material [13]. These measurements reveal the necessity of further studies on the low-frequency noise characteristics of this material. The acquired results could be helpful for the development of electronic devices based on the two-dimensional CDW materials.

References:

[1] G. Grüner, *Denisty Waves in Solids*, Perseus Publishing (1994).

[2] G. Liu, B. Debnath, T. R. Pope, T. T. Salguero, R. K. Lake and A. A. Balandin, *Nature Nanotechnology*, 11, 845-851 (2016).

[3] M. Yoshida, R. Suzuki, Y. Zhang, M. Nakano, Y. Iwasa, *Sci. Adv.*, 1 (9) (2015).

[4] J. M. Khan, D. Teweldebrhan, C. M. Nolen and A. A. Balandin, *Mater. Res. Soc. Symp. Proc.*, 1344 (2011).

[5] K. Xu, P. Chen, X. Li, C. Wu, Y. Guo, J. Zhao, X. Wu and Y. Xie, *Angew. Chem.*, 125, 10671-10675 (2013).

[6] M. Falmbigl, A. Fiedler, R. E. Atkins, S. F. Fischer and D. Johnson, *Nano Lett.*, 15, 943-948 (2015).

[7] R. Samnakay, D. Wickramaratne, T. R. Pope, R. K. Lake, T. T. Salguero and A. A. Balandin, *Nano Lett.*, 15, 2965-2973 (2015).

[8] K. Sugawara, Y. Nakata, R. Shimizu, P. Han, T. Hitosugi, T. Sato and T. Takahashi, *ACS Nano*, 10, 1341-1345 (2016).

[9] J. Wang, H. Zheng, G. Xu, L. Sun, D. Hu, Z. Lu, L. Liu, J. Zheng, C. Tao and L. Jiao, *J. Am. Chem. Soc.*, 138, 16216-16219 (2016).

[10] D. L. Duong, G. Ryu, A. Hoyer, C. Lin, M. Burghard and K. Kern, *ACS Nano*, 11, 1034-1040 (2017).

[11] Y. Yu, F. Yang, X. F. Lu, Y. J. Yan, Y. Cho, L. Ma, X. Niu, S. Kim, Y. Son, D. Feng, S. Li, S. Cheong, X. H. Chen and Y. Zhang, *Nature Nanotechnology*, 10, 270-276 (2015).

[12] F. N. Hooge, T. G. M. Kleinpenning and L. K. J. Vandamme, *Rep. Prog. Phys.*, 44, 480-532 (1981).

[13] R. Hovden, A. W. Tsen, P. Liu, B. H. Savitzky, I. Baggari, Y. Liu, W. Lu, Y. Sun, P. Kim, A. N. Pasupathy and L. F. Kourkoutis, *PNAS*, 113 (41), 11420-11424 (2016).