Title
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TECHNOLOGICAL APPROACHES IN NANOPOLISHING FOR MICROSTRUCTURES

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ABSTRACT

Polishing technology has been broadly used in manufacturing of components to enhance the surface quality at final processing stage. On the threshold for the 21th century, all of technologies are changing more rapidly than the past. One of them is the miniaturization of the smart systems that require new technological approaches in manufacturing processes. Scientists and engineers have some responsibilities to revise the terminology and expand the area of each technology from the conventional one to nanoengineering.

This paper focuses on the introduction of new technological approaches in nanopolishing for microstructures that imply new additional concepts on the conventional polishing. New concepts include damage-free, planarization, nanotopography and conformalization. Damage-free means to get not only atomic level surface roughness, but also subsurface without any physical defects. As one of the emerging methods, chemical mechanical polishing (CMP) is introduced with chemical reaction on the conventional mechanical polishing. Planarization is one of the fabrication processes for semiconductor devices, to make flat from the bumpy or rugged pattern surfaces for rearrangement of ULSI below quarter microns. Representative applications are reported with IMD, STI, copper and low-k CMP. Nanotopography means nanofeatures having 0.2~20mm wave length covered between nanoroughness (10-100nm) and flatness. It influences on the deterioration of threshold voltage, dielectric breakdown and failure of CMP of thin blanket film. Final issue is pointed to the conformalization which means isotropic removal of microstructures to improve the roughness while maintaining the micro three dimensional forms. Electrorheological and magnetorheological fluid (ERF or MRF) assisted polishing techniques are summarized with their material removal mechanisms and some results.

INTRODUCTION

Sir Isaac Newton reported in Opticks(1695)[1], "The smaller the particles of the substance(abrasives), the smaller will be the scratches by which they continually fret and wear away the glass until it is polished...". This talk means the basic idea of fine polishing was already established in before the industrial revolution. Several keynote papers which have been presented at the CIRP General Assemblies in the end of 20th century by Taniguchi(1983)[2], König(1986)[3], McKeown(1987)[4], Töenshoff(1990)[5], Ikawa(1991)[6] and Venkatesh(1995)[7] have related to the

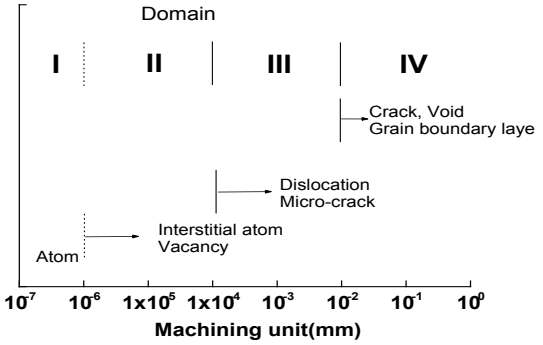
technology of finishing with fine abrasives. From the history, authors can say that polishing technology has been broadly developed to improve the surface quality of system components as a mechanical material removal process at final processing stage.

On the threshold for the 21th century, researchers are moving to nanotechnology field which can make a new technopia and have some responsibilities to revise the terminology and expand the area of each technology from the conventional one to nanoengineering. As one of nanoengineering, polishing technology should be expanded or changed to new form adjusted to current situation.

This paper focuses on the introduction of new technological approaches in nanopolishing for microstructures which implies new additional concepts on the conventional polishing. New concepts in nanopolishing for microstructures include damage-free, planarization, nanotopography and conformalization. Each concept is briefly explained with its necessity, definition, methods to be realized and application examples.

DAMAGE-FREE

As the usage of the electronic and optical devices are increased, the demands for the ideally flaw free or defect free surface and bulk materials have been essential to ensure their electrical and optical functions. The damages on the surface or in the bulk material cause the failure of electron or photon flow.

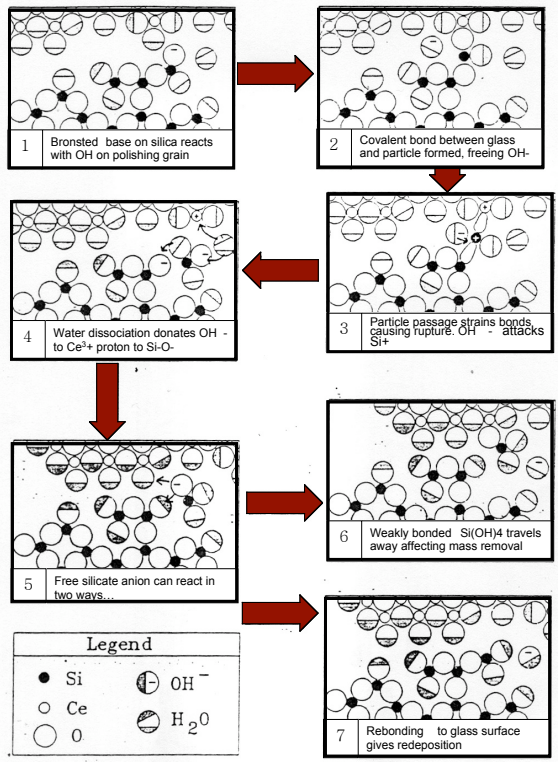


1. THE SIZE OF THE STRESS FIELD AND "WORKING UNITS"

Yoshikawa(1967)[8] conducted pioneering studies on the brittle-ductile behavior of crystal surfaces in finishing. He considered the size of the stress field in terms of "working units" and classified it into four domains as shown Fig. 1.

Each domain is characterized by the defect structure which either pre-exists or has been generated by the processing method. In domain I, the material removal is considered only on the order of a few atoms or molecules. Material removal on this order could not possibly occur by pure mechanical action. Chemical reaction enhanced by mechanical stress and temperature may play an important role in the material removal process in this domain.

It is interesting to note that there are several terms used to describe the processing of chemo-mechanical or mechano-chemical polishing (Vora, 1982[9]), the second one is called tribo-chemical polishing (Heinicke, 1984[10]; Fisher, 1988[11]) and third one is called chemical mechanical polishing (Nanz, 1995[12]). These distinctions are made by researchers as well as practitioners mainly to place proper emphasis on a particular factor that plays a major role in the material removal process. In chemical mechanical polishing (CMP), the driving force for material removal is chemical action, which is followed by mechanical action for the removal of chemically reacted layer. Now CMP is the most common process used in the finishing of Si wafers in semiconductor industry.



2. POLISHING REACTION SEQUENCE PROPOSED BY COOK[13]

The polishing mechanism suggested by Cook[13] is depicted in Fig. 2. In this chemical reaction model, the surface of the silicon oxide is first reacts with OH- ion to form $Si(OH)^4$ and make covalent bonding with the abrasive surface to remove the reacted materials on the surface of oxide (1-4). Then the removed silicate can acts in two ways of either travel away from the polishing site or redeposit on the oxide surface (5-7). The surface of material can be protected from scratch, flaw or crack by the formation of reacted layer which is fundamental source of damage-free mechanism along with the minimal amount of machining unit(domain I~II in Fig. 1). The rate of surface removal during polishing is determined by the relative rates of five processes; (i) the rate of molecular water diffusion into the glass surface, (ii) subsequent glass dissolution under the load imposed by polishing particles (iii) the adsorption rate of dissolution products onto the surface of the polishing grain (iv) the rate of silica redeposition back onto the glass surface (v) the aqueous corrosion rate between particle impacts.

Manufacturing of single crystal silicon wafer is among the most widely known and critical application area of polishing process because of its high requirement level for the subsequent device manufacturing process. The requirements of bare silicon wafers related with polishing can be classified as geometric specifications and defect related issues.

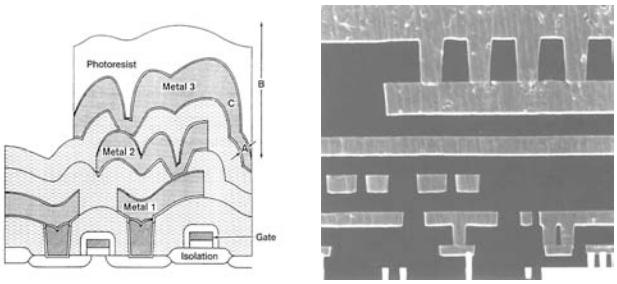
Geometric requirements can be classified in the viewpoint of wavelength of surface topography, such as roughness, nanotopography and flatness. The roughness is reduced to atomic level value by a 2 or 3 steps polishing with different size and concentration of silica abrasives and soft polishing pads. Recently, nanotopography, which will be mentioned later in this paper, is gaining a great importance as the design rule of the device is getting smaller and highly integrated device manufacturing process, specifically, for the isolation process of transistors.

There are several kinds of defects after polishing of wafers, such as, macro-scratches, micro-scratches, flake type chips, edge chips, cracks, crow-feet, pin holes, pits, dimples, waves, dirt, haze or orange peel. Both abrasives in slurry and crystallographic defects in wafer itself are the source of these defects.

The detection of these defects was done by naked eye or microscope with appropriate lighting condition regulated by JIS[46], ASTM [47] and SEMI[48]. However, all of these methods depend on the discipline or the ability of each worker. Therefore, these inspection methods had been replaced by light scattering method which can classify various kinds of defect judging from the angle of scattered light (pit or dirt) and pattern recognition (single pit or scratch).

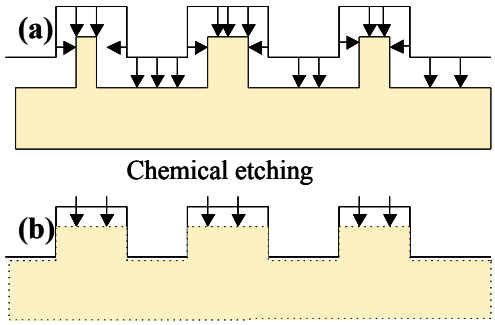
PLANARIZATION

Over the last decade, chemical mechanical planarization (CMP) has been widely accepted as a breakthrough in the planarization of sub-half micrometer integrated circuits (IC) device manufacturing. Because of its excellent planarization capacity to meet stringent lithographic requirements, CMP has been widely used for the planarization of device surface.



(a) without planarization (b)with planarization

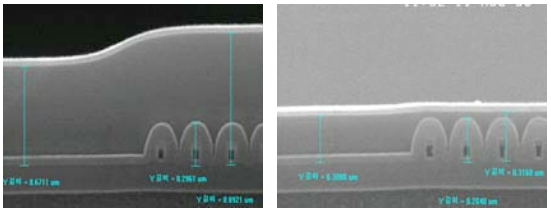
3. MULTILEVEL METALIZATION FOR AN INTEGRATED CIRCUITS; THE EFFECT OF PLANARIZATION (IBM)



4. SCHEMATIC OF THE FUNDAMENTAL MECHANISM OF PLANARIZATION (B) COMPARED WITH ISOTROPIC CHEMICAL MATERIAL REMOVAL PROCESS (A).

CMP is a process of wear which make patterned surface to be flat to ensure the subsequent layer deposition process. As shown in Fig. 3, the planarization gives tremendous advantage to make a 3-dimensional layering or multilevel

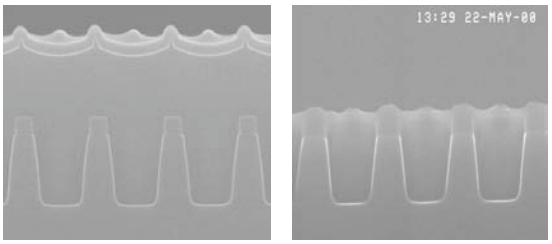
deposition process. The fundamental mechanism of the planarization is an anisotropic material removal process from the protruded area of the surface by the combined actions between chemical and mechanical energy sources. The source of anisotropic material removal is selective mechanical contact and pressure concentration on the summits of topography (Fig. 4). Fig. 4 shows the basic differences between isotropic removal process by chemical reaction and mechanically assisted materials removal process (CMP). In this process of anisotropic removal, the pressure sensitivity and the surface topography of the mating surface, namely polishing pad, have great effect on the efficiency of planarization.



(a) (b)

5. RESULT OF OXIDE PLANARIZATION BEFORE (A) AND AFTER (B) CMP[45]

Planarization of dielectric layer is among the most widely used process for aluminum interconnection. During the dielectric CMP process (Fig. 5), the steps on the patterns induced by conformal chemical vapor deposition process are planarized to meet the requirement of depth of field (DOF). Once the layer is planarized within DOF range, then the subsequent structures can be fabricated on a nearly planar surface to make multilevel interconnection. The main issues of dielectric CMP are uniformity of removal rate across the wafer and within the die and scratch problem. These issues have been reduced by various efforts, such as adopting advanced polishing head with uniform or zone control pressurizing system, dummy filling method, slurry filtering system, advanced process control algorithm (APC) and so on. Recently, the incorporation of low-k material becomes great concern for its comparatively low mechanical strength which causes destruction of the layer by the down force during polishing. To prevent the breakage of the low-k materials, low pressure CMP has been emerged as an alternative polishing method.

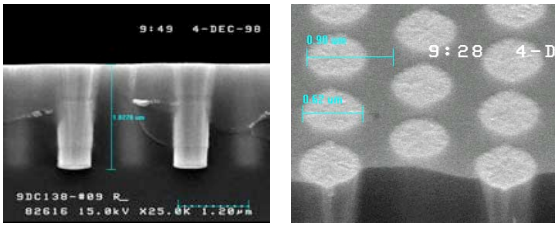


(a) (b)

6. SHALLOW TRENCH ISOLATION (STI) BEFORE (C) AND AFTER (D) CMP[45]

Shallow trench isolation (STI) process (Fig. 6), which can be realized only by the CMP process, enables to make highly integrated devices by the benefits of preventing current leakage between transistors, hence, making it possible to design densely populated active area. Cerium oxide abrasives are usually used to get a highly planarized layer and also various kinds of chemical additives, such as organic additives, are used to enhance the selectivity between oxide and silicon nitride layer[45].

Polishing of tungsten, as well as other types of metal, requires a two-step process in which an oxide layer is formed over the metal surface and then abraded away in the CMP process. The roughened pad and slurry particles remove the oxide layer at the highest points, where the exposed metal then regrows the oxide layer. With appropriate metal slurry, the oxidation process is self-limiting, so the oxide ceases to grow in low, unabraded areas. By continuing this process, the metal layer is planarized and removed (Fig. 7).

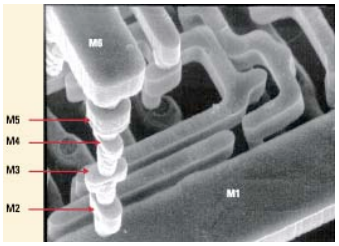


(a) (b)

7. CMP RESULT OF TUNGSTEN PLUG CROSS SECTION (A) AND TOP VIEW (B)[45]

CMP technology enabled the replacement of aluminum interconnects with lower-resistivity copper, because copper cannot be subtractively etched in a practical manner. The process of forming a trench for the interconnect and then planarizing it so copper remains only in the trenches is often referred to as damascene processing[49] (Fig. 8). Although the CMP is a unique solution for the copper interconnection, the complicated chemical interactions between

copper and slurry chemicals, such as oxidizers, complexing agent, acid, pH, corrosion inhibitors, make it difficult to stabilize the copper CMP.



8. COPPER DAMASCENE PROCESS (TSMC)

In the CMP process, the material removal rate is determined by several tens of stand-alone variables and their numerous interactions including pressure, velocity, temperature, properties of abrasives, chemical composition of slurry, properties of polishing pad and so on[14]. However, there has been exist simple empirical governing equation named Preston's equation (Eq. 1) or Prestonian equations that includes only two independent variables (pressure and velocity) and other effects are veiled in a black box of Preston's constant "k" [15-21].

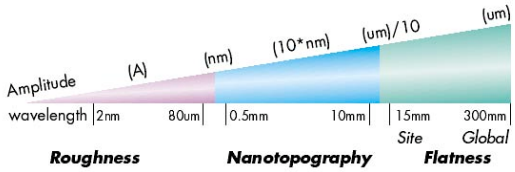
$$Removal\ rate = k\,P\,V \qquad (Eq.\ 1)$$

Recently, some studies have been turn their focus on the black box "k" by incorporating more variables and more complex theories, such as probability functions, contact mechanics, colloid and their interactions and tribological approaches[22-26]. Although most of these studies are not able to delineate all the complex phenomena of CMP, they enhance the fundamental understanding of multivariable CMP process.

The main concern in CMP process is good planarity across a die (less than 150nm height deviation), low film thickness uniformity within the wafer (±2-5%, 1σ), high removal rate for high throughput and low cost-of-ownership, less defect and good selectivity and/or good endpoint technology to avoid under or over-polishing[27]. To meet these requirements, sophisticated CMP processes are under development and also it will become more and more critical issues for subtle 100nm device planarization strategy.

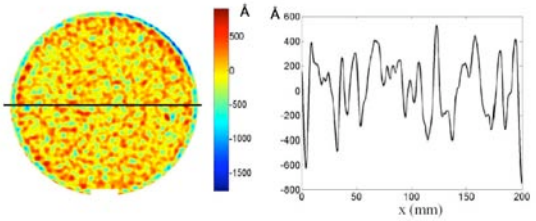
NANOTOPOGRAPHY

Measuring and analyzing surface topography of Si wafers at heights in the nanometer range are gaining increasing importance for manufacturing bare polished Si wafers appropriate for future CMOS processes[28]. As the design rules of the semiconductor devices are down to quarter micrometers, nanotopography has emerged as an important concern in shallow trench isolation (STI) on wafers polished by means of CMP.

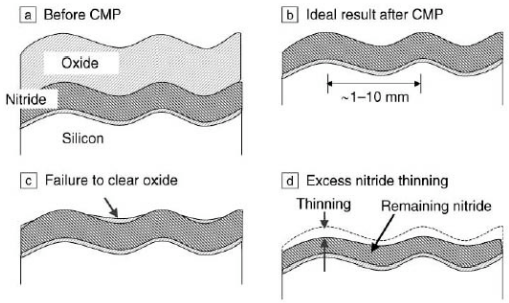


9. REGIME OF NANOTOPOGRAPHY[31]

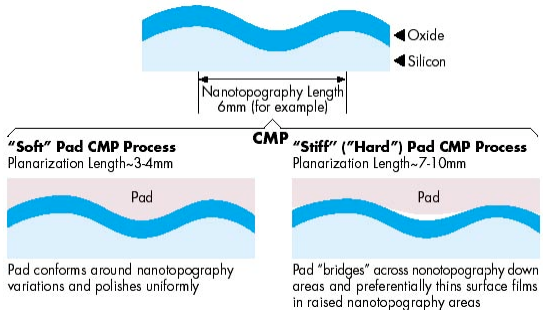
Nanotopography bridges the gap between roughness and flatness in the topology map of wafer surface irregularities in spatial frequency (Fig. 9). Wafer nanotopography is defined to subtle 10 to 100nm height variations which occur over lateral distances of 0.2 to 20mm on unpatterned silicon wafers[29], the so called nanotopography are especially of interest due to their strong impact on the yield of CMP[30] as shown in Fig. 10.



10. TOP VIEW AND CROSS SECTION OF WAFER NANOTOPOGRAPHY[32]



11. NANOTOPOGRAPHY ISSUES AFTER CMP[33]



12. CMP WITH NANOTOPOGRAPHY; CONCEPT OF POLISHING BY SOFT (LEFT) AND HARD (RIGHT) PAD[34]

The impact on nanotopography on the wafer after CMP is appeared either in the form of failure to clear the oxide layers on the nitride thin film (Fig. 11 c) or in the excess nitride thinning (Fig. 11 d) which leads to the operation failure of transistors. The primary effect of oxide uniformity is due to the hardness of the CMP pad. The fundamental concept is very simple that soft polishing pads conform to local topology variations while hard pads do not (Fig. 12).

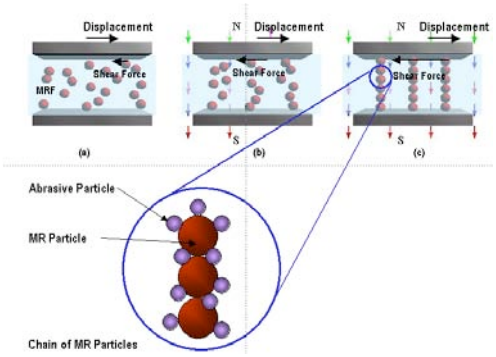
Although the soft pad is beneficial to achieve uniform removal of the oxide film, it generally degrades the planarity of the patterned surface. Therefore, the nanotopography should be controlled before FEOL(Front End of Line) process, that is, during the wafering process.

The nanotopography can be reduced by both polishing method and polishing parameters during bare wafer polishing process. Wax mounted polishing is a method that has weak effect on improving the nanotopography issues because the wafer is pressed to the carrier to polish the wafer surface. After the wafer is released from the carrier surface, the stress remained in the wafer makes the surface uneven. However, free mounting method with backing materials having viscoelastic properties gives better results because of its stress less fixturing method[31]. Double side polishing (DSP) is known as the best way to reduce nanotopography and also has great benefit on enhancing the flatness of the wafer, namely total thickness variation (TTV)[35].

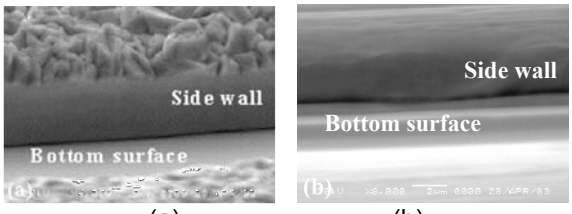
CONFORMALIZATION

Conformalization is a polishing process that finishes the surfaces of micro patterns, structures or wavy surfaces with maintaining their shape but reduces the roughness of the surface. Most widely used process for conformal polishing is the use of magnetorheological fluid (MRF) or electrorheological fluid (ERF), since their ability to easily conform to mating surface and reversible characteristics by controlling magnetic or electric field. A recently written review article provides an overview of the history, theory, and implementation of these technology[36]. The utility and productivity of MRF have been proven for a wide spectrum of optical glasses and demonstrated for a variety of non-glass optical materials[37].

A magnetorheological (MR) fluid is a suspension of magnetically soft ferromagnetic particles in a carrier liquid. Typically, the particles are of the order of a few microns in diameter, and their volume concentration is 30% to 40%. When exposed to a magnetic field, the viscosity and yield stress of the suspension increase several orders of magnitude because of rearrangement of the particles[44]. As shown in Fig. 13, the magnetic force can change the arrangement of the ferromagnetic particles in the fluid to increase or decrease the viscosity of the MRF. The transition is rapid and reversible and this characteristic makes the process a prominent method to polish various microstructures effectively.



13. BEHAVIOR OF MAGNETORHEOLOGICAL FLUID UNDER THE EFFECT OF MAGNETIC FIELD.



(a) (b)

14. COPPER MICROSTRUCTURES BEFORE (A) AND AFTER (B) MAGNETORHEOLOGICAL FLUID POLISHING [43]

Recently, these technologies expand their application area to microstructures such as MEMS structures. With the advent of MEMS technology, it is possible to fabricate many novel three-dimensional microstructures. In some MEMS devices, surface quality is often very important because it affects the performance of the final device. However, there has been no polishing technique useful to microstructures, while various existing polishing methods are applicable only to flat surfaces or macro scaled structures. For instance, in case of a micro channel structure, which is generally manufactured by subsequent deposition and etching process, it can be used as a part of a micro fluidic system, a signal transmission line in radio frequency (RF) applications, and a micro optical device [38-41]. As surface roughness increases, such problems as flow resistance, conducting loss and optical loss will increase and the resulting efficiency will decrease[42].

Fig. 14 is an example of microstructure before and after MRF polishing. The advantage of MRF polishing is that there is virtually no wear of polishing tools, flexibility of tool shape change and low stress polishing. Therefore, a continuous polishing is possible and various kinds of workpieces having macro or microstructures can be polished under low polishing stress condition which gives way wide open to numerous application area.

CONCLUSION

In this paper, review of technological approaches in nanopolishing for microstructures, which implies new additional concepts on the conventional polishing, was mentioned. Concepts in nanopolishing for microstructures included damage-free, planarization, nanotopography and conformalization. Each concept was briefly explained with its necessity, definition, method to be realized and application examples.

1. The use of nano size abrasives and appropriate aid of chemical reaction with the minimal amount of machining unit make it possible to achieve virtually defect-free surface which enables to implement electronic devices on the surface of polished materials.
2. The introduction of dual damascene copper interconnection, shallow trench isolation, IC design demands, the search for low-k materials, and the introduction of noble metals are turning CMP into a hub process in the fab.
3. Nanotopography bridges the gap between roughness and flatness in topology map of wafer surface irregularities in spatial frequency. The research on the source and the method for reducing nanotopography have been an important issues as the design rules of devices are down to quarter micrometers. Double side polishing is known as an efficient method to reduce the nanotopography but there still remains research area of fundamentals on its mechanism.
4. The polishing process using MRF or ERF has tremendous advantage on conformal finishing of workpieces having macro or microstructures and the characteristics of tool shape flexibility, low stress and wear-free are the merits of the process, which enables to be used in various application area.

The polishing technologies will be more and more important area of research as the technology node goes to nano-level manufacturing.

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49. M. Oliver, Chemical Mechanical Polishing, Semiconductor International, June, 2003.