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III-V $In_xGa_{1-x}As$ / InP MOS-HEMTs for 100-340GHz Communications Systems

A dissertation submitted in partial satisfaction

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in

Electrical and Computer Engineering

by

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ABSTRACT

III-V $In_xGa_{1-x}As$ / InP MOS-HEMTs for 100-340GHz Communications Systems

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This work summarizes the efforts made to extend the current gain cutoff frequency of InP based FET technologies beyond 1 THz. Incorporation of a metal-oxide-semiconductor field effect transistor (MOSFET) at the intrinsic Gate Insulator-Channel interface of a standard high electron mobility transistor (HEMT) has enabled increased $g_{m,i}$ by increasing the gate insulator capacitance density for a given gate current leakage density. Reduction of $R_{S,TLM}$ from 110 Ω•μm to 75 Ω•μm and $R_{on}(0)$ from 160 Ω•μm to 120 Ω•μm was achieved by removing/thinning the wide bandgap modulation doped link regions beneath the highly doped contact layers. Process repeatability was improved by developing a gate metal first process and D_{it} was improved by inclusion of a post-metal H_2 anneal. $In_xGa_{1-x}As$ / InAs composite quantum wells clad with both InP and $In_xAl_{1-x}As$ were developed for high charge density and low sheet resistance to minimize source resistance.

With these improvements a L_g = 8 nm, t_{ch} = 6.5 nm transistor with f_τ = 511 GHz, f_{max} = 283 GHz, a L_g = 18 nm, t_{ch} = 2.5 nm transistors with f_τ = 350 GHz, f_{max} = 400 GHz, a L_g = 40 nm, t_{ch} = 7.0 nm transistor with f_τ = 420 GHz, f_{max} = 592 GHz were demonstrated. Power gain was sometimes limited by R_G more than 10 Ω due to poor T-Gate stem filling.

Based on these results and those reported in [1-3], a theory on the effects of channel thickness on quantum well ballistic devices was proposed. Simply, thin quantum wells have large Eigen-state energies limiting the amount of available ($E_F - E_1$) beyond threshold.

Because a quantum well device's maximum conductance occurs when E_F is equal to or nearly equal to the conduction band minimum of the barrier material, current in thin channel devices is limited not by effective mass effects (i.e. density of states or injection velocity) but by band-offset limitations.

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1. Introduction

Demand for high data rate communication systems has exploded in the last decade. Higher frequency systems enable access to higher data rates, currently unallocated bands, and wide bandwidth. As industry begins to introduce 5G technologies at 25-100 GHz, research must aim to facilitate >100 GHz communication systems. For amplifiers to exhibit low noise figure and high-power efficiency, their cutoff frequencies (f_τ and f_{max}) must be ~10x the operating frequency due to the 20 dB/decade gain roll off at high frequencies [1]. Because FETs exhibit lower parasitic resistance $(R_S + R_G) \bullet g_m$ than bipolar transistors $R_{bb} \bullet g_m$, they can realize smaller charging times (RC) and larger current gain cut-off frequencies (f_τ) which is useful for low-noise applications. Amplification at $f >$ 600 GHz has been widely demonstrated using both HEMTs and HBTs [2]–[5]. Further improvement in cutoff frequencies is required to realize power efficient amplification for frequencies more than 100 GHz.

Despite the highly scaled dimensions of Si devices, f_τ and f_{max} are limited to ~500 GHz due to large end capacitances intrinsic to very-large-scale integration (VLSI) devices [6]. InP-based HEMTs are widely used in RF applications because of their low parasitic capacitances and high transconductance (g_m). State-of-the-art (SOA) high frequency HEMTs generally use an $In_xGa_{1-x}As$/InAs composite channels that have smaller m^* than Si and thus large injection velocity (v_{inj}). However, they are limited by large gate leakage current (I_G) density, low gate insulator capacitance (C_{ins}), and large source resistance (R_S). Gate leakage current density determines the minimum thickness (t_{ins} = 5 nm) of the $In_{0.52}Al_{0.48}As$ gate insulator which also limits the intrinsic transconductance ($g_{m,i}$) [7], [8]. The extrinsic transconductance is limited by large R_S associated with conduction across the widegap modulation doped "Link" layer.

Figure 1.1a illustrates a typical HEMT cross-section. The channel region is controlled by the gate capacitor where the gate insulator is a wide bandgap semiconductor. The epitaxially smooth interface between the gate insulator and channel reduces scattering and enables extremely high g_m. To enable low parasitic gate-source (C_{GS}) and gate-drain capacitances (C_{GD}), the source and drain electrodes are located far from the gate (50 – 200 nm). To get electrons from the source to the channel, a conductive quantum well is used. The quantum well is comprised of modulation doped wide bandgap semiconductor barriers and a narrow bandgap, high mobility channel.

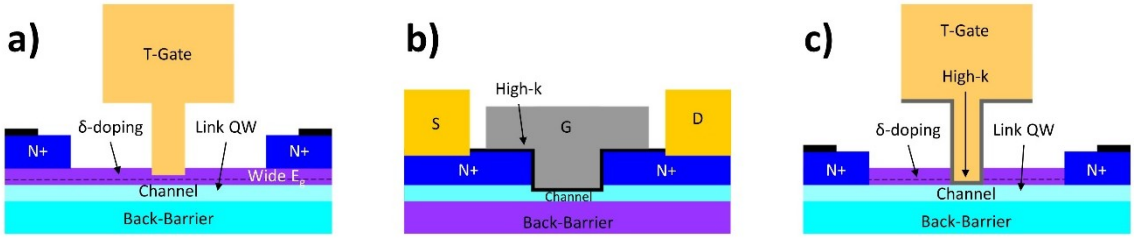

Figure 1.1 Cross-sectional illustration of a standard a) InP-based HEMT b) III-V DC optimized MOSFET c) proposed InP-based MOS-HEMT

InP based high-electron mobility transistors (HEMTs) have been widely reported exhibiting f_τ in excess of 400 GHz [7]–[12]. Recent devices report f_τ > 600 GHz and f_{max} > 800 GHz using high-indium content, 8-10 nm thick channels [3], [13]. Chang *et al.* reported record f_τ = 710 GHz using a 5 nm thick $In_{0.70}Ga_{0.30}As$ channel [14]. Pushing the cutoff frequencies beyond 1 THz requires increased $g_{m,i}$ and reduced R_S.

To further scale $g_{m,i}$ the gate insulator must be thinned. Due to the small conduction band offset (CBO) of metal / $In_{0.52}Al_{0.48}As$ / $In_xGa_{1-x}As$, thermionic and tunneling currents are large. The larger CBO of an oxide truncates the thermionic emission and reduces the tunneling current at a given thickness, enabling further scaling of t_{ins} thus facilitating larger $g_{m,i}$.

Despite the attractive transport properties of III-V materials, III-V metal-oxide-semiconductor-field-effect-transistor (MOSFET) technology was elusive for many years due to large interface trap densities (D_{it}) at the semiconductor-oxide interface. Major recent advancements in oxide deposition facilitated an abundance of research in III-V MOS. Lee *et al.* reported $g_{m,e}$ = 3.0 mS/μm using a 6 nm pseudomorphic-InAs channel [15]. Huang *et al.* reported on improved drain conductance and reduced source-drain leakage using $AlAs_{0.56}Sb_{0.44}$ back-barriers [16] and also demonstrated $g_{m,e}$ > 2.0 mS/μm for ultra-thin-body (UTB) devices [17]. Lin *et al.* reported the effect of channel thickness on $g_{m,i}$ as well as record $g_{m,e}$ = 3.45 mS/μm [18], [19]. Regrowth processes were common among the MOS community, enabling a bottom-up process rather than the top-down processes often used for HEMTs. Despite the extraordinary DC results, most III-V MOSFET research targeted VLSI applications, imposing certain design constraints:

1. Device footprint – requires small gate-source and gate-drain spacing resulting in larger parasitic C_{GS} and C_{GD}
2. Low supply voltage – limits the gate overdrive and degree of channel inversion
3. Intrinsic transistor designed to maximize I_{on}/I_{off} at set I_{off} – requires spacers and/or barriers as well as a doped back-barrier. The former increases R_S and the latter introduces parasitic body capacitance

Additionally, because the intrinsic device is of primary interest, III-V MOSFET work aimed to simplify the extrinsic device. **Figure 1.1b** illustrates a typical III-V MOSFET cross-section optimized for VLSI. As a result, the above reported devices have large gate footprints and doped back-barriers, resulting in additional parasitic capacitances, making them unsuitable for high-frequency operation.

Our proposed device combines the MOSFET with the HEMT, illustrated in **Figure 1.1c**. The gated region is a MOSFET and contains a high-k gate dielectric with a pseudomorphic-InAs channel enabling increased $C_{g\text{-}ch}$ and $g_{m,i}$. The access regions and extrinsic device are a HEMT. The source-drain is pulled 50 nm away from the gate and connected by a conductive quantum well while a T-Gate is used rather than an I-gate. To minimize R_S, a regrowth process, similar to that in [15]–[17], is proposed to place the source-drain directly on the channel. The RF performance of MOS-HEMTs is increased by:

1. Reducing intrinsic transit delays by reducing L_g and increasing $g_{m,i}$
2. Reducing RC charging delays by adding Gate-Source (L_{GS}) and Gate-Drain (L_{GD}) recesses in order to reduce both $C_{GS,f}$ and $C_{GD,f}$
3. Reducing RC charging delays by increasing I_{DS} and $g_{m,e}$ by reducing R_S.

Successful scaling requires lithographic resolution of the gate to be < 25 nm while the Gate-Contact alignment must be better than 20 nm. Further scaling challenges include aligning, resolving, and filling high-aspect ratio (<50 nm wide 200 nm tall) T-Gates. Alignment of the T-Gate to the Gate-Recess must be better than 20 nm and occurs late in the process after the 0-layer alignment marks have experienced significant processing. This thesis describes the design and fabrication of $In_xGa_{1-x}As$ / InP MOS-HEMTs and is organized as follows:

Chapter 2 describes the basic operation of long and short gate-length MOSFETs and explores the effects of channel eigenstates in ultra-thin body (UTB) devices. Chapter 3 explains the regrowth fabrication process of MOS-HEMTs later described and discusses in detail process considerations and tradeoffs. Chapter 4 discusses the first Generation of regrown MOS-HEMTs which exhibited peak f_τ = 511 GHz for a drawn L_g = 8 nm device.

Increased f_τ compared to [20] was achieved by including an $In_{0.52}Al_{0.48}As$ back-barrier, scaling the source-drain metal spacing, and decreasing resistance through the wide band-gap modulation doped region. Short gate length devices exhibited small power-gain cut-off frequencies (f_{max}) due to excessively large gate resistance (R_G) which is attributed to poor T-Gate stem filling. Chapter 5 discusses second Generation devices which exhibited peak f_τ = 356 GHz for a drawn L_g = 12 nm device. The decrease in current-gain-cutoff-frequency is attributed to the ultra-thin channel (t_{ch} = 2.5 nm) which limits the intrinsic transconductance. Moderately reduced R_S was achieved by digital etching through the modulation doped InP layer immediately prior to re-growing the N+ $In_{0.53}Ga_{0.47}As$ source-drain regions. End resistance (R_{end}) associated with charge imaging on the link semiconductor surface rather than in the quantum well due to the isotropic etch profile limited the benefit of link removal. Chapter 6 discuss third Generation devices which exhibited peak f_τ = 420 GHz for a drawn L_g = 40 nm and peak f_{max} = 604 GHz for a drawn L_g = 50 nm device. Increased channel thickness, decreased t_{ins}, and reduced R_S compared to Generation 1 enabled extremely high $g_{m,e}$ = 2.9 mS/µm. The current gain cutoff frequency was limited by large C_{GS} > 0.85 fF/µm and C_{GD} > 0.25 fF/µm. Improved gate resistance compared to Generation 1 enabled balanced (f_τ , f_{max}). Generation 3 devices exhibited $I_{off} \approx$ 10 nA/µm, I_g < 10 nA/µm, and g_m / g_{ds} > 12 demonstrating the significant improvements in leakage and electrostatics realizable with a MOS-HEMT. Chapter 7 introduces a confined selective regrowth technique – template assisted selective epitaxy (TASE) – and explores process considerations for template fabrication as well as the template effects on growth. Finally, Chapter 8 aims to summarize the work and propose future device generations for the MOS-HEMT and possible device applications for TASE.

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2. FET Theory and Design

In this chapter, ideal MOSFET theory and practical design considerations will be discussed. Ballistic FET theory for quantum well devices will be derived, and quantum mechanical effects in the channel included to provide further guidance for future high frequency FET/HEMT channel design. High frequency figure of merits and the common-source small-signal-equivalent-circuit (SSEC) are introduced. Radio frequency (RF) measurement, pad de-embedding, and SSEC extraction are also discussed. Multiple device parameters used throughout the rest of this thesis are defined and discussed in this chapter.

A. Principle of Operation

A MOSFET is a four-terminal device: gate, source, drain and body [1]. Usually the body is tied to the source and will be assumed to be grounded. A MOSFET, as all FETs and HEMTs, operates based on the field effect; charges on the controlling terminal (gate) induce opposite charges elsewhere in the device. In the case of a MOSFET, charge on the gate induces charge in the channel which is supplied by the source and drain. **Figure 2.1** illustrates a standard MOSFET cross-section as well as a top-down layout. A MOSFET has three regions of operation: thermionic emission (subthreshold), resistive (linear), and current source (saturation). The basic operation of a MOSFET can be understood by considering a long gate length device (i.e. $L_g >> \lambda_n$ where λ_n is the electron mean-free-path). Many textbooks detail MOSFET operation in the long-gate length limit [2]–[4].

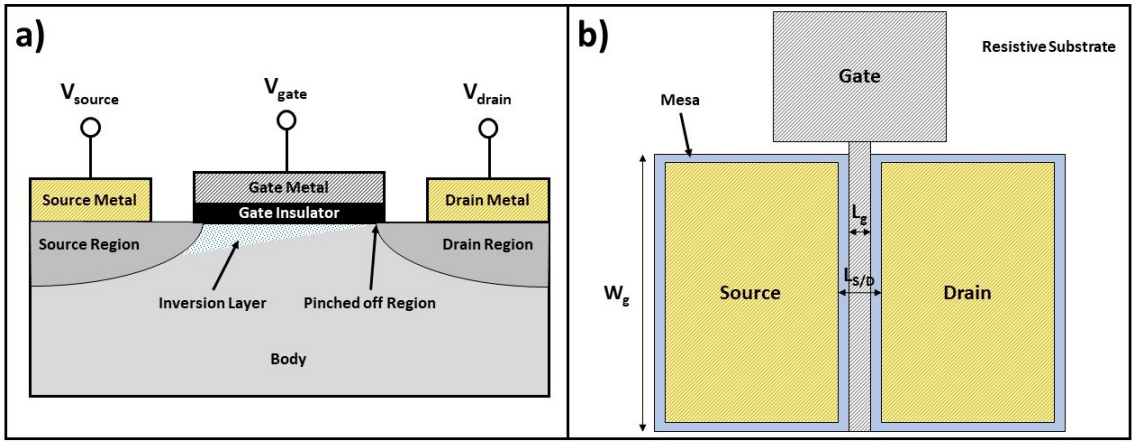

Figure 2.1 a) cross-sectional illustration of long channel MOSFET operating at $V_{DS} = V_{GS} - V_{TH}$ b) top-down view of a typical MOSFET

In the long gate length limit, transistors are simple to describe. A n-channel transistor drain current can be written:

$$I_{DS} = q \cdot n_{ch} \cdot v_n \tag{2.1.1}$$

where q is the elementary charge, n_{ch} is the channel charge density, and v_n is the electron velocity. In the linear region, the transistor is simply a resistor where:

$$n_{ch} = C_{GS}(V_{GS} - V_{TH}) \tag{2.1.2}$$

Where C_{GS} is the intrinsic gate-source capacitance and V_{TH} is the threshold voltage. C_{GS} describes the capacitive coupling of the gate-metal to the surface potential of the semiconductor and is described in more detail in **Section D**. The threshold voltage can be thought of as the voltage required to make the channel conductive. For long gate length, thick oxide devices, $C_{GS} \approx C_{ox}$. If the gate length (L_g) is much longer than the electron mean-free-path, implying many scattering events occur within the channel, electron mobility (μ_n) can be used to describe the velocity:

$$v_n = \mu\mathcal{E} = \mu\frac{V_{DS}}{L_g} \tag{2.1.3}$$

where $\mathcal{E}$ is the lateral electric field and V_{DS} is the drain-source voltage. The electron mobility describes the dependence of electron velocity on electric field inside the semiconductor, in the direction of current flow. The channel potential is therefore lower at the drain edge than at the source edge. Combining equations (2.1.1) – (2.1.3) and integrating the channel potential from source-to-drain, we get the familiar expression:

$$\frac{I_{DS,lin}}{W_g} = \left(\frac{q\mu C_{ox}}{L_g}\right) \cdot \left[(V_{GS} - V_{TH}) \cdot V_{DS} - \frac{{V_{DS}}^2}{2}\right] \tag{2.1.4}$$

Simply put – in the linear region, a MOSFET is a resistor where the lateral field, from source-to-drain is modulated by applying V_{DS}. The resistance of the channel is modulated by increasing or decreasing the channel charge density which is done by modulating ($V_{GS} - V_{TH}$). **Figure 2.2** illustrates an ideal long gate length, MOSFET transfer and output characteristics.

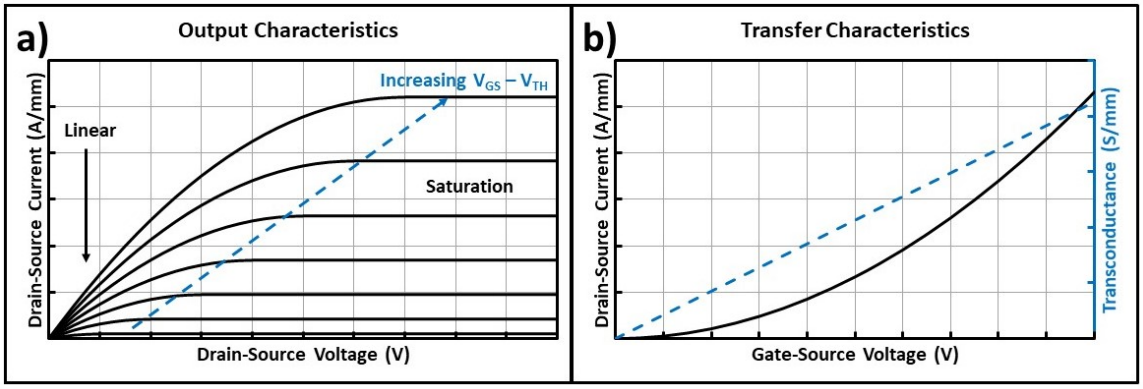

Figure 2.2 Ideal long L_g MOSFET a) output characteristics b) transfer characteristics at large V_{DS} (saturation region)

If a large V_{DS} is applied, the drain side depletion region will begin to encroach on the channel. When the channel-surface potential at the drain edge of the gate is reduced below V_{TH}, the channel is "pinched off", illustrated in **Figure 2.1**. Beyond this point, all additional applied V_{DS} drops across the drain-side depletion region. Applying more drain voltage does not result in more current beyond this point as the lateral electric field, beneath the channel,

is saturated. This is called the saturation regime – where the transistor behaves as a current source – and occurs when $V_{DS} \geq (V_{GS} - V_{TH})$. Equation (2.1.4) then becomes:

$$\frac{I_{DS,sat}}{W_g} = \left(\frac{q\mu C_{ox}}{L_g}\right) \cdot \frac{(V_{GS} - V_{TH})^2}{2} \tag{2.1.5}$$

Transconductance is a metric analogous to gain and describes how well a voltage on the gate modulates the conductivity of the overall device:

$$g_m \equiv \frac{dI_D}{dV_{GS}} \tag{2.1.6}$$

Using equation (2.1.5) and (2.1.6):

$$g_m = \left(\frac{q\mu C_{ox}}{L_g}\right) \cdot (V_{GS} - V_{TH}) \tag{2.1.7}$$

Transconductance is linear when the transistor is operating in saturation mode and increases without bound. The transfer characteristics and transconductance of an ideal, long L_g MOSFET are illustrated in **Figure 2.2b**.

The final regime of interest for MOSFETs is the thermionic region, often referred to as subthreshold. Below threshold, the Fermi level (E_F) is far below the channel conduction band minimum and the channel charge density is dominated by thermal physics. When $E_F << E_C$ the carrier concentration can be described using Boltzmann statistics:

$$n_{ch} = N_C \exp\left(\frac{-(E_C - E_F)}{k_B T}\right) \tag{2.1.8}$$

Where k_B is the Boltzmann constant, T is the device junction temperature, and N_C is the conduction band effective density of states. In this regime, the current is controlled by the rapidly changing channel charge density. Relating the channel surface Fermi-level position to the gate-voltage, using $(E_C - E_F) = q \bullet (V_{GS} - V_{TH})$, we can write:

$$\frac{I_{DS}}{W_g} = I_0 \exp\left(\frac{q(V_{GS} - V_{TH})}{mk_B T}\right) \tag{2.1.9}$$

where I_0 is the "dark current" and m describes the degree of gate capacitive coupling to the channel's surface potential. Any capacitor in parallel with the gate-oxide and source will result in $m > 1$.

B. Subthreshold Slope & Interface Defects

Subthreshold slope (SS) is a figure-of-merit (FOM) commonly used to characterize the thermionic region of operation and describe the off-state performance of a MOSFET:

$$SS \equiv \left[\frac{d(\log_{10} I_D)}{dV_{GS}}\right]^{-1} \tag{2.2.1}$$

Subthreshold slope is usually reported in mV/decade and represents the amount of gate voltage required to modulate the drain current by an order of magnitude. If a significant density of defects (D_{it}) exists at the gate-insulator / semiconductor interface, some V_{GS} will be required to fill / empty these states and SS will increase. Historically it has been difficult to form defect free dielectrics on III-V surfaces [5], [6]. Defects often sit at the oxide / semiconductor interface and manifest themselves as a parallel capacitance (C_{it}) that screens the semiconductor surface potential from the gate potential. Including C_{it}, SS becomes [3]:

$$SS = ln(10)\left(\frac{k_B T}{q}\right)\left(\frac{C_{ox} + C_{it}}{C_{ox}}\right) \tag{2.2.2}$$

Defects at the semiconductor / dielectric interface can be of many different forms: dangling bonds, vacancies, anti-sites, and native oxides [6]. Significant D_{it} can result in Fermi-level pinning which prevents carrier modulation. From [7] and [8], the Fermi level of GaAs is surface pinned for $D_{it} \approx 10^{12} - 10^{13}$ $cm^{-2}eV^{-1}$. Concentrations below this allow carrier modulation but limit the channel conductivity and degrade transistor performance. Defects

can exist in the channel material's bandgap (E_g), valence band (E_V), or conduction band (E_C). Defects that are filled or emptied over the V_{GS} range of interest will affect the performance of the transistor. Spicer *et al.* demonstrated the energy levels of donors and acceptors due to missing atoms and proposed the levels of interfacial states for InP, GaAs, and GaSb [9] – shown in **Figure 2.3**. The energy level of Fermi-level pinning has been calculated for $In_xGa_{1-x}As$ [10] and is also shown in **Figure 2.3**. Recent results of III-V MOSFETs on InAs [11], InGaAs [12], and InP [13] suggest that the defect energy levels that exist inside the semiconductor bandgap are likely more detrimental to *SS* than defects deep in the conduction band.

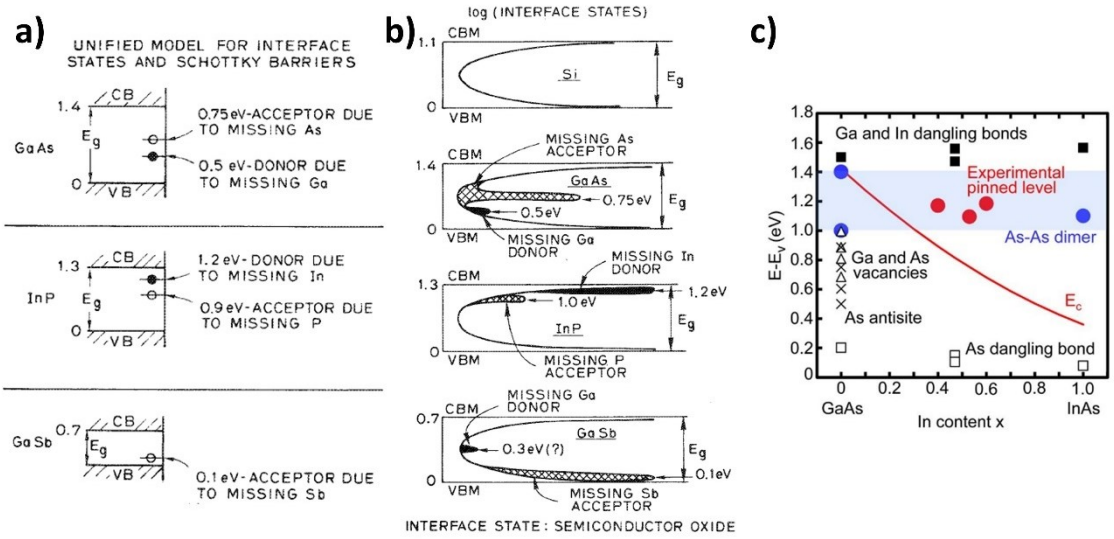

Figure 2.3 a) unified model of interface states and associated Schottky barriers of GaAs, InP, and GaSb. Reprinted with permission from [9]. © 1980 AIP Publishing LLC b) Energy level of interface states of GaAs, InP, and GaSb. Reprinted with permission from [9]. © 1980 AIP Publishing LLC c) Fermi level pinning energy levels relative to valence band maximum for $In_xGa_{1-x}As$ as a function of Indium content. Reprinted with permission from [10]. © Copyright 2013 IEEE

Formation of an oxide can remove Fermi level pinning on Si; III-V oxides move or modify the Fermi-level pinning [14]. Additionally, the mechanism for oxide formation on III-V is

different than on silicon. Oxygen moves through the oxide to form SiO_2 at the Si-oxide interface where III-V atoms move outward to form oxides [15], leaving behind interface defects. Finally, wet chemical treatment can also cause the formation of surface oxides, requiring careful attention be paid to surface preparation prior to high-k formation on III-Vs. In summary, surface and bulk chemistry of the channel material need to be carefully chosen and understood to form a low D_{it} high-k gate dielectric on III-V semiconductors. Surface preparation, treatment, channel material, and choice of high-k gate dielectrics are discussed in detail in [6], [16]–[18].

C. Short-Channel Effects

MOSFETs are two-dimensional devices and thus require 2D electrostatics to be properly described. So far the device has been treated in one-dimension, ignoring the effect of the drain voltage on the channel surface potential. At long gate lengths, only the drain-edge of the channel potential is affected by the drain voltage. As the gate-length is reduced, proportionally more of the channel is coupled to the drain. At extremely short-gate lengths, the gate losses control of the channel potential and the drain dictates device performance.

If the gate length is short compared to the drain-side depletion width, the drain will also modulate the channel surface potential. This encroachment of the drain depletion width into the channel lowers the surface potential which effectively decreases V_{TH}. This effect is referred to as drain-induced-barrier-lowering (DIBL) and is the root of most short channel effects:

$$DIBL \equiv \frac{V_{TH,sat} - V_{TH,lin}}{V_{DS,sat} - V_{DS,lin}} \tag{2.3.1}$$

DIBL is related to the drain-source capacitance (C_{DS}) and causes threshold voltage roll-off, increase in subthreshold slope, and output conductance modulation. At long gate lengths,

C_{DS} / C_{ox} is small so short channel effects are small. As the gate length decreases, C_{DS} / C_{ox} increases because C_{ox} decreases and the drain begins to modulate the channel surface potential.

Subthreshold slope increases because the drain-channel modulation prevents ideal gate-channel modulation. Output conductance modulation occurs because of the encroachment of the drain-side depletion width into the gated region. Beyond pinch-off, additional V_{DS} further depletes the drain-side, lowering the source-channel barrier under the gate. This effectively shortens the gate-length. If the depleted region is a significant portion of the nominal gate-length, the output conductance increases.

To improve short-channel effects, a MOSFET must be designed so that the gate has stronger capacitive coupling than the drain. Brews *et al.* derived empirical formulas for inversion mode FETs and provided guidance regarding the aspect ratios where devices would begin to suffer from short-channel effects [19]. Planar inversion mode FETs generally have better electrostatic coupling when the substrate doping is high, creating a more tightly confined inversion layer. However, this technique creates another capacitive term which can further reduce *SS* and increase *RC* charging times. Consequently, other confinement techniques are desired. Confinement of channel carriers can be achieved by using hetero-barriers (common to HEMTs) or oxides (common to SOI or III-V on insulator) as the channel back-barrier. A commonly used parameter to characterize the 2D electrostatics in a MOSFET is the natural length (λ):

$$\lambda = \sqrt{\frac{\varepsilon_{ch}}{N\varepsilon_{ins}} t_{ins} t_{ch}} \tag{2.3.2}$$

where N is the number of gate fingers, ε_{ch} , ε_{ins} is the dielectric permittivity of the channel and gate-insulator respectively, and t_{ins} , t_{ch} are the thicknesses of the gate-insulator and

channel respectively. The natural length describes the ratio of the electrostatic strength of the gate and drain and depends on the structure of the device. A smaller natural length implies better gate control. Double-gates, finFETs, and gate-all-around structures have smaller λ than a planar FET. Generally, a transistor should be designed so $\lambda > 5$ to mitigate short-channel effects. Because III-V materials have large dielectric permittivity (ε_{ch}), a III-V channel of a given geometry will have worse electrostatics than a Si device.

D. Gate-Channel Capacitance

Gate control of the channel is the foundation of MOSFET operation. In previous sections, $C_{GS} = C_{GS,i} = C_{g\text{-}ch}$ was used to describe the capacitive coupling of the gate potential to the channel charge density. A larger gate-channel capacitance results in more charge for the same applied gate-voltage.

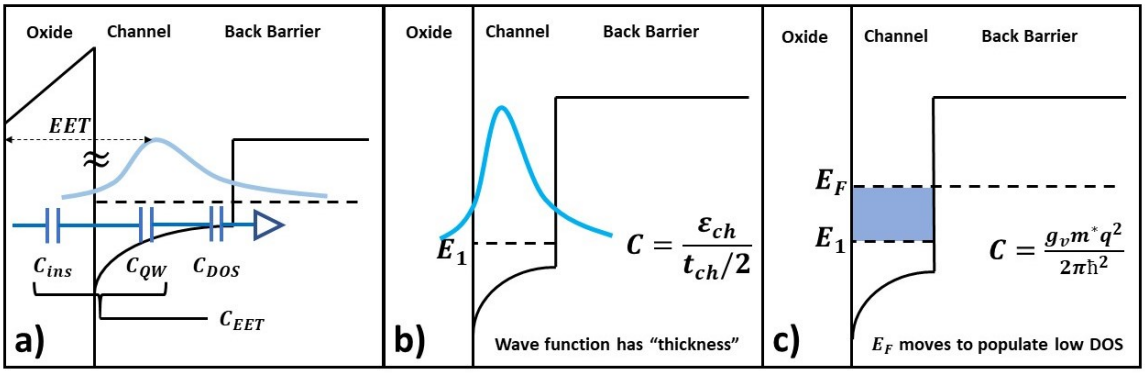

Figure 2.4 illustration of a) the gate-channel series capacitance b) C_{QW} and c) C_{DOS}

The total Gate-Channel capacitance ($C_{GS,i}$) in a highly scaled quantum well device is series combination of 3 capacitors, illustrated in **Figure 2.4**.

$$C_{GS,i}{}^{-1} = C_{ins}{}^{-1} + C_{QW}{}^{-1} + C_{DOS}{}^{-1} \tag{2.4.1}$$

Where C_{ins} is that gate insulator capacitance, C_{QW} is the wave-function capacitance (referred to as the quantum well capacitance in this thesis), and C_{DOS} is the density of states

capacitance. The gate insulator capacitance is the most discussed and is simply the parallel plate capacitance that a MOSFET is usually designed around. C_{QW} arises due to the spatial separation of the channel electron wave-function from the insulator / semiconductor interface:

$$C_{QW} \approx \frac{\varepsilon_{ch}}{t_{ch}/2} \tag{2.4.2}$$

C_{DOS} occurs because the channel Fermi-level must move to provide charge. Because the density of states is low for low effective mass materials, the resulting capacitance is small:

$$C_{DOS} = \frac{d(qN_S)}{d\left(\frac{E_F - E_1}{q}\right)} = \frac{g_v \frac{q^2 m^{*2}}{\pi \hbar^2}}{1 + \exp\left(-\frac{E_F - E_1}{k_B T}\right)} \tag{2.4.3}$$

where g_v is the electronic band degeneracy. In the highly degenerate limit (i.e. when the channel is strongly inverted):

$$\lim_{(E_F - E_1)\to\infty} \exp\left(-\frac{E_F - E_1}{k_B T}\right) = 0$$

Then:

$$C_{DOS} = g_v \frac{q^2 m^{*2}}{\pi \hbar^2} \tag{2.4.4}$$

Because series capacitors result in an overall smaller capacitance, $C_{GS,i}$ in highly scaled III-V devices are limited by C_{DOS}. Because the electrostatic gate control vs. drain control is important for both VLSI (*SS* and DIBL) and RF devices (g_m/g_{ds}), the electrostatic terms can be grouped:

$${C_{EET}}^{-1} = {C_{ins}}^{-1} + {C_{QW}}^{-1} \tag{2.4.5}$$

E. Ideal Ballistic MOSFET Theory

MOSFETs exhibit current saturation for two reasons: 1) $\mathcal{E}$ saturation when the drain-depletion width encroaches into the gated-region or 2) v_n saturation where electrons cannot

travel faster despite an increased lateral electric field. Long gate length devices exhibit current saturation due to $\mathcal{E}$ saturation while short channel devices experience v_n saturation. The above described drift-diffusion model does not accurately describe MOSFETs with extremely small gate lengths. Modern transistors have gate lengths of order or smaller than the electron mean free path (λ_n). Consequently, electrons can travel from source-to-drain without scattering. In previous chapters, MOSFET performance depended heavily on mobility. Mobility is defined $\mu = q\tau/m^*$ where τ is the mean scattering time, q is the elementary charge, and m^* is the effective mass. If we assume that no scattering occurs between source and drain, mobility is not a meaningful parameter. Instead, the $E(k)$ diagram of the channel material can be used to describe the maximum electron velocity. The resulting ballistic FET model has been widely investigated [20]–[23].

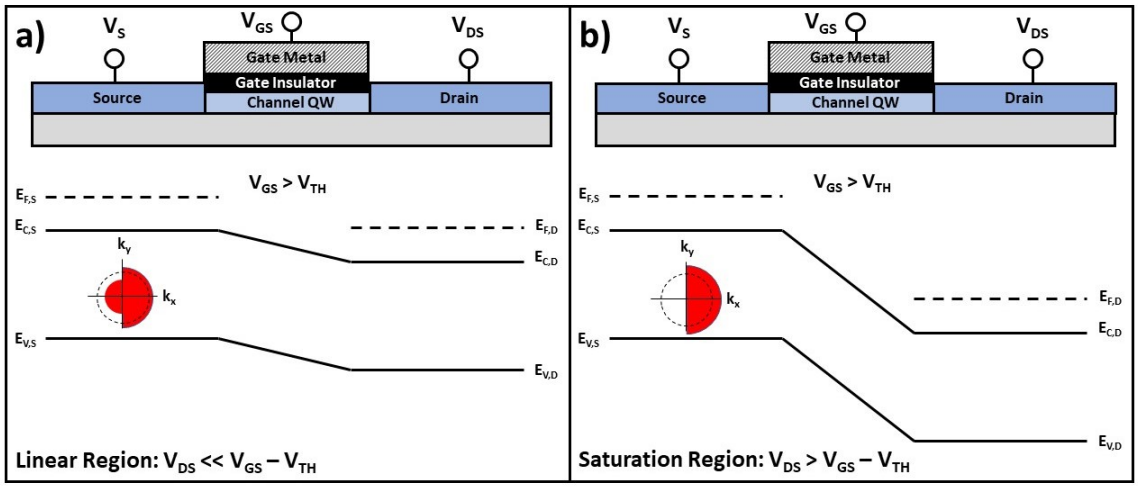

Figure 2.5 Band diagrams of ballistic FET a) low V_{DS} b) high V_{DS}

Figure 2.5 illustrates the band diagrams for a ballistic FET at low and high V_{DS}. The circles in the source electrode illustrate the population of k_x , k_y for a given bias. Because a bias is applied in x, the electrons redistribute in k-space. More positive k_x states are populated, so current flows in x^+. At low V_{DS}, $E_{F,D}$ remains above the channel eigenstate (E_1) and electrons

can flow in both directions. The current is then the sum of the positively moving electrons from the source and negatively moving electrons from the drain:

$$I_{DS} = I_S{}^{+} + I_D{}^{-} \tag{2.5.1}$$

When a large V_{DS} is applied, $E_{F,D}$ drops below E_1 and no backward moving electrons can transmit from drain-to-source. The current is then dictated only by positively moving electrons from the source:

$$J_S{}^{+} = qn_S\left(E_{F,S} - E_1\right)v_S\left(E_{F,S} - E_1\right) \tag{2.5.2}$$

Where n_S is the sheet carrier density of the channel and v_S is the injection velocity as dictated by the source-electrode. Both n_S and v_S are determined by the source $E(k)$ diagram and are thus a function of $(E_{F,S} - E_{1,ch})$. The electron density can be calculated:

$$n_S = \frac{N_{2D}}{2}F_0 = \frac{N_{2D}}{2}\ln\left(1 + exp\left(\frac{E_{F,S} - E_1}{k_B T}\right)\right) \tag{2.5.3}$$

Where F_0 is the zero-order Fermi-Dirac integral and N_{2D} is the two-dimensional density of states of the channel quantum well. It is divided by two as only electrons moving in x^+ contribute to the drain current. The electron velocity is calculated as:

$$v_S = \frac{\sum_{k_x>0,k_y} v_x f_0\left(E_{F,S} - E_1\right)}{\sum_{k_x>0,k_y} f_0\left(E_{F,S} - E_1\right)} \tag{2.5.4}$$

Where v_x is the band-limited, x-directed velocity component of each state and f_0 is the zero-order Fermi-Dirac occupancy function. The velocity changes as a function of energy; to properly account for this, the velocity at a given point must be weight by the probability of electron occupancy at that point. Assuming parabolic bands of the form $(E_{F,S} - E_{1,ch}) = (\hbar k)^2/2m$ and $v = (1/\hbar)(\mathrm{d}E/\mathrm{d}k)$ then $v_x = \hbar k_x/m^*$. The expression for v_s can be simplified in the highly degenerate case, $E_{F,S} >> E_1$ using a 0 K approximation. Because the source is degenerately doped, thermal fluctuations are small compared to the carrier density and can

thus be ignored. In this case, electrons move with an average velocity that is the centroid of the positively facing semi-circle in k_x , k_y:

$$\langle v_{S,deg} \rangle = \frac{4}{3\pi} \frac{\hbar k_f}{m^*} \tag{2.5.5}$$

Where $<v_{s,deg}>$ is the average velocity in the degenerate limit and k_f is the k-state at the Fermi-level. We can also write the expression for $n_{S,deg}$:

$$n_{s,deg} = \frac{D_{2D}}{2}\left(E_{F,S} - E_1\right) = \frac{D_{2D}}{2}\frac{\hbar^2 {k_f}^2}{2m^*} \tag{2.5.6}$$

With $D_{2D} = m^* k_B T/\pi\hbar^2$ and $[C_{EET}/(C_{EET} + C_{DOS})](V_{GS} - V_{TH})$, combining equations (2.1.1), (2.1.2), and (2.5.5), we can write:

$$J_{ballistic} = q \cdot C_{GS}(V_{GS} - V_{TH}) \cdot \frac{4}{3\pi}\frac{\hbar k_f}{m^*} \tag{2.5.6}$$

Accounting for the voltage divider between the electrostatic gate control and C_{DOS}, we can substitute in the total expression for $C_{GS} = C_{EET} \bullet C_{DOS}/(C_{EET} + C_{DOS})$, relating k_f to $(V_{GS} - V_{TH})$, and simplifying:

$$J_{ballistic} = q \cdot \frac{C_{EET} \cdot C_{DOS}}{C_{EET} + C_{DOS}}(V_{GS} - V_{TH}) \cdot \frac{4}{3\pi}\sqrt{\frac{2q\frac{C_{EET}}{C_{EET} + C_{DOS}}(V_{GS} - V_{TH})}{m^*}} \tag{2.5.7}$$

The fundamental components can then be separated from the material dependent components (i.e. anything dependent on effective mass) [23]:

$$J_{ballistic} = J_0 K_1 \left(\frac{V_{GS} - V_{TH}}{1V}\right)^{\frac{3}{2}} \tag{2.5.8}$$

Where J_0 is the fundamental current:

$$J_0 = \sqrt{\frac{2q}{m_0}}\left(\frac{4}{3\pi}\right)\left(\frac{q^2 m_0}{2\pi\hbar^2}\right)(1V)^{\frac{3}{2}} \tag{2.5.9}$$

And K_1 is the normalized drive current:

$$K_1 = n\sqrt{\frac{m^*}{m_0}}\left(1+\left(\frac{C_{DOS}}{C_{EET}}\right)g_v\left(\frac{m^*}{m_0}\right)\right)^{-3/2} \tag{2.5.10}$$

Figure 2.6 shows a plot of K_1 at various channel thicknesses using a 5 nm $In_{0.52}Al_{0.48}As$ gate insulator (common to III-V HEMTs) and a 2 nm ZrO_2 gate insulator (common to III-V MOSFETs). Because C_{EET} depends on both C_{QW} and C_{ins}, it is important to specify ε_{ins}, t_{ins} and ε_{ch}, t_{ch}. Low effective mass materials are limited by their low density of states and correspondingly low channel charge densities; high effective mass materials are limited by low injection velocity. For a given channel thickness, there is an optimal channel effective mass. From **Figure 2.6**, thin channels can realize higher I_{DS} than thick channels.

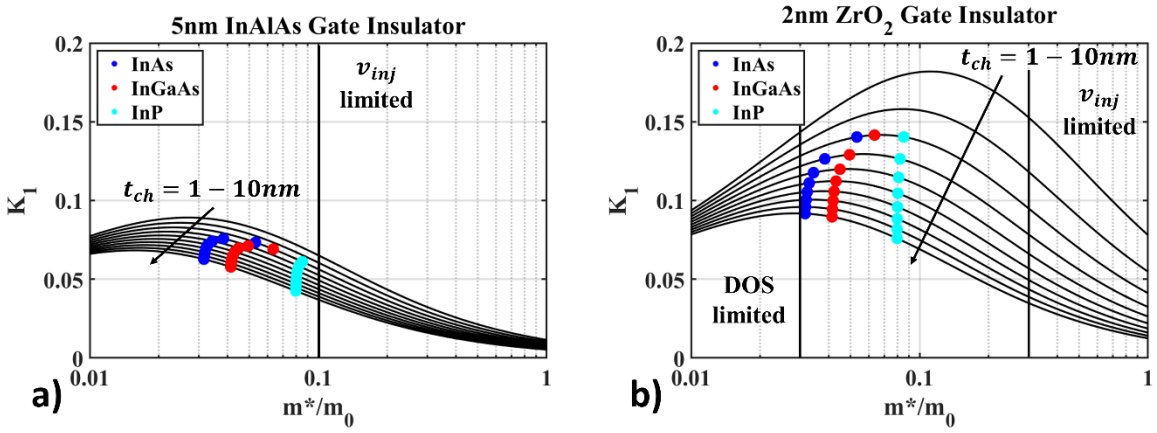

Figure 2.6 Normalized drive current as a function of channel effective mass for a) 5 nm $In_{0.52}Al_{0.48}As$ gate insulator b) 2 nm ZrO_2 gate insulator

State-of-the-art HEMTs [24]–[26] use high indium content channels with t_{ch} = 8 – 10 nm and 5 nm $In_{0.52}Al_{0.48}As$ gate insulators. For the associated, relatively low C_{EET}, $In_{0.53}Ga_{0.47}As$ and InAs have near optimum effective mass. Because the 2 nm ZrO_2 high-k gate dielectric facilitates larger C_{EET}, the normalized drive current increases; however, the optimal effective mass is larger suggesting channel materials like InP or GaAs are preferred for extremely thin channel MOSFETs.

F. Channel Quantum Well

Normalized drive current suggests thinner channels are always better. However, as the channel is thinned, the narrow E_g semiconductor is quantum confined between the gate insulator and the wide E_g back barrier. The quantum confinement results in the formation of discreet energy levels in the channel quantum well. Because the maximum ($E_F - E_1$) that the channel can be inverted to occurs when E_F is equal to the conduction band minimum in the wide E_g back barrier, the energy of E_1 is critical. Normalized drive current K_1 compares channels of a given thickness at ($V_{GS} - V_{TH}$) = 1 V. Commonly used channel material systems ($In_{0.53}Ga_{0.47}As$ | $In_{0.52}Al_{0.48}As$ and pseudomorphic InAs | $In_{0.52}Al_{0.48}As$) do not have the same band-offsets and therefore must compared at their maximum available ($E_F - E_1$). For example, an $In_{0.53}Ga_{0.47}As$ | $In_{0.52}Al_{0.48}As$ device has a conduction band offset ≤ 0.5 eV while a pseudomorphic InAs | $In_{0.52}Al_{0.48}As$ has a conduction band offset ≤ 0.7 eV. Additionally, different channel materials have different m^* which determines how quickly E_1 increases as t_{ch} is decreased. To first order, the Eigenstates can be estimated using an infinite potential approximation [27], [28]:

$$E = \frac{\hbar^2 k^2}{2m^*} = \frac{\hbar^2 k^2}{2m^*}\left(\frac{n\pi}{t_{ch}}\right)^2 \tag{2.6.1}$$

Because $E \propto 1/t_{ch}^2$ the eigenstate energy grows quickly as the channel is thinned. Additionally, $E \propto 1/m^*$ meaning that small effective mass materials will exhibit larger E_1 for a given channel thickness. In a real MOSFET, the eigenstate energy will vary more slowly than this because it exists in a finite quantum well. Because the conduction band-offset of the channel to the oxide is extremely large (≥ 3.0 eV), a MOSFET can be treated as a single-sided well. The time-independent Schrodinger equation can be used solve for the electron energy levels in a quantum well system [27], [28]:

$$-\frac{\hbar^2}{2m}\nabla^2\varphi + V(x,y,z)\varphi = E\varphi \tag{2.6.2}$$

For simplicity, only 1D wells will be considered: $\nabla^2 \rightarrow \frac{\partial^2}{\partial x^2}$ and $V(x,y,z) \rightarrow V(x)$.

$$-\frac{\hbar^2}{2m}\frac{\partial^2\varphi}{\partial x^2} + V(x)\varphi = E\varphi \tag{2.6.3}$$

This is a wave equation and has solutions:

$$\varphi = Ae^{-ikx} + Be^{ikx} \tag{2.6.4}$$

When $E > V(x)$, k is real and the solution is either a standing wave or a propagating wave and when $E < V(x)$, k is imaginary and the wave-function is an exponential decay or growth. Because the oxide side of the well is approximated as an infinite potential, the boundary condition at $x = 0$ is $\varphi_{ch}(0) = 0$. There is no requirement on the first derivative as the infinite potential will cause a discontinuity. Because the semiconductor back-barrier is a small potential barrier, the electron wave-function can leak into it. If the eigenstate energy becomes larger than the confining potential, then it is no longer a bound state. Because a quantum well FET requires the electrons to be confined, we will use E_1 = CBO as an upper limit to our analysis and not consider the free electron case. The boundary conditions are then:

$$\varphi_{ch}(x = t_{ch}) = \varphi_{BB}(x = t_{ch})$$

$$\varphi_{ch}'(x = t_{ch}) = \varphi_{BB}'(x = t_{ch})$$

$$\varphi_{BB}(x = \infty) = 0$$

Because $\varphi_{ch}(0) = 0$, the solution in the channel quantum well must be $\varphi_{ch} = A \bullet \sin(k_{ch} \bullet x)$ while the requirement that $\varphi_{BB}(\infty) = 0$ gives $\varphi_{BB} = B \bullet \exp(\kappa_{BB} \bullet x)$. Applying the wave-function and first derivative continuity requirements at the Channel / Back-barrier interface:

$$Asin(k_{ch}x) = Bexp(-\kappa_{BB}x) \tag{2.6.5}$$

$$Ak_{ch}cos(k_{ch}x) = -B\kappa_{BB}exp(-\kappa_{BB}x) \tag{2.6.6}$$

Dividing equation (2.6.5) by equation (2.6.6):

$$tan(k_{ch}x) = -\frac{k_{ch}}{\kappa_{BB}} \tag{2.6.7}$$

which can be solved iteratively. Assuming no band-bending in the quantum well, the maximum ($E_F - E_1$) is now known. C_{QW} can be determined more precisely than in equation (2.4.2) by calculating the centroid of the wave-function. With the Eigenstates determined, the wave function can be completely described after normalization:

$$\int_{-\infty}^{\infty} |\varphi(x)|^2 dx = 1 \tag{2.6.8}$$

$$\int_{0}^{t_{ch}} Asin^2(k_{ch}x)dx + \int_{t_{ch}}^{\infty} Bexp(2\kappa_{BB}x)dx = 1 \tag{2.6.9}$$

The maximum ballistic drive current and transconductance can be evaluated for the condition E_F = CBM of the back-barrier (BBCBM). The in-plane effective mass increases for quantum confined structures [29]. Band offsets were extracted from BandProf. Future efforts to refine the below calculations should include more rigorous material band diagram calculations and better band offset estimation such as those reported in [29].

The conduction band is isotropic around Γ for III-Vs but anisotropic near L and X. To properly treat the satellite valleys the anisotropy of the bands must be considered. However, from equation (2.6.1), the heaviest effective mass orientation will move the slowest. The other orientations will increase in energy more quickly, splitting the originally degenerate bands into sub-bands. The lowest energy sub-band is conservatively estimated by simply solving the single-sided quantum well using the maximum bulk values of m_L^* and m_X^*. **Figure 2.7** shows the calculate eigenstate energies of the Γ, L, and X valleys as well as peak $g_{m,i}$ and I_{DS} of InAs, $In_{0.53}Ga_{0.47}As$, and InP channel devices with an $In_{0.52}Al_{0.48}As$ back-barrier, common in III-V FETs and HEMTs.

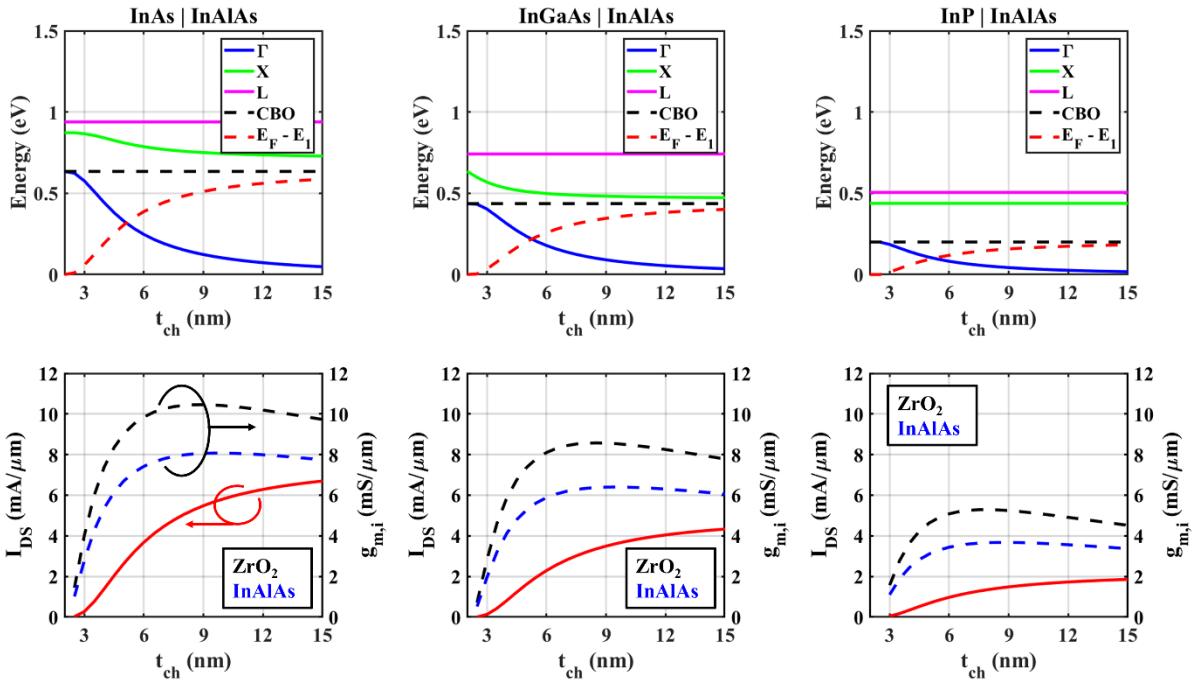

Figure 2.7 InAs, $In_{0.53}Ga_{0.47}As$, and InP channels on $In_{0.52}Al_{0.48}As$ a) Eigenstate energies (Γ, L, X) b) Peak ballistic I_{DS} and $g_{m,i}$ using 0.5 nm $Al_xO_yN_z$ / 1.5 nm ZrO_2 high-k gate dielectric and 5.0 nm $In_{0.52}Al_{0.48}As$ gate dielectric, note I_{DS} is independent of gate insulator.

In all cases, both I_{DS} and $g_{m,i}$ increase as the channel thickness increases and saturates, decreasing for $t_{ch} \geq 8.0$ nm. Peak $g_{m,i}$ occurs at $t_{ch} = 9.0$, 8.5, 8.0 nm for InAs, $In_{0.53}Ga_{0.47}As$, and InP channels respectively. Thin channel devices are primarily limited by large $E_{1,ch}$ which limits the maximum ($V_{GS} - V_{TH}$), not v_{inj} or DOS. InAs exhibits larger I_{DS} and $g_{m,i}$ than $In_{0.53}Ga_{0.47}As$ and InP because of the larger CBO. InAs, $In_{0.53}Ga_{0.47}As$ and InP channel devices can all be inverted to the BBCBM without interacting with satellite valleys. The L-valleys of InAs and $In_{0.53}Ga_{0.47}As$ are located < 100 meV above the BBCBM while the L-valley of InP is located 240 meV above the BBCBM suggesting that wider E_g back-barriers can provide substantial performance improvement for InP devices but not InAs or $In_{0.53}Ga_{0.47}As$ devices.

To validate the above calculations, we compare against a multitude of reported III-V FETs. Huang *et al.* reported on 3 nm thick InAs and $In_{0.53}Ga_{0.47}As$ MOSFETs [18] and showed

that I_{DS} and $g_{m,e}$ of InAs devices were nearly double that of $In_{0.53}Ga_{0.47}As$ devices. Lee *et al.* reported 6 nm InAs channel devices exhibiting $g_{m,e}$ = 3.0 mS/μm [30]. Values reported in [18] correspond to $g_{m,i}$ = 2.9 mS/μm and 1.7 mS/μm for InAs and $In_{0.53}Ga_{0.47}As$ channel devices respectively while those reported in [30] correspond to $g_{m,i}$ = 4.4 mS/μm assuming g_{ds} = 0.2 mS/μm. The above calculations over-estimate $g_{m,i}$ for both thin and thick channels. For simplicity, the above calculations were done without a self-consistent Schrödinger-Poisson solver and thus neglect the strong band-bending exhibited at the oxide-semiconductor interface. For extremely thin-channel devices similar to [18], band-bending will increase the effective quantum well depth which will increase the available ($E_F - E_1$) resulting in larger n_{ch}. For thick channel devices, n_{ch} can exceed 2 x 10^{12} cm^{-2} and source-starvation can limit g_m. The general trend of peak $g_{m,i}(t_{ch})$ was reported by Lin *et al.* for high Indium content channel devices and found that maximum $g_{m,i}$ occurred for t_{ch} = 9.0 nm [31], in excellent agreement with the above calculations. **Figure 2.7** suggests that both I_{DS} and $g_{m,i}$ slowly decrease in the thick channel limit; however, [31] observed a steep drop in $g_{m,i}$. The authors attribute the fast drop-off in $g_{m,i}$ to poor electrostatics and the onset of short-channel effects which are neglected in the above treatment. Additionally, $t_{ch} \geq$ 10 nm devices detailed in [31] are fabricated with high-k on InP. Compared to high-k on $In_xGa_{1-x}As$ devices in the same study, long L_g minimum *SS* is higher suggesting high D_{it}. It should also be noted that all devices reported in [31] exhibit long gate length *SS* > 80 mV/dec and likely exhibit less than ideal DC $g_{m,i}$ due to high D_{it}. The trend of channel thickness and $g_{m,i}$, rather than the specific values, is of primary interest.

Despite the deviation of this simplified approach, the observed trend matches literature and it is therefore of interest to consider how much the performance can be improved if a material with a larger CBO were used as the back-barrier. **Figure 2.8** shows the eigenstate

energies of the *Γ, L,* and *X* valleys as well as peak $g_{m,i}$, and I_{DS} of InAs, $In_{0.53}Ga_{0.47}As$, and InP channel devices with an $AlAs_{0.56}Sb_{0.44}$ back-barrier.

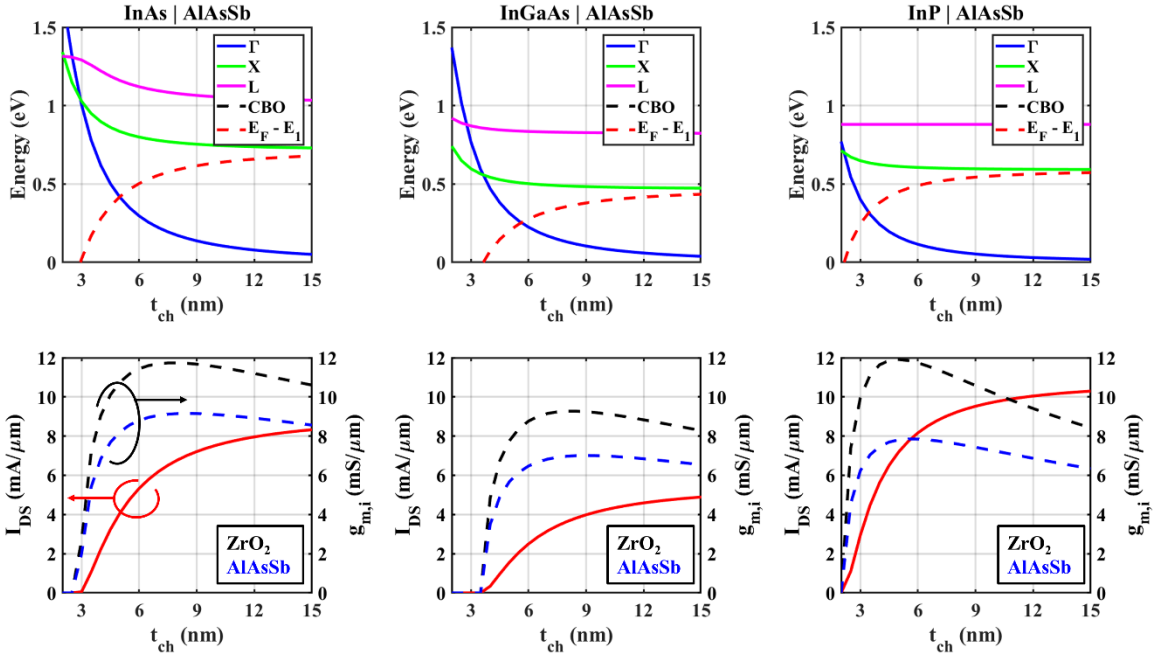

Figure 2.8 InAs, $In_{0.53}Ga_{0.47}As$, and InP channels on $AlAs_{0.56}Sb_{0.44}$ a) Eigenstate energies (*Γ*, *L*, *X*) b) Peak ballistic I_{DS} and $g_{m,i}$ using 0.5 nm $Al_xO_yN_z$ / 1.5 nm ZrO_2 high-k gate dielectric and 5.0 nm $AlAs_{0.56}Sb_{0.44}$ gate dielectric, note I_{DS} is independent of gate insulator.

In all cases, both I_{DS} and $g_{m,i}$ increase as the channel thickness increases and then saturates and slowly, decreases beyond some maximum. Peak $g_{m,i}$ occurs at t_{ch} = 8.0, 8.0, and 5.0 nm for InAs, $In_{0.53}Ga_{0.47}As$, and InP channels respectively. Peak $g_{m,i}$ is larger and has shifted to thinner t_{ch} compared to $In_{0.52}Al_{0.48}As$ back-barrier devices. Increased g_m and decreased g_{ds} can therefore be realized simultaneously. Because maximizing both f_τ and f_{max} is desired, t_{ch} that significantly reduces g_{ds} while only moderately reducing $g_{m,i}$ is preferred. Peak $g_{m,i}$ is 11.7, 9.2, and 11.9 mS/μm while devices reach 90% of peak $g_{m,i}$ at t_{ch} = 5.0, 5.5, and 3.5 nm for InAs, $In_{0.53}Ga_{0.47}As$, and InP channels respectively.

Again, ultra-thin channel devices are primarily limited by the large eigenstate energy while thick channel devices are limited by reduced $C_{g\text{-}ch}$. InAs and $In_{0.53}Ga_{0.47}As$ devices with

$AlAs_{0.56}Sb_{0.44}$ back-barriers do not exhibit significant improvement compared to $In_{0.52}Al_{0.48}As$ back-barriers due to intervalley scattering. Interestingly, because of the increased CBO and later onset of intervalley scattering, InP | $AlAs_{0.56}Sb_{0.44}$ devices exhibit performance comparable to InAs channel devices. InAs MOSFETs have low breakdown voltage (V_{br}) due to InAs's narrow E_g which limits power output. A device with similar performance and larger V_{br} is desirable for high-power, low-noise applications. Therefore, an InP | $AlAs_{0.56}Sb_{0.44}$ MOS-HEMT capable of $g_{m,i} \geq 4.0$ mS/μm would be of significant interest.

In summary, based on normalized drive current (K_1) InP channel devices should perform similarly to $In_xGa_{1-x}As$ and InAs channel devices, despite significant evidence against it. Historically, high indium content channels have been used with the justification that their low m^* and high v_{inj} facilitates improved performance. However, highly scaled HEMTs are predominately limited by parasitic and extrinsic capacitances [25], [32] and thus require scaling of g_m rather than L_g/v_{inj}. Elementary quantum mechanics requires $E_{1,ch}$ to increase as the t_{ch} decreases, resulting in an optimal channel thickness where large $C_{g\text{-}ch}$ and large available ($V_{GS} - V_{TH}$) are balanced. Use of a wider E_g back-barrier material provides more ($E_F - E_1$) at a given t_{ch} and facilitates larger I_{DS} and $g_{m,i}$. Performance is then limited by satellite valley scattering rather than loss of confinement.

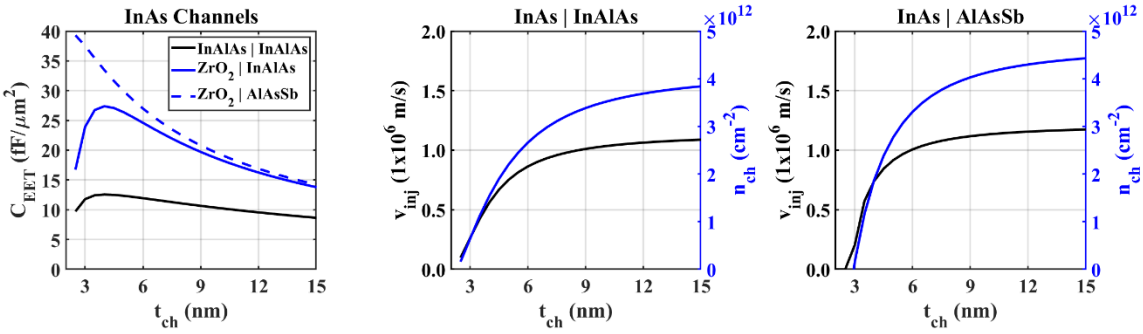

Figure 2.9 (left) CEET for InAs channels for HEMT, FET with $In_{0.52}Al_{0.48}As$ back-barrier, and FET with $AlAs_{0.56}Sb_{0.44}$ back-barrier and peak n_{ch} and v_{inj} for InAs channel devices with (middle) $In_{0.52}Al_{0.48}As$ back-barrier and (right) $AlAs_{0.56}Sb_{0.44}$ back-barrier

As a final note, the source 2DEG must be engineered to have twice the number of carriers that the intrinsic transistor requires at peak inversion. The total amount of carriers in the 2DEG ($k_x^{\pm}$, $k_y^{\pm}$) do not contribute to current in the transistor, as illustrated in **Figure 2.5**. Only positively moving k_x^{+} carriers contribute such that $n_{2DEG} \geq n_{ch} / 2$ to realize the above predicted values. If n_{2DEG} does not meet this requirement, source-starvation will limit $g_{m,max}$. Calculated peak n_{ch} and average v_{inj} for InAs channel devices are shown in **Figure 2.9**.

We acknowledge many approximations were made in these calculations. More sophisticated simulations and cursory experimental work should be explored.

G. Increasing f_τ and f_{max}

The figures of merit (FOM) f_τ and f_{max} are often used to determine the maximum bandwidth of a transistor. The current-gain-cutoff-frequency (f_τ) is defined as the frequency where the small-signal, short-circuit current gain $|h_{21}|^2 = 0$ dB. The power-gain-cutoff-frequency (f_{max}) is defined as the frequency where Mason's unilateral power gain $U = 0$ dB. Both values can be described directly with Y-parameters [33]:

$$|h_{21}| = \left|\frac{i_{out}}{i_{in}}\right| = \left|\frac{Y_{21}}{Y_{11}}\right| \tag{2.7.1}$$

$$U = \frac{|Y_{21} - Y_{12}|^2}{4[Re(Y_{11})Re(Y_{22}) - Re(Y_{12})Re(Y_{21})]} \tag{2.7.2}$$

Because both values describe gain, the natural question is how much gain is necessary to design efficient amplifiers and, therefore, how high do f_τ and f_{max} need to be? Since f_τ and f_{max} are proportional to $1 / (1 + \omega^2)$ they decay at 20 dB/dec. Assuming 10 dB of small-signal gain is enough and an operating frequency (f_{op}) of 100 GHz, then f_τ , f_{max} = 350 GHz is sufficient.

Increasing f_{op} to 300 GHz requires f_τ , $f_{max} \geq 1$ THz . Further increasing the cutoff frequencies increases the amount of gain available at a given f_{op}.

Gain is critical for amplifier design because it determines the efficiency. Two measures of efficiency are commonly used: drain efficiency (DE) and power added efficiency (PAE). Drain efficiency is defined as:

$$DE = \frac{P_{RF,out}}{P_{DC}} \tag{2.7.3}$$

Where $P_{RF,out}$ is the RF output power and P_{DC} is the DC power. Power added efficiency is defined as:

$$PAE = \frac{P_{RF,out} - P_{RF,in}}{P_{DC}} \tag{2.7.4}$$

where $P_{RF,in}$ is the RF input power. The two values can be related:

$$PAE = \frac{P_{RF,out} - P_{RF,in}}{P_{DC}} = \frac{P_{RF,out}}{P_{DC}}\left(1 - \frac{1}{G}\right) = DE\left(1 - \frac{1}{G}\right) \tag{2.7.5}$$

Transistors with more gain exhibit higher PAE. Increasing f_{max} results in more power gain at a given frequency and thus higher PAE; increasing f_τ results in higher current gain which results in lower noise and higher f_{max} for a given geometry. Maximum voltage gain ($A_{V,max}$) in a FET is the ratio of transconductance to output conductance:

$$A_{V,max} = \frac{g_m}{g_{ds}} \tag{2.7.7}$$

To increase $A_{V,max}$ and PAE for FET circuits, transconductance must be increased and output conductance decreased. As discussed in **Section E**, replacing the $In_{0.52}Al_{0.48}As$ gate insulator in a standard InP-based HEMT with a 2 nm ZrO_2 high-k gate-dielectric should increase g_m due to larger $C_{g\text{-}ch}$ and simultaneously decrease g_{ds} due to improved electrostatics.

Noise figure is also important for IC designers, especially for front-end, low noise amplifiers. Noise figure can be used to describe the noise of a single stage while cascaded noise factor describes the noise of cascaded stages. Minimum noise figure is given by [34], [35]:

$$F_{min} = 1 + 2\sqrt{g_m(R_S + R_G + R_i)\Gamma}\left(\frac{f}{f_\tau}\right) + 2g_m(R_S + R_G + R_i)\Gamma\left(\frac{f}{f_\tau}\right)^2 \quad (2.7.8)$$

Where R_i is gate-source intrinsic channel resistance. Cascaded noise factor is given by the Friis formula:

$$F_\infty = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots \quad (2.7.9)$$

Where F_N is the noise figure of a given stage and G_N is the power gain of a given stage. Noise figure illustrates the importance of increasing f_τ. The cascaded noise factor can be related to the more commonly used Noise Measure (M): $M = F_\infty - 1$. However, noise figure is dependent on terms that also effect f_{max} (i.e. R_G). Therefore, to provide low noise figure, devices should exhibit balanced f_τ , f_{max}. Noise factor says that without gain in the first stage (G_1), it is difficult to achieve acceptable noise factor for cascaded amplifiers further motivating balanced f_τ , f_{max}.

Relating device components to a small-signal equivalent circuit model (SSEC) is a useful technique to identify components limiting the high-frequency FOMs and optimize the device structure. SSECs also provide a compact description of a device that can be used by IC designers to simulate complex layouts quickly. Therefore, it is useful to relate the measured S-parameters to a SSEC.

H. Equivalent Circuit Model

A small-signal equivalent circuit (SSEC) is a useful tool to model the device behavior over a broad-range of frequencies. Models are determined by fitting measured S-parameter data with a circuit model, providing a compact description of the device that can be used by integrated circuit (IC) designers. Common source SSECs have been widely studied [36]–[38].

The simplest equivalent circuit used to model common source FETs is illustrated in **Figure 2.10a**. Most simply, a FET is a voltage controlled current source where the controlling capacitor (C_{GS}) modulates the current source $g_{m,i}v_{gs}$'. The gate is also coupled to the drain (C_{GD}) and the drain can exhibit some influence over the conductivity of channel ($g_{d,i}$). The illustrated circuit parameters change with bias and are considered "intrinsic" elements. Because the intrinsic device is in parallel, admittance (Y) parameters are useful to describe the frequency response.

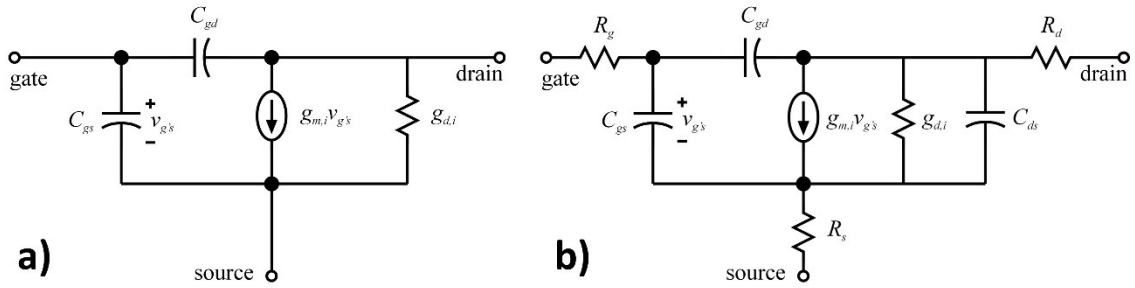

Figure 2.10 Common source FET equivalent circuit a) simple b) moderate complexity

Practical devices exhibit additional circuit elements. The drain is capacitively coupled to the source (C_{DS}), there are series source (R_S) and drain (R_D) resistances, as well as gate resistance (R_G). These elements are in series with the intrinsic device and are most easily described using impedance (Z) parameters. The resulting small-signal equivalent circuit is shown in **Figure 2.10b**. Kwon *et al.* analyzed an equivalent circuit in order to model CMOS

transistors, similar to **Figure 2.10**. Notable differences in their model are the exclusion of series R_S and R_D and inclusion of body effects [38]. CMOS transistors are fabricated on doped substrates and therefore have conductive bodies (R_{sub}), the resulting equivalent circuit is illustrated in **Figure 2.11**.

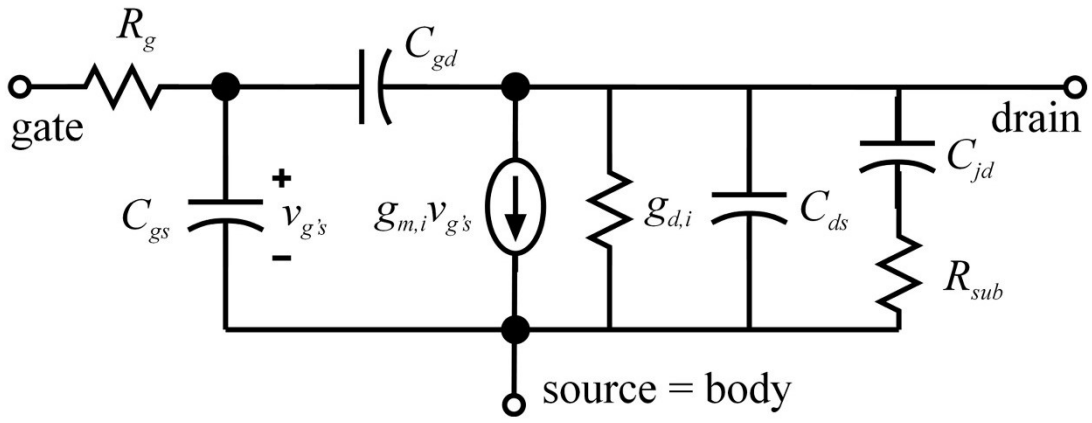

Figure 2.11 Equivalent circuit used to derive Y-parameters reported in [38]

MOS-HEMTs in this thesis are fabricated on semi-insulating substrates, therefore $R_{sub} \approx \infty$. Generation 1 and Generation 2 devices, to be discussed in later chapters, contained unintentionally conductive etch stops. Therefore, R_{sub} and C_{jd} can be used to characterize drain coupling to this layer. The Y-parameters, assuming $\omega^2(C_{GS} + C_{GD})^2 R_G^2 \ll 1$, are:

$$Y_{11} = \omega^2(C_{GS} + C_{GD})^2 R_G + j\omega(C_{GS} + C_{GD}) \tag{2.8.1}$$

$$Y_{12} = \omega^2 C_{GD}(C_{GS} + C_{GD}) R_G - j\omega C_{GD} \tag{2.8.2}$$

$$Y_{21} = [g_m - \omega^2 C_{DG}(C_{GS} + C_{DG})^2 R_G] - [j\omega C_{DG} + j\omega g_m R_G(C_{GS} + C_{DG})] \tag{2.8.3}$$

$$Y_{22} = \left[g_{DS} + \omega^2 {C_{DG}}^2 R_G + \frac{\omega^2 {C_{jd}}^2 {R_{sub}}^2}{1 + \omega^2 {C_{jd}}^2 {R_{sub}}^2}\right] + \left[j\omega C_{DS} + j\omega C_{DG} + \frac{j\omega C_{jd}}{1 + \omega^2 {C_{jd}}^2 {R_{sub}}^2}\right] \tag{2.7.4}$$

Using reported values from [24], [25], [39], the above low frequency assumption is valid for $f < 100$ GHz if $R_G < 10\ \Omega$. $C_{GD} \neq C_{DG}$ because of the different excitation direction; however

they are nearly equal and are not treated separately below. Small-signal-equivalent circuit parameters C_{GS}, C_{GD}, R_G, g_m, and g_{ds} can be easily extracted:

$$C_{GD} = -\frac{Im[Y_{21}]}{\omega} \tag{2.8.5}$$

$$C_{GS} = \frac{Im[Y_{11}]}{\omega} - C_{GD} \tag{2.8.6}$$

$$R_G = \frac{Re[Y_{21}]}{(Im[Y_{11}])^2} \tag{2.8.7}$$

$$g_m = Re[Y_{21}]|_{\omega^2=0} \tag{2.8.8}$$

$$g_{ds} = Re[Y_{22}]|_{\omega^2=0} \tag{2.8.9}$$

In addition to the treatment above, impact ionization or BTBT can occur at the drain-edge when biased at high V_{DS}. Both mechanisms create electron-hole pairs. The generated holes then move back into the channel of the transistor where they get trapped in the potential well of the channel. The resulting positive charge in the channel further lowers then channel surface potential allowing more electrons to flow into the channel. The holes remain trapped in the channel until they recombine with electrons transiting the channel resulting in a parasitic bipolar current gain. This can be modeled in several ways [39]–[41]. For this thesis, a series *LR* network is included between source and drain where the *LR* time constant represents the hole lifetime (τ_p).

The above treatment neglects the presence of extrinsic device components R_S and R_D. As a result, the extracted transconductance values are $g_{m,e}$ and $g_{ds,e}$. TLMs and transistor gate-length series are used to estimate R_S but additional measurements are desirable. At V_{DS} = 0.0 V, the devices reported are symmetric and $R_S = R_D$. The transistor is then biased so the channel is strongly inverted, making the channel conductive. With this, R_S, R_D, and R_G are then determined [42]:

$$R_D = Re(Z_{22}) - Re(Z_{11}) \tag{2.8.10}$$

$$R_S = R_D \tag{2.8.11}$$

$$R_G = Re(Z_{11}) - \frac{Re(Z_{12})}{2} - R_S \tag{2.8.12}$$

f_τ and f_{max} can then be determined directly from the SSEC. Tasker and Hughes derived the expression for f_τ and f_{max} for AlGaN/GaN HEMTs; the model can be extended to FETs [43]:

$$f_{\tau,int} = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \tag{2.8.13}$$

$$f_\tau = \frac{g_m}{2\pi\left[(C_{GS} + C_{GD})\left(1 + g_{ds}(R_S + R_D)\right) + g_m C_{GD}(R_S + R_D)\right]} \tag{2.8.14}$$

$$f_{max} = \frac{f_{\tau,int}}{\sqrt{4g_{ds}(R_S + R_G + R_{GS}) + (1 + F)}} \tag{2.8.15}$$

$$F = \frac{\omega_\tau L_S}{R_{in}} + \frac{2\omega_\tau C_{GD}}{g_{ds}}\left(1 + \frac{R_G}{R_{in}} + \frac{\omega_\tau L_S}{2R_{in}} + \frac{2\pi\tau}{C_{GS}R_{in}}\right) \tag{2.8.16}$$

Where $R_{in} = R_S + R_G + R_{GS}$ and $\omega_\tau = 2\pi f_\tau$. As previously discussed, to increase f_τ it is necessary to increase $g_{m,i}$ while simultaneously reducing C_{GS}, C_{GD}, and R_S. Increasing f_τ also increases f_{max}; however additional attention must be paid to minimize R_G and g_{ds}.

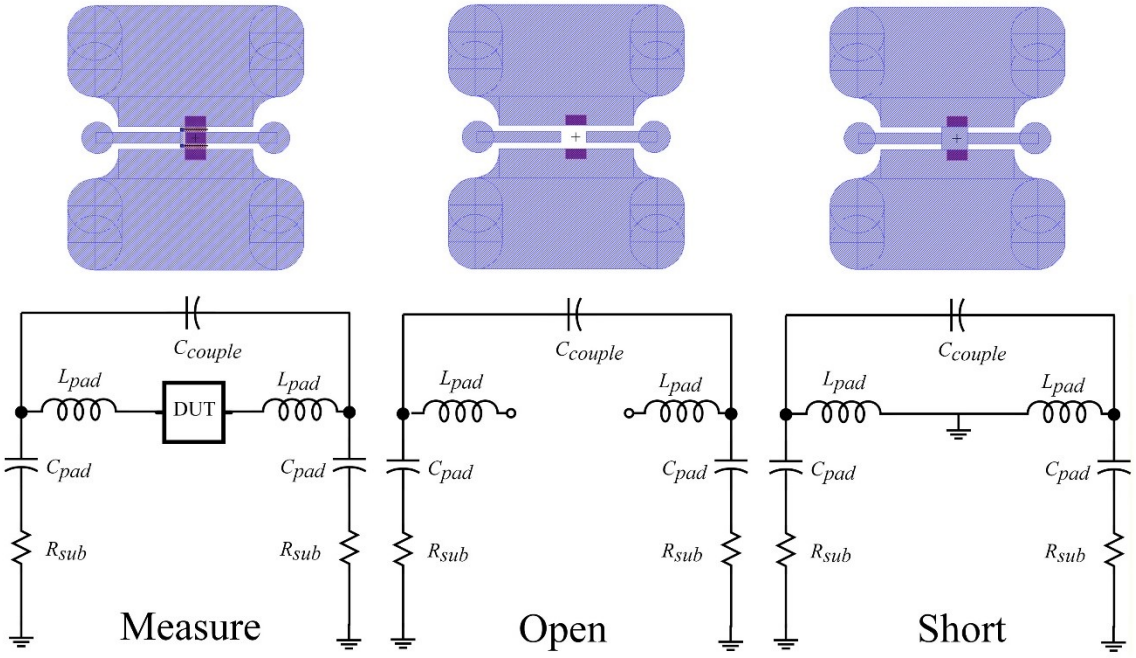

Figure 2.12 Mask layout and equivalent circuit used for de-embedding

Practical devices are embedded in a wiring environment, either to be used or to be measured; therefore, on wafer calibration structures must be used to de-embed the wiring capacitance and inductance. **Figure 2.12** illustrates the pad structures used throughout this thesis and the equivalent circuit model with and without pads present. For this thesis, Open-Short and Short-Open de-embedding is used, and the more conservative FOM values reported (Open-Short). Open-short de-embedding is done by removing the pad capacitance:

$$Y'_{DUT} = Y_{DUT} - Y_{Open} \tag{2.8.10}$$

Before removing the inductance, the pad capacitance in the short must be removed:

$$Y'_{Short} = Y_{Short} - Y_{Open} \tag{2.8.11}$$

The Y-parameters are then converted to Z-parameters and the pad inductance can be removed:

$$Z''_{DUT} = Z'_{DUT} - Z'_{Short} \tag{2.8.12}$$

Figure 2.13 shows the Y''_{DUT} for an open-short and short-open de-embedded, Generation 1 device.

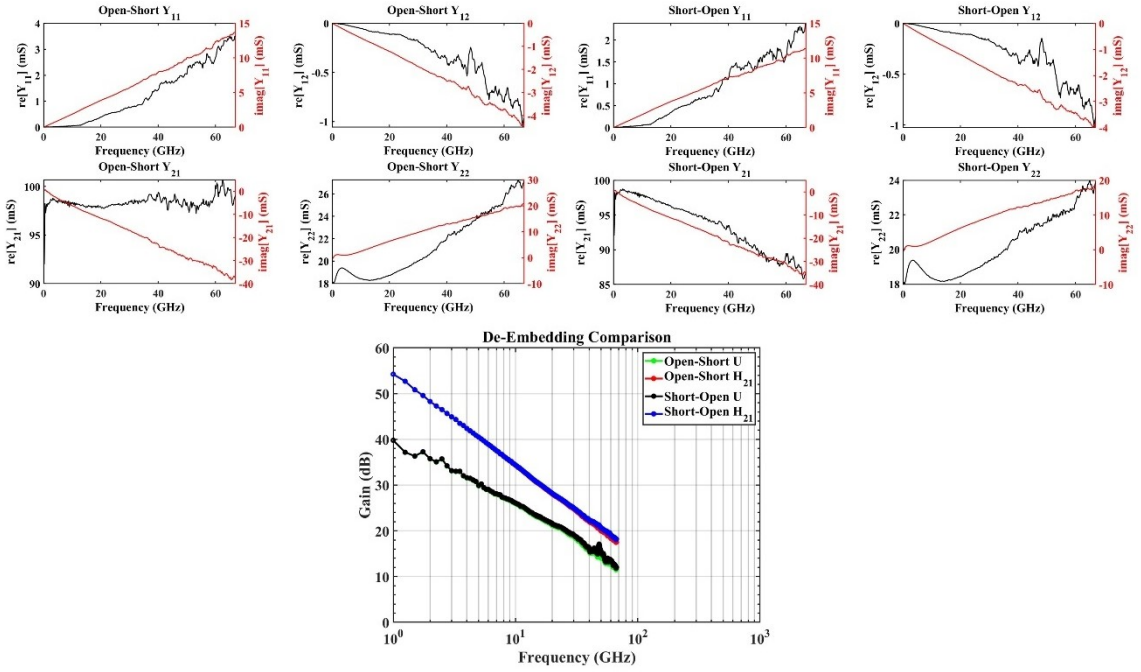

Figure 2.13 De-embedded Y-parameters by open-short and short-open and their FOMs

Finally, some devices in this thesis exhibit large R_G and C_{DS}. Consequently, higher order terms contribute to the high frequency Y-parameters. Circuit components extracted by the above described technique are used as a starting point for SSEC modeling and finalized by modeling in Keysight Advanced Design Systems (ADS) software.

E. Summary

In this chapter, basic MOSFET theory was discussed and ballistic transport in ultra-thin-body devices was expanded on. In short summary, the channel of a MOSFET must be thin enough to provide good electrostatics while being thick enough so that the channel eigenstate does not limit I_{DS} and $g_{m,i}$. High transconductance transistors for mm-wave applications are optimized at t_{ch} = 5 – 10 nm using wide bandgap back-barrier materials such as $AlAs_{0.56}Sb_{0.44}$.

Finally, high frequency FOMs were introduced and the FET common-source small-signal equivalent circuit described.

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3. Fabrication Process

In the following section, the bottom-up fabrication process of MOS-HEMTs presented in this thesis is discussed. For brevity, certain process modules are abbreviated: dummy gate 1 (DG1), dummy gate 2 (DG2), T-Gate foot (TGF), and T-Gate head (TGH).

A. Overview

High electron mobility transistors are generally fabricated in a top down approach where the highly doped N+ source-drain regions sit on top of the wide bandgap, modulation doped link regions [1]–[4]. Electrons must get from the N+ layer into the conductive quantum well by passing through the wide bandgap link region. While the heavy doping in the N+ pulls the bands down in the top part of the UID-link, the depleted modulation doping introduces a large barrier to electrons illustrated in **Figure 3.1**. This manifests itself as series resistance in R_S and decreases $g_{m,e}$ and thus f_τ.

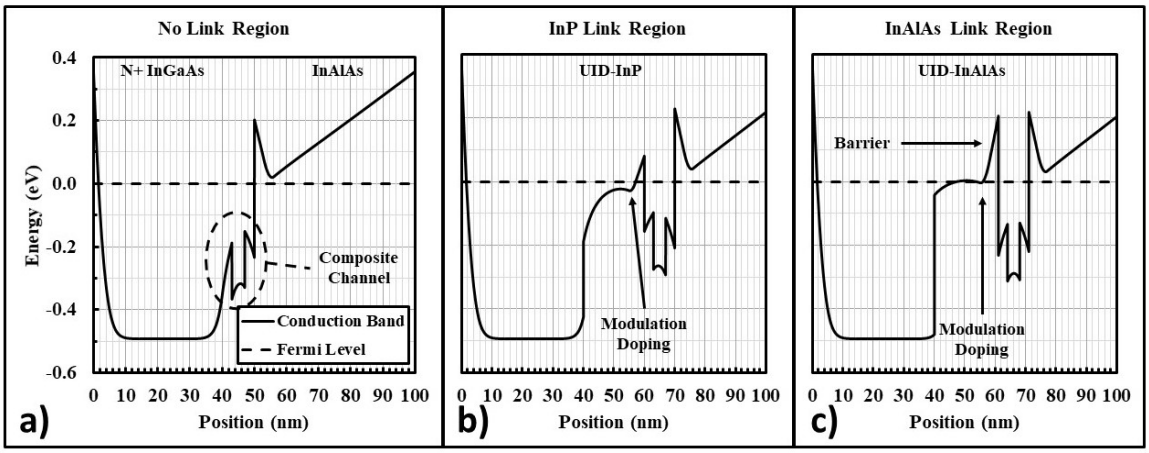

Figure 3.1 Band diagrams beneath N+ $In_{0.53}Ga_{0.47}As$ source-drains in HEMT structures for a) link region removed b) modulation doped InP link c) modulation doped $In_{0.52}Al_{0.48}As$ link

To address this issue and to maintain compatibility with the UCSB III-V FET process – widely reported in [5]–[8] – a regrowth process is proposed. Rather than beginning with all

epi layers present, this thesis details processes starting with capped channel epi. The modulation doped link regions are regrown similar to the source-drain regrowth in [5]–[8]. By masking the recess regions with a second dummy gate lithography and etching – either dry or wet – it is possible to remove the link region in the field enabling the N+ contact layer to be regrown directly on the channel. **Figure 3.1** compares regrowth of the N+ $In_{0.53}Ga_{0.47}As$ on modulation doped InP and $In_{0.52}Al_{0.48}As$ as well as directly on the channel. Device generations 1 – 3 used regrown InP link regions as $In_{0.52}Al_{0.48}As$ was not yet available at UCSB. Attempts to use regrown $In_{0.52}Al_{0.48}As$ links were made but limited by the inability to dope > 5 x 10^{18} cm^{-3}. Importantly, InP link regions do not provide a large barrier to electrons while $In_{0.52}Al_{0.48}As$ does. However, due to the small conduction band-offset of InP to $In_{0.53}Ga_{0.47}As$, the maximum quantum well sheet charge density (n_{Link}) achievable is ~5 x 10^{12} cm^{-2}. Because the channel charge density (n_{ch}) at large ($V_{GS} - V_{TH}$) can approach 1 x 10^{13} cm^{-2}, it is desirable to use an $In_{0.52}Al_{0.48}As$ top barrier to prevent source starvation.

B. Alignment Marks

The double recess structure of HEMTs requires that the source-drain recess and gate recess be aligned, at least, within 50 nm. Because the Gate-Source and Gate-Drain spacing in [1], [3], [9] is 50 – 100 nm, the alignment needs to be better than 20 nm for the structure to behave as designed. Precision alignment in scaled heterojunction bipolar transistors (HBTs) is achieved by aligning to the emitter metal. However, because HBTs are planarized later, the emitter metal is thick (0.5 μm) and the alignment marks etched simultaneously are easy to detect in the electron beam lithographer (EBL). In a regrown MOSFET process, the first lithography steps are used to define the gate recess as well as the gate-source and gate-drain recesses. Both layers are thin regrowth structures that are difficult to detect in an EBL and

thus cannot be used as alignment marks. Regrowing more material can provide additional contrast, however, there are limitations on the recess depth:

A. T-Gate foot height (~200 nm) which limits $t_{Link} + t_N \leq 0.5 \bullet t_{foot}$ so that the T-Gate head does not short to the N+ and so that the foot resist can fully planarize the surface
B. Link thickness 12 nm $\leq t_{Link} \leq$ 25 nm so that the modulation doping primarily images in the quantum well and so that the vertical access resistance (R_A) through the modulation doped link region is minimized.

Clearly, the thickest a regrowth layer can be is ~100 nm; however, it is difficult to find thin alignment marks of like materials in an scanning electron microscope (SEM) and electron beam lithographer (EBL) and it is clear that either or both of the regrowth layers cannot be used for later alignments.

Because the wafers will be regrown on by metal organic chemical vapor deposition (MOCVD), any material deposited prior to regrowth must be compatible with temperatures in excess of 600°C. Common refractory metals that are compatible with these temperatures (W, Mo, Ru) must be sputtered or electron beam evaporated which both can cause damage that manifests as high D_{it} [10]. It is possible any damage caused during this 0-layer deposition could be annealed out during the regrowth. Wet etched alignment marks can also be used, avoiding possible damage. While metal marks have significant Z-contrast *and* edge scattering, etched marks only exhibit edge scattering and must be deep enough to be detected. Generally, it is "easy" to see and detect 1 μm deep trenches in the JEOL 6300FS EBL at UCSB. It is challenging at d_{trench} = 500 nm and requires more rastering to get acceptable signal. Because the required alignment is at the limit of the tool's ability (20 nm), maximizing signal is desirable and generally results in best alignment.

Because there are 3 layers that must be critically aligned (DG2 to DG1, TGF to DG1), and because the JEOL 6300FS performs alignment by rastering across a single point, it is necessary to preserve the integrity of the alignment marks until the T-Gate process module is complete. Significant edge roughness (>10 nm) is expected for micron scale, wet etched features. Because alignment is performed by scanning a single point on each cross arm, edge roughness in the alignment mark etch can result in severe misalignment if different locations on the mark used for each step. Consequently, it is critical to preserve the original alignment marks throughout the process and scan the same location, using the same gain values, and same beam current to maximize reproducibility.

Given that the alignment marks must be preserved throughout the process there is a limit on their depth. The mesa isolation etch is done before the T-Gate deposition and can modify the size and shape of the alignment marks. It is important that the alignment marks be deep enough to be seen in an SEM but shallow enough to be planarized and protected by the mesa isolation resist. Generally, with commonly available/utilized photoresists at UCSB, this limits the alignment marks to d_{trench} = 1 μm.

C. Dummy Gate 1 + Link Regrowth

The first dummy gate and link regrowth step are critical as they define the minimum metallurgical gate length and quantum well thickness in the link region. To protect the channel surface from contaminants, 1 nm ALD Al_2O_3 is deposited prior to spinning 2% HSQ on the surface. Because HSQ exhibits a large electron blur, it is desirable to use the thinnest possible HSQ to achieve the smallest feature size. Because subsequent layers must be precisely aligned to dummy gate 1 (DG1), the alignment parameters used to align DG1 to the 0 layer define the gain values, scan parameters, and beam current to be used throughout the process.

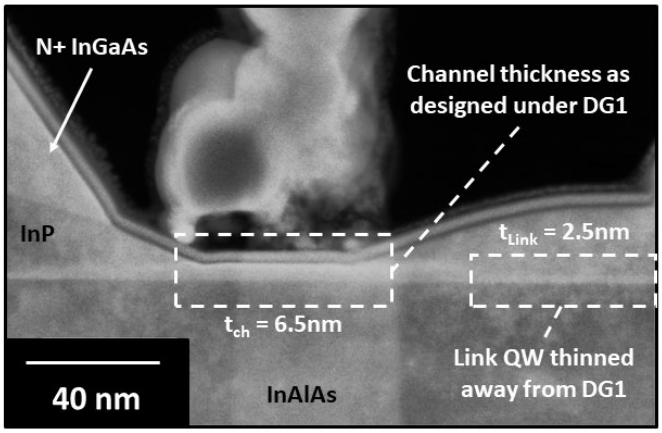

Figure 3.2 Cross-section TEM of completed device Ch2-L1G2SD3 showing link region thinning due to overdevelopment of dummy gate 1 HSQ (90s NaOH:NaCl:H2O 2g:8g:200mL + 120s AZ300-MIF) where InGaAs / InAs composite channel etched in dilute base chemistry

HSQ development is done using NaOH:NaCl:H_2O 2g:8g:200mL due to its extremely high contrast [11]. Because HSQ is converted to SiO_2 during exposure, it has a nearly zero etch rate in the above developer suggesting that it can be overdeveloped with minimal effect on pattern integrity. While overdeveloping is desirable in order to ensure complete removal of both the HSQ and the underlying Al_2O_3 (etches in most basic chemistries) prior to regrowth, Na *et al.* demonstrated that dilute NaOH also etches InAs [12]. Device run Ch2-L1G2SD3, shown in **Figure 3.2,** exhibited an unintentionally thinned link region due to overdevelopment, illustrating the importance of optimizing development time. Short development can leave residual HSQ or Al_2O_3 on the surface resulting in micro-masking during regrowth.

Finally, HSQ has been shown to completely cure at temperatures ≥550°C [13]. During the curing process HSQ patterns shrink ~10-20% [13]. It is expected that the regrown separation is smaller than the initially resolved pattern. Because of low Z-contrast, minimal edge scattering, impracticability of finding small isolated patterns, pattern warping during imaging, and pattern shrinkage during growth, it is not practical or useful to image the as exposed HSQ.

Test structures should be located near large features to optically verify pattern integrity and good adhesion prior to regrowth. Patterns should be imaged by SEM *after* regrowth and dummy gate removal to estimate gate length.

Finally, MOCVD selective area regrowth has nearly perfect selectivity of oxide to semiconductor at extremely low fill factors, enabling the use of bulk growth recipes. Modifications of temperature, V/III ratio, and pressure can be used to promote the formation of desired facets at the gate edge. Kunert *et al.* investigated this parameter space for moderate fill factor selective area regrowth and can be used as a general reference [14], [15].

D. Dummy Gate 2 + Link Etch + Source-Drain Regrowth

Dummy gate 2 (DG2) defines the Gate-Source and Gate-Drain recesses. Because the recess lengths are of order 50 nm, $L_{DG2} = L_g + L_{gs} + L_{gd}$, the minimum feature size is ≥100 nm. Generally, this would allow for larger beam currents to be used and lower write times to be achieved. However, this comes at the expense of alignment. Because of the larger beam size, the observed alignment mark shape is less sharp. While this should, in principle, not affect the position of the "center" of the alignment mark, using larger beam currents to write the second dummy gate results in misalignment ~20 – 40 nm (see Ch1-L1G1SD1 and Ch2-L1G2SD3) while using the same beam current as DG1 yields misalignment < 20nm (see device runs Ch3-L1G2SD3 and after) as illustrated in **Figure 3.3**.

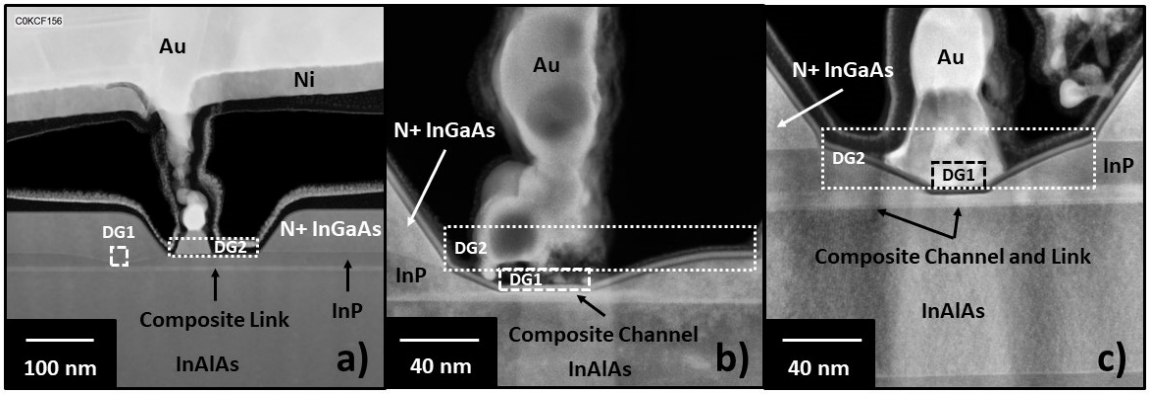

Figure 3.3 Cross-sectional TEM images demonstrating the reliability of aligning dummy gate 2 to dummy gate 1 using a) different beam current and scan locations b) different beam current and same scan location c) same beam current and same location

In addition to alignment considerations, there is surface topography t_{Link} in the area of interest. Because the link thickness is comparable to the thickness of 2% HSQ, 6% HSQ is used instead. Due to the increased feature size, the larger HSQ thickness is not a concern; complete planarization, however, is paramount. Again, to protect the channel surface from contaminants, 1nm ALD Al_2O_3 layer is deposited immediately prior to spinning HSQ. Because the 6% HSQ is thicker (~130 nm) and it is not necessary to preserve the link thickness in regions not protected by the second dummy gate, significant overdevelopment should be utilized to ensure complete removal of both the HSQ and underlying Al_2O_3.

If the link region will be removed beneath areas where the N+ source-drain will be regrown, it can be done two ways: wet etching or dry etching. Wet etching is highly desirable to avoid damaging the channel either by ion bombardment or with UV radiation (plasma glow). However, HSQ exhibits only moderately good adhesion to InP and $In_{0.53}Ga_{0.47}As$ and thus the interface between HSQ and the semiconductor is susceptible to wet chemistries [16]. Additionally, most crystallographic wet etches are extremely fast, ~100 nm/min [17], [18]. While they exhibit slow undercut rates in specific crystallographic directions, any penetration

at the HSQ / Link interface will result in an immediate clearing of the link region. As a result, wet removal of the link region was done by digital etching: cycles of 3 minutes UV-ozone followed by 60 seconds HCl:H_2O 1:10. Measured etch rates and sheet resistance values for InP and $In_{0.52}Al_{0.48}As$ links are shown in **Figure 3.4**. As the modulation doped, widegap link is thinned, the lever rule requires more charge from the modulation doping image on the semiconductor surface and less charge image in the quantum well resulting in increased link sheet resistance.

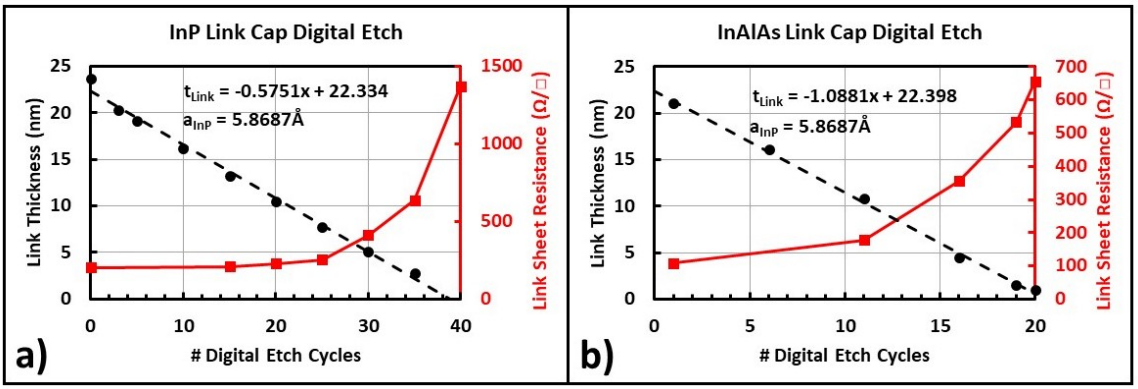

Figure 3.4 Fitted digital etch rate and link region sheet resistance dependence on link cap thickness for a) InP link (3 nm UID-InP spacer, 2 nm 1x10^{19} cm^{-3} InP modulation doping, 20 nm UID-InP cap) b) InAlAs link (3 nm UID-$In_{0.52}Al_{0.48}As$ spacer, 3 nm 1x10^{19} cm^{-3} $In_{0.52}Al_{0.48}As$ modulation doping, 15 nm UID-$In_{0.52}Al_{0.48}As$ cap)

Dry etching the link is possible using two tools in the UCSB cleanroom: 1) Unaxis VLR 2) RIE #2 (Materials Research Corporation RIE-51 Parallel Plate).

The Unaxis is a chlorine chemistry tool with T_{chuck} = 200°C so that III-chlorides are volatile during etching. Because the Panasonic ICPs operate with T_{chuck} = 90°C, they cannot be used for most III-V etching due to the formation of non-volatile III-chlorides or III-fluorides. Because the Unaxis is designed to accept 4" wafers, pieces must be mounted using thermal grease. Samples are often thin InP wafers; consequently, demounting the wafers and cleaning the backside can cause them to break. Additionally, because the thermal grease is

silicone based, it is difficult to completely remove (as it is not soluble in acetone, methanol, or IPA) and can contaminate the MOCVD chamber. Finally, the Unaxis exhibits a strong loading effect and thus pieces of different sizes, with different exposed areas, will etch unpredictably.

RIE #2 uses methane, hydrogen, and argon (MHA) to etch III-Vs. The inclusion of hydrogen can passivate carbon doped $In_{0.53}Ga_{0.47}As$ and is thus not suitable for highly doped p- $In_{0.53}Ga_{0.47}As$ etching. However, this should not be a concern for UID or N-type III-Vs. Like the Unaxis, RIE #2 exhibits a strong loading affect for pieces smaller than a 2" wafer. Consequently, a calibration piece must be used immediately prior to sample loading and must be the same size. Because the dummy gates take up an extremely small area, a blank sample with the same epi can be used for etch calibration.

InP can be etched at low self-bias of 170 V [19]. $In_{0.52}Al_{0.48}As$ does not etch in MHA unless a self-bias in excess of 300 V is used [20]. In both cases, damage by ion bombardment is possible even through the HSQ hard mask. Additionally, $In_{0.53}Ga_{0.47}As$ (channel) etches faster than InP and $In_{0.52}Al_{0.48}As$ (link), making process control difficult [19], [20]. To prevent channel removal, the etch should be timed to stop 2-3 nm above the $In_{0.53}Ga_{0.47}As$ and digital etch the remaining material.

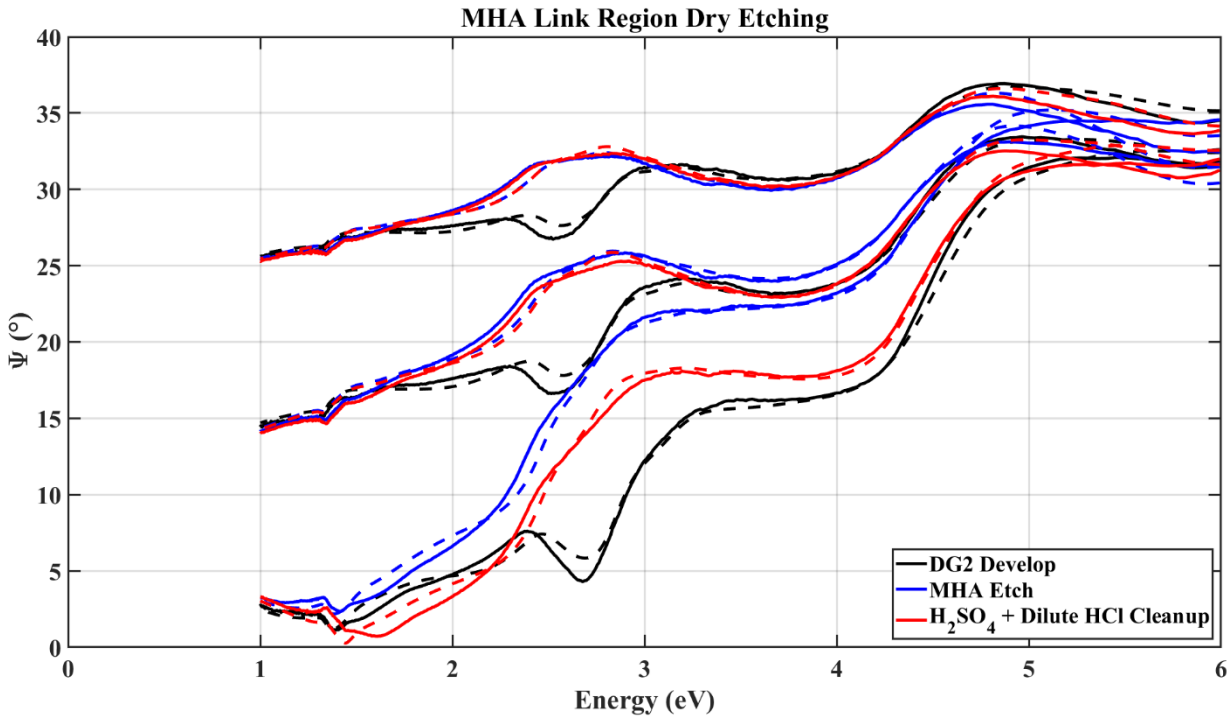

Figure 3.5 Ellipsometry of MHA dry etch of $In_{0.52}Al_{0.48}As$ link region where solid lines are measured and dashed lines are modeled

Cleaning the sample after etching is critical since the methane and hydrogen polymerize forming compounds analogous to polyethylene which can be difficult to remove. After etching in MHA to remove the semiconductor link layer, an *in-situ* oxygen clean should be performed at the same power as the semiconductor etch to remove any polymer. **Figure 3.5** shows ellipsometry measurements that suggests surface modification during MHA etching. The modified surface can be fit assuming ~5 nm In_xO_y is present. III-oxides can be easily removed with a 60 second $HCl:H_2O$ 1:10 dip. Ellipsometry measurements at this point suggest a clean surface. However, regrowth results in ~100 nm hillocks when targeting 35 nm regrowth, suggesting micro-masking, possibly due to organic residue not removed during the *in-situ* oxygen ash. To ensure complete removal of any organic residue, a concentrated H_2SO_4 etch can be used immediately after unloading. Best practice is:

1. Measure etched material with ellipsometry, expect to see modified surface
2. 30-60s concentrated H_2SO_4 etch to remove residual polymer not removed during O_2 clean
3. HCl:H_2O 1:10 etch to remove surface oxide
4. Measure by ellipsometry to determine remaining link thickness, expect targeted thickness defined by MHA etch
5. Digital etch to desired thickness
6. Regrow source-drain by MOCVD

E. Mesa Isolation

While mesa isolation is often not discussed, it is critically important for MOS-HEMTs. Because T-Gates are low yield structures, it is important to pay close attention to points of failure. Specifically, T-Gates are intolerant of topography which is most extreme at the mesa edges. To ensure continuity and limit resistive chokes, $d_{mesa} < t_{foot}$. In the region where the T-Gate is expected to traverse the mesa edge, $d_{mesa} = t_{ch} + t_{Link} + t_{BB}$ where t_{BB} is the back-barrier thickness. The T-Gate should *NOT* be sitting on the source-drain regrowth at any point along the gate-perimeter. Given that $t_{ch} \approx 7$ nm, $t_{Link} \approx 30$ nm, $t_{BB} \approx 100$ nm ($In_{0.52}Al_{0.48}As$ + InP etch stop), $d_{mesa} \approx 130$nm. Because t_{ch} and t_{Link} are integral parts of the device design, the only way to reduce d_{mesa} is to reduce t_{BB}. If t_{BB} is scaled too aggressively, a parasitic 2DEG can form at the $In_{0.52}Al_{0.48}As$ / InP back-barrier interface.

Additionally, the mesa isolation photoresist must also be thick enough to planarize the alignment marks; otherwise, the mesa isolation etch will attack the alignment marks, modifying their size and shape. Aligning the TGF to DG1 with damaged marks is difficult. Process parameters must be optimized for the resulting structure after the etch. Because

ternary III-V etches are isotropic [17], the pattern will shrink by at least 2•d_{mesa}. Additionally, to completely clear $In_{0.52}Al_{0.48}As$ often requires an over-etch of 20 – 50% resulting in a total pattern size reduction of ~3•d_{mesa}. Because small mesa width (W_{mesa}) is necessary for low gate resistance (R_G) and therefore high power-gain cut-off frequency (f_{max}), it is desirable to push the limits of alignment tolerance and maximize contact area to minimize contact resistance (R_C) and thus R_S. Pattern shrinkage during the mesa etch later reduces available contact area (A_C) or exacerbates alignment tolerance.

F. High-K Dielectric

High-K gate dielectrics on III-V materials were a challenge due to high D_{it} for many years. Extensive work at UCSB has been done to improve D_{it} on III-V. Initial improvements were realized through *in-situ* hydrogen plasma surface treatment [21] and additional progress achieved with *in-situ* nitrogen plasma surface treatment [22]. Many implementations of the techniques described in [21], [22] can be found in [23], [24].

In short summary, there are 4 necessary steps to form an acceptable high-k gate dielectric on $In_{0.53}Ga_{0.47}As$ and InAs surfaces:

1. Surface preparation by wet chemistry
2. Surface cleaning / passivation by plasma-enhanced atomic layer deposition (ALD)
3. ALD deposition of high-k
4. Forming gas anneal to passivate dangling bonds

First, it is imperative to have a clean surface to begin. Careful attention is paid in previous process steps such that the area destined to become the channel / high-k interface is *only* exposed to ALD Al_2O_3. This is the most similar material to the cleaning / passivation layer to be described. Cycling UV-ozone and $HCl:H_2O$ serves the dual purpose of controllably

thinning the channel (~1 nm/cycle) and cleaning the surface. Immediately prior to loading into the ALD, a BHF dip removes the native oxide and forms a temporary, protective layer.

The ALD deposition begins with trimethyl-aluminum (TMA) + nitrogen plasma (N*) cycling to clean the surface of native oxide [25]. Some $Al_xO_yN_z$ is formed on the semiconductor surface during this step which is expected to have ε_r comparable to Al_2O_3. Because this layer is in series with the high-k, it limits the overall capacitance density of the high-k stack and should be kept as thin as possible. For VLSI devices reported in [5]–[7] where minimum subthreshold slope is critical to achieve maximum I_{on}/I_{off} at set $V_{DS} = V_{GS} =$ 0.5 V, 9 cycles of TMA+100W\N* was used prior to high-k deposition. Chobpattana showed that C_{ins} and D_{it} both decrease with increasing TMA + nitrogen plasma cleaning steps [22]. Because RF devices are not bias constrained, higher D_{it} can be tolerated and the number of cleaning cycles can be reduced.

Next the high-k is deposited by thermal ALD using either Tetrakis-(ethylmethylamido)-zirconium(IV) (TEMAZ) or Tetrakis-(ethylmethylamido)-hafnium(IV) (TEMAH) and H_2O. TEMAZ is often used because of the larger dielectric constant of ZrO_2, resulting in a larger C_{ins} for a given number of cycles as demonstrated in [22]. **Figure 3.6** shows a plot of maximum measured gate leakage current density using TEMAZ + H_2O as measured on large gate footprint devices at $(V_{DS} - V_{GS}) = 0.7$ V. Because RF devices can tolerate more I_G than VLSI devices, the gate dielectric can be thinned below 25 cycles. However, the breakdown voltage decreases as the oxide is thinned. Devices with 9 cycles of TMA + 100W\N* and 25 cycles of TEMAZ + H_2O undergo gate rupture at $(V_{DS} - V_{GS}) \approx 2.0$ V. Further thickness scaling is difficult because thick channel devices (necessary for high g_m and f_τ) have $V_{TH} \approx$ -0.2 V but

exhibit f_{max} at V_{DS} = 1.0 V. Consequently, it is likely that a device may be biased at V_{GS} = -0.7 V (off) and V_{DS} = 1.0 V which could cause breakdown if fewer cycles are used.

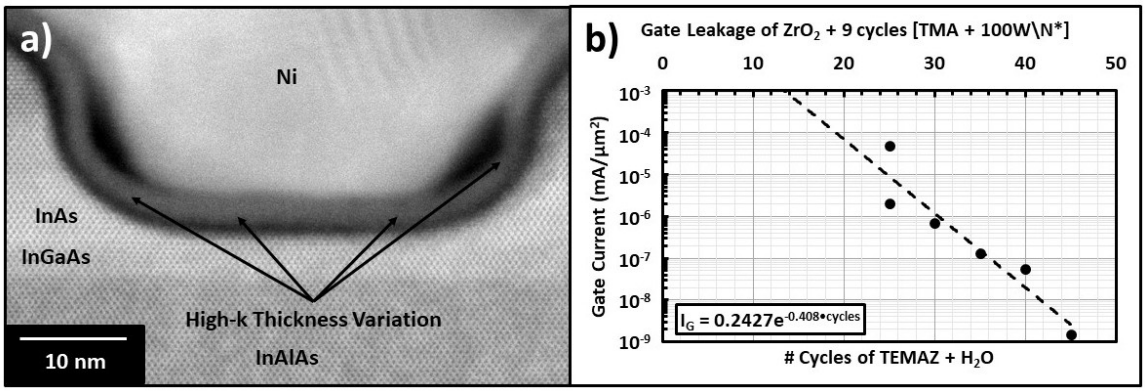

Figure 3.6 a) cross-sectional TEM image showing thickness variation across the length of the channel b) Gate leakage current as a function TEMAZ + H_2O cycles as extracted from long gate length devices with ($V_{DS} - V_{GS}$) = 0.7 V.

Finally, characterization of the absolute thickness is difficult and unnecessary. **Figure 3.6** clearly illustrates the difficulty of determining the thickness of the high-k and/or the passivation layer at any given point in the channel. Tracking metrics of interest such as C_{ins} by CV, I_G and g_m on transistors is most important.

G. T-Gate Formation

Because of the proposed double regrowth structure, the TGF must be realigned to the gate recess as defined by DG1. Additionally, the T-Gate footprint must be minimized in order to reduce parasitic gate-source capacitance ($C_{GS,p}$) as illustrated in **Figure 3.8**. This requires that the T-Gate be aligned to DG1 with equal precision as DG2. Again, as discussed in **Section B**, this requires that the same beam current, gain values, and detection scan settings be the same as for DG1 and DG2.

Because T-Gate formation requires multiple layers of electron beam resist (EBR), two approaches can be used:

1. All resists are spun on the wafer at once. The foot resist must require a larger dose than the head resist. Both resists are exposed in a single pass so that the overlapping head exposure does not turn the underlying foot resist.
2. The foot resist is spun, exposed, and developed before the head resist is spun, exposed, and developed.

Approach 1 reduces set up and exposure time but imposes two major limitations:

1. Electrons exposing the bottom resist (critical dimension) will scatter in the top resist. The resulting blurred electron beam will be larger than the incident beam and will result in lower resolution.
2. Developers for foot resist and head resist must be compatible. This limits the choice of foot resist and narrows the process window. This is particularly limiting when using foot resists such as ZEP/CSAR where the high contrast developers (polar solvents) dissolve most unexposed photo/electron beam resists.

Additionally, for lift-off to work, an underlayer or an undercut profile must be present in the resist. Realizing an undercut profile is different for electron beam lithography (EBL) than photolithography. In photolithography, photoresist (PR) quickly attenuates light at the exposure wavelength. Negative PR – which becomes resistant to develop when exposed – is used because the top absorbs more light and is thus more resistant to developing. Given that the bottom removes more quickly than the top, an undercut profile is achieved. In EBL, most of the incident electrons are *not* absorbed in the resist; rather they are transmitted into the substrate. Once in the substrate, they scatter, through multiple mechanisms, until they thermalize or are escape the substrate back into the EBR. Electrons that scatter back into the resist have lost significant energy and are generally absorbed in lower layers. Consequently,

the bottom of the resist is more highly exposed than the top of the resist. To a realize an undercut profile then requires that a positive EBR be used.

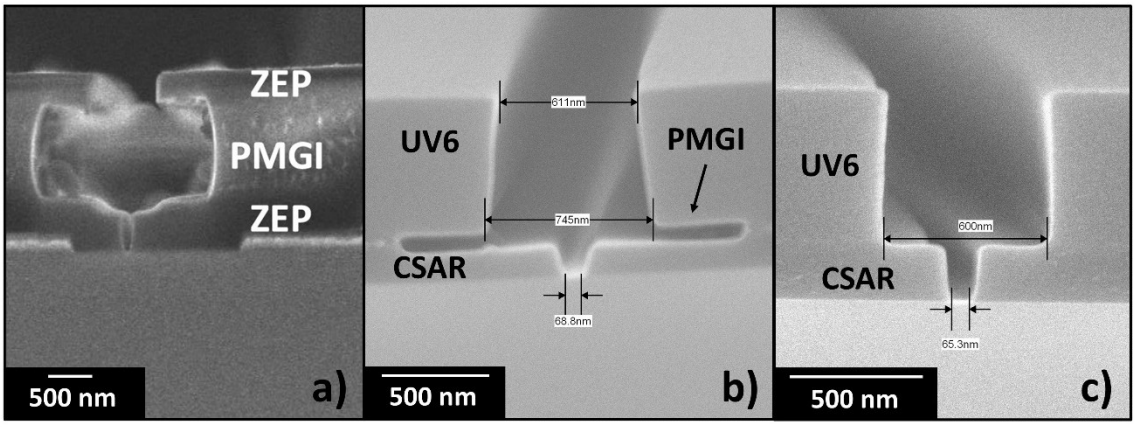

Figure 3.7 T-Gate resists stacks commonly used a) Trilayer ZEP / PMGI stack used in [26] b) Trilayer, single exposure CSAR / PMGI / UV6 stack used at UCSB, PMGI thickness can be modified to facilitate easier liftoff c) Bilayer, double exposure CSAR / UV6 stack used at UCSB

Common T-Gate resist stacks are layers of PMMA, ZEP, or CSAR with a PMGI lift-off layer [26], shown in **Figure 3.7**. For simplicity, we will assume PMMA is the aperture defining electron beam resist (EBR). Both ZEP and CSAR are low dose alternatives where CSAR is a newer version of ZEP.

Generally, a large dose PMMA is used in the foot while a smaller dose PMMA is used to define the aperture for the head. The PMGI is a thermal underlayer that undercuts at a rate determined by prebake temperature and duration. In this thesis, CSAR was used as the foot resist because it exhibits higher aspect ratio, lower base dose, and higher contrast than PMMA. The head resist is UV6-0.8 which is a deep UV resist commonly used in the ASML. UV6 is often used at UCSB as an extremely low dose positive electron beam resist and realizes enough of an undercut profile to be used for T-Gate heads without a PMGI underlayer. For single exposure T-Gates, a PMGI layer is used to prevent intermixing while for two exposure

T-Gates, no PMGI is used. The trilayer, single exposure stack and bilayer, double exposure stacks are illustrated in **Figure 3.7**.

After exposure, T-Gates must be metalized. Multiple studies have shown that gate metallization technique can cause damage to the high-k / semiconductor interface [10]. Consequently, only thermal evaporation or a thermal ALD processes should be used for gate metallization. Most recent work from UCSB utilizes thermal Ni / Au gate stacks [8], [9], [27]. Generally, choice of gate metal is dictated by two things: 1) metal work function to set the threshold voltage 2) adhesion to the high-k. For example, Au has a similar work function to Ni, is more conductive, and is mostly chemically inert; however, Au does not adhere well to most surfaces and T-Gates fabricated with only Au delaminate from high-k surfaces.

Given these constraints – must be thermal evaporated, must adhere to high-k surfaces, must have proper work function – the only available option at UCSB is Ni. Gate stacks for previous generation DC devices did not have to be highly conductive and were usually only ~100 nm thick [7], [8]. For RF applications, gate resistance is an important factor in f_{max} and thus T-Gates generally have $t_{head} \geq 300$ nm. Given the UCSB thermal evaporator geometry and boat size, multiple Au boats must be used to achieve this thickness. Because the thermal evaporator at UCSB is *not* a pocket source evaporator and because the stage is located near the sources, shadowing effects during deposition can cause failed lift-off, voids in the T-Gate stem, and voids in the T-Gate head. These all result in reduced yield and large gate resistance.

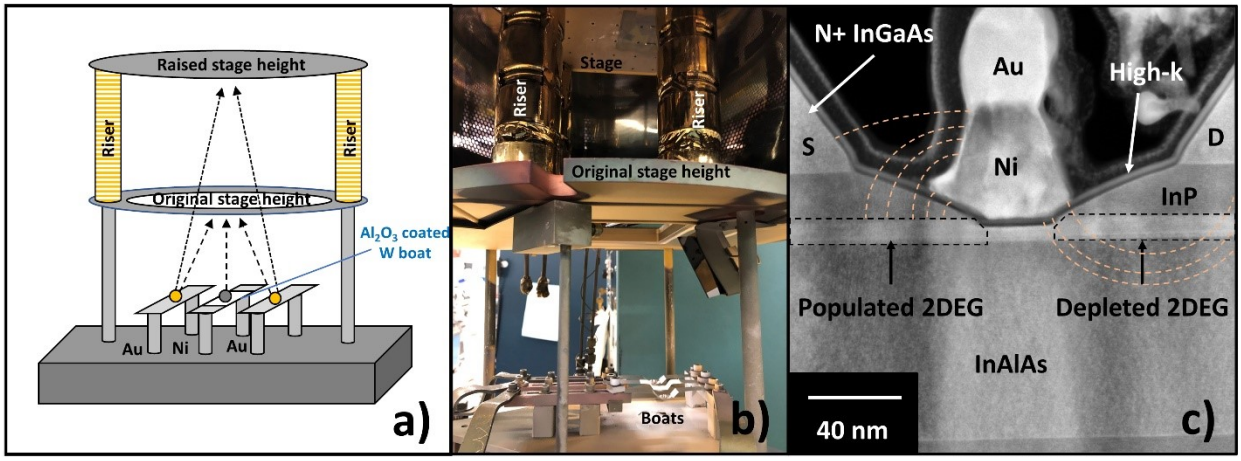

Figure 3.8 T-Gate process considerations a) illustration of UCSB thermal evaporator set up and modification for T-Gate evaporation b) picture of thermal evaporator set up c) Resulting T-Gate footprint and illustration of electric field lines that cause C_{GS} and C_{GD}

It is necessary to raise the stage in order to reduce the incident angle of evaporated metal as illustrated and photographed in **Figure 3.8**. The initial sample-stage separation is 17 cm while the risers provide an additional 22 cm of separation correspondingly to a $d_{mod}^2/d_{orig}^2 = 4.74$.

The observed deposition rate is ~1/5 of the rate observed by the crystal monitor, consistent with the expected $1/d^2$ variation, and the acceptance angle is reduced from 9.2° to 4.0°. However, despite best efforts, significant shadowing due to the off-center location of the two Au boats is still observed. Possible solutions include depositing enough Ni to fill the T-Gate foot or to deposit a small amount of Ni with a cap of Au, to prevent oxidation, followed by an electron beam evaporation of the remaining Au. Depositing enough Ni to fill the foot results in larger R_{foot} due to the higher resistivity of Ni compared to Au. Depositing thin Ni and capping with thin Au can still result in shadowing effects that obstruct further stem filling in the electron beam evaporator.

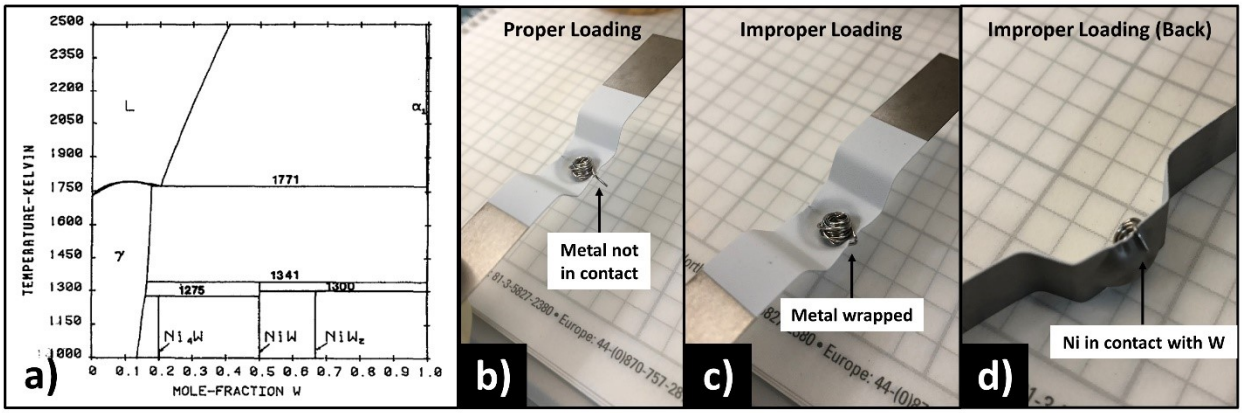

Figure 3.9 a) Ni-W binary phase diagram reproduced from [28] b) proper loading of Ni in aluminum coated, tungsten boat for gate thermal evaporation c) improper loading of Ni d) contact region of Ni-W when improperly loaded

Evaporating Ni is challenging itself. Because the UCSB thermal evaporator uses resistive, heated boats the boat must be conductive. So that the boat does not contaminate the evaporated material, it must have a high melting temperature (T_m) and low vapor pressure. Tungsten boats are commonly used and work well for low T_m metals (Al, Au, Cr, Zn). Nickel, however, has high T_m, is not noble, and readily alloys with other metals. Evaporating Ni using a W boat generally results in the boat breaking due to the formation of a Ni / W alloy, as seen in the binary phase diagram shown in **Figure 3.9**. To mitigate this, Al_2O_3 coated W boats are used. The Al_2O_3 coating provides a diffusion barrier between the Ni and W and prevents the formation of the alloy. However, the cryogenic pump vibrates the chamber, which can cause the Ni to vibrate out of the boat. This can be prevented by wrapping the Ni wire around the body of the boat. This can create contact between the Ni and W on the backside. During evaporation, the alloy on the backside melts first, and a conduit of molten metal forms connecting the front of the boat (coated with Al_2O_3) to the backside of the boat (alloy). When this occurs, the evaporation rate cannot be increased (or realized at all) and the backside of the boat is often completely evaporated. To mitigate this, crimp the Ni wire so that it can settle

into the dimple of the evaporation boat, providing an anchor point that prevents it from shaking out of the boat. The crimp must be short enough to break immediately upon melting, preventing a connection to the backside during evaporation, as shown in **Figure 3.9**.

Other Al_2O_3 boats are available which do not have these limitations. However, they are larger and have higher thermal mass. Because evaporating Ni is already at the limit of the power supply, these boats cannot practically be used. Using the above described loading method, if evaporation rate cannot be realized, sanding the connection points can help. The metal leads are Cu and oxidize when exposed to air. Over time the oxide on the copper leads cause significant series resistance, limiting the current.

H. Source-Drain Via

To reduce R_S and increase $g_{m,e}$, the source-drain ohmic spacing must be minimized. Because the N+ regrowth has $R_N \approx 20 – 40$ Ω/□ and 10/10/10 nm of deposited Ti / Pd / Au has $R_O \approx 1 – 2$ Ω/□, it is necessary to move the ohmic metal as close to the gate edge as possible. Topography near the gate edge makes T-Gate lithography and lift-off more difficult. Additionally, more metal options are available and less shadowing effects are observed in electron beam evaporation (with available tooling at UCSB). Consequently, it is desirable deposit the T-Gate metal first rather than Source-Drain Ohmic metal first. By doing the T-Gate metal first process, electron beam evaporated metals can be used for the source-drain without causing damage to the high-k / semiconductor interface [5]–[8].

The minimum source-drain ohmic spacing (L_{SDM}) possible with the T-Gate present is the width of the T-Gate head (W_{head}) if a self-aligned process is used. While spacings of order W_{head} can be realized via UV lithography, the alignment tolerance limits the spacing: $L_{SDM} = L_{PR} + 2 \bullet L_{MA}$ where L_{PR} is the minimum resolution and L_{MA} is the misalignment. Using the

Autostep 200 at UCSB, this practically limits spacings to ~1.5 μm with a W_{head} = 700 nm. Alignment tolerance of 0.25 μm can be achieved with local alignment and calibration of the systematic misalignment in the stepper immediately prior to exposure. However, deep etched alignment marks often do not produce enough optical contrast for the Autostep to reliably perform local alignment and thus alignment tolerance ≥0.40 μm should be assumed. To reduce the spacing further, electron beam lithography can be used for its superior alignment at the expense of process time and cost. Given that alignment can be better than 50 nm, the minimum non-self-aligned spacing becomes L_{SDM} = 800 nm.

Ultimately a self-aligned process is desired as it relaxes both the alignment and minimum feature size constraints. Typically, prior to source-drain ohmic evaporation, the high-k gate dielectric needs to be removed in the windows to be evaporated. In non-self-aligned structures this is simply done with 30-60 seconds BHF. In a self-aligned structure, there is no resist masking the T-Gate foot / high-k interface which can result in undercutting of the T-Gate foot. Sample run Ch6-L5G3SD7 sample B die 5 was an attempt at this technique – all devices exhibit Gate-Source shorts while non-self-aligned structures exhibited minimal gate leakage.

Another way to self-aligning is to dry etch the high-k. Because the exposed sections of the T-Gate are capped with Au, they should be minimally affected by most dry etch chemistries. High-k gate dielectrics are notoriously difficult to etch, and no studies have examined the selectivity of etch chemistries of high-k vs. III-V. Multiple studies have examined the selectivity of HfO_2, ZrO_2, and Si in Cl_2 / BCl_3 ICP etch chemistries [29]–[31] and found that increasing BCl_3 concentration generally increases the selectivity [31]. While this chemistry is available at UCSB in the Panasonic ICPs, the chuck temperature is too low to form volatile III-chlorides. As a result, the etch rate of the underlying III-V is only determined by sputtering;

damaged, chemically modified species are left on the surface. Attempts at using this technique resulted in poorly controlled etch depths and large specific contact resistances.

More work can be done to improve the viability of the dry-etched, self-aligned source-drain ohmic contact process. Higher ICP bias resulted in better etching of both the high-k and III-V at the expense of accelerated etch rate in the III-V. Future attempts should use thicker N+ regrowth layers (50 – 80 nm) in conjunction with ICP biases of ~700 W in order to ensure complete removal of the high-k and leave less residue in the contact window.

I. Pad Metal

The final step is to deposit pad metal. The pad metal is used to set the electromagnetic environment and is in a co-planar waveguide (CPW) geometry. From elementary electromagnetics, the closer the ground lines are to the signal line, the more confined the electromagnetic field. Measurements are performed on thick wafers (300 – 750 μm) resulting in substrate mode coupling at $f \geq 30$ GHz. Because S-parameters are measured to 67 GHz, strong field confinement is necessary for $f \geq 30$ GHz. Commercial MOSFETs and HBTs rely on multiple metal layers to provide a low loss microstrip transmission line environment. Metal-to-metal vertical spacings ≤ 5 μm cutoff dielectric slab modes while metal thicknesses of ≥ 1 μm provides low loss. This technique, however, requires that the transistor be encapsulated with a dielectric material. Additional ε_r increases parasitic capacitances while dielectric curing induces stress which can break the T-Gate. State-of-the-art HEMTs rely on wafer thinning, through-substrate-vias (TSVs), and air-bridges in order to provide a low loss microstrip environment and truncate substrate modes [1], [32]. Both approaches add significant process complexity; it is therefore desirable to measure on thick substrates with a CPW and thus close attention must be paid to the pad structure.

At 67 GHz on an InP substrate $\lambda \approx 1.33$ mm meaning that the $\lambda/4$ condition is 325 μm. Because 2" InP wafers are 325 – 600 μm thick and 4" wafers (industry purchased epi) are thicker than 600 μm, it is possible to begin coupling to substrate modes at frequencies below 67 GHz. Additionally, the pad metal must be thick to provide low loss and be resilient to probing. Pad resistance and pad inductance are important when considering on-wafer open-short de-embedding. Because this method assumes perfect open and perfect short, any pad resistance results in error and incomplete de-embedding of the pad structure.

Pads used through this thesis are comprised of a $W_{signal} = 7.1$ μm and $W_{gap} = 6.1$ μm CPW. Additionally, pad metal thicker than 300 nm is necessary to be resilient to probing with Cascade Infinity probes and conductive enough to prevent significant losses.

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4. Generation 1

A. Device Structure and Fabrication

Initial devices were fabricated to demonstrate the feasibility of the entire regrowth MOS-HEMT process and provide a benchmark for future generations. The starting epi structure, shown in **Figure 4.1**, was compromised of a 200 nm $In_{0.52}Al_{0.48}As$ back-barrier, 20 nm InP etch stop, and 100 nm $In_{0.52}Al_{0.48}As$ back-barrier with a 3 / 4 / 5 nm $In_{0.53}Ga_{0.47}As$ / InAs / $In_{0.53}Ga_{0.47}As$ composite channel on an semi-insulating InP substrate. The InP etch stop is present to insure a controllable mesa-thickness and epitaxially smooth field. Both are necessary to maximize T-Gate yield. However, due to the large effective mass of InP and the large quantum well thickness, the etch stop Eigen-state is located near the bottom of the well and is populated 4 x 10^{16} cm^{-3} resulting in a parallel conduction path and thus poor off-state source-drain leakage.

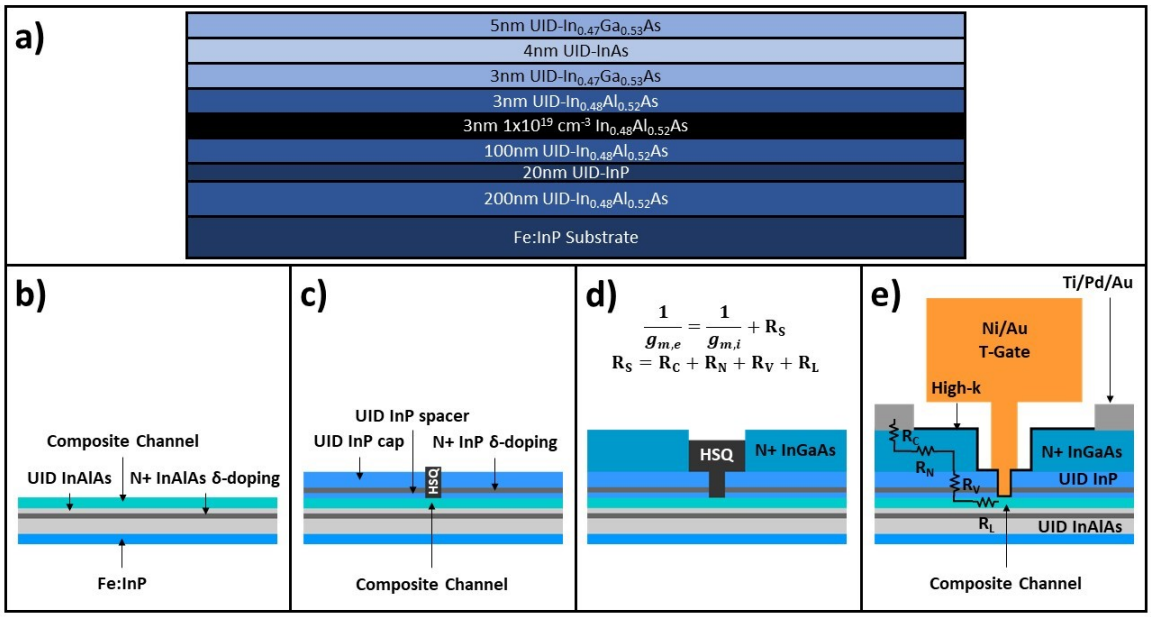

Figure 4.1 a) Beginning epi stack, MBE grown and ordered from IntelliEpi b) Initial starting surface c) First dummy gate and link regrowth d) Second dummy gate and source-drain regrowth e) Final structure after T-Gate metallization and source-drain contact formation

Prior to any device related steps, a 0-layer is exposed to define alignment marks which are necessary for <50 nm realignment. A 5 nm atomic layer deposition (ALD) protection layer of Al_2O_3 is deposited by 50 cycles of trimethyl-aluminum (TMA) and H_2O. The protection layer is chemically similar to the $Al_xO_yN_z$ passivation layer used during the high-k deposition and prohibits photoresist residue from contaminating the channel surface. The alignment marks are defined by UV-lithography using SPR-955 and developed in AZ300-MIF. The 5 nm protection layer is removed in BHF before the alignment marks are deep etched using selective wet chemistry. The target depth of the alignment marks is 1 μm: they must be deep enough to be "seen" in the EBL and shallow enough to planarize / protect during mesa isolation.

The gate recess was defined using an electron beam lithography (EBL) exposure of hydrogen silsesquioxane (HSQ). One cycle of digital etching in dilute HCl was done immediately before loading into the metal organic chemical vapor deposition (MOCVD) chamber. A modulation doped InP link region was then grown at 600°C: 3 nm UID-InP spacer, 2 nm Si:InP 1.0 x 10^{19} cm^{-3} modulation doping, 15 nm UID-InP cap. Hall measurements were performed on parallel samples without dummy gates and yielded electron sheet carrier density and mobility of n_L = 2.5 x 10^{12} cm^{-2} and μ_L = 11,000 cm^2/Vs. The high mobility suggest that the strained InAs is not relaxed and is of high quality. The sheet carrier concentration is lower than that reported in [1] but the mobility double, resulting in similar link sheet resistance (ρ_L).

The first dummy gate is then removed in BHF. It should be noted that the process of depositing and removing the ALD Al_2O_3 thins the channel by 0.5 – 1.0 nm/cycle. This must be accounted for when designing the channel epi since this process is repeated three times: alignment mark lithography and strip, dummy gate 1 lithography and strip, dummy gate 2

lithography and strip. The second dummy gate is then defined by the same HSQ EBL process where $L_{DG2} = L_{DG1}$ + 100 nm providing symmetric 50 nm gate-source and gate-drain recesses. A single digital etch in dilute HCl, to clean the surface, was done immediately prior to re-loading into the MOCVD chamber and re-growing 60 nm N+ $In_{0.53}Ga_{0.47}As$ (target 4 x 10^{19} cm^{-3}) source-drain regions on-top of the modulation doped InP.

Growth steps define the electronic band-structure in the channel, modulation doped link regions, and source-drain contact regions. Post-growth steps involve mesa isolation, high-k deposition, T-Gate formation, and source-drain metallization. The second dummy gate is left in place during mesa isolation to protect the channel interface from contamination. The mesa is etched with a series of selective chemistries stopping on the 200 nm $In_{0.52}Al_{0.48}As$ back-barrier resulting in $d_{mesa} \approx 200$ nm. The mesa resist is then removed in NMP and the second dummy gate removed by BHF. The intrinsic channel region was then thinned using 3 cycles of UV-ozone and HCl:H_2O 1:10. Immediately prior to loading in the ALD, a BHF dip was done to remove the native oxide. To clean/passivate the surface, 9 cycles of TMA + 100W Nitrogen plasma were used followed by 40 cycles of ZrO_2. The high-k was then annealed in forming gas at 400°C to passivate dangling bonds at the high-k / semiconductor interface.

Next the T-Gate was formed by a two-step lithography were the foot was exposed and developed using CSAR:Anisole 1:1 and Amyl Acetate and the head using UV6-0.8 and AZ300-MIF. The 30 nm Ni / 300 nm Au T-Gate was then thermally evaporated, stripped, and annealed at 350°C in H_2 in the ALD to recover any UV-damage accumulated during evaporation. Finally, the source-drain vias were exposed and etched using BHF and 20/20/100 nm Ti/Pd/Au source-drain metal was electron beam evaporated and lifted-off.

Figure 4.2 shows a cross-sectional TEM of a drawn 22 nm, (011) conduction device. Excellent alignment of dummy gate 2 to dummy gate 1 is observed as well as excellent re-alignment of the T-Gate to the gate recess. Minimal gate metal overlap is observed which is critical to maintain low gate-source fringe capacitance ($C_{GS,f}$). Gradual faceting is observed in the link regrowth at the gate edge consistent with the {201}. It is unlikely that the modulation doping behaves as designed in the faceted regions of regrowth, likely resulting in reduced n_L near the gate edge. This potentially can result in large R_S due to large R_L. Devices oriented with $(0\bar{1}1)$ conduction exhibit vertical (011) faceting with {201} forming on-top, shown in **Figure 4.2**. This results in a larger separation of the parasitic gate metal overlap to source-side two-dimensional electron gas (2DEG) yielding lower $C_{GS,f}$ than (011) conduction devices.

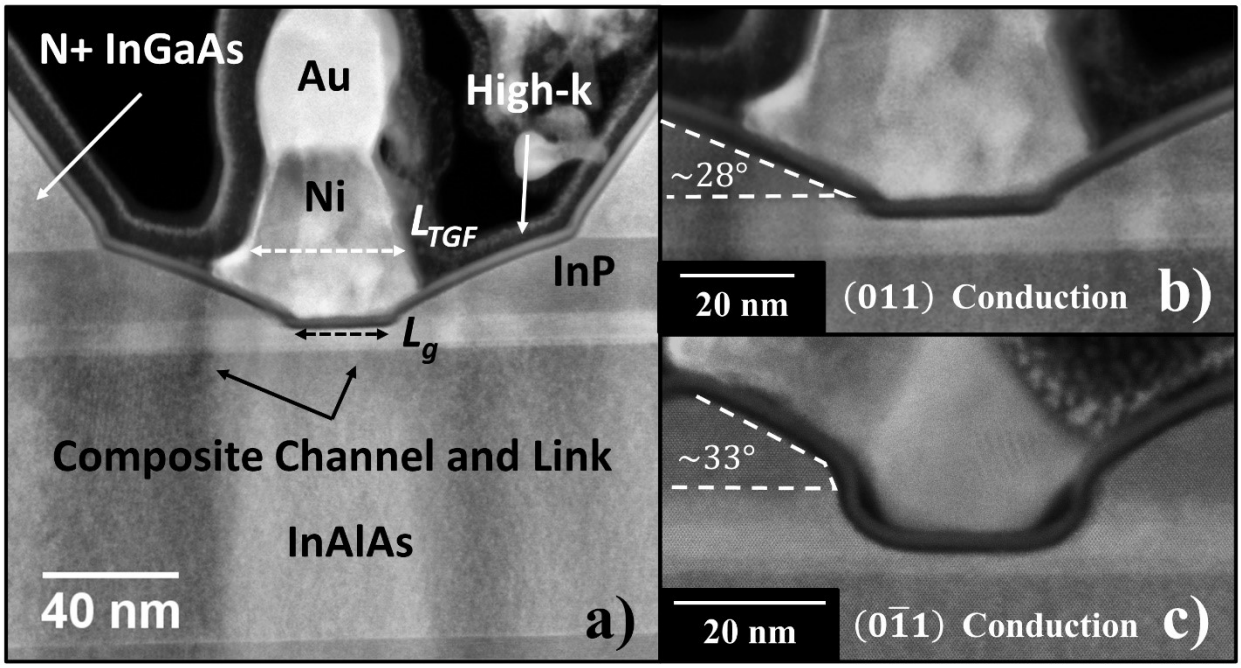

Figure 4.2 a) Cross-section TEM device structure b) (011) conduction devices [Generation 1 device shown] and c) $(\mathbf{0\bar{1}1})$ conduction devices [Generation 2 device shown]

B. Band Diagrams

Band diagrams were calculated using the 1D self-consistent Schrödinger-Poisson solver, BandProf: the source-drain, link quantum well, and channel region at V_{GS} = 0.0 V are illustrated in **Figure 4.3**. The degenerate doping of the N+ $In_{0.53}Ga_{0.47}As$ pulls the conduction band of the UID-InP link cap down making it conductive. A triangular barrier, 82 meV high by 4.0 nm wide, is present beneath the source-drain region due to the depleted modulation doping. The designed link quantum well charge density is $n_{Link} \approx 4.0 – 5.0 \times 10^{12}$ cm^{-2} while the Hall measured $n_{Link} \approx 2.5 \times 10^{12}$ cm^{-2}. The small CBO of InP | $In_{0.53}Ga_{0.47}As$ prevents further modulation doping from being added in top-side modulation doping without thinning the UID-InP link cap.

In the intrinsic channel, the back-side modulation doping pulls the back-barrier conduction band minimum down beyond the plane of modulation doping. As a result, maximum ($E_F – E_1$) is expected to occur when the back-side parallel 2DEG begins populating (i.e. roughly CBO – 0.2 eV). When this occurs, $n_{ch} \approx 7.5 \times 10^{12}$ cm^{-2} suggesting that source-starvation will occur before and be the primary limitation of I_{DS} and g_m.

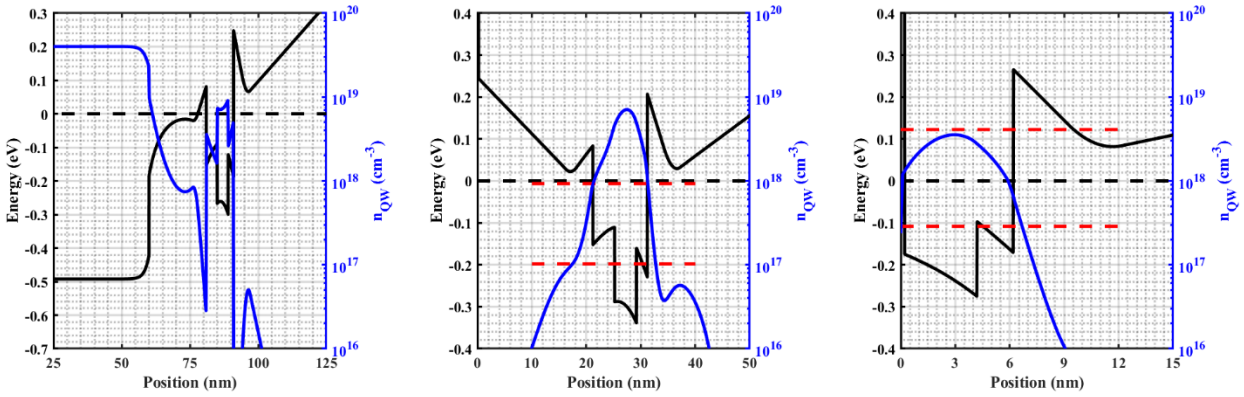

Figure 4.3. Band diagrams for Generation 1 devices

C. DC Results

Initial MOS-HEMT results reported in [1], exhibited peak DC $g_{m,e}$ = 1.5 mS/μm at V_{DS} = 0.5 V using t_{ch} = 5 nm. By reducing the source-drain metal spacing from L_{SD} = 5 μm to L_{SD} = 2 μm and increasing t_{ch} to 6.5 nm, peak DC $g_{m,e}$ = 2.23 mS/μm is observed at V_{DS} = 0.5 V, V_{GS} = 0.3 V and I_{DS} = 0.93 mA/μm. Transfer and output characteristics of three representative devices are shown in **Figure 4.4**. Device 1 is L_g = 8 nm $(0\bar{1}1)$ conduction [peak f_τ], device 2 is L_g = 22 nm (011) conduction [peak $g_{m,e}$], and device 3 is L_g = 90 nm $(0\bar{1}1)$ conduction (peak f_{max}).

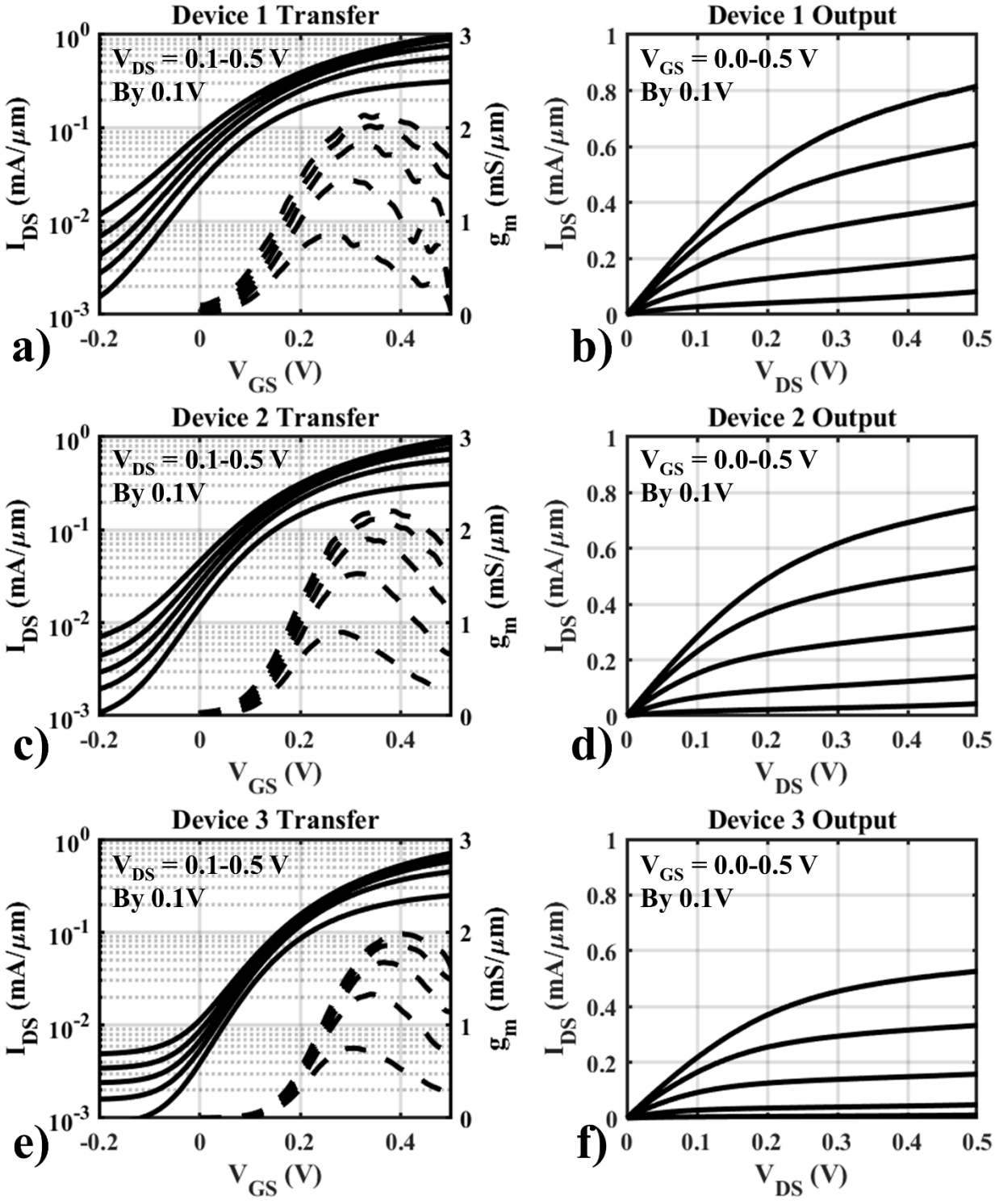

Figure 4.4 Transfer and output characteristics of three representative devices

The off-state leakage current is extremely high (1 µA/µm at V_{DS} = 0.1 V) and independent of gate length suggesting parallel conduction. The off-state resistance increases with decreasing mesa width suggesting leakage through the quantum well etch stop rather than along the mesa sidewalls. Unfortunately, the steepest part of the sub-threshold slope (SS_{min}) is likely convoluted with the leakage. Looking at *SS* vs. L_g is not meaningful for these devices. **Figure 4.5** shows the peak transconductance, minimum *SS*, and DIBL as a function of L_g for Generation 1 devices. Peak DC $g_{m,e}$ plateaus at ~2.2 mS/µm for $L_g \leq 50$ nm. Because of the thick channel, it is not surprising to see ballistically limited conduction achieved at $L_g \geq 20$ nm as the mean free path is expected to be long.

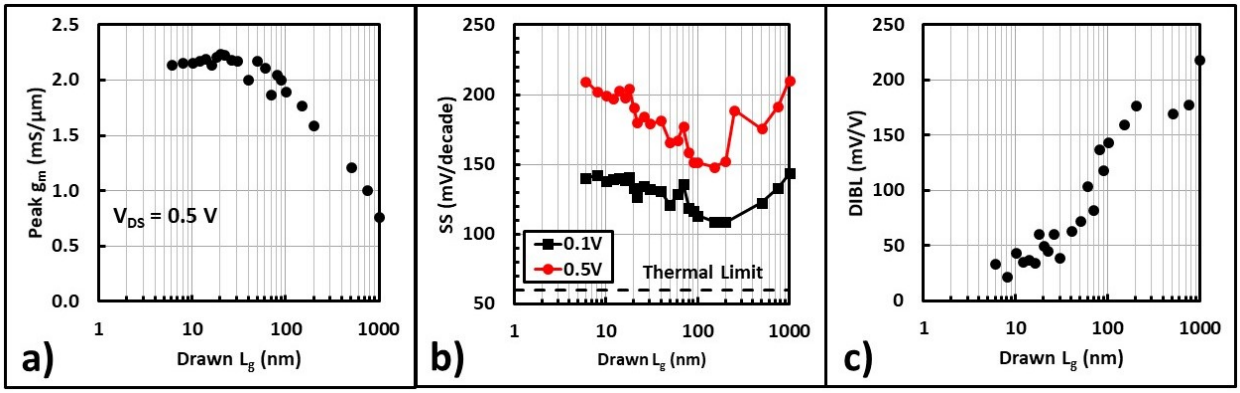

Figure 4.5 DC lot characterization of Generation 1 devices a) Peak transconductance b) *SS* at V_{DS} = 0.1 V and 0.5 V c) DIBL

While the true SS_{min} is convoluted with the source-drain leakage, the observed SS_{min} decreases with increasing L_g as expected due to improved electrostatics. At $L_g \geq 200$ nm, SS_{min} abnormally increases. This increase is because of the smaller I_{on} due to higher R_{ch} at a given V_{DS} for long gate length devices. Consequently, the transfer curve begins to roll over at lower I_{DS}. Given that the off-state leakage is set, not by the channel but by the etch-stop conductivity, the swing between I_{off} and I_{on} is smaller and the steepest part of the curve – usually observed at small V_{GS}, V_{DS} and I_{DS} – is likely found at $I_{DS} < I_{off}$, shown in **Figure 4.6**.

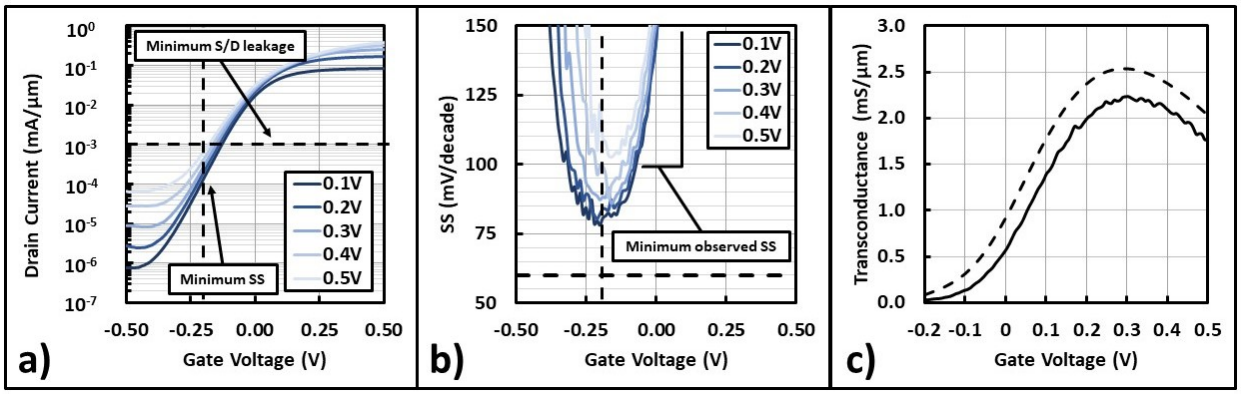

Figure 4.6 L_g = 150 nm device from device run Ch5-L3G3SD3 illustrating where minimum *SS* occurs and why it is not observed for Generation 1 devices a) transfer characteristics b) *SS* as a function of V_{GS} c) DC and 1 GHz $g_{m,e}$ for drawn L_g = 22 nm Generation 1 device at V_{DS} = 0.5 V

In this case, SS_{min} cannot be used to infer the quality of the oxide / semiconductor interface. Another way to estimate the quality of the oxide / semiconductor interface is to compare the DC and RF $g_{m,e}$. Because traps can only respond to f < 1 MHz, measuring the transistor at f > 1 MHz prevents the traps from responding and thus contributing to the measurement. **Figure 4.6c** illustrates the observed DC and 1 GHz $g_{m,e}$ for Generation 1 devices. Peak DC $g_{m,e}$ at V_{DS} = 0.5 V is 2.23 mS/μm while peak $g_{m,e}$ at 1 GHz is 2.53 mS/μm. This is a 12% deviation, consistent with [1], suggesting the quality of the high-k / semiconductor interface.

DIBL is opposite of the expected trend: better electrostatics should cause DIBL to decrease as L_g increases. Because the etch stop causes leakage on the order of the threshold current, extraction of the threshold voltage, especially at large V_{DS}, is not reliable. Additionally, comparing Generation 1 devices DIBL to previous works is not meaningful because [2]–[4] defines V_{TH} as 1 μA/μm which is the observed $I_{off,min}$. Rather than using constant current, V_{TH} was determined by extrapolating the linear portion of ($V_{GS} - V_{TH}$).

Because etch stop leakage prevents the proper extraction of *SS*, I_{off}, and DIBL and will be convoluted with G_{DS} (as a parallel R_{Leak}) in RF measurements, extracting a value is useful. R_{off}

is extracted by fitting I_{DS} vs. V_{DS} at V_{GS} = -0.2 V. For $L_g \geq 100$ nm, R_{off} represents the resistivity of the etch stop (R_{Leak}) while $L_g \leq 100$ nm exhibits a convolution of I_{off} and I_{Leak}, especially at V_{DS} = 0.5 V. Furthermore, long gate length devices exhibit a constant R_{off} while R_{off} varies with L_g for short gate lengths, shown in **Figure 4.7**.

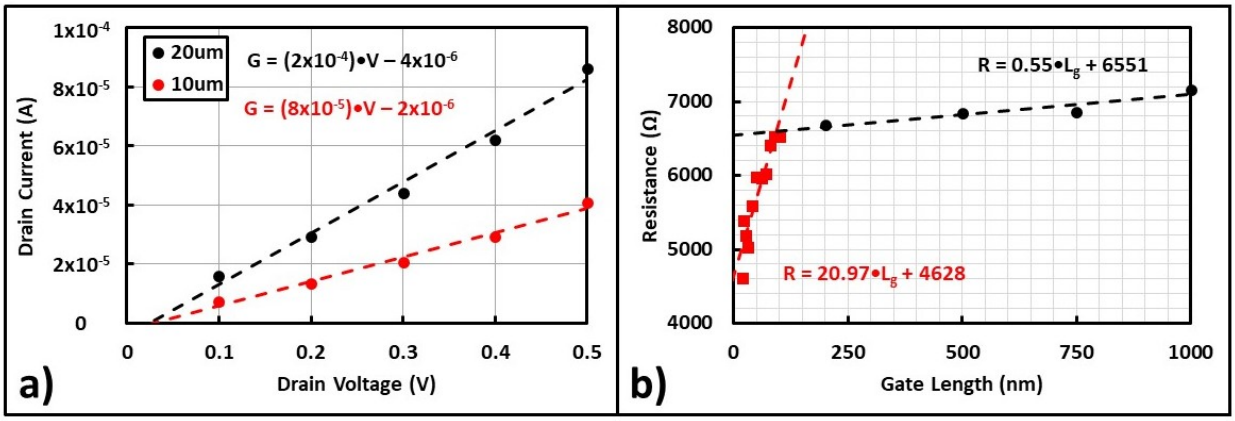

Figure 4.7 a) Extraction of etch stop conductance for L_g = 1 µm devices at W_g = 20 µm and W_g = 10 µm b) R_{off} vs L_g for W_g = 20 µm

Figure 4.8 shows two sets of TLMs used to estimate components of source-resistance. First, the N+ TLMs give R_N = 22 Ω•µm and R_C = 8 Ω•µm. The link TLMs give R_L = 13 Ω•µm and R_A = 69 Ω•µm resulting in a total R_S = 112 Ω•µm. Extrapolating R_{on} vs L_g gives R_S = 162 Ω•µm, ~50% larger than the source resistance measured by TLM, suggesting possible source-side depletion at high V_{GS} as $n_{ch} > n_{Link}$.

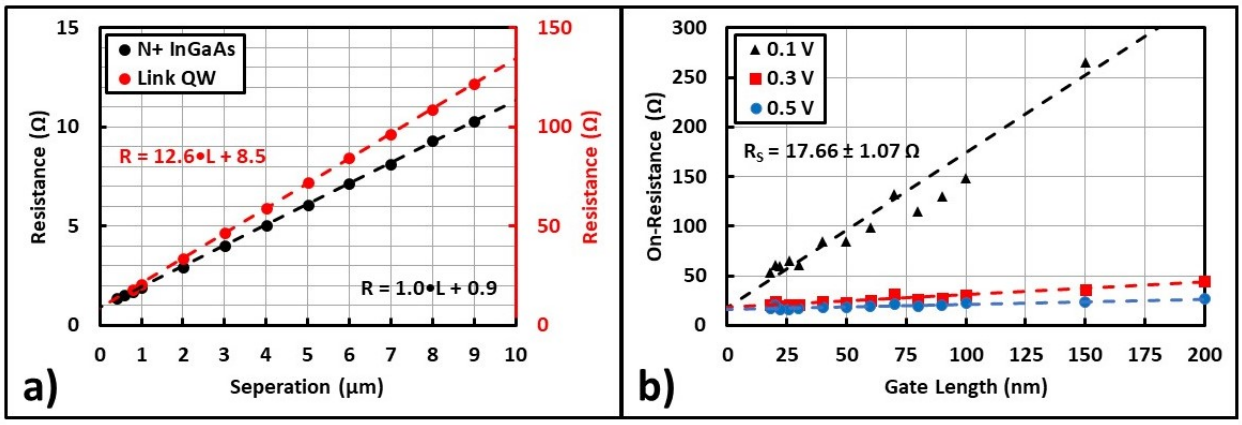

Figure 4.8 Extracted resistances a) N+ InGaAs and Link Quantum Well TLMs b) On-resistance measurements at various ($V_{GS} - V_{TH}$)

D. RF Results

A drawn L_g = 8 nm device oriented with conduction in $(0\bar{1}1)$ exhibited peak f_τ = 511 GHz and peak f_{max} = 285 GHz while a drawn L_g = 90 nm device oriented with conduction in (011) exhibited peak f_τ = 286 GHz and peak f_{max} = 460 GHz. Figure of merit (FOM) contour plots and extraction at peak (f_τ , f_{max}) are shown in **Figure 4.10**.

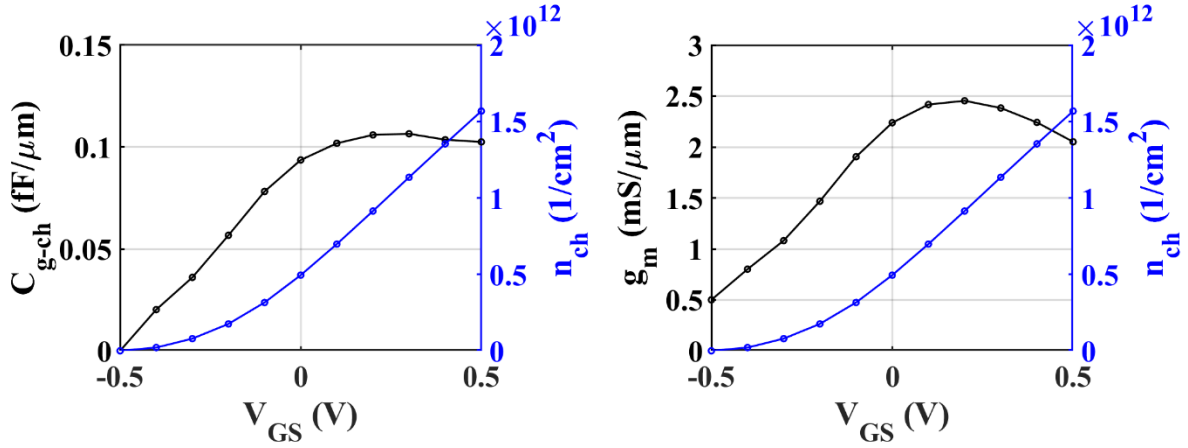

Figure 4.9 L_g = 8 nm $(\mathbf{0\bar{1}1})$ conduction device, S-parameter extracted a) CV-characteristics b) n_{ch}, $g_{m,e}$ vs. V_{GS} at V_{DS} = 0.7 V

Short gate length devices oriented in the $(0\bar{1}1)$ generally exhibit higher f_τ than those oriented in (011). This is likely due to the steeper faceting observed in the link regrowth at the

gate edges. As a result, the gate metal is further separated from the source-side 2DEG resulting in lower $C_{GS,f}$. Additionally, by the lever rule, the further the link surface is from the link quantum well, the more charge will image in the link quantum well for a given modulation doping. At peak g_m bias (large $V_{GS} - V_{TH}$) the channel is strongly inverted and $n_{ch} \approx n_{Link}$. To prevent source starvation to higher ($V_{GS} - V_{TH}$), maximizing n_{Link} is critical, implying that the link surface needs to be far from the plane of modulation doping. Since the vertical faceting realized in $(0\bar{1}1)$ oriented devices moves the semiconductor surface further away from the plane of modulation doping, it is expected that $(0\bar{1}1)$ conduction devices should exhibit larger n_{Link} at the gate edge. This means that the source-side 2DEG can supply more electrons, preventing source-side depletion to higher biases. S-parameter extracted CV characteristics are shown in **Figure 4.9** for a L_g = 8 nm $(0\bar{1}1)$ conduction device. From **Figure 4.9** and **Figure 4.11**, $C_{GS,i}$ = 0.1 fF/μm and $C_{GS,f} \approx$ 0.5 fF/μm. Clearly the parasitic T-gate overlap is limiting the high frequency performance.

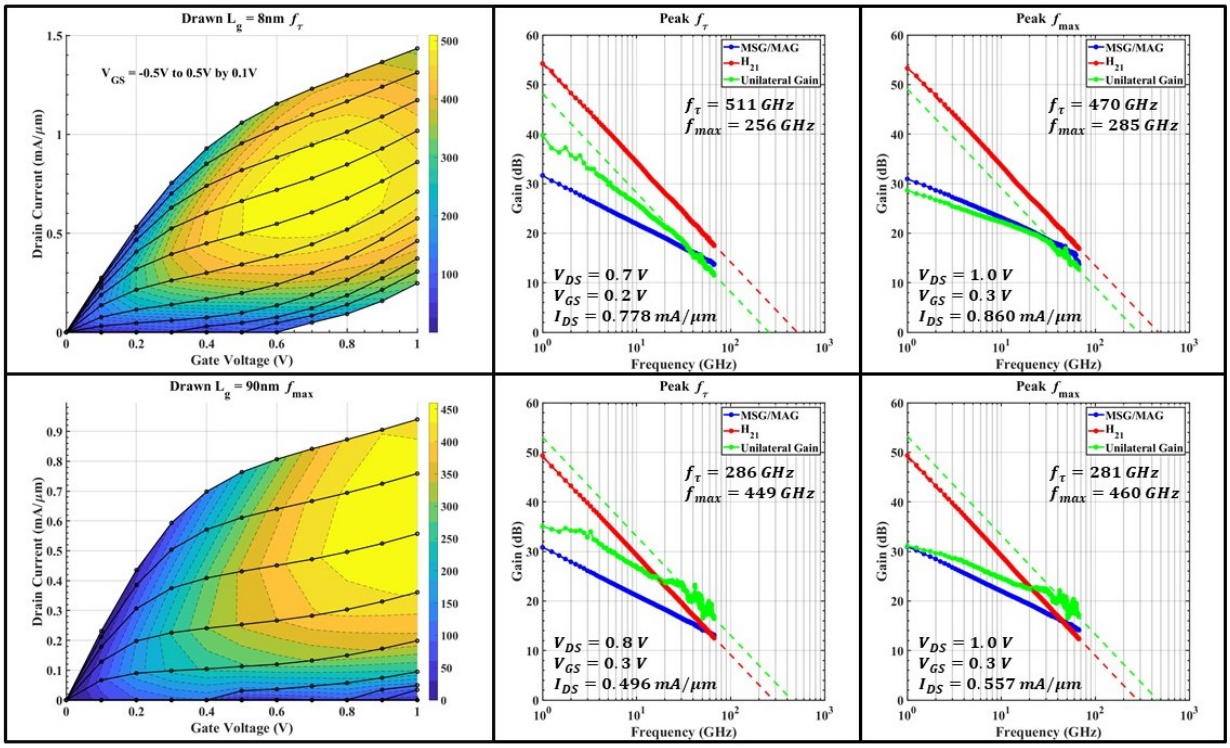

Figure 4.10 (top) L_g = 8 nm $(0\bar{1}1)$ oriented device (left) f_τ contour plot (middle) FOM fitting at peak f_τ (right) FOM fitting at peak f_{max} (bottom) L_g = 90 nm (011) oriented device (left) f_τ contour plot (middle) FOM fitting at peak f_τ (right) FOM fitting at peak f_{max}

Short gate length devices often exhibit high f_τ but low f_{max} because of large R_G, G_{DS}, C_{GS} and R_{Leak}. **Figure 4.11** shows the distribution of FOMs for (011) and $(0\bar{1}1)$ oriented devices versus L_g as well as extracted C_{GS}, C_{GD}, R_G, $g_{m,e}$, and $G_{DS,e}$. While $C_{GD} \approx 0.2$ fF/μm is consistent with state-of-the-art HEMTs, $C_{GS} \approx 0.6$ fF/μm is large for $L_g \leq 50$ nm devices. Large C_{GS} is due to large $C_{GS,i}$ associated with C_{ins} inherent to the MOS-HEMT and large $C_{GS,f}$ due to the parasitic T-Gate overlap in regrown regions. The T-Gate overlap manifests itself as an additional parallel plate capacitor between the T-Gate foot metal and 2DEG on the source side. Because of the gradual faceting observed at the gate edge, illustrated in **Figure 4.4**, $C_{GS,f}$ is larger than designed. Additionally, the spacing between the T-Gate foot metal and source-

side 2DEG is larger for $(0\bar{1}1)$ devices compared to (011) devices resulting in smaller $C_{GS,f}$ for $(0\bar{1}1)$ devices.

The extracted gate resistance for $L_g \leq 50$ nm severely limits power gain. Large R_G is a result of poor T-Gate stem filling due to shadowing in the thermal evaporator. Typically, larger f_{max} can be realized at smaller W_{mesa} because end-to-end R_G is smaller. However, that is not observed in Generation 1 devices because R_G is predominately due to a vertical resistance component associated with T-Gate "necking".

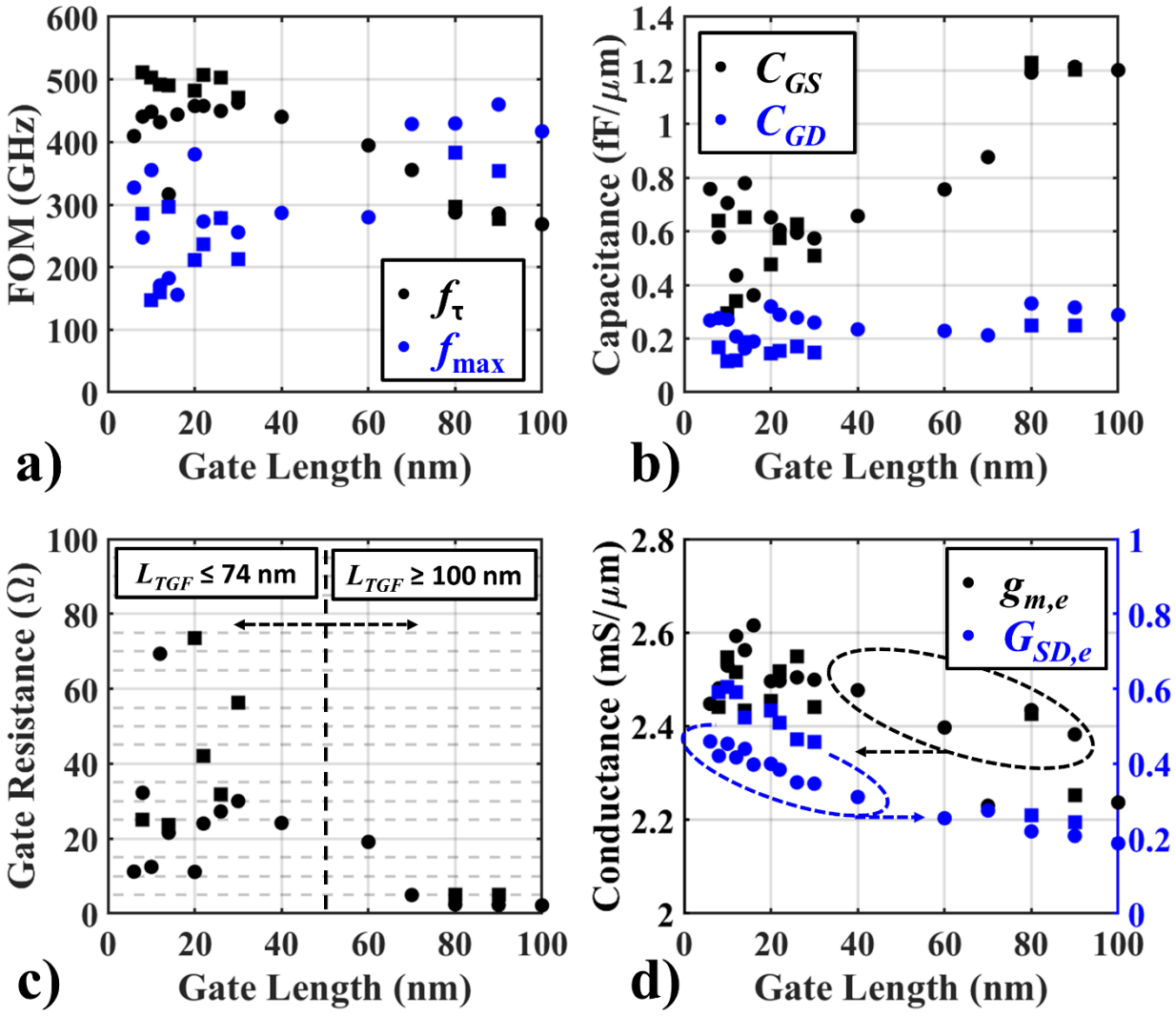

Figure 4.11 Extracted equivalent circuit parameters at peak f_τ bias where circles are (011) conduction and triangles are (0-11) conduction a) f_τ, f_{max} b) C_{GS} and C_{GD} c) R_G d) $g_{m,e}$ and $G_{DS,e}$

Extracted $g_{m,e}$ is flat for $L_g \leq 100$ nm, peaking at 2.6 mS/μm and only moderately rolling off for $L_g \leq 10$ nm. At extremely short gate lengths, a g_m roll-off is expected due to loss of aspect ratio and poor electrostatics. Roll-off in g_m is not expected until V_{DS} is large enough to fully deplete the drain side. Due to the recess structure, the drain 2DEG ($n_{Link} = 2.5 \times 10^{12}$ cm^{-2}) can deplete, absorbing $V_{DS} = 0.5$ V in less than 30 nm. Consequently, significant roll off is not expected until $V_{DS} \geq 0.5$ V . Because $f_{\max}$ requires small C_{GD} and large $g_{m,e}$, the peak $f_{\max}$ condition is expected to occur at a V_{DS} were $g_{m,e}$ is maximized and C_{GD} is minimized. C_{GD} will reach a minimum when the drain 2DEG fully depletes – leaving only fringing capacitances through the substrate. $g_{m,e}$ will maximize and begin to roll off at the same time – as the drain begins to influence the channel without the drain 2DEG as an electrostatic buffer. Consequently, we expect to find $f_{\max}$ at this bias. The approximate drain side depletion can be easily calculated from Poisson's Law in 1D:

$$V_{DS} = \frac{q n_{Link} L_{GD}}{2\varepsilon_{ch}} \tag{4.4.1}$$

Using $n_{Link} = 2.5 \times 10^{12}$ cm^{-2}, $\varepsilon_{r,ch} \approx 12$, and $L_{GD} = 50$ nm, the drain side will fully deplete at $V_{DS} = 1.0$ V. Peak $f_{\max}$ is often observed at $V_{DS} = 1.0$ V. Extracted $G_{DS,e}$ is ~0.45 mS/μm for $L_g \leq 50$ nm and ~0.20 mS/μm for $L_g \geq 50$ nm at peak f_τ bias. This is larger than $G_{DS,e} = 0.2$ mS/μm for $L_g = 30$ nm reported in [1]. The leaky etch stop layer in Generation 1 devices manifests itself as a resistor between source and drain, in parallel with the channel. As a result, increasing V_{DS} will give additional I_{DS} through the etch stop layer: $R_{Leak} = \mathrm{d}V_{DS}/\mathrm{d}I_{DS}$. Given that this is $1/G_{DS}$, it is difficult to differentiate the two effects. Consequently, the extracted values are $G_{DS,e} \parallel R_{Leak}$. Because fitting is not unique, $G_{DS,i} \approx R_{Leak}$ makes it difficult to extract meaningful values for either parameter.

Extracted $g_{m,e}$, $G_{DS,e}$, C_{GS}, and C_{GD} as a function of V_{DS} at V_{GS} = 0.2 V are illustrated in **Figure 4.12**. Peak f_τ occurs at V_{DS} = 0.7 V where $g_{m,e}$ is maximized and (C_{GS} + C_{GD}) is minimized. Gate-drain capacitance decreases as V_{DS} increases due to additional depletion of the drain side while G_{DS} minimizes at V_{DS} = 0.7 V and then increases as the drain-side depletion region begins to encroach into the channel. Interestingly, peak f_{max} does not occur at peak $g_{m,e}/G_{DS,e}$; however, this may be an artifact of the poor extraction of $G_{DS,e}$ at high V_{DS}.

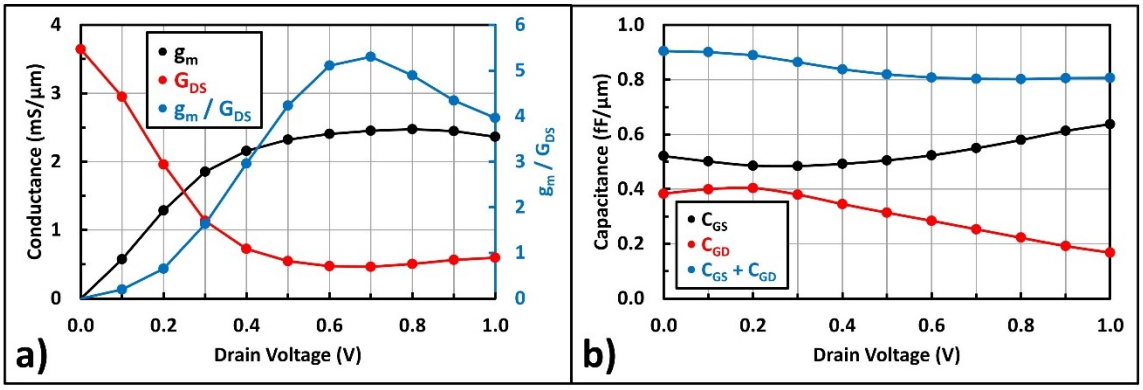

Figure 4.12 Extracted equivalent circuit parameters from Y-parameter fitting drawn L_g = 8 nm, W_{mesa} = 20 μm, 2 finger device oriented in $(\mathbf{0\bar{1}1})$ under peak f_τ bias of V_{DS} = 0.7 and V_{GS} = 0.2 V a) $g_{m,e}$ and $G_{DS,e}$ b) C_{GS} and C_{GD}

E. 8nm Equivalent Circuit Model

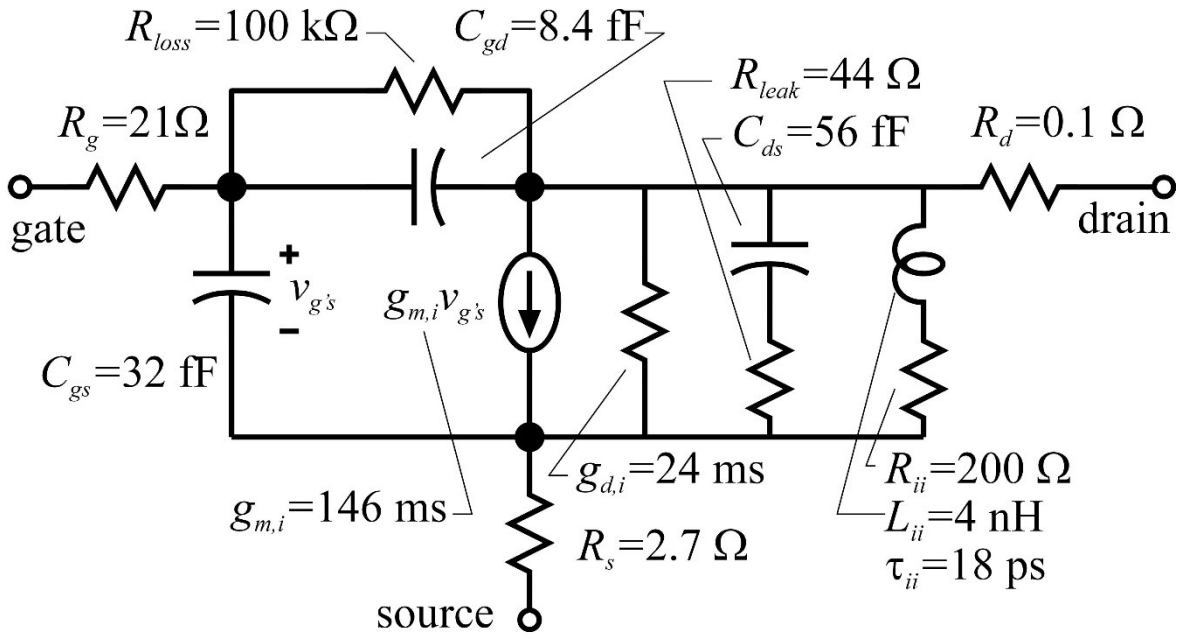

Figure 4.13 Equivalent circuit model of drawn L_g = 8 nm, W_{mesa} = 20 µm, 2 finger device oriented in $(0\bar{1}1)$ under peak f_τ bias of V_{DS} = 0.7 and V_{GS} = 0.2 V

The equivalent circuit model for a L_g = 8 nm, f_τ = 511 GHz device is shown in **Figure 4.13**, measured and fit Z-parameters in **Figure 4.14**, and measured and fit Y-parameters in **Figure 4.15**. Extraction of the equivalent circuit is as follows.

Measured S-parameters are converted to Z-parameters and fit at large V_{GS} (fully inverted) and V_{DS} = 0.0 V to extract R_S, R_D, and R_G. At zero V_{DS}, the source and drain are symmetric, R_S = R_D. At higher V_{DS} the drain depletes and R_D decreases (i.e. at V_{DS} > 0.0 V, R_D < R_S). The faceting observed at the gate-source edge, shown in **Figure 4.2**, likely results in gate modulation of the source-side 2DEG near the gate edge. Like the channel charge, the source-side n_{Link} in the overlapped region likely increases as V_{GS} increases. Because the measured 2DEG charge density is 2.5 x 10^{12} cm^{-2}, unintentional modulation of it is expected to only

minorly effect the conductivity. In this section, the assumption is that R_S independent of both V_{DS} and V_{GS}. Extracted R_S = 108 Ω•µm is consistent with the 112 Ω•µm measured by TLM.

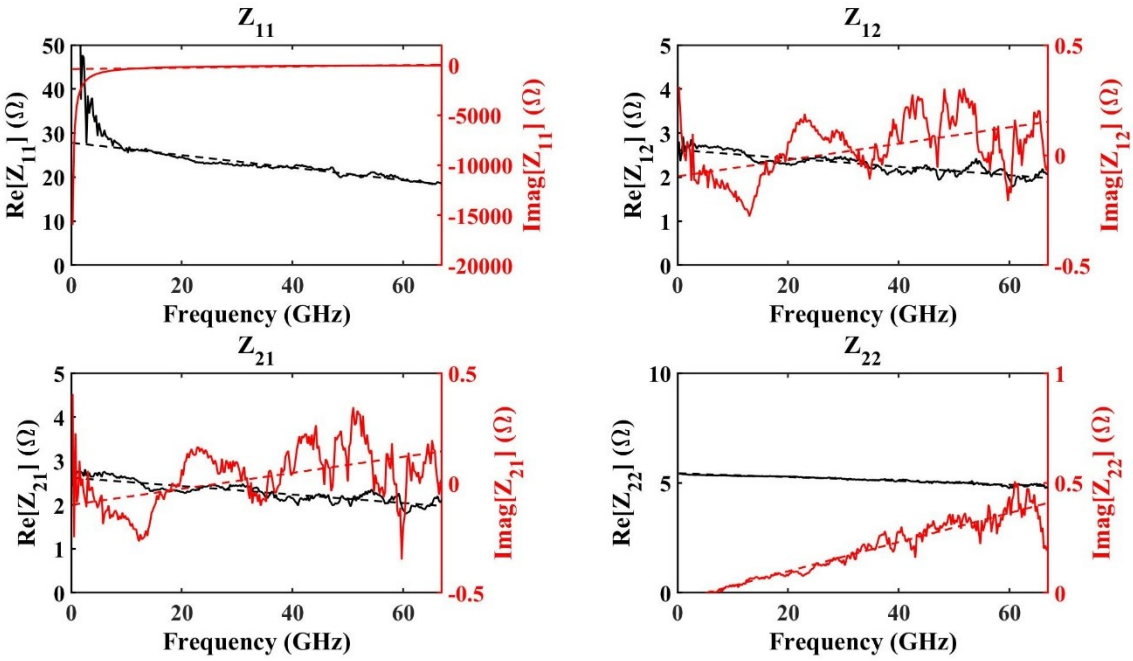

Figure 4.14 Measured and fit Z-parameters drawn L_g = 8 nm, W_{mesa} = 20 µm, 2 finger device oriented in $(0\bar{1}1)$ under peak f_τ bias of V_{DS} = 0.7 and V_{GS} = 0.2 V shown with automatic fitting

Next, Z-parameters are converted to Y-parameters and the intrinsic device is fit at the bias of interest (peak f_τ). Intrinsic parameters C_{GS}, C_{GD}, and $g_{m,e}$ are easily extracted while additional parameters such as G_{DS} and C_{DS} are more challenging. Both Imag(Y_{12}) and Imag(Y_{11}) are well conditioned and extraction of C_{GS} and C_{GD} are reliable. Re(Y_{11}) and Re(Y_{12}) exhibit significant curvature due to large R_G but are well conditioned with the extracted value. Interestingly Re(Y_{21}) remains flat with frequency. Short-open de-embedded Y-parameters exhibits the expected decreasing Re(Y_{21}) with frequency, however open-short de-embedding provided a more conservative FOM extrapolation and is thus used instead: extracted $g_{m,i}$ = 3.65 mS/µm. Low frequency Y_{22} exhibits a resonance attributed to the parasitic

bipolar current gain caused by the creation of electron-hole pairs at the drain edge under larger V_{DS}. The base level extraction does not consider this effect and therefore does not fit this region. Therefore, the parabolic fit of $\mathrm{Re}(Y_{22})$ is poorly condition and the initially extracted G_{DS} is unreliable. The low frequency resonance fits with a series LR network of 4 nH and 200 Ω giving a hole lifetime (τ_p) of 18 ps.

$\mathrm{Imag}(Y_{22})$ is difficult to fit due to large C_{DS} and R_G as well as small R_{Leak}. A series $C_{DS}R_{Leak}$ is used to improve the fit of Y_{22}. Extracted C_{DS} is very large while R_{Leak} is very small; both are attributed to the leaky etch stop layer: C_{DS} = 1.40 fF/μm and R_{Leak} = 1.76 kΩ•μm. R_{Leak} extracted from Y-parameters is less than half that determined in **Section C**, shown in **Figure 4.7**. Thermal emission of carriers over the conduction band minimum of the $In_{0.52}Al_{0.48}As$ back-barrier at large V_{DS}, similar to mechanism proposed in [5], could explain the reduced R_{Leak}. Because R_{Leak}, R_{II}, and $1/G_{DS}$ are all comparable and in parallel, it is unreliable to claim a precise number for any.

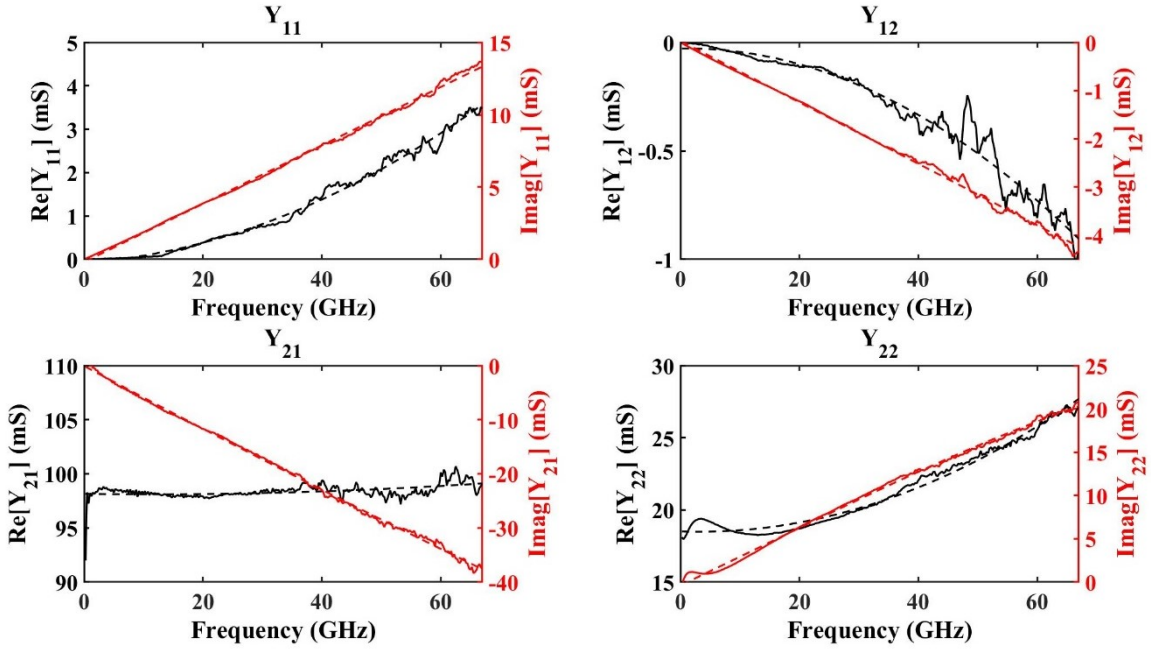

Figure 4.15 Measured and fit Y-parameters for drawn L_g = 8 nm, W_{mesa} = 20 µm, 2 finger device oriented in $(0\bar{1}1)$ under peak f_τ bias of V_{DS} = 0.7 and V_{GS} = 0.2 V shown with automatic fitting

From the Y-parameters discussed in **Chapter 2**, it is evident that higher order terms are present in the measured data. Because the extraction done by automatic fitting only considers linear and parabolic terms, the extracted values do not provide an optimal fit to the measured S-parameters. In order to accurately account for the higher order terms, the device was modeled at peak f_τ in ADS and the resulting equivalent circuit is shown in **Figure 4.13**. Measured and modeled S-parameters and high-frequency FOMs are shown in **Figure 4.16**. Modeled f_τ is comparable to the extrapolated f_τ while f_{max} is difficult to determine by the model due to >20 dB/dec roll off observed likely due to higher order terms associated with R_G, C_{DS}, and R_{leak}.

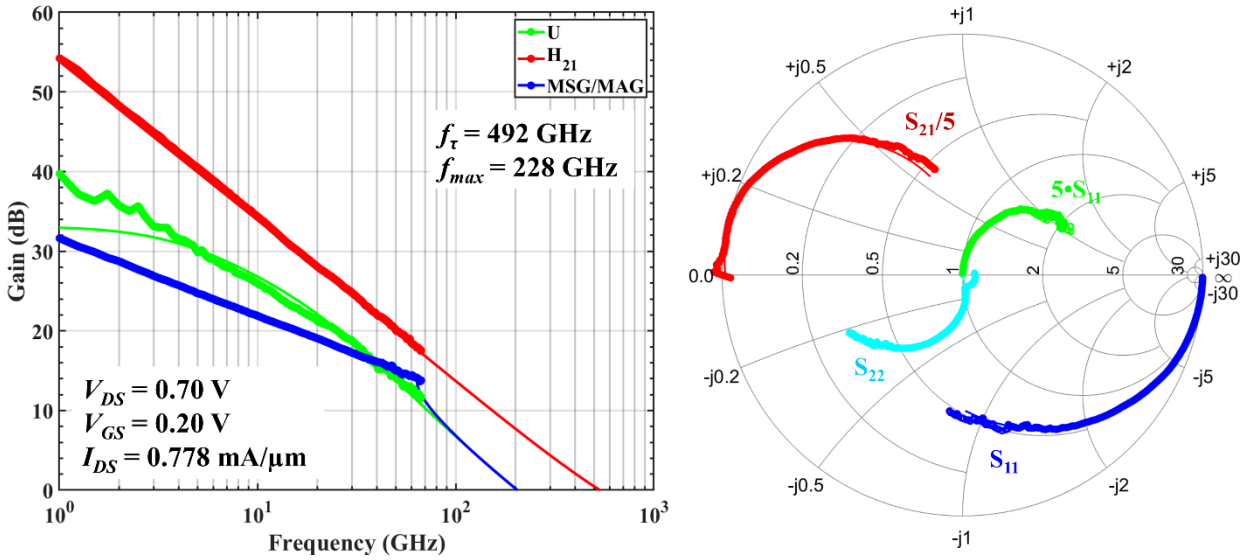

Figure 4.16 Measured and modeled S-parameters and high-frequency FOMs for L_g = 8nm $(0\bar{1}1)$ device biased for peak f_τ

F. Summary

In this section, we have reported 6.5 nm thick, InAs / $In_{0.53}Ga_{0.47}As$ composite channel MOS-HEMTs exhibiting peak $g_{m,e}$ = 2.23 mS/µm at V_{DS} = 0.5 V and R_S = 170 Ω•µm. A drawn L_g = 8 nm $(0\bar{1}1)$ conduction device exhibited peak f_τ = 511 GHz while a drawn L_g = 90 nm (011) exhibited peak f_{max} = 460 GHz. Power gain in short L_g devices is limited by large R_G attributed to poor T-Gate metal filling. Because of the several parasitic components are severely limiting the performance (R_G, C_{DS} and R_{Leak}) it is useful to modify the SSEC to predict the peak performance of the intrinsic device. Improving R_G = 21 Ω to R_G = 7 Ω while eliminating the leaky etch would increase f_τ from 511 GHz to >600 GHz and f_{max} from 256 GHz to >500 GHz as shown in **Figure 4.17**. R_G = 7 Ω is commonly observed for Generation 2, W_{mesa} = 20 µm devices. $C_{GD} \leq$ 0.2 fF/µm and $G_{DS,e}$ = 0.2 mS/µm is commonly observed in Generation 3 devices which have a thicker channel and no leaky etch stop.

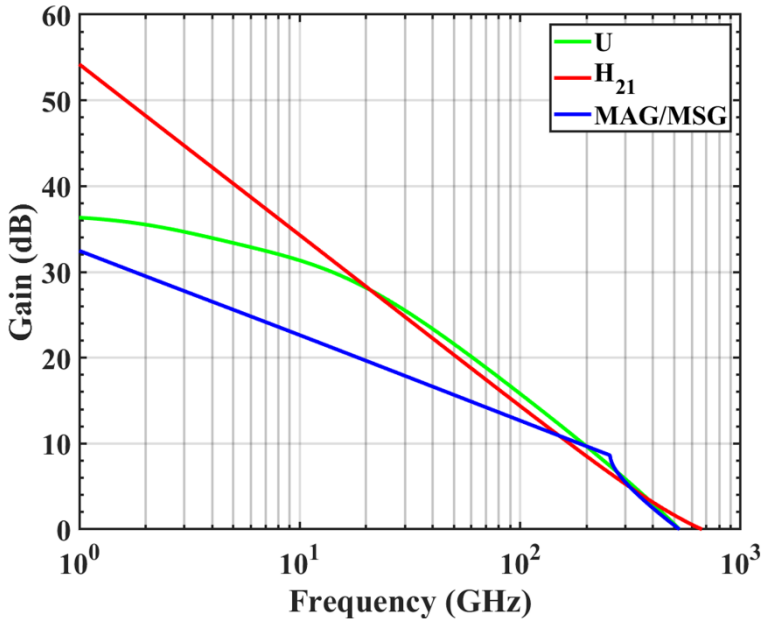

Figure 4.17 Simulated high-frequency FOMs for Generation 1 L_g = 8 nm device with R_G = 7 Ω, C_{GD} = 0.2 fF/um, and G_{DS} = 0.2 mS/um

References

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5. Generation 2

A. Device Structure and Fabrication

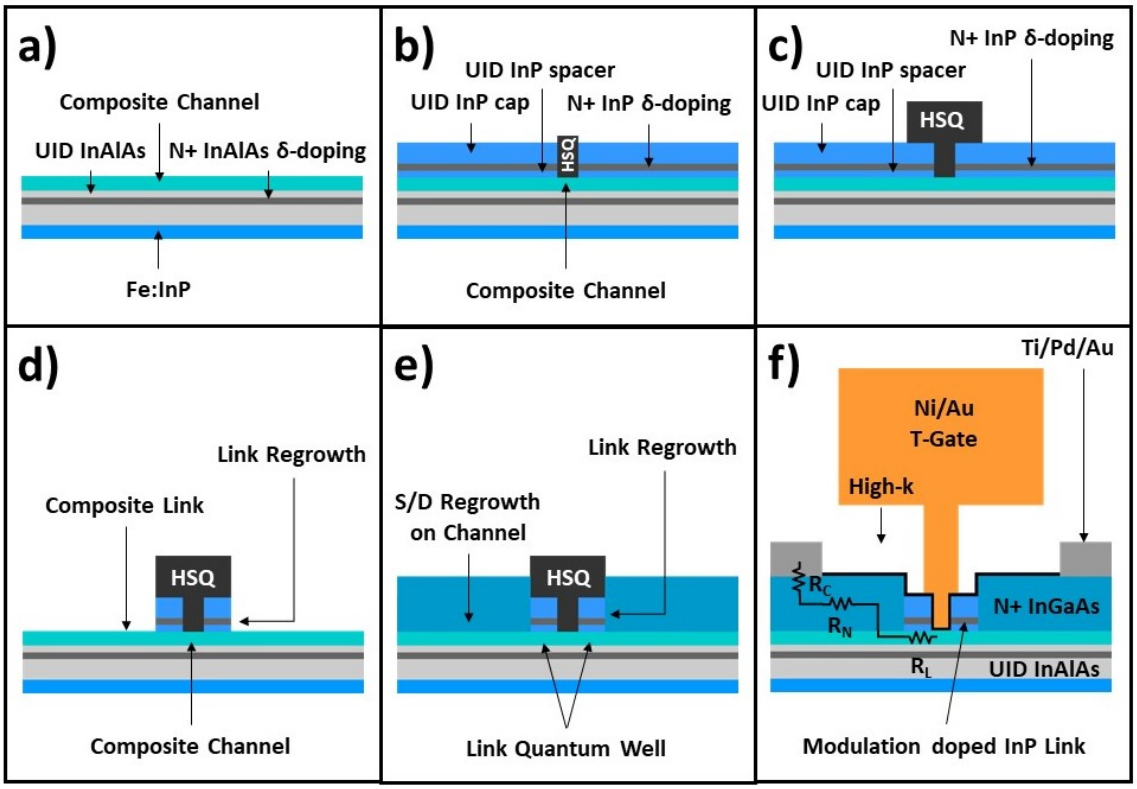

Figure 5.1 a) Initial starting surface b) First dummy gate and link regrowth c) Second dummy gate d) Link region wet etch e) source-drain regrowth on channel f) Final structure after T-Gate metallization and source-drain contact formation

Devices were fabricated on a (100) semi-insulating InP substrate. Beginning epitaxial layers – substrate to channel cap – were purchased from Intelligent Epitaxy: 200 nm UID-$In_{0.52}Al_{0.48}As$ buffer, 20 nm UID-InP etch stop, 100 nm UID-$In_{0.52}Al_{0.48}As$, 3 nm modulation doped Si:$In_{0.52}Al_{0.48}As$ 1.2 x 10^{19} cm^{-3}, 3 nm UID-$In_{0.52}Al_{0.48}As$ spacer, 2 / 4 / 5 nm UID-$In_{0.53}Ga_{0.47}As$ / strained UID-InAs / UID-$In_{0.53}Ga_{0.47}As$ composite channel. Because this is the same epitaxial structure used for Generation 1 devices, the same leaky etch stop is present and the off-state performance is expected to be similar.

Processing begins with 1.0 nm ALD Al_2O_3 deposited immediately prior to spinning and exposing hydrogen silsesquioxane (HSQ) by electron beam lithography (EBL) to define the gate recess. The HSQ was developed in NaCl:NaOH:H_2O and the channel cap digital etched in UV ozone + dilute HCl to clean the surface and define the link quantum well thickness. The sample was immediately loaded into the metal organic chemical vapor deposition (MOCVD) chamber where the modulation doped link region was regrown at 600°C: 3 nm UID-InP spacer, 2 nm Si:InP ($1x\ 10^{19}$ cm^{-3}) modulation doping, 15 nm UID-InP cap. Parallel Hall samples confirmed n_L = 2.5 x 10^{12} cm^{-2} and μ_L = 11,000 cm^2/Vs. The high mobility suggests that the strained InAs is not relaxed and is of high quality. Both the n_L and μ_L are like Generation 1 devices, confirming the repeatability of the regrowth recipe and process. The first dummy gate was then stripped in BHF and the process repeated to define the second dummy gate. The gate-source and gate-drain recess lengths are both designed to be 50 nm. Prior to loading into the MOCVD, the link region was removed in the unmasked regions by cyclic digital etching: 3 minutes UV-ozone + 1 minute HCl:H_2O 1:10. The thickness of the modulation doped InP link region and sheet resistance of the access region quantum wells were periodically measured by ellipsometry and four-point probing respectively. Due to the lever rule, as the UID-InP cap is thinned, more charge from the modulation doping images on the surface rather than in the quantum well. This is observed as a reduction in n_L resulting in larger R_L – illustrated in **Figure 5.2**. Once the InP link region appeared to be removed – as determined by ellipsometry – a final digital etch cycle was done immediately prior to reloading the sample into the MOCVD chamber. A 45 nm contact layer of N+ $In_{0.53}Ga_{0.47}As$ (target 4 x 10^{12} cm^{-3}) was then regrown at 600°C. In comparison to Generation 1, the N+

$In_{0.53}Ga_{0.47}As$ was thinned by 15 nm to reduce the parasitic capacitance between the T-Gate head and the highly doped source-drain regrowth.

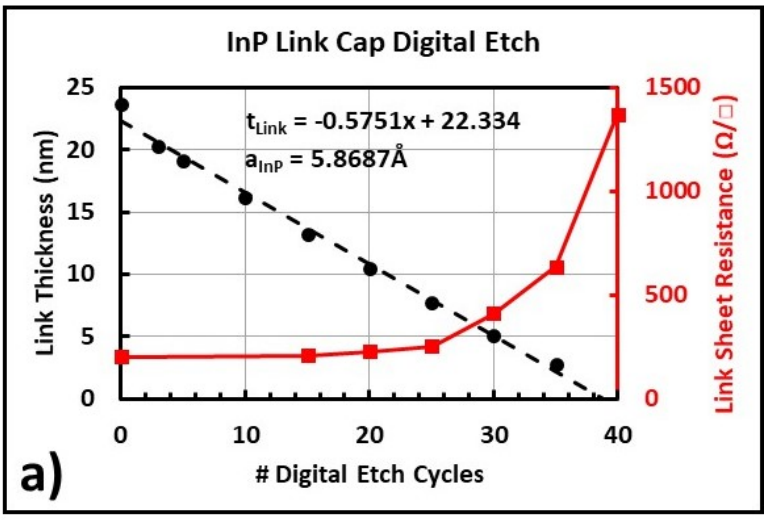

Figure 5.2 Digital etch rate and link sheet resistance for InP link, Generation 2 devices

Post regrowth processing involves mesa isolation, High-k deposition, T-gate formation, and source-drain metallization. Devices are mesa isolated by selective wet etching. The $In_{0.53}Ga_{0.47}As$ channel cap was then thinned by 5 cycles of digital etching in dilute HCl. Samples are dipped in BHF immediately prior to loading into the ALD where the channel surface was passivated using 9 cycles of N_2-plasma and trimethyl-aluminum (TMAl) followed by 30 cycles of H_2O and tetrakis(ethylmethylamido)zirconium(IV) (TEMAZ). Following ALD deposition, the sample was annealed at 400°C for 15mins in forming gas to passivate dangling bonds at the semiconductor / high-k interface. A two-step T-Gate EBL exposure is used to realize sub-100nm T-Gate footprints. CSAR 62:Anisole 2:1 was spun (6 kRPM for 30 seconds) and exposed at high dose (proximity effect corrected, base dose = 220 $\mu C/cm^2$) and developed in amyl acetate, defining the T-Gate foot. Samples were then coated in UV6-0.8 (3 kRPM for 30 seconds), exposed at low dose and develop in AZ300-MIF to define the T-Gate

head. Ni/Au 35/290 nm T-Gates were then thermally evaporated and lifted off. A post metal anneal of 350°C in H_2 for 30 minutes is done to recover any UV damage incurred during evaporation. Source-drain vias are then exposed in the EBL using CSAR. The CSAR is double spun at 3 kRPM for $t_{CSAR} \approx 900$ nm to completely planarize the T-Gate. The source-drain vias are then etched in BHF for 45 seconds, exposing the underlying N+ $In_{0.53}Ga_{0.47}As$. Finally, Ti/Pd/Au 20/20/300 nm pads are evaporated and lifted-off. **Figure 5.3** shows a TEM cross-section of a drawn 18 nm device.

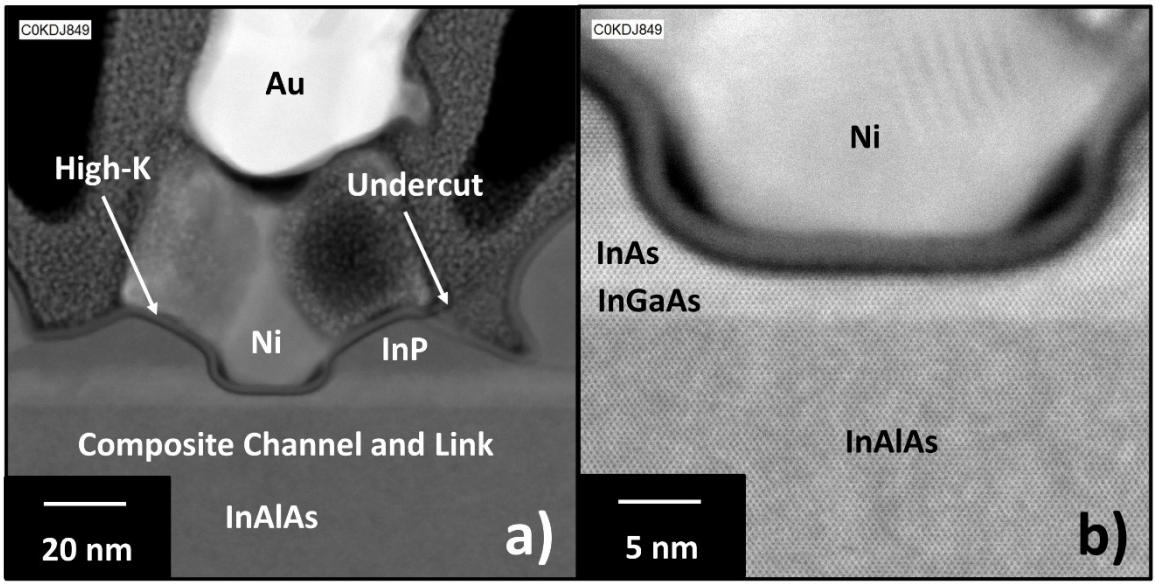

Figure 5.3 Cross-sectional TEM of L_g = 18 nm device a) intrinsic device b) gated region

The measured metallurgical gate length is 17.6 nm, demonstrating precise control of <30nm gate lengths that are difficult to characterize by scanning electron microscopy (SEM). Excellent alignment between the first and second dummy gate is observed as well as excellent re-alignment of the T-Gate foot to the gate recess. The channel thickness is 2.5 nm rather than the targeted 5.0 nm. This suggests a digital etch rate of ~2 nm/cycle for strained InAs.

Missing Ni is observed at the edges of the T-Gate head while an isotropic etch profile is observed at the edge of the T-Gate foot. It is unknown why the Ni is etched but is an effect

that was commonly observed for multiple intermediate generations. Suspected reasons include: 1) galvanic effects due to the presence of titanium 2) galvanic effects due to dirty glassware and the presence of dissolved aluminum 3) galvanic effects due to exposed semiconductor layers.

B. Band Diagrams

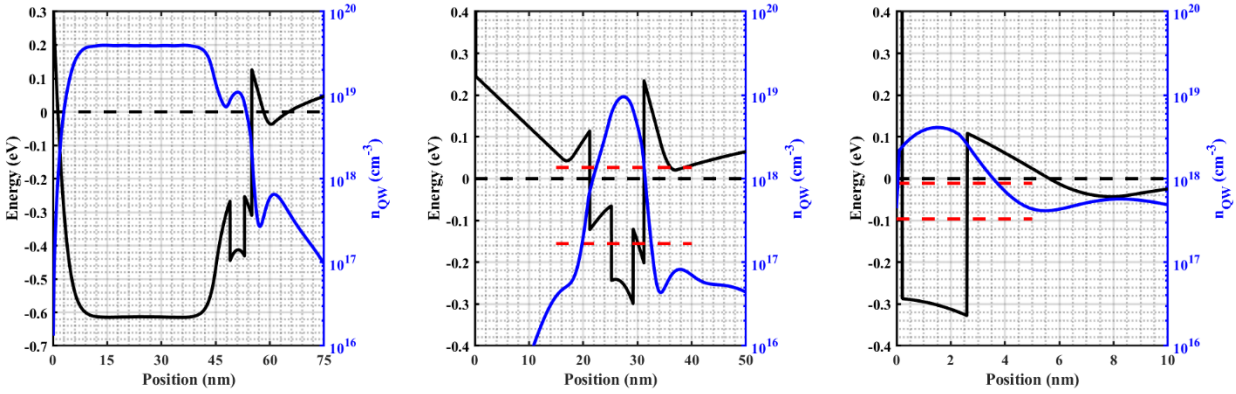

Figure 5.4 Band diagrams of the (left) source-drain regions and (right) link quantum well plotted on (top) log-scale to show parallel 2DEGs and (bottom) linear scale to show wave-function distribution

Band diagrams were calculated using the 1D self-consistent Schrödinger-Poisson solver, BandProf, using dimensions determined by TEM cross-sectional imaging of the fabricated device. Band-diagrams are shown for the source-drain, link quantum well, and intrinsic channel at V_{GS} = 0.3 V in **Figure 5.4**. No barrier to electrons exists beneath the source-drain regions as the modulation doped InP was removed. The link region is the same design as Generation 1 and is expected to exhibit n_L = 4.0 – 5.0 x 10^{12} cm^{-2} with little margin to add modulation doping in the top barrier. The isotropic undercutting observed due to the link region wet etch can be best predicted using the measured R_L vs. t_{cap} shown in **Figure 5.2** since unknown defect density on the link surface will effect the charge imaging in that region.

The thin channel results in increase E_1 and a positively shifted V_{TH}. Peak $\underline{g_{m,i}}$ is expected to occur when E_F crosses the conduction band-minimum in the back-barrier beyond the modulation doping and the parallel 2DEG begins populating. This is expected to occur at V_{GS} ≈ 0.3 – 0.4 V corresponding to n_{ch} = 1.5 – 4.5 x 10^{12} cm^{-2} and is likely convoluted with the onset of source-starvation as $n_{ch} = n_L/2$ occurs within this same bias range.

C. DC Results

Figure 5.5 shows the transfer and output characteristics of a drawn L_g = 18 nm $(0\bar{1}1)$ device. The device exhibits peak DC transconductance ($g_{m,e}$) of 1.6 mS/μm at V_{DS} = 0.5 V and V_{GS} = 0.6 V. Low $g_{m,e}$ and shift to higher V_{GS} compared to Generation 1 are both explained by the thinner channel. As discussed in **Section 2F**, thin channel devices have larger eigenstate energies and less available ($E_F – E_1$) resulting in less available ($V_{GS} – V_{TH}$) and smaller $g_{m,i}$. Furthermore, $In_{0.53}Ga_{0.47}As$ has a smaller conduction band offset (CBO) to $In_{0.52}Al_{0.48}As$ than pseudomorphic InAs resulting in further limited $g_{m,i}$. Generation 2 devices cannot be compared at $V_{GS} = V_{DS}$ = 0.5 V, common to reported VLSI devices, as the threshold voltage is positively shifted due to the large channel eigenstate energy. A more meaningful comparison can be done at ($V_{GS} – V_{TH}$) = V_{DS} = 0.5 V.

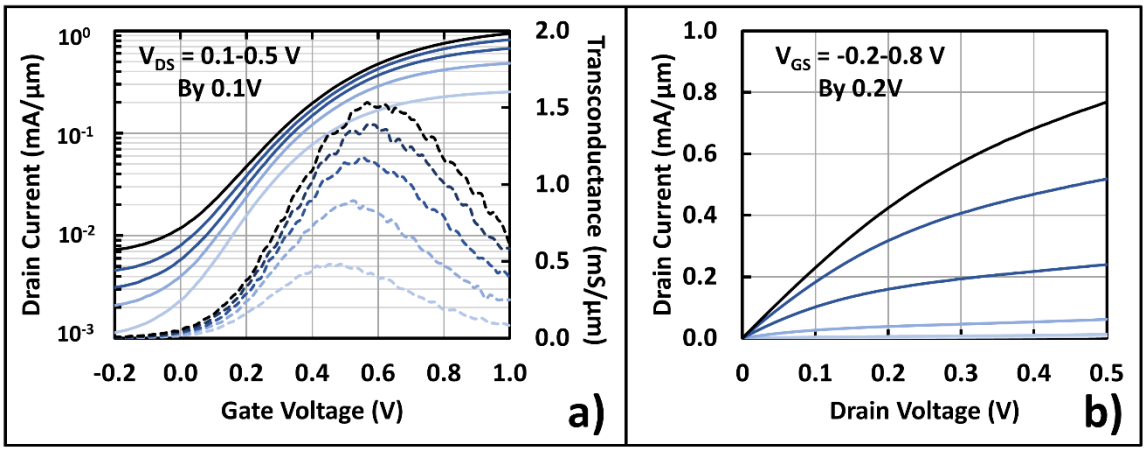

Figure 5.5 Drawn L_g = 18 nm ($\mathbf{0\bar{1}1}$) oriented device a) transfer and b) output characteristics

Figure 5.6 shows the peak transconductance, minimum sub-threshold swing, and DIBL as a function of L_g for Generation 2 devices. Peak DC $g_{m,e}$ plateaus at ~1.5 mS/μm for $L_g \leq 20$ nm. Given that the channel is extremely thin, the channel electron wavefunction is strongly interacting with both the high-k and the $In_{0.52}Al_{0.48}As$ back-barrier. Both surface scattering effects result in a short electron mean-free-path. It is therefore expected that the ballistic limit will be reached at shorter gate lengths. The observed roll-off in $g_{m,e}$ for $L_g \leq 18$ nm is because of partial gating. Devices with $L_g \leq 18$ nm have a drawn L_{foot} = 50 nm which cannot be effectively filled with the thermal evaporator at UCSB.

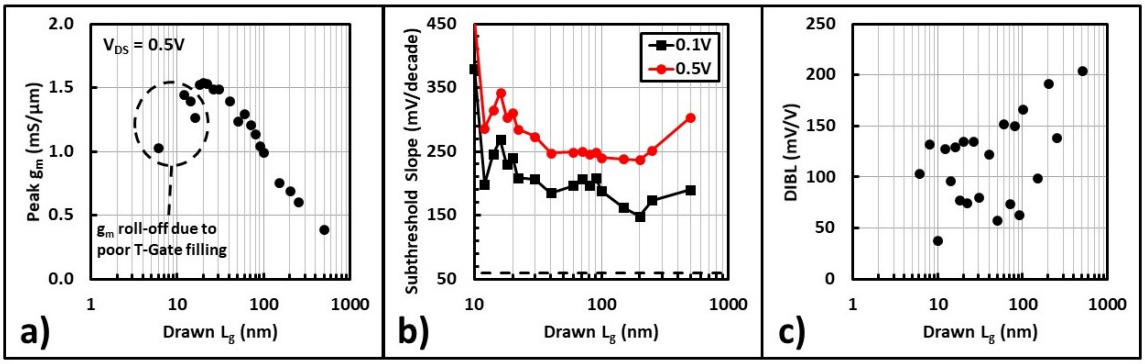

Figure 5.6 DC lot characterization of Generation 2 devices a) Peak transconductance b) subthreshold slope at V_{DS} = 0.1 V and 0.5 V c) DIBL

Like Generation 1 devices, all devices exhibited I_{off} = 1 µA/µm at V_{DS} = 0.1 V due to leakage through the InP etch stop layer. The steepest part of the subthreshold slope (*SS*) is convoluted with this leakage and *SS* cannot be used to infer the quality of the high-k gate dielectric. The observed minimum *SS* decreases with increasing L_g as expected due to improved electrostatics. Like Generation 1, minimum *SS* abnormally increases for $L_g \geq 200$ nm since I_{DS} begins to roll over. The true minimum *SS* is expected to shift to lower I_{DS} as the thin channel's superior electrostatics and increased R_{ch} should reduce I_{off}. The thermionic and saturation regions therefore also shift to lower I_{DS}. Additionally, Ref [1] demonstrated steeper *SS* and decreased C-V dispersion for InAs channels than for $In_{0.53}Ga_{0.47}As$ channels; it is expected that Generation 2 (high-k / $In_{0.53}Ga_{0.47}As$) would exhibit moderately larger *SS* than Generation 1 (high-k / InAs).

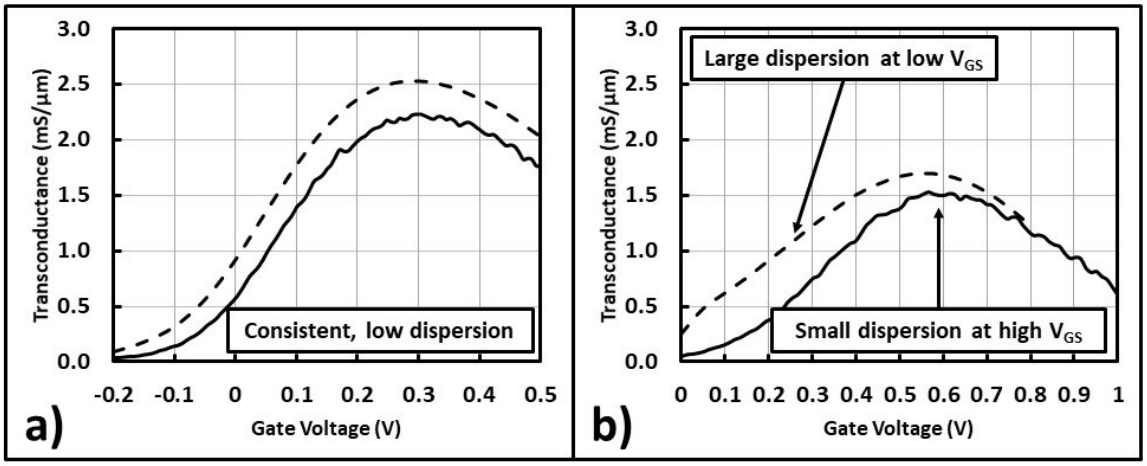

Figure 5.7 DC and 1 GHz $g_{m,e}$ for a) Generation 1 t_{ch} = 6.5 nm with high-k / InAs interface and b) Generation 2 t_{ch} = 2.5 nm with high-k / $In_{0.53}Ga_{0.47}As$ interface

Since *SS* cannot be used to infer the quality of the oxide / semiconductor interface, DC / RF $g_{m,e}$ dispersion must be used. Peak DC $g_{m,e}$ of a drawn L_g = 12 nm device at V_{DS} = 0.5 V is 1.51 mS/µm while peak $g_{m,e}$ at 1 GHz is 1.70 mS/µm, corresponding to 11% deviation. This is consistent with both [2] and Generation 1, suggesting the quality of the high-k /

semiconductor interface. **Figure 5.7** compares the DC and 1 GHz $g_{m,e}$ measurements of both Generation 1 and Generation 2 devices. Generation 2, $In_{0.53}Ga_{0.47}As$ channel devices exhibit larger dispersion at low V_{GS}, eventually converging at large V_{GS}. Because V_{TH} occurs at $E_F = E_{1,ch}$, dispersion near threshold is indicative of defect levels near the channel conduction band minimum. Previous studies determined that defect levels in $In_{0.53}Ga_{0.47}As$ exist near the conduction band minimum while those in InAs exist deep inside the conduction band and therefore exhibit less influence on SS_{min} [3]–[5].

Like Generation 1, *DIBL* is difficult to attribute meaning to due to the presence of the leaky etch stop. Ref [6] reports *DIBL* of 100 and 125 mV/V for L_g = 20 nm, t_{ch} = 3.0 nm InAs and $In_{0.53}Ga_{0.47}As$ channel devices respectively. Devices in [6] have a 13 nm UID-$In_{0.53}Ga_{0.47}As$ vertical spacer between the gate-edge and N+ source-drain $In_{0.53}Ga_{0.47}As$ which moderately improves device electrostatics. Generation 2 devices have a 50 nm 2.5 x 10^{12} cm^{-2} lateral spacer which can deplete at large V_{DS}, shielding the channel surface potential from the drain potential better than in [6]. While it cannot be directly extracted from DC measurements, *DIBL* is expected to be lower than in [6] because of the thinner gate dielectric, thinner channel, and lateral spacer.

Figure 5.8 shows the two sets of TLMs used to estimate components of source-resistance. First, the N+ TLMs give R_N = 32 Ω•μm and R_C = 10 Ω•μm. The link TLMs give R_L = 11 Ω•μm and R_A = 69 Ω•μm resulting in total R_S = 122 Ω•μm. All resistances are comparable to Generation 1 devices with R_N increasing from 22 Ω•μm to 32 Ω•μm due to the thinner N+ regrowth. Interestingly R_A is the same. The isotropic undercutting caused by the link wet etch brings the surface of the link region closer to the plane of modulation doping. More charge will therefore image on the semiconductor surface rather than in the quantum well resulting

in increased quantum well sheet resistance at the ends of the link TLMs. This additional end resistance (R_{end}) will be convoluted as part R_A possibly explaining the unexpectedly high result. Extrapolating R_{on} vs. L_g gives R_S = 147 Ω•µm corresponding to a ~15 Ω•µm improvement compared to Generation 1 devices. To be more rigorous, $R_L(t_{cap})$ from **Figure 5.2** can be used in conjunction with the profile observed in **Figure 5.3** to estimate $R_{L,act}$ = 17 Ω•µm for R_S = 128 Ω•µm. TLM extracted R_S represents the extrinsic component of R_S; however, [7] showed that a significant fraction of R_{SD} is ballistic resistance ($R_{ballistic}$): $R_{S,total}$ = R_{EXT} + $R_{ballistic}$. Therefore the difference of $R_{on}(L_g$ = 0 nm) and R_{TLM} is attributed to $R_{ballistic}$. Analysis like [7] needs to be done in the future.

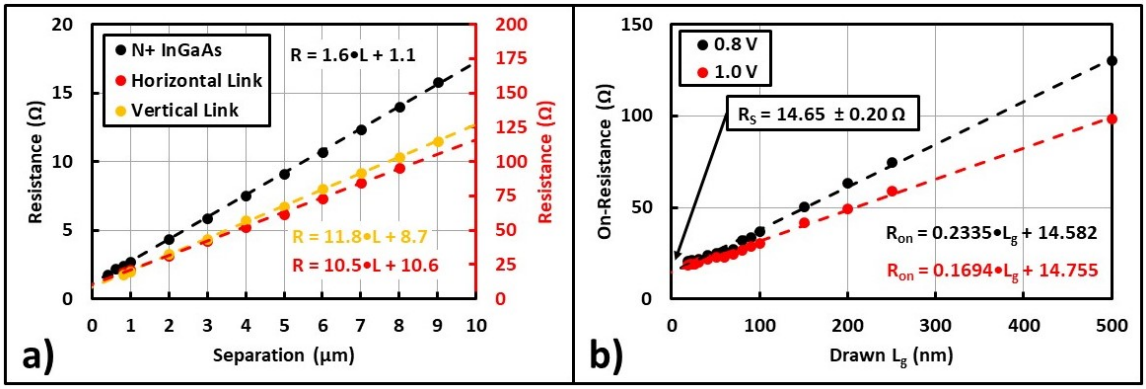

Figure 5.8 Extracted resistances a) N+ $In_{0.53}Ga_{0.47}As$ and Link Quantum Well TLMs, where "Horizontal" refers to (011) conduction and "Vertical" is $(0\bar{1}1)$ conduction b) On-resistance measurements at various ($V_{GS} - V_{TH}$)

While the moderate improvement in $R_{on}(L_g$ = 0 nm) is anti-climactic, a significant improvement in R_S is <u>*NOT*</u> expected when using a modulation doped InP link region. **Figure 1.1** shows the band-diagrams of the N+ $In_{0.53}Ga_{0.47}As$ grown directly on the channel while the band-diagram of N+ $In_{0.53}Ga_{0.47}As$ grown ontop of the InP link were shown in **Chapter 4**. Because InP has a small band-offset to $In_{0.53}Ga_{0.47}As$, there is not a large barrier for electrons transiting from source to channel. The high doping in the source drags the bands in the UID-

InP cap down, making the InP beneath the source-drain regrowth degenerate. The only barrier exists in the region between the modulation doping and the channel. However, the barrier is extremely small (~0.08 eV). **Chapter 1 Section A** showed the source-drain region band-diagrams using a modulation doped $In_{0.52}Al_{0.48}As$ link instead. Because of the larger CBO, the UID-$In_{0.52}Al_{0.48}As$ cap is not made to be heavily n-type by the source. The barrier associated with the modulation doping is significant (~0.20 eV). Despite the minimal reduction in R_S for Generation 2 devices, the viability of digital etching through the modulation doped link in the source-drain regions has been demonstrated. Despite the isotropic undercutting and regrowth faceting – removal of the link to reduce R_S is promising.

D. RF Results

S-parameters were measured from 250 MHz to 67 GHz using on-wafer probing and –27 dBm port power. Prior to measurement, off-wafer load-reflect-reflect-match calibration was done. On-wafer open and short-circuit pad parasitics were de-embedded from the transistor measurements. f_T and f_{max} are determined by fitting the –20 dB/dec roll-off of H_{21} and U from 10 GHz to 50 GHz and 30 GHz to 45 GHz respectively. The order of pad extraction (open first vs. short first) only minimally changes the transistors extracted 2-port parameters, where the more pessimistic values (open-short) are reported. Interestingly, despite predicting moderately more optimistic FOMs, short-open de-embedding produces typical Y-parameter behavior while open-short exhibits increasing $Re(Y_{21})$ with frequency. More robust de-embedding (TRL) is desired to eliminate this discrepancy.

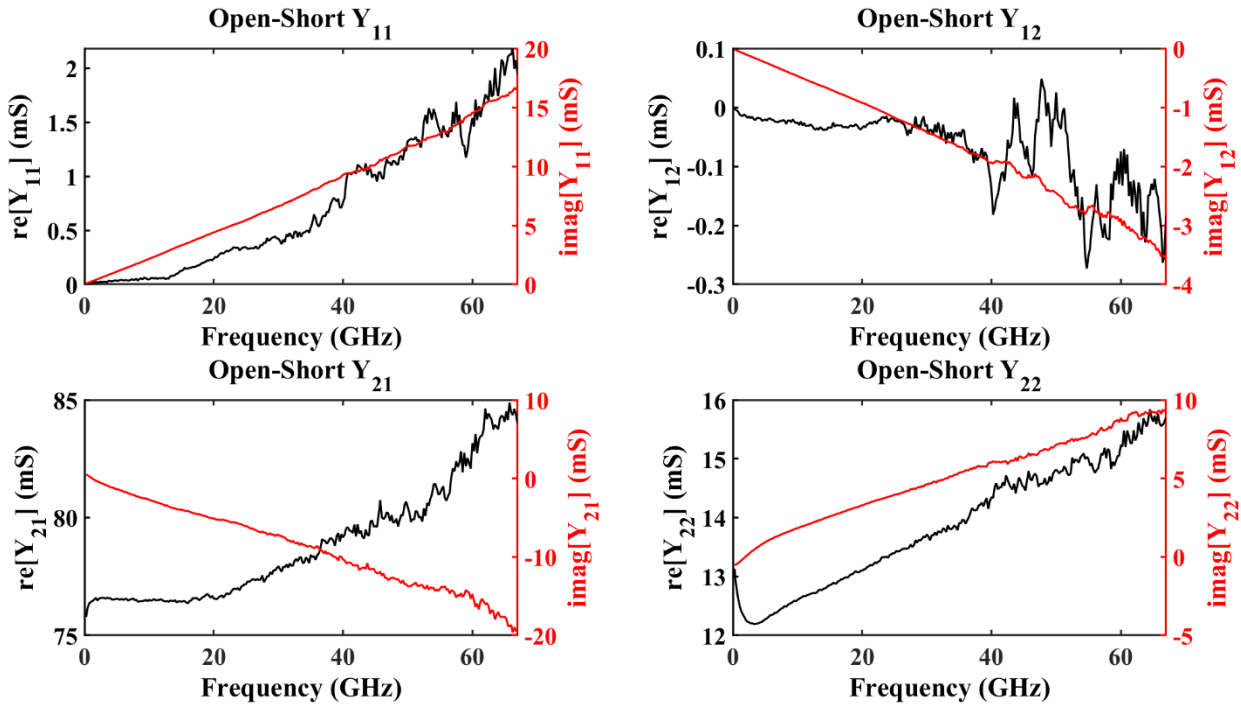

Figure 5.9 Open-Short de-embedded Y-parameters for L_g = 12 nm device

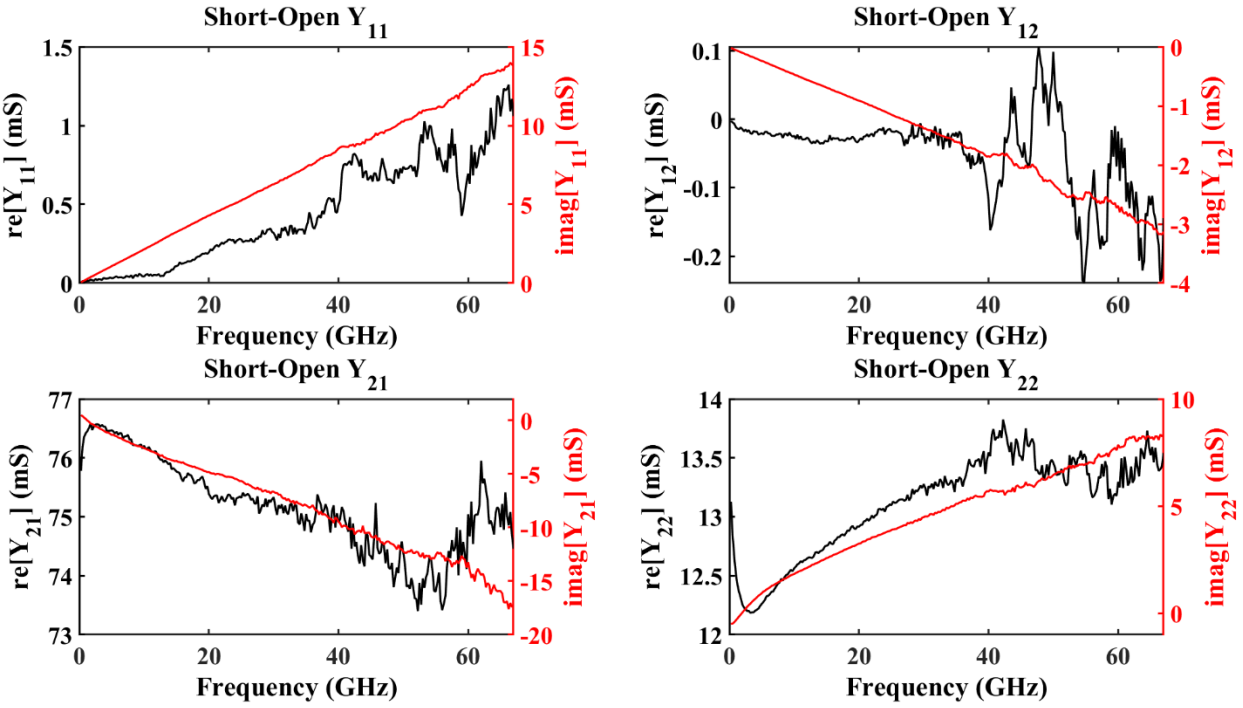

Figure 5.10 Short-Open de-embedded Y-parameters for L_g = 12 nm device

Figure 5.9 shows open-short de-embedded Y-parameters while **Figure 5.10** shows short-open de-embedded Y-parameters. Automatic fitting is done to extract the small signal equivalent circuit parameters, shown in **Figure 5.12**. Generally, f_τ is lower in Generation 2 devices than in Generation 1 devices because of larger $C_{GS,i}$ and smaller $g_{m,i}$. Both f_τ and f_{max} drop off quickly for $L_g \geq 30$ nm due to increasing C_{GS}, non-ballistic transport, and high channel resistance. The large increase in C_{GS} is attributed to parasitic T-Gate overlap. The thinner high-k dielectric (30 cycles) and a thinner channel (2.5 nm) results in larger C_{ins} and C_{QW} which increases $C_{GS,i}$. Additionally, because the in-plane effective mass increases with decreasing channel thickness, C_{DOS} is also larger [8]. The ultrathin $In_{0.53}Ga_{0.47}As$ channel also increases the Eigenstate energy reducing the available ($V_{GS} - V_{TH}$), limiting $g_{m,i}$.

Extracted short gate-length $C_{GS} = 0.85 - 1.00$ fF/μm and is extremely high compared to SOA HEMTs while $C_{GD} \approx 0.23$ fF/μm is only moderately high. Because L_{foot} is not scaled with each gate length, the parasitic overlap is not constant, and it is therefore difficult to extract extrinsic capacitances. To estimate parasitic gate-source capacitance ($C_{GS,p}$), a linear fit is applied to devices with $L_g = 20 - 40$ nm which all contain $L_{foot} = 74$ nm. As the gate length decreases, the parasitic T-Gate overlap increases. Therefore, a larger fraction of the measured C_{GS} is due to $C_{GS,p}$ rather than $C_{GS,i}$. To first order, the aim is to roughly separate these values and this effect is therefore ignored. Extracted $C_{GS,p} = 0.72$ fF/μm leaving $C_{GS,i} = 0.17 - 0.25$ fF/μm. Calculated $C_{GS,i}$ is 0.15 fF/μm for $L_g = 25$ nm $In_{0.53}Ga_{0.47}As$ channel devices, slightly lower than extracted, suggesting that $C_{GS,p}$ is severely limiting RF performance. More rigorous calculations of band-structure in quantum confined structures generally results in larger in-plane effective masses than calculated by the effective mass theory (as done here), further increasing C_{DOS} and $C_{GS,i}$ [8]. Because C_{DOS} is limiting for thin channel III-V devices, changes

in C_{DOS} are expected to significantly impact $C_{GS,i}$ which should reduce the discrepancy between measured and extracted $C_{GS,i}$. CGS,I can be determined by CV; **Figure 5.11** shows S-parameter extracted CV-characteristics and n_{ch}, $g_{m,e}$ vs. V_{GS} for a L_g = 12 nm $(0\bar{1}1)$ device. Extracted $C_{GS,i}$ = 0.15 – 0.20 fF/µm, consistent with extracted and calculated values. Interesting C_{GS} does not saturate with V_{GS}, possibly because $n_{2DEG} \approx n_{ch}$ and continues populating as V_{GS} is increased. Peak $g_{m,e}$ is observed at $n_{ch} \approx n_{Link}$ again suggesting that source-starvation limits I_{DS} and g_m.

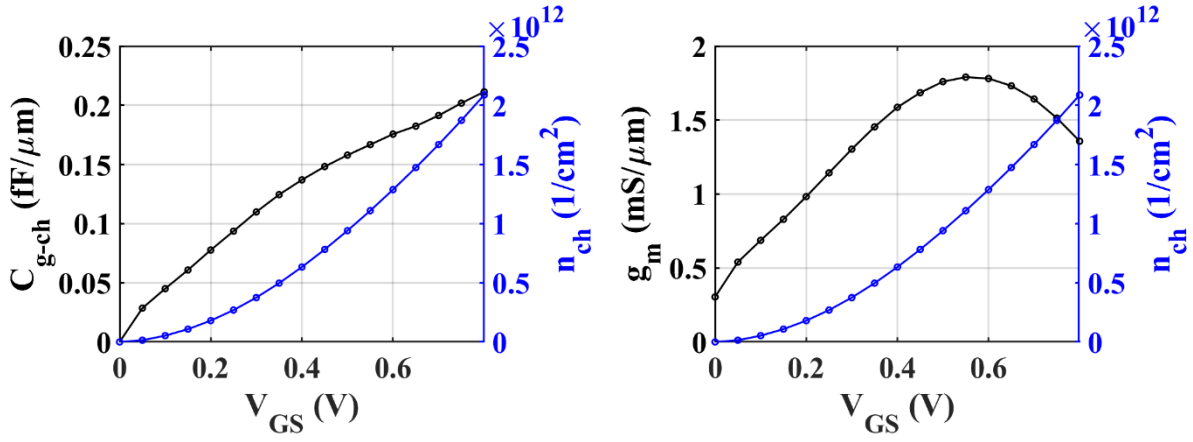

Figure 5.11 L_g = 12 nm $(\mathbf{0\bar{1}1})$ S-parameter extracted a) CV characteristics b) $g_{m,e}$ and n_{ch} at V_{DS} = 0.7 V

Power-gain and current gain cut-off frequency is balanced in short-channel devices because of improved R_G and g_{ds}. Compared to Generation 1, R_G was reduced to 7 Ω from ≥15 Ω. Extracted $g_{ds,e}$ = 0.20 – 0.35 mS/µm for $L_g \leq$ 40 nm when biased for peak f_τ. The resulting g_m / g_{ds} ratio is 7.5 at L_g = 20 nm which is lower than [2]. Leakage through the etch stop layer (R_{Leak}) is convoluted with g_{ds} which increases the extracted value. It is expected that g_{ds} is lower than extracted but; however it is difficult to assert due to the impracticability of separating g_{ds} || R_{Leak} || R_{II} at large V_{DS}.

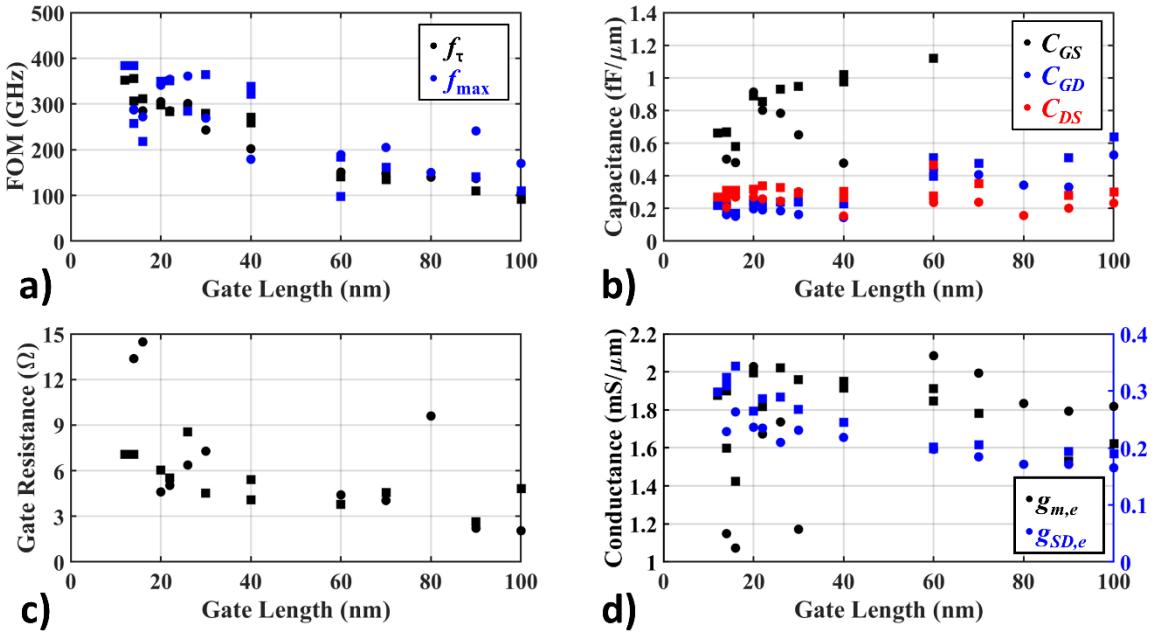

Figure 5.12 Extracted FOMs and common source small signal equivalent circuit parameters for Generation 2 devices

Peak f_τ = 356 GHz and peak f_{max} = 403 GHz were observed on the same drawn L_g = 12 nm $(0\bar{1}1)$ conduction device. Figure of merit (FOM) contour plots and extraction at peak (f_τ , f_{max}) are shown in **Figure 5.13**. Extract small-signal equivalent circuit parameters are: $g_{m,e}$ = 1.91 mS/μm, $g_{ds,e}$ = 0.30 mS/um, R_S = 178 Ω•μm, R_G = 7 Ω, C_{GS} = 0.71 fF/μm, C_{GD} = 0.19 fF/μm, and C_{DS} = 0.25 fF/μm. Moderately improved f_τ compared to L_g = 20 nm devices is due to decreased C_{GS} and C_{GD} due to a reduction in L_{foot} from 74 nm to 50 nm. However, due to poor T-Gate stem filling, short-gate length devices have poor yield and often exhibit large R_G.

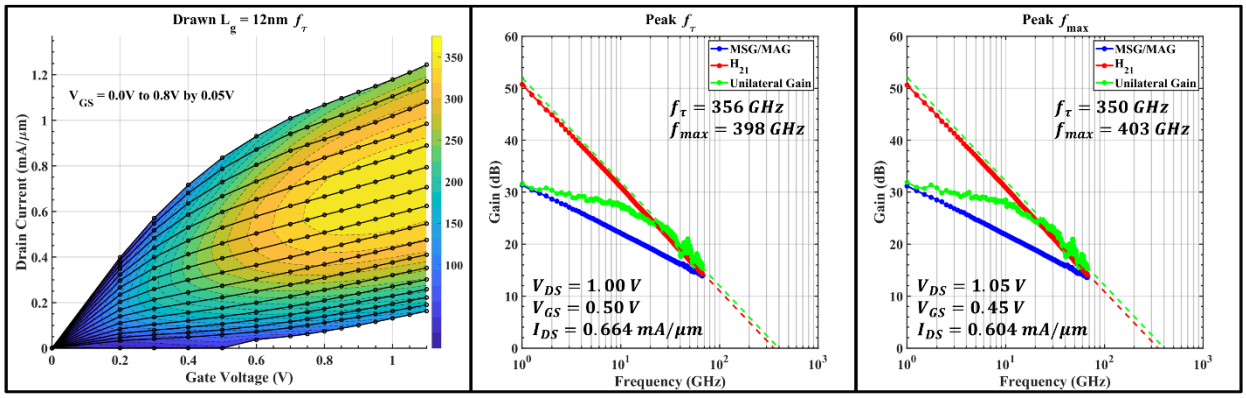

Figure 5.13 L_g = 12 nm ($\mathbf{0\bar{1}1}$) conduction device (left) f_τ contour plot (middle) FOM fitting at peak f_τ (right) FOM fitting at peak f_{max} (bottom)

E. Equivalent Circuit Model

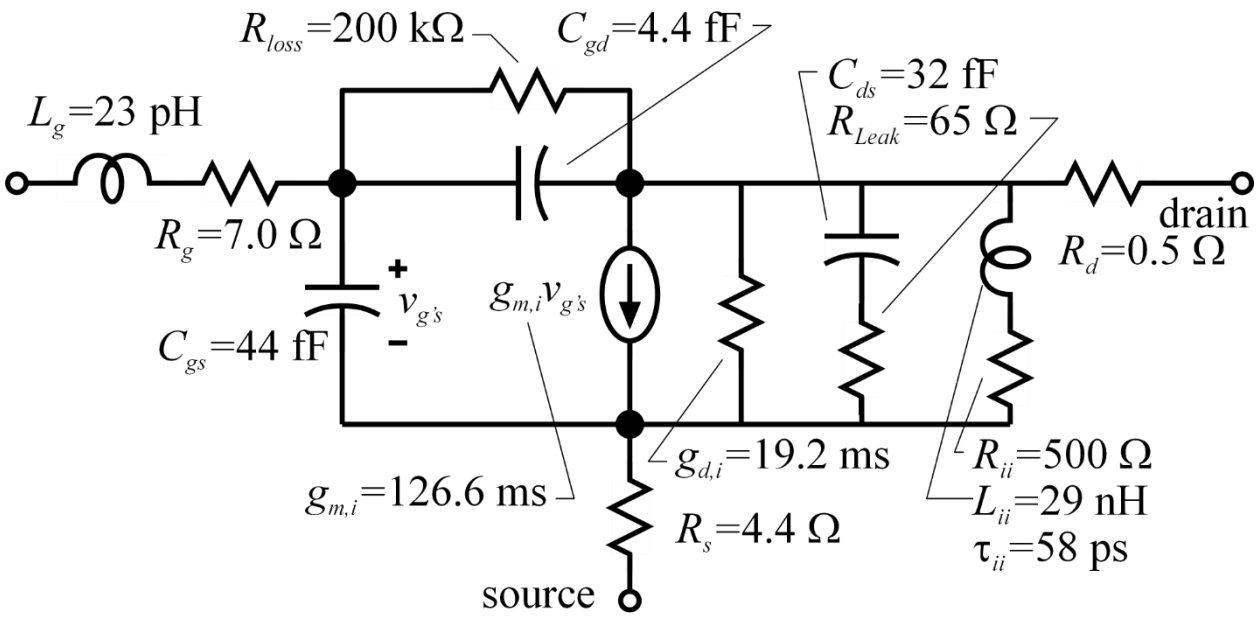

Figure 5.14 Small signal equivalent circuit of L_g = 12 nm ($\mathbf{0\bar{1}1}$) conduction device at V_{DS} = 1.00 V, V_{GS} = 0.50, I_{DS} = 0.664 mA/μm

The common-source small-signal equivalent circuit (SSEC) model for the above described L_g = 12 nm, f_τ = 356 GHz device is shown in **Figure 5.14**. Extraction of the equivalent circuit is as follows: measured S-parameters are converted to Z-parameters and fit at large (V_{GS} – V_{TH}) (fully inverted) and V_{DS} = 0 V to extract R_S, R_D, and R_G. At V_{DS} = 0 V, the source and

drain are symmetric so $R_S = R_D = R_{SD} / 2$. At large V_{DS} the drain side depletes, and R_D becomes very small. Extracted R_S is 160 – 180 Ω•μm, higher than the 120 – 150 Ω•μm measured by TLM and R_{on} extrapolation. The extraction technique described in [9] assumes that the channel resistance is small compared to R_{SD} at large ($V_{GS} - V_{TH}$). However, due to the ultra-thin channel, this is not the case. Extracted R_{SD} increases with increasing L_g and therefore likely contains a significant contribution from $1/g_m$. Therefore, the extracted R_{SD} is used only as a starting point for SSEC development.

Next, the measured S-parameters are converted to Y-parameters and fit to extract g_m, g_{ds}, C_{GS}, C_{GD}, and C_{DS}. Imag(Y_{12}) is fit from 250 MHz to 40 GHz to extract C_{GD} while Imag(Y_{11}) is fit over the same range to extract C_{GS}. High frequency components result in slight curvature in Imag(Y_{11}) and Imag(Y_{12}) and thus 40 – 67 GHz data is ignored during initial fitting. Re(Y_{21}) and Re(Y_{22}) are fit and extrapolated to $f = 0$ GHz to determine extrinsic g_m and g_{ds} respectively. Moderate D_{it} causes low frequency dispersion in Re(Y_{12}). Because this effect is minor and only causes deviation below 3 GHz, the entire frequency range is fit. Because Y_{22} is complicated and contains many high and low frequency contributions, Re(Y_{22}) is fit from 20 – 40 GHz to avoid convoluting the series L-R network associated with breakdown effects at low frequency while also avoiding high-frequency contributions. Similarly, Imag(Y_{22}) is fit over the same range to extract C_{DS}. This extraction technique assumes an ideal device and does not consider the parallel conduction through the etch stop layer, the associated etch stop capacitance, or the series L-R network present due to breakdown at the drain edge. These parameters are therefore viewed as a starting point for the SSEC construction and parameters are adjusted to realize best fit.

The SSEC is modeled and simulated in Keysight's Advanced Design System (ADS) software. SSEC parameters are adjusted until the best fit is realized over the entire 250 MHz – 67 GHz range. Once a best fit is established, the model is simulated from 250 MHz to 1 THz to determine the high-frequency FOMs. **Figure 5.15** shows measured and modeled S-parameters and FOMS. At peak f_τ bias, the extrapolated f_τ = 356 GHz and f_{max} = 398 GHz while modeled f_τ = 358 GHz and f_{max} is not meaningful due large deviation of measured and modeled unilateral power gain. Modeled U rolls off >20 dB/dec likely due to higher order terms associated with C_{DS} and R_{leak}, like Generation 1.

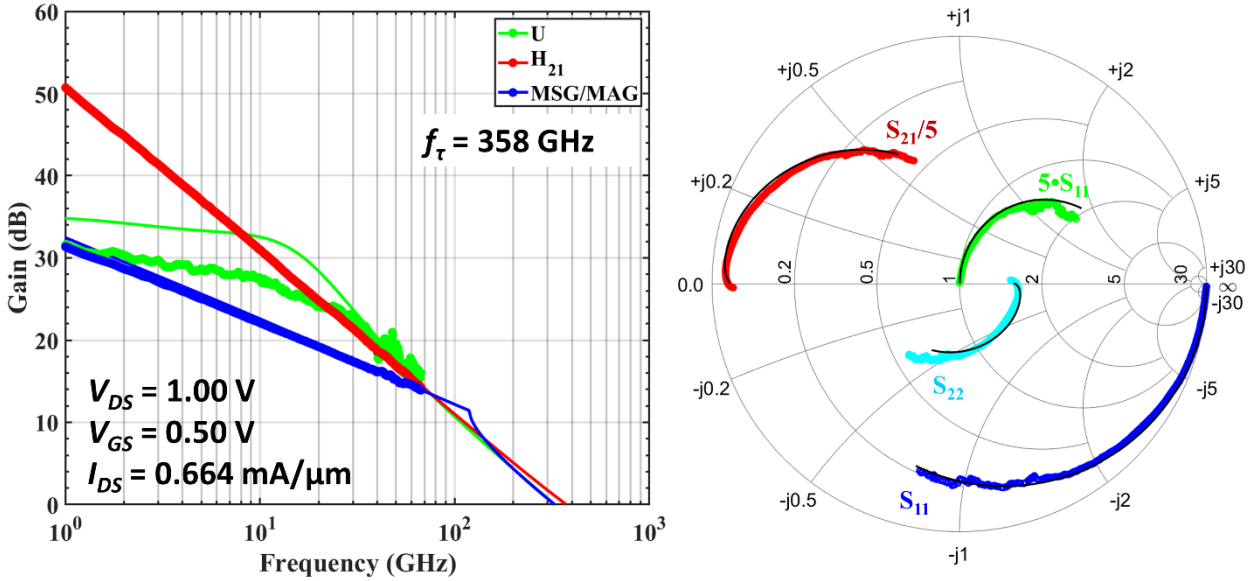

Figure 5.15 Measured and modeled high frequency FOMs and S-parameters of L_g = 12 nm $(\mathbf{0\bar{1}1})$ conduction device at V_{DS} = 1.00 V, V_{GS} = 0.50, I_{DS} = 0.664 mA/µm

Severe deviation of measured and modeled unilateral power gain is observed despite reasonable agreement of the S-parameters. Both Re(Y_{22}) and Imag(Y_{22}) cannot be matched to the model while added gate inductance (L_G) rectifies the increasing Re(Y_{21}). It is possible that incomplete de-embedding is to blame for the deviation of measured and modeled S-parameters; future mask sets should include TRL structures.

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6. Generation 3

A. Device Structure and Fabrication

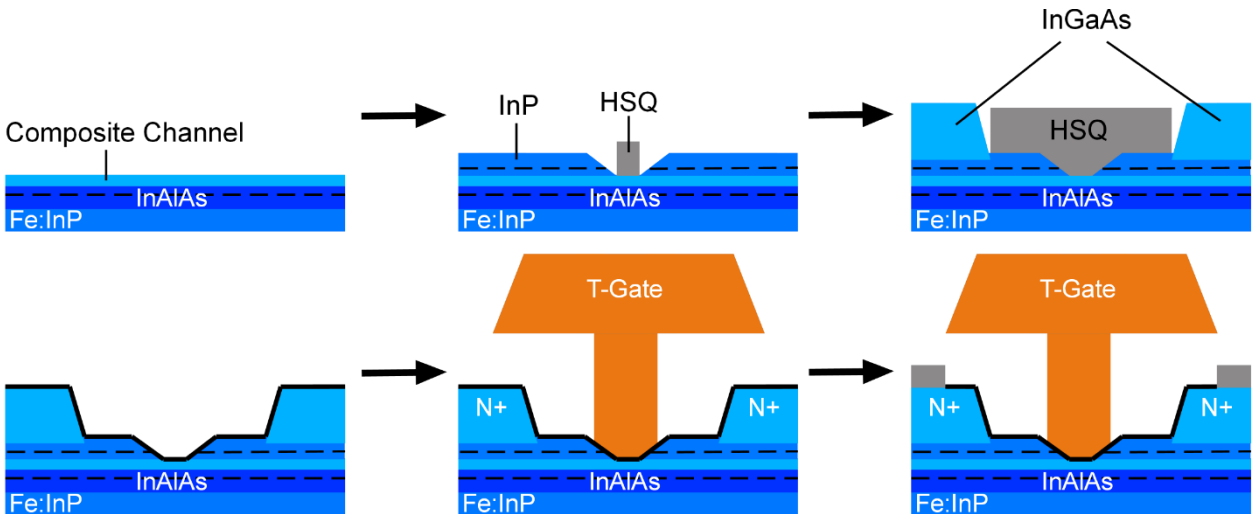

Figure 6.1 Regrowth fabrication process flow of Generation 3 devices with digitally etched recessed link design

Devices were fabricated on a (100) semi-insulating InP substrate. Beginning epitaxial layers – substrate to channel cap – were purchased from Intelligent Epitaxy: 100 nm UID-$In_{0.52}Al_{0.48}As$ buffer, 3 nm modulation doped Si:$In_{0.52}Al_{0.48}As$ (1.2 x 10^{19} cm^{-3}), 3 nm UID-$In_{0.52}Al_{0.48}As$ spacer, 3 / 4 / 6 nm UID-$In_{0.53}Ga_{0.47}As$ / strained UID-InAs / UID-$In_{0.53}Ga_{0.47}As$ composite channel. Removal of the InP etch stop layer compared to Gen. 1 and Gen. 2 facilitated $I_{off} \approx$ 10 nA/µm.

Processing begins with 1 nm ALD Al_2O_3 deposited immediately prior to spinning and exposing hydrogen silsesquioxane (HSQ) by electron beam lithography (EBL) to define the gate recess. The HSQ was developed in NaCl:NaOH:H_2O and the channel cap digital etched in UV ozone + dilute HCl to clean the surface and define the link quantum well thickness. The sample was immediately loaded into the metal organic chemical vapor deposition

(MOCVD) chamber where the modulation doped link region was regrown at 600°C: 3.0 nm UID-InP spacer, 3.5 nm Si:InP (1.0 x 10^{19} cm^{-3}) modulation doping, 10 nm UID-InP cap. Parallel Hall samples confirmed n_L = 5.8 x 10^{12} cm^{-2} and μ_L = 6,200 cm^2/Vs. The high mobility suggests that the strained InAs is not relaxed and is of high quality. Compared to Generation 1, increased N_δ was used to reduce the energy barriers to electrons in the source-drain region and increase n_L to prevent source starvation. Additionally, to completely remove the energy barrier for electrons in the source-drain regions, a thinner link cap was used. The smaller separation of surface-N_δ likely results in more charge imaging on the link surface rather than in the quantum well. The first dummy gate was then stripped in BHF and the process repeated to define the second dummy gate. The gate-source and gate-drain recess lengths are both designed to be 50 nm. Prior to loading into the MOCVD, the link region was thinned in the unmasked regions by cyclic digital etching: 3 minutes UV-ozone + 1 minute HCl:H_2O 1:10. The InP link region was thinned until the cap layer was < 5.0 nm to reduce source-resistance. A final digital etch cycle was done immediately prior to reloading the sample into the MOCVD chamber. A contact layer of 75nm N+ $In_{0.53}Ga_{0.47}As$ (target 4 x 10^{19} cm^{-3}) was then regrown at 600°C. In comparison to Gen. 1 and Gen. 2, the N+ $In_{0.53}Ga_{0.47}As$ was made thicker to reduce source-resistance.

Post regrowth processing involves mesa isolation, High-k deposition, T-gate formation, and source-drain metallization. Devices are mesa isolated by selective wet etching. The $In_{0.53}Ga_{0.47}As$ channel cap was then thinned by 3 cycles of digital etching in dilute HCl. Samples are dipped in BHF immediately prior to loading into the ALD where the channel surface was passivated using 9 cycles of N_2-plasma and trimethyl-aluminum (TMAl) followed by 30 cycles of H_2O and tetrakis(ethylmethylamido)zirconium(IV) (TEMAZ). Following

ALD deposition, the sample was annealed at 400°C for 15mins in forming gas to passivate dangling bonds at the semiconductor / high-k interface. A two-step T-Gate EBL exposure is used to realize sub-100nm T-Gate footprints. CSAR 62:Anisole 2:1 was spun (6 kRPM for 30 seconds) and exposed at high dose (proximity effect corrected, base dose = 220 μC/cm^2) and developed in amyl acetate, defining the T-Gate foot. Samples were then coated in UV6-0.8 (3 kRPM for 30 seconds), exposed at low dose and develop in AZ300-MIF to define the T-Gate head. Ni/Au 50/350 nm T-Gates were then thermally evaporated and lifted off. A post metal anneal of 350°C in H_2 for 30 minutes is done to recover any UV damage incurred during evaporation. Source-drain vias are then exposed in the EBL using bilayer PMMA. PMMA 50k is first spun at 3 kRPM and used as a liftoff layer. PMMA 950k is then spun at 1 kRPM and used to define the lift-off aperture. This bilayer stack was used due to its small undercut compared to CSAR/PMGI, and thus tighter source-drain spacing. The source-drain vias are then etched in BHF for 45 seconds, exposing the underlying N+ $In_{0.53}Ga_{0.47}As$, then Pd/Ni/Au 5/30/30 nm ohmic contacts are immediately electron beam evaporated. Finally, Ni/Au 10/300 nm pads are evaporated and lifted-off. **Figure 6.2** shows a TEM cross-section of a drawn L_g = 20 nm device.

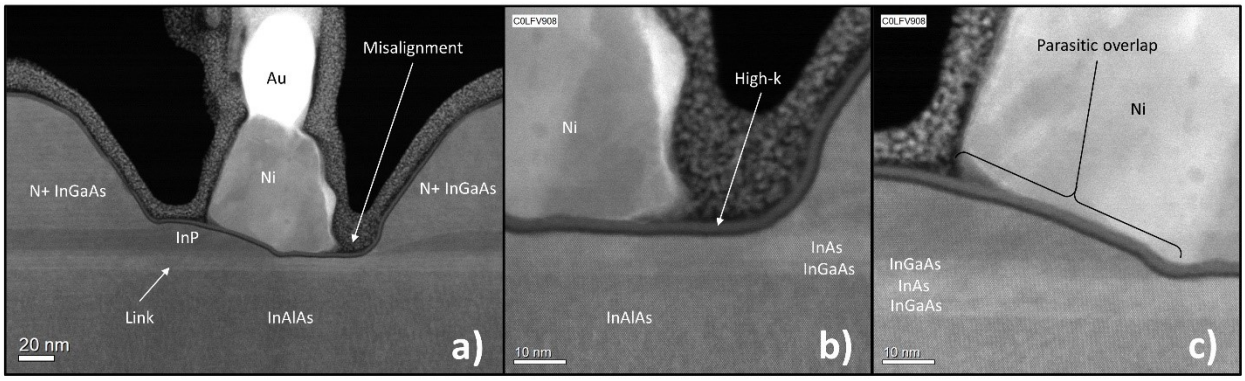

Figure 6.2 Cross-sectional TEM of drawn L_g = 20 nm ($\mathbf{0\bar{1}1}$) conduction device

Misalignment is observed between the first and second dummy gate while excellent alignment of the T-Gate to the second dummy gate is exhibited. The channel is only partially gated and severe parasitic overlap is observed. Due to the two-finger layout, large $C_{GS,p}$ and $C_{GD,p}$ are expected as well as excessive R_S due to the ungated region. The channel thickness is 7.0 nm, near optimal as discussed in **Chapter 2 Section F**. The link region is 15 nm in the access regions and 11 nm beneath the source-drain. No isotropic undercutting is observed.

B. Band Diagrams

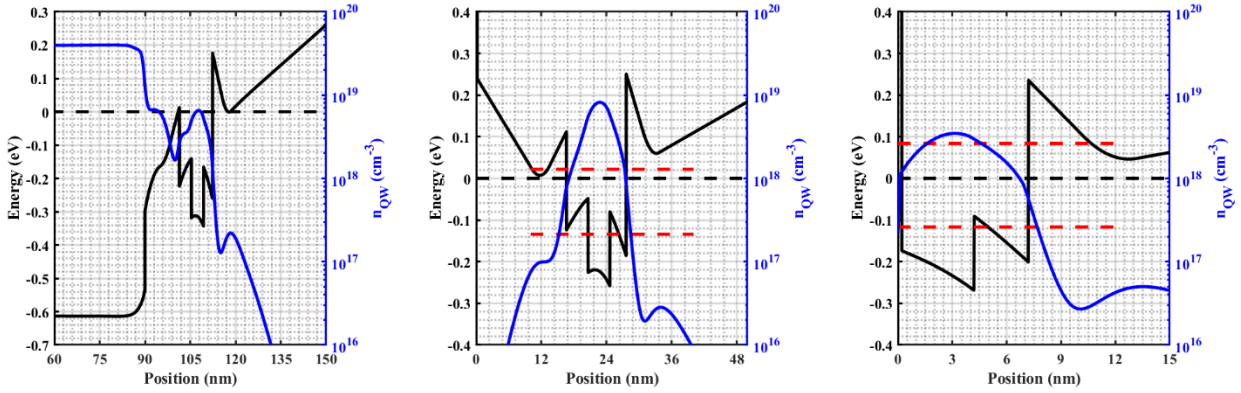

Figure 6.3 Band diagrams Generation 3 devices

Band diagrams were calculated using the 1D self-consistent Schrödinger-Poisson solver, BandProf, using dimensions determined by TEM cross-sectional imaging of the fabricated device. Band-diagrams of the source-drain, link quantum well, and channel at V_{GS} = 0.0 V are shown in **Figure 6.3**. No barrier to electrons exists beneath the source-drain regions despite the modulation doped InP not being completely removed. The link region is expected to exhibit n_L = 5.0 x 10^{12} cm^{-2} with no margin to add modulation doping in the top barrier. By reducing the link cap thickness, more modulation doping is expected to image on the surface rather than in the channel which could result in lower than designed n_L. t_{ch} = 7.0 nm gives

lower E_1 and more useable ($E_F - E_1$) enabling larger g_m. At large V_{GS}, n_{ch} exceeds $n_L/2$ and source-starvation is expected to limit both I_{DS} and g_m similar to Generation 1 devices.

C. DC Results

Figure 6.4 shows the transfer and output characteristics of a drawn L_g = 18 nm, $(0\bar{1}1)$ conduction device. The device exhibits peak DC transconductance ($g_{m,e}$) of 2.4 mS/μm at V_{DS} = 0.5 V and V_{GS} = 0.4 V. The extremely high DC $g_{m,e}$ is attributed to near optimal channel thickness as discussed in **Chapter 2 Section F**. At $t_{ch} \approx$ 7.0 nm, the in-plane effective mass is larger than bulk resulting in increased C_{DOS} while the channel Eigenstate is strongly confined yielding large C_{QW}. At this thickness, $E_{1,ch}$ is not excessive and most of the channel / back-barrier CBO is accessible, resulting in large $g_{m,i}$. Finally, the composite channel is predominately pseudomorphic-InAs which provides the largest available band-offset further maximizing $g_{m,i}$.

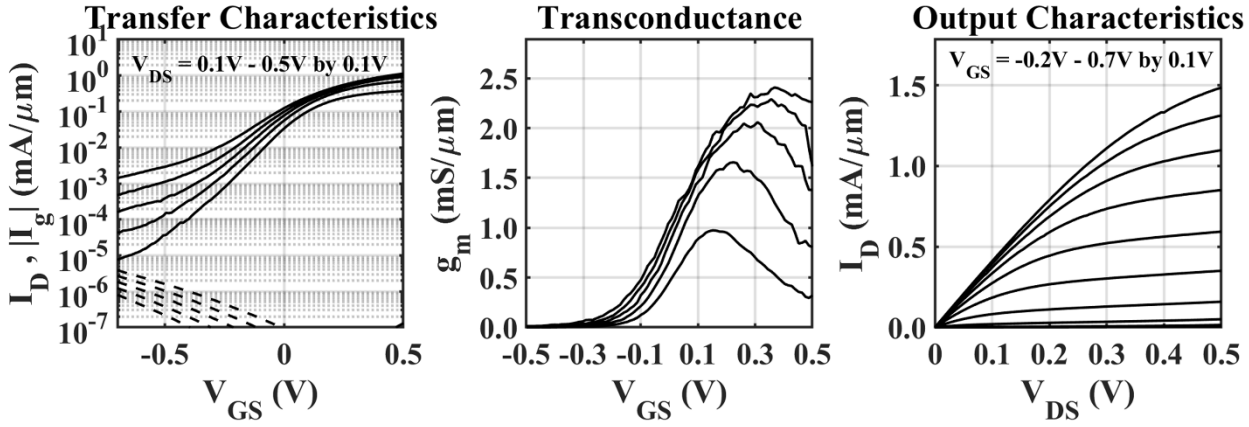

Figure 6.4 Drawn L_g = 18 nm, $(\mathbf{0\bar{1}1})$ conduction device a) transfer and b) output characteristics

Gate length series of DC figures of merits (FOMs) are shown in **Figure 6.5**. Peak g_m at V_{DS} = 0.5 V reaches 2.4 mS/μm before saturating for $L_g \leq$ 80 nm. Due to the thick channel, the wave-function is not strongly interacting with the quantum well edges (gate dielectric and

back-barrier) and a long electron mean-free-path is expected. Saturation at long L_g and $g_{m,e}$ < 3.0 mS/µm is unexpected since [1] and [2] reported higher DC $g_{m,e}$ for t_{ch} = 6.0 and 2.5 nm respectively. Based on **Section 2F**, t_{ch} = 7.0 should exhibit higher DC $g_{m,e}$ than [1] and [2], source resistance and/or source-starvation may be limiting $g_{m,e}$ [3], [4].

Unlike Generation 1 and 2 devices, Generation 3 devices exhibit $I_{off} \leq$ 10 nA/µm at V_{DS} = 0.1 V and $I_{off} \leq$ 10 µA/µm at V_{DS} = 0.5 V. The excellent I_{off} at V_{DS} = 0.1 V confirms that the InP etch-stop was the source of off-state leakage in previous generations while the relatively large I_{off} at V_{DS} = 0.5 V is expected for thick channel devices and is consistent with [1]. Additionally, $I_g \leq$ 10 nA/µm suggests that additional thickness scaling of the high-k can be done. Long gate length minimum subthreshold slope (SS_{min}) is 76 mV/dec corresponding to $D_{it} \approx 8 \times 10^{12}$ cm^{-2}.

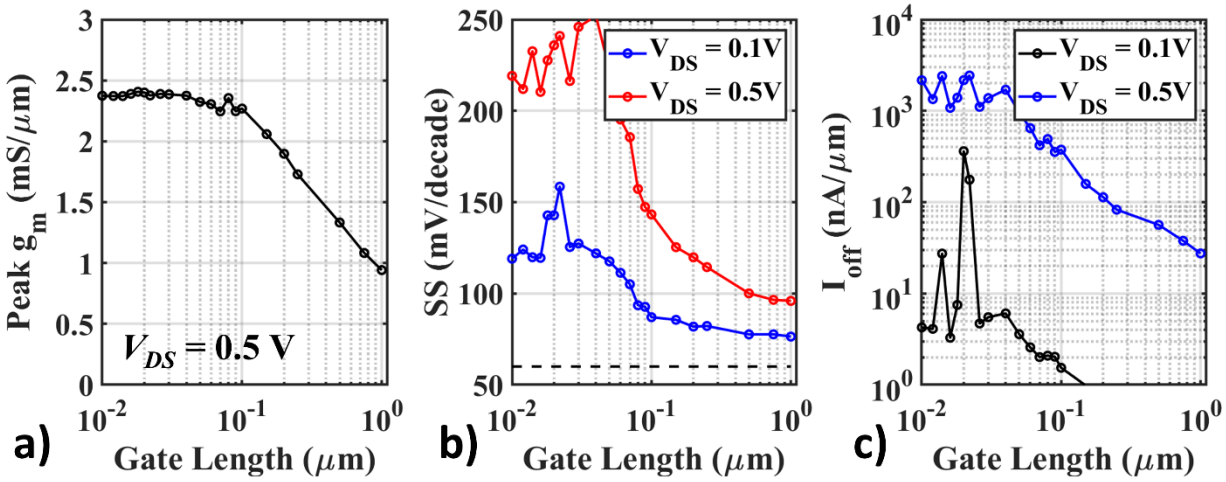

Figure 6.5 DC figures of merit for Generation 3 devices a) Peak g_m b) *SS* at V_{DS} = 0.1 V and 0.5 V c) DIBL

Figure 6.6 shows two sets of TLMs used to estimate components of the source-resistance. First, the N+ TLMs give R_N = 7.4 Ω•µm and R_C = 6.6 Ω•µm. The link TLMs give R_L = 11.2 Ω•µm and R_A = 49.4 Ω•µm resulting in a total R_S = 75.4 Ω•µm. Extrapolating R_{on} vs L_g gives

R_S = 121 Ω•µm. The increased top-side modulation doping and thinned link region enabled a 36 – 41 Ω•µm improvement in R_S compared to Generation 1. Moderate thinning of the link region beneath the source-drain regions preserved the process simplicity of Generation 1 while avoiding the severe isotropic undercutting observed in Generation 2.

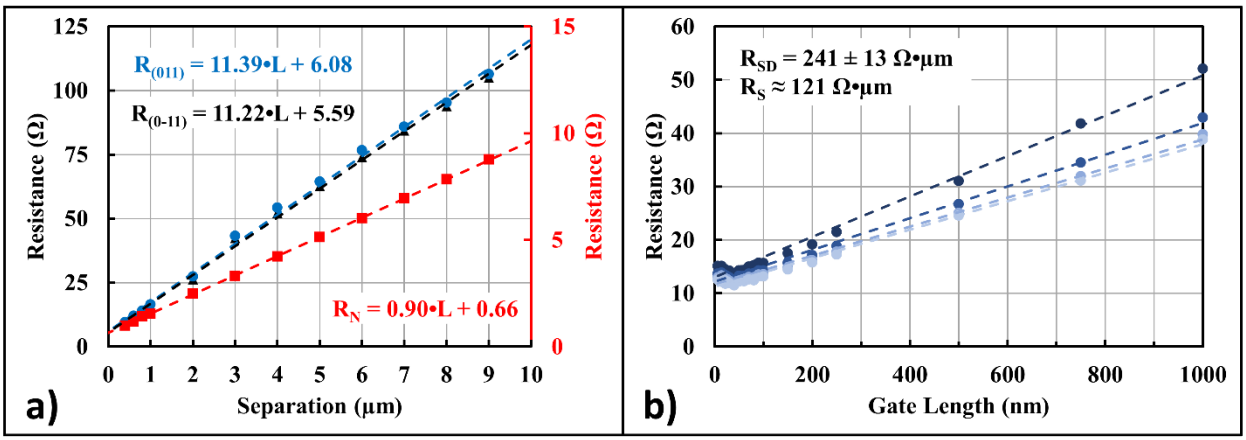

Figure 6.6 Generation 3 source-resistance extraction a) on wafer TLMs b) R_{ON} extrapolation at V_{GS} = 0.4 to 0.7 V

Increased modulation doping to reduce the tunnel barrier thickness was first proposed by [5] and utilized in subsequent $In_{0.52}Al_{0.48}As$ link devices [6]–[8]. Moderate link thinning beneath the source-drain region immediately prior to regrowth can further improve R_A as demonstrated by the improvement observed from Generation 1 to Generation 3 devices. To the best of our knowledge, R_S = 75 – 121 Ω•µm is the lowest reported in an InP-based HEMT. However, InP-based MOSFETs have reported $R_{on} \leq 200$ Ω•µm when the degenerately doped source-drain regions are directly adjacent the gate edge and narrow bandgap vertical spacers are used [1], [2], [9], suggesting that further improvements can be made. Increasing n_L to further prevent source-starvation will also decrease R_L further decreasing R_S. In the current design, using an InP top barrier, n_L cannot be further increased without populating a parallel 2DEG. Switching to $In_{0.52}Al_{0.48}As$ top barriers will facilitate increased n_L due to the larger

CBO. Unfortunately, this comes at the expense of larger R_A due to increased vertical sheet resistance and a larger tunnel barrier between the depleted δ-doping and channel.

D. RF Results

S-parameters were measured from 250 MHz to 67 GHz using on-wafer probing and –27 dBm port power. Prior to measurement, off-wafer load-reflect-reflect-match calibration was done. On-wafer open and short-circuit pad parasitics were de-embedded from the transistor measurements. f_T and f_{max} are determined by fitting the –20 dB/dec roll-off of H_{21} and U from 10 GHz to 50 GHz and 30 GHz to 45 GHz respectively. The order of pad extraction (open first vs. short first) only minimally changes the transistors extracted 2-port parameters, where the more pessimistic values (open-short) are reported. Like Generation 2 devices, short-open de-embedding produces typical Y-parameter behavior while open-short exhibits increasing $Re(Y_{21})$ with frequency. More robust de-embedding (TRL) is required to eliminate this discrepancy.

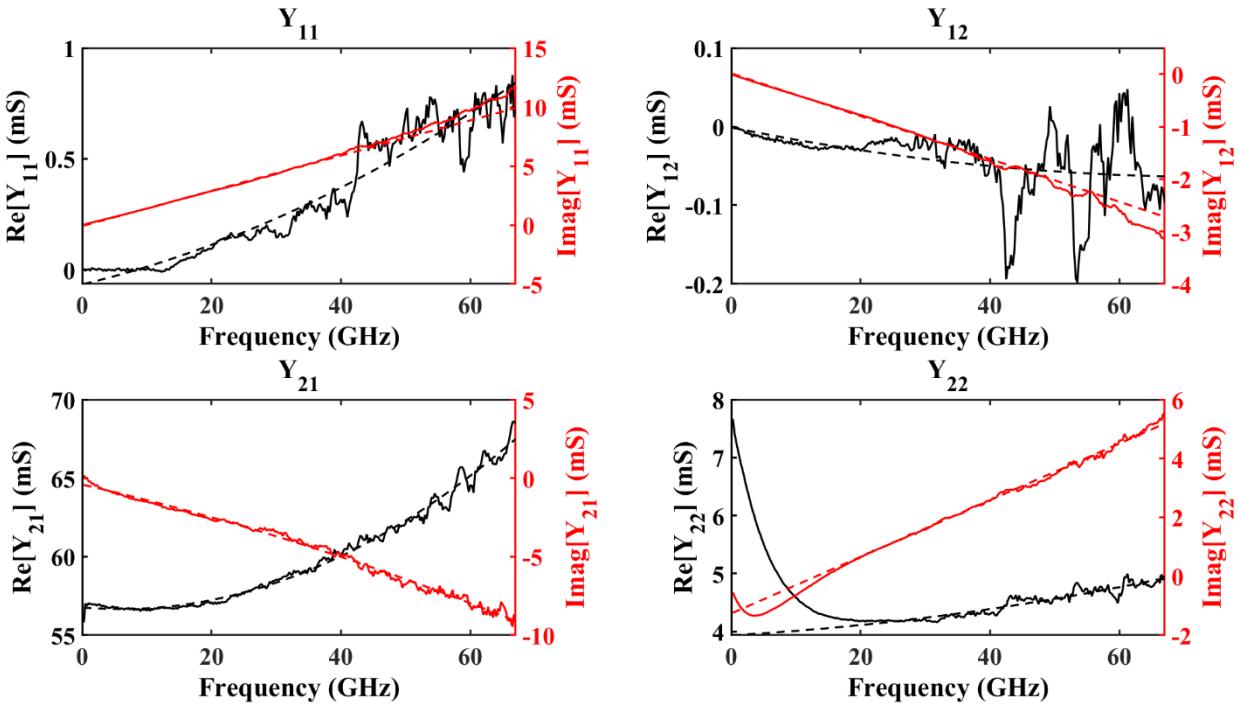

Figure 6.7 Open-Short de-embedded Y-parameters of L_g = 30 nm $(0\bar{1}1)$ conduction device shown with automated fitting used to determine SSEC parameters

Figure 6.7 shows open-short de-embedded Y-parameters of a L_g = 40 nm $(0\bar{1}1)$ conduction device. Automatic fitting is done to extract the small signal equivalent circuit parameters, shown in **Figure 6.7**. Devices exhibit f_τ , f_{max} in excess of 400 and 600 GHz respectively. f_{max} on many devices is difficult to determine by extrapolation due to peaking in the unilateral gain, like that seen in [10]. Values reported in **Figure 6.9** are determined by extrapolation which sometimes requires the f_{max} fitting range to be modified. **Chapter 6 Section E** discusses the model of a L_g = 30 nm device and likely more accurately represents the true f_{max}.

Peak $g_{m,e}$ is 2.8 – 3.0 mS/μm, higher than both Generation 1 and 2 devices and comparable to SOA HEMTs [7], [11] and MOSFETs [1], [9]. Despite the excellent g_m, the high frequency FOMs are lower than [7], [11] because $C_{GS} \geq 0.8$ fF/μm and $C_{GD} \geq 0.3$ fF/μm. To estimate the

parasitic gate-source capacitance ($C_{GS,p}$), a linear fit is applied to devices with L_g = 20 – 40 nm which all contain L_{foot} = 74 nm. As the gate length decreases, the parasitic T-Gate overlap increases. Therefore, a larger fraction of the measured C_{GS} is due to $C_{GS,p}$ rather than $C_{GS,i}$. Interestingly, C_{GS} is "U" shaped for L_g = 20 – 40 nm and separation of the two contributions is not possible. Given that the calculated value of $C_{GS,i}$ was in reasonable agreement with extracted parameters in **Chapter 5**, $C_{GS,i}$ was calculated and the remaining capacitance was attributed to $C_{GS,p}$. Calculated $C_{GS,i}$ is 0.093 fF/μm for L_g = 25 nm InAs channel devices, leaving $C_{GS,p}$ = 0.70 – 0.80 fF/μm. Because $C_{GS,i}$ is calculated at $V_{GS} = V_{TH}$, it severely underestimates C_{QW} and C_{DOS}. As n_{ch} increases, band-bending near the semiconductor / oxide interface moves the wave-function towards the interface, increasing C_{QW}. Simultaneously, due to non-parabolicity, m^* will increase as E_F increases, thus increasing C_{DOS}. However, from this rough calculation, it is clear that $C_{GS,p}$ is severely limiting RF performance. C_{GS} can be more rigorously determined by extraction from S-parameter measurements. **Figure 6.8** shows the S-parameter extracted CV characteristics and n_{ch}, $g_{m,e}$ vs. V_{GS} for a L_g = 40 nm device to be discussed further in **Section E**. $C_{GS,i}$ = 0.30 fF/μm corresponding to $C_{GS,p} \geq$ 0.50 fF/μm. Peak $g_{m,i}$ is observed at $n_{ch} \approx n_L/2$ and decreases with increasing V_{GS} suggesting source-starvation and a virtual increase in L_g as the source quantum well depletes.

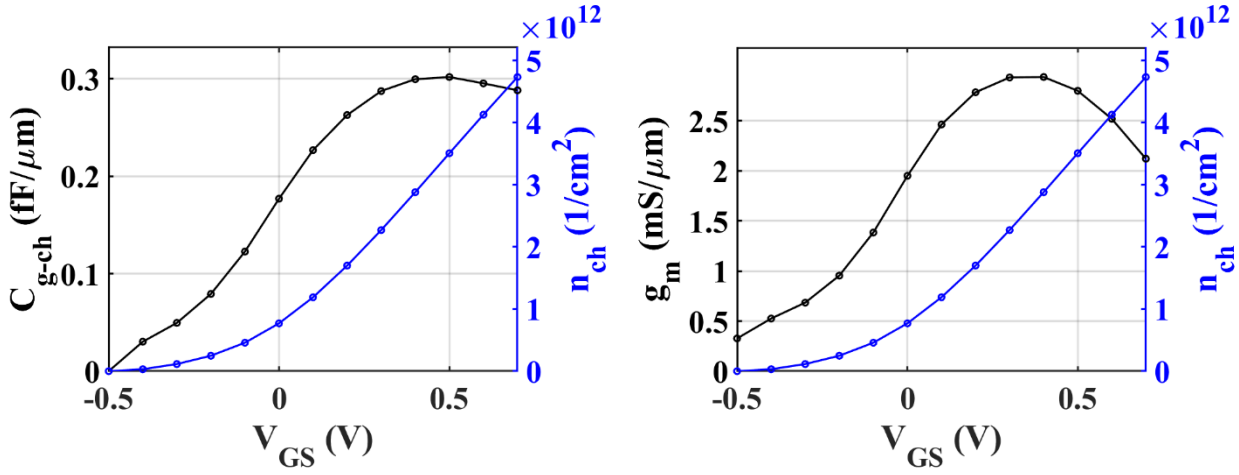

Figure 6.8 L_g = 40 nm $(\mathbf{0\bar{1}1})$ S-parameter extracted a) CV characteristics b) $g_{m,e}$ and n_{ch} at V_{DS} = 0.7 V

Given that g_m = 2.9 mS/µm is comparable to SOA, further improvements in the high frequency FOMs requires a significant reduction in $C_{GS,p} \leq 0.3$ fF/µm. This requires that the parasitic T-gate overlap be reduced. However, this is difficult due to re-alignment and T-Gate stem filling. A self-aligned regrowth reversal process, similar to the one reported in [12], may facilitate scaled gate-length MOS-HEMTs with acceptable R_G and $C_{GS,p}$.

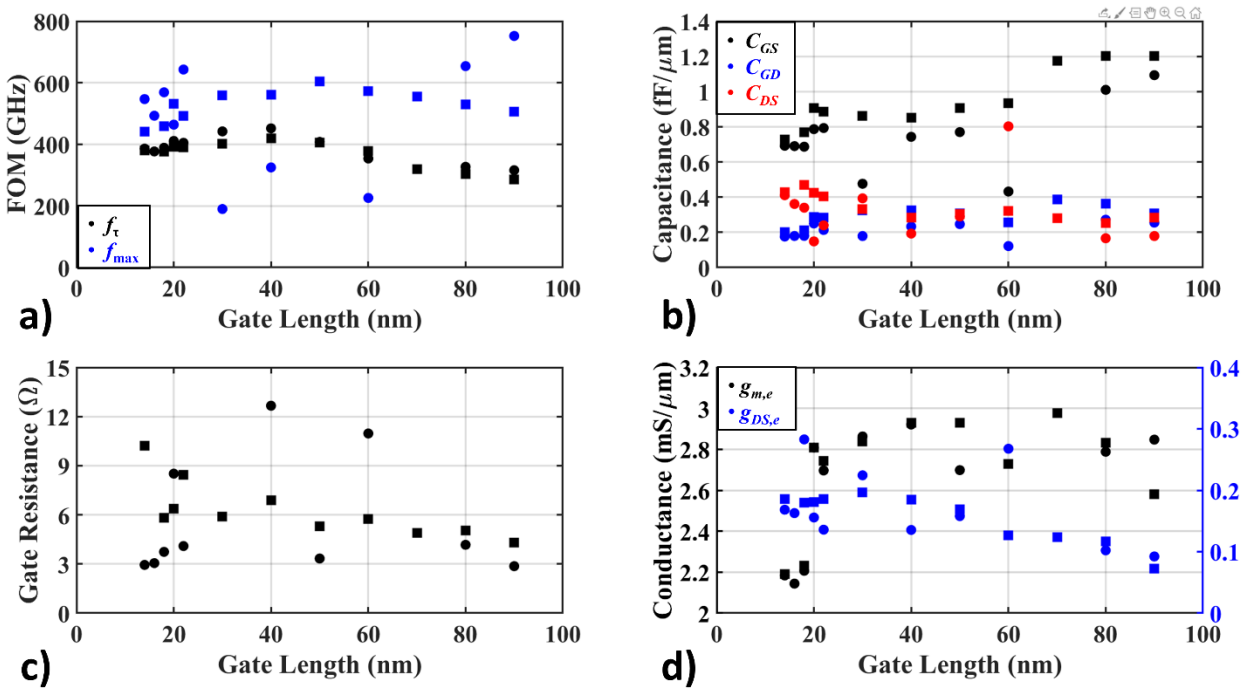

Figure 6.9 RF FOM and SSEC extraction of Generation 3 devices a) high frequency FOMs b) C_{GS}, C_{GD}, and C_{DS} c) R_G d) $g_{m,e}$ and $g_{ds,e}$

Generally $g_{ds,e} \leq 0.2$ mS/μm for $L_g \leq 60$ nm, corresponding to $g_{ds} = 0.18$ mS/μm and $g_m / g_{ds} = 15.5$ at $L_g = 20$ nm device. Generation 3 devices exhibit a more than 2x improvement in g_{ds} compared to [7] who reports $g_{ds} = 0.73$ mS/μm for $L_g = 25$ nm, $t_{ch} = 9.0$ nm. The clear improvement in electrostatics and excellent transconductance demonstrates that the MOS-HEMT can exceed the performance of standard HEMTs if the parasitic capacitances can be reduced. Finally, $C_{DS} \geq 0.30$ fF/μm is high compared to [7]. The high modulation doping (3.6 x 10^{12} cm^{-2}) allows electrons from the source to be injected into the back-barrier which could then be modulated by the drain [13]. Future channel designs will move charge from the back-barrier modulation doping to the top-barrier modulation doping which will enable better confinement in the gated region, facilitate higher ($V_{GS} - V_{TH}$), improve R_S, and reduce C_{DS}.

E. Equivalent Circuit Model

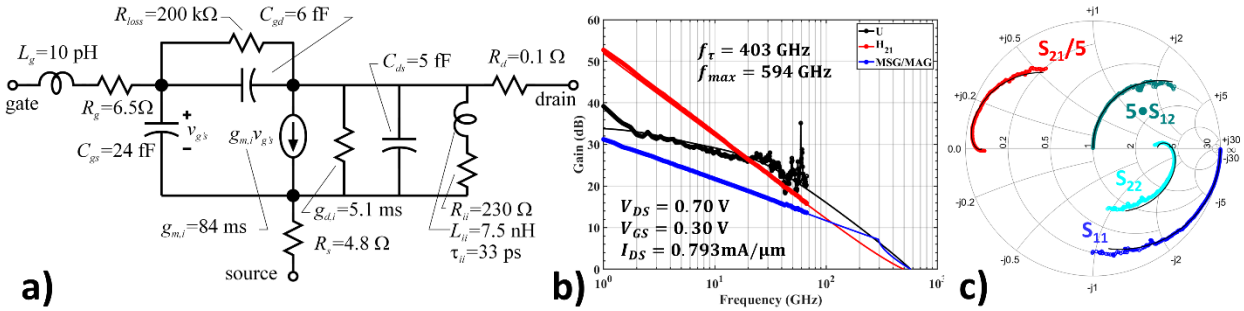

Figure 6.10 a) Small signal equivalent circuit b) measured / modeled FOMs c) and measured / modeled S-parameters of L_g = 40 nm $(\mathbf{0\bar{1}1})$ conduction device at V_{DS} = 0.70 V, V_{GS} = 0.30, I_{DS} = 0.793 mA/µm

The common-source small-signal equivalent circuit (SSEC) model for the above described L_g = 40 nm $(0\bar{1}1)$ conduction device is shown in **Figure 6.10**. Extraction of the equivalent circuit is as follows: measured S-parameters are converted to Z-parameters and fit at large $(V_{GS} - V_{TH})$ (fully inverted) and V_{DS} = 0 V to extract R_S, R_D, and R_G. At V_{DS} = 0 V, the source and drain are symmetric so $R_S = R_D = R_{SD} / 2$. At large V_{DS} the drain side depletes, and R_D becomes very small. Extracted R_S is 90 – 110 Ω•µm, higher than the 75 Ω•µm measured by TLM and comparable to the 121 Ω•µm from R_{on} extrapolation.

Next, the measured S-parameters are converted to Y-parameters and fit to extract g_m, g_{ds}, C_{GS}, C_{GD}, and C_{DS}. Imag(Y_{12}) is fit from 250 MHz to 40 GHz to extract C_{GD} while Imag(Y_{11}) is fit over the same range to extract C_{GS}. High frequency components result in slight curvature in Imag(Y_{11}) and Imag(Y_{12}) and thus 40 – 67 GHz data is ignored during initial fitting. Re(Y_{21}) and Re(Y_{22}) are fit and extrapolated to f = 0 GHz to determine extrinsic g_m and g_{ds} respectively. Moderate D_{it} and gate inductance (L_G) causes low frequency dispersion in Re(Y_{12}). Because this effect is minor and only causes deviation below 3 GHz, the entire frequency range is fit. Because Y_{22} is complicated and contains many high and low frequency contributions, Re(Y_{22})

is fit from 20 – 40 GHz to avoid convoluting the series *L*-*R* network associated with breakdown effects at low frequency while also avoiding high-frequency contributions. Similarly, Imag(Y_{22}) is fit over the same range to extract C_{DS}.

The SSEC is modeled and simulated in Keysight's Advanced Design System (ADS) software. SSEC parameters are adjusted until the best fit is realized over the entire 250 MHz – 67 GHz range. Fitting open-short de-embedded real(Y_{21}) and Imag(Y_{21}) is not possible with reasonable SSEC values. Including $L_G \approx 10$ pH and $\tau = 0 - 2$ ps flattens Re(Y_{21}) but does not account for the high frequency increase observed in **Figure 6.7**. Short-open de-embedded data is more easily fit with the SSEC shown in **Figure 6.10** but yields larger high frequency FOMs and is therefore not discussed. Future measurements must include more robust TRL calibrations. Once a best fit is established, the model is simulated from 250 MHz to 1 THz and to determine the high-frequency FOMs. **Figure 6.11** shows measured and modeled S-parameters and FOMS. At peak f_τ bias, measured and modeled are identically f_τ = 403 GHz and f_{max} = 594 GHz.

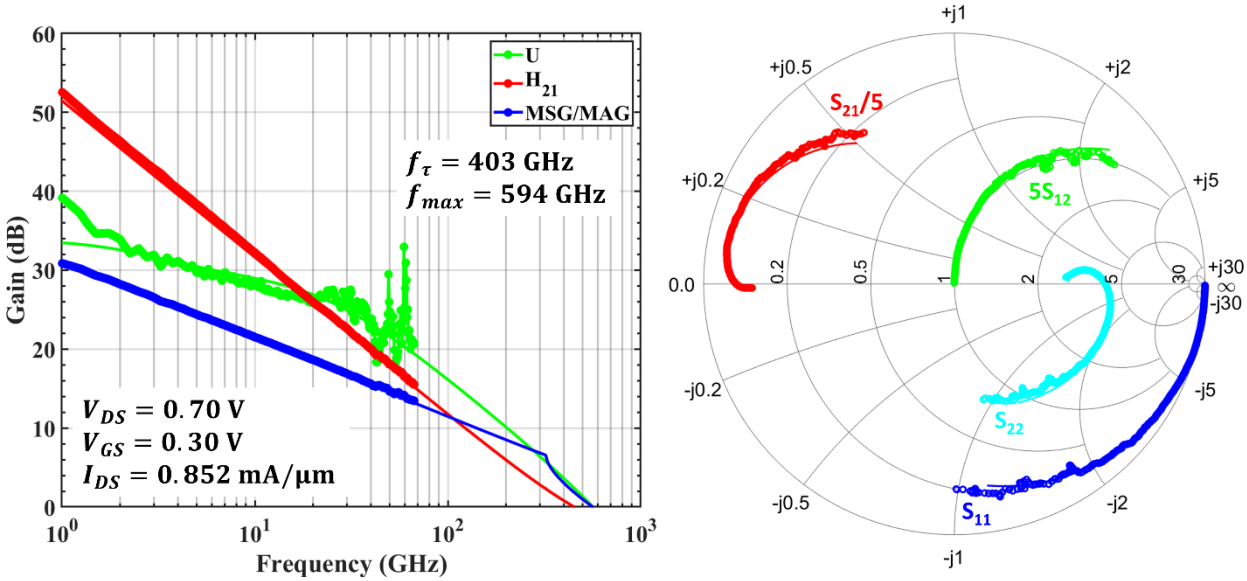

Figure 6.11 Measured and modeled U, H_{21}, and MAG/MSG for L_g = 40 nm $(\mathbf{0\bar{1}1})$ device

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7. Confined Epitaxial Lateral Overgrowth (CELO)

A. Motivation

Hetero-integration of III-V on Si has long been a goal of research. Bulk planar growth of III-V on Si is difficult because of the severe lattice and thermal mismatch as well as polarity differences between substrate and grown material [1]. Selective area growth (SAG) has gained significant attention because defects can be spatially confined by a dielectric mask and reduced defect density, lateral overgrowth can be realized [2], [3]. However, standard SAG generally yields overgrowth thickness (t_{OG}) on the order of the lateral overgrowth length (L_{OG}) which are not compatible with CMOS manufacturing [4]. While the resulting growth geometry is controlled by growth parameters (temperature, pressure, III/V), arbitrary geometries cannot be realized. Because highly scaled electronic devices require ultra-thin-bodies (UTB), t_{OG} must be kept small (~50 nm) while L_{OG} must be large (~1 μm) [4]. Consequently, some way of defining high aspect ratio, arbitrarily oriented III-V overgrowth is desired. Template assisted selective epitaxy (TASE) is a SAG technique where a top dielectric is used to confine vertical growth while a hollow cavity is used to define the growth direction. While TASE was initially developed for SOI applications [5]–[7] and later adapted for heterogenous integration [8]–[11], the ability to laterally turn the growth front and define an arbitrary growth geometry opens an additional degree of design space previously not available to III-Vs [12], [13]. Limited studies about growth physics in confined structures have been conducted [14], [15]. The following sections will discuss the development of homoepitaxy TASE on InP for tunneling field effect transistors, to be discussed below.

Moore's Law guided transistor scaling for 50 years and is most generalized as the doubling of transistor density each generation (~2 years). MOSFET scaling, laid out in [16], says that

the supply voltage V_{DD} should be decreased while a large I_{on}/I_{off} maintained. In very large-scale integration (VLSI), static leakage ($P_{static} = I_{leak}V_{DD}$) determines the maximum supply voltage (V_{DD}) which can be used. However, because subthreshold slope in a MOSFET is dictated by thermal physics, discussed in **Chapter 2**, the minimum *SS* achievable is 60 mV/dec. As a result, if V_{DD} is reduced below 0.5 V, I_{on} becomes unacceptably low; if instead designing for I_{on}, I_{off} becomes unacceptably high. In order to continue scaling V_{DD} while maintaining I_{on}/I_{off}, transistors with $SS < 60$ mV/dec are required, illustrated in **Figure 7.1**. Because a tunnel FET's IV characteristics are dictated by quantum mechanical tunneling probability, not thermal population of states, they can achieve sub-thermal switching and are of significant interest for future VLSI applications.

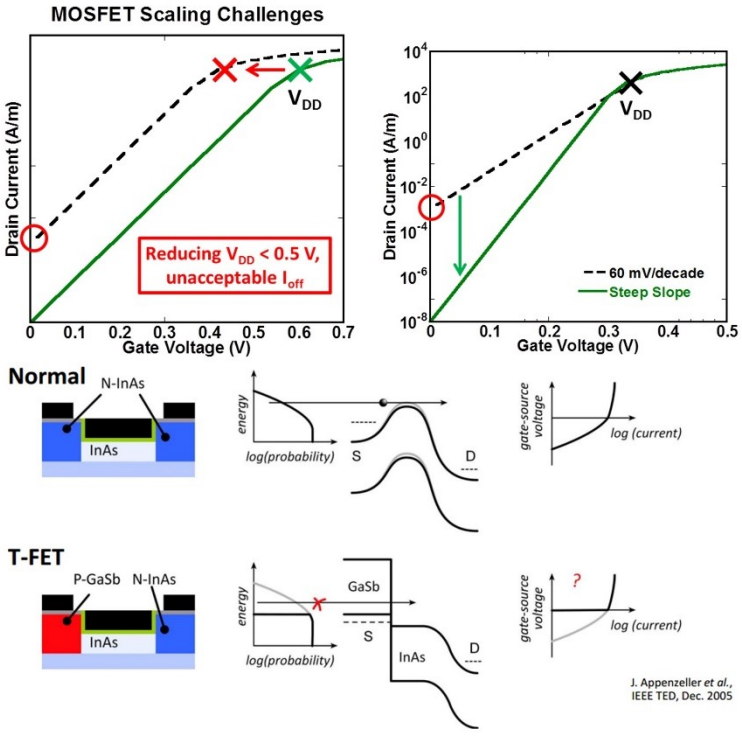

Figure 7.1 a) Transfer characteristics of MOSFET b) motivation for steep-slope device c) illustration of the mechanisms responsible for sub-threshold behavior.

Many TFETs exhibiting sub-thermal switching have been demonstrated. However, state-of-the-art TFETs exhibit I_{on} < 100 μA/μm, limited by the large tunneling barrier [17]–[19]. Small I_{on} results in large charging time-constants and limits frequency of operation. Recently proposed triple heterojunction (3HJ) TFETs can realize $I_{on} \geq 100$ μA/μm by using two-dimensional quantum confinement near the tunnel junction [20] and $[1\bar{1}0]$ conduction [21]. Subsequent simulated generations leveraged materials to which a high-quality gate oxide can be made [22] and simplified the 3HJ to use only binary materials [23], simplifying growth.

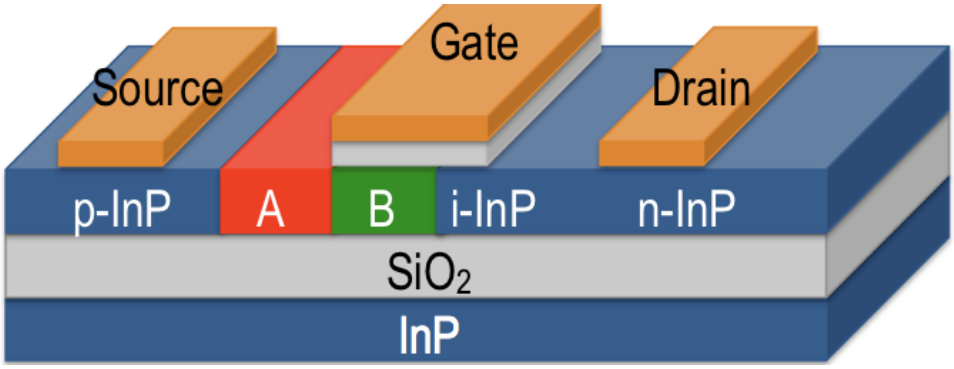

Figure 7.2 Simplified 3HJ-TFET fabricated using laterally grown material by CELO

Modern TFET fabrication techniques include edge fabrication by facet selective etching [24], nanowire etching [25], and nanowire growth [26]; however, none have produced structures < 5 nm to be useful for the TFET designs detailed in [20]–[23]. Facet selective etching and transistor fabrication on the etched facets does not provide the necessary lateral confinement and forces conduction in <111> rather than [110]. Etching nanowires can provide for self-aligned gate processes and <100> conduction but has only produced channel widths of ~25 nm – not the < 10 nm required for strong quantum confinement [25]. Finally, nanowire growth often suffers from "fuzzy" heterojunctions due to the reservoir effect of metal catalyzed nanowire growth [27], channel thickness of > 40 nm as defined by nanowire diameter, and poor gate alignment along the vertically oriented junction [26]. To produce an

effective 3HJ-TFET it is critical to have a channel thickness of < 10 nm, gate alignment < 2 nm (to insure high field region is at tunnel junction) [28], and atomically abrupt heterojunctions.

IBM's demonstration of confined epitaxial lateral overgrowth (CELO) and template assisted selective epitaxy (TASE) provide pathways to create low defect density, laterally oriented heterojunctions [9], [10], [29], [30]. CELO enables rotated, atomically abrupt heterojunctions grown from a non-metal catalyzed, lattice-matched semiconductor seed. Additionally, it provides the ability to leverage staggered gate-alignment and monolayer channel thickness control. Finally, CELO material is compatible with the widely reported UCSB FET process [31]–[33], enabling fast learning cycle as well as yet unimagined 3D devices. The proposed TFET structure from [23] using laterally grown material by CELO [29] is illustrated in **Figure 7.2**.

In this section, homoepitaxy TASE will be discussed to be applied to InP based tunneling field effect transistors (TFETs). The focus will be on process considerations for TASE templates and template effects on growth. Specific information regarding growth parameters, facet control, and characterization of homo and heteroepitaxy TASE can be found in the theses of Simone Tommaso Šuran Brunelli (MOCVD growth) and Aranya Goswami (characterization).

B. Fabrication Process

Three layers are required for TASE on III-V: 1) growth window 2) sacrificial layer 3) gas inlet. A typical TASE template geometry, used throughout this thesis, is illustrated in **Figure 7.3**. The growth window, referred to as the "seed", is a hole in the bottom dielectric that exposes a small area of III-V material for the metal-organic precursors to nucleate on. Because

the bottom surface, inside the target cavity, is defined by the seed dielectric, it must provide high growth selectivity. Additionally, the seed can be defined in many geometries (point, square, line, etc.) and at many locations (edge, center, pinch-point, etc.) within the cavity.

The sacrificial layer defines the cavity volume (length, width, and thickness) to be grown and must be selectively removeable from the seed dielectric layer and the top dielectric layer. Growth inside the template strongly depends on the geometry of the template as well as the quality of the internal surfaces. Rough edges and chemically modified surfaces can cause unwanted parasitic nucleation. As a result, the choice of sacrificial material, etch technique, and removal technique is perhaps the most important.

The gas inlet layer, referred to as the "source", defines the SAG surface and determines growth selectivity as well as the mechanical stability of the cavity. Because TASE patterns reported in this thesis were fabricated by electron beam lithography (EBL) and because the growth front in a cavity is only a cross-section (t_{sac}•W_{cavity}), the fill-factor is extremely low (<10%). Consequently, the growth selectivity of the III-V growth front to the source layer dielectric must be extremely high otherwise growth will predominately occur randomly across the dielectric. Because the cavities are hollow, the top dielectric layer can expand and contract during growth due to the thermal mismatch of the dielectric and semiconductor. This can cause the cavity to bow or collapse. With these constraints in mind, the following sections will address each layer in detail.

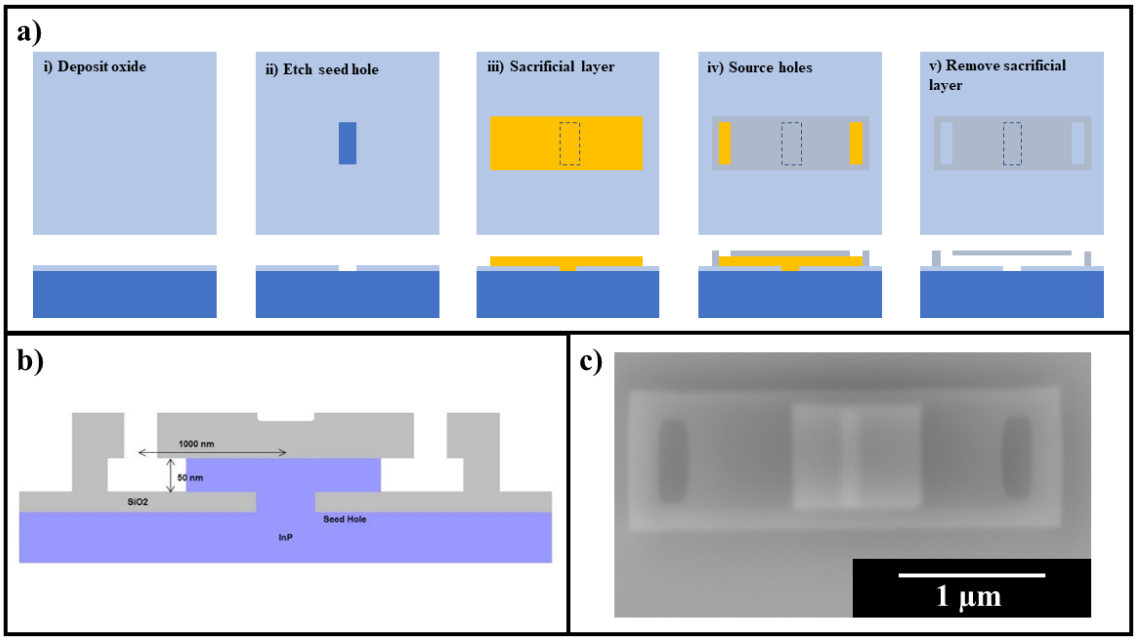

Figure 7.3 a) cross-sectional and top-down view of CELO template fabrication b) illustration of template cross-section after growth c) top-down SEM of CELO structure with visible overgrowth

The general fabrication of TASE structures is illustrated in **Figure 7.3**. First, the seed dielectric is deposited, and growth windows are defined and etched. The sacrificial layer is then deposited and patterned. The source dielectric is then deposited, patterned, and etched to expose a small portion of the sacrificial layer. Finally, the sacrificial layer is selectively removed, and the growth window cleaned of contaminants.

Before beginning the discussion of template fabrication, the target geometry needs to be defined considering the final device. Atomistic simulations of 3HJ-TFETs detailed in [23] require 30 – 50 nm of lateral growth and 5 nm thick bodies. Body thickness is defined by the sacrificial layer thickness and can be controlled by deposition technique. Additionally, post-growth thinning of the laterally overgrown material can be done if a thicker body facilitates better or easier growth. While only 30 – 50 nm of lateral overgrowth is required for the intrinsic device, the overall lateral dimensions are determined by the extrinsic device. Because

the designed TFET should operate at V_{DS} = 0.3 V, it is necessary to minimize the parasitic series resistance: contact resistances and sheet resistance. To properly measure the intrinsic device when the junction is turned on, the source resistance (R_S) should account for <10% of the total supply voltage drop V_{DS}: no more than 30 mV.

To realize sufficiently low contact resistivity, it is necessary for at least one transfer length L_T to be contacted. From [34], degenerately doped n-InGaAs and p-InGaAs, can achieve specific contact resistance (ρ_c) of 4 Ω•μm^2 if doped ~4.0 x 10^{19} cm^{-3}. For the structure illustrated in **Figure 7.3**, using estimated mobility from [34], this corresponds to R_{sheet} = 650 Ω/□. The resulting contact resistance for a 300 nm x 1.0 μm is 14 Ω and $L_T \geq$ 80 nm. The corresponding voltage drop for I_{on} = 300 μA/μm is V_{source} = 5 mV. Including 50 nm alignment tolerance in the EBL, an additional $I_{on}R_{sheet} = V_{sheet}$ = 10 mV is included. With intrinsic device length of 30 nm and extrinsic device length of 350 nm (on either side), the total cavity length should be ≥750 nm. Therefore, standard cavity lengths discussed in this thesis are 1 μm to enable sufficient lateral overgrowth for device fabrication while preventing outgrowth from the source hole.

1. Seed Layer

The seed dielectric must provide a window to the substrate for growth to occur and be highly selective. Generally, oxides are used as masks in selective area growth because of their high growth selectivity, easy patterning, and thermal stability. Previous TASE studies have used both thermal oxides and deposited oxides for top and bottom dielectrics [5], [7], [29]. Because thermal oxides are not available on III-Vs, a deposited oxide must be used. The chemistry and topography of deposited oxides are determined by the deposition technique. For example, atomic layer deposition (ALD) oxides generally have large background oxygen

and nitrogen content due to incomplete reaction of the metal organic precursors. In contrast, sputtered material can be extremely pure because the beginning source material can be single element, solid source, electronic quality. However, the sputter chambers at UCSB have many sources simultaneously loaded – including metals – and there is likely background contamination of the chamber. Additionally, sputtering parameters can be modified to determine the film and topography.

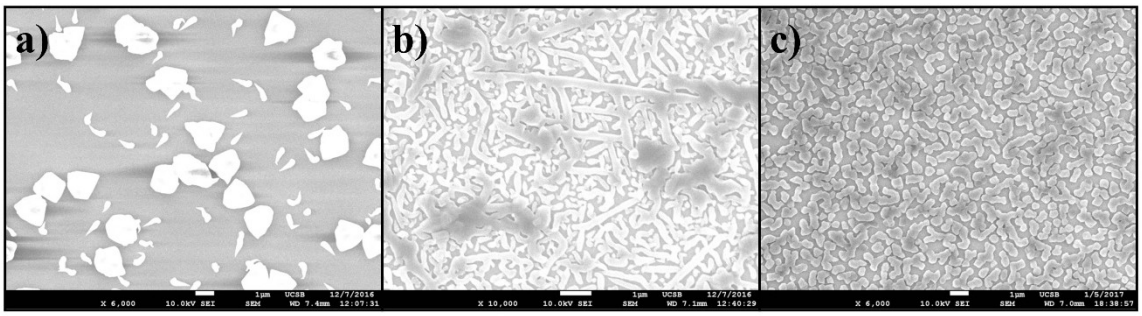

Figure 7.4 MOCVD SAG trials on un-patterned SiO_x deposited by a) PECVD b) ALD c) sputter

Given the many degrees of freedom for each tool, the simplest way to determine the optimal dielectric deposition technique is to compare growth on all available oxides. Oxides were deposited on blank silicon wafers and InP MOCVD growth was conducted using standard growth conditions: T = 600°C, P = 350 Torr, V/III = 375 for two minutes. The substrates were un-patterned as the intent was to determine which oxide exhibited to the least parasitic growth. **Figure 7.4** illustrates a comparison between plasma enhanced chemical vapor deposition (PECVD), ALD, and sputtered SiO_x. ALD and sputtered SiO_x are completely covered in growth while PECVD SiO_x has isolated areas of growth. PECVD SiO_x was determined to have the highest MOCVD growth selectivity of available oxides at UCSB.

Thickness control of the oxide is not critical as the channel thickness is set but the sacrificial layer thickness; however, roughness is critical because roughness in the seed oxide

becomes roughness in the field during lateral overgrowth. For a UTB device, roughness in the semiconductor corresponds to variation in body thickness resulting in variation in Eigenstate energy, which limits performance. Because roughness increases with increasing thickness, it is necessary to keep the bottom oxide thin. Additional thickness in the bottom oxide also effectively lengthens the cavity, forcing the precursors to travel further to the growth front during growth initiation.

Next, growth windows can be defined in an oxide by dry etching or wet etching. Trials of both are shown in **Figure 7.5**. SiO_x is commonly dry etched using fluorine chemistries or wet etched using hydrofluoric acid (HF). Wet etching using HF is isotropic and causes pattern growth which is undesirable. Additionally, BHF etches SiO_x ~500 nm/min making it extremely difficult to control etch depth and time for 20 – 50 nm thick oxides. Dilute HF can slow the etch rate but still exhibits isotropic etch profiles.

Dry etching provides better control of etch rate and exhibits anisotropic profiles. Inductively coupled plasma (ICP) etching of SiO_x is typically done with combinations of CHF_3, CF_4, and O_2 and yields etch rates of 1-3 nm/s with etch angles of 60-90°. To test the growth window opening, PECVD SiO_x was blanket deposited on n-InP substrates, patterned with EBL, then ICP etched in $CHF_3/CF_4/O_2$ using 500W/50W ICP/CCP power. The photoresist was then stripped in NMP. Samples were then grown on by MOCVD and chemical beam epitaxy (CBE). Chemical beam epitaxy is like molecular beam epitaxy (MBE) except metal organic (MO) precursors are used. Like MBE, CBE has small diffusion lengths and is very sensitive to surface preparation. Interestingly, MOCVD grown samples exhibit smooth topology while CBE grown samples exhibited island growth. Micro-masking of the InP growth surface by In_xF_y dry etch residues is suspected. Because CBE has small surface

diffusion length compared to MOCVD, precursors would not diffuse across the micro-masked area to coalesce. In MOCVD, precursors have a long diffusion length and thus growth quickly coalesces and propagates smoothly. In order to clean the InP surface of residues prior to growth, 1-5 cycles of digital etching with cycles of 10 minutes of UV ozone and 1 minute of $HCl:H_2O$ 1:10 was done. No improvement in CBE growth topology was observed. More aggressive cleaning with H_3PO_4:HCl 3:1, shown in **Figure 7.5**, exhibited improved growth quality at the expense of rapid undercutting of the dielectric mask.

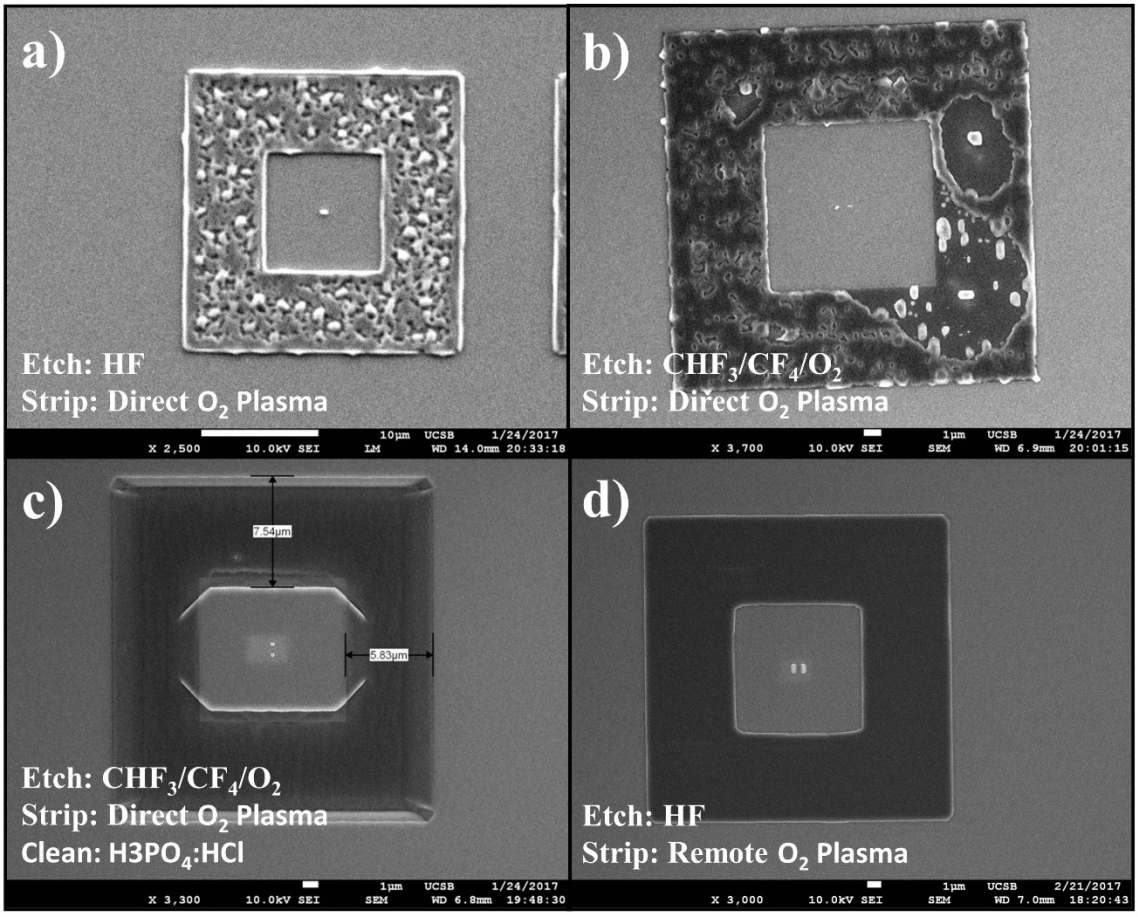

Figure 7.5 SAG window patterning and resist stripping trials

Rather than clean the surface after damaging it, an etch stop layer can be used to prevent the InP surface from being exposed to fluorine. Aluminum oxide is a suitable etch stop layer

as it exhibits high etch selectivity in fluorine chemistry due to the formation of non-volatile Al_xF_y. It can also be deposited by thermal ALD, preventing ion damage to the growth surface, and protecting it during the PECVD SiO_x deposition. Finally, it can be easily removed in NaOH, KOH, or TMAH. Because resist developers are commonly based on TMAH and are already used in the process flow, AZ300-MIF was used to remove the Al_2O_3 layer after dry etching.

Finally, resist stripping must also be considered. Dry etching can cause the formation of fluorinated "skins" on exposed surfaces of the photoresist. Skins are cross-link fluorocarbons that are analogous to Teflon and are therefore difficult to remove. Resist "ashing" is commonly done to remove skins. Classically, a direct O_2 plasma is used to chemically react with and physically sputter the cross-linked resist. At UCSB, this is done using the PEIIs at 300 mTorr and 100 W – higher power than the ICP used to etch the SiO_x. CBE growth on PEII ashed samples exhibit growth exclusions suggesting damage, possibly due to ion bombardment, illustrated in **Figure 7.5**.

Rather than ashing with direct plasma, ashing can also be done using an indirect plasma. In this technique, a remote plasma is generated and then flowed across a heated wafer where the dissociated oxygen aggressively reacts with organic residues. Remote plasma etching does not introduce any ion damage and can be done at UCSB using the Gasonics or the YES. Samples ashed using the Gasonics exhibit smooth CBE growth in exposed areas suggesting a damage free surface. Best CBE growth topology in selective area growth, dry etched growth windows were observed when:

i. ALD Al_2O_3 – protects the surface from ion damage in PECVD deposition, ICP etch, and resist strip and is easily removed at the end of the process in photoresist developer

ii. PECVD SiO_x – exhibits the highest growth selectivity and is easily dry etched in $CHF_3/CF_4/O_2$

iii. ICP dry etch – controllably removes SiO_x and stops on Al_2O_3

iv. Indirect plasma resist strip – does not introduce ion damage and aggressively removes fluorinated skins formed during ICP etching

Finally, because the desired TFET requires the use of (110) substrates [21], wafers must be diced rather than cleaved. Dicing produces micron sized dust particles that re-deposit on the oxide surface. Removal of the dicing protection resist without redeposition of the dust on the oxide is necessary to prevent parasitic nucleation on the dust rather than in the growth window. To do so, the wafers are spun at 5 kRPM for 2 minutes while spraying with NMP. The resist slowly removes from the top side and the dust is flung from the surface. The NMP strip is insufficient to produce a clean surface for regrowth, as illustrated in **Figure 7.6** and an additional remote plasma treatment must be done to remove any remaining resist residue.

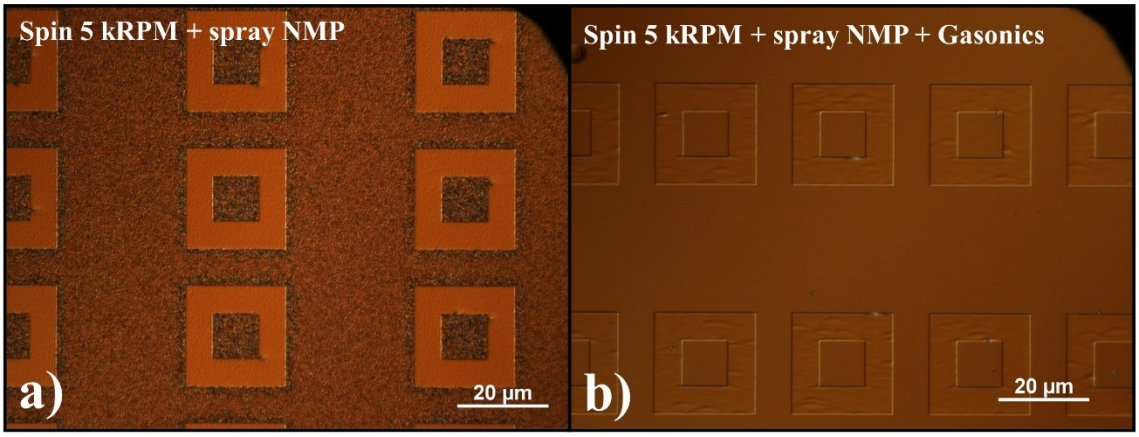

Figure 7.6 SAG growth on substrates with various surface preparation

2. Sacrificial Layer

The sacrificial layer is used to define the geometry and dimensions (L, W, t) of the cavity. It must be easily and selectively removed from the top and bottom dielectric and must also be

smoothly etched to prevent edge roughness that can cause parasitic nucleation. Because the sacrificial layer removal etch progresses laterally from the "source hole" to the "seed hole", the effective "etch depth" is the length of the cavity. If the sacrificial etch chemistry attacks SiO_x, that etch will manifest itself as a vertical etch from the inside *and* outside SiO_x surfaces. To realize the designed structure without unintentionally exposing the substrate, the etch selectivity must be better than L_{cavity} / t_{ox} = 1 μm / 20 nm = 50.

Silicon and aluminum oxide are commonly used materials that can be selectively removed from SiO_x. Aluminum oxide can be selectively removed by wet etching in TMAH. However, the etch rate is slow unless heated and heated TMAH slowly attacks SiO_x. Attempts at using an Al_2O_3 sacrificial layer had multiple problems:

1. Deposition of Al_2O_3 is generally done by ALD which can be advantageous for very thin cavity structures but is a limitation if $t_{cavity} \geq 20$ nm
2. Etching Al_2O_3 requires high power which can burn photoresist unless a hard-mask is used, adding to process complexity
3. TMAH removal of Al_2O_3 is slow and etches SiO_x which results in collapsed cavities and etch stop removal if pinholes are present in the seed SiO_x
4. If cavities of different lengths are present on sample, the removal etch must proceed long enough to clear the longest cavity resulting in an undercut of the Al_2O_3 etch stop in the growth window of shorter cavities
5. Capillary forces associated with liquid leaving the cavity during drying can cause the cavities to collapse

Silicon on the other hand can be removed with nearly infinite selectivity to SiO_x and Al_2O_3 using XeF_2. Because XeF_2 is a gas, concerns about capillary forces in the small cavity are

mitigated. Silicon can be deposited by PECVD or sputtering and can be etched in fluorine or chlorine chemistry at low power. Structures fabricated with an Al_2O_3 and an a-Si sacrificial layer are shown in **Figure 7.7**.

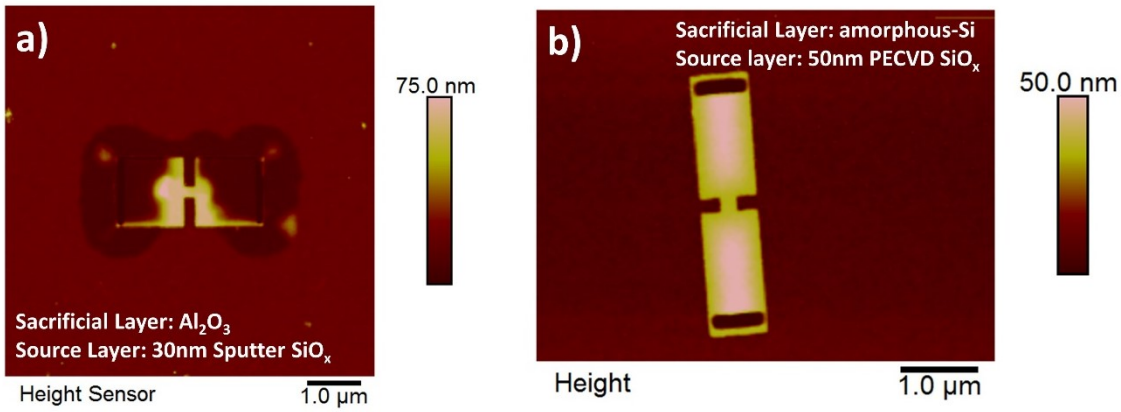

Figure 7.7 Fabricated CELO structures after sacrificial layer removal a) Al_2O_3 sacrificial layer b) amorphous-Si sacrificial layer

Another technique, also used in this thesis, is to use photoresist (PR) as the sacrificial layer. PR can be spun to a desired thickness, planarizes surface topography, is easily patterned, and easily removed. Aggressively thinned cavities, formed using the described a-Si process, exhibit pinch points due to conformal deposition of the sacrificial layer that can prohibit gas flow. Planarization of the surface eliminates this constriction, illustrated in **Figure 7.8**.

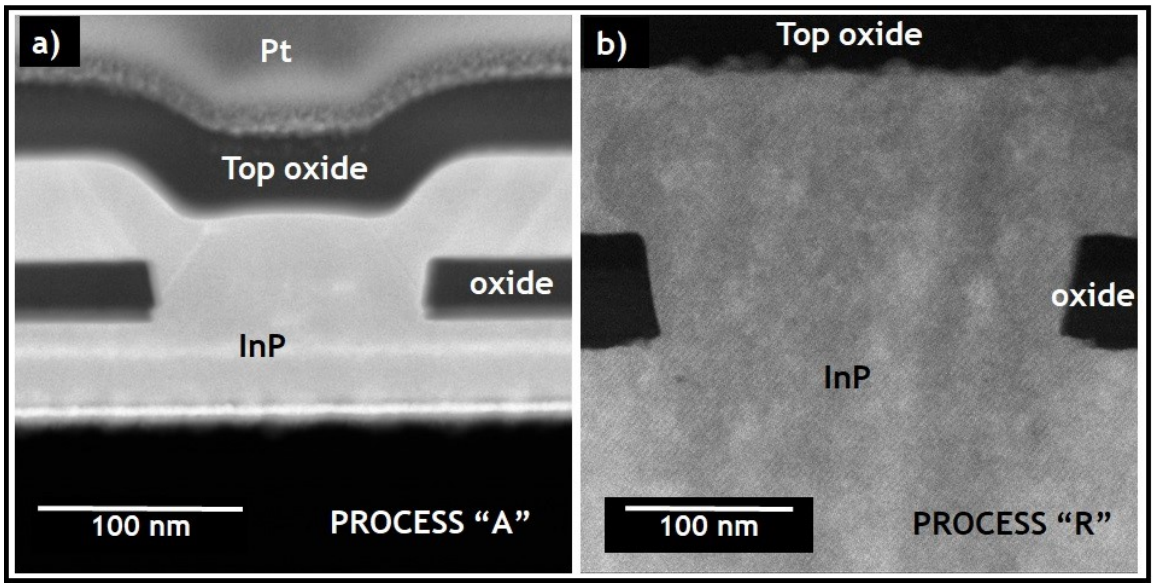

Figure 7.8 cross-sectional TEM of CELO cavities fabricated with a) a-Si sacrificial layer and PECVD SiO_x source layer b) resist sacrificial layer and HSQ source layer. Reprinted (adapted) with permission from [12]. Copyright (2019) American Chemical Society.

Specifically, the positive electron beam resist (EBR) CSAR-62 was used. However, because PECVD oxide is deposited at $T \geq 250°C$, a different top oxide should be used to prevent chamber contamination. For this process, CSAR is spun where $t_{resist} \approx 2 \bullet d_{oxide}$ to planarize over the growth windows [35]. The outline of CELO boxes were then patterned by EBL to reduce write time – a bright field UV lithography process could achieve the same affect.

3. Source Layer

The source layer defines the top and edges of the cavity while also defining the field dielectric. The growth selectivity of the sample is determined by the quality of the source layer. Because the sacrificial layer is islands on the substrate, the source layer deposition must be conformal to coat the exposed edges. Fortunately, PECVD SiO_x is conformal ($t_{sidewall} \approx 0.5 \bullet t_{field}$) and exhibits the best growth selectivity. The same etch used to define the growth window can be used to define the cavity opening, deemed the "source hole". Samples

fabricated this way are referred to as “type A”. This technique leaves a sidewall present that acts as a barrier to adatoms diffusing to the growth front, illustrated in **Figure 7.9**.

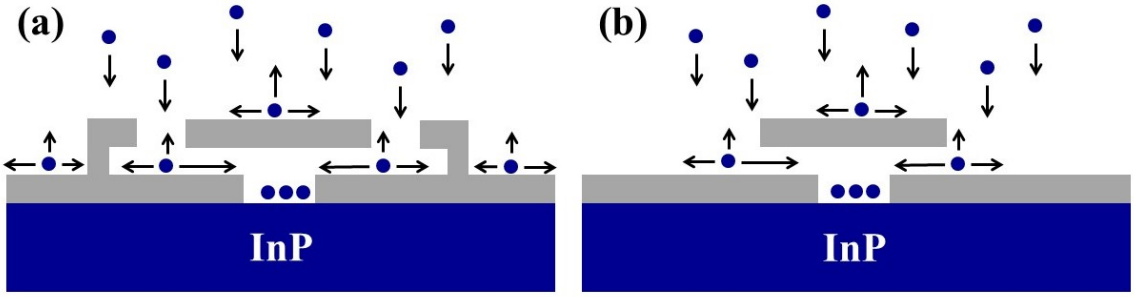

Figure 7.9 Illustration of adatom motion during growth for CELO structures fabricated using a) a-Si sacrificial layer and PECVD SiO_x source layer b) resist sacrificial layer and HSQ source layer

Samples using CSAR as the sacrificial layer used an HSQ top-oxide which allows the field to remain PECVD SiO_x, maintain high growth selectivity. Samples fabricated this way are referred to as “type R”. HSQ with $t_{HSQ} \approx 2 \bullet t_{CSAR}$ was then used to define the boxes. Patterning of HSQ over-doses the underlying CSAR enabling CSAR inside the cavities to be removed by a subsequent CSAR develop step. Additionally, HSQ develops in basic chemistry and CSAR develops in polar solvents thus development of HSQ leaves the CSAR “scaffolding” in-tact. Since the field is coated with un-exposed CSAR after the HSQ develop – a DUV flood exposure of 10 mins is used to expose the CSAR still present in the field. CSAR is DUV active, though it requires a very large dose, HSQ is not. To ensure cleanliness of the field and the cavities, the DUV flood exposure is followed by 30 minutes Amyl Acetate/30 minutes IPA/2 minutes DI rinse, 2 hours in NMP, and 3 minutes >350°C in remote oxygen plasma. Due to the elimination of two dry etch steps and the requirement of two overnight, wet resist strips, process time is reduced. While process time is reduced, EBL time and cost substantially increase as the top oxide “boxes” are now completely written in HSQ [high dose resist]. The

entire box structure (750 nm x 2.5 μm) must be defined in this step whereas the previously described process defines small holes (650 nm x 150 μm) in CSAR [low dose resist], resulting in significantly lower EBL exposure time. While increased EBL time is undesirable, an advantage of the resist process over the a-Si process is that the sidewall barrier present near the source-hole openings is removed, as illustrated in **Figure 7.9**. Removal of this barrier may facilitate easier diffusion to the growth front and increase growth rate.

HSQ is dissolved in MIBK which is a high-contrast developer of CSAR. When dispensing the HSQ on the CSAR, some intermixing likely occurs as the MIBK dissolves the CSAR. The intermixing creates roughness and porosity in the top oxide which is not observed in type A templates, shown in **Figure 7.8**.

C. Template Effects on Growth

Borg *et al.* originally reported on the mechanisms of growth for TASE nanowires, illustrated in **Figure 7.10** [14]. Because faceting is strongly dependent on V/III ratio, the resulting facets can be used to infer the effective V/III ratio inside the template. By adjusting growth time, the effective V/III ratio at a given *L* can be inferred and matched to various mass transport models. Small diameter nanotubes exhibited facets consistent with lower effective V/III ratio. Additionally, growth deep inside the nanotubes exhibited similar facets. As the growth front approaches the top of the nanotube or the diameter is increased, facets consistent with higher V/III ratio are observed.

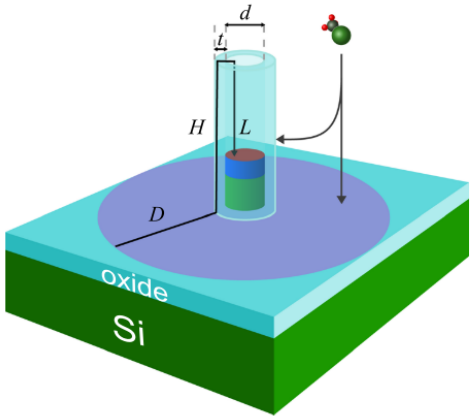

Figure 7.10 Illustration of TASE nanowire structure used in [14]. Reprinted from [14], with the permission of AIP Publishing.

Previous SAG reports found that lateral gas phase diffusion is the dominant material transport phenomenon [36]. Borg *et al*. found that this cannot be the case for TASE templates as pressure gradients are only present inside templates, as determined by finite element simulations. Instead a combination of Knudsen and surface diffusion was suggested.

Molecular transport in long tubes with aspect ratio > 6 is given by [37]:

$$\Phi_{Kn}^{i} = \hat{v}_i \frac{\Delta p_i}{3LRT} d \tag{7.3.1}$$

Where $\hat{v}_i$ is the mean molecular speed of species *i*, Δp_i is the partial pressure difference across the length, *L*, of the nanotube, *R* is the gas constant, and *T* is the temperature. For the surface diffusion model, the collection area determines the amount of material delivered to the growth front. The collection area is determined by the surface migration length (λ_i) of species *i*. The radial contribution of the precursor collection from the field oxide is given by:

$$D = \lambda_i - (H + t + L) \tag{7.3.2}$$

The molar flow per area by surface diffusion for a nanowire can be expressed as:

$$\Phi_{SD}^{i} = \frac{4 a_{ads} p_i}{RT} \left(\frac{A_0(\lambda_i)}{d^2} + \frac{\lambda_i}{d} \right) \tag{7.3.3}$$

$$A_0 = D^2 + 2(D + H)t + t^2 \tag{7.3.4}$$

Where a_{ads} is the adsorption rate and A_0 is the total collection area. While there is no pressure gradient outside of the template, a pressure gradient does exist inside. As a result, both p_i and a_{ads} decrease inside the template as the molecules traverse from opening to growth front. However, to determine geometric effects, it is simplest to assume these are constant.

A faster growth rate was observed for small diameter nanowires and facets consistent with lower V/III ratio. Knudsen diffusion alone cannot explain either of these effects. Because the surface migration length is uniform across the sample, growth rate enhancement is expected in smaller diameter nanotubes. Because no lateral partial pressure gradient exists, surface diffusion of the group III material can explain the observed growth rate enhancement. Assuming that the group V precursor is only transported by Knudsen diffusion while the group-III precursor is transported by both Knudsen and surface diffusion, the V/III ratio can be written:

$$V/III = \frac{\Phi_{Kn}^{V}}{\Phi_{Kn}^{III} + \Phi_{SD}^{III}} = \frac{\widehat{v_V}\Delta p_V}{\widehat{v_{III}}\Delta p_{III} + 12La_{ads}p_{III}\left(\frac{A_0(\lambda_{III})}{d^3} + \frac{\lambda_{III}}{d^2}\right)} \tag{7.3.5}$$

As d decreases, transport of the group III material increases due to surface diffusion and the effective V/III ratio deep inside the nanotube decreases. This model was found to be in good agreement with observed growth behavior in [14]. Additionally, with simple modifications to the geometry and Knudsen diffusion expression, this theory can be adapted to arbitrary geometries. In this section we aim to provide insight about growth in laterally oriented, rectangular TASE templates with t_{cavity} = 50 nm.

To investigate growth effects on templates described in the above sections, processed wafers were diced into 7 × 7 mm^2 samples, each containing four die and >1 mm of edge exclusion. Immediately prior to loading into the MOCVD chamber, samples were dipped in 0.3% HF for 10 seconds. MOCVD was done in a horizontal reactor using trimethylindium (TMIn), tertiary- butylphosphine (TBP), and H_2 as carrier gas. Various growth pressures, ranging from 50 Torr to 350 Torr, were explored in initial trials. Increased selectivity was observed with decreasing pressure. The best selectivity observed was with P = 50 Torr and T = 580 – 650°C. Lower pressures could exhibit further improved selectivity but are not realizable with the current tooling available at UCSB. The molar flow of TMIn was 1.3 x 10^{-6} mol/min for 500 seconds and then increased to 2.7 x 10^{-6} mol/min using V/III = 400. The high V/III ratio compared to those reported in [14] was chosen to promote the formation of (110) facets, necessary for devices reported in [21], while limiting effects of local variation in V/III.

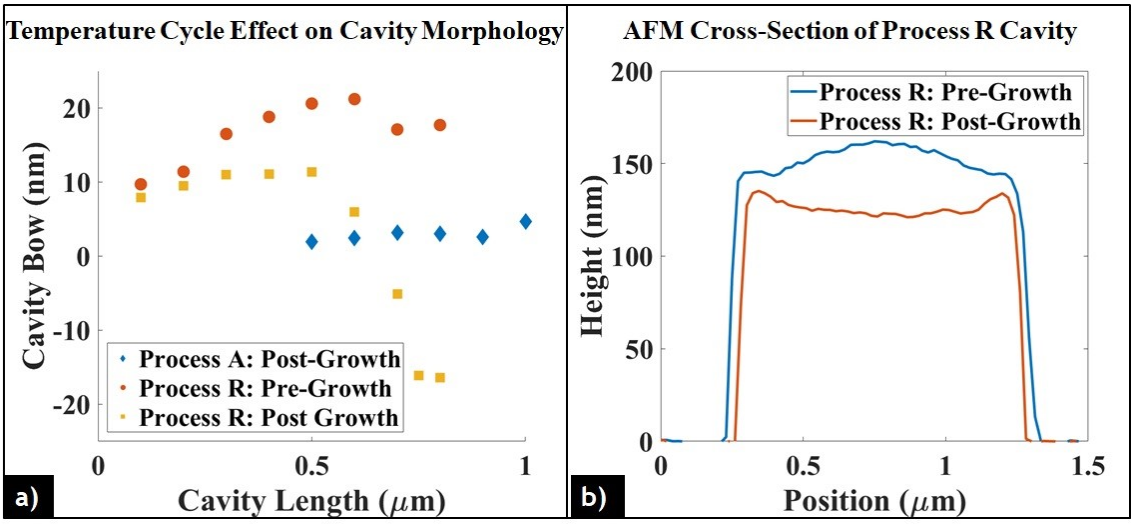

Figure 7.11 Cavity bowing of a) type A and R templates before and after growth b) cross-sectional profile for type R template as measured by AFM. Reprinted (adapted) with permission from [12]. Copyright (2019) American Chemical Society.

Growth of InP-based material by MOCVD is generally conducted at 480 – 650°C. Because the TASE cavity ceiling is free-standing and because of the thermal mismatch of the oxide mask and semiconductor, pattern distortion is possible during warmup and cooldown. **Figure 7.11** shows observed pattern bow prior to and after growth for type A and R templates. While type A templates exhibit minimal bowing, type R templates exhibit significant bowing both before and after growth – dependent on box width. The downward bowing observed post-growth results in a "pinched" cavity and reduced growth rate, likely due to constricted gas flow inside the template. The grown film was measured by removing the top oxide in BHF and found to have similar bow to the cavity suggesting that bowing occurs early in growth – likely during warm up. Curing of HSQ at 600°C induces a compressive stress of -100 MPa [38], less than the measured -250 MPa stress observed in PECVD deposited SiO_x. It is thus unlikely that stress in the source oxide is responsible for cavity collapse. It has also been reported that HSQ films shrink >20% for $T > 600$°C [38]. Additionally, when the cavity width exceeds 1 μm, type R cavities often become disconnected from the underlying substrate during HSQ development and CSAR removal. This suggests poor adhesion of HSQ to PECVD SiO_x or pronounced mid-range electron scattering effects common in both InP and HSQ. In conjunction with the reported thermal properties, it is likely that the observed bowing in type R templates is due to the expansion/contraction of HSQ on the oxide surface during growth. The resulting bowing pinches the cavity and reduces growth rate for templates with $W_{cavity} >$ 0.5 μm.

Type R cavities also exhibited improved growth selectivity when a pre-growth *in-situ* anneal was conducted: 350°C for 10 min in H_2, followed by 10 min at 660°C under both H_2 and TBP to avoid group V desorption from the InP surface. The poor initially observed

selectivity may be because of incomplete curing of the HSQ during exposure. It is possible that the pattern edges are not fully transformed into SiO_x and thus present either hydroxyl or residual organic groups that can behave as nucleation cites. The high temperature anneal in H_2 facilitates additional curing and organic removal, improving growth selectivity.

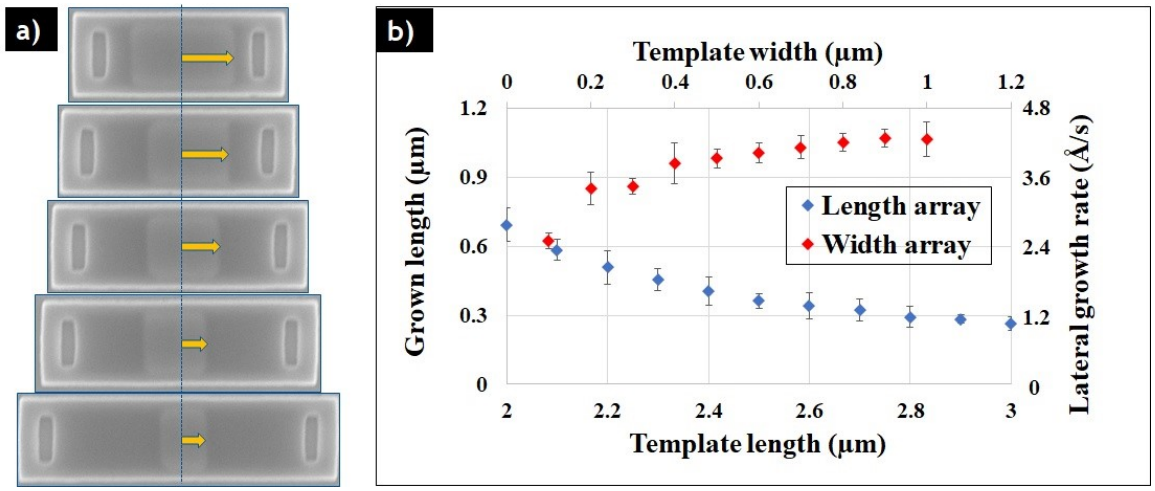

Figure 7.12 (a) top-down SEM images of template length array after growth (b) growth-rate as a function of template length (w = 0.35 µm, t = 50 nm) and width (L = 1.0 µm, t = 50 nm). Reprinted (adapted) with permission from [12]. Copyright (2019) American Chemical Society.

As referenced above, template geometry effects mass transport and thus effects growth rate and faceting. Template length was observed to effect growth length in both processes A and R templates. Templates of varying lengths (2 – 4 µm), corresponding to (1 – 2 µm) source-to-seed spacing on either side, were compared for structures with width and thickness fixed, shown in **Figure 7.12**. Growth rate was observed to decrease as the template length increased. This growth rate reduction can be intuitively explained by the increased length that precursors must traverse, measured from the source hole to the growth front, to initiate/continue growth. This is consistent with the growth mechanisms presented in [14]: as L increases Φ_{SD}^{III}, Φ_{Kn}^{III}, and Φ_{Kn}^{V} all decrease for a given source hole geometry.

Growth in templates of constant length but varying widths (150 – 550 nm) was also conducted and exhibited an increase in the growth rate with increasing template width, shown in **Figure 7.12**. While all other template parameters are kept constant, the width of the source hole and seed hole increase. This results in more material reaching the growth front and a wider growth interface.

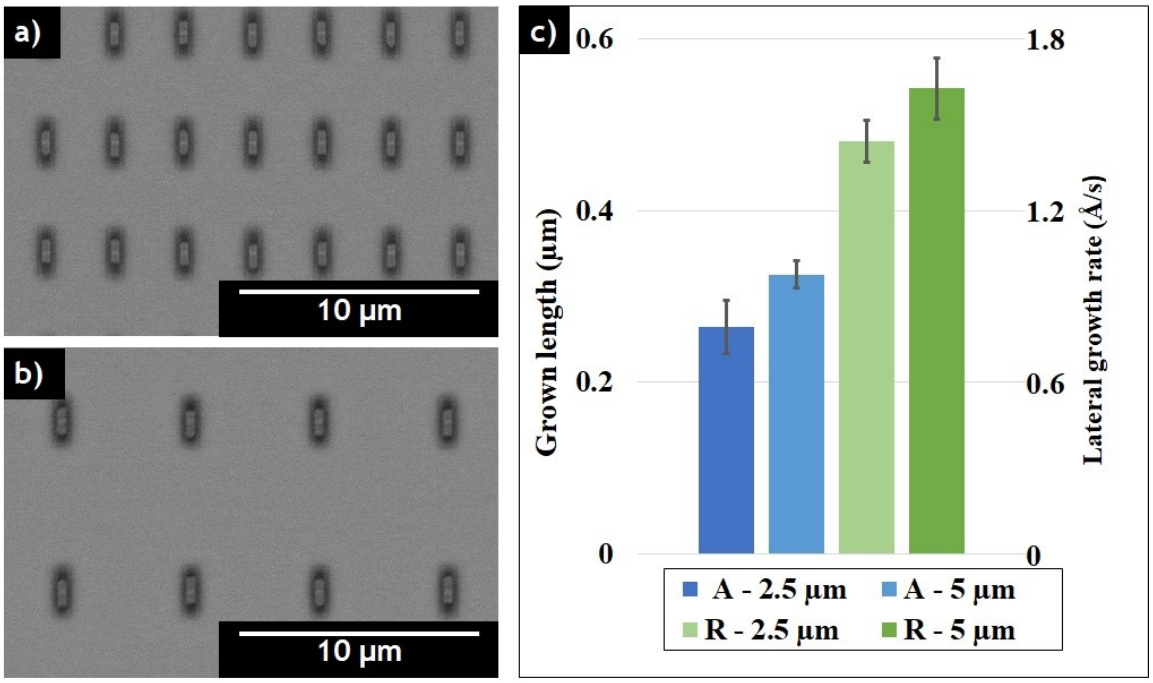

Figure 7.13 top-down SEM of multiple structures with a) 2.5 µm edge-to-edge spacing b) 5.0 µm edge-to-edge spacing c) average growth length and rate as function of edge-to-edge spacing for type A and R templates. Reprinted (adapted) with permission from [12]. Copyright (2019) American Chemical Society.

To investigate the effect of fill factor, identical templates spaced by 2.5 µm and 5 µm from template edge-to-edge, on the same die, were compared in the same growth. The growth rate decreases with increasing packing density. While this is expected due to loading effects typical in SAG, it is in contrast with the growth rate independence of packing density for TASE structures reported in [14]. This could be attributed to differences in geometry or to differences in packing density. While [14] investigated pattern spacings less than the mean free path of

adatoms, we report on spacings greater than the mean-free-path. Additionally, the lower sidewall height in this work, compared to tall nanowire templates in [14], may allow for lateral gas phase diffusion mechanisms to be noticeable or reduce the adatom total diffusion length necessary to reach the growth front at a given L.

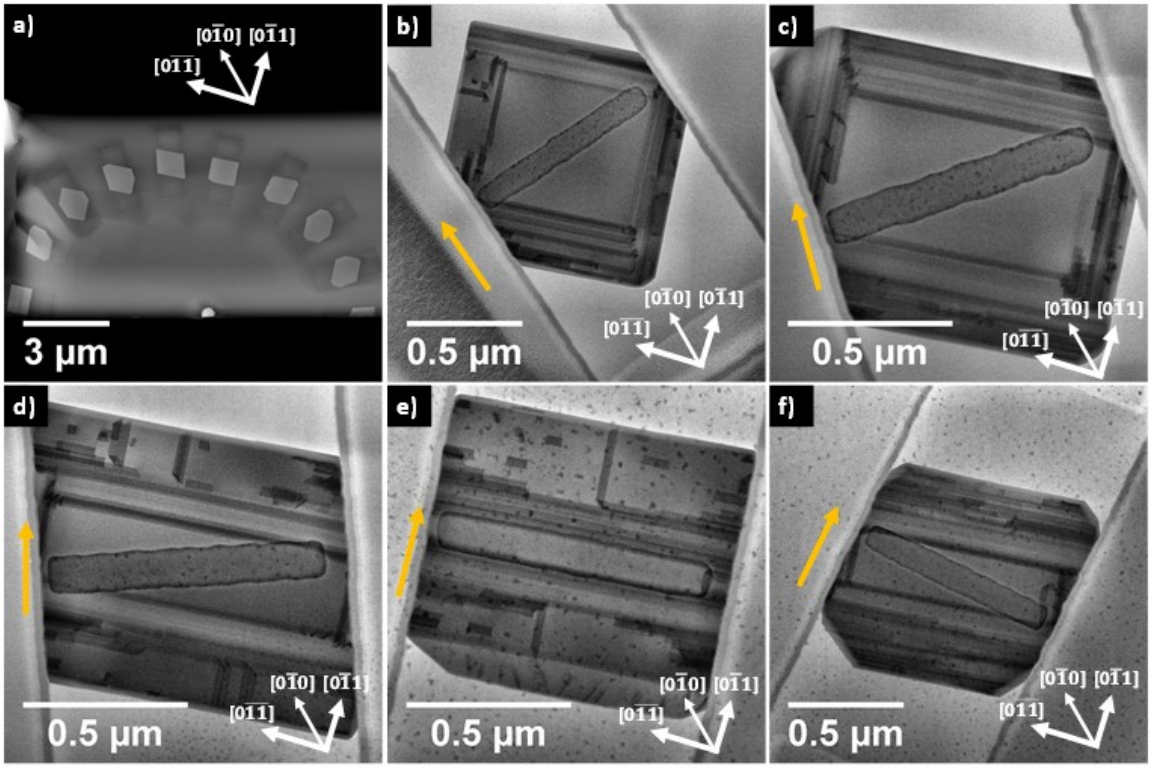

Figure 7.14 Plan view TEM micrographs analyzing growth in different orientations on a (100) InP substrate. (a) shows the HAADF-STEM of the entire lamella with a flower pattern of CELO templates starting from the one oriented along [110] and with separations of 22.5° between consecutive templates. (b)-(f) BF-STEM of individual templates oriented in different directions on the wafer. The nature and density of defects change as the orientations of the templates vary from [0$\bar{\mathbf{1}}\bar{\mathbf{1}}$] to [0$\bar{\mathbf{1}}$**1**]. The yellow arrows point to the direction the templates are oriented. Reprinted with permission from Aranya Goswami, paper submission [39].

Finally, imperfections in the template can translate to defects in the laterally overgrown film. Renard *et al*. reported that roughness in a dielectric template can cause bond distortions that result in the formation of stacking faults and twins in GaAs [40]. Because InP has the lowest stacking fault energy of common cubic III-V semiconductors [41], it is expected to be

extremely sensitive to surface roughness. Goswami *et al*. reported on defects in CELO grown InP and found a high rate of twins and stacking faults [39]. **Figure 7.14** shows plan-view TEM images of rotated CELO structures where various defect types and densities can be seen. Defects often nucleate and propagate from the dielectric sidewall. Interestingly, defects do not appear to be forming at the growth seed or in regions of bulk overgrowth suggesting that the ~1 – 2 nm roughness of the field dielectric is sufficient to suppress defects under these growth conditions. Defect nucleation on the dielectric sidewall could be because of residues on the inner surface from incomplete removal of the sacrificial layer or edge roughness due to the sacrificial dry etch. While the dry etch edge roughness are not known, type R templates should exhibit larger sidewall edge roughness due to HSQ/CSAR intermixing and should thus exhibit higher defect densities. This remains untested.

D. Conclusions

Homoepitaxy InP TASE has been demonstrated and basic template effects on growth have been explored. Increasing the template width and decreasing its length increases the growth rate at a given thickness. However, the maximum width is determined by the mechanical stability of the template. The minimum length is generally determined by the desired application. Higher packing densities lead to reduced growth rates due to increased fill-factors and higher pre-cursor consumption rate.

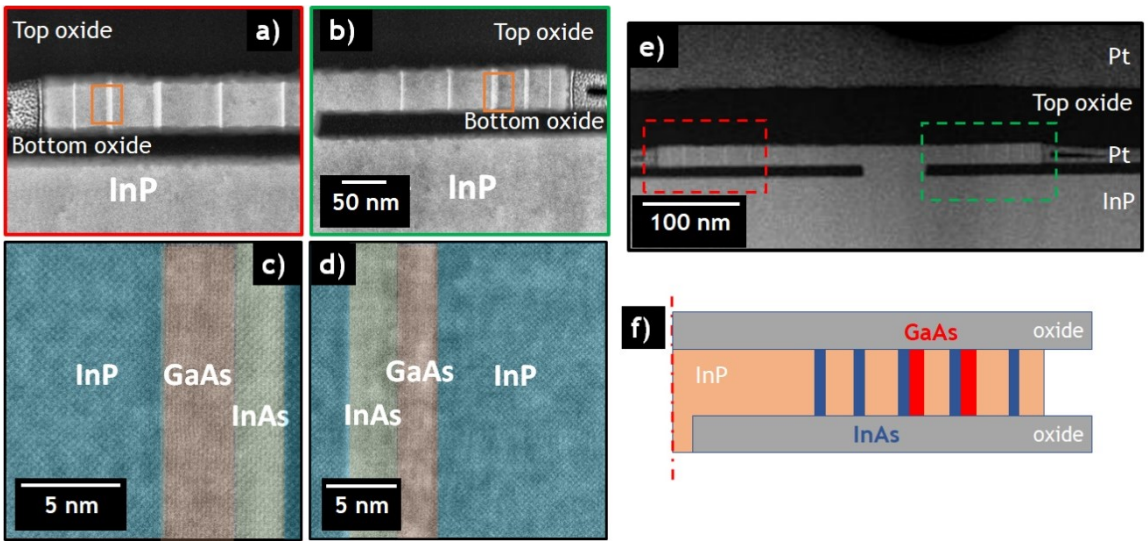

Figure 7.15 Cross-sectional TEM of 3HJ in type R template. Reprinted (adapted) with permission from [13]. Copyright (2019) American Chemical Society.

Detailed studies of growth parameters, heterojunction and ternary growth, and defect formation for InP TASE can be found in Simone Tommaso Šuran Brunelli and Aryana Goswami's theses. Importantly, though not detailed in this thesis, a laterally oriented, vertical 3HJ has been demonstrated and is illustrated in **Figure 7.15**. Achieving uniform, controllable growth free of parasitics remains difficult and prevented further investigation of devices based on TASE material.

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8. Conclusions

A. Summary

We have demonstrated the viability of the MOS-HEMT technology. World record $f_\tau = 511$ GHz for the MOS-HEMT has been demonstrated. **Figure 8.1** and **Table 8-1** show the highest reported figures-of-merit for InP-based HEMTs and illustrates that the InP MOS-HEMTs can be competitive with the SOA. Challenges with metal deposition usually resulted in large gate-resistance, severely limiting f_{max}. This can be simply fixed by adopting a pocket evaporator or using a multi-step evaporation. It can also be addressed, less simply but more scalable, by adopting an ALD gate-metal process. Due to the improved electrostatics, realized by replacing a 5 nm $In_{0.52}Al_{0.48}As$ gate insulator with 2 nm ZrO_2, larger f_{max} at a given f_τ should be possible with an improved gate-metal-process.

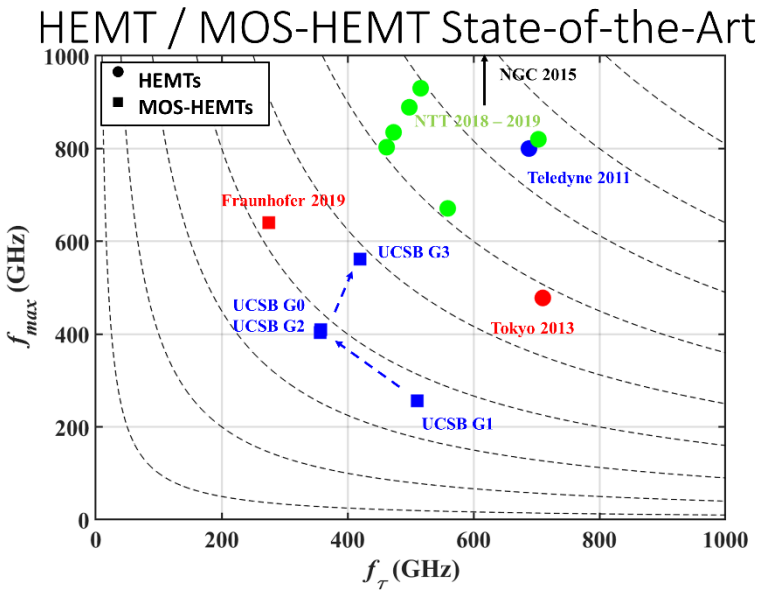


Figure 8.1 State of the art HEMTs and MOS-HEMTs also reported in Table 8-1

Specifically, transistors with t_{ch} = 6.5 nm exhibited peak f_τ = 511 GHz at L_g = 8 nm and peak f_{max} = 460 GHz at L_g = 90 nm. The devices were comprised of a 2 / 4 nm $In_{0.53}Ga_{0.47}As$ / InAs composite channel and a 1 / 3 nm $Al_xO_yN_z$ / ZrO_2 high-k gate dielectric. The back-barrier was $In_{0.52}Al_{0.48}As$ with 3.6 x 10^{12} cm^{-2} modulation doping located 3 nm from the bottom $In_{0.53}Ga_{0.47}As$ sub-channel. Extremely low gate-leakage current density of 5 x 10^{-8} $mA/\mu m^2$ was observed at ($V_{DS} - V_{GS}$) = 0.7 V and low DC / RF $g_{m,e}$ dispersion of 0.2 mS/µm exemplifies the superiority of the high-k gate-dielectric to standard $In_{0.52}Al_{0.48}As$. This result demonstrates that the MOS-HEMT technology is competitive with state-of-the-art HEMTs.

Removal of the wide bandgap, modulation doped link region beneath the highly doped, source-drain was demonstrated for an InP barrier device. Transistors with t_{ch} = 2.5 nm exhibited peak f_τ = 357 GHz and peak f_{max} = 403 GHz at L_g = 12 nm. The devices were comprised of a 2.5 nm $In_{0.53}Ga_{0.47}As$ channel and a 1 / 2 nm $Al_xO_yN_z$ / ZrO_2 high-k gate dielectric. The back-barrier was $In_{0.52}Al_{0.48}As$ with 3.6 x 10^{12} cm^{-2} modulation doping located 3 nm from the bottom $In_{0.53}Ga_{0.47}As$ sub-channel. Extremely low gate-leakage current density of 7 x 10^{-7} $mA/\mu m^2$ was observed at ($V_{DS} - V_{GS}$) = 0.7 V, suggesting that the high-k thickness can be further scaled. Larger dispersion is seen for Generation 2 devices (InGaAs channel) than is observed in Generation 1 devices (InAs channel), consistent with previously reported III-V MOS devices.

A L_g = 30 nm transistors with t_{ch} = 7.0 nm exhibited f_τ = 402 GHz and f_{max} = 560 GHz and a L_g = 40nm device exhibited f_τ = 420 GHz and f_{max} = 562 GHz. The devices were comprised of a 3 / 4 nm $In_{0.53}Ga_{0.47}As$ / InAs composite channel and a 1 / 2 nm $Al_xO_yN_z$ / ZrO_2 high-k gate dielectric. The back-barrier was $In_{0.52}Al_{0.48}As$ with 3.6 x 10^{12} cm^{-2} modulation doping located 3 nm from the bottom $In_{0.53}Ga_{0.47}As$ sub-channel. Extremely low gate-leakage current

density of 5 x 10^{-7} mA/μm^2 was observed at ($V_{DS} - V_{GS}$) = 0.7 V. Extremely high $C_{GS} \geq 0.80$ fF/μm and $C_{GD} \geq 0.25$ fF/μm limited the high-frequency performance despite excellent $g_{m,e}$ = 2.9 mS/μm and $g_{ds,e} \leq 0.25$ mS/μm. Moving to a self-aligned process is necessary to reduce parasitic C_{GS} and C_{GD}.

Table 8-1. State of the art high-frequency HEMTs and MOS-HEMTs

Institution	Process Type	g_m (mS/μm)	t_{ch} (nm)	t_{ins} (nm)	f_τ (GHz)	f_{max} (GHz)
Northrop [1]	HEMT	3.1	9.5	7.0 (?)	610	1500
NTT [2]	HEMT	2.8	9.0	5.0	703	820
Teledyne [3]	HEMT	2.75	10.0	4.0	688	800
Tokyo [4]	HEMT	2.1	5.0	4.0	710	478
UCSB [5]	MOS-HEMT	1.5	5.0	3.0	357	410
Fraunhofer [6]	MOS-HEMT	2.4	8.0	4.4	200	640
UCSB Gen. 1	MOS-HEMT	2.3	6.5	3.0	511	285
UCSB Gen. 2	MOS-HEMT	1.6	2.5	2.0	356	403
UCSB Gen. 3	MOS-HEMT	2.9	7.0	2.0	402	560

Ballistic FET theory was further developed without the bias constraints of VLSI. Optimal channel thickness for peak intrinsic transconductance of ≥7.0 nm was found to be in good agreement with previously reported devices. In contrast to previous reports, it is hypothesized that conduction-band-offset limits device performance not ballistic injection velocity. Additionally, inclusion of an $AlAs_{0.56}Sb_{0.44}$ back-barrier and use of an InP channel was proposed. While this may introduce further process difficulties, it promises to deliver larger intrinsic transconductance and increased breakdown voltage.

In addition to the RF MOS-HEMT work, a TASE process was developed for InP homoepitaxy and proof of concept demonstrated. Two separate processes were developed and

growth of InP, $In_xGa_{1-x}As$, strained GaAs, strained InAs, and the 3HJ were all demonstrated. Type A templates were found to be more mechanically stable but were susceptible to surface modification during the XeF_2 removal of amorphous-Si. Template geometry and packing density was found to effect growth rate while growth parameters and template orientation were found to effect facet formation. Further details regarding growth and defects in TASE InP-based materials can be found in the theses of Simone Tommaso Suran Brunelli and Aranya Goswami.

B. Future Work

Future transistors will require $In_{0.52}Al_{0.48}As$ link region top barriers to supply more charge to the channel at large ($V_{GS} - V_{TH}$). Due to the larger conduction-band-offset of $In_{0.53}Ga_{0.47}As$ | $In_{0.52}Al_{0.48}As$, removal of the link beneath the highly doped source-drain regions will be necessary. Additionally, when using $In_{0.52}Al_{0.48}As$ back-barriers, to prevent population of parallel 2DEG in the back-barrier, lighter modulation doping should be adopted. Any modulation doping removed from the back-barrier design must be compensated with additional modulation doping in the top barrier to prevent source-starvation. Ultimately, adopting wider bandgap back-barrier materials such as $AlAs_{0.56}Sb_{0.44}$ should enable the use of wider bandgap channel materials. Wider bandgap channels and back-barriers should facilitate higher breakdown voltages, lower off-current, and better electrostatics. Because $AlAs_{0.56}Sb_{0.44}$ cannot be highly doped, a composite structure like that used in [7] will need to be implemented, providing a lower limit to ($V_{GS} - V_{TH}$).

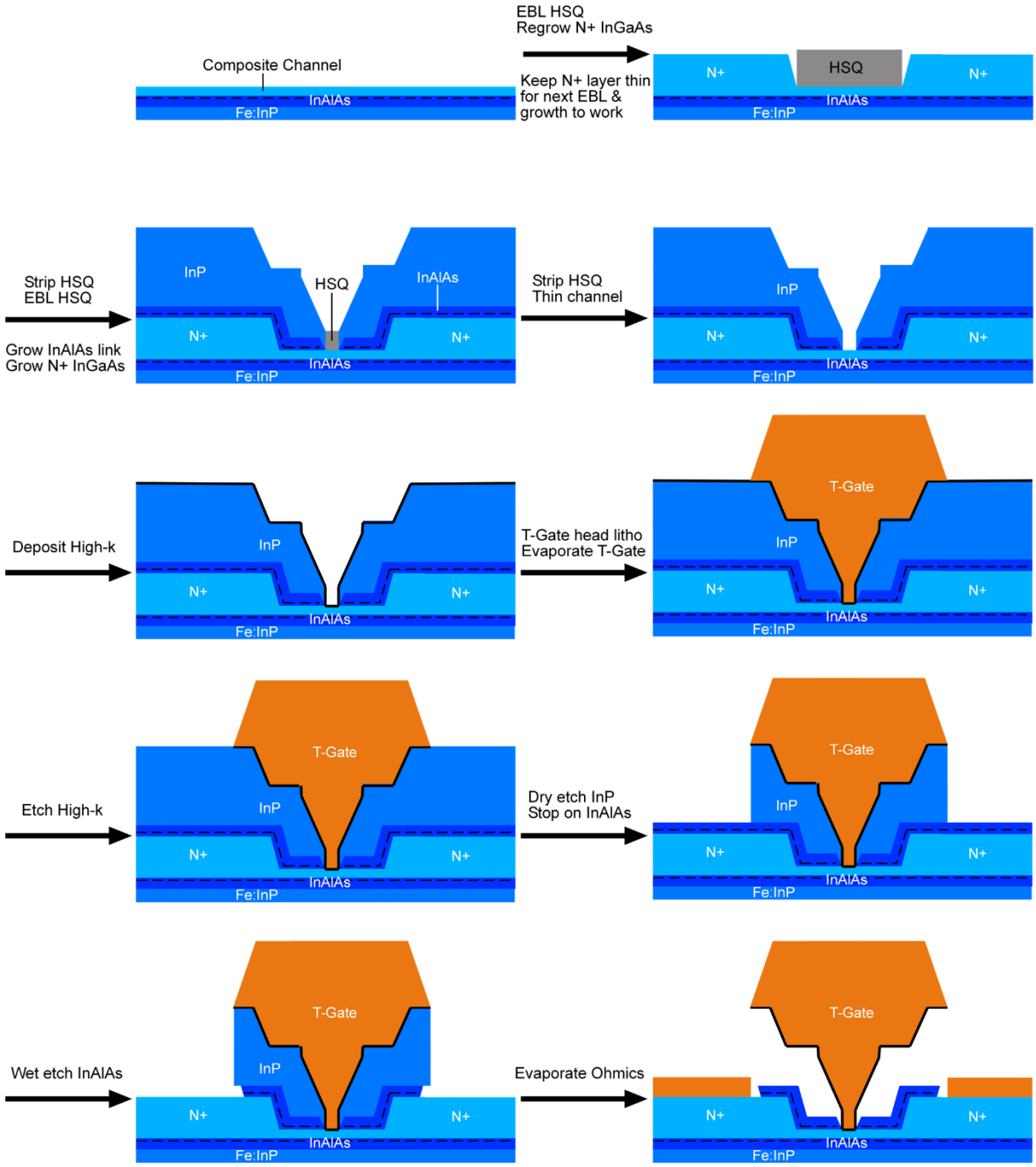


Figure 8.2 Proposed double regrowth with regrowth reversal and self-align T-Gate to gate-recess process

Due to the large observed parasitic components of C_{GS} and C_{GD} in conjunction with re-alignment challenges, a self-aligned process is necessary. Egard *et al*. published a self-aligned,

sacrificial regrowth process for RF III-V MOSFETs [8]. These devices, however, place the source and drain directly adjacent the gate edge, similar to most other III-V FET literature, resulting in a large parasitic C_{GS} and C_{GD}. We propose a similar regrowth reversal process such that the conductive quantum well can be included between the highly doped source and gate, shown in **Figure 8.2**. A non-self-aligned T-Gate, regrowth reversal process was attempted but not reported in this thesis. A cross-sectional TEM is shown in **Figure 8.3**. While it is unclear if the process can be made to work by this single attempt, it is clear by the asymmetry of the link regrowth, that the source-drain regrowth should be kept thin in order to facilitate mass transport into the gate recess during the link regrowth.

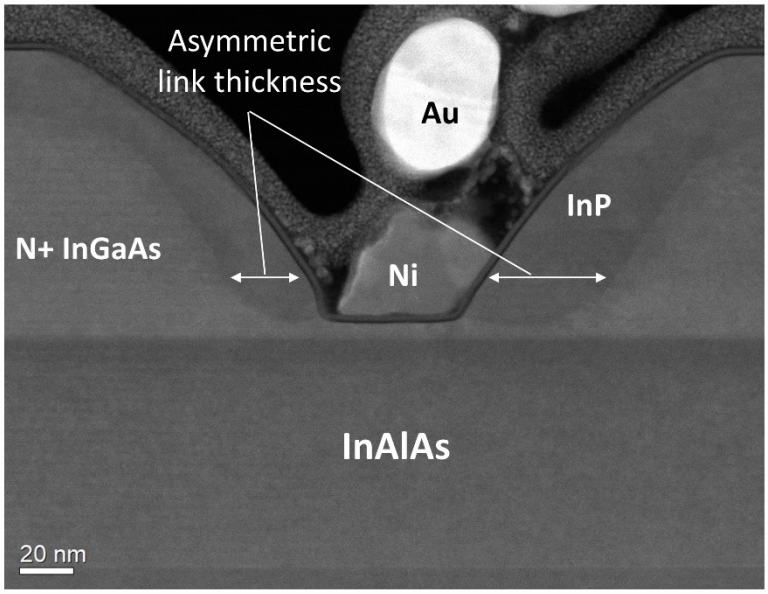
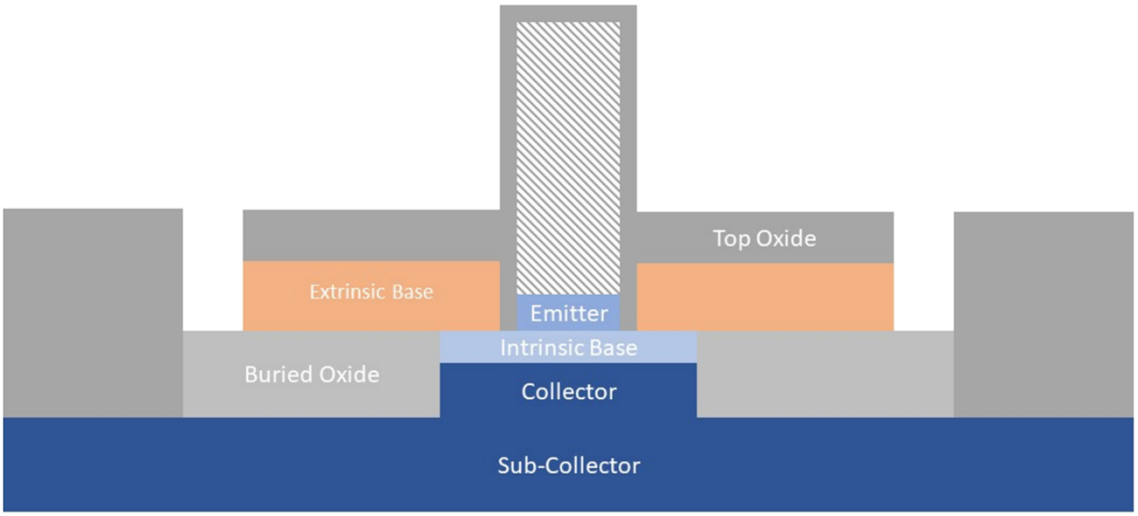


Figure 8.3 Cross-section TEM image of L_g = 40 nm device from process run Ch4-L1G2SD4 – an initial attempt at regrowth reversal using a non-self-aligned T-Gate

Proof of concept for TASE has been demonstrated but no device implementations, at UCSB, have been demonstrated. While the 3HJ necessary for the 3HJ-TFET was demonstrated, parasitic growth created additional challenges for device processing. Initial work on maskless cleaning technique has been discussed and demonstrated but improvements

need to be made before practical devices can be realized. Additionally, dopant incorporation needs to be studied and understood in-order to fabricate devices. In-order to demonstrate the broad usefulness of the technique, additional devices should be demonstrated leveraging TASE. For example, TASE can be utilized to regrow the extrinsic base contact region in a bipolar transistor, shown in **Figure 8.4**. The overgrown material need not be lattice matched to the intrinsic base, only highly doped, resulting in reduced R_{bb}. Because $\varepsilon_{ox} < \varepsilon_{semi}$, C_{cb} is simultaneously decreased facilitating improved f_{max}.



$$f_{\max} \cong \sqrt{f_\tau / 8\pi R_{bb} C_{cbi}}$$

Figure 8.4 Proposed regrown extrinsic base, buried oxide HBT leveraging TASE

While significant progress has been made on both fronts, there is much more to do. Both the MOS-HEMT and TASE involve complicated processing and growth and have many degrees of freedom. Experimental throughput is critical to further develop design principles for future device designers.

C. References

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Appendix 1 – Generation 1 Process

Start Date: 05/24/2019				Sample: Ch3-L1G2SD3	
Loop	Step #	Process Step	Equipment	Process	X
Epi	10.0	Measure Layer Thicknesses	J.A. Woolam	**1. Back Barrier: 80nm InAlAs / 20nm InP / 200nm InAlAs 2. Modulation Doping: 3nm InAlAs / 3nm 1x10^{19} cm^{-3} InAlAs 3. Channel: 4nm InAs / 2nm InGaAs 4. Cap: 5nm InGaAs**	
Alignment Mark Etch	20.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI rinse 60s	
	20.1	Hard Mask Deposition	Oxford-FlexAL ALD	TMA+H2O-300C for 50 cycles	
	20.2	**Measure Alumina Thicknesses**	**J.A. Woolam**	**Measure Al2O3 Thickness**	
	21.0	Solvent Clean	Solvent Bench	Acetone/IPA/DI	
	21.1	Dehydration	Hotplate	Bake 110°C for 5mins	
	21.2	Spin SPR 955-0.9	PR Bench	1) Dispense SPR 955-0.9, wait 30s 2) Spin 4000 RPMs for 30s	
	21.3	Pre-Bake	PR Bench	Bake 90°C for 90s	
	21.4	Expose Alignment Marks	GCA200	Mask = 0-RF-MARK, Job = RFMARK\MARK Focus-offset = 0, Exposure-time = 0.45 s	
	21.5	Post-Bake	PR Bench	Bake 110°C for 90s	
	21.6	Develop	Develop Bench	1) AZ300-MIF for 60s 2) DI Rinse 60s	
	21.7	Hard-Bake	PR Bench	Bake 120°C for 15mins	
	22.0	Etch Alignment Marks	Acid Bench	1. HF for 8s to remove 5nm Al2O3 2. H3PO4:H2O2:H2O 1:1:25 for 60s to remove channel + back barrier (1.33 nm/s) **Check to insure complete removal** 3. HCl:H2O 1:1 for 15s to etch InP (8 nm/s) **Check to insure complete removal** 4. H3PO4:H2O2:H2O 1:1:25 for 120s to back barrier (1.33 nm/s) **Check to insure complete removal** 5. HCl:H2O 1:1 for 2 mins to etch InP substrate (8nm/s)	
	22.1	Strip Resist	Isothermal Bath	1. NMP at 80°C for 2 hours 2. IPA/DI rinse	
	22.2	Remove Hard Mask	HF Bench	1. BHF for 2mins 2. DI rinse for 2mins	
	22.3	**Measure Layer Thicknesses**	**J.A. Woolam**	**Measure InGaAs cap thickness using same model from section 10**	
Link Region EBL + Regrowth	30.0	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s	
	30.1	Adhesion Layer Deposition	Oxford-FlexAL ALD	TMA+H2O-300C for 10 cycles	
	31.0	Spin 2% HSQ	PR Bench	1. Warm 2% HSQ to RT for 15mins 2. Dispense 2% HSQ, wait 30s 3. Spin 5000 RPMs for 30s	
	31.1	Pre-Bake	PR Bench	Bake 200°C for 120s	
	31.2	EBL Exposure	JEOL 6300	500 pA, Aperature 5, Dose 5000 uC/cm^2 Gain: x60/5/85/50/1320 Scan Parameters: 10scans/10kns/20um wide/15um position Recipe: 0725_Campaign7_DG1 (.sdf .jdf .mgn)	
	31.3	Develop	Develop Bench	1. NaOH:NaCl:H2O = 2g:8g:200mL for 60s (**DO NOT STIR**) 2. DI rinse for 10mins **(DO NOT STIR)** --> move to fresh DI twice (1min & 5min)	
	31.4	**Write Check**	**Optical Microscope**	**Check to see if dummy gates are visible, straight, and well adhered**	
	31.5	Dummy Gate Bake	PR Bench	Bake 150°C for 30mins to avoid HSQ outgas in MOCVD	
	31.6	**Measure Layer Thicknesses**	**J.A. Woolam**	**Measure InGaAs cap thickness using same model from section 10**	
	32.0	Digital Etch	UV Ozone Acid Bench	10min UV Ozone HCl:H2O 1:10 for 60s **(DO NOT STIR)**	
	32.1	**Measure Layer Thicknesses**	**J.A. Woolam**	**Measure InGaAs cap thickness using same model from section 10**	
	32.2	Link Region Regrowh	Thomas Swan MOCVD	1. 3nm UID-InP at 600°C 2. 2nm 1x10^19 cm^-13 Si:InP at 600°C 3. 15nm UID-InP at 600°C	
	32.3	**Measure Layer Thicknesses**	**J.A. Woolam**	**Measure regrown InP thicknes + channel cap thickness**	
	32.4	**Sheet Resistance Check**	**Four Point Probe**	**Measure link sheet resistance**	
	32.5	**Growth Check**	**Optical Microscope**	**Check to make sure growth is smooth no major impurities on wafer**	

S/D EBL + Regrowth	40.0	Remove HSQ Dummy Gate	HF Bench	1. BHF for 2mins 2. DI rinse for 2mins	
	40.1	Adhesion Layer Deposition	Oxford-FlexAL ALD	TMA+H2O-300C for 10 cycles	
	40.2	Spin 6% HSQ	PR Bench	1. Warm 6% HSQ to RT for 15mins 2. Dispense 6% HSQ, wait 30s 3. Spin 5000 RPMs for 30s	
	40.3	Pre-Bake	PR Bench	Bake 200°C for 120s	
	40.4	EBL Exposure	JEOL 6300	500 pA, Aperature 5, Dose 5000 uC/cm^2 Gain: x60/5/85/50/1320 Scan Parameters: 10scans/10kns/20um wide/15um position Recipe: 0726_Campaign7_DG2 (.sdf .jdf .mgn)	
	40.5	EBL Exposure	JEOL 6300	10 nA, Aperature 7, Dose 5000 uC/cm^2 Gain: x1/7/150/200/1710 Scan Parameters: 10scans/5kns/20um wide/15um position Recipe: 0726_Campaign7_DG2_UV (.sdf .jdf .mgn)	
	40.6	Develop	Develop Bench	1. NaOH:NaCl:H2O = 2g:8g:200mL for 60s (**DO NOT STIR**) 2. DI rinse for 5-10mins **(DO NOT STIR)**	
	40.7	**Write Check**	**Optical Microscope**	**Check to see if dummy gates are visible, straight, and well adhered**	
	40.8	Dummy Gate Bake	PR Bench	Bake 150°C for 30mins to avoid HSQ outgas in MOCVD	
	41.0	Digital Etch (x3)	UV Ozone Acid Bench	10min UV Ozone **(DO NOT STIR)** HCl:H2O 1:10 for 60s **(DO NOT STIR)**	
	41.1	**Measure Layer Thicknesses**	**J.A. Woolam**	**Measure InP link thickness**	
	42.0	S/D Regrowth	Thomas Swan MOCVD	1. 50nm 4x10^19 cm^-3 Si:InGaAs	
	42.1	**Growth Check**	**Optical Microscope**	**Check to make sure growth is smooth no major impurities on wafer**	
	42.2	**Thickness Check**	**J.A. Woolam**	**Measure S/D InGaAs thickness**	
	42.3	**Sheet Resistance Check**	**Four Point Probe**	**Sheet resistance 19Ω/□ for 80nm; 25Ω/□ for 50nm n++ InGaAs**	
Mesa Isolation	50.0	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s	
	50.1	Dehydration	PR Bench	Bake 110°C for 5mins	
	50.2	Spin SPR 955-0.9	PR Bench	1) Dispense SPR 955-0.9, wait 30s 2) Spin 4000 RPMs for 30s	
	50.3	Pre-Bake	PR Bench	Bake 90°C for 90s	
	50.4	Expose Alignment Marks	GCA200	Mask = 1-RF-ISO, Job = RFISO\ISO Focus-offset = 0, Exposure-time = 0.42 s	
	50.5	Post-Bake	PR Bench	Bake 110°C for 90s	
	50.6	Develop	Develop Bench	1) AZ300-MIF for 60s 2) DI Rinse 60s	
	51.0	Etch Mesa	Acid Bench	1. H3PO4:H2O2:H2O 1:1:25 for 90s to etch regrown S/D (1..33 nm/s) **Check to insure complete removal** 2. HCl:H2O 1:1 for 15s to etch InP link region(8 nm/s) **Check to insure complete removal** 3. H3PO4:H2O2:H2O 1:1:25 for 60s to remove channel + back barrier (1.33 nm/s) **Check to insure complete removal** 4. HCl:H2O 1:1 for 15s to etch InP etch stop layer (8 nm/s) **Check to insure complete removal**	
	51.1	Strip Resist	Isothermal Bath	1. NMP at 80°C for 2 hours 2. IPA/DI rinse	
	51.2	**Etch Check**	**DEKTAK/Bruker AFM**	**Check to make sure etched to InAlAs buffer**	
High-k	60.0	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s	
	60.1	Remove HSQ Dummy Gate	HF Bench	1. BHF for 2mins 2. DI rinse for 2mins	
	60.2	Digital Etch (x3)	UV Ozone Acid Bench	10min UV Ozone HCl:H2O 1:10 for 60s, DI rinse 60s	
	60.3	**Measure Layer Thicknesses**	**J.A. Woolam**	**Measure InGaAs S/D thickness to infer amount of channel removed**	
	60.4	Remove Native Oxide	HF Bench	BOE for 2mins, DI rinse 60s	
	60.5	High-k Deposition	Oxford-FlexAL ALD	1. Season/shake plasma shutter CH3-TMA+100W/N*-300C for 15 cycles 2. CH3-TMA+100W/N*-300C for 9 cycles 3. CH3-TEMAZ+H2O-300C for 40 cycles	
	60.6	Forming Gas Anneal	Rodwell Furnace	Recipe: Lee	
	60.7	**Measure High-k Thicknesses**	**J.A. Woolam**	**Measure High-k thickness Thickness**	

T-Gate	70.0	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s	
	70.1	Dehydration	PR Bench	Bake 110°C for 5mins	
	70.2	Spin CSAR:A 2:1	PR Bench	1) Surpass 4000 soak for 60 sec 2) DI rinse 30 sec 3) Spin 3000 RPM for 30 sec 4) Spin CSAR:A 2:1 5000 RPMs for 30 seconds (Recipe 8) 5) Bake 180°C for 5 mins	
	70.3	EBL Exposure	JEOL 6300	500 pA, Aperature 5, Dose 220 uC/cm^2 Gain: x60/5/85/50/1320 Scan Parameters: 10scans/10kns/15um wide/15um position Recipe: 0801_Campaign7_TGF (.sdf .jdf .mgn)	
	70.4	Develop	Solvent Bench	1) Amyl Acetate for 60s 2) IPA Rinse 20s	
	70.5	Spin UV-6	PR Bench	1) Spin 3000 RPMs for 30s 2) Bake 115C for 90s	
	70.6	EBL Exposure	JEOL 6300	500 pA, Aperature 5, Dose 100 uC/cm^2 Gain: x60/5/85/50/1320 Scan Parameters: 10scans/10kns/15um wide/15um position Recipe: 0801_Campaign7_TGH (.sdf .jdf .mgn)	
	70.7	Post-Bake	Solvent Bench	Bake 135°C for 2mins	
	70.8	Develop	Solvent Bench	1) AZ300-MIF for 60s (slow stir) 2) DI rinse 60s (water flush)	
	71.0	Gate Metal Deposition	Thermal Evaporator	Ni/Au 30nm/300nm Rates: 1.0/3.0 Å/s	
	71.1	PR Strip	Isothermal Bath	1. NMP at 80°C for 8+ hours 2. IPA/DI rinse	
	71.2	Post Metal Anneal	Oxford-FlexAL ALD	Bake in H2 at 350°C for 30mins	
	71.3	**Sheet Resistance Check**	**Four Point Probe**	**Check Gate Metal Sheet Resistance**	
	71.4	**Check Gate Metal**	**JEOL SEM**	**Check for T-Gate collapse and alignment**	
S/D Via Opening	80.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI rinse 60s	
	80.1	Dehydration	PR Bench	Bake 110°C for 5mins	
	80.2	Spin 100% CSAR x2	PR Bench	1) Surpass 4000 soak for 60 sec 2) DI rinse 30 sec 3) Spin 3000 RPM for 40 sec 4) Spin 100% CSAR 3000 RPMs for 30 seconds (Recipe 5) 5) Bake 180°C for 5 mins	
	80.3	EBL Exposure	JEOL 6300	2 nA, Aperature 6, Dose 230 uC/cm^2 Gain: x1/8/245/3/2077 Scan Parameters: 30scans/5kns/15um wide/15um position Recipe: 0802_Campaign7_SDV (.sdf .jdf .mgn)	
	80.4	Develop	Solvent Bench	1) Amyl Acetate for 60 seconds 2) IPA rinse for 20 seconds	
	81.0	Open S/D Vias	HF Bench	1. BHF for 45s (DO NOT STIR) 2. DI rinse for 2mins (DO NOT STIR)	
	81.1	PR Strip	Isothermal Bath	1. NMP at 80°C for 2 hours 2. IPA/DI rinse	
S/D Metal	90.0	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s	
	90.1	Dehydration	PR Bench	Bake 110°C for 5mins	
	90.2	Spin nLoff-5510	PR Bench	1) Dispense HMDS, wait 20s 2) Spin HMDS 4000 RPMs for 30 seconds (Recipe 7) 3) Dispense nLoff-5510, wait 30s 4) Spin 2500 RPMs for 30s (Recipe 4)	
	90.3	Pre-Bake	PR Bench	Bake 90°C for 60s	
	90.4	Expose S/D Metal	GCA200	Mask = 1-RFSD-INTER, Job = RFSD\SD Focus-offset = 0, Exposure-time = 0.42 s	
	90.5	Post-Bake	PR Bench	Bake 110°C for 90s	
	90.6	Develop	Develop Bench	1) AZ300-MIF for 60s 2) DI Rinse 60s	
	90.7	Hard-Bake	Solvent Bench	Bake 120°C for 15mins	
	90.8	Native Oxide Removal	Acid Bench	1) HCl:H2O 1:10 for 60s 2) DI rinse for 60s	
	91.0	S/D Metal Deposition	E-Beam #4	Ti/Pd/Au 20/20/300nm Rates: 0.7/1.2/3.0 Å/s	
	91.1	PR Strip	Isothermal Bath	1. NMP at 80°C for 2 hours 2. IPA/DI rinse	
	91.2	**Sheet Resistance Check**	**Four Point Probe**	**Check S/D Metal Sheet Resistance**	
	91.2	**Check S/D metal & recess**	**JEOL SEM**	**Check S/D recess etches and S/D metal quality/alignment**	
	91.3	**Check Gate Lengths**	**JEOL SEM**	**Measure all gate lengths on die without gate metal**	

Appendix 2 – Generation 2 Process

Start Date: 09/25/2019				Sample: Ch4-L2G2SD5	
Loop	Step #	Process Step	Equipment	Process	X
Epi	10.0	Measure Layer Thicknesses	J.A. Woolam	**1. Back Barrier: 80nm InAlAs / 20nm InP / 200nm InAlAs** **2. Modulation Doping: 3nm InAlAs / 3nm 1x10^{19} cm^{-3} InAlAs** **3. Channel: 4nm InAs / 2nm InGaAs** **4. Cap: 5nm InGaAs**	
Alignment Mark Etch	20.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI rinse 60s	
	20.1	Hard Mask Deposition	Oxford-FlexAL ALD	TMA+H2O-300C for 50 cycles	
	20.2	**Measure Alumina Thicknesses**	**J.A. Woolam**	**Measure Al2O3 Thickness**	
	21.0	Solvent Clean	Solvent Bench	Acetone/IPA/DI	
	21.1	Dehydration	Hotplate	Bake 110°C for 5mins	
	21.2	Spin SPR 955-0.9	PR Bench	1) Dispense SPR 955-0.9, wait 30s 2) Spin 4000 RPMs for 30s	
	21.3	Pre-Bake	PR Bench	Bake 90°C for 90s	
	21.4	Expose Alignment Marks	GCA200	Mask = 00-RFMARK, Job = RFMARK\MARK Focus-offset = 0, Exposure-time = 0.45 s	
	21.5	Post-Bake	PR Bench	Bake 110°C for 90s	
	21.6	Develop	Develop Bench	1) AZ300-MIF for 60s 2) DI Rinse 60s	
	21.7	Hard-Bake	PR Bench	Bake 120°C for 15mins	
	22.0	Etch Alignment Marks	Acid Bench	1. HF for 8s to remove 5nm Al2O3 2. H3PO4:H2O2:H2O 1:1:25 for 60s to remove channel + back barrier (1.33 nm/s) **Check to insure complete removal** 3. HCl:H2O 1:1 for 10s to etch InP (8 nm/s) **Check to insure complete removal** 4. H3PO4:H2O2:H2O 1:1:25 for 120s to back barrier (1.33 nm/s) **Check to insure complete removal** 5. HCl:H2O 1:1 for 2 mins to etch InP substrate (8nm/s)	
	22.1	Strip Resist	Isothermal Bath	1. NMP at 80°C for 2 hours 2. IPA/DI rinse	
	22.2	Remove Hard Mask	HF Bench	1. BHF for 2mins 2. DI rinse for 2mins	
	22.3	**Measure Layer Thicknesses**	**J.A. Woolam**	**Measure InGaAs cap thickness using same model from section 10**	
Link Region EBL + Regrowth	30.0	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s	
	30.1	Adhesion Layer Deposition	Oxford-FlexAL ALD	TMA+H2O-300C for 10 cycles	
	30.2	Spin 2% HSQ	PR Bench	1. Warm 2% HSQ to RT for 15mins 2. Dispense 2% HSQ, wait 30s 3. Spin 5000 RPMs for 30s	
	30.3	Pre-Bake	PR Bench	Bake 200°C for 120s	
	30.4	EBL Exposure	JEOL 6300	500 pA, Aperature 5, Dose 5000 uC/cm^2 Gain: x60/5/85/50/1320 Scan Parameters: 10scans/10kns/20um wide/15um position Recipe: 0927_Campaign9_DG1 (.sdf .jdf .mgn)	
	30.5	Develop	Develop Bench	1. NaOH:NaCl:H2O = 2g:8g:200mL for 60s (**DO NOT STIR**) 2. DI rinse for 10mins **(DO NOT STIR)** --> move to fresh DI twice (1min & 5min)	
	30.6	**Write Check**	**Optical Microscope**	**Check to see if dummy gates are visible, straight, and well adhered**	
	30.7	Dummy Gate Bake	PR Bench	Bake 150°C for 30mins to avoid HSQ outgas in MOCVD	
	30.8	**Measure Layer Thicknesses**	**J.A. Woolam**	**Measure InGaAs cap thickness using same model from section 10**	
	31.0	Digital Etch (x1)	UV Ozone Acid Bench	10min UV Ozone HCl:H2O 1:10 for 60s **(DO NOT STIR)**	
	31.1	**Measure Layer Thicknesses**	**J.A. Woolam**	**Measure InGaAs cap thickness using same model from section 10**	
	32.0	Link Region Regrowh	Thomas Swan MOCVD	1. 3.0nm UID-InP at 600°C 2. 2.0nm 1.1x10^19 cm^-13 Si:InP at 600°C 3. 15nm UID-InP at 600°C 3. 2.0nm UID-InGaAs at 600°C	
	32.1	**Measure Layer Thicknesses**	**J.A. Woolam**	**Measure regrown InP thicknes + channel cap thickness**	
	32.2	**Sheet Resistance Check**	**Four Point Probe**	**Measure link sheet resistance**	
	32.3	**Growth Check**	**Optical Microscope**	**Check to make sure growth is smooth no major impurities on wafer**	

S/D EBL + Regrowth	40.0	Remove HSQ Dummy Gate	HF Bench	1. BHF for 2mins 2. DI rinse for 2mins	
	40.1	Adhesion Layer Deposition	Oxford-FlexAL ALD	TMA+H2O-300C for 10 cycles	
	40.2	Spin 6% HSQ	PR Bench	1. Warm 6% HSQ to RT for 15mins 2. Dispense 6% HSQ, wait 30s 3. Spin 5000 RPMs for 30s	
	40.3	Pre-Bake	PR Bench	Bake 200°C for 120s	
	40.4	EBL Exposure	JEOL 6300	500 pA, Aperature 5, Dose 5000 uC/cm^2 Gain: x60/5/85/50/1320 Scan Parameters: 10scans/10kns/20um wide/15um position Recipe: 0930_Campaign9_DG2 (.sdf .jdf .mgn)	
	40.5	EBL Exposure	JEOL 6300	10 nA, Aperature 7, Dose 5000 uC/cm^2 Gain: x1/7/150/200/1710 Scan Parameters: 10scans/5kns/20um wide/15um position Recipe: 0930_Campaign9_DG2_UV (.sdf .jdf .mgn)	
	40.6	Develop	Develop Bench	1. NaOH:NaCl:H2O = 2g:8g:200mL for 60s (**DO NOT STIR**) 2. DI rinse for 5-10mins **(DO NOT STIR)**	
	40.7	**Write Check**	**Optical Microscope**	**Check to see if dummy gates are visible, straight, and well adhered**	
	40.8	Dummy Gate Bake	PR Bench	Bake 150°C for 30mins to avoid HSQ outgas in MOCVD	
	40.9	**Measure Layer Thicknesses**	**J.A. Woolam**	**Measure InP link thickness**	
	41.0	Digital Etch (x40)	UV Ozone Acid Bench	10min UV Ozone **(DO NOT STIR)** HCl:H2O 1:10 for 60s **(DO NOT STIR)**	
	41.1	**Measure Layer Thicknesses**	**J.A. Woolam**	**Measure InP link thickness**	
	42.0	S/D Regrowth	Thomas Swan MOCVD	1. 50nm 4x10^19 cm^-3 Si:InGaAs	
	42.1	**Growth Check**	**Optical Microscope**	**Check to make sure growth is smooth no major impurities on wafer**	
	42.2	**Thickness Check**	**J.A. Woolam**	**Measure S/D InGaAs thickness**	
	42.3	**Sheet Resistance Check**	**Four Point Probe**	**Sheet resistance 19Ω/□ for 80nm; 25Ω/□ for 50nm n++ InGaAs**	
Mesa Isolation	50.0	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s	
	50.1	Dehydration	PR Bench	Bake 110°C for 5mins	
	50.2	Spin SPR 955-1.8	PR Bench	1) Dispense SPR 955-1.8, wait 30s 2) Spin 3000 RPMs for 30s	
	50.3	Pre-Bake	PR Bench	Bake 90°C for 90s	
	50.4	Expose Alignment Marks	GCA200	Mask = 1-RF-ISO, Job = RFISO\ISO Focus-offset = 0, Exposure-time = 0.42 s	
	50.5	Post-Bake	PR Bench	Bake 110°C for 90s	
	50.6	Develop	Develop Bench	1) AZ300-MIF for 60s 2) DI Rinse 60s	
	51.0	Etch Mesa	Acid Bench	1. H3PO4:H2O2:H2O 1:1:25 for 90s to etch regrown S/D (1..33 nm/s) **Check to insure complete removal** 2. H3PO4:H2O2:H2O 1:1:25 for 30s to remove channel + back barrier (1.33 nm/s) **Check to insure complete removal** 3. HCl:H2O 1:1 for 15s to etch InP etch stop layer (8 nm/s) **Check to insure complete removal**	
	51.1	Strip Resist	Isothermal Bath	1. NMP at 80°C for 2 hours 2. IPA/DI rinse	
	51.2	**Etch Check**	**DEKTAK/Bruker AFM**	**Check to make sure etched to InAlAs buffer**	
High-k	60.0	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s	
	60.1	Remove HSQ Dummy Gate	HF Bench	1. BHF for 2mins 2. DI rinse for 2mins	
	60.2	Digital Etch (x5)	UV Ozone Acid Bench	10min UV Ozone HCl:H2O 1:10 for 60s, DI rinse 60s	
	60.3	**Measure Layer Thicknesses**	**J.A. Woolam**	**Measure InGaAs S/D thickness to infer amount of channel removed**	
	60.4	Remove Native Oxide	HF Bench	BOE for 2mins, DI rinse 60s	
	60.5	High-k Deposition	Oxford-FlexAL ALD	1. Season/shake plasma shutter CH3-TMA+100W/N*-300C for 15 cycles 2. CH3-TMA+100W/N*-300C for 9 cycles 3. CH3-TEMAZ+H2O-300C for 30 cycles	
	60.6	Forming Gas Anneal	Rodwell Furnace	Recipe: Lee	
	60.7	**Measure High-k Thicknesses**	**J.A. Woolam**	**Measure High-k thickness Thickness**	

T-Gate	70.0	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s	
	70.1	Dehydration	PR Bench	Bake 110°C for 5mins	
	70.2	Spin CSAR:A 2:1	PR Bench	1) Surpass 4000 soak for 60 sec 2) DI rinse 30 sec 3) Spin 3000 RPM for 30 sec 4) Spin CSAR:A 2:1 6000 RPMs for 30 seconds (Recipe 8) 5) Bake 180°C for 5 mins	
	70.3	EBL Exposure	JEOL 6300	500 pA, Aperature 5, Dose 220 uC/cm^2 Gain: x60/5/85/50/1320 Scan Parameters: 10scans/10kns/15um wide/15um position Recipe: 1004_Campaign9_TGF (.sdf .jdf .mgn)	
	70.4	Develop	Solvent Bench	1) Amyl Acetate for 60s 2) IPA Rinse 20s	
	70.5	Spin UV-6	PR Bench	1) Spin 3000 RPMs for 30s 2) Bake 115C for 90s	
	70.6	EBL Exposure	JEOL 6300	500 pA, Aperature 5, Dose 100 uC/cm^2 Gain: x60/5/85/50/1320 Scan Parameters: 10scans/10kns/15um wide/15um position Recipe: 1004_Campaign9_TGH (.sdf .jdf .mgn)	
	70.7	Post-Bake	Solvent Bench	Bake 135°C for 2mins	
	70.8	Develop	Solvent Bench	1) AZ300-MIF for 60s (slow stir) 2) DI rinse 60s (water flush)	
	71.0	Gate Metal Deposition	Thermal Evaporator	Ni/Au 30nm/300nm Rates: 1.0/3.0 Å/s	
	71.1	PR Strip	Isothermal Bath	1. NMP at 80°C for 8+ hours 2. IPA/DI rinse	
	71.2	Post Metal Anneal	Oxford-FlexAL ALD	Bake in H2 at 350°C for 30mins	
	71.3	**Sheet Resistance Check**	**Four Point Probe**	**Check Gate Metal Sheet Resistance**	
	71.4	**Check Gate Metal**	**JEOL SEM**	**Check for T-Gate collapse and alignment**	
S/D Via Opening	80.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI rinse 60s	
	80.1	Dehydration	PR Bench	Bake 110°C for 5mins	
	80.2	Spin 100% CSAR x2	PR Bench	1) Surpass 4000 soak for 60 sec 2) DI rinse 30 sec 3) Spin 3000 RPM for 40 sec 4) Spin 100% CSAR 3000 RPMs for 30 seconds (Recipe 5) 5) Bake 180°C for 5 mins	
	80.3	EBL Exposure	JEOL 6300	2 nA, Aperature 6, Dose 230 uC/cm^2 Gain: x1/8/245/3/2077 Scan Parameters: 30scans/5kns/15um wide/15um position Recipe: 1007_Campaign9_SDV (.sdf .jdf .mgn)	
	80.4	Develop	Solvent Bench	1) Amyl Acetate for 75 seconds 2) IPA rinse for 20 seconds	
	81.0	Open S/D Vias	HF Bench	1. BHF for 45s (DO NOT STIR) 2. DI rinse for 2mins (DO NOT STIR)	
	81.1	PR Strip	Isothermal Bath	1. NMP at 80°C for 2 hours 2. IPA/DI rinse	
S/D Metal	90.0	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s	
	90.1	Dehydration	PR Bench	Bake 110°C for 5mins	
	90.2	Spin nLoff-5510	PR Bench	1) Dispense HMDS, wait 20s 2) Spin HMDS 4000 RPMs for 30 seconds (Recipe 7) 3) Dispense nLoff-5510, wait 30s 4) Spin 2500 RPMs for 30s (Recipe 4)	
	90.3	Pre-Bake	PR Bench	Bake 90°C for 60s	
	90.4	Expose S/D Metal	GCA200	Mask = 1-RFSD-INTER, Job = RFSD\SD Focus-offset = 0, Exposure-time = 0.44 s	
	90.5	Post-Bake	PR Bench	Bake 110°C for 90s	
	90.6	Develop	Develop Bench	1) AZ300-MIF for 60s 2) DI Rinse 60s	
	90.7	Hard-Bake	Solvent Bench	Bake 120°C for 15mins	
	90.8	Native Oxide Removal	Acid Bench	1) HCl:H2O 1:10 for 60s 2) DI rinse for 60s	
	91.0	S/D Metal Deposition	E-Beam #4	Ti/Pd/Au 20/20/300nm Rates: 0.7/1.2/3.0 Å/s	
	91.1	PR Strip	Isothermal Bath	1. NMP at 80°C for 2 hours 2. IPA/DI rinse	
	91.2	**Sheet Resistance Check**	**Four Point Probe**	**Check S/D Metal Sheet Resistance**	
	91.2	**Check S/D metal & recess**	**JEOL SEM**	**Check S/D recess etches and S/D metal quality/alignment**	
	91.3	**Check Gate Lengths**	**JEOL SEM**	**Measure all gate lengths on die without gate metal**	

Appendix 3 – Generation 3 Process

Start Date:				Sample: Ch7-L6G3SD8 Regrowths
Loop	Step #	Process Step	Equipment	Process
Epi	10.0	Measure Layer Thicknesses	J.A. Woolam	1. Back Barrier: 100nm InAlAs 2. Modulation Doping: 3nm InAlAs / 3nm 1.2x10^{19} cm^{-3} InAlAs 3. Channel: 4nm InAs / 3nm InGaAs 4. Cap: 6nm InGaAs
Alignment Mark Etch	20.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI rinse 60s
	20.1	Hard Mask Deposition	Oxford-FlexAL ALD	TMA+H2O-300C for 50 cycles
	20.2	Measure Alumina Thicknesses	J.A. Woolam	Measure Al2O3 Thickness
	21.0	Solvent Clean	Solvent Bench	Acetone/IPA/DI
	21.1	Dehydration	Hotplate	Bake 110°C for 5mins
	21.2	Spin SPR 955-0.9	PR Bench	1) Dispense SPR 955-0.9, wait 30s 2) Spin 4000 RPMs for 30s
	21.3	Pre-Bake	PR Bench	Bake 90°C for 90s
	21.4	Expose Alignment Marks	GCA200	Mask = 0-FET-ALIGN, Job = RFMARK\MARK Focus-offset = 0, Exposure-time = 0.50s
	21.5	Post-Bake	PR Bench	Bake 110°C for 90s
	21.6	Develop	Develop Bench	1) AZ300-MIF for 60s 2) DI Rinse 60s
	21.7	Hard-Bake	PR Bench	Bake 120°C for 15mins
	22.0	Etch Alignment Marks	Acid Bench	1. HF for 8s to remove 5nm Al2O3 2. H3PO4:H2O2:H2O 1:1:25 for 90s to remove channel + back barrier (2.77 nm/s) Check to insure complete removal 3. HCl:H2O 1:1 for 2 mins to etch InP substrate (8nm/s)
	22.1	Strip Resist	Isothermal Bath	1. NMP at 80°C for 1 hour 2. IPA/DI rinse
	22.2	Remove Hard Mask	HF Bench	1. BHF for 2mins 2. DI rinse for 2mins
	22.3	Measure Layer Thicknesses	J.A. Woolam	Measure InGaAs cap thickness using same model from section 10
Link Region EBL + Regrowth	30.0	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
	30.1	Adhesion Layer Deposition	Oxford-FlexAL ALD	TMA+H2O-300C for 10 cycles
	31.0	Spin 2% HSQ	PR Bench	1. Warm 2% HSQ to RT for 15mins 2. Dispense 2% HSQ, wait 30s 3. Spin 5000 RPMs for 30s
	31.1	Pre-Bake	PR Bench	Bake 200°C for 120s
	31.2	EBL Exposure	JEOL 6300	500 pA, Aperature 5, Dose 5000 uC/cm^2 Gain: x60/8/75/60/1125 Scan Parameters: 10scans/10kns/10um wide/20um position Recipe: 0618_Campaign13_DG1 (.sdf .jdf .mgn)
	31.3	Develop	Develop Bench	1. NaOH:NaCl:H2O = 2g:8g:200mL for 60s (**DO NOT STIR**) 2. DI rinse for 10mins **(DO NOT STIR)** --> move to fresh DI twice (1min & 5min)
	31.4	Write Check	Optical Microscope	Check to see if dummy gates are visible, straight, and well adhered
	31.5	Dummy Gate Bake	PR Bench	Bake 150°C for 30mins to avoid HSQ outgas in MOCVD
	31.6	Measure Layer Thicknesses	J.A. Woolam	Measure InGaAs cap thickness using same model from section 10
	32.0	Digital Etch (x1)	UV Ozone	10min UV Ozone
			Acid Bench	HCl:H2O 1:10 for 60s **(DO NOT STIR)**
	32.1	Measure Layer Thicknesses	J.A. Woolam	Measure InGaAs cap thickness using same model from section 10
	32.2	Link Region Regrowh	Thomas Swan MOCVD	1. 3.0nm UID-InP at 600°C 2. 3.5nm 1x10^19 cm^-13 Si:InP at 600°C 3. 10nm UID-InP at 600°C
	32.3	Measure Layer Thicknesses	J.A. Woolam	Measure regrown InP thicknes + channel cap thickness
	32.4	Sheet Resistance Check	Four Point Probe	Measure link sheet resistance
	32.5	Growth Check	Optical Microscope	Check to make sure growth is smooth no major impurities on wafer

S/D EBL + Regrowth	40.0	Remove HSQ Dummy Gate	HF Bench	1. BHF for 2mins
				2. DI rinse for 2mins
	40.1	Adhesion Layer Deposition	Oxford-FlexAL ALD	TMA+H2O-300C for 10 cycles
	40.2	Spin 6% HSQ	PR Bench	1. Warm 6% HSQ to RT for 15mins
				2. Dispense 6% HSQ, wait 30s
				3. Spin 5000 RPMs for 30s
	40.3	Pre-Bake	PR Bench	Bake 200°C for 120s
	40.4	EBL Exposure	JEOL 6300	500 pA, Aperature 5, Dose 5000 uC/cm^2
				Gain: x60/8/75/60/1125
				Scan Parameters: 10scans/10kns/10um wide/20um position
				Recipe: 0620_Campaign13_DG2 (.sdf .jdf .mgn)
	40.5	EBL Exposure	JEOL 6300	10 nA, Aperature 7, Dose 5000 uC/cm^2
				Gain: x1/9/150/200/1721
				Scan Parameters: 5scans/5kns/10um wide/20um position
				Recipe: 0620_Campaign13_DG2_UV (.sdf .jdf .mgn)
	40.6	Develop	Develop Bench	1. NaOH:NaCl:H2O = 2g:8g:200mL for 60s **(DO NOT STIR)**
				2. DI rinse for 1 min **(DO NOT STIR)**
				3. NaOH:NaCl:H2O = 2g:8g:200mL for 30s **(DO NOT STIR)**
				4. DI rinse for 5-10mins **(DO NOT STIR)**
	40.7	**Write Check**	**Optical Microscope**	**Check to see if dummy gates are visible, straight, and well adhered**
	40.8	Dummy Gate Bake	PR Bench	Bake 150°C for 30mins to avoid HSQ outgas in MOCVD
	41.0	Digital Etch (x9 + x1)	UV Ozone	10min UV Ozone **(DO NOT STIR)**
			Acid Bench	HCl:H2O 1:10 for 60s **(DO NOT STIR)**
	41.1	**Measure Layer Thicknesses**	**J.A. Woolam**	**Measure InP link thickness periodically during link etching**
	41.2	**Sheet Resistance Check**	**Four Point Probe**	**Measure link quantum well sheet resistance as cap is thinned**
	42.0	S/D Regrowth	Thomas Swan MOCVD	1. 75nm 4x10^19 cm^-3 Si:InGaAs
	42.1	**Growth Check**	**Optical Microscope**	**Check to make sure growth is smooth no major impurities on wafer**
	42.2	**Thickness Check**	**J.A. Woolam**	**Measure S/D InGaAs thickness**
	42.3	**Sheet Resistance Check**	**Four Point Probe**	**Sheet resistance 19Ω/□ for 80nm; 25Ω/□ for 50nm n++ InGaAs**
Mesa Isolation	50.0	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
	50.1	Dehydration	PR Bench	Bake 110°C for 5mins
	50.2	Spin SPR 955-1.8	PR Bench	1) Dispense SPR 955-1.8, wait 30s
				2) Spin 3000 RPMs for 30s
	50.3	Pre-Bake	PR Bench	Bake 90°C for 90s
	50.4	Expose Mesa Isolation	GCA200	Mask = 1-RF-ISO, Job = RFMARK\PAD
				Focus-offset = 0, Exposure-time = 0.42 s
	50.5	Post-Bake	PR Bench	Bake 110°C for 90s
	50.6	Develop	Develop Bench	1) AZ300-MIF for 60s
				2) DI Rinse 60s
	51.0	Etch Mesa	Acid Bench	1. H3PO4:H2O2:H2O 1:1:25 for 45s to etch regrown S/D (2.77 nm/s)
				Check to insure complete removal
				2. HCl:H2O 1:1 for 10s to etch InP link region(8 nm/s)
				Check to insure complete removal
				3. H3PO4:H2O2:H2O 1:1:25 for 60s to remove channel + back barrier (2.77 nm/s)
				Check to insure complete removal
				4. HCl:H2O 1:1 for 8s to etch into InP substrate (8 nm/s)
				Check to insure complete removal
	51.1	Strip Resist	Isothermal Bath	1. NMP at 80°C for 2 hours
				2. IPA/DI rinse
	51.2	**Measure Layer Thicknesses**	**J.A. Woolam**	**Measure InP link thickness periodically during link etching**
	51.3	**Etch Check**	**DEKTAK/Bruker AFM**	**Check to make sure etched into InP substrate**

High-k	60.0	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
	60.1	Remove HSQ Dummy Gate	HF Bench	1. BHF for 2mins
				2. DI rinse for 2mins
	60.2	Digital Etch (x3)	UV Ozone	10min UV Ozone
			Acid Bench	HCl:H2O 1:10 for 60s, DI rinse 60s
	60.3	**Measure Layer Thicknesses**	**J.A. Woolam**	**Measure InGaAs S/D thickness to infer amount of channel removed**
	60.4	Remove Native Oxide	HF Bench	BOE for 2mins, DI rinse 60s
	60.5	High-k Deposition	Oxford-FlexAL ALD	1. Season/shake plasma shutter CH3-TMA+100W/N*-300C for 15 cycles
				2. CH3-TMA+100W/N*-300C for 9 cycles
				3. CH3-TEMAZ+H2O-300C for 30 cycles
	60.6	Forming Gas Anneal	Rodwell Furnace	Recipe: Lee
	60.7	**Measure High-k Thicknesses**	**J.A. Woolam**	**Measure High-k thickness Thickness**
T-Gate	70.0	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
	70.1	Dehydration	PR Bench	Bake 110°C for 5mins
	70.2	Spin CSAR:A 2:1	PR Bench	1) Surpass 4000 soak for 60 sec
				2) DI rinse 30 sec
				3) Spin 3000 RPM for 30 sec
				4) Spin CSAR:A 2:1 6000 RPMs for 30 seconds (Recipe 8)
				5) Bake 180°C for 5 mins
	70.3	EBL Exposure	JEOL 6300	500 pA, Aperature 5, Dose 220 uC/cm^2
				Gain: x60/8/75/60/1125
				Scan Parameters: 10scans/10kns/10um wide/20um position
				Recipe: 0629_Campaign13_TGF (.sdf .jdf .mgn)
	70.4	Develop	Solvent Bench	1) Amyl Acetate for 75s
				2) IPA Rinse 20s
	70.5	Spin UV-6	PR Bench	1) Spin 3000 RPMs for 30s
				2) Bake 115C for 90s
	70.6	EBL Exposure	JEOL 6300	500 pA, Aperature 5, Dose 100 uC/cm^2
				Gain: x60/8/75/60/1125
				Scan Parameters: 10scans/10kns/10um wide/20um position
				Recipe: 0629_Campaign13_TGF (.sdf .jdf .mgn)
	70.7	Post-Bake	Solvent Bench	Bake 135°C for 2mins
	70.8	Develop	Solvent Bench	1) AZ300-MIF for 60s (slow stir)
				2) DI rinse 60s (water flush)
	71.0	Gate Metal Deposition	Thermal Evaporator	Ni/Au 30nm/300nm
				Rates: 1.0/3.0 Å/s
	71.1	PR Strip	Isothermal Bath	1. NMP at 80°C for 1 hour
				2. IPA/DI rinse
	71.2	Post Metal Anneal	Oxford-FlexAL ALD	Bake in H2 at 350°C for 30mins
				Cool in H2 to 300°C (~10 mins)
	71.3	**Sheet Resistance Check**	**Four Point Probe**	**Check Gate Metal Sheet Resistance**
	71.4	**Check Gate Metal**	**JEOL SEM**	**Check for T-Gate collapse and alignment**

Start Date: 07/07/2020				Sample: Ch7-L6G3SD8 Source-Drain Process
Loop	Step #	Process Step	Equipment	Process
S/D Via + Ohmic	80.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI rinse 60s
	80.1	Dehydration	PR Bench	Bake 110°C for 5mins
	80.2	Spin PMMA Bilayer	PR Bench	1) Surpass 4000 soak for 60 sec 2) DI rinse 30 sec **3) Spin 3000 RPM for 30 sec (BLOW DRY INSTEAD IN FUTURE)** 4) Spin PMMA 50k 3000 RPMs for 30s (Recipe 5) 5) Bake 180°C for 5 mins 6) Spin PMMA 950k 1000 RPMs for 45s (Recipe 2) 7) Bake 180°C for 5 mins
	80.3	EBL Exposure	JEOL 6300	2 nA, Aperature 6, Dose 650 uC/cm^2 Gain: x1/15/145/3/2000 Scan Parameters: 10scans/5kns/10um wide/45um position Recipe: 0707_Campaign13_SDV (.sdf .jdf .mgn)
	80.4	Develop	Develop Bench	1) MIBK:IPA 1:1 for 60s 2) IPA rinse for 20s
	81.0	Open S/D Vias	HF Bench	1. BHF for 45s (DO NOT STIR) 2. DI rinse for 2mins (DO NOT STIR)
	81.1	Clean Surface	Acid Bench	1. HCl:H2O 1:10 for 60s 2. DI rinse 60s
	81.2	S/D Metal Deposition	E-Beam #4	Pd/Ni/Au 5/30/30 Rates: 0.7/1.0/1.0 Å/s
	81.3	PR Strip	Isothermal Bath	1. NMP at 80°C for 2 hours 2. IPA/DI rinse
Pad Metal	90.0	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
	90.1	Dehydration	PR Bench	Bake 110°C for 5mins
	90.2	Spin nLoff-5510	PR Bench	1) Dispense HMDS, wait 20s 2) Spin HMDS 4000 RPMs for 30 seconds (Recipe 7) 3) Dispense nLoff-5510, wait 30s 4) Spin 2500 RPMs for 30s (Recipe 4)
	90.3	Pre-Bake	PR Bench	Bake 90°C for 60s
	90.4	Expose S/D Metal	GCA200	Mask = 08-FET-PAD, Job = RFMARK\MARK Focus-offset = 0, Exposure-time = 0.46s
	90.5	Post-Bake	PR Bench	Bake 110°C for 90s
	90.6	Develop	Develop Bench	1) AZ300-MIF for 60s 2) DI Rinse 60s
	90.7	Hard-Bake	Solvent Bench	Bake 120°C for 15mins
	91.0	S/D Metal Deposition	E-Beam #4	Ni/Au 20/300nm Rates: 1.0/3.0 Å/s
	91.1	PR Strip	Isothermal Bath	1. NMP at 80°C for 2 hours 2. IPA/DI rinse
	91.2	**Sheet Resistance Check**	**Four Point Probe**	**Check S/D Metal Sheet Resistance**
	91.2	**Check S/D metal & recess**	**JEOL SEM**	**Check S/D metal quality/alignment**

Appendix 4 – TASE/CELO Process A

Start Date: 04/22/19				Sample: 042219	
Loop	**Step #**	**Process Step**	**Equipment**	**Process**	**X**
Alignment Marks	10.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	X
	10.1	Etch Stop Deposition	Oxford-FlexAL ALD	TMA+H2O-300C for 50 cycles	X
	10.2	**Deposition Verification**	**J.A. Woolam**	**Check Al2O3 thickness**	**X**
	10.3	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	X
	10.4	Chamber Season	PECVD1	STD SiO2 coat	X
		Hard Mask Deposition	PECVD1	STD SiO2 deposition for 30s	X
	10.5	**Deposition Verification**	**J.A. Woolam**	**Check SiO2 thickness**	**X**
	11.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	X
	11.1	Activate Surface	PEII	300 mTorr / 100 W for 15 sec	X
	11.2	Dehydration	Hotplate	Bake 110°C for 5 mins	X
	11.3	Spin SPR955-0.9	PR Bench	1) Dispense HMDS, wait 20 seconds 2) Spin 4000 RPMs for 30 seconds 3) Spin SPR-955-0.9 4000 RPMs for 30 seconds 4) Bake 90°C for 90 sec	X
	11.4	Exposure	GCA 2000	Mask = CELOv15, Job = CELOV2\ALIGN Focus-offset = 0, Exposure-time = 0.45	X
	11.5	Hard Bake	Hotplate	Bake 110°C for 90 sec	X
	11.6	Develop	Develop Bench	1) AZ300-MIF for 60 seconds 2) DI Rinse 60 sec	X
	11.7	**Pattern Inspection**	**Optical Microscope**	**Check that patterns are fully exposed/developed with no systematic deviations**	**X**
	12.0	Chamber Season	ICP2	1) 5 min O_2 clean (#103) 2) 5 min $CHF_3/CF_4/O_2$ 35/5/10 (#123), ICP/CCP = 500/50 Watts, Pressure = 0.5 Pa	X
		Etch SiO_2	ICP2	$CHF_3/CF_4/O_2$ = 35/5/10 sccm (#123) for 23 seconds ICP/CCP = 500/50 Watts, Pressure = 0.5 Pa Etch rates: SiOx = 1.24 nm/s, Al2O3 = 0.13 nm/s	X
	12.1	Strip Resist	Isothermal Bath	ACT-410 at 80°C for 2 hours/IPA/DI rinse	X
			Gasonics	275°C for 180 sec	
	12.2	Etch Al2O3	Develop Bench	AZ300-MIF for 5 mins DI rinse for 60 sec	X
	12.3	Chamber Season	RIE #2	1) O2 clean 20 mTorr, 500 V for 30 mins 2) CH4/H2/Ar 4/20/10 mTorr, 300 V for 30 mins	X
		RIE Etch Alignment Marks	RIE #2	1) CH4/H2/Ar 4/20/10 mTorr, 300 V for 5 mins 2) O2 clean 20 mTorr, 300 V for 10 mins	X
	12.4	Strip Hard Mask	HF Bench	BOE for 3 mins	X
Seed Holes	20.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	X
	20.1	Etch Stop Deposition	Oxford-FlexAL ALD	TMA+H2O-300C for 50 cycles	X
	20.2	**Deposition Verification**	**J.A. Woolam**	**Check Al2O3 thickness**	**X**
	20.3	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	X
	20.7	Chamber Season	PECVD1	STD SiO2 coat	X
		Seed Layer Deposition	PECVD1	STD SiO2 deposition for 35s	X
	20.8	**Deposition Verification**	**J.A. Woolam**	**Check SiO2 thickness**	**X**
	21.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	X
	21.1	Activate Surface	PEII	300 mTorr / 100 W for 15 sec	X
	21.2	Dehydration Bake	Hotplate	110°C for 5 mins	X
	21.3	Spin CSAR:A 1:1	PR Bench	1) Surpass 4000 soak for 60 sec 2) DI rinse 30 sec 3) Spin 3000 RPM for 30 sec 4) Spin CSAR:A 1:1 3000 RPMs for 30 seconds (Recipe 5) 5) Bake 180°C for 5 mins	X
	21.4	EBL Exposure	JEOL 6300	2 nA, Aperature 6, Dose 220 Gain: x1/8/245/3/2077 Scan Parameters: 60scans/10kns/10um wide/40um pos Recipe: 0523_0226CELO_SEED (.sdf .jdf .mgn)	X
	21.5	Develop	Solvent Bench	1) Amyl Acetate for 60 seconds 2) IPA rinse for 20 seconds 3) DI Rinse	X
	21.6	Post-Bake	Hotplate	Bake 135°C for 60 sec	X
	22.0	Chamber Season	ICP2	1) 5 min O_2 clean (#103) 2) 5 min $CHF_3/CF_4/O_2$ 35/5/10 (#123), ICP/CCP = 500/50 Watts, Pressure = 0.5 Pa	X
		Etch SiO_2	ICP2	$CHF_3/CF_4/O_2$ = 35/5/10 sccm (#123) for 28 seconds ICP/CCP = 500/50 Watts, Pressure = 0.5 Pa Etch rates: SiO_x = 1.24 nm/s, CSAR= 2.84 nm/s, Al2O3 = 0.14 nm/s	X
	22.1	Strip Resist	Gasonics	>350°C for 180 sec	X
	22.2	**Etch Verification**	**Bruker AFM**	**Check SEED in center die and edge die for flat bottom/etch depth**	**O**
	22.3	**Etch Verification**	**JEOL SEM**	**Check 150x150nm SEED on edge and center die**	**O**

Sacrificial Layer	30.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	X
	30.1	Sacraficial Layer Deposition	Sputter #3	BM_Si_200W_1400s Gun Tilt = 4, Height = 1.52"	X
	30.2	**Deposition Verification**	**J.A. Woolam**	**Check a-Si thickness**	**X**
	31.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	X
	31.1	O2 Descum	PEII	O2 descum 300 mTorr / 100 W for 15 seconds	X
	31.2	Dehydration Bake	Hotplate	110°C for 5 mins	X
	31.3	Spin maN-2403	PR Bench	1) Surpass 4000 soak for 60 sec 2) DI rinse 30 sec 3) Spin 3000 RPM for 30 sec 4) Spin maN 3000 RPM for 30 sec (Recipe 5) 5) Bake 90°C for 60 seconds	X
	31.4	EBL Exposure	JEOL 6300	10 nA, Aperature 7, Dose 700 FDA module: 2.5um = 750 uC/cm^2, 5.0um = BD, 10.0um = 1250 uC/cm^2 Gain: x1/7/200/170/1710 Scan Parameters: 10scans/5kns/10um wide/40um pos Recipe: 0526_0422CELO_SAC (.sdf .jdf .mgn)	X
	31.5	Develop	Develop Bench	1) AZ300-MIF for 60 seconds 2) DI Rinse for 60 seconds	X
	32.0	Chamber Season	ICP2	1) 5 min O_2 clean (#103) 2) 5 min $CHF_3/CF_4/O_2$ 35/5/10 (#123), ICP/CCP = 500/50 Watts, Pressure = 0.5 Pa	X
		Etch a-Si	ICP2	$CHF_3/CF_4/O_2$ = 35/5/10 sccm (#123) for 80s ICP/CCP = 500/50 Watts, Pressure = 0.5 Pa Etch rates: SiO_x = 1.24 nm/s, maN = 2.18 nm/s, a-Si = 0.97 nm/s, SiN = 1.83 nm/s	X
	32.1	**Etch Verification**	**J.A. Woolam**	**Check a-Si thickness to verify completely removed**	**X**
	32.2	Strip Resist	Isothermal Bath	ACT-410 at 80°C for 2 hours	X
			Gasonics	>350°C for 180 sec	
	32.4	**Etch Verification**	**Bruker AFM**	**Check patterns on edge and center to ensure a-Si complete removal and t_cav**	**O**
	32.5	**Etch Verification**	**JEOL SEM**	**Check patterns on edge and center die**	**O**
Source Holes	40.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	X
	40.1	Chamber Season	PECVD1	STD SiO2 coat	X
		Source Deposition	PECVD1	STD SiO2 deposition for 75s	X
	40.2	**Deposition Verification**	**J.A. Woolam**	**Check SiO2 thickness**	**X**
	41.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	X
	41.1	O_2 Descum	PEII	300 mTorr / 100 W for 15 sec	X
	41.2	Dehydration Bake	Hotplate	110°C for 5 mins	X
	41.3	Spin 100% CSAR	PR Bench	1) Surpass 4000 soak for 60 sec 2) DI rinse 30 sec 3) Spin 3000 RPM for 30 sec 4) Spin 100% CSAR 3000 RPMs for 30 seconds (Recipe 5) 5) Bake 180°C for 5 mins	X
	41.4	EBL Exposure	JEOL 6300	2 nA, Aperature 6, Dose 220 Gain: x1/8/245/3/2077 Scan Parameters: 60scans/10kns/10um wide/40um pos Recipe: 0528_0422CELO_SOURCE (.sdf .jdf .mgn)	X
	41.5	Develop	Solvent Bench	1) Amyl Acetate for 60 seconds 2) IPA rinse for 20 seconds 2) DI Rinse	X
	41.6	Post-Bake	Hotplate	Bake 135°C for 60 sec	X
	42.0	Chamber Season	ICP2	1) 5 min O_2 clean (#103) 2) 5 min $CHF_3/CF_4/O_2$ 35/5/10 (#123), ICP/CCP = 500/50 Watts, Pressure = 0.5 Pa	
		Etch SiO_2	ICP2	$CHF_3/CF_4/O_2$ = 35/5/10 sccm (#123) for 55 seconds ICP/CCP = 500/50 Watts, Pressure = 0.5 Pa Etch rates: SiO_x = 1.24 nm/s, CSAR = 2.84 nm/s, a-Si = 0.97 nm/s	
	42.1	Strip Resist	Isothermal Bath	ACT-410 80°C for 2 hours	
			Solvent Bench	IPA/DI rinse for 60 seconds	
Backend	50.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	
	50.1	Dehydration Bake	PR Bench	110°C for 5 mins	
	50.2	Spin SPR 955-0.9	PR Bench	1) Dispense HMDS, wait 20 seconds 2) Spin 3000 RPMs for 30 seconds 3) Spin SPR 955-0.9, spin 3000 RPMs for 30 seconds 4) Bake 100°C for 60 sec	
	50.3	Dice Sample	Dicing Saw	Brian_InP_LEO dice wafer into 25 samples	
	50.4	Strip Resist	Solvent Bench	1) Spin 5000 RPM for 60 sec while spraying NMP 2) Spin 5000 RPM for 15 sec while spraying IPA	
	42.2	Remove a-Si	XeF2	4 Torr, 180s, 2 cycles	
	42.3	**Etch Verification**	**JEOL SEM**	**Check patterns to make sure completel a-Si removal**	
	42.4	Strip Resist	Gasonics	>350°C for 180 sec	

Appendix 5 – TASE/CELO Process R

Start Date: 11/27/18				Sample: 112718	
	Step #	Process Step	Equipment	Process	X
Alignment Marks	10.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	X
	10.1	Etch Stop Deposition	Oxford-FlexAL ALD	TMA+H2O-300C for 30 cycles	X
	10.2	**Deposition Verification**	**J.A. Woolam**	**Check Al2O3 thickness**	**X**
	10.3	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	X
	10.4	Chamber Season	PECVD1	_30CLNSiO	X
		Hard Mask Deposition	PECVD1	_SiO02	X
	10.5	**Deposition Verification**	**J.A. Woolam**	**Check SiO2 thickness**	**X**
	11.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	X
	11.1	Activate Surface	PEII	300 mTorr / 100 W for 15 sec	X
	11.2	Dehydration	Hotplate	Bake 110°C for 5 mins	X
	11.3	Spin SPR955-0.9	PR Bench	1) Dispense HMDS, wait 20 seconds 2) Spin 4000 RPMs for 30 seconds 3) Spin SPR-955-0.9 4000 RPMs for 30 seconds 4) Bake 90°C for 90 sec	X
	11.4	Exposure	GCA 2000	Mask = CELOv10, Job = CELOV2\ALIGN Focus-offset = 0, Exposure-time = 0.45 s	X
	11.5	Hard Bake	Hotplate	Bake 110°C for 90 sec	X
	11.6	Develop	Develop Bench	1) AZ300-MIF for 60 seconds 2) DI Rinse 60 sec	X
	12.0	Chamber Season	ICP2	1) 5 min O_2 clean (#103) 2) 5 min $CHF_3/CF_4/O_2$ 35/5/10 (#123), ICP/CCP = 500/50 Watts, Pressure = 0.5 Pa	X
		Etch SiO_2	ICP2	$CHF_3/CF_4/O_2$ = 35/5/10 sccm (#123) for 23 seconds ICP/CCP = 500/50 Watts, Pressure = 0.5 Pa Etch rates: SiOx = 1.24 nm/s, Al2O3 = 0.13 nm/s	X
	12.1	Strip Resist	Isothermal Bath Gasonics	ACT-410 at 80°C for 2 hours/IPA/DI rinse 275°C for 180 sec	X
	12.2	Etch Al2O3	Develop Bench	AZ300-MIF for 5 mins DI rinse for 60 sec	X
	12.3	Chamber Season	RIE #2	1) O2 clean 20 mTorr, 500 V for 30 mins 2) CH4/H2/Ar 4/20/10 mTorr, 300 V for 30 mins	X
		RIE Etch Alignment Marks	RIE #2	1) CH4/H2/Ar 4/20/10 mTorr, 300 V for 5 mins 2) O2 clean 20 mTorr, 300 V for 10 mins	X
	12.4	Strip Hard Mask	HF Bench	BOE for 3 mins	X
Seed Holes	20.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	X
	20.1	Etch Stop Deposition	Oxford-FlexAL ALD	TMA+H2O-300C for 30 cycles	X
	20.2	**Deposition Verification**	**J.A. Woolam**	**Check Al2O3 thickness**	**X**
	20.3	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	X
	20.7	Chamber Season	PECVD1	_30CLNSiO	X
		Seed Layer Deposition	PECVD1	_SiO01	X
	20.8	**Deposition Verification**	**J.A. Woolam**	**Check SiO2 thickness**	**X**
	21.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	X
	21.1	Activate Surface	PEII	300 mTorr / 100 W for 15 sec	X
	21.2	Dehydration Bake	Hotplate	110°C for 5 mins	X
	21.3	Spin 100% CSAR	PR Bench	1) Surpass 4000 soak for 60 sec 2) DI rinse 30 sec 3) Spin 3000 RPM for 30 sec 4) Spin 100% CSAR 3000 RPMs for 30 seconds (Recipe 5) 5) Bake 180°C for 5 mins	X
	21.4	EBL Exposure	JEOL 6300	2 nA, Aperature 6, Dose 220 Gain: x1/8/245/3/2077 Scan Parameters: 60scans/10kns/10um wide/40um pos Recipe: 1129_1127CELO_SEED (.sdf .jdf .mgn)	X
	21.5	Develop	Solvent Bench	1) Amyl Acetate for 60 seconds 2) IPA rinse for 20 seconds 3) DI Rinse	X
	21.6	Post-Bake	Hotplate	Bake 135°C for 60 sec	X
	22.0	Chamber Season	ICP2	1) 5 min O_2 clean (#103) 2) 5 min $CHF_3/CF_4/O_2$ 35/5/10 (#123), ICP/CCP = 500/50 Watts, Pressure = 0.5 Pa	X
		Etch SiO_2	ICP2	$CHF_3/CF_4/O_2$ = 35/5/10 sccm (#123) for 25 seconds ICP/CCP = 500/50 Watts, Pressure = 0.5 Pa Etch rates: SiO_x = 1.24 nm/s, CSAR= 2.84 nm/s, Al2O3 = 0.14 nm/s	X
	22.1	Strip Resist	Gasonics	>350°C for 180 sec	X
	22.2	Etch Verification	JEOL SEM	Check 150x150nm SEED on edge and center die	N/A

Sacraficial Layer	30.1	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	X
	30.2	Activate Surface	PEII	O2 descum 300 mTorr / 100 W for 15 seconds	X
	30.3	Dehydration Bake	Hotplate	110°C for 5 mins	X
	30.4	Spin CSAR:A 1:2	PR Bench	1) Surpass 4000 soak for 60 sec 2) DI rinse 30 sec 3) Spin 3000 RPM for 30 sec 4) Spin CSAR:A 1:2 6000 RPMs for 30 seconds (Recipe 9) 5) Bake 180°C for 5 mins	X
	30.5	EBL Exposure	JEOL 6300	2 nA, Aperature 6, Dose 200 uC/cm^2 Gain: x1/8/245/3/2077 Scan Parameters: 60scans/10kns/10um wide/40um pos Recipe: 1203_1127CELO_SAC (.sdf .jdf .mgn)	X
	30.6	Develop	Solvent Bench	1) Amyl Acetate for 60 seconds 2) IPA rinse for 20 seconds	X
Source Layer	40.0	Spin 6% HSQ	PR Bench	1) Spin 6% HSQ 3000 RPMs for 30 seconds (Recipe 5) 2) Bake 200°C for 120 sec	X
	40.1	EBL Exposure	JEOL 6300	10 nA, Aperature 7, Dose 1000 uC/cm^2 Gain: x1/7/200/170/1710 Scan Parameters: 20scans/5kns/10um wide/40um pos Recipe: 1206_1127CELO_SOURCE (.sdf .jdf .mgn)	X
	40.2	Develop	Solvent Bench	1) 25% TMAH for 60 seconds 2) DI Rinse	X
	41.0	Flood Exposure	DUV Flood Exp.	Flood Exposure for 10mins	X
	41.1	Remove CSAR	Solvent Bench	Amyl Acetate (30 mins)/IPA (30 mins)/DI (1 min)	X
			Isothermal Bath	NMP at 80°C for 2 hours	
			Gasonics	>350°C for 180 sec	
	41.2	Remove Etch Stop	Develop Bench	AZ300-MIF for 10 mins	X
	41.3	Etch Verification	JEOL SEM	Check SA or SAR pattern on edge and center die	X
Dicing	50.0	Solvent Clean	Solvent Bench	Acetone/Methanol/IPA/DI	X
	50.1	Dehydration Bake	PR Bench	110°C for 5 mins	X
	50.2	Spin AZ-5214	PR Bench	1) Dispense HMDS, wait 20 seconds 2) Spin 3000 RPMs for 30 seconds 3) Spin AZ-5214 at 3000 RPMs for 30 seconds 4) Bake 100°C for 60 sec	X
	50.3	Dice Sample	Dicing Saw	Brian_InP_LEO dice wafer into 25 samples	X
	50.4	Strip Resist	Solvent Bench	1) Spin 5000 RPM for 60 sec while spraying NMP 2) Spin 5000 RPM for 15 sec while spraying IPA	N/A
			Gasonics	>350°C for 180 sec	