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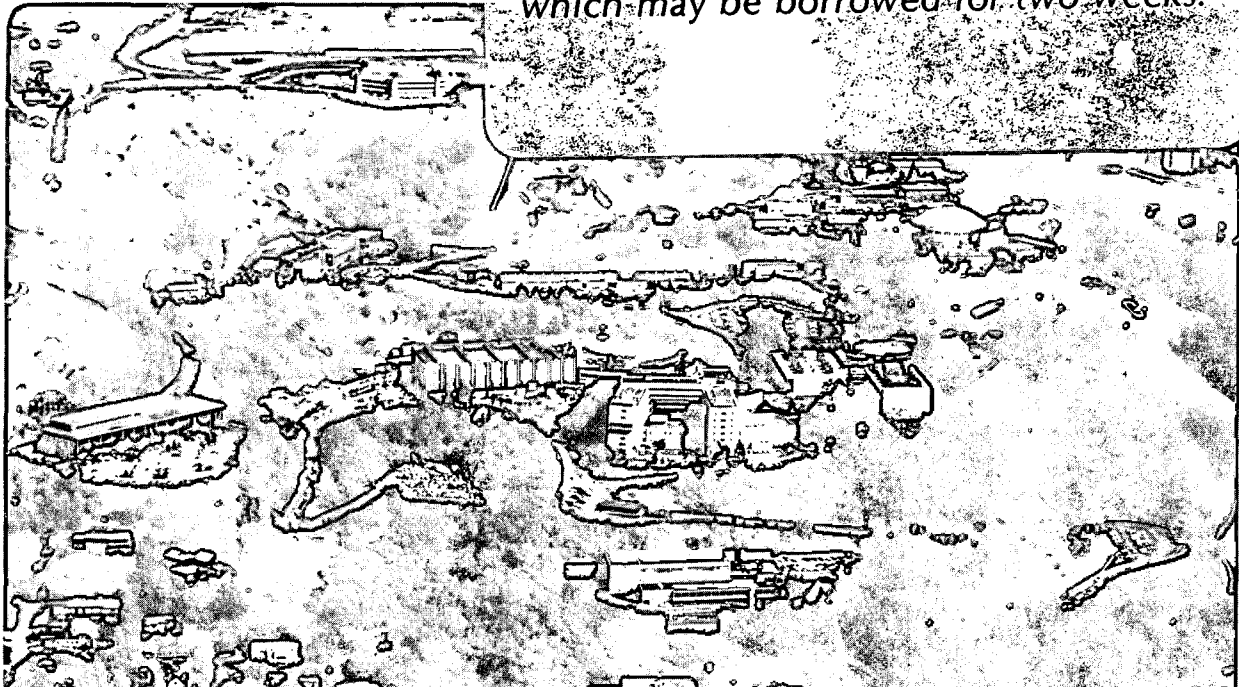
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October 1986

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FAST SIGNAL CALIBRATION SYSTEMS FOR LARGE DETECTOR SYSTEM FRONT ENDS

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Berkeley, California 94720 U.S.A.ABSTRACT

The fast risetime of the calibration signal in a 10 ns front end of a large detector system presents problems not generally encountered in a slower system. The distribution of these signals also presents its own unique set of problems. We have arrived at solutions which are applicable to large systems requiring fast risetime calibration signals in a small volume of space.

INTRODUCTION

The distribution of programable calibration signals of 10 ns risetime to 10,000 channels in a large detector system raises several significant design problems. Feed-through and crosstalk are difficult to avoid because of the fast leading edges of the calibration signals. Multiplexing techniques to reduce the otherwise enormous number of wires and cables must be considered.

The Central Drift Chamber (CDC) for the SLD facility¹ for the SLAC Linear Collider (SLC) is presently under construction. It is an example of a large detector which requires programable calibration pulses of fast risetime. In the SLD, calibration pulses will be used to calibrate and monitor the amplitude and time response of each channel. To do this realistically, the calibration system must be able to simulate the pulses generated by the drift chamber in actual operation.

The design requirements for this system specified that the charge injected by the calibration pulses at the preamplifier input be controllable over the range 50 fC - 5 pC (corresponding to about 0.1 - 10 min ionizing particles). They also required that the amplitude of the calibration pulses be reproducible to less than 1%. The reproducibility of the time-of-arrival of the calibration pulses should be less than 2 ns.

Each channel in the CDC is being instrumented with a preamplifier, a calibration pulse generator for amplitude and timing calibration, and a time-slicing analog storage unit. In order to place all of these components close to the chambers in the small available space, this electronics is being constructed in hybrid integrated circuit form². It will include a preamplifier hybrid that contains eight channels of preamplification. To reduce the cable plant to reasonable proportions, both digital and analog control and data signals are to be transmitted to and from each hybrid in a serial mode.

Because the CDC is being read out by the current division method, and because of the time-slicing storage at the output, the preamplifiers are designed with low (30 ohm) input resistance and fast (about 15 ns) risetime.

The conceptual design of the overall CDC electronics has been described^{1,2}. The authors of the present paper have been involved with the detailed design of the hybrid preamplifier. This paper is especially concerned with part of that design - i.e., the system for distributing programable, fast, calibration pulses

to the 10,000 preamplifier channels. Although the particular system is intended for use in the CDC, the principles are applicable to similar problems in other detector systems.

GENERAL TECHNIQUE

A possible design technique would have been to generate precision pulses at a central location and then distribute them to all of the hybrid integrated circuits. This technique immediately presents the problem of designing a compact repeater system that adequately preserves the amplitude and shape of the pulses to the required precision. To avoid this problem, it was decided to distribute a dc amplitude-control signal and a strobe (timing) pulse. Although the timing pulse must also be distributed to each of the thousands of channels, it need only preserve a time-of-arrival. Within each preamplifier hybrid, then, a pulse can be generated whose amplitude is controlled by the dc signal and whose timing is controlled by the strobe.

It is also required to be able to control which preamplifiers receive calibration pulses and which do not. In other words, it is required to be able to simulate any particular pattern of "hits" at the drift chamber wires. This is done by controlling the application of the calibration pulse to each of the eight channels within the hybrid by one bit of an 8-bit shift register. The shift register, of course, can be loaded in bit-serial format.

Within the hybrid, calibration pulses to individual channels are distributed via diode or FET switches which are controlled by the shift registers. Eight signal channels are placed in each hybrid unit.

The wide bandwidth of the calibration signals cause feedthrough and crosstalk problems. Analyses of the characteristics of FET's and diodes led us to solutions of the feedthrough problem, which are presented in this paper. Applications of these analyses can be made to future systems of even wider bandwidths.

CALIBRATION SYSTEMS

Figures 1 and 2 show block diagrams of two possible schemes for generating calibration pulses and distributing them to the individual preamplifier inputs.

In both systems, the contents of shift registers control whether the pulse is applied to a given channel. The use of shift registers reduces the number of digital control signals to just three; i.e., data in, clock and data out. The shift registers in individual hybrid chips can be daisy-chained together to increase the level of multiplexing in interfacing to the world external to the chamber environment. The data-out line goes to the data-in line of the next chip while the clock signal is bussed to all systems.

Calibration pulses are generated in response to the strobe, which is a digital pulse - a pulse whose amplitude is not accurately controlled. The amplitude of the calibration pulses are determined by the level of the dc calibration voltage. Because the calibration pulses are generated close to the input of each signal

preamplifier, only dc levels and digital signals need be brought into the hybrid integrated circuit. Therefore, the problems of crosstalk and feedthrough can be more closely controlled than if the calibration pulses were generated at a central location and then distributed globally.

Figure 1 illustrates a system using eight individual calibration pulse generators, one for each channel. This configuration is acceptable provided that each pulse generator is very simple and has few components. For a system requiring risetimes slower than 100 ns, a very simple pulser circuit such as a single FET switch is adequate. However, for systems requiring risetimes as short as 10 ns, the feedthrough through the gate to drain capacitance is excessive. A more complex circuit is therefore required.

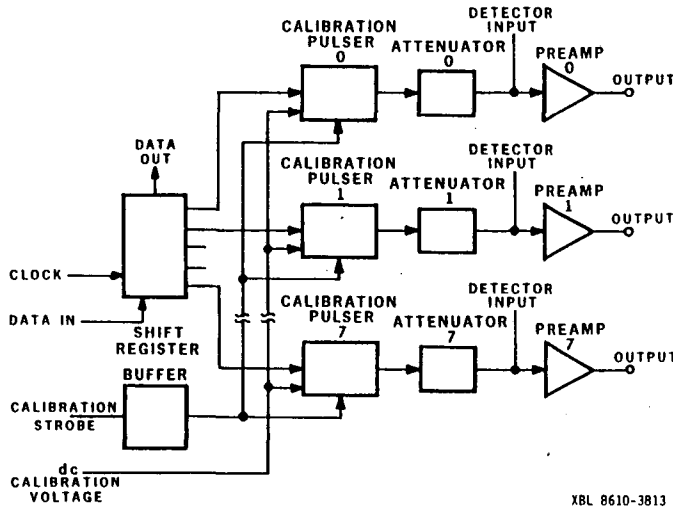


Fig. 1 Block diagram of a calibration system using multiple pulse generators

Figure 2 shows another system which uses a single calibration pulse generator whose output signal is distributed to the eight preamplifiers via switches which may be diodes or CMOS devices. In this system, the calibration pulser can afford to have more complexity and hence more components. Low cost and parts count are considerations to be weighed against performance in designing hybrid integrated circuits.

Since a wide dynamic range of the calibration signal is required, it is necessary that a dc voltage in the range of millivolts to a few volts be switched, on command of the strobe pulse, without the strobe pulse contaminating the calibration signal by feedthrough in the switching device. In a fast system, however, the stray capacitance of the switching elements can contribute significantly to feedthrough. The signal distribution technique also plays an important role in minimizing undesirable signal feedthrough to channels which are turned off. Other calibration systems have been described elsewhere³⁻⁵.

FEEDTHROUGH TRANSIENT ANALYSIS

A high-frequency equivalent circuit of an FET and a few associated components operating as a step generator is shown in Fig. 3. In this circuit, the charge injection capacitor, C_c , is charged to the dc calibration voltage, V_{cal} . A strobe pulse introduced at point G turns on the FET and drops point D to ground potential. A charge equal to $V_{cal} \times C_c$ is thus injected into the preamp input. This is the "desired" charge that is used for calibration.

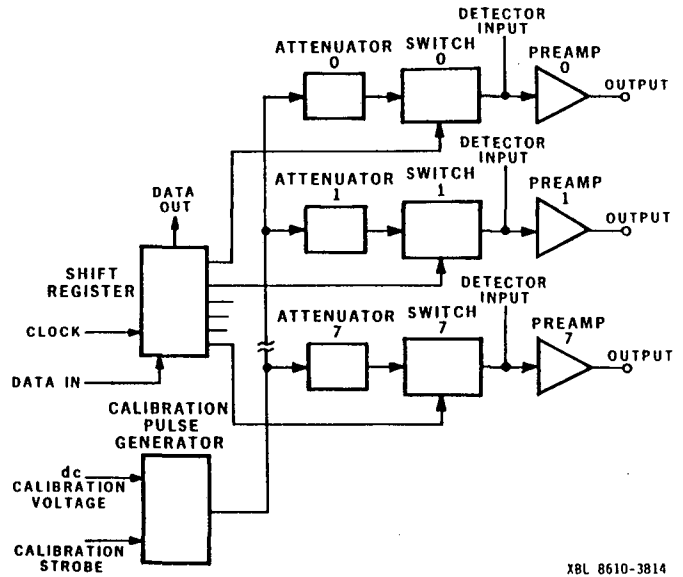


Fig. 2 Block diagram of a calibration system using a single pulse generator and signal distribution switches.

An additional path for "undesired" charge injection is created by the capacitance between the gate and the source of the FET. Part of this, C_{gd} , is internal to the FET, and part, C_{so} , is due to strays in the wiring. This capacitance results in a charge, $V_{gs} \times (C_{gd} + C_{so})$ being injected into node D at the instant the strobe is applied. As the FET turns on, this charge is dissipated through R_{ds} . Since there is a finite turn-on time, however, some of this charge is initially injected through C_c , and is later withdrawn as R_{ds} reaches its low turn-on value. After turn-on is complete, the net charge injected via C_c is zero. If the bandwidth of the preamplifier were sufficiently low, this feedthrough component would not present a problem. However, if the bandwidth is high, the result of the feedthrough can be observed, and can disturb the accuracy of the calibration.

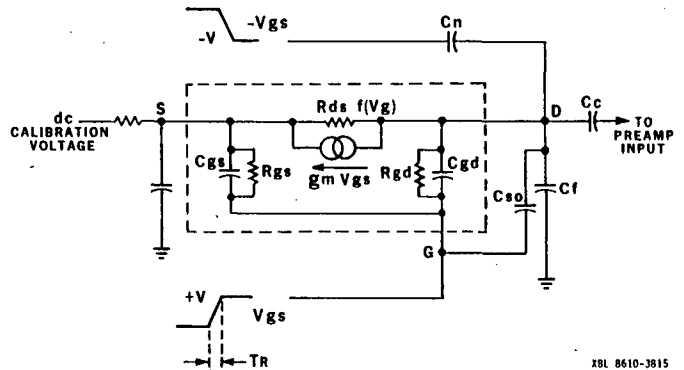


Fig. 3 High frequency equivalent circuit of an FET.

One technique for reducing the effect of the feedthrough charge injection is to inject a compensating charge of the opposite polarity. This is accomplished via C_n . Choice of the appropriate standard value of C_n resulted in a reduction in feedthrough to 20 fC. Further improvement would require fine trimming the value of C_n and the delay time of the compensation pulse with respect to the strobe. In hybrid integrated circuits, this may be accomplished by laser trimming, but with additional cost.

CALIBRATION SIGNAL GENERATOR

Figure 4 is the schematic diagram of the calibration pulse generator used in the system. Q1 is a phase splitter for the strobe pulse; it generates two similar voltage steps with opposite polarities. The positive step is used to turn Q2 on where as the negative step induces a charge of opposite polarity to cancel the feedthrough effect of the positive step. The three diodes are used as capacitors; their total physical size is less than that of a "real" capacitor of the same capacitance. The 10 pF capacitor is used to trim the risetime of the step at the drain of Q2. Q3 and Q4 form a White follower with a 1-2 ohm output impedance. The low output impedance is essential to drive the eight voltage dividers while maintaining amplitude accuracy.

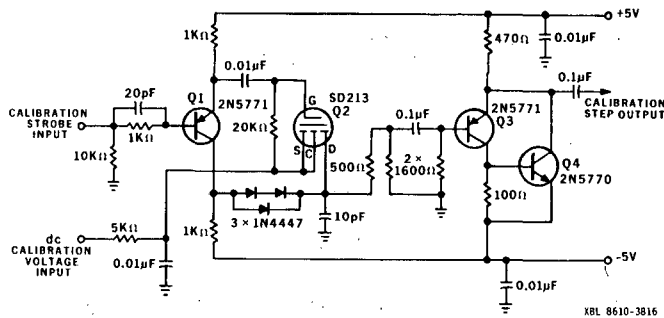


Fig. 4 Schematic diagram of the calibration pulse generator.

SIGNAL GENERATOR PERFORMANCE

The effect of the feedthrough cancellation scheme can be seen by comparing Figs. 5 and 6, which show output waveforms observed at the output of a preamplifier channel. In both cases, the dc calibration voltage is set to zero, so any transient seen is due to feedthrough of the strobe pulse.

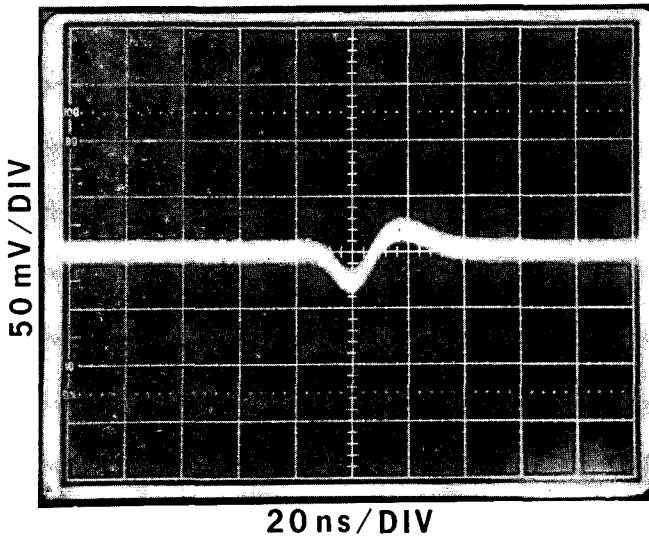


Fig. 5 Preamplifier output showing gate drive feedthrough without transient cancellation in the calibration pulse generator.

Figure 5 shows the output of a preamplifier due to a signal developed by the simple switching circuit with the transient cancellation loop disabled. The amplitude of the feedthrough resultant depends on the time response of the preamplifier and the turn-on time of the FET switch as described earlier. In our initial design, we used an SD213 FET and a C_c of 2 pF. The peak amplitude of the feedthrough pulse was equivalent to 80 fC. Since the lower limit of the calibration range is 50 fC, this feedthrough was deemed too large.

Figure 6 shows the same input conditions but with the transient cancellation loop enabled. Here the effect of the feedthrough is reduced to 20 fC equivalent at the preamplifier input. The effectiveness of the transient cancellation technique is obvious. As mentioned previously, better cancellation would be possible by fine tuning, particularly the value of the capacitor used to cancel the feedthrough component.

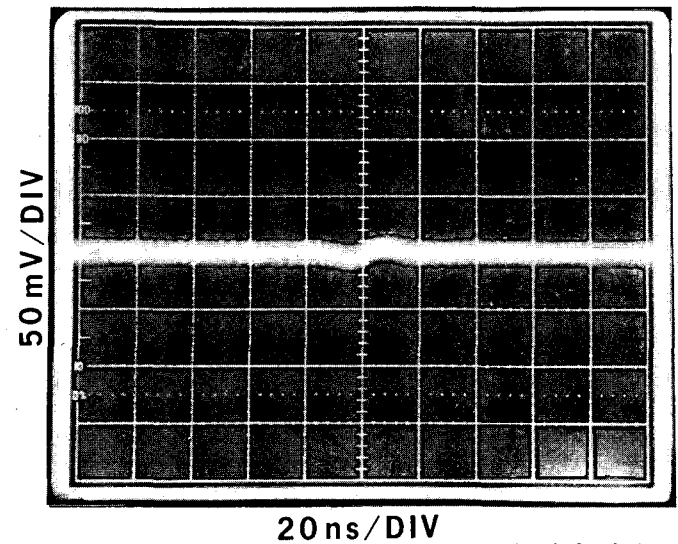


Fig. 6 Preamplifier output showing gate drive feedthrough with transient cancellation in the calibration pulse generator.

Since the calibration signal must meet a certain risetime requirement, it is important that the switching circuit itself not contribute excessively to slowing down the risetime. The on-resistance, R_{ds} , of the FET switch and C_f provide a time constant which is used to trim the overall calibration signal risetime. C_f also helps to suppress the feedthrough transient, however, a large C_f may degrade the overall risetime to an unacceptable level. The transient cancellation scheme provides enough freedom to choose a proper C_f to obtain an acceptable calibration signal risetime and still keep the amount of feedthrough to an acceptable level.

SIGNAL DISTRIBUTION SWITCHES

Two systems for distributing and controlling the application of calibration pulses will be discussed. The first scheme uses high speed CMOS FET switches capable of passing 10 ns risetime pulses while the second scheme uses diode switches. It is important that (a) when the switch is "on" that it does not degrade the amplitude precision or the shape of the calibration signal; and (b) when the switch is "off" it allows little or no signal feedthrough. It is also extremely important to adequately shield adjacent channels from each other. This requires careful design of the hybrid

integrated circuit to provide ground strips on the substrate, or by full-scale shielding if possible.

In the first system, shown in Fig. 7, two CMOS devices are used³ in a series-shunt configuration such that when one is "on" the other is "off". This provides a higher on/off ratio than a single CMOS device used as a series switch. CMOS switches used in this way should be selected on the basis of risetime and on-resistance measurements, since these parameters are crucial to good performance. The substrate bias requirement must also be correct for the polarity of pulses the CMOS switches will be required to handle.

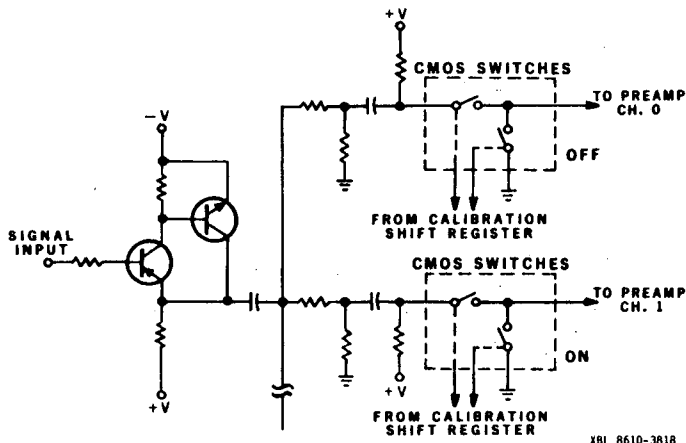


Fig. 7 Schematic diagram showing two signal distribution switches using CMOS devices.

Commercial integrated circuits having four such switches on a single substrate are available. The 74HC4066 is the device used in our design. The compactness afforded by this type of integrated circuit is ideal for applications like this. These CMOS switches are made using 3.5 micron technology and are capable of handling 10 ns risetime signals in the "on" state. In the "off" state, a signal attenuation of 40 dB was obtained.

Figure 8 shows a second type of signal distribution switch using diodes and transistors. Two such switches are shown in the figure. Here, the on/off switching is controlled by the calibration shift register via transistors Q1 and Q2, etc. A switch of this type was found to provide 46 db attenuation in its off state. The transistors used, Q1 and Q2, were 2N5770; the diodes were 1N4447. This design has the advantage of improved performance and also more flexibility in the design to accommodate a wide range of signals. It has the disadvantage of requiring more parts.

FINAL DESIGN

Our final design for the CDC used the signal generator circuit shown in Fig. 4, along with the switch design shown in Fig. 7. The performance of this design is shown in Fig. 9 in which the peak output voltage from the preamplifier and the equivalent input charge are plotted as a function of the dc calibration voltage. The transfer function is linear to within 0.1% until the preamplifier starts to show gain compression at 2 V.

CONCLUSION

We have presented a calibration pulse generator capable of generating voltage steps having rise times in

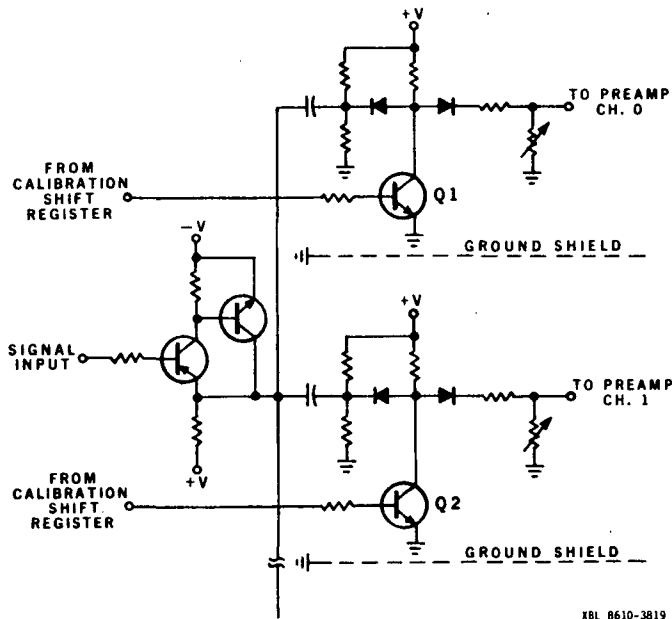


Fig. 8 Schematic diagram showing two signal distribution switches using diodes and transistors.

the 10 ns range. The charge feedthrough due to the fast leading edge of the trigger pulse via inherent circuit and device capacitance is cancelled by introducing an equal charge of the opposite polarity at the summing point. Using standard value components, i.e., without laser trimming the compensation capacitance - the feedthrough charge was reduced to below 20 fC as compared to 80 fC for no compensation.

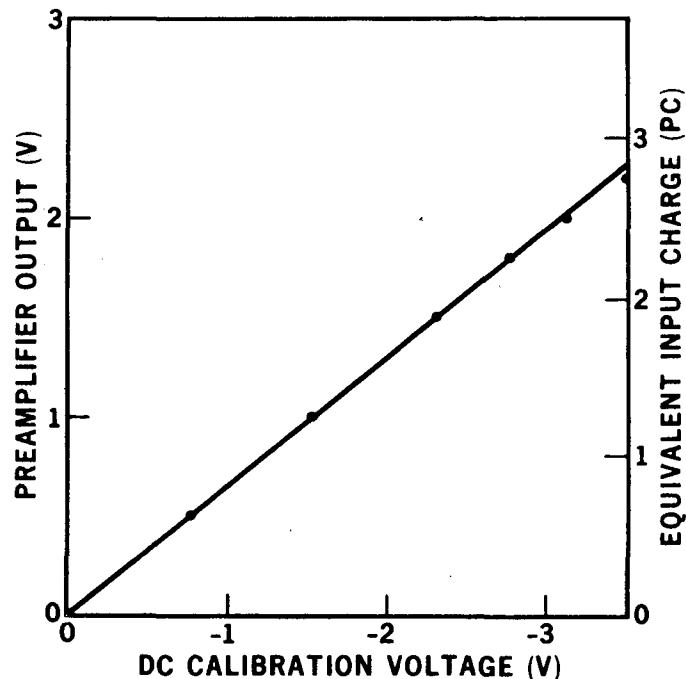


Fig. 9 Preamplifier output and equivalent input charge as a function of dc calibration voltage of the calibration pulse generator.

The signal distribution switch utilizing high speed CMOS devices achieved an off state attenuation of 40 dB whereas the switch utilizing diodes and transistors achieved an on/off ratio of over 46 dB.

For systems requiring risetimes much slower than 10 ns, a slower gate drive and a larger Cf can be used to minimize feedthrough. Transient cancellation then is not necessary. For systems requiring risetimes below the few nanoseconds range the fast diode switch for signal distribution is preferred over the high speed CMOS switch because of its larger bandwidth. However, implementation of diode switches on a hybrid requires more space than an equivalent number of CMOS switches and shielding inside a hybrid is limited to implementation of ground traces and placement of components which may not be adequate to achieve extremely good on/off ratio. A system not limited by these factors will achieve better cancellation than the case presented here using the same technique. The balance of cost, space and performance dictate the final configuration of the design.

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REFERENCES

1. SLD Design Report, SLAC Report 273, May 1984.
2. R.S. Larsen, Overview of the Data Acquisition Electronics System Design for the SLAC Linear Collider Detector (SLD), IEEE Trans. Nucl. Sci., NS-33, No.1 (1986).
3. D. Bernstein and D. Hutchinson, An Integrated Amplifier and Sample and Hold Multiplexer Module, IEEE Trans. Nucl. Trans. Sci., NS-29, No.1 (1982).
4. J. Dawson, et al, Soudan 2 Data Acquisition And Trigger Electronics, IEEE Trans. Nucl. Sci., NS-33, No. 1 (1986).
5. M. Yamauchi, et al, Geiger Mode Calorimeter For PEP-4, IEEE Trans. Nucl. Sci., NS-30, No. 1 (1983).

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