UNIVERSITY OF CALIFORNIA SAN DIEGO

Fully Integrated mm-wave ICs for High Performance Instrumentation Circuits and Systems

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Hyunchul Chung

Committee in charge:

Professor Gabriel Rebeiz, Chair
Professor Gert Cauwenberghs
Professor Drew Hall
Professor William Hodgkiss
Professor Daniel Sievenpiper

2018

The dissertation of Hyunchul Chung is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

_____

_____

_____

_____

_____

Chair

University of California San Diego

2018

DEDICATION

To my family

EPIGRAPH

Man proposes, God disposes.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACKNOWLEDGEMENTS

As I stand on the end of my doctoral studies, I have chance to reflect back on the long journey that has lead to me at this point. In my third year of elementary school in 1996, I traveled to U.S with my family. Since my father studied at UC Berkeley and MIT, I was able to visit many renowned universities. A strong impression on diverse discussions of various fields of studies, unparalleled quality of classes and resources and informal academic environment was a trigger for me to set a goal to study in U.S. During my middle school, I decided to study further on engineering, and my four-year-studies in undergraduates was the first step towards my dream. Being independent from my parents during my undergraduate years helped me to become self-reliant, and continuous aspiration on graduate studies led me to have a chance to join TICS group.

This dissertation would not have been completed without the help of encouragement of many people. First of all, I would like to thank my adviser Professor Gabriel M. Rebeiz for his guidance, support and encouragement my doctoral studies. As a entry-level student, his training and guidance was demanding at the beginning, however, such a series of processes are priceless lesson for me to learn how to 'think' as a independent researcher. I am also thankful to Prof. Gabriel M. Rebeiz allowing me to attend conferences all over the countries, expanding my knowledge of my profession and inspiring me to be exposed to many people from academia and industries and their technical experiences.

I also would like to thank my dissertation committee members, Prof. Gert Cauwenberghs, Prof. Drew Hall, Prof. William Hodgkiss Drew Hall, Prof. William Hodgkiss and Prof. Daniel Sievenpiper for their time, interest, and valuable comments.

No acknowledgment would be complete without recognizing TICS group members over five years. First, I must thank current TICS group members Qian Ma, Hasan Al-Rubaye, Kerim Kibaroglu, Eric Wagner, Umut Kodak, Bhaskar Rupakula, Li Gao, Yaochen Wang, Abdurrahman Alijuhani, Omar Elaasar, Ahmed Nafe, Tom Phelps, Yusheng Yin, Kevin Low, Siwei Li, and

Sultan Alqarni for their technical interactions and friendship. I would also like to thank previous TICS group members, Kevin Ho, Youngho Cho, Hyun-Ho Yang, Bon-Hyun Ku, Hsin-Chang Lin, Samet Zihir, Tümay Kanar, Seungdeok Ko, Abdullah Alazemi and Mustafa Sayginer for their help and support.

I also must thank Korean friends in UCSD and in San Diego. I would not have been able to complete my studies without their sincere encouragement, friendship, and support. My appreciation should go to Jayoung Kim, Jungmin Ha, Taeseok Oh, Byeongkeun Kang, Seongcheol Choi, Eric Kim, Junhee Park, Yonghee Han, Jongha Ryu, and Wanwoo Noh, to name only a few.

My research in RFIC field has begun with in my undergraduate senior research, with the help of Professor Byung-wook Min, a TICS group alumni, from Yonsei University, South Korea. The research experience under his guidance greatly increased my interest in RFIC design, motivating me to explore cutting-edge, fast changing RFIC world. Therefore, I would like to express my gratitude for his inspirational guidance and support.

Most of all, I would like to express my sincere thank to my parents and brother, Jee-Woong Chung, Young-Ja Kim, and Seunghwan Chung for their unconditional love and support. My life and doctoral studies in UCSD would have not been ever started without their devotion.

The material in this dissertation is based on the following papers which are either published, has been submitted for publication, or contains material that is currently being prepared for submission for publication.

Chapter 2, in part, is a reprint of the material as it appears in: H. Chung, Q. Ma, M. Sayginer, and G. M. Rebeiz, "A packaged 0.01−26 GHz single-chip SiGe reflectometer for two-port vector network analyzers", *IEEE International Microwave Symposium (IMS)*, June, HI, 2017, pp. 1259-1261. The dissertation author was the primary investigator and author of this paper.

Chapter 2 is also, in full, has been submitted for publication of the material as it may appear in: H. Chung, Q. Ma, M. Sayginer, and G. M. Rebeiz, "A packaged 0.01−26 GHz single-

chip SiGe reflectometer for two-port vector network analyzers", *IEEE Trans. Microw. Theory Techn.*, submitted. The dissertation author was the primary investigator and author of this paper.

Chapter 3, in full, is a reprint of the material as it appears in: B.-H. Ku, H. Chung and G. M. Rebeiz, "A 70-110 GHz Single-Chip SiGe Reflectometer with Integrated Local Oscillator Quadrupler", *IEEE International Microwave Symposium (IMS)*, June, HI, 2017, pp. 980-982. The dissertation author was the secondary investigator and second author of this paper.

Chapter 4, in part, is a reprint of the material as it appears in: H. Chung, Q. Ma, and G. M. Rebeiz, "A 10-40 GHz frequency quadrupler source with switchable bandpass filter and >30 dB harmonic rejection," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June, HI, 2017, pp.49-52. The dissertation author was the primary investigator and author of this material.

Chapter 4 is also, in full, has been submitted for publication of the material as it may appear in: H. Chung, Q. Ma, and G. M. Rebeiz, "A 10-40 GHz 4-channel frequency quadrupler with switchable bandpass filter and >30 dBc harmonic rejection with flip-chip packaging", *IEEE Journal of Solid-State Circuits)*, in preparation. The dissertation author was the primary investigator and author of this material.

Chapter 5, in part, contains material that is currently being prepared for submission for publication as may appear in: B.-H. Ku, H. Chung and G. M. Rebeiz, "A Milliwatt-Level $70-110$ GHz Frequency Quadrupler with 30 dBc Harmonic Rejection", *IEEE Trans. Microw.Theory Techn.*, in preparation. The dissertation author was the secondary investigator and second author of this material.

Chapter 6 is mostly a reprint of the material as it appears in: Q. Ma, H. Chung and G. M. Rebeiz, "A 4-Channel 10–40 GHz Wideband Receiver with Integrated Frequency Quadrupler for High Resolution Millimeter-Wave Imaging Systems", *IEEE International Microwave Symposium (IMS)*, June, PA, 2018, pp.883-886. The dissertation author was the secondary investigator and second author of this paper.

Chapter 7, in full, is a reprint of the material as it appears in: Q. Ma, H. Chung and G. M.

Rebeiz, “A low EVM SiGe BiCMOS 40–100 GHz direct conversion IQ modulator for multi-Gbps communications systems”, *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June, PA, 2018, pp.188-191, The dissertation author was the secondary investigator and second author of this paper.

Chapter 8, in full, is a reprint of the material as it appears in: Q. Ma, H. Chung and G. M. Rebeiz, “A 35–105 GHz high image-rejection-ratio IQ receiver with integrated LO doubler and $>$ 40 dB IRR”, *IEEE International Microwave Symposium (IMS)*, June, PA, 2018, pp.595-598. The dissertation author was the secondary investigator and second author of this paper.

VITA

2013	B. S. in Electrical and Electronics Engineering, Yonsei University, South Korea
2015	M. S. in Electrical Engineering, University of California San Diego
2018	Ph. D. in Electrical Engineering, University of California San Diego

PUBLICATIONS

H. Chung, Q. Ma, M. Sayginer, and G. M. Rebeiz, "A packaged 0.01−26 GHz single-chip SiGe reflectometer for two-port vector network analyzers", *IEEE Trans. Microwave Theory and Tech.*, submitted.

H. Chung, Q. Ma, and G. M. Rebeiz, "A 10−40 GHz 4-channel frequency quadrupler with switchable bandpass filter and >30 dBc harmonic rejection with flip-chip packaging", *IEEE J. Solid-State Circuits*, submitted.

B.-H. Ku, H. Chung, and G. M. Rebeiz, "A milliwatt-level 70−110 GHz frequency quadrupler with 30 dBc harmonic rejection", *IEEE Trans. Microwave Theory and Tech.*, in preparation.

H. Chung, Q. Ma, M. Sayginer, and G. M. Rebeiz, "A 0.01−26 GHz single-chip SiGe reflectometer for two-port vector network analyzers", *in IEEE International Microwave Symposium (IMS)*, HI, June, 2017, pp.1259−1261.

B.-H. Ku, H. Chung, and G. M. Rebeiz, "A 70−110 GHz single-chip SiGe reflectometer with integrated local oscillator quadrupler", *in IEEE International Microwave Symposium (IMS)*, HI, June, 2017, pp.980−982.

H. Chung, Q. Ma, and G. M. Rebeiz, "A 10−40 GHz frequency quadrupler source with swiatchable bandpass filter and >30 dBc harmonic rejection", *in IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, HI, June, 2017, pp.49−52.

Q. Ma, H. Chung, and G. M. Rebeiz, "A 4-channel 10−40 GHz wideband receiver with integrated frequency quadrupler for high resolution millimeter-wave imaging systems", *in IEEE International Microwave Symposium (IMS)*,PA, June, 2018, pp.883−886.

Q. Ma, H. Chung, and G. M. Rebeiz, "A 35−105 GHz high image-rejection-ratio IQ receiver with integrated LO doubler and >40 dB IRR", *in IEEE International Microwave Symposium Dig. (IMS)*, PA, June, 2018, pp.595−598.

Q. Ma, H. Chung, and G. M. Rebeiz, "A low EVM SiGe BiCMOS 40−100 GHz direct conversion IQ modulator for multi-Gbps communications systems", *in IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, PA, June, 2018, pp.188−191.

ABSTRACT OF THE DISSERTATION

Fully Integrated mm-wave ICs for High Performance Instrumentation Circuits and Systems

by

Hyunchul Chung

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2018

Professor Gabriel Rebeiz, Chair

The exponential growth of demands of simultaneous, multiple, high-speed and high-volume data transfer opens the new era, called 4th Industrial Revolution. A new wave of the fifth generation mobile communication systems (5G) and its ancillary industries such as autonomous vehicle, Internet-of-Things (IoT) and low-latency remote medical monitoring demand unprecedented solutions for both software platform and hardware designs. The requirement of hardware design, especially, is more stringent since the frequency band utilized for 5G will be in millimeter-wave region ($\sim$30 GHz), which will be more than $>$10 times higher than what we have currently employed. The development of mm-wave integrated circuits (ICs), therefore,

requires delicate characterization with sophisticated measurement and testing infrastructures. The research projects in this dissertation, in consequence, focus on different integrated mm-wave ICs for various instrumentation circuits and systems. These fully integrated mm-wave ICs were designed with the state-of-the-art performance considering the packaging effects (wirebond or flip-chip packaging) for wideband vector network analyzers (VNAs), signal generators, and modulator/demodulators.

Chapter 1

Introduction

1.1 Background

The upcoming fifth-generation (5G) era utilizes millimeter-wave, an electromagnetic signal with frequencies ranging from 30 to 300 GHz. These frequency ranges, in turn, results in the wavelength of 10 to 1 mm in the free space. Making use of mm-wave is considered as an inevitable way to resolve massive growth of connected mobile devices as well as significant increment in the data traffic volume. In fact, mm-wave region is readily capable of employing several GHz of bandwidth, which can support up to tens of Gb/s data rate. In contrast, the previous forth-generation (4G) communication system can only handle hundreds of Mb/s at most due to its limited bandwidth at sub-6 GHz. The breakthrough of $\sim$100 times higher data rate enables capabilities recently rising demands of near-perfect high-quality video streaming and real-time gaming.

Despite of its superior characteristics, due to mm-wave's physical limitations, few electronic devices were able to employ it as complete products until now. The mm-wave signals usually suffer from higher free space loss, atmospheric absorption and mechanical resonance of gaseous molecules in the air [1]. In addition, millimeter wave signals can be scattered by raindrops

due to its comparable size as the radio wavelengths. The more frequent lack of line-of-sight (LOS) connectivity created additional propagation loss compared with LOS transmission [2].

The obstacles also exist from the device and design perspective point of view. Continuous development of SiGe HBT (silicon-germanium hetero-junction bipolar transistor) and bulk, SOI (silicon-on-insulator), FDSOI (fully depleted SOI), and CMOS FET (complementary metal-oxide-semiconductor field effect transistor) provides higher RF performance (f_{T} and f_{MAX}) and high level of integration compared to previously used GaAs and InP technologies [3, 4]. However, due to aggressive down-scaling of the device, the transistors are much more vulnerable due to its lower break-down voltage (BDV) and lower available power per device. Furthermore, the use of mm-wave inevitably increases the parasitic effect and substrate loss which compensates the increased performance of transistors. The uncertainty of design that research/developer experience is also higher due to inaccurate model parameters provided by the foundry, less-precise 3-D electromagnetic simulation tools for passive and active devices, and higher chance of researcher/developer's imperfect modeling due to much more complicated design parameters.

Nevertheless, the demand of high-speed, high-data rate communication system is a strong driving factor of implementing fully integrated mm-wave circuits. Therefore, various research and development are actively in progress both in academia and industry at different frequency ranges in mm-wave region (Ka-,V-,E-,W-,D-, G-band).

1.2 Motivation

The rapid demands of mm-wave circuit design for next generation communication systems necessitate high-precision, high performance measurement equipment for accurate characterization. The test equipment such as vector network analyzer (VNA), signal generator and spectrum analyzers are still highly employed in order to verify electronic performance of device-under-test (DUT). However, compared to the previous test and measurement procedures, which mostly

requires DUT's conventional parameters, such as S-parameters, 1-dB compression point and output power, recent requirement of measurement in both academia and industry not only include these conventional parameters mentioned above, but also require complex parameters, such as AM-AM, AM-PM distortion, I/Q amplitude/phase mismatch, phase noise, image rejection, error vector magnitude (EVM), and bit-error-rate (BER) of different modulation conditions at mm-wave frequencies.

The specification for the test equipment is usually extremely stringent in order not to limit the measurement result by the test equipment setup. Furthermore, widespread demands of mm-wave devices also require easy, portable, cost-effective measurement setups. Therefore, the reduction in size, weight, cost while maintaining the high performance of the measurement instruments is essential in order to cope with the new wave of 5G era.

1.3 Thesis Overview

This thesis presents fully integrated mm-wave circuits for high performance instrumentation circuits and systems in SiGe technology.

Chapter 2 presents a packaged SiGe BiCMOS reflectometer for two-port vector network analyzers (VNA) operated at $0.01-26$ GHz. The reflectometer chip is composed of a bridge coupler and two wideband heterodyne receivers for coherent magnitude and phase detection. For wideband operation, a low-loss high-directivity resistive bridge coupler is implemented. In addition, a high-linearity receiver channel is designed so as to accommodate $\sim$20 dBm of RF input power to the reflectometer. A pair of external sources are used to provide stimulus over the entire bandwidth, and high-linearity shunt 50 Ω switch is placed at the input of each reflectometer chip to provide a matched condition for better measurement accuracy. The measured dynamic range of the heterodyne receiver is 129 ± 3 dB at 0.01–26 GHz with an IF resolution bandwidth (RBW) of 10 Hz. The reflectometer chip is bonded on a low-cost printed circuit board (PCB) with

multi-stage matching networks, and connecterized for repeatable measurements. Several passive and active device-under-test (DUTs) such as filters and amplifiers are measured in single- and dual-port complex S-parameter setup at 0.01–26 GHz. The single-chip reflectometer results in excellent agreement with commercially available test equipment, and with minimal magnitude and phase difference. Several definitions (mean deviation, EV) are used to quantify the measurement accuracy. The measured S_{21} of -80 dB is observed with high-rejection filter. An in-depth dynamic range analysis of possible limiting factors of the measurement setups is also addressed.

Chapter 3 presents a 70–110 GHz single-chip SiGe reflectometer for one-port vector network analyzer. Two directional couplers are implemented together with two high-linearity heterodyne receivers on a single chip at 70-110 GHz. In addition, a x4 frequency multiplier chain is also implemented on the same chip. A CPW (Coplanar Waveguide) coupled-line directional is used with a shielded ground plane for improved isolation and directivity. The dynamic range of the receiver is 110–115 dB at 70–110 GHz with 10 dB back-off and 10 Hz resolution bandwidth (RBW). The SiGe chip is 5.86 mm^2 and consumes 440 mW from a 2 V supply. The chip is mounted on a printed circuit board (PCB), and RF and LO signals are applied using probes. A 95 GHz bandpass filter is measured as the device-under-test (DUT) and the results obtained using the on-chip VNA and a commercial VNA show good agreement over a wide frequency range.

Chapter 4 presents a 4-channel $10-40$ GHz frequency quadrupler with GF8HP 0.12-μm SiGe BiCMOS process. For wideband operation, three independent bands (low-, mid-, and high-band) are implemented with band selection switch. Frequency multiplication is done by cascading frequency doublers, and multiple harmonics generated by each frequency doublers are suppressed by on-chip bandpass filters located after the first and the second frequency doubler. However, the large fractional bandwidth (FBW) of each bands about $\sim$45 % inevitably has one of the dominant harmonics being located in-band of the bandpass filters, resulting in significant degradation of harmonic rejection ratio (HRR). Therefore, this work introduces an on-chip 3-pole/2-zero switchable elliptic bandpass filter to control the passband to locate the undesired harmonics

out-of-band at given input frequency. This results in greatly improved HRR with minimum number of bands used. After multiplier chain, a 1:4 driver stage is designed to achieve OP_{1dB} of $\sim$ 5 dBm. The chip is flipped and placed on the low-cost printed circuit board (PCB), with connecterized interfaces for repetitive measurements. The measurement of P_{out} and harmonics are +3 dBm with $>$ 30 dBc worstcase HRR at $10-40$ GHz. The worstcase HRR remains same from -3 to +3 dBm P_{out}. The chip is 8.03 mm^2 and consumes $296-320$ mW for 4-channel operation. This work, to author's knowledge, is the first to introduce the on-wafer switchable bandpass filter for wideband frequency multiplier of FBW $>$100% with flip-chip packaging. This work can be implemented with various systems at rising interest of mm-wave application with high signal purity.

Chapter 5 presents a 2-channel $70-110$ GHz wideband frequency quadrupler in GF8HP 0.12 μm SiGe BiCMOS process. The x4 frequency multiplication is achieved based on cascaded frequency doubler and inter-stage bandpass filter is implemented to reject adjacent undesired harmonics. Two inter-stage amplifiers are also implemented to drive enough power to the second frequency doubler and boost output power. The measured peak output power is -1.5 to 2.9 dBm from $70-110$ GHz, with the worstcase harmonic rejection ratio (HRR) of $>$ 29 dBc. The chip is 1.9 mm^2 and consumes 240 mW for 2-channel/ 170 mW for 1-channel operation with the input power of 0 dBm. To authors' knowledge, this work represents state-of-the-art in terms of bandwidth, output power with great HRR. It can be utilized high frequency LO source for various applications such as point-to-point communication, automotive radar (E-band), and high-resolution imaging system (W-band).

Chapter 6 presents a wideband 4-channel 10–40 GHz receiver (RX) with integrated LO quadrupler and flip-chip packaging in GF8HP 0.12 μm SiGe BiCMOS technology. The system-level measurements are done with the chip flipped on a low cost RF board. Each receiver channel results in 20–37 dB power conversion gain with a 3-dB RF gain bandwidth (BW) of 10–40 GHz. The measured single-sideband noise figure (SSB NF) and input P1dB at the center frequency of

25 GHz are 9.3 dB (and 8.2 dB) and -17.2 dBm (and -33 dBm), respectively, at low (and high) gain mode. Frequency-modulated-continuous-wave (FMCW) experiment at 15–27 GHz shows the capability of detecting 2 objects with a separation of 1.3 cm.

Chapter 7 presents a 40–100 GHz wideband direct conversion IQ modulator with IQ correction capability and flip-chip packaging in GF8HP 0.12μm SiGe BiCMOS technology. The modulator chip covers Q-, V-, E-, and W-bands and is flipped on a low-cost RF board for connecterized measurements. The measured IQ modulator conversion gain is $5-8$ dB at $40-100$ GHz with an OP1dB of -2 to -5 dBm. A single-sideband (SSB) rejection higher than 42 dBc and an LO leakage rejection better than 35 dBc is measured. A 64-QAM modulated waveform with a data rate of 12 Gb/s (2Gbaud/s) and 2.4% error vector magnitude (EVM) is successfully demonstrated at 72 GHz. To our knowledge, this modulator achieves state-of-the-art performance in terms of bandwidth, wideband SSB rejection, and EVM at multi-Gbps data rate, and with applications in millimeter-wave high data-rate 5G systems.

Chapter 8 presents a 35–105 GHz wideband direct conversion IQ receiver and a 30–105 GHz IF receiver with integrated LO doubler in GF8HP 0.12-μm SiGe BiCMOS technology. Both receiver chips covers Q-, V-, E-, and W-bands and are flipped on a low cost RF board for connecterized measurements. The IQ receiver presents a measured flat conversion gain of 21–33 dB at 35–105 GHz and a double-sideband (DSB) noise figure (NF) of 5–12 dB. With the on-chip I/Q phase-error correction, the IQ receiver maintains better than 40 dBc image-rejection-ratio (IRR) over the entire bandwidth. The IF receiver demonstrates a measured flat conversion gain of 18–33 dB at 30–105 GHz with a similar NF as the IQ receiver. Both receivers have greater than 5 GHz IF (baseband) bandwidth.

Chapter 2

A Packaged 0.01−26 GHz Single-Chip SiGe Reflectometer for Two-Port Vector Network Analyzers

2.1 Introduction

Vector network analyzers (VNA) are essential and versatile pieces of test equipment used to characterize the RF performance of any device-under-test (DUT), by measuring scattering matrix of single, dual, and multi-port systems. Various applications related to electronics at RF, microwave [5–8], and millimeter-wave frequencies [9–12] rely on accurate S-parameter measurements. Moreover, vector analysis is essential in the measurement of complex dielectric properties of materials in numerous research fields such as material characterization and biomedical sensing [13–15]. However, due to the vector network analyzer's high-cost, high-volume and considerable weight, most of vector analysis has been limited to stationary laboratories. With growing demands for low-cost portable test equipment and flexible measurements, a reduction in size, weight and cost while maintaining high performance and accuracy becomes an essential

breakthrough for expediting the next-generation test systems.

Several approaches for low-cost network analysis have been introduced in the past decades. The non-coherent topology such as non-linear transmission line (NLTL) technology and time-domain sampling enables a compact design up to 100 GHz region and allows magnitude and phase information using essentially scalar power measurements [16, 17]. Six-port reflectometer (SPR) architecture has been deeply investigated up to now, due to its simple structure based on power meters and relatively low-cost [18–20]. Quasi-optical scalar network analysis using sinuous antennas and harmonic mixing was also introduced in [21, 22] for $15-50$ GHz and >100 GHz applications. However, all of these approaches are generally bulky and suffer from harmonics that cannot be eliminated, resulting in lower dynamic range (typically $50-60$ dB). In general, the standard approach based on frequency conversion circuits and coherent detection still results in the highest performance network analyzers and is the corner stone of all S-parameter measurement techniques.

There are only a limited number of publications addressing integrated chipsets for vector analysis, and with the capabilities of measuring complex S-parameters with high dynamic range [23–26]. A dedicated chipset at $50-100$ GHz is reported in [23] with integrated frequency synthesizer and an external PLL. A $70-110$ GHz reflectometer design with integrated LO frequency quadrupler is introduced in [24]. A miniaturized VNA design at $4-32$ GHz range is recently addressed in [25, 26]. The work in [23–26] paves the way for vector analysis with multi-channel heterodyne receivers, but the measurement setup shown in [23] still requires a dedicated probe station, and further measurements are necessary in [24] to characterize two-port vector analysis. Also, while [25, 26] show excellent one- and two-port S-parameter measurements with high accuracy, the frequency of operation is limited to 4 GHz.

This paper is an extended version of [27], and consists of following sections. In Section 2.2, the VNA system architecture of VNA and realization are presented. With a brief technology description (Section 2.3), the circuit blocks in the reflectometer chip are introduced in Section

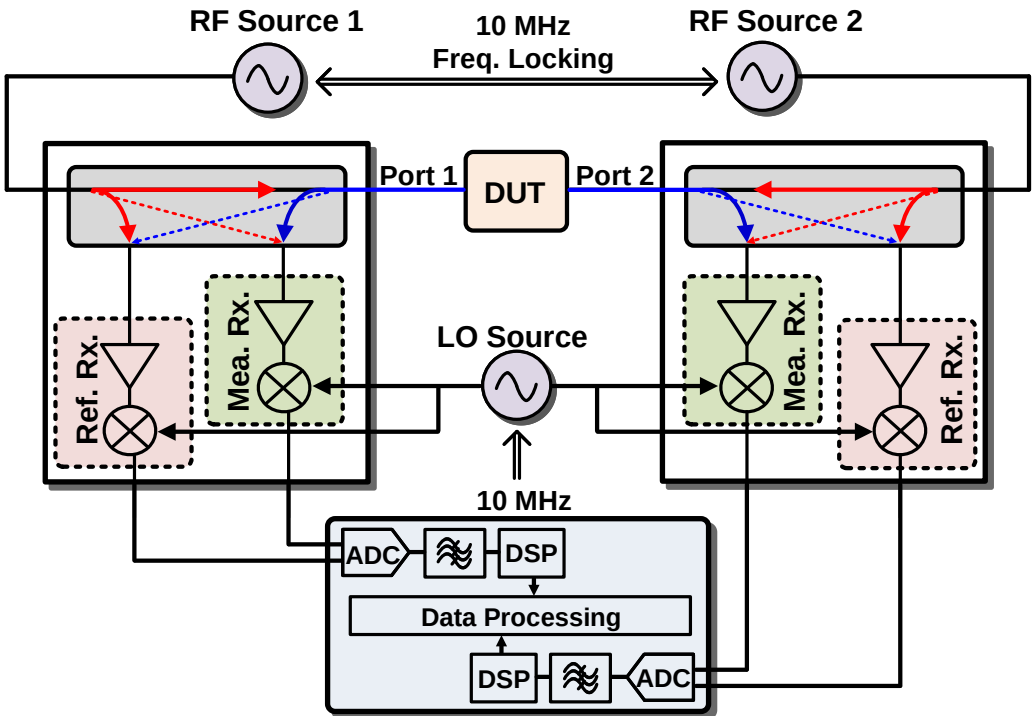


Figure 2.1: Block diagram of two-port vector network analyzer. A single RF source and a high isolation single-pole double-throw (SPDT) can also be used instead of two RF sources.

2.4. The measured chip performance and receiver dynamic range is shown in Section 2.5 and 2.6, followed by the details of a dedicated PCB design (Section 2.7). The concept of one- and two-port calibration is introduced in Section 2.8. In Section 2.9 and Section 2.10, several one- and two-port DUT measurements are presented with an in-depth discussion of the limitations caused by the measurement setup.

2.2 VNA Architecture

Fig. 2.1 presents simplified block diagram of a vector network analyzers with 4 main building blocks: 1) directive coupler, 2) multi-channel heterodyne receiver, 3) signal generation component, and 4) digital back-end. The directive coupler is realized using a directional coupler or a resistive bridge coupler, and separates the incident and reflected waves. The separated signals are then fed into two heterodyne receivers (reference channel and the measurement channel) and

down-converted to an intermediate frequency (IF). Analog-to-digital converters (ADCs) digital filtering for easier amplitude and phase measurement.

In addition, a RF source is needed to excite the device-under-test (DUT). A single RF source with a very high isolation switch (>100 dB) is typically used in commercial VNA due to its compact design, but separate signal sources with frequency locking can also used for improved isolation. Finally, the down-converted IF signals are sampled by analog-to-digital converters (ADCs) to retrieve the magnitude and phase of the measured signal from each receiver channel. Further mathematical processing is performed by dedicated computational unit to reconstruct the DUT S-parameters.

Fig. 2.2 presents details of reflectometer chip for a two-port vector network analyzer. When RF source 1 is activated, it couples through the bridge coupler followed by reference channel receiver. The propagated signal is not intended to couple to the measurement channel receiver, however, due to finite directivity of the bridge coupler, a small amount of signal is leaked into the measurement channel receiver. After bridge coupler, the signal is either transmitted or reflected by the amount of (Γ or τ), where Γ and τ are the reflection and transmission coefficient of DUT. The reflected signal is now coupled to measurement channel receiver (leakage to reference channel is now undesirable) and the amount of signal measured at the output of each receivers is gathered to reconstruct Γ. In a similar manner, the transmitted signal is now coupled to the measurement channel in the second reflectometer, and the amount of signal measured is obtained to calculate τ.

The heterodyne receivers are implemented as a differential design and with a high input P1dB, since a relatively large RF signal (up to 20 dBm) is generally sent from the RF source. The signal level into the reference channel is much higher than the measurement channel, resulting in unequal powers in each channels which can degrade the measurement accuracy unless a large IP1dB is used for the reference channel. The down-converted IF signal is amplified by an IF amplifier with a 3-dB bandwidth of 40 MHz) or an IF amplifier with 3-dB BW of 2.5 GHz,

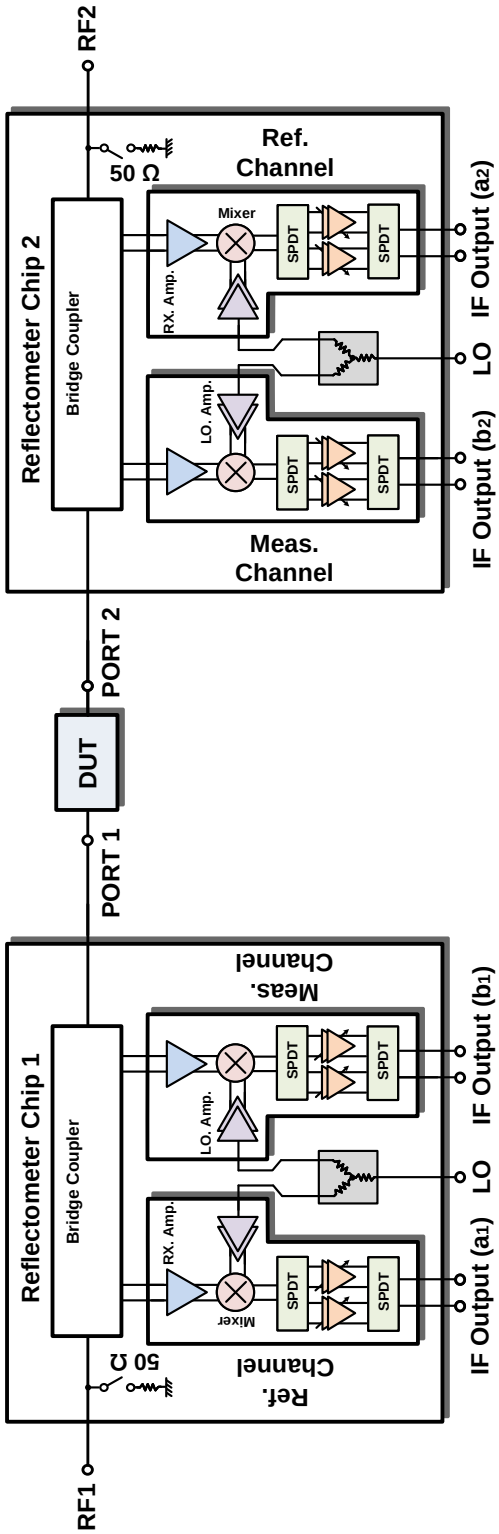


Figure 2.2: VNA system realization with two reflectometer chips.

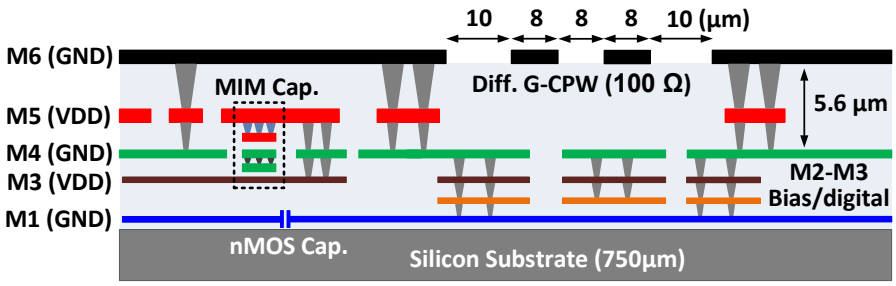


Figure 2.3: Cross section of the TowerJazz SBC18H3 technology.

selected by a single-pole double-throw (SPDT) switch. In general, the IF signal of a commercial VNA is between $5-20$ MHz. However, when a fast measurement response is required (such as a pulse-mode or to measure the turn-on S-parameters of an amplifier), and IF bandwidth of $2-3$ GHz can be used. The 4 differential IF outputs (a_1, b_1, a_2, b_2) are simultaneously sampled by external ADCs with a fast enough sampling rate to reconstruct the complex S-parameters.

Also, a 50 Ω shunt switch is placed before the resistive bridge coupler in each reflectometer chip to provide a matched condition when the RF signal is excited from the other direction. (i.e., the switch in reflectometer chip 1 is turned on when the RF signal is applied from the reflectometer chip 2).

An RF amplifier is also used before the mixer with the main purpose to isolate LO leakage from the mixer to the measurement channel port, resulting in reduced measurement accuracy. An isolation of ~ 40 dB is desired to sufficiently suppress LO-to-RF leakage. Also, wideband LO driver with an active balun are implemented to drive the mixers. The LO drivers also act as isolators and greatly attenuate the mixer RF-to-LO leakage between the reference channel and the measurement channel.

2.3 Technology

The reflectometer chip is designed using TowerJazz SBC18H3 0.13-µm SiGe BiCMOS process with 6-layer metal back-end-of-line (BEOL) (Fig. 2.3). The f_T and f_{MAX} of a 10-µm

HBT transistor is 220−230 GHz, referenced to the top metal (M6). A 100-Ω differential coplanar waveguide (CPW) transmission line (10−8−8−8−10 μm) is implemented with patterned ground planes (M1, M4, M6). Additional 0.18-μm CMOS transistors are also available for digital control and biasing. The simulated 100-Ω differential CPW transmission line loss is 0.35 dB/mm at 26 GHz with transmission line Q of 18. Measurements of line loss agree well with simulations [28].

2.4 Reflectometer Design

2.4.1 Resistive Bridge Coupler

Due to the wideband operation at DC−26 GHz, a resistive bridge coupler is used (Fig. 2.4a) [29]. The design is extremely small when integrated on-chip (70 ×160 μm) and with a nearly frequency-independent response. The coupling ratio is chosen to -25 dB in order to handle RF input power of up to +20 dBm and to set the reference channel input P1dB to -5 dBm. so that the following receiver input 1-dB compression point is -5 dBm. The elegant design shown in [29] uses single-ended signal and DUT ports, and results in differential ports for the reference and measurement channels. It also achieves low insertion loss and high directivity. The resistance values are obtained by using

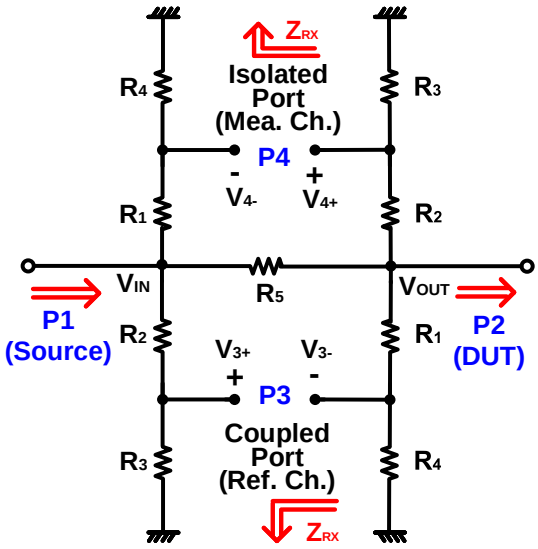
$$\frac{V_{\mathrm{IN}}-V_{3+}}{R_2}=\frac{V_{3+}}{R_3}+\frac{V_{3+}-V_{3-}}{Z_{\mathrm{Rx}}} \tag{2.1}$$

$$\frac{V_{\mathrm{OUT}}-V_{3-}}{R_2}=\frac{V_{3-}}{R_4}-\frac{V_{3+}-V_{3-}}{Z_{\mathrm{Rx}}} \tag{2.2}$$

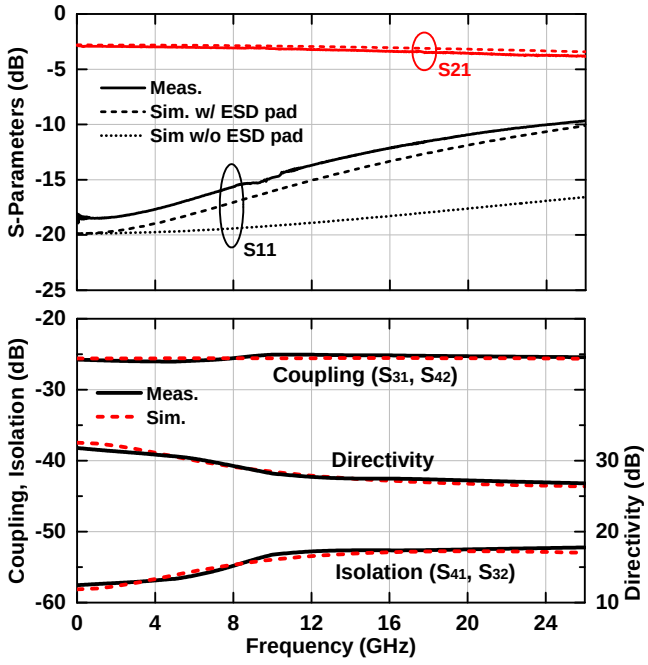
$$\frac{V_{\mathrm{IN}}-V_{4-}}{R_1}=\frac{V_{4-}}{R_4}-\frac{V_{4+}-V_{4-}}{Z_{\mathrm{Rx}}} \tag{2.3}$$

$$\frac{V_{\mathrm{OUT}}-V_{4+}}{R_2}=\frac{V_{4+}}{R_3}+\frac{V_{4+}-V_{4-}}{Z_{\mathrm{Rx}}} \tag{2.4}$$

$$\frac{V_{\mathrm{OUT}}-V_{\mathrm{IN}}}{R_5}+\frac{V_{\mathrm{OUT}}-V_{3-}}{R_1}=-\frac{V_{\mathrm{OUT}}-V_{4+}}{R_2}-\frac{V_{\mathrm{OUT}}}{R_o} \tag{2.5}$$



(a)



(b)

Figure 2.4: Resistive bridge coupler : (a) Schematic, and (b) insertion loss, return loss, coupling, isolation and directivity.

where Z_{Rx} is the differential impedance of the coupled (Ref. Channel) or isolated (Meas. Channel) port (100 Ω) and R_o= 50 Ω. The insertion loss (IL), coupling ratio (C) and isolation (I) are derived from (2.1)−(2.5) and are

$$IL = \frac{g + \frac{2acd}{be-c^2}}{f - \frac{1}{be-c^2}(bd^2 + a^2e)} \tag{2.6}$$

$$C = \frac{1}{be-c^2}[a(e-c) + d(c-b)IL] \tag{2.7}$$

$$I = \frac{1}{be-c^2}[d(b-c) + a(c-e)IL] \tag{2.8}$$

where $a = 1/R_2$, $b = 1/Z_{\mathrm{Rx}} + 1/R_2 + 1/R_3$, $c = 1/Z_{\mathrm{Rx}}$, $d = 1/R_1$, $e = 1/Z_{\mathrm{Rx}} + 1/R_1 + 1/R_4$, $f = 1/R_1 + 1/R_2 + 1/R_5 + 1/R_o$, and $g = 1/R_5$, respectively. Using (2.1)$-$(2.8), the calculated IL, C and I are -1.9 dB, -24 dB, and -62 dB, and R_1, R_2, R_3, R_4, R_5 are equal to 196 Ω, 144 Ω, 288 Ω, 235 Ω, and 9 Ω, respectively.

The simulated and measured insertion loss of a bridge-coupler test cell are 2.5 dB and 2.8$-$3.5 dB, respectively, with simulated return loss of $<$-17 dB up to 26 GHz (Fig. 2.4b). Note that the measured return loss rises to $\sim$ -10 dB due to the electrostatic discharge (ESD) diode capacitance placed at the RF pad. Additional simulations with ESD diode model agrees well with measurements. The measured coupling ratio and isolation at 0.01$-$26 GHz are -25 dB and -57 to -52 dB, respectively, resulting in directivity of 27$-$32 dB. In general, a directivity of 20$-$30 dB is considered excellent in network analyzers, and the integrated design is superior to off-chip directional couplers. The simulated S_{43} (leakage between two channels) is -35 dB.

2.4.2 Low-Gain/High Isolation RF Amplifier

Fig. 2.5a presents the low-gain, high isolation differential amplifier placed after the resistive bridge coupler. A resistive input matching is used for wideband operation, and an emitter degeneration resistor of 20 Ω is employed to improve the input compression point. After the first-stage cascode amplifier, a two-stage DC level shifter is implemented to lower the common-mode voltage so as to be compatible with the passive mixer (no DC blocks are allowed due to wideband

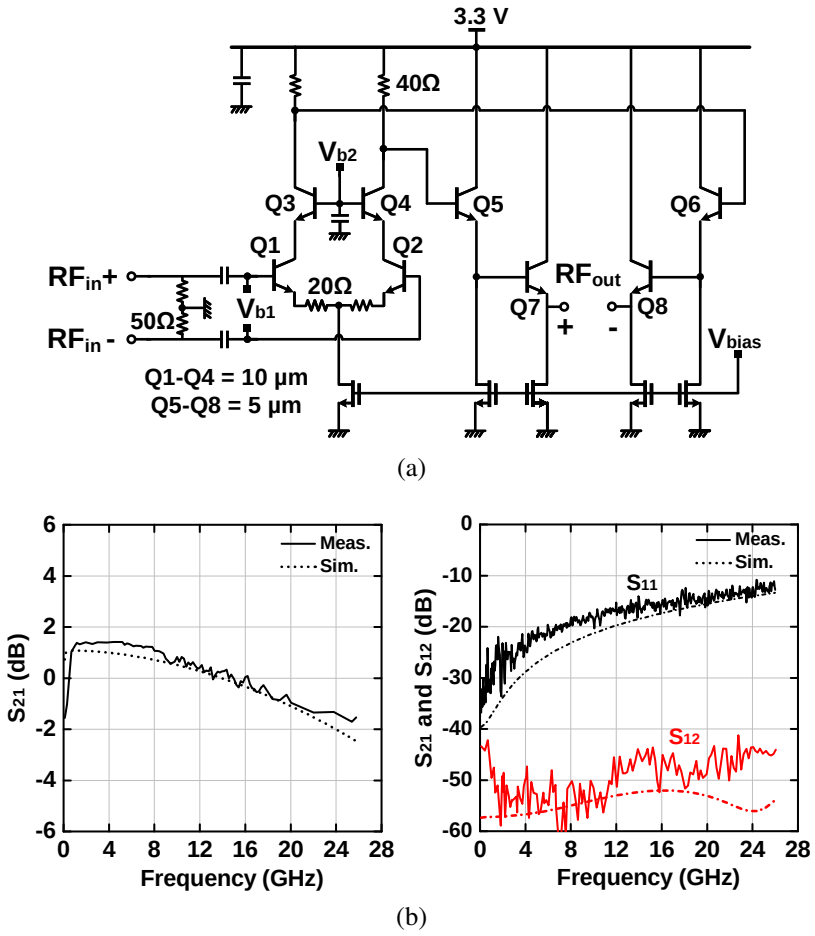
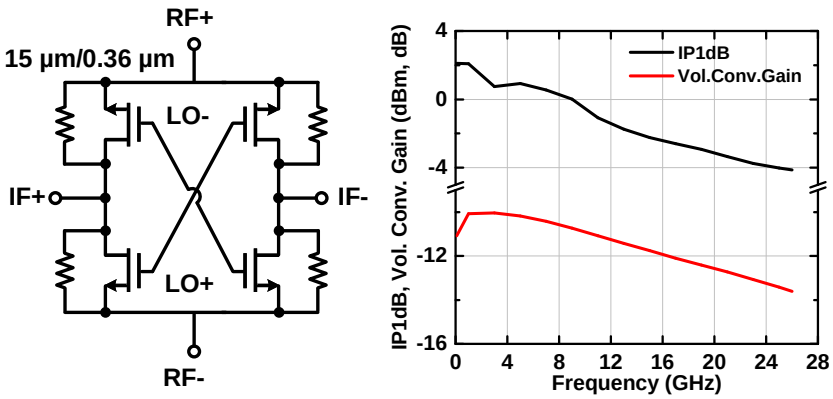


Figure 2.5: High-linearity RF amplifier:(a) schematic, and (b) S_{21}, S_{11} and S_{12}.

operation). The amplifier current consumption is 22.5 mA from a 3.3 V supply.

Fig. 2.5b presents the measured S_{21} with value of +2 to -1 dB up to 26 GHz, and with a 3-dB BW of 26 GHz. The lower-edge 3-dB BW is determined by the input series DC block capacitance (5 pF) and is 15 MHz. The measured S_{12} is <-40 dB up to 26 GHz, which is enough to suppress any LO-to-RF leakage from the mixer. The measured S_{11} is <-10 dB up to 26 GHz. The simulated IP1dB is 0.5 to -6.5 dBm at $0.01-26$ GHz, and the reduced IP1dB at high frequencies is due to limited bias current in the first-stage of DC level shifter. In hindsight, more bias current should have been used in the DC level shifter to maintain a constant IP1dB over frequency. The simulated noise figure is $10-12$ dB at $0.1-26$ GHz, and increases to 18 dB at 10 MHz due to the DC block capacitor.



(a) (b)

Figure 2.6: Double balanced passive mixer: (a) schematic and (b) simulated IP1dB and voltage conversion gain.

2.4.3 Passive Mixer

The passive mixer is designed for wideband operation as well as for handling a high RF power from the previous stage. A differential double-balanced structure is chosen for good LO-IF and RF-IF isolation, with compact, symmetrical, and inter-digitated layout to minimize imbalances as well as common-mode leakage (Fig. 2.6a) [30]. The simulated mixer voltage conversion gain and IP1dB at 0.01−26 GHz are -10 to -14 dB, and +2 to -4 dBm, respectively with IF load of 200 Ω (Fig. 2.6b). The LO swing (V_{pp}) at the mixer gate varies between 2.2 and 1 V from 0.01−26 GHz, however, the conversion gain does not vary significantly for LO voltages above 1 V. Thick oxide transistors are used in this design to handle high DC and AC gate voltage (V_g=2.1 V/ V_{pk}=1.2 V). The simulated mixer single-sideband (SSB) NF is 12−14 dB at 0.01−26 GHz.

2.4.4 IF Amplifiers

The passive mixer is followed by two different IF amplifiers. The low-frequency IF amplifier is a fully differential Miller operational transconductance amplifier (OTA) with common-mode feedback and 19 dB gain control (Fig. 2.7a). A 1 kΩ load impedance is used for ADC

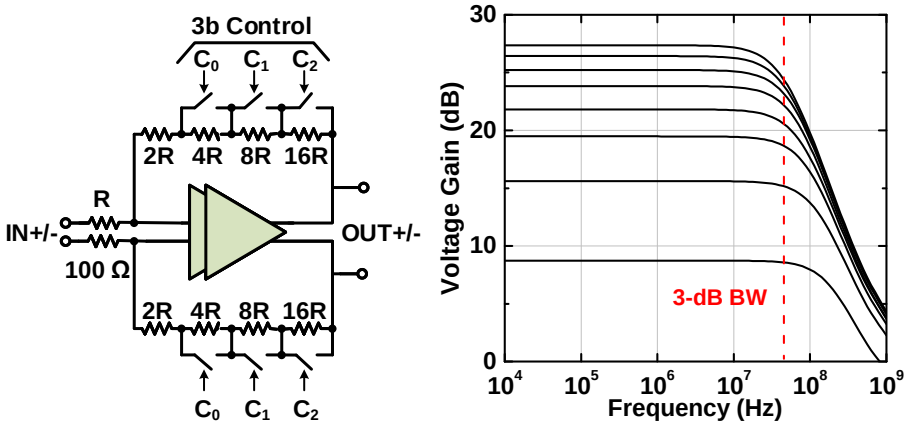


Figure 2.7: Low frequency operational transconductance amplifier (OTA): (a) a three-bit gain control and (b) its simulated gain.

block input impedance. The amplifier voltage gain is 9−27.5 dB with a 3-dB bandwidth of 40 MHz (Fig. 2.7b). The simulated OP_{1dB} at the maximum gain state is 4 dBm with a 1 kΩ load.

Fig. 2.8a presents the high-frequency IF amplifier. The design is based on a cascode and a common emitter (CE) stage with an inter-stage level shifter, and gain control is achieved by current steering method [31]. The simulated voltage gain is -1 to 19 dB with a differential 100 Ω load used to represent the wideband ADC (Fig. 2.8b).

2.4.5 50 Ω Shunt Switch

The operation principle of the 50 Ω shunt switch placed before at the RF source input is shown in Fig. 2.9a. When the RF signal is applied from port 1, the shunt switch is turned off to pass the signal, and the measured insertion loss is 0.1−2 dB at 0.01−26 GHz (Fig. 2.9b). On the other hand, when the RF signal is applied from port 2 to measure S_{12} or S_{22}, the 100 µm transistor results in on-resistance of 18 Ω, which together with the 35 Ω series resistance, shows a resulting in simulated S_{11} <-20 dB up to 26 GHz (Fig. 2.9b). However, the measured S_{11} is -10 dB at 26 GHz due to the ESD diode at the RF port. The measured shunt switch input P1dB is 15−18 dBm at 0.01−26 GHz and agrees well with simulations.

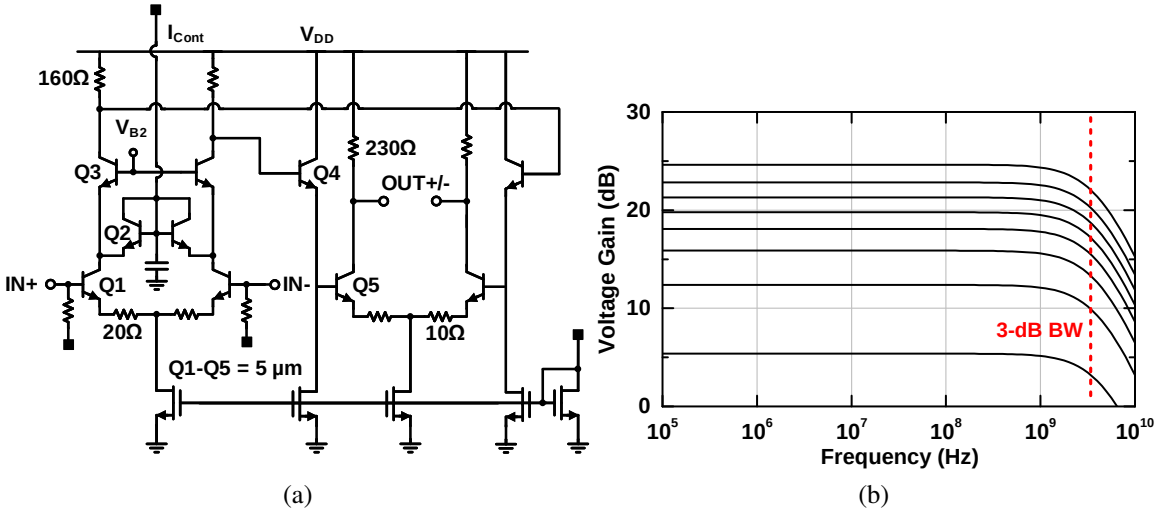


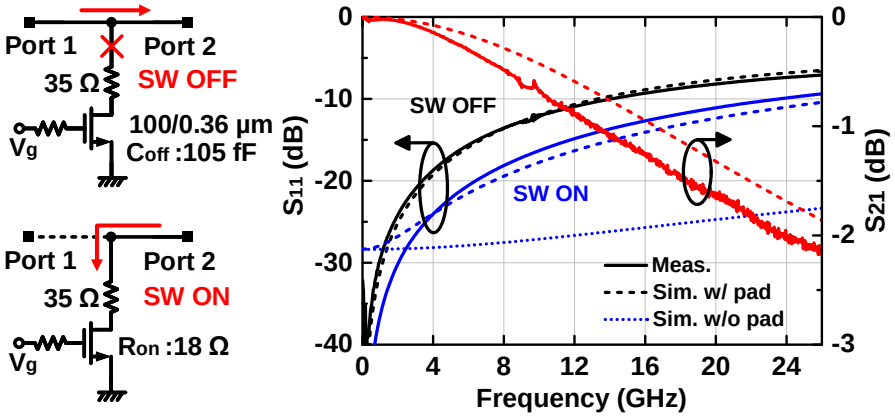
Figure 2.8: High frequency IF amplifier: (a) schematic and (b) simulated voltage gain.

2.4.6 LO Driver

The wideband LO driver is shown in Fig. 2.10a. The single-ended LO input is converted to a differential signal using a resistively-matched active balun, and an additional gain stage is employed to maximize the voltage swing at the mixer. The simulated saturated peak-to-peak output voltage ($V_{g\text{-}pp}$) is 2.5−1 V at 0.01−26 GHz (Fig. 2.10b) , due to the frequency roll-off effect of the inductorless design. However, as noted before, the mixer conversion gain does not change significantly for $V_{g\text{-}pp} > 1$ V. The required LO power to drive mixer is -3 to -12 dBm. The output LO voltage for input LO power of -5 dBm is basically a square-wave at 1−10 GHz due to highly saturated operation, and becomes close to sinusoidal at 26 GHz. The simulated small signal gain is 18−10 dB, with an reverse isolation of <-50 dB at 0.01−26 GHz.

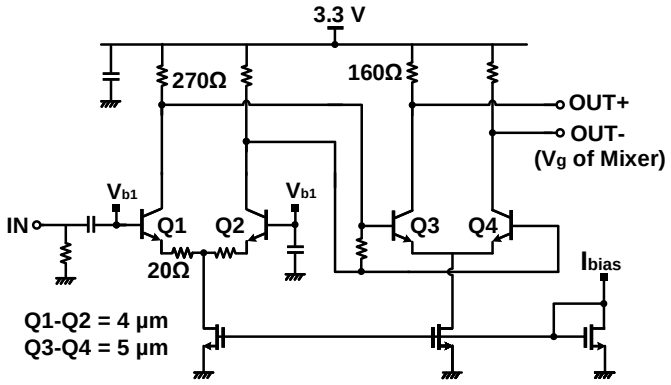
2.4.7 Receiver Simulations

Fig. 2.11a presents the receiver block diagram. A differential 100 Ω RF signal is applied from the bridge coupler, and a 1 kΩ and 100 Ω load impedance are used for the low- and high IF amplifier. The simulated voltage conversion gain at 0.01−26 GHz is 18.5−15 dB (low IF) and 8 to 5 dB (high IF) in the maximum gain state. The simulated SSB receiver NF is 19−22 dB (low

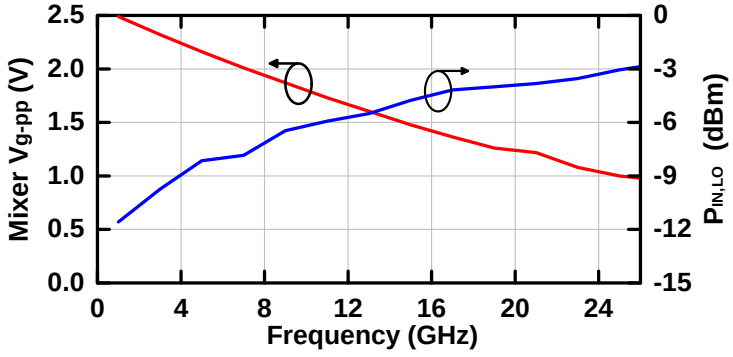


(a) (b)

Figure 2.9: 50 Ω shunt switch: (a) switch on and off case, and (b) measured and simulated S-parameters.

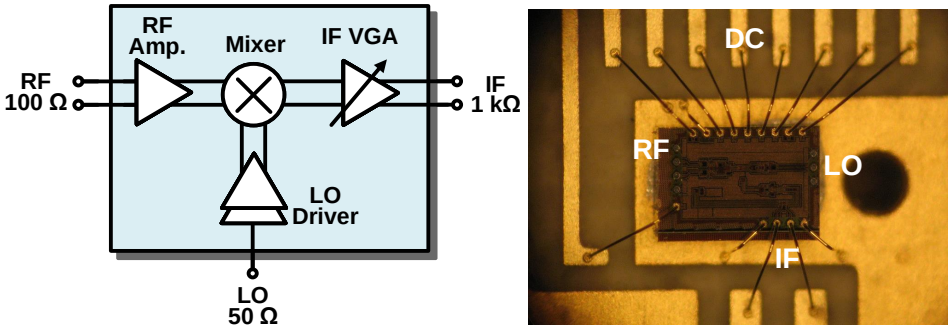


(a)



(b)

Figure 2.10: Two-stage LO driver : (a) schematic, and (b) $V_{g\text{-}pp}$ and LO power to drive the mixer vs frequency.



(a) (b)

Figure 2.11: Heterodyne receiver: (a) block diagram, and (b) assembled chip for RF and LO probing (DC and IF bonded only).

IF), and 21−25 dB (high IF), respectively, and the IP1dB is -4 to -8 dBm (low IF), and -10 to -8 dBm (high IF).

2.4.8 RF-to-LO and LO-to-RF isolation

The effect of RF-to-LO and LO-to-RF leakage is critical in reflectometer design and should be minimized. First, the RF signal leaked through the mixer is substantially suppressed by the two-stage LO driver which has a reverse isolation of -50 dB (Fig. 2.12). However, since there is little isolation between two LO paths from the resistive T-junction, any RF signal leaked from one channel will be amplified and present at the mixer of the other channel, as shown path (A) in Fig. 2.12. Based on simulated RF-to-LO feedthrough in mixer (<-40 dB)and reverse isolation (-50 dB) with forward gain of 10−18 dB in the current system, the effective RF-to-LO leakage is in the range of -80 to -72 dB, and is mixed with the LO signal (red dot-line). This effect, however, cannot be solely measured due to 1) direct path from bridge coupler (S_{41} of -52 dB, path (X)), 2) imperfect S_{11} of the 50 Ω termination (path (Y)). Besides, another RF-to-LO leakage path exists which passes through the T-junction and propagates to the other reflectometer LO port through the external splitter. This effect can be estimated by measuring b_2 signal (path (B)), as b_2 can be only generated by mixing LO signal with the RF leakage in path (B). The measurement result

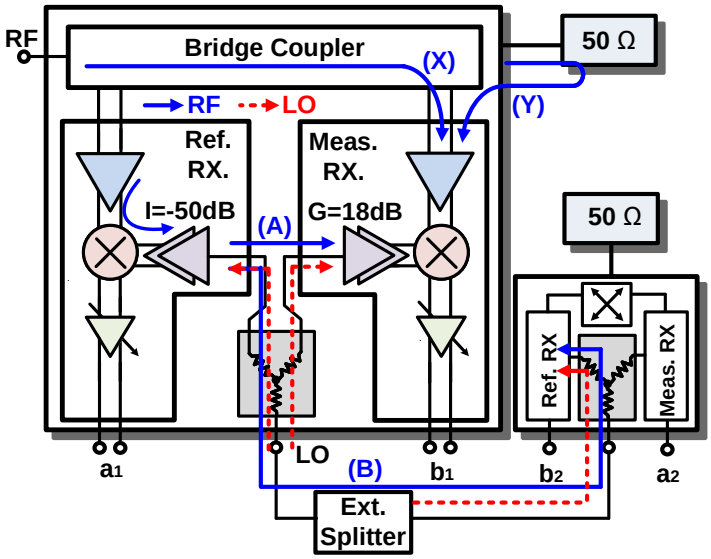


Figure 2.12: Graphical viewgraph of RF-to-LO leakage paths.

with an in-depth analysis will be discussed in section2.10.1.

Fig. 2.13 presents two paths of LO-to-RF leakage. The large LO swing (3−5 dBm) at the output of LO driver leaks through mixer by -40 dB. With 35 dB isolation between Ref. Rx. and Meas. Rx. in the bridge coupler (See section) and an additional -40 dB isolation of RF amplifier, the LO signal at both paths (A1, A2) are significantly suppressed (∼ -100 dB) and can be negligible.

2.5 Receiver Measurements

The stand-alone receiver chip microphotograph is shown in Fig. 2.11b. The RF and LO signals are applied through 100 µm pitch GSSG and GSG probe, and IF outputs are wire-bonded and routed out on the PCB. The power conversion gain is measured using the Keysight PNA-X 5247A (differential 100 Ω input and output configuration), and the measured power gain is then transferred to a voltage gain to 1 kΩ.

Fig. 2.14a presents the measured voltage conversion gain versus IF gain control at

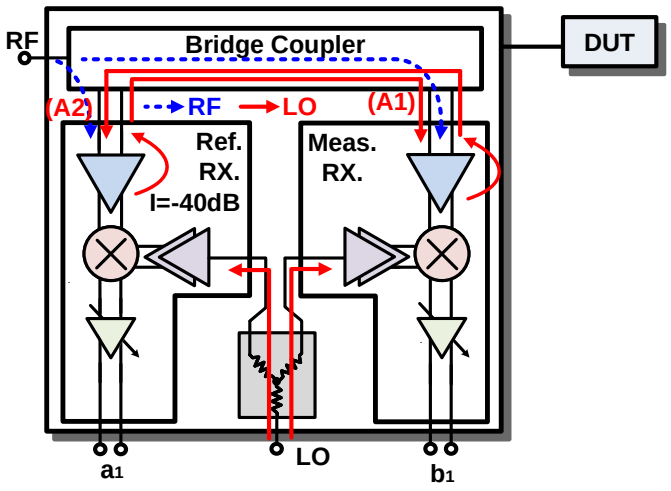


Figure 2.13: Graphical viewgraph of LO-to-RF leakage paths.

0.01−26 GHz for the maximum gain state. The measured IP_{1dB} with a 1 kΩ load is -4 to -9 dBm and 0 to -9 dBm for the maximum and minimum gain states, respectively (Fig. 2.14b). Note that the receiver IP_{1dB} at the maximum gain state is limited by the IF amplifier. For minimum gain state, the IP1dB follows that of the first-stage RF amplifier. The receiver SSB NF is also measured using Keysight PNA-X 5247A with a single-ended input and output using external balun (all the passive loss is de-embedded after the measurement). The measured SSB NF is 22−26 dB, and 26−30 dB at the maximum and minimum gain state, respectively, and is 2−3 dB higher than simulations. The difference between simulations and measurements with a system NF of 20 dB is within the error range. The voltage conversion gain versus IF frequency is also measured and shows a 3-dB bandwidth of 40 MHz (Fig. 2.14c), and agrees well with simulations. The required LO power to drive mixer is -5 to +2 dBm at 0.01−26 GHz.

A similar set of measurements was done with the high-IF amplifier, and the measured voltage conversion gain at 0.01−26 GHz is 6.5−2 dB with 100 Ω load at the maximum gain state. The measured IP1dB and NF at the maximum gain state is -9 to -6 dBm, and 24−28 dB, respectively, again 2−3.5 dB higher than the simulation. The measured 3-dB bandwidth of high-IF receiver is 2.5 GHz for the maximum gain state, agreeing well with simulations.

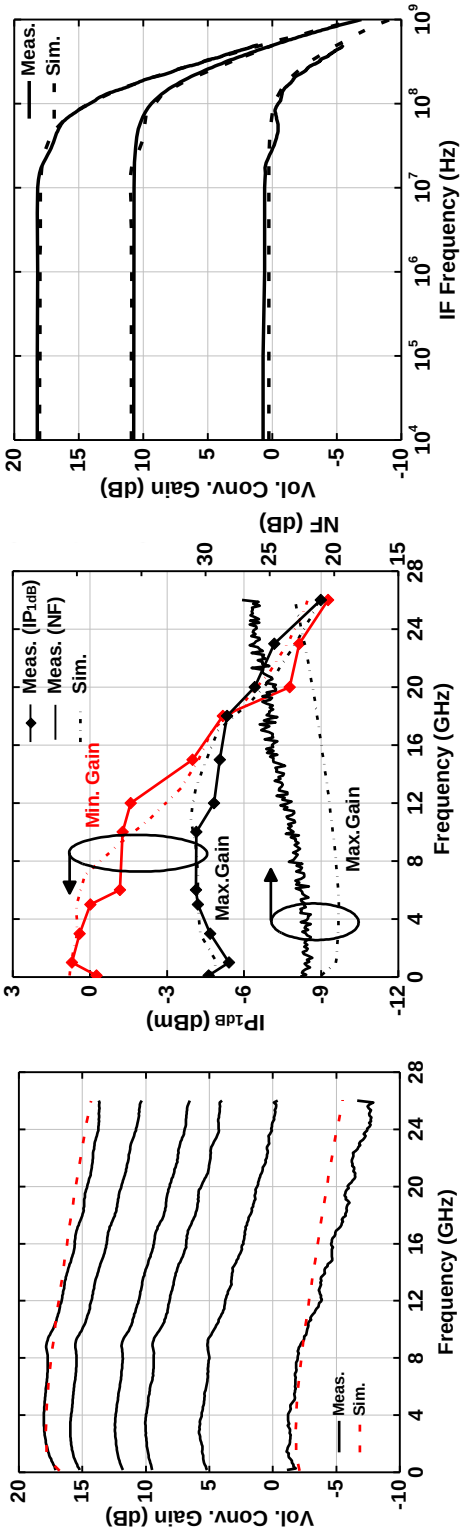
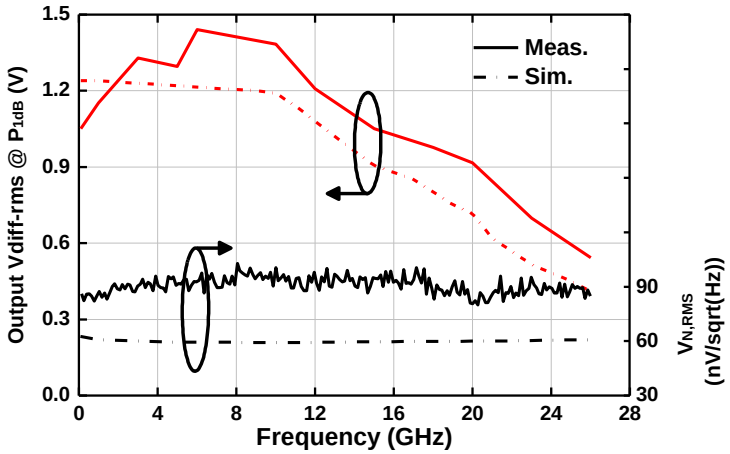
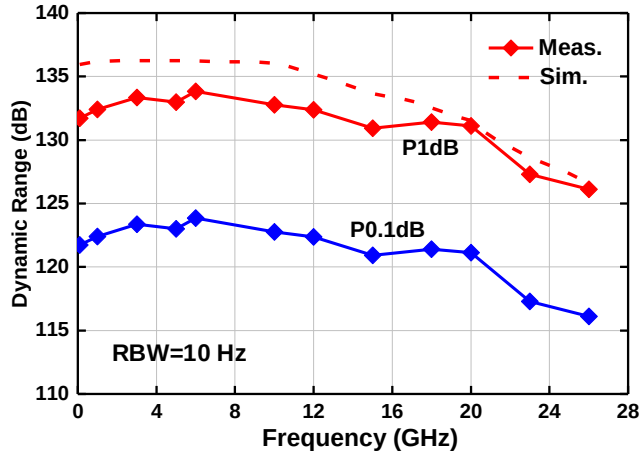


Figure 2.14: Measured receiver performance: (a) voltage conversion gain, (b) IP1dB and NF, and (c) IF bandwidth (low-IF).



(a)



(b)

Figure 2.15: Receiver output noise voltage and dynamic range: (a) measured output $V_{diff\text{-}RMS}$ and RMS output noise voltage, and (b) dynamic range of the receiver.

2.6 Dynamic Range Calculations

The receiver dynamic range (DR) is derived by measuring the difference between the RMS IF output power for the reference channel driven at the 1-dB compression point, and the IF RMS noise floor. A resolution bandwidth (RBW) of 10 Hz is used, which is the nominal value for commercial VNAs. However, since the receiver output is directly connected to ADC (voltage domain), the dynamic range is defined as the ratio of the differential IF RMS voltage ($V_{diff\text{-}RMS}$) at the 1-dB compression point and the IF RMS noise voltage ($V_{N,RMS}$). The IF RMS

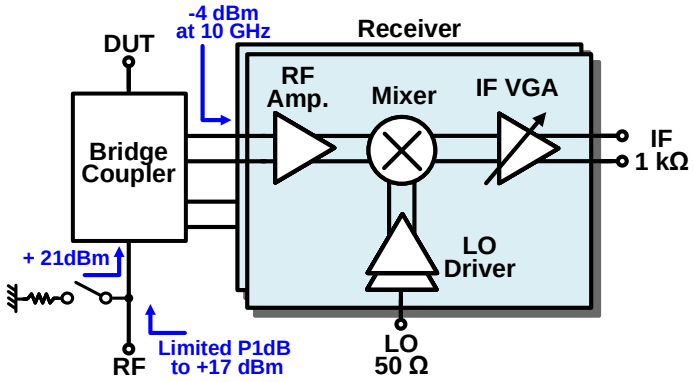


Figure 2.16: Derivation of reflectometer IP1dB.

noise voltage ($V_{N,RMS}$) is calculated by using

$$V_{N,RMS} = V_{NS,RMS} \times 10^{[(NF_{SSB}+VCG)/20]} \tag{2.9}$$

where $V_{NS,RMS}$ is the thermal noise voltage with 1 Hz bandwidth at room temperature (290 K) in 50 Ω system (0.89 nV/$\sqrt{\text{Hz}}$), NF_{SSB} is SSB NF of the receiver, and VCG is the voltage conversion gain of the receiver. The simulated and measured $V_{diff\text{-}rms}$ and $V_{N\text{-}RMS}$ at 0.01−26 GHz are 1.2−0.4 V (1.4−0.54 V), and 58−63 nV/$\sqrt{\text{Hz}}$ (81−98 nV/$\sqrt{\text{Hz}}$), respectively (Fig. 2.15a), resulting in measured dynamic range of 133−126 dB with a RBW of 10 Hz (Fig. 2.15b).

The dynamic range is desirable to be same as the receiver dynamic range, however, in practice, is lower due to limitations from other circuit blocks. In this case, and due to input absorptive switch IP1dB of 15−18 dBm (Fig. 2.16), the measured reflectometer dynamic range at 0.01−26 GHz is 133−126 dB with a 10 Hz RBW, which is 4 dB lower than the receiver dynamic range.

A stricter dynamic range definition is based on P0.1dB, which is the 0.1 dB compression point. In most cases, P0.1dB is P1dB-10 dB. Using this definition, the reflectometer dynamic range is 123−116 dB at 0.01−26 GHz in a 10 Hz RBW (Fig. 2.15b).

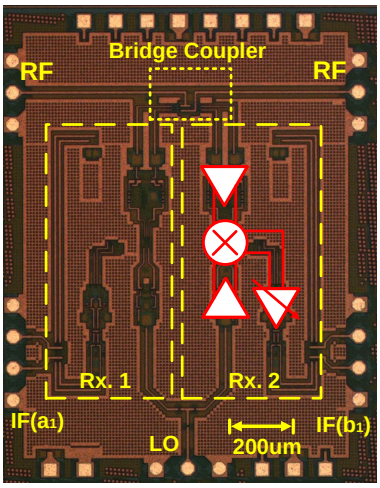
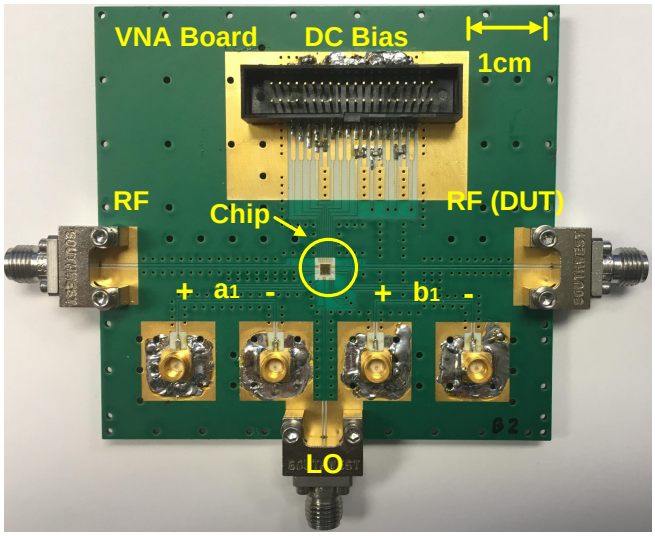
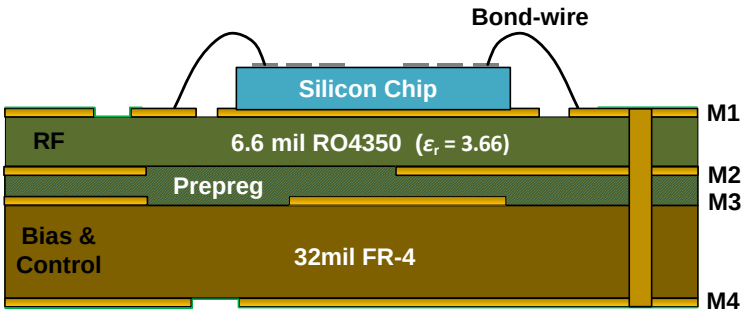


Figure 2.17: Chip microphotograph of 0.01−26 GHz reflectometer (1.5×1.2 mm^2).



(a)



(b)

Figure 2.18: (a) Chip-on-board of 0.01−26 GHz reflectometer, and (b) PCB stackup.

2.7 Chip-on-board packaging

The reflectometer chip microphotograph is shown in Fig. 2.17. The chip area is 1.8 mm^2 with a power consumption of 640 mW from a 3.3 V supply. The compact size of the chip is due to an inductorless design.

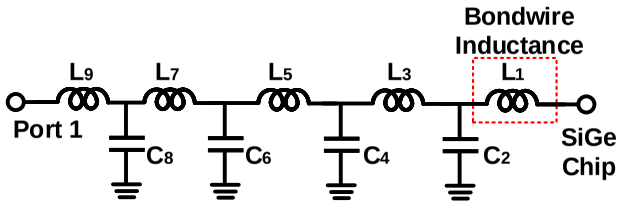
This chip is placed on low-cost RF laminate (RO4350B, ε_r = 3.66, $\tan\delta$ = 0.004 at 10 GHz) with a thickness t=6.6 mil (0.168 mm). A 0.75 mm FR-4 is also used for DC biasing as well as mechanical support (Fig. 2.18b). The RF and DC pads are connected to the PCB using bond-wires and G-CPW transmission lines are routed on the top layer to end-launch connectors (Fig. 2.18a). The transmission-line length for each RF and LO path is around 3 cm and is mainly limited by the physical dimensions of the IF surface-mounted connector. The measured transmission line loss is 0.68 dB/cm at 26 GHz (W=13.2 mil, S=8 mil), and is higher than simulations due to metal roughness of the top layer ($1-2$ μm) and extra loss from the solder mask which are not modeled. Due to the wideband operation and high bondwire reactance (L_{bw}= 0.6 nH, X_{bw}= $j114$ Ω at 26 GHz), a multi-stage open-stub matching network is implemented for wideband operation up to 26 GHz (Fig. 2.19a). The network is modeled using lumped elements (L, C) as

$$L_k = \frac{g_k Z_k}{\omega_0} \quad (k : \text{odd}) \tag{2.10}$$

$$C_k = \frac{g_k}{Z_k \omega_0} \quad (k : \text{even}) \tag{2.11}$$

where g_k is the filter coefficient, Z_k is the characteristic impedance of each stub (k =$1-9$), ω_o is the cutoff frequency (26 GHz), and L_k,C_k are the series inductance and shunt capacitance, respectively [32, 33]. Assuming L_{bw}=L_1= 500 pH, then g_1=1.7 with 9th order Chebyshev filter (0.5 dB ripple) is chosen. These lumped elements (L_k, C_k) are then transformed as shown in Fig. 2.19b.

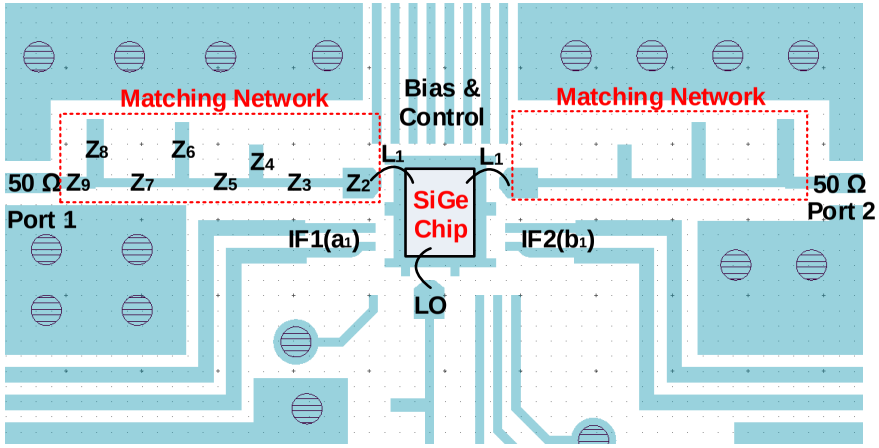
The simulated insertion loss and return loss of the bond-wire transition for L_{bw}= $500-700$



Transformed Stub Impedance and electrical lengths

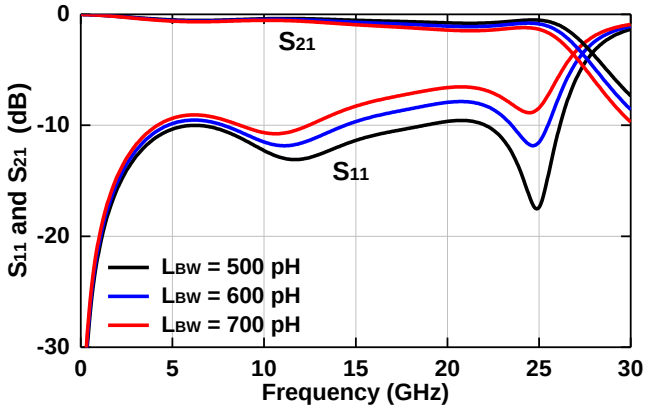
i	2	3	4	5	6	7	8	9
$Z_i(\Omega)$	50	100	85	100	85	100	77	90
$\theta_i(°)$	27	70	32	60	50	72	50	38

(a)

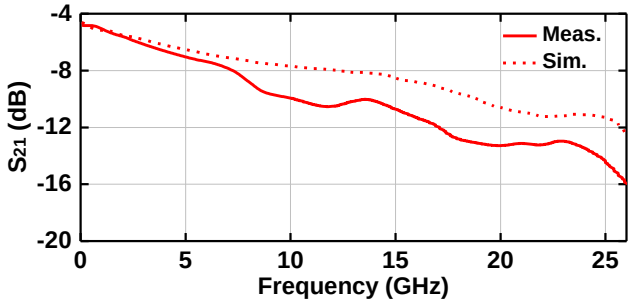


(b)

Figure 2.19: (a) Multi-stage stub design for wideband matching network , and (b) layout of RF lines on PCB near the SiGe chip area.



(a)



(b)

Figure 2.20: (a) Simulated S_{21} and S_{11} of matching network with different bond-wire inductances, and (b) measured S_{21} of reflectometer chip and chip-on-board including packaging effect.

pH is 0.5−1.35 dB and <-8 dB, respectively up to 25 GHz (Fig. 2.20a). The measured S_{21} of the chip-on-board (COB) reflectometer with connecterized RF ports is shown in Fig. 2.20b. The measured S_{21} can be broken as : 1) 0.05−3.8 dB $\times$2 for the input and output transmission-line loss, 2) 0.05−0.7 dB $\times$2 for the end-launch connectors at 0.01−26 GHz, and 3) 4.6−6.8 dB loss for the SiGe reflectometer chip. A similar matching network is implemented on LO path (not shown for brevity), and the two differential IF outputs of multi-channel receivers are routed out through surface-mounted connectors (Fig. 2.18a).

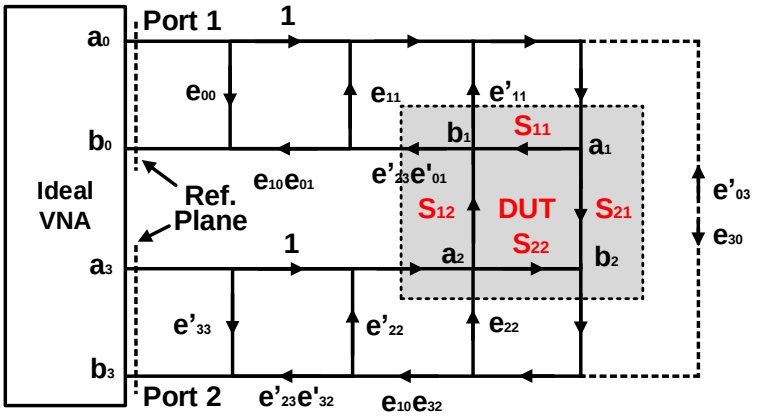


Figure 2.21: Graphical viewgraph of 12-term error components.

2.8 Calibration

Calibration is required to determine the systematic error terms surrounding the measurement setup. The conventional 12-term error matrix is used for two-port calibration, and Fig. 2.21 presents a graphical description of the error terms [34, 35]. For one-port calibration, three error terms can be resolved by measuring three well-known OSL (open, short, load) standards. Due to inherent imperfection of these standards, their reflection coefficients are not perfect (i.e., $\Gamma_{S,O} \neq 1$, $\Gamma_{S,S} \neq -1$, $\Gamma_{S,L} \neq 0$) and this can introduce calibration errors. Therefore, the reflection coefficients of the three standards ($\Gamma_{S,O}$, $\Gamma_{S,S}$, $\Gamma_{S,L}$) are first independently pre-measured using a commercial VNA. The three error terms (e_{00}, e_{11}, $e_{10}e_{01}$) are then obtained as

$$e_{00} + \Gamma_{S,O}\Gamma_{M,O}e_{11} - \Gamma_{S,O}\Delta_e = \Gamma_{M,O} \tag{2.12}$$

$$e_{00} + \Gamma_{S,S}\Gamma_{M,S}e_{11} - \Gamma_{S,S}\Delta_e = \Gamma_{M,S} \tag{2.13}$$

$$e_{00} + \Gamma_{S,L}\Gamma_{M,L}e_{11} - \Gamma_{S,L}\Delta_e = \Gamma_{M,L} \tag{2.14}$$

$$\Delta_e = e_{00}e_{11} - e_{10}e_{01} \tag{2.15}$$

where Γ_M ($\Gamma_{M,O}$, $\Gamma_{M,S}$, $\Gamma_{M,L}$) is the measured reflection coefficient using the reflectometer

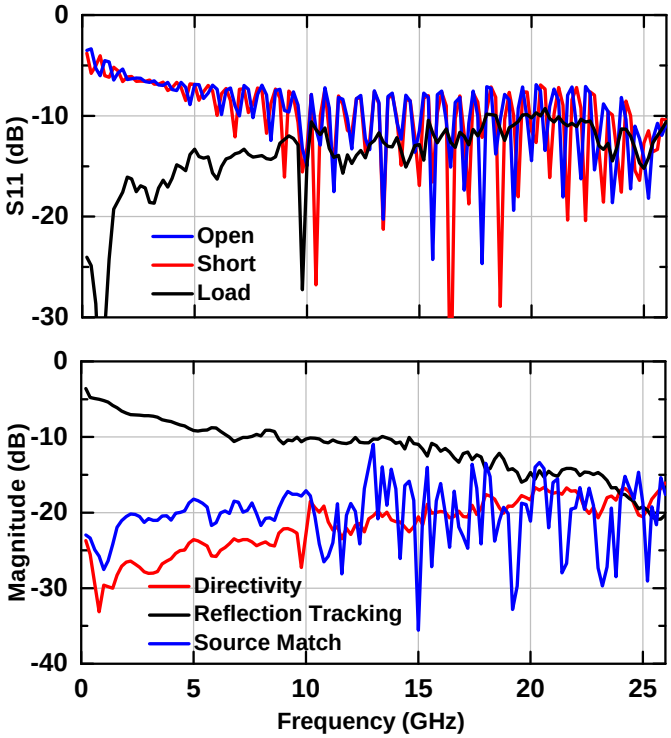


Figure 2.22: Measured reflection coefficient of open, short and load ($\Gamma_{M,O}$, $\Gamma_{M,S}$, $\Gamma_{M,L}$), and one-port calibration coefficients (directivity, reflection tracking and source match).

chip, and e_{00}, e_{11}, and $e_{10}e_{01}$ are the three systematic error term which are referred to as directivity, source match, and reflection tracking. Fig. 2.22 presents the measured reflection coefficient of the OSL standards ($\Gamma_{M,O}$, $\Gamma_{M,S}$, $\Gamma_{M,L}$), and includes the three systematic error terms. Due to the wideband response of the bridge coupler, a $>$20 dB directivity is present up to 15 GHz, and is reduced to 16 dB at 20$-$26 GHz due to the output transmission-line loss. The measured source match is $<$ -10 dB at 0.01$-$26 GHz. The reflection tracking is $\sim$ 4.5 dB at 1 GHz, and increases to -22 dB at 26 GHz, due to higher packaged loss.

For two-port calibration, there are 12-error terms that need to be resolved. Individual one-port OSL calibration at each port provides 6 error terms (directivity, source match and reflection tracking) and two-port thru calibration provides additional 4 error terms (transmission

tracking and source match). The derivation is

$$S_{11,\mathrm{M}} = e_{00} + e_{10}e_{01}\frac{S_{11} - e_{22}\Delta_s}{1 - e_{11}S_{11} - e_{22}S_{22} + e_{11}e_{22}\Delta_s} \tag{2.16}$$

$$S_{21,\mathrm{M}} = e_{30} + e_{10}e_{32}\frac{S_{21}}{1 - e_{11}S_{11} - e_{22}S_{22} + e_{11}e_{22}\Delta_s} \tag{2.17}$$

$$S_{12,\mathrm{M}} = e'_{03} + e'_{23}e'_{01}\frac{S_{12}}{1 - e'_{11}S_{11} - e'_{22}S_{22} + e'_{11}e'_{22}\Delta_s} \tag{2.18}$$

$$S_{22,\mathrm{M}} = e'_{33} + e'_{23}e'_{32}\frac{S_{22} - e'_{11}\Delta_s}{1 - e'_{11}S_{11} - e'_{22}S_{22} + e'_{11}e'_{22}\Delta_s} \tag{2.19}$$

$$\Delta_s = S_{11}S_{22} - S_{21}S_{12} \tag{2.20}$$

where $S_{ij,M}$ (i and j=1, 2) is the measured transmission coefficient when a thru standard is connected, and S_{ij} is the pre-measured S-parameter of the thru standard.

Finally, the two crosstalk error terms (e_{30}, e'_{03}) are determined by measuring the transmission coefficient in the forward and reverse direction where both test ports are terminated to in 50 Ω. However, the effect of crosstalk error is negligible for the most applications, and therefore, this measurement is omitted during calibration (e_{30}=e'_{03}=0).

With two one-port OSL and a two-port thru calibration, the 10-error terms are extracted at each RF frequency and are used to retrieve the DUT S-parameter. [34]. There are a couple of other error model, such as 8- or 16-error models, however, these can be also derived from the 12-term model [36, 37].

2.9 One-port S-Parameter Measurements

The one-port S-parameter measurement setup is shown in Fig. 2.23. Separate signal generators are used for the RF and LO signals, and the relatively low b_1 signal is connected to an external VGA for added signal gain. The IF signals (a_1, b_1) are simultaneously sampled by an Agilent U2531A with a maximum sampling rate of a 2MS/s, and the digital processing is done

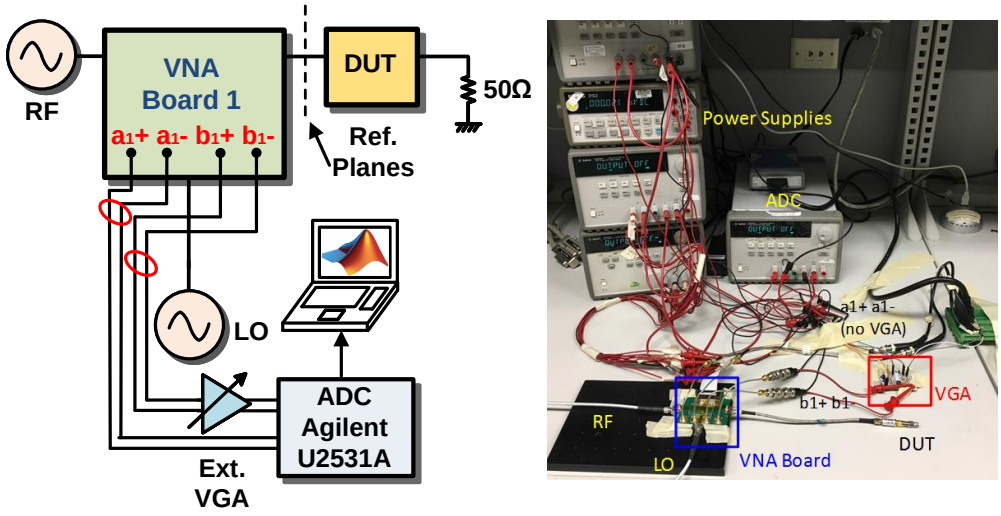


Figure 2.23: One-port S-parameter measurement setup.

using MATLAB software. An IF of 200 kHz to 500 kHz is typically used. The DUT is placed at the connecterized RF port (Ref. plane), and an one-port OSL calibration is performed to calibrate the reflectometer board.

Fig. 2.24 presents the one-port DUT measurement of a 50 Ω load up to 26 GHz. The measured S_{11} using the SiGe chip VNA (red dots) shows excellent agreement with high-performance VNA measurements (Agilent E8361A, blue line). The S-parameter difference for magnitude and phase is also shown in Fig. 2.24 (right axis). Its maximum amplitude and phase difference is $<$ 0.6 dB, $<$ 5°, respectively. Note that the amplitude and phase difference in dB scale is high only when S_{11} is very low ($<$-25 dB).

Fig. 2.25 presents S_{11} measurements on a Ku-band horn antenna. The return loss agrees well with commercial VNA system, and with the maximum amplitude and phase difference of $<$0.7 dB, $<$4.5°.

The mean deviation, defined as the average amplitude and phase difference in dB and

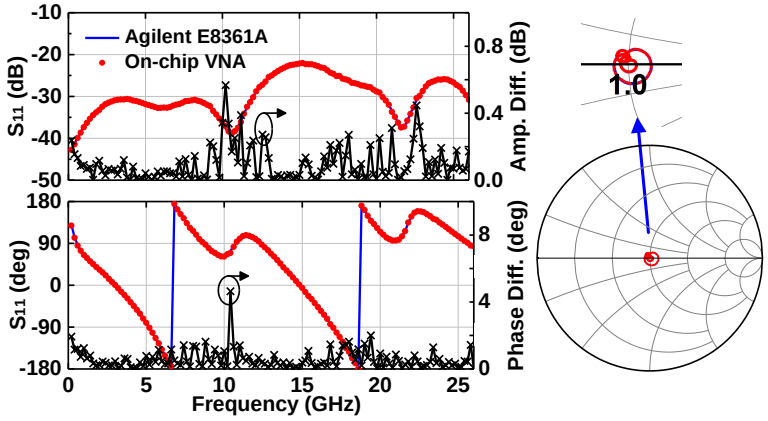


Figure 2.24: Measurement comparison of S_{11} by commercial VNA and on-chip VNA of 50 Ω load.

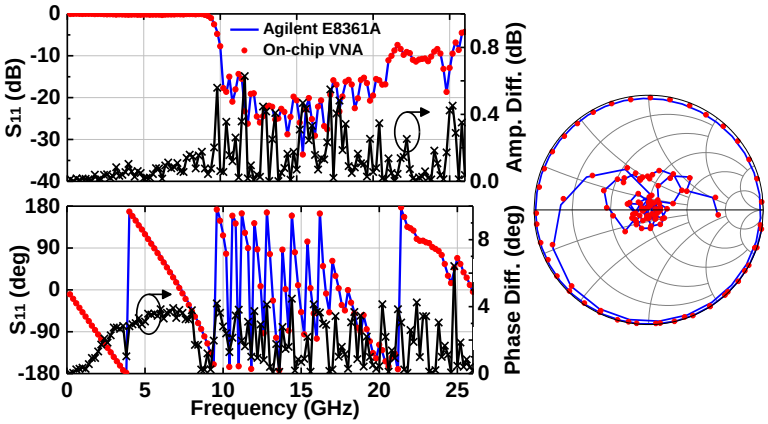


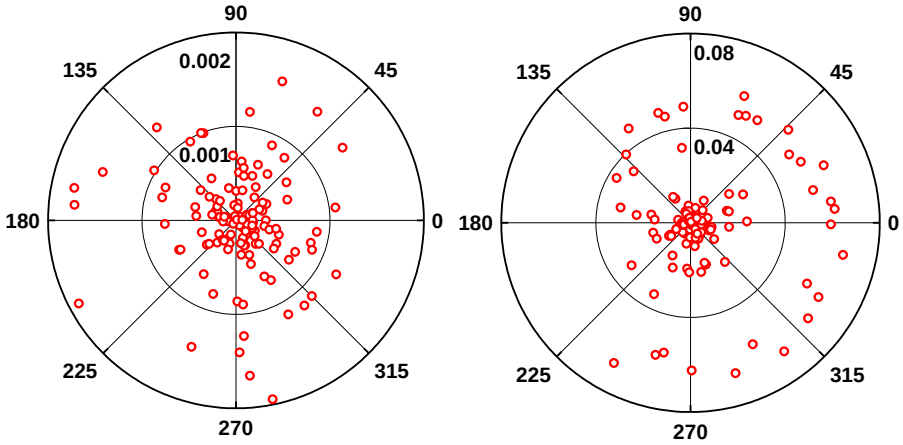
Figure 2.25: Measurement comparison of S_{11} by commercial VNA and on-chip VNA of Ku-band horn antenna.

degree ($\overline{|\Delta S_{11}|}$), is

$$\overline{|\Delta S_{11,\text{load}}|} = 0.09\text{dB}\angle 0.54^\circ \tag{2.21}$$

$$\overline{|\Delta S_{11,\text{antenna}}|} = 0.14\text{dB}\angle 1.92^\circ \tag{2.22}$$

However, the amplitude and phase difference in dB scale is not appropriate to determine the quality of measurement accuracy. Instead, the complex difference error vector (EV) between



(a) (b)

Figure 2.26: EV of (a) 50 Ω load, and (b) Ku-band horn antenna.

two measured results is introduced as

$$\mathrm{EV} = S_{\text{on-chip VNA}} - S_{\text{comm.VNA}} \tag{2.23}$$

and is shown in Fig. 2.26a, 2.26b [26]. For both cases, the maximum EV ($|EV_{\max}|$) is 0.002 and 0.067, indicating an excellent agreement between the on-chip SiGe reflectometer and the commercial VNA. In addition, in order to verify the repeatability, 5 identical measurements were taken using load DUT, and the measured amplitude and phase difference are $<$0.002 and $<2°$, respectively (Fig. 2.27).

2.10 Two-port S-parameter Measurements

The two-port measurement is similar to the one-port measurement setup with additional RF source to excite port 2 (Fig. 2.28). In addition, a wideband power splitter is used to distribute identical LO power to the each reflectometer chip. As an initial measurement, a thru DUT measurement is performed and its measured S-parameters are described in Fig. 2.29a. The measured S-parameters using the reflectometer chip agree well with the measurement done

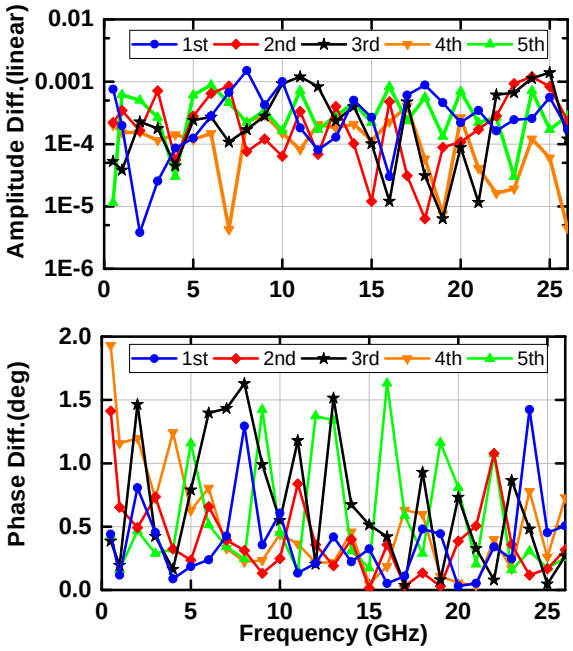


Figure 2.27: Amplitude and phase difference of 5 repeated measurements of load DUT.

by commercial VNA, with amplitude and phase difference of $<$0.02 dB, and $<$1.6°. Another measurement was taken with a 10-dB attenuator and its measurement result is shown in Fig. 2.29b.

The next step is to perform DUT measurement which has high dynamic range in order to verify whether the current measurement setup handles desired dynamic range. The lowpass filter with very low S_{21} was used as a DUT without external VGA, and its measured S_{21} is shown in Fig. 2.33a (green line). Compared to measurement result using commercial VNA, the measured S_{21} is limited to -60 dB and it leads to the in-depth analysis to investigate the limiting factor of current measurements, described in 2.10.1.

2.10.1 Measurement Dynamic Range Analysis

Based on the initial measurements, there are several possible factors that limit the dynamic range in current measurement setup: 1) ADC, 2) RF-to-LO feed-through, 3) radiation 4) crosstalk and 5) and measurement error.

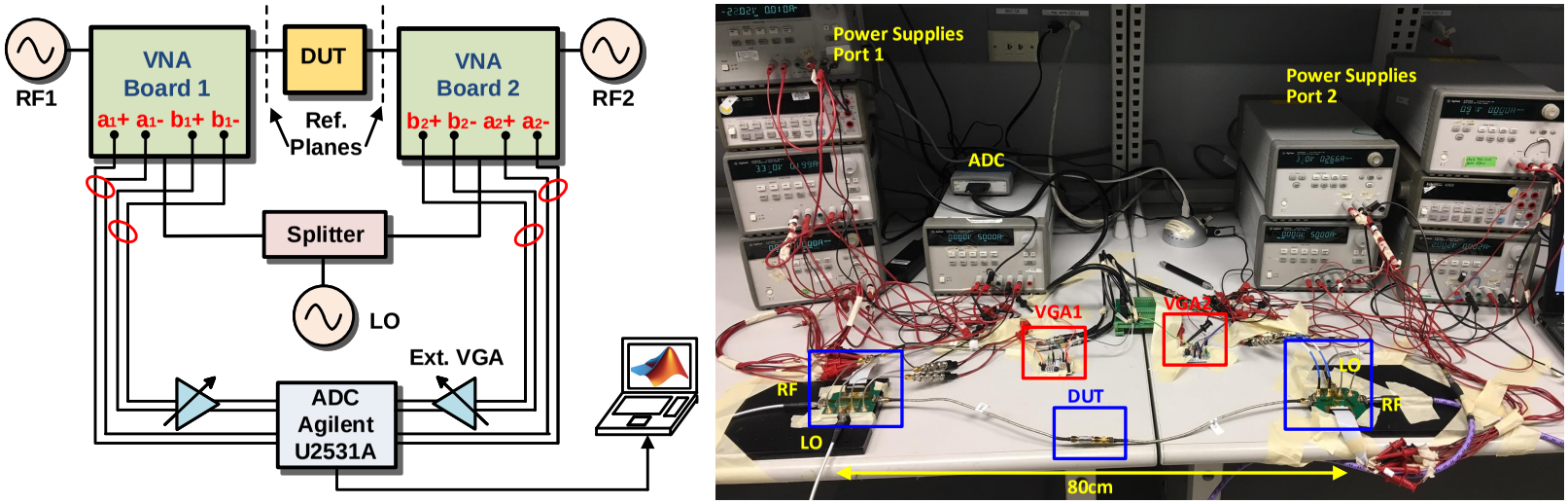


Figure 2.28: Two-port S-parameter measurement setup.

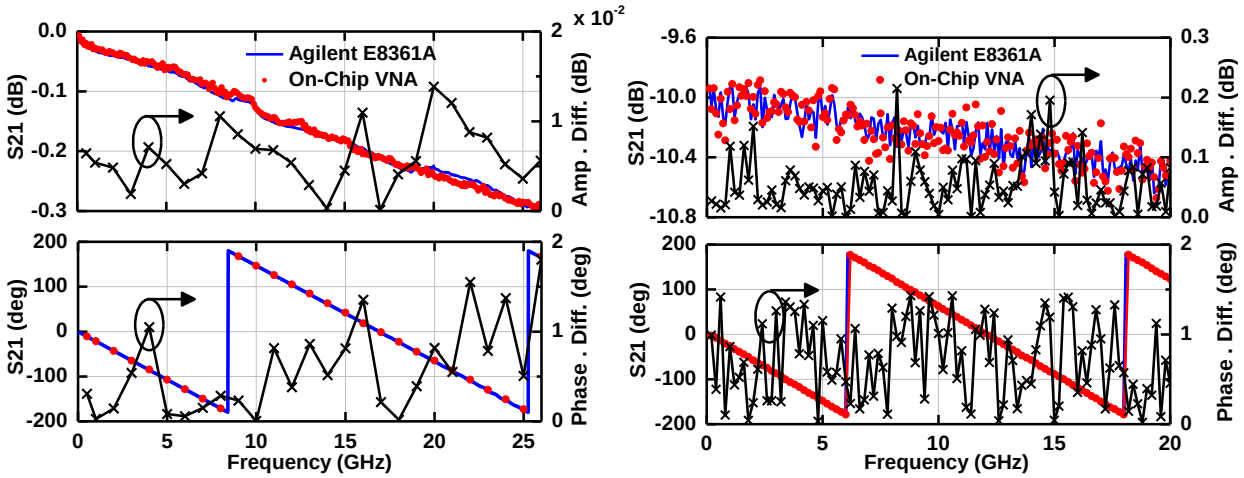


Figure 2.29: Measured S_{21} of (a) thru, and (b) 10-dB attenuator DUT.

The limitation coming from the ADC used in the measurement setup (Keysight U2531A) is due to its effective number of bit (ENOB) of 11.3-bit, resulting in a theoretical dynamic range of 69.8 dB. In practice, it is reduced to ∼65 dB. With the input range of ADC (± 1.25 V), the step voltage (Δ) is

$$\Delta = \frac{2.5\text{V}}{2^{\text{ENOB}}} = 990\mu\text{V} \tag{2.24}$$

Therefore, the minimum detectable voltage (MDV) becomes $\Delta/2$= 495 µV, resulting in

$$\frac{b_2}{a_1} = \frac{\text{MDV}}{490m\text{V}} = -60\text{dB} \tag{2.25}$$

when P_{RF}=10 dBm (input P0.1dB for linear operation) is applied . However, for very low S_{21} measurement, b_2 signal is tens of µV or even lower. Therefore, additional amplification stage is employed to boost b_2 signal and it is achieved by the external variable gain amplifiers (VGAs) with variable gain of $0-40$ dB (See. Fig. 2.28). The measured b_2/a_1 with external VGA

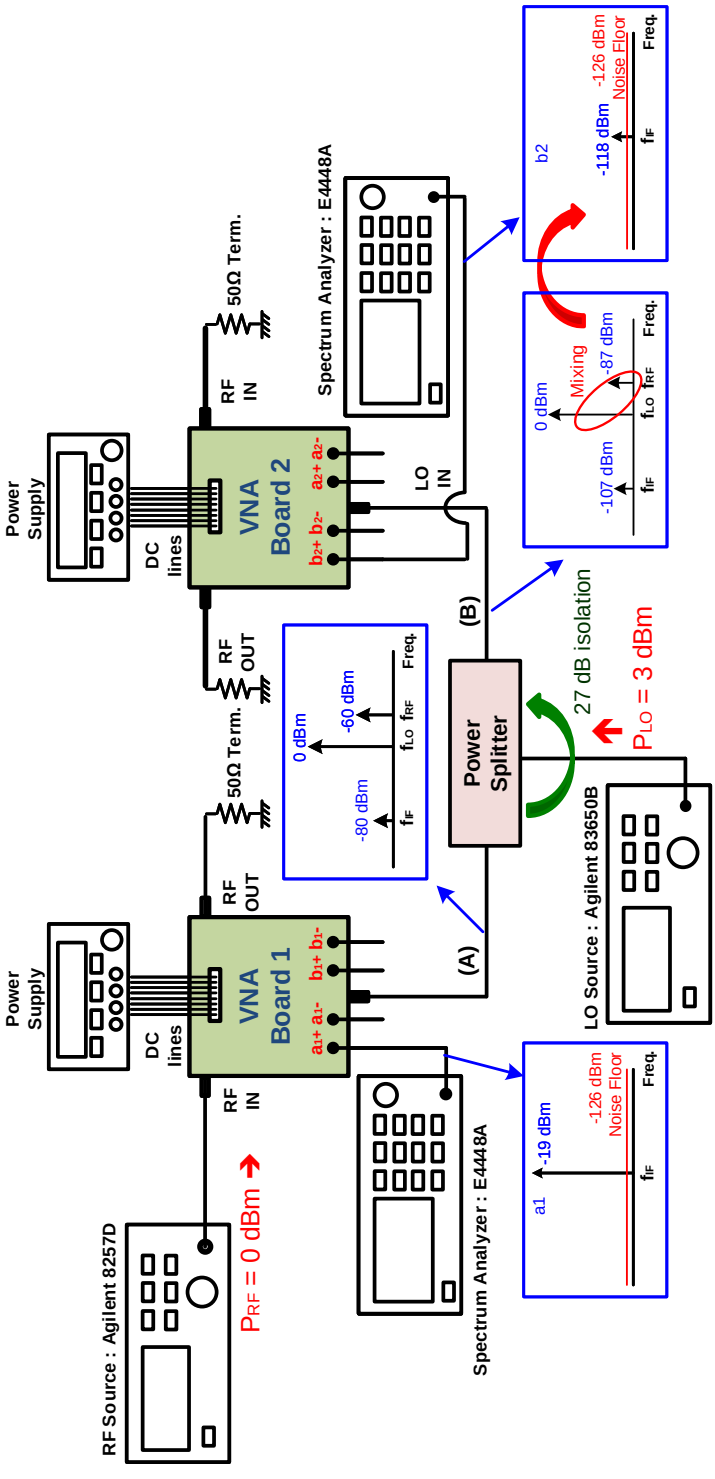


Figure 2.30: Measurement setup of RF-to-LO feed-through effect.

($G_{\text{EXT.VGA}}$=40 dB) becomes

$$\frac{b_2}{a_1} = \frac{5m\text{V}}{490m\text{V}} \frac{1}{G_{\text{EXT.VGA}}} = -79.8\text{dB} \tag{2.26}$$

Note that the amplified b_2 signal of 5 mV is 10 times higher than MDV, and is readily measured. Several S_{21} measurements with different P_{RF} show identical result until b_2 signal is comparable to the minimum detectable voltage. The S_{21} of low-pass filter is measured down to -80 dB, $\sim$20 dB improved measured S_{21} (Fig. 2.33a, red dot). Note that the dynamic range should ideally be improved by 40 dB, meaning that there are other limitation factors that start to dominate when measuring S_{21} below -80 dB.

The RF-to-LO isolation, which discussed in 2.4.8, may be one of these limitation factors. It comes from the finite on-chip RF-to-LO feedthrough as well as the external LO splitter. Fig. 2.30 presents the amount of RF-to-LO leakage at each LO and IF ports. With P_{RF}=0 dBm (linear operation), the measured RF and IF power at node (A) is -60 and -80 dBm, respectively. After considering the measured power splitter isolation of 27 dB, the measured RF power is -87 dBm at node (B). The amount of LO and RF signal is distributed and amplified by the integrated T-junction (6 dB) and LO driver (18 dB forward gain), and then mixed with its own LO signal, generating the undesired IF signal. Note that this is at the same frequency of the desired IF signal, and is always present even without connecting RF source at VNA board 2. The measured b_2 signal in this case is -118 dBm, 8 dB higher than noise floor. This leads to a voltage ratio (b_2/a_1) of -99 dB at 5 GHz with the shared LO source. The same measurement is performed from $1-25$ GHz, and the measurement b_2/a_1 remains $<$-85 dB. As the current setup is limited at measuring -80 dB S_{21}, one con conclude that the RF-to-LO feedthrough is not a dominant limiting factor in the current measurement setup. Still, it indicates that to measure S_{21} of -100 dB or lower, more RF-to-LO isolation is required and it can be achieved by adding amplifiers with high directivity between the LO splitter and (A) or (B) node.

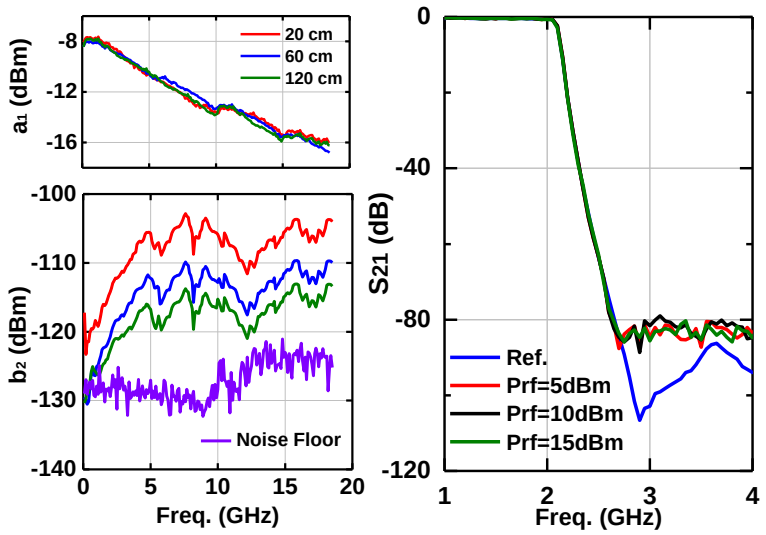
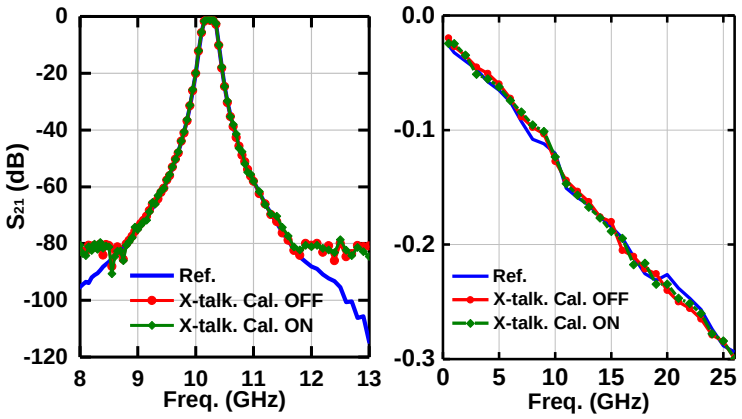


Figure 2.31: (a) Measured a_1, b_2, and noise floor when both ports are terminated to 50 Ω (no DUT connection) , and (b) Measured S_{21} with different RF stimulus input (5, 10 and 15 dBm).

The radiation effect can be also considered as one of the possible limiting factors when it comes to S_{21} of <-80 dB. The radiation effect mainly comes from the unshielded bond-wires and the transmission-line on PCB. The effect of radiation effect is not easy to characterize, however, its effect can be investigated by placing the two test VNA boards with different distance. Fig. 2.31a presents the measured a_1 and b_2 signal when the two RF ports are terminated to 50 Ω with the distance between two VNA boards of 20, 60, and 120 cm. The measurement setup is similar as Fig. 2.30 with LO source disconnected from the VNA board 2 (node (B) disconnection). The a_1 signal is measured using spectrum analyzer, and is -8 to -16 dBm up to 18 GHz for all three cases. However, The measured b_2 at farthest distance (120 cm) is -130 to -115 dBm, which is $\sim$10 dB lower than b_2 signal at shortest distance (20 cm). The noise floor is also measured for the comparison, and is -130 to -120 dBm (RBW of 1 Hz) up to 18 GHz. This implies that the RF radiation plays a role when $b_2/a_1 <$ -100 dB. The effect of radiation is also investigated in an alternative way, by comparing S_{21} with different RF power, and is shown in Fig. 2.31b. An identical LPF (Fig. 2.33a) is measured with P_{RF}= 5, 10, 15 dBm, and the measurement results



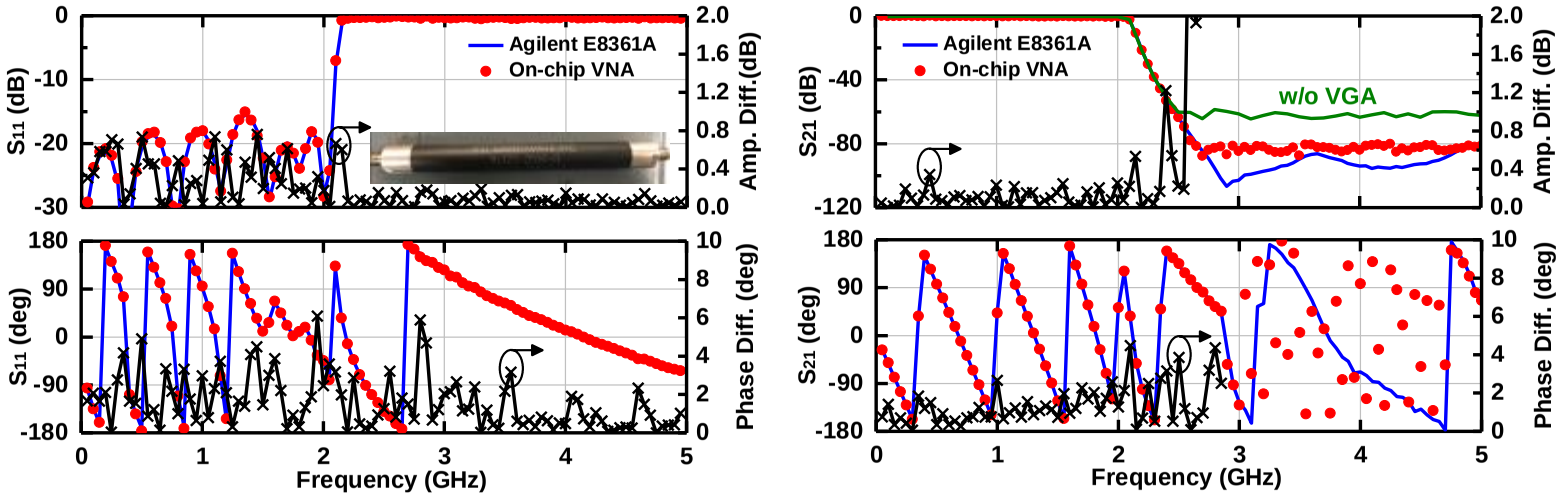
(a) (b)

Figure 2.32: Comparison of measured S_{21} with and without crosstalk calibration (e_{30}, e'_{03}) of (a) bandpass filter, and (b) thru DUT.

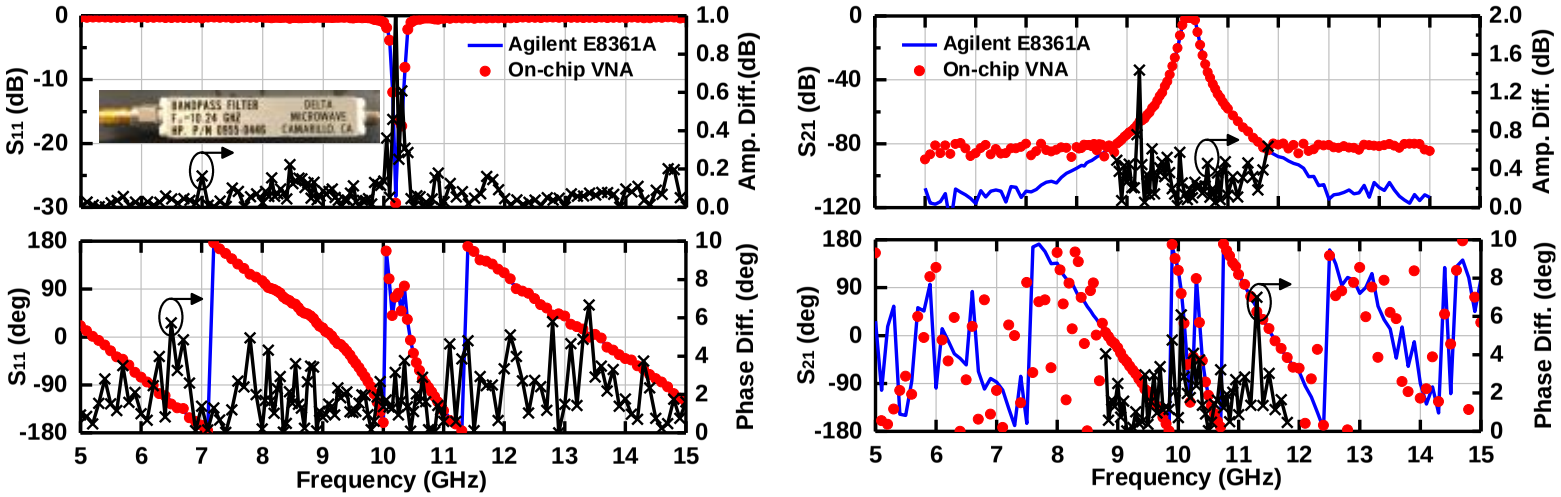
shows identical result within an error range. Therefore, it shows that the radiation is also not a dominant limiting factor at -80 dB level. Still, it implies that sophisticated packaging of IC as well as PCB is required to measure S_{21} < -100 dB.

The effect of crosstalk calibration is also investigated. Two measurements were performed with and without taking into account of crosstalk error terms (e_{30}, e'_{03}) using BPF (Fig. 2.32a) and thru DUT (Fig. 2.32b), and both results shows that two measurements are almost overlapped each other. In general, the crosstalk calibration is performed in commercial VNA only if DUT S_{21} <-100 dB.

With all the experiments done so far, the measurement error could be the reason that limits the measured S_{21} <-80 dB. In fact, in the current measurement setup, the reflectometer boards are prone to move during calibration or especially during the DUT replacement. Any of these effects can generate a certain random error. In addition, all IF signals (e.g., a_1, b_2) are connected to the ADC with bare wires without sufficient ground around it. Therefore, any coupling between wires (even at -80 dB level) may affect the measurement results considerably. These random error can be easily in the range of tens of μV, and affect S_{21} dynamic range in the current measurement setup. The more sophisticated packaging interface can greatly reduce these error so that the

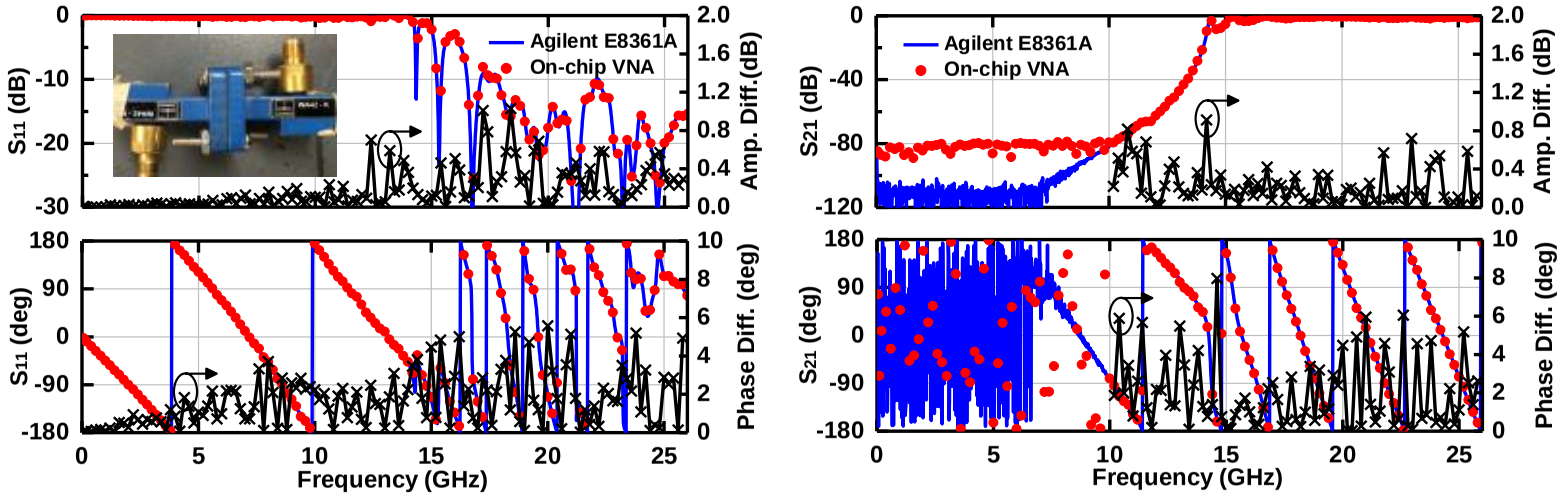


(a)

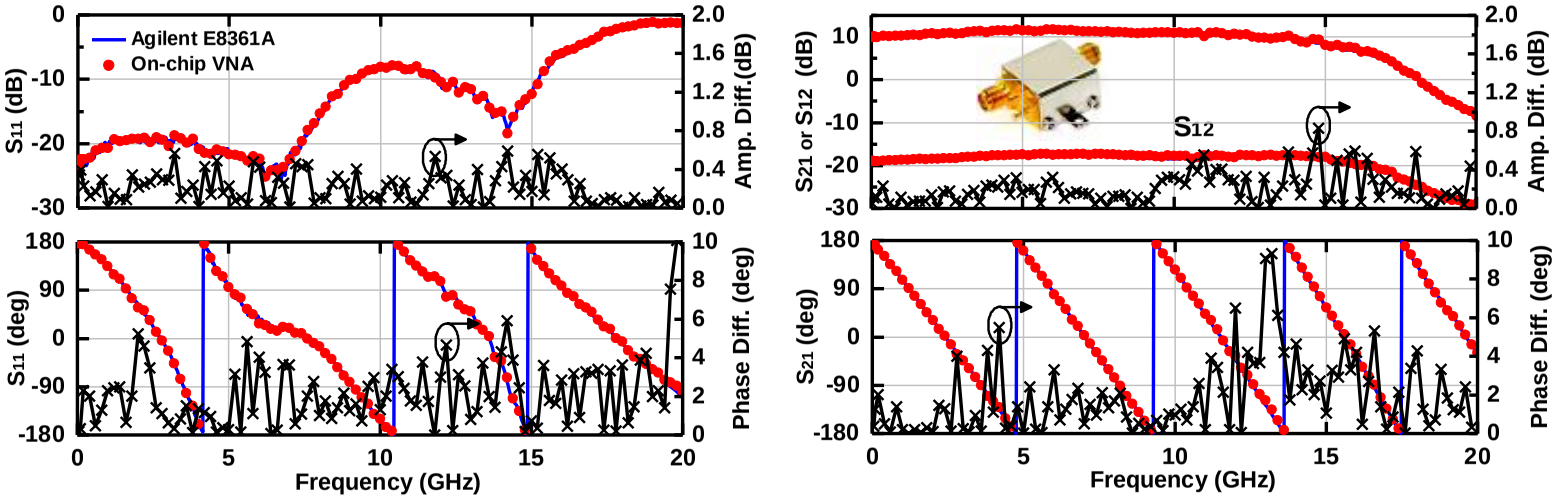


(b)

Figure 2.33: Two-port S-parameter measurement for (a) LPF, and (b) BPF.



(a)



(b)

Figure 2.34: Two-port S-parameter measurement for (a) HPF, and (b) AMP.

Table 2.1: Summarized two-port S-parameter DUT measurements

DUT	Freq (GHz)	Spacing (MHz)	$\overline{\lvert\Delta S_{11}\rvert}$	$\overline{\lvert\Delta S_{21}\rvert}$	EV_{11}	EV_{21}
Thru	$0.01-26$	100	0.14dB $\angle 1.5^\circ$	0.001dB $\angle 0.7^\circ$	<0.03	<0.001
ATT	$0.01-20$	100	0.13dB $\angle 1.4^\circ$	0.07dB $\angle 0.81^\circ$	<0.07	<0.04
LPF	$0.01-5$	50	0.18dB $\angle 1.6^\circ$	0.14dB $\angle 1.3^\circ$	<0.07	<0.04
BPF	$5-15$	$50/200$	0.09dB $\angle 1.9^\circ$	0.31dB $\angle 1.95^\circ$	<0.06	<0.06
HPF	$0.05-20$	200	0.18dB $\angle 2.05^\circ$	0.24dB $\angle 1.98^\circ$	<0.11	<0.12
AMP	$0.05-20$	200	0.19dB $\angle 1.95^\circ$	0.2dB $\angle 1.87^\circ$	<0.1	<0.4

measurement setup is limited by the noise floor.

2.10.2 DUT Measurements

Two-port S-parameter measurements are performed using different DUTs, and the results are shown in Fig. 2.33 and Fig. 2.34. As mentioned in 2.10.1, the LPF S_{21} of $\sim$ -80 dB is achieved with the help of external VGA (2.33a, red dot). Other three DUT measurements (BPF, HPF, AMP) are also performed and shown in Fig. 2.33 and Fig 2.34. For the measurement of S_{21} $<$ -80 dB, maximum gain of external VGA and RF power is used and the VGA gain is taken into account during the calibration and DUT measurement. However, for active circuit measurement, the down-converted IF signals bypass the external VGA ($G_{\mathrm{EXT,VGA}} = 0$ dB) with lower RF power so as not to saturate the receivers in the reflectometer chip. The EV plot of each DUT is also shown in Fig. 2.35. The measurement results of six DUT measurements are summarized in Table 2.1.

In overall, two-port measurement results show an excellent agreement with the com-

mercial VNA with measured S_{21} of -80 dB range with minimum measurement error. For low S_{21} measurement, multiple number of points are sampled at the same frequency to minimize measurement error.

2.11 Conclusion

This work presented a packaged $0.01-26$ GHz reflectometer chip for two-port VNA. The wideband resistive bridge coupler is employed for improved directivity, followed by a high-linearity receiver. The receiver dynamic range of $133-126$ dB is achieved with RBW of 10 Hz. The RF/LO signals as well as DC and digital controls are wire-bonded, and a wideband matching network is implemented on a low-cost PCB. Various one- and two-port DUT S-parameter measurements are performed with excellent agreement with the commercial VNA. The measured S_{21} of -80 dB is achieved, and an in-depth analysis of S_{21} dynamic range analysis is addressed for various possible limiting factors.

2.12 Acknowledgment

This work was supported by Keysight Technologies and TowerJazz.

Chapter 2, in part, is a reprint of the material as it appears in: H. Chung, Q. Ma, M. Sayginer, and G. M. Rebeiz, "A packaged $0.01-26$ GHz single-chip SiGe reflectometer for two-port vector network analyzers", *IEEE International Microwave Symposium (IMS)*, June, HI, 2017, pp. 1259-1261. The dissertation author was the primary investigator and author of this paper.

Chapter 2 is also, in full, has been submitted for publication of the material as it may appear in: H. Chung, Q. Ma, M. Sayginer, and G. M. Rebeiz, "A packaged $0.01-26$ GHz single-chip SiGe reflectometer for two-port vector network analyzers", *IEEE Trans. Microw. Theory*

Techn., submitted. The dissertation author was the primary investigator and author of this paper.

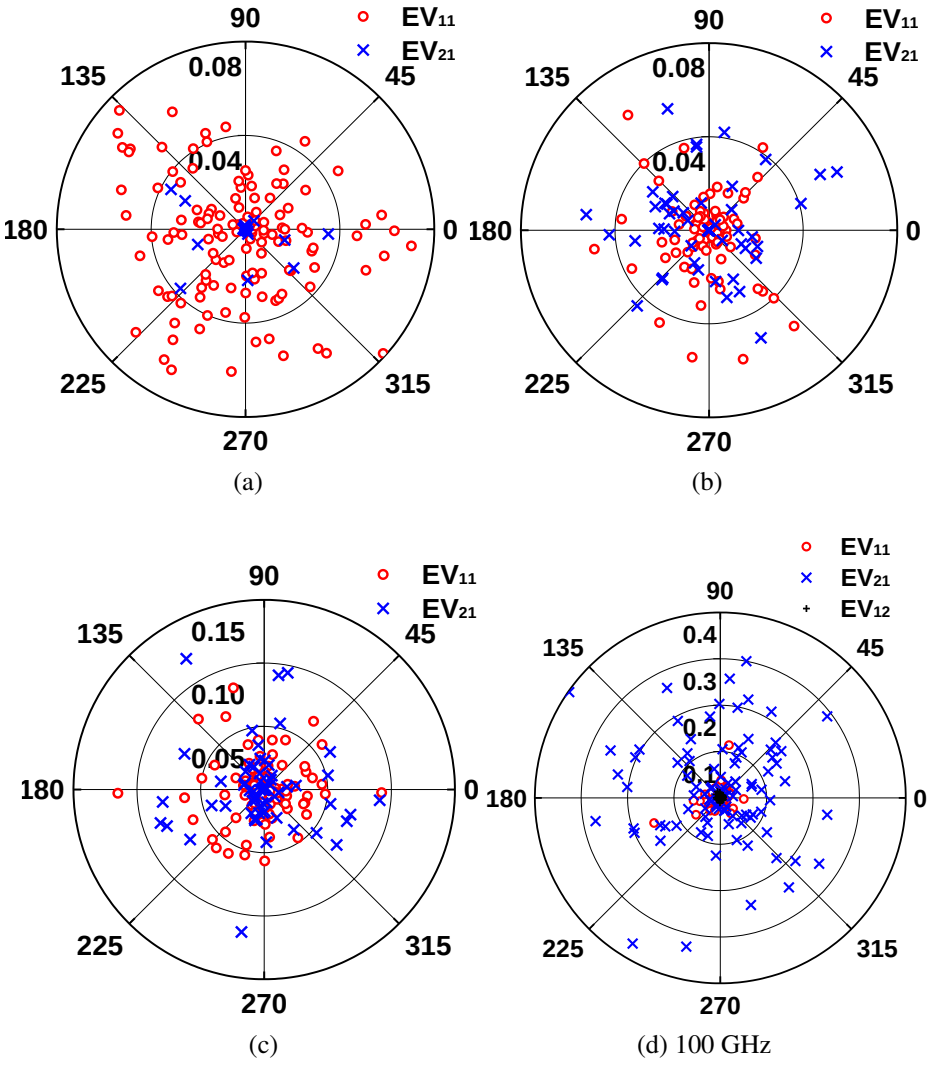


Figure 2.35: EV of two-port S-parameter DUTs: (a) LPF,(b) BPF, (c) HPF, and (d) AMP.

Chapter 3

A 70-110 GHz Single-Chip SiGe Reflectometer with Integrated Local Oscillator Quadrupler

3.1 Introduction

Advances in mm-wave communication systems at 70–75 GHz and 80–85 GHz have pushed for lower cost instrument to be available for reduced testing costs, including vector network analyzers (VNA). Several efforts have been demonstrated using single-chip reflectometers up to 100 GHz (especially for biomedical applications), but most lack the dynamic range required for high performance VNAs [18, 21–23, 25]. This work demonstrates the first W-band single-chip reflectometer for one-port VNA, including integrated directive components and x4 LO frequency multipliers.

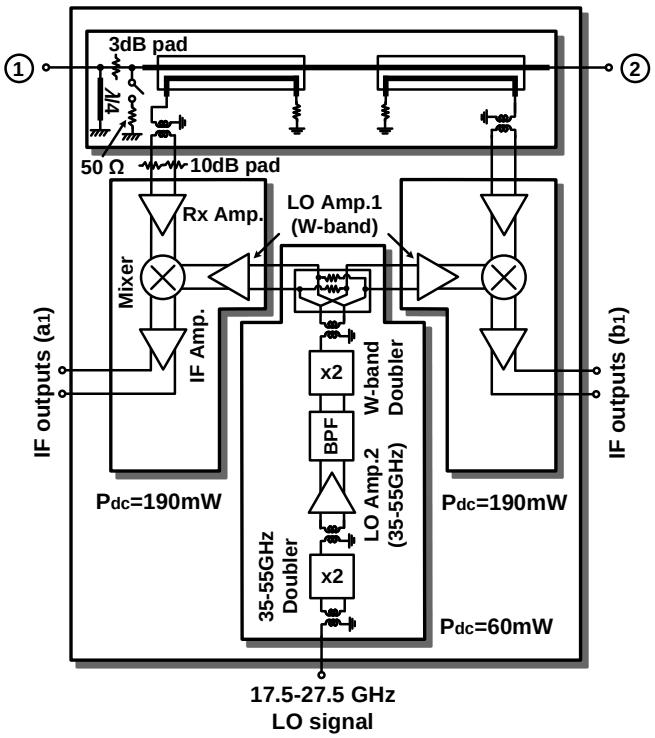


Figure 3.1: Block diagram of the 70–110 GHz SiGe reflectometer for mm-wave vector network analyzers.

3.2 70−110 GHz Reflectometer Design

Fig. 3.1 presents the 70–110 GHz single-chip SiGe reflectometer. The incident RF signal is coupled to the wideband receivers using two directional couplers so as to measure reference and reflected signals. Each receiver has identical gain response except for an additional 10 dB attenuator placed in the reference-channel receiver since the reference signal is typically much larger than the reflected signal. The receive channels down-convert the 70–110 GHz signals to an intermediate frequency (IF) using a fundamental active mixer for lower conversion loss. The magnitude and phase of the IF output for reference and reflected channels are generally obtained using ADCs and signal processing at the IF, but in this case, they are fed into a digital scope which does the same function.

The coupler directivity is one of the most important specifications for high performance VNAs, and a high directivity enables the VNA to achieve accurate measurements even in the

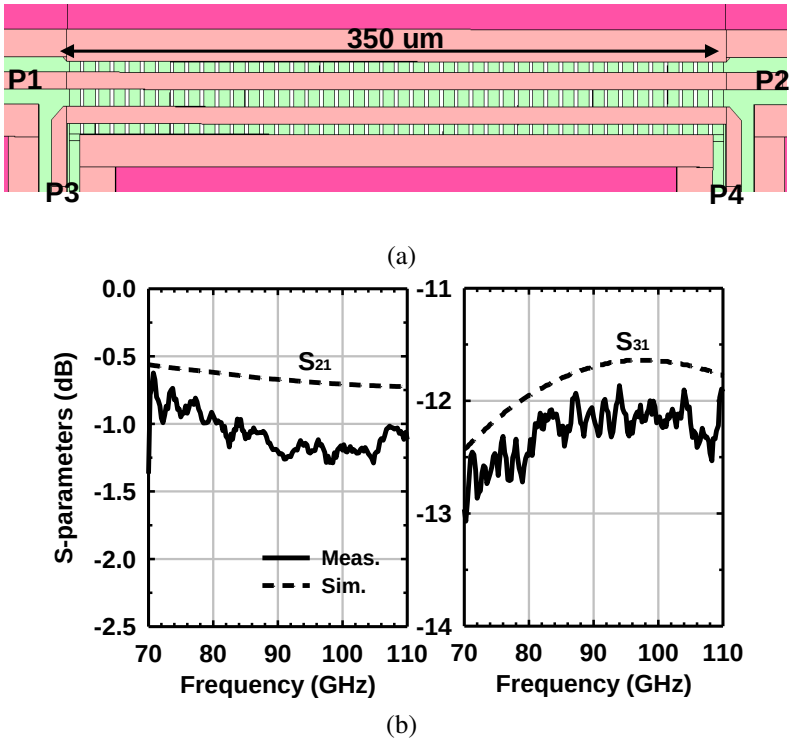
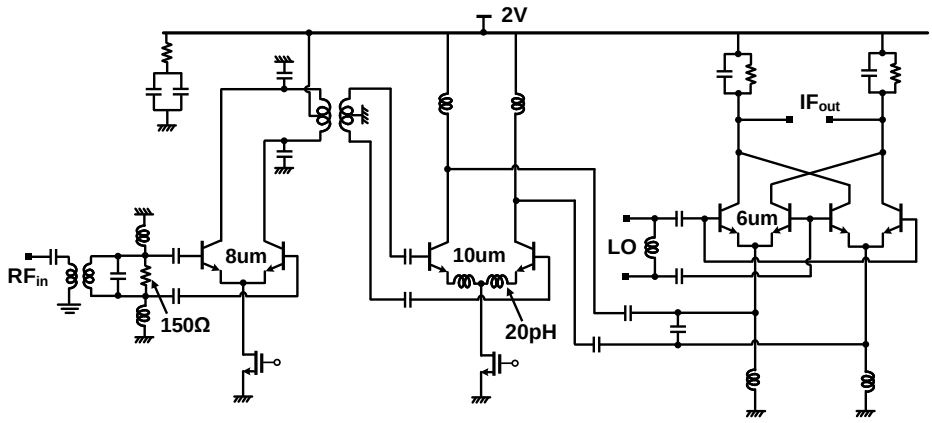


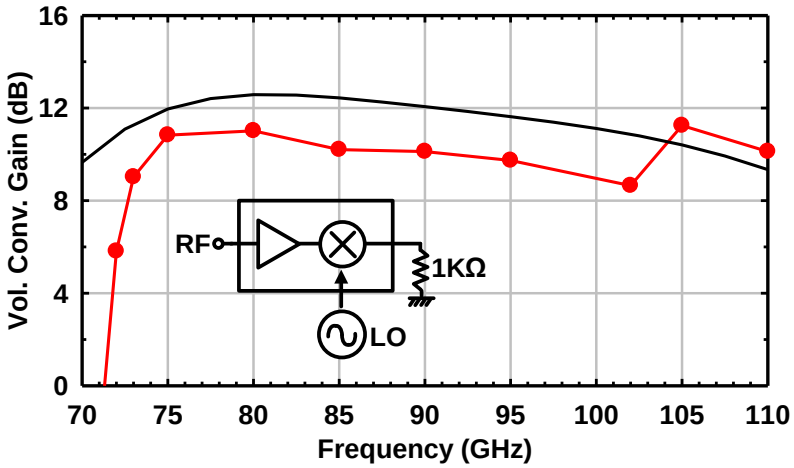
Figure 3.2: (a) Layout of CPW directional coupler, and (b) insertion loss and coupling ratio.

precense of loss between the reflectometer and the DUT [18]. In order to achieve such requirements, a CPW coupled-line with patterned ground shield is implemented as shown in Fig. 3.2a. The patterned ground underneath the coupled line removes the effect of the image current in the bottom ground, and equalizes the even and odd mode propagation coefficients, Coupled lines with signal-gap-signal of 8-8-8 µm and a length of 350 µm are built using the top and ground metal layer, result in Z_e and Z_o of 67 Ω and 38 Ω, respectively. Fig. 3.2b presents the insertion loss (1 ± 0.2 dB) and coupling ratio (-12 dB) at 70–110 GHz. The simulated isolation and directivity are -40 dB and 27 dB at 90 GHz, respectively, and the measured isolation is $6-10$ dB higher than simulations (not shown).

The receiver is built using a two-stage common-emitter wideband amplifier followed by a high-linearity Gilbert-cell mixer (Fig. 3.3a). The receive chain requires high linearity instead of low noise figure, and inductive degeneration is used in the second stage. Also, the amplifier



(a)



(b)

Figure 3.3: 70–110 GHz wideband amplifier and mixer: (a) schematic, and (b) voltage conversion gain.

is matched using a 150 Ω differential resistor at its input port, for added linearity and wideband performance. A high isolation is achieved using the two-stage amplifier design (S_{12} <-40 dB), greatly reducing the LO-to-RF leakage from the mixer. Note that this leakage increases the VNA measurement error since the LO leakage signal will generate an undesired IF signal in the second heterodyne receiver, and therefore, it is important to minimize it. The down-converted signal is fed into IF amplifiers with 2-bit gain control and a 3-dB bandwidth of 5 MHz and 2.5 GHz (two different amplifiers selected by SPDT switches). The measured input P_{1dB} of the amplifier+mixer stage is -1 to -3 dBm at 70–110 GHz (not shown). The measured voltage conversion gain of the amplifier+mixer is shown in Fig. 3.3b. Note that the output voltage swing is measured using a

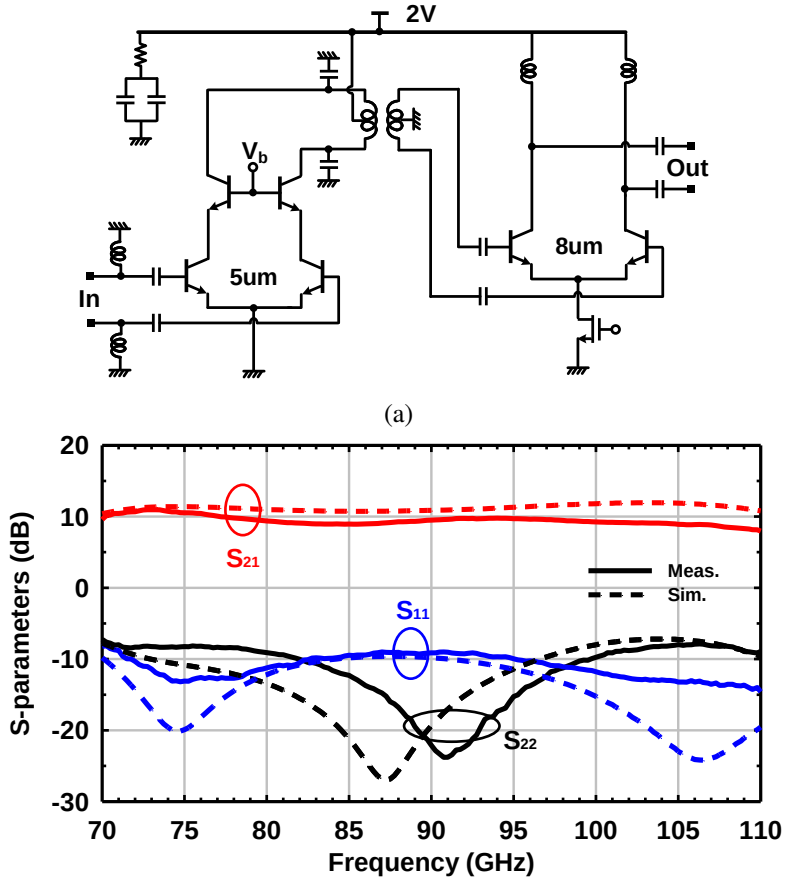


Figure 3.4: 70–110 GHz LO amplifier: (a) schematic, and (b) S-parameters.

high-impedance scope at an IF of 1 MHz.

Fig. 3.4a presents the schematic of 70–110 GHz two-stage LO amplifier. This amplifier is used to and is to generate enough LO power to drive the high-linearity mixer, and provides a measured output power of -2 to 4 dBm over the W–band range. The LO amplifier S-parameters are shown Fig. 3.4b, with a gain of 8–10 dB at 70–110 GHz and a good impedance match. Frequency doublers with bandpass filter and inter-stage amplifier are also implemented in the LO chain, and upconvert the 17.5−27.5 GHz LO signal to 70–110 GHz signal for measurement easiness.

Fig. 3.5 presents the receiver power conversion gain using the low-IF amplifier. The measured power gain is 15 to 20 dB and -5 to +3 dB for high and low-gain settings, respectively,

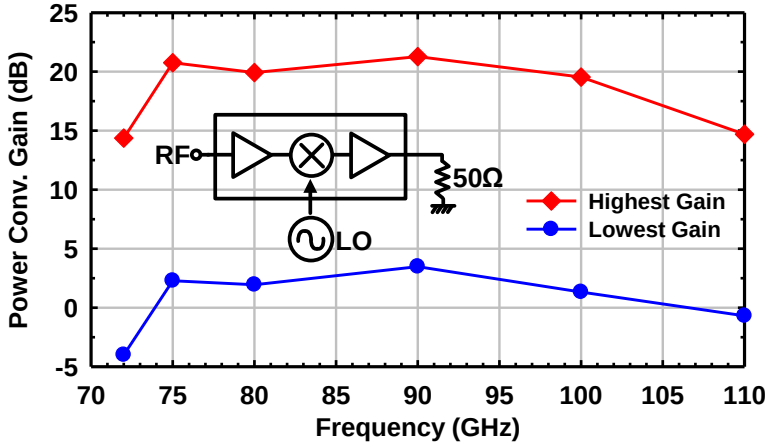


Figure 3.5: Measured receiver power conversion gain.

over the entire 70-110 GHz range. The simulated receiver noise figure in the high gain mode is 18–24 dB at 70–110 GHz. The input P_{1dB} is -20 dBm in the high-gain mode, resulting in a receiver dynamic range of 120–125 dB at 70–110 GHz in 10 Hz resolution bandwidth (RBW). The input P_{1dB} is limited by the IF amplifier output current drive. The system dynamic range is therefore 110–115 dB with a 10 dB back-off. Note that a λ/4 shorted-stub is used at port 1 and acts as an electrostatic discharge (ESD) protector. Also, a switched 50 Ω load is attached to the RF port so as to provide a matched impedance at port 1 when port 2 is activated for two-port measurements. Finally, a 3-dB pad is also placed at port 1 to de-Q any open and short circuits due to the source when deactivated.

3.3 One-Port Measurements

The chip was fabricated in the Global Foundries GF8HP SiGe BiCMOS process with 7 metal layers and a 4 µm- thick top layer. Separate V_{CC} and GND areas are used for the x4 LO frequency multiplier block and two receivers for better isolation. The chip consumes 440 mW from a 2 V power supply, and the size is 5.86 mm^2 (2.39 × 2.45 mm^2) including all pads (Fig. 3.6). For one-port S–parameter measurements, the chip is mounted on a printed circuit board

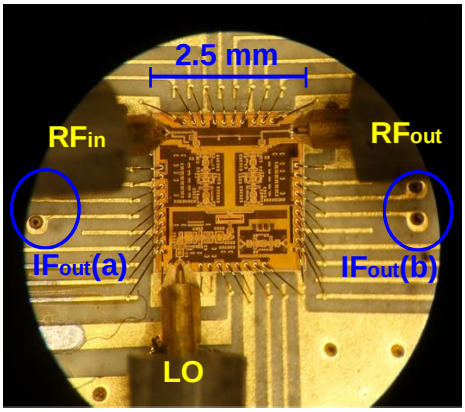


Figure 3.6: Single-chip SiGe reflectometer with GSG probes.

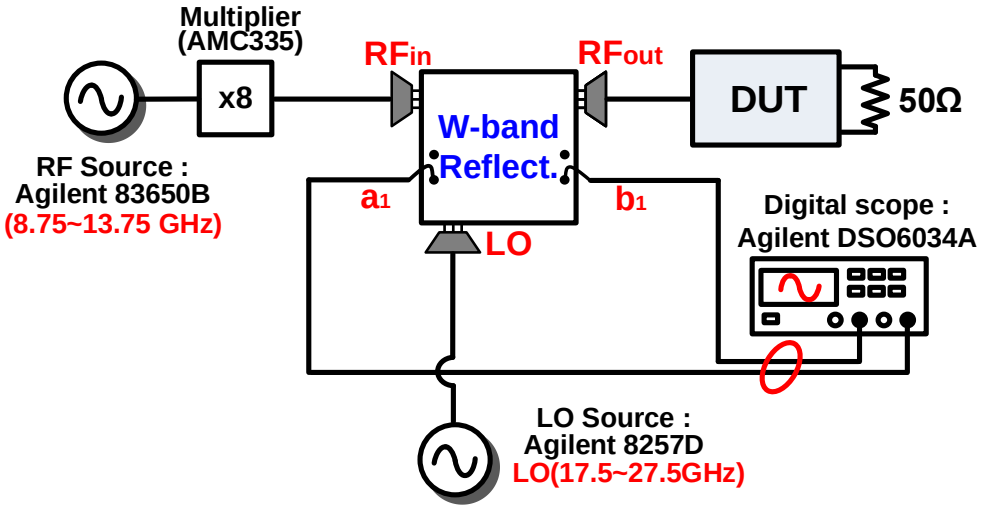


Figure 3.7: Measurement setup of the single-chip one-port system.

(PCB) and all DC biasings and digital controls are bonded on the PCB. The RF and LO signals are applied using GSG W–band and coaxial probes.

Fig. 3.7 presents the one-port S–parameter measurement setup. The W-band RF input is generated using a x8 multiplier chain. The 17.5−27.5 GHz LO signal is directly fed into the chip using a GSG coaxial probe and is up-converted by the integrated x4 multiplier chain. The down-converted signals are fed a digital scope to measure for magnitude and phase measurements of the reference and reflected signals. For the RF output, another GSG WR-10 probe is used to

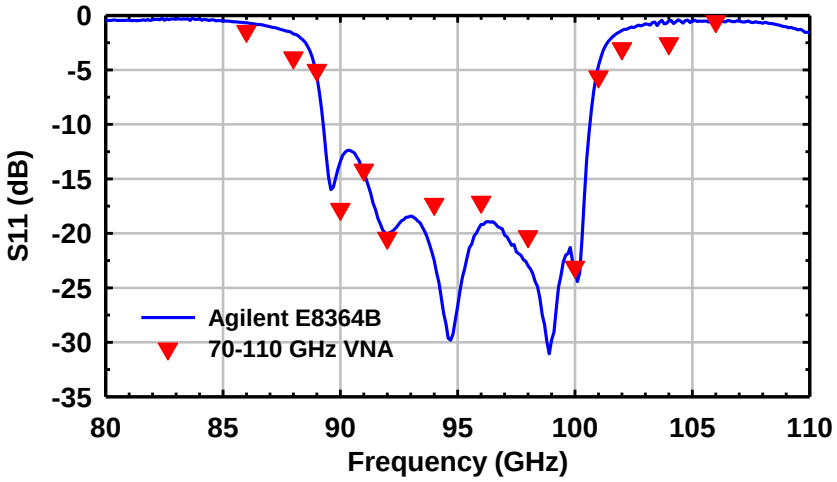


Figure 3.8: Measured S_{11} of a 95 GHz bandpass filter using a commercial VNA and the single-chip 70–110 GHz reflectometer.

connect to the WR-10 calibration kit and DUT.

The one-port magnitude measurement of a WR-10 bandpass filter with a center frequency of 95 GHz is shown in Fig. 3.8. The DUT S_{11} is measured using both a commercial VNA and the single-chip reflectometer. Open-short-load (OSL) calibration is performed using WR-10 calibration kit before the DUT measurement. Note that the waveguide measurements using the commercial VNA does not include the GSG WR-10 output probes which is required for the single-chip reflectometer measurements. The measured S_{11} by 70–110 GHz VNA and commercial VNA agrees well with an average difference of 1.68 dB.

3.4 Conclusion

This work presented a 70–110 GHz single-chip SiGe reflectometer for one-port vector network analyzer. Two directional couplers are implemented together with two high-linearity heterodyne receivers on a single chip at 70-110 GHz. In addition, a x4 frequency multiplier chain is also implemented on the same chip. A CPW (Coplanar Waveguide) coupled-line directional is used with a shielded ground plane for improved isolation and directivity. The dynamic range of

the receiver is 110–115 dB at 70–110 GHz with 10 dB back-off and 10 Hz resolution bandwidth (RBW). The SiGe chip is 5.86 mm^2 and consumes 440 mW from a 2 V supply. The chip is mounted on a printed circuit board (PCB), and RF and LO signals are applied using probes. A 95 GHz bandpass filter is measured as the device-under-test (DUT) and the results obtained using the on-chip VNA and a commercial VNA show good agreement over a wide frequency range.

3.5 Acknowledgment

This work was supported by the Keysight Technologies and Global Foundries.

Chapter 3, in full, is a reprint of the material as it appears in: B.-H. Ku, H. Chung and G. M. Rebeiz, "A 70-110 GHz single-chip SiGe reflectometer with integrated local oscillator quadrupler", *IEEE International Microwave Symposium (IMS)*, June, HI, 2017, pp. 980-982. The dissertation author was the secondary investigator and second author of this paper.

Chapter 4

A 10−40 GHz 4-Channel Frequency Quadrupler with Switchable Bandpass Filter and >30 dBc Harmonic Rejection with Flip-Chip Packaging

4.1 Introduction

The design of a high-speed and high-data rate communication system at millimeter-wave frequency range (∼30 GHz), has recently been in high demand for commercial use as well as high interest in various research applications. [38]. With a remarkable improvement of silicon technology together with a skyrocketed demands of using less crowded frequency bands for less interference to each other, numerous mm-wave MMICs are introduced in many applications such as automotive radar [39–41], short-range backhaul [42, 43], imaging systems [44, 45], wideband phased-array [46], wideband modulator with complex modulation for high-data rate wireless link [47, 48], and the 5G mobile communication system [49–51]. Therefore, the performance

of signal generation at mm-wave frequency becomes one of the most important figure of merits (FOM) in the entire system. However, due to the stringent requirement in the market, the design of wideband, high-power, high spectral purity LO generation remains ongoing challenges.

One of the straightforward methods to obtain LO signal is to directly generate the signal by implementing mm-wave VCO and PLL [52–55]. Even with improved performance, however, this approach is generally limited due to high power dissipation and poor phase noise in which both parameters are critical and should be minimized for most of the applications. First of all, high power consumption is mainly coming from frqeuency divider (prescalar) circuit operated at mm-wave frequency regime and is inevitable to suppress the noise floor [54]. In addition, the design of VCO and PLL at mm-wave frequency itself is challenging due to comparable parasitic capacitance of the transistor (C_{gs}, C_{gd}, etc), resulting in poor phase noise and reduced tuning range [55].

On the contrary, making use of $\times$N frequency multiplier placed after low-phase noise VCO+PLL circuits can be a good solution to resolve both problems at the same time. The frequency synthesizer operated at sub-10 GHz range has superb phase noise performance even with theoretically added phase noise by 20·log(N) dB, where N is the multiplication factor. The circuit implementation operated at $\times$N lower frequency relaxes design complexity with the help of better quality factor (Q-factor) of the passive components and the negligible parasitic effect. Therefore, the studies of integrated VCO+PLL with injection locking frequency multipliers (ILFM) are active and have recently published at different frequencies [56–58].

Although this approach provides an optimum solution in terms of integrated phase noise (IPN), power dissipation, and area efficiency, the frequency locking inevitably limits the tuning ranges of the VCO, resulting in having relatively narrowband frequency source. Therefore, instead of using integrated ILFM, wideband off-chip frequency synthesizer followed by a wideband frequency multiplier is considered to obtain a super-wideband ($>$100 % FBW) signal source and is shown in Fig. 4.1. The input frequency of $2.5-10$ GHz is generated by low-phase noise

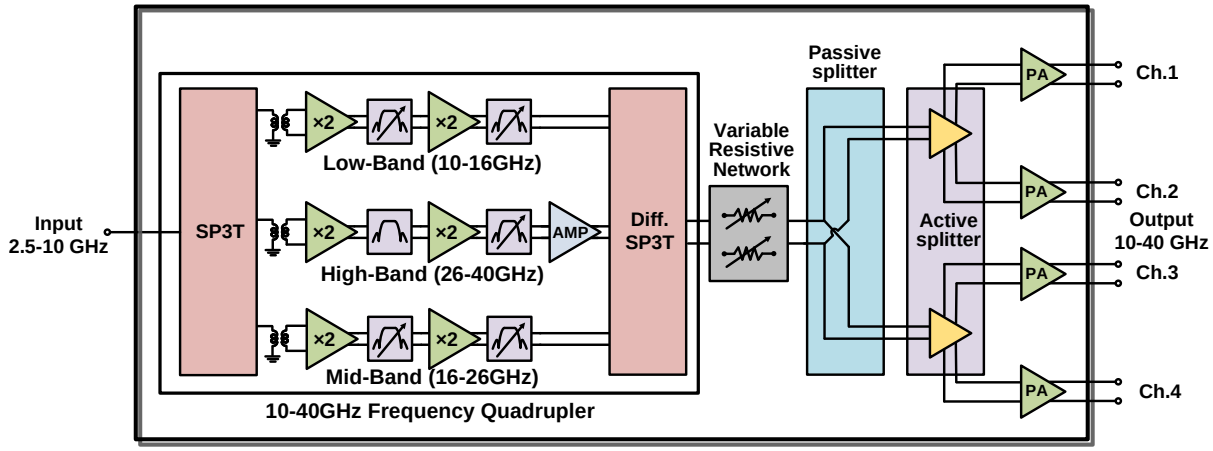


Figure 4.1: Block diagram of 4-channel $10-40$ GHz frequency quadrupler.

frequency synthesizer and the input signal passes through one of the frequency bands for frequency multiplication depending on the operation. The frequency multiplied signal is then split and amplified while maintaining HRR $>$ 30 dB, which will be discussed in the following section. The wideband frequency source operated at $10-40$ GHz becomes very popular in many applications such as dual-band 5G operation at 28-GHz and 39-GHz region [59], and high-resolution imaging radar system for $<$1cm resolution for security screening [60, 61].

The stream of this paper is following. The design goals of this work are introduced together with on-chip switchable bandpass filter operation for improved harmonic rejection in Section 4.2. Brief process technology information is followed by details of circuit designs in Section 4.3 and 4.4. Section 4.5 introduces the packaging details for the flip-chip, and experimental results and conclusion are presented in Section 4.6 and 4.7, respectively.

4.2 x4 Frequency Quadrupler Topologies

There are three main goals for this design: 1) $10-40$ GHz wideband operation ($>$100% FBW), 2) $>$30 dBc in-band harmonic rejection, 3) enough output power ($\sim$3 dBm) with 4-channel distribution. In order to fulfill the first requirement, the input signal is separated into three different

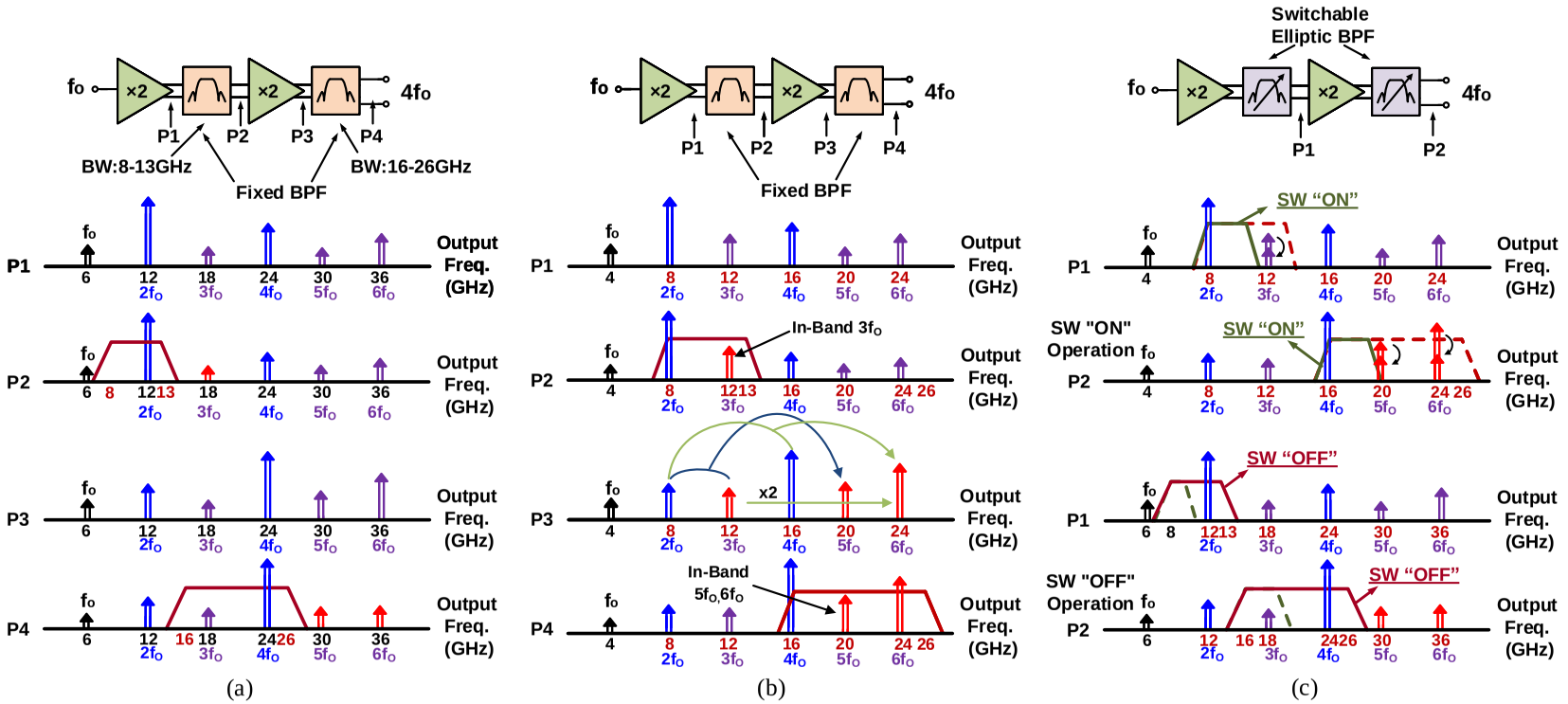


Figure 4.2: (a) Viewgraph of harmonics with fixed bandpass filter , (b) switchable bandpass filter (SW ON mode), and (c) SW OFF mode at mid-band multiplier chain.

bands using SP3T to relax the FBW of each bands (46, 47, 42%) shown in Fig. 4.1 The optimum number of bands is carefully investigated before implementation, and three-band operation is the best solution for circuit realization (feasible FBW of the circuit blocks), reasonable chip area and passive loss of SPNT, and the required harmonic level at the output. The way to generate x4 frequency signal from the input is to make use of cascaded frequency doubler, rather than using a standalone frequency quadrupler, since it takes advantages of much weaker g_{m4}, resulting in much lower power at the output [62]. However, the frequency multiplier composed of cascaded frequency doublers generates not only $2f_o$, but also generates undesired harmonics, such as f_o, $3f_o$, and $4f_o$ at the output of the first doubler, and these 'seed harmonics' are inter-mixed or frequency doubled at the second stage doubler, resulting in large amount of harmonic components ($2f_o$,$3f_o$,$5f_o$,$6f_o$, etc) at the output ($>$ -20 dBc) [63]. Note that such undesired harmonics are $\sim 6-10$ times lower than f_T, therefore, much stronger harmonic currents are generated after each frequency doubler compared to same order harmonic currents that are generated at W-band or even higher frequency region for $>$100 GHz frequency multiplier designs. This leads to come up with using inter-stage bandpass filteres between frequency doublers so as to fulfill the second design goal, shown in Fig. 4.2a. Two fixed bandpass filters are located after each frequency doubler and the harmonic contents of each nodes (P1, P2, P3 and P4) are described with the input frequency of 6 GHz, which is the right-edge of the middle-band ($4-6.5$ GHz). After the first stage doubler, large even harmonics ($2f_o$, $4f_o$) with smaller odd harmonics (f_o, $3f_o$, $5f_o$) are generated (Fig. 4.2a-P1). The passband of the fixed bandpass filter is $8-13$ GHz and this only passes the desired harmonic ($2f_o$) and suppresses all the remaining harmonics (Fig. 4.2a-P2). Therefore, even after the second stage doubler, the amount of undesired harmonics (all harmonics except $4f_o$) are decently rejected (Fig. 4.2a-P3). Plus, the effect of second bandpass filter further rejects out-of-band (OOB) harmonics such as $2f_o$, $5f_o$, and $6f_o$, while passing the $4f_o$ (Fig. 4.2a-P4). The role of the fixed bandpass filter seems well suited for the harmonic rejection at this point, however, the other observation shows that it is problematic, in which Fig. 4.2b is the case. When

the input frequency is at 4 GHz, which is the left-edge of the middle-band, similar amount of harmonics are generated at Fig. 4.2b-P1, however, the undesired $3f_o$ remains unfiltered together with the $2f_o$ (Fig. 4.2b-P2), which results in larger 'seed harmonics' at the input of the second frequency doubler. The effect of intermixing and self-mixing of larger 'seed harmonics' is not linearly proportional, and larger harmonic contents are generated at the output of the second doubler (Fig. 4.2b-P3). Unfortunately, the largest two harmonics ($5f_o$, $6f_o$) are located in the passband of the second bandpass filter, and there is no way to suppress these while keeping the main tone unchanged. This results from frequency division that each bands is required to operate $\sim$45% FBW, and relaxing the bandwidth of each band enables to push the undesired harmonics out-of-band with the expense of additional one more band, which results in more chip area and extra loss of switches.

The solution to avoid aforementioned drawbacks is to control the passband of the bandpass filters as shown Fig. 4.2c. Instead of using fixed bandpass filter, switchable bandpass filter helps to reduce the passband so that the $3f_o$ content is suppressed by using multi-order elliptic filter for sharp skirts at the cutoff frequency (Fig. 4.2c-P1, SW ON). Lower $3f_o$ generates much lower undesired harmonics at the output of the second doubler (Fig. 4.2c-P2, SW ON), and these can be further rejected by reducing the passband of the second bandpass filter. When the input frequency is at 6 GHz, the switch is off to behave it as a normal bandpass filter (Fig. 4.2c, SW OFF).

In order to satisfy the last design goal, the output of the multiplier chain is connected to 1:4 driver to provide identical output power to the each channels. The resistive attenuator is placed right after multiplier chain so as to relax the linear operation of active splitter and PA at the last stage. For 1:4 channel distribution, one passive and one active splitters are used to reduce the power consumption and achieve channel-to-channel isolation at the same time. The last stage power amplifier is carefully designed to have its $\mathrm{OP_{1dB}}$ of $4-5$ dBm, in order not to generate too much 3rd harmonic referenced to the signal after multiplier chain ($12f_o$ from the input), since it limits the worstcase HRR at given input frequency, especially when $12f_o$ is located in-band

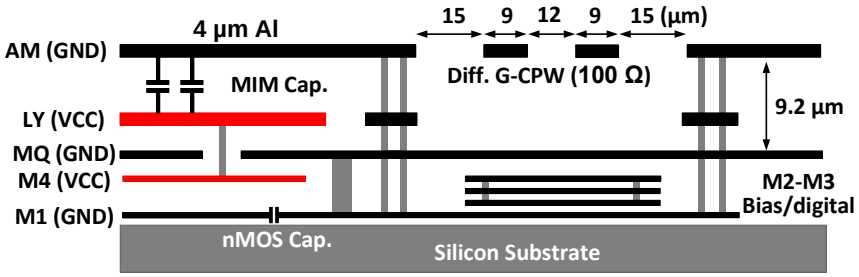


Figure 4.3: Stack-up with differential GCPW line in GF8HP technology.

region (<40 GHz). The output power of +3 dBm is set per each channels, since the required LO power for most multi-channel applications ranges from -5 to 0 dBm [39, 49, 50].

In summary, using three bands with the switchable elliptic bandpass filters allows wider fractional bandwidth to be used in each path with desired harmonic rejections. In addition, the design of wideband 1:4 driver with OP_{1dB} of $4-5$ dBm enables the frequency converted signal to be equally distributed as well as with lower 3rd harmonic content. Note that for high-band operation, only one switchable bandpass filter is used in the multiplier chain since the $5f_o$, $6f_o$ harmonics are out-of-band for $f_o > 8$ GHz, and the in-band $5f_o$ and $6f_o$ harmonics are sufficiently suppressed by using one switchable bandpass filter at the second stage (6.5 GHz $< f_o <$8 GHz).

4.3 Technology

The 4-channel $10-40$ GHz frequency quadrupler is designed using GF8HP 0.12-µm SiGe BiCMOS process. In addition, 0.13-µm CMOS transistors are also available for digital circuit and biasing. Fig. 4.3 shows the back-end-of-line (BEOL) of this process, including seven metal layers with two thick metal layers, AM (=4 µm) and LY (=1.25 µm), for low-loss RF routing. The f_T and f_{MAX} of the bipolar transistor is 200 GHz. The 100-Ω differential coplanar waveguide (CPW) transmission line (15-9-12-9-15 µm) is implemented with AM and MQ ground plane, and a simulated loss is 0.3 dB/mm at 40 GHz.

The simulated Q of the transmission line is 18 at 40 GHz. For V_{CC} distribution around

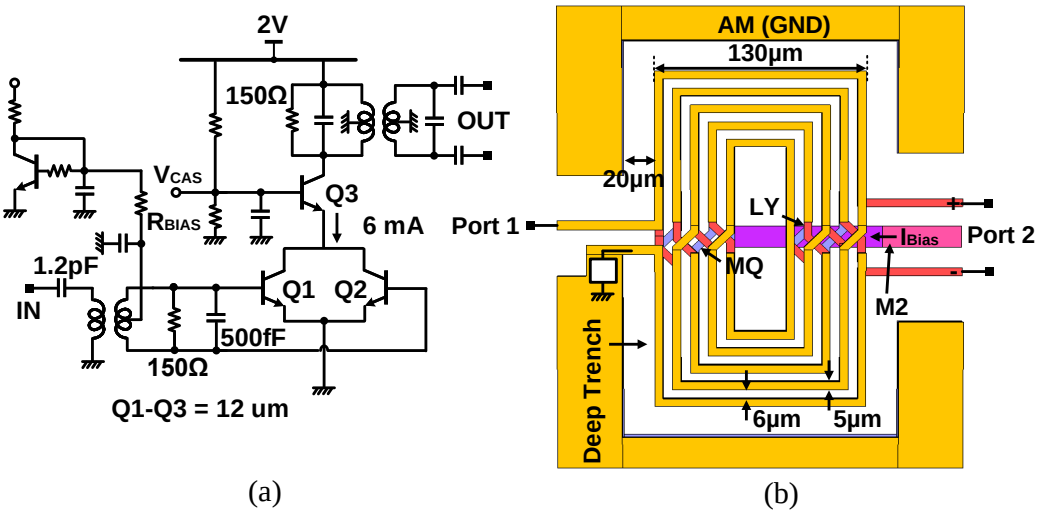


Figure 4.4: (a) Schematic of 1st-stage doubler in low-band path (input is 2.5−4 GHz, output is 5−8 GHz), and (b) EM layout of input balun.

the active core, both LY and M4 layers are stacked in parallel to minimize IR voltage drop.

4.4 Circuit Designs

4.4.1 Doublers

For a 10−40 GHz frequency quadrupler, 6 different frequency doublers (2 for each bands) are necessary, and Fig. 4.4a presents the schematic of one of the frequency doublers implemented in the multiplier chain (1st-stage, low-band). The single-ended input signal (2.5−4 GHz) is converted into differential using passive balun with caution for low amplitude and phase imbalance in order to reduce the odd harmonics (f_o, $3f_o$) at the output [64]. Due to low frequency operation, multiple spiral lines at top (AM) and bottom (LY) layer are vertically coupled with insertion loss of ∼1.5 dB at 2.5−4 GHz (Fig. 4.4b). The center tap on the secondary tap is directly connected to 3 pF degenerated capacitor to provide solid ground, and the bias voltage is applied through it. A push-push balanced 12-um HBTs are used to maximize strong second harmonic output with fundamental and odd harmonic suppression [65]. The simulated S_{11} and

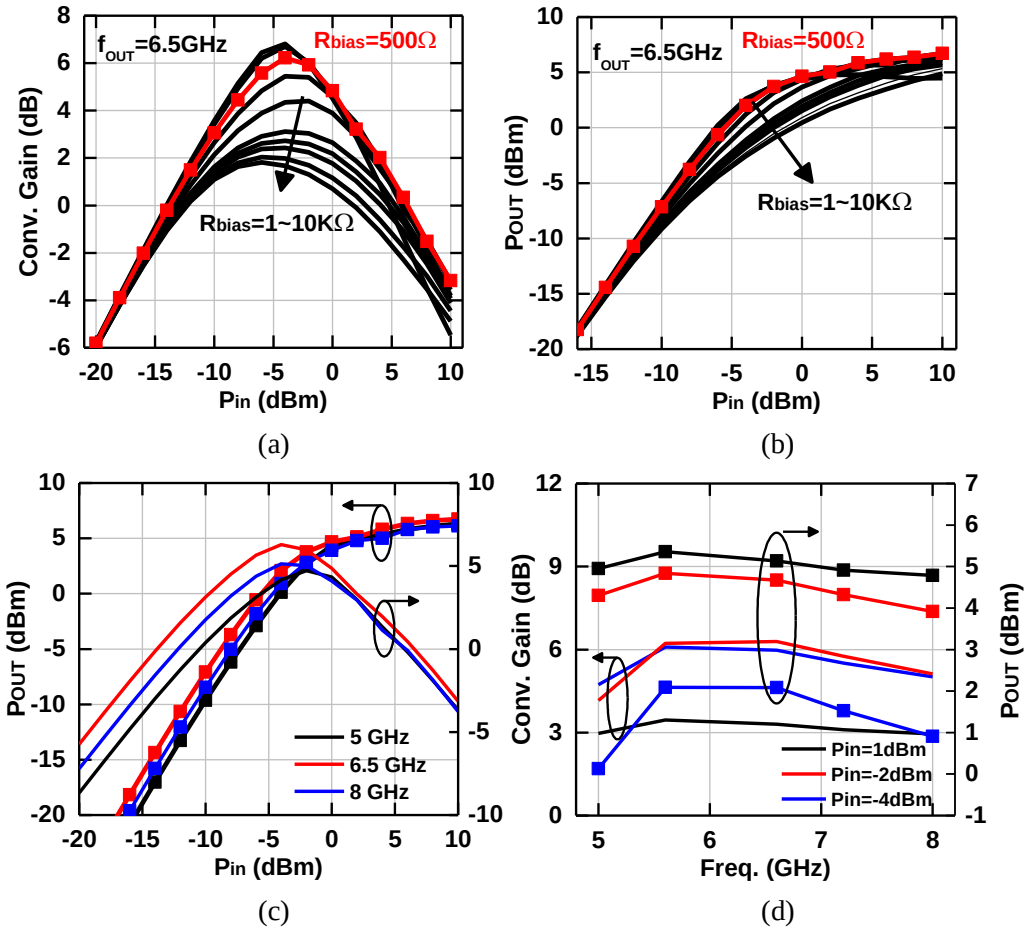


Figure 4.5: Low-band, 1st-stage doubler: (a) Conversion gain, (b) P_{out} vs P_{in} with different R_{bias} (c) conversion gain and P_{out} vs P_{in} with different output frequencies, and (d) conversion gain and P_{out} vs freq.

S_{22} are below -10 dB at $2-7$ GHz, $5-8$ GHz, respectively (not shown). The frequency doubler consumes 15 mA from a 2 V supply at an input power of 1 dBm.

The output power and conversion gain of the frequency doubler are highly dependent on the bias voltage V_{BE}, and it can be determined by bias resistor R_{Bias} (see Fig. 4.4a). The relationship between conversion gain vs R_{Bias}, and P_{out} vs R_{Bias} are described in Fig. 4.5a-b. There is an optimum value that provides enough conversion gain and high output power, and R_{Bias} of 500 Ω is chosen with good compromise. Decreasing R_{Bias} results in reduced V_{BE}, turning transistors into class C region, and this region is generally chosen as a bias point to maximize the output power for $>$100 GHz doubler design, which is difficult to achieve $3-5$ dBm output

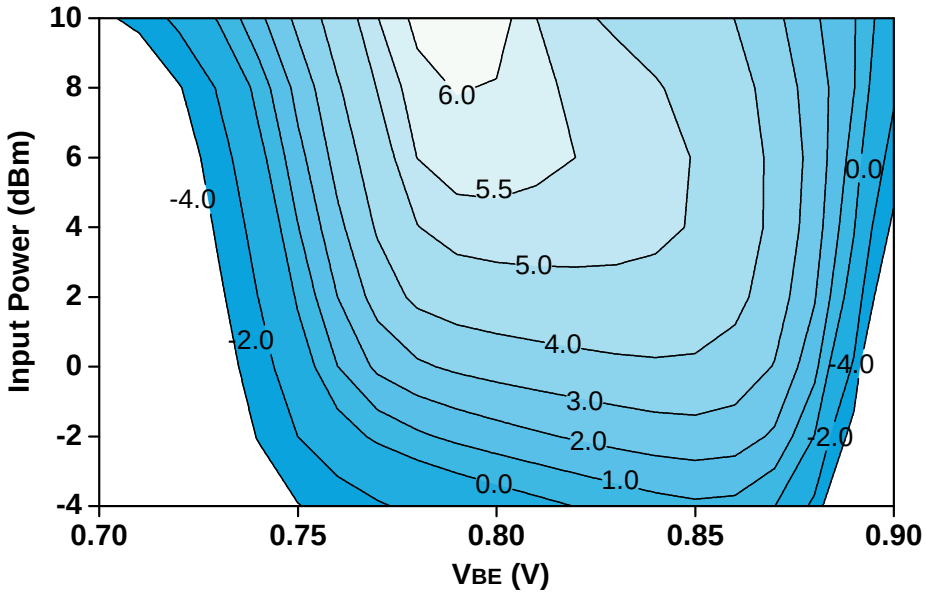
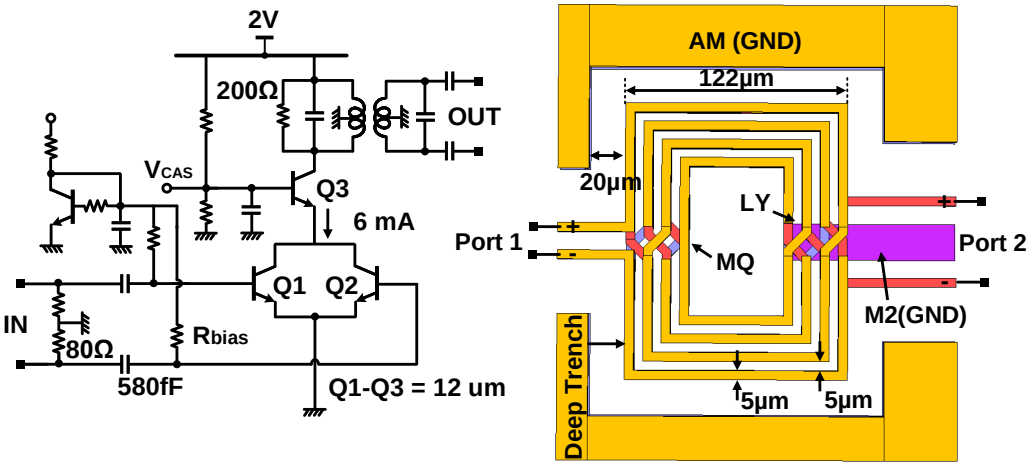


Figure 4.6: Output power contour vs input power and V_{BE} at 6.5 GHz output



(a) (b)

Figure 4.7: (a) Schematic of 1st-stage doubler in mid-band path (input is 5−8 GHz, output is 10−16 GHz), and (b) EM layout of output balun.

power [66]. However, sub-threshold bias operation requires lots of input power to achieve such an output power, and it is not suitable for low-frequency frequency multiplication since class AB or B mode can easily achieve required output power with greatly reduced input power requirement [67]. The peak output power of 5.8 dBm with peak conversion gain of 6.5 dB is simulated at 6.5 GHz, and >5 dBm output power is achieved with P_{in}=1 dBm for entire band (Fig. 4.5c-d). Output

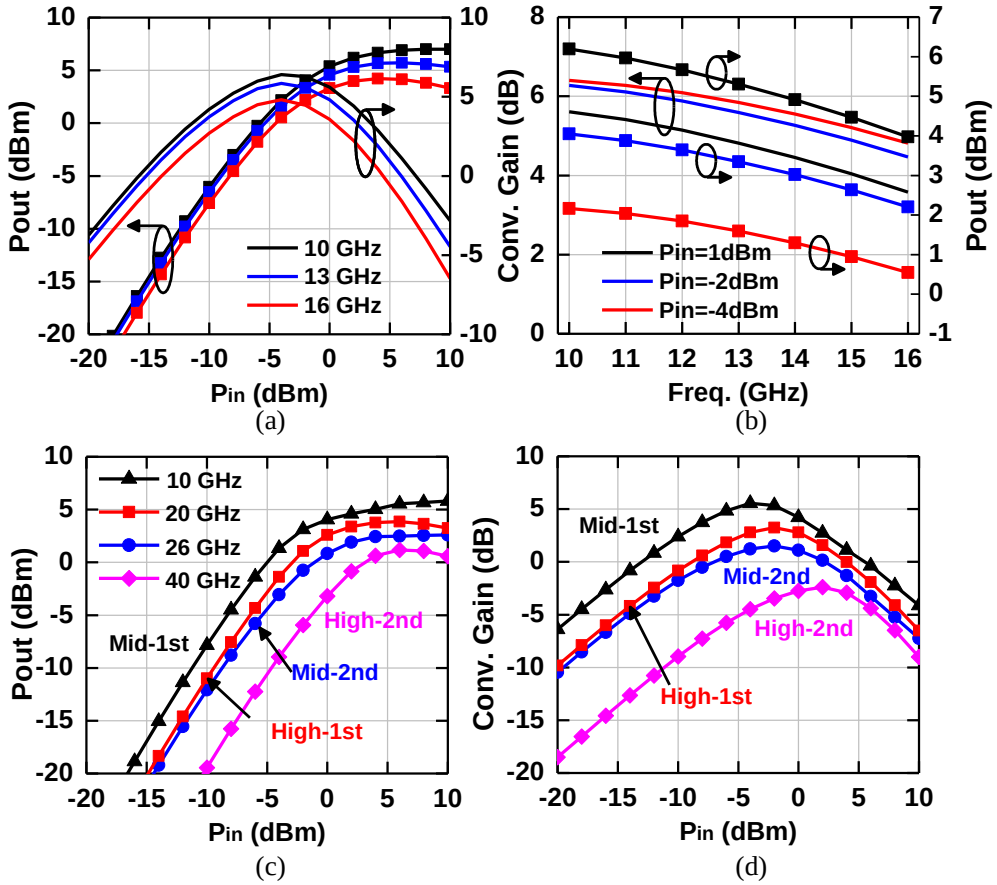


Figure 4.8: Low-band, 2nd-stage doubler:(a) Conversion gain, (b) P_{out} vs P_{in} with different R_{bias} (c) conversion gain and P_{out} vs P_{in} with different output frequencies, and (d) conversion gain and P_{out} vs freq.

power of $\sim$ 5 dBm is required in order to provide enough power to drive next stage doubler after taking into account of insertion loss of bandpass filter (See Section 4.4.2). Fig. 4.5d shows P_{out} and conversion gain vs frequency, showing that its 3-dB BW is larger than 45% FBW. Fig. 4.6 presents the P_{out} contour vs P_{in} and V_{BE} at 6.5 GHz output, and for P_{out} of 5 dBm, static V_{BE} of 0.8 V (slightly higher than threshold) is chosen. Note that V_{BE} drops to 0.7 V for $P_{in} \sim 0$ dBm, turning into class B mode.

Fig. 4.7 presents the schematic and EM structure of the second stage doubler operated at the output frequency of $10-16$ GHz. Similar analysis is done for the second frequency doubler, and the optimum R_{bias} of 2 KΩ is chosen instead of 500 Ω. The output power and peak conversion gain at 10, 13 and 16 GHz is $4-6$ dBm and $3.5-6.2$ dB, respectively (Fig. 4.8a-b). The other

Table 4.1: Design Parameters of 5-8 GHz Switchable Bandpass Filter

C_{1p}	460 fF	L_{1p}	920 pH
C_{2p}	550 fF	L_{1s}	1080 pH
C_{1s}	1450 fF	L_{2s}	370 pH
C_{2s}	620 fF	C_{OFF}	60 fF
C_{3s}	470 fF	T/R	72 µm

four frequency doublers are implemented in the same manner, and its P_{out} and conversion gain are plotted in Fig. 4.8c-d. The $2f_o$, $\lambda/2$ resonators are generally implemented at the input of doubler to further improve conversion gain for sub-terahertz or terahertz multiplier design [66], but is not suitable for this work due to bulky dimension of resonators.

4.4.2 Switchable Bandpass Filters

As discussed in Fig. 4.2, the switch operation in bandpass filter is critical to improve harmonic rejection especially the harmonic contents adjacent to the desired signal. This requires a very sharp rejection at the stopband, and it is challenging to implement on-chip with > 40 % FBW. In order to achieve sharp stopband response, elliptic filter is chosen due to its better rejection at the stopband compared to other types of filter. The order of the filter is carefully investigated to achieve desirable stopband rejection together with acceptable insertion loss and area consumption, and a 3rd-order 3-pole/2-zero elliptic filter is chosen. A 1-bit control switch is employed in series with the capacitors (C_{1p}, C_{3s}) to control the passband of the filter, and its schematic is shown in Fig. 4.9a. The schematic of six bandpass filters is identical except the first-stage fixed bandpass filter at the high-band multiplier chain. The design parameters of the filter for the first-stage bandpass filter at low-band are shown in Table 4.1.

The differential switchable bandpass filter can be simplified by using half-circuit analysis with the case of switch on and off, respectively, and each cases is described as shown in Fig. 4.9b and d. When the switch is on, Fig. 4.9a can be simplified to Fig. 4.9b by adding C_{1p} to

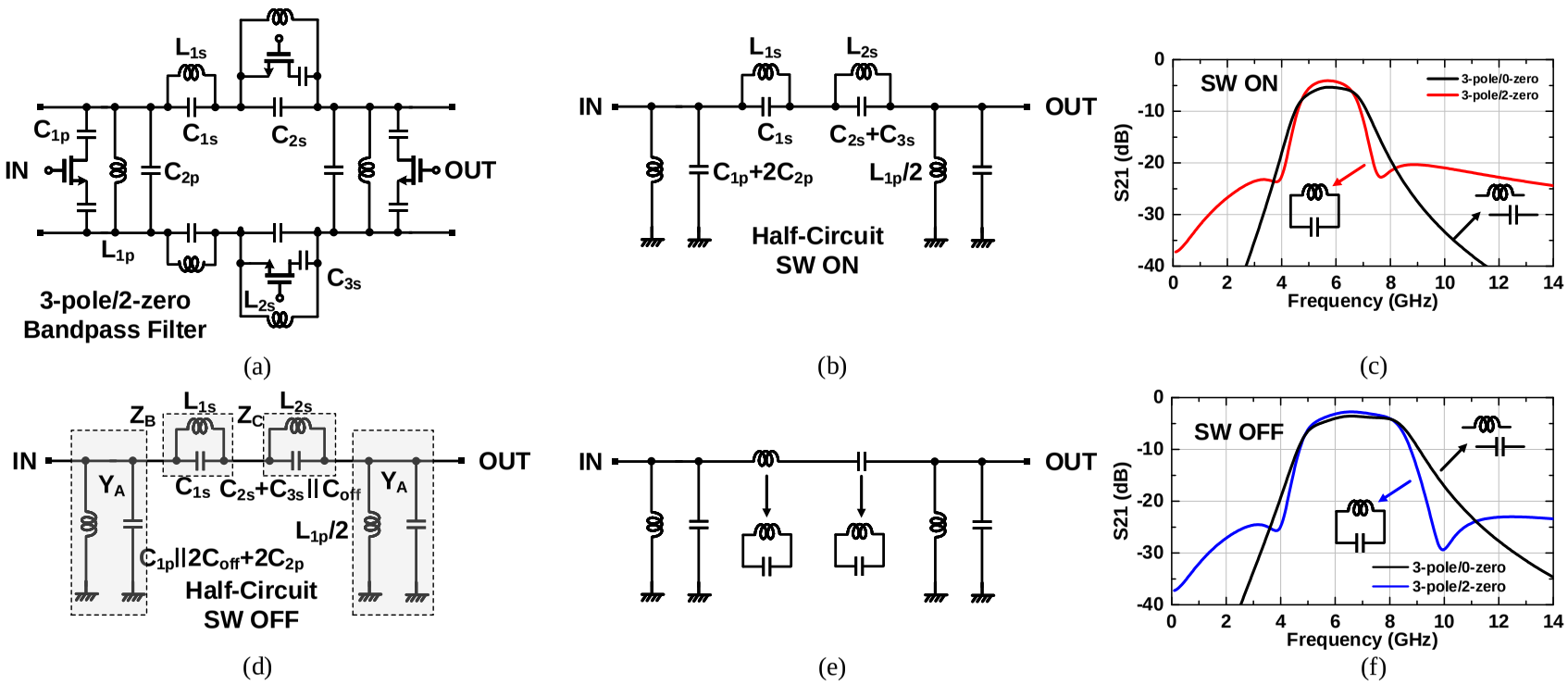


Figure 4.9: (a) Schematic of 1st-stage switchable bandpass filter (low-band), (b,d) half circuit when the switch is on and off, (c,f) S_{21} comparison with 3-pole 0-zero and 3-pole 2-zero when SW is on and off, and (e) simplified schematic of 3-pole bandpass filter.

half-circuit capacitance $2C_{2p}$ in parallel and the C_{3s} to C_{2s} in series. These additional capacitance enables to control the position of the second zero (f_{z2}), resulting in narrower passband. When the switch is off, the effect of C_{OFF} is combined together with C_{1p} and C_{2p} in parallel, and the overall series capacitance becomes C_{2s}+C_{3s} $||C_{OFF}$ (Fig. 4.9d). The location of the two transmission zeros (f_{z1},f_{z2}) can be calculated by

$$f_{z1} = \frac{1}{2\pi\sqrt{L_{1s}C_{1s}}} = 4.02 \text{ GHz} \tag{4.1}$$

$$f_{z2,\text{OFF}} = \frac{1}{2\pi\sqrt{L_{2s}(C_{2s}+C_{3s}||C_{\text{OFF}})}} = 10.08 \text{ GHz} \tag{4.2}$$

$$f_{z2,\text{ON}} = \frac{1}{2\pi\sqrt{L_{2s}(C_{2s}+C_{3s})}} = 7.92 \text{ GHz} \tag{4.3}$$

The location of the poles are derived from the transfer function of the filter, and an easier way to obtain it is to break the circuits into sub-block of each shunt L/C networks and calculate ABCD matrix in series (See Fig. 4.9d). The impedance and admittance of sub-blocks when the SW is off are

$$Y_{\text{A}} = \frac{1}{sL_{1p}}||s(C_{1p}||2C_{\text{OFF}}+2C_{2p}) \tag{4.4}$$

$$Z_{\text{B}} = sL_{1s}||\frac{1}{sC_{1s}} \tag{4.5}$$

$$Z_{\text{C}} = sL_{2s}||\frac{1}{s(C_{2s}||(C_{\text{OFF}}+C_{3s}))} \tag{4.6}$$

Hence, the ABCD matrix of the filter can be simplified

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y_{\text{A}} & 1 \end{bmatrix} \begin{bmatrix} 1 & Z_{\text{B}} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & Z_{\text{C}} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y_{\text{A}} & 1 \end{bmatrix} \tag{4.7}$$

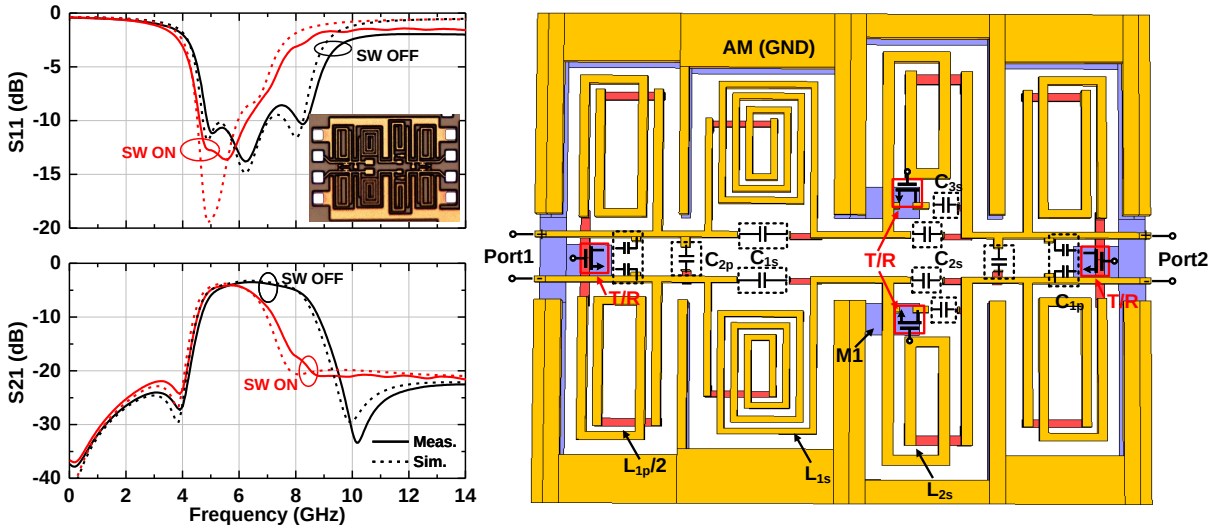


Figure 4.10: (a) S-parameters, and (b) complete EM layout of switchable bandpass filter.

The transfer function is derived from ABCD matrix, and can be written as

$$H(s)_{\mathrm{OFF}} = \frac{2Z_o}{(1+Y_{\mathrm{A}}Z_o)(Z_{\mathrm{B}}+Z_{\mathrm{C}}+(2+Y_{\mathrm{A}}(Z_{\mathrm{B}}+Z_{\mathrm{C}}))Z_o)} \tag{4.8}$$

The structure of the simplified bandpass filter is shown in Fig. 4.9e, which is 3 poles/0 zero structure. Instead of using the basic structure, the series L and C are replaced to the combination of L/C to create two transmission zeros very close to the edges of the passband for improved filter selectivity. The frequency response of 3 poles/0 zero and 3 poles/2 zeros are shown in Fig. 4.9c and f, and additional two zeros provide two null points at the edge of passband, providing higher rejection in vicinity of the passband.

Fig. 4.10a presents the S-parameters of switchable bandpass filter of each switch operation. The passband of the bandpass filter when the switch is off remains 5−8 GHz with the measured insertion loss of 3.5−5 dB (simulated 3−4.5 dB). When the switch is ON, its passband becomes 5−6.5 GHz with the insertion loss of 4−5.5 dB (simulated 3.7−4.6 dB). Slightly high insertion loss is due to high-order filter design with low-Q inductors (Q of 8−10) at low frequency as well

Table 4.2: Performance Summary of Six Bandpass filters

Freq. (GHz)	Band	S_{21} (dB)	Freq. (GHz)	Band	S_{21} (dB)
5−8	Low	3.5−5 4−5.5	10−16	Low	3.6−5.4 4−5.8
8−13	Mid	3−4.8 4.3−4.8	16−26	Mid	3.4−4.8 4.6−5.6
13−20	High	2.8−3.8	26−40	High	3.9−5 4.4−5.6

as the integration with relatively lossy switches compared to the switch in CMOS technology. Still, the output of the bandpass filter is enough to drive the next-stage frequency doubler. The return loss of each case is <-10 dB at desired bandwidth. The filter measurement is done by using fully differential 4-port PNA-X (Keysight N5247A).

Fig. 4.10b shows the layout of the switchable bandpass filter. Due to the presence of many inductors together with switches inside the passive structure, careful EM modeling is necessary in order to predict RF performance accurately. The electromagnetic (EM) simulation of entire structure takes account of all possible couplings between inductors as well as the effect of the ground plane around the CMOS transistor, and is performed by 2.5-D EM simulator [68]. The bottom ground plane of the inductors are not used to minimize the parasitic capacitance for low-loss, high-inductance design with a compact size [69]. The measured S-parameters shown Fig. 4.10a matches the simulation result well based on thorough EM analysis. Identical analysis is performed for all other bandpass filter with different circuit parameters, and Table 4.2 summarizes the measured six bandpass filters in three bands.

4.4.3 SP3T Switches and amplifier

The input single-pole-three-through (SP3T) is implemented before the multiplier chain in single-ended, with simulated insertion loss of 0.8−1 dB at 2.5−10 GHz. For switching transistor, triple-well device is used to improve the isolation. The output SP3T, however, is

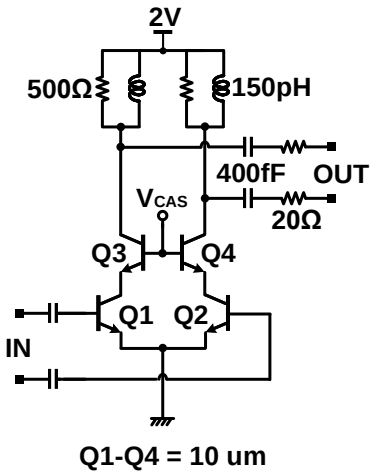


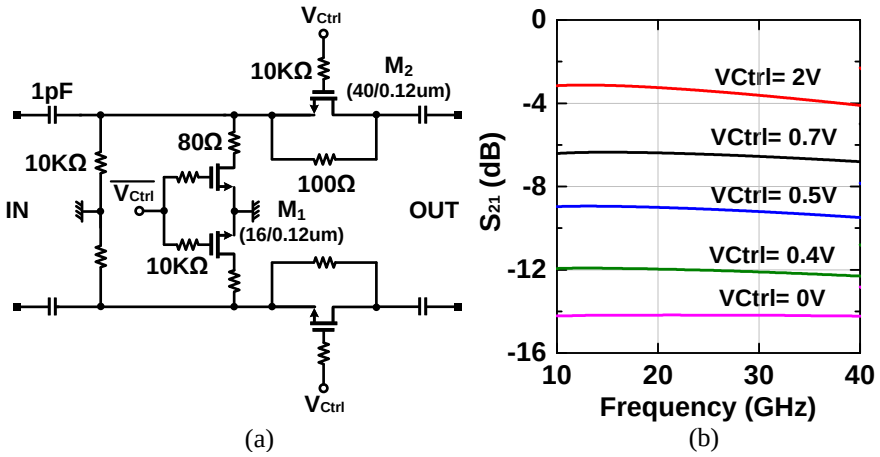
Figure 4.11: Schematic of high-band amplifier.

a differential input/output and its transistor size is carefully chosen to minimize the effect of parasitic capacitance at 20−40 GHz. As a result, a 48-µm wide device is selected and its simulated insertion loss is 1.6−3.6 dB at 10−40 GHz. In general, frequency roll-off at 20−40 GHz can be improved with peaking inductors, but it was not implemented at the end since its improvement is only ∼1 dB and it requires a pair of inductors at the each bands, which leads to additional 1 mm^2 area consumption.

Fig. 4.11 presents the schematic of the amplifier. This amplifier is only implemented in high-band path to compensate lower conversion gain of the frequency doublers and switch loss. The function of this amplifier is to improve output power and it is operated in non-linear region, resulting in high harmonic 3rd harmonic contents ($12f_o$). However, $12f_o$ component at high-band is located at 78−120 GHz, and it is greatly attenuated after amplification stages. The small signal gain of the amplifier is 9−10 dB at 26−40 GHz, but its actual gain is 4−6 dB with the OP_{1dB} of -3 dBm. The bias current of the amplifier is 4 mA per branch.

4.4.4 Variable Resistive Network

Variable resistive network is implemented after 3-band frequency multiplier chains in order not to saturate following active splitters and power amplifier at the output (Fig. 4.12a).



(a) (b)

Figure 4.12: (a) Schematic of variable resistive gain network, and (b) simulated S_{21} with different gain settings.

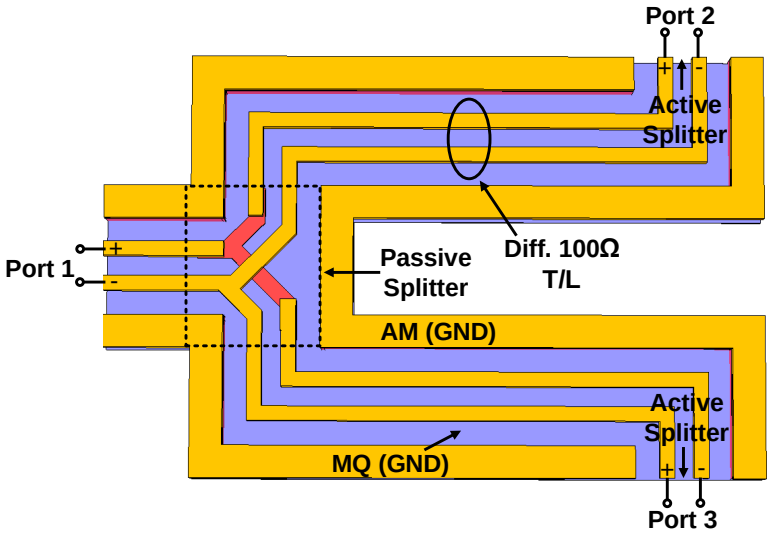


Figure 4.13: Layout of 1:2 passive splitter.

The attenuation level is controlled by gate voltage (V_{Ctrl}) of the series and shunt transistor (M1 and M2) and attenuation level is from -3.5 to -15 dB (11.5 dB gain control) at 10−40 GHz. The attenuation level with several different V_{Ctrl} is shown Fig. 4.12b. The attenuation level is changed rapidly around the threshold of the transistor (V_{Ctrl}=0.4 V). Linear attenuation steps can be achieved digitally by N-bit control, but it was not chosen due to limited available number of pads surrounding the flip-chip.

4.4.5 1:2 Passive Splitter

A 1-to-2 passive splitter is implemented shown in Fig. 4.13. A cross-coupled passive splitter is followed by differential 100 Ω transmission lines and 1:2 active splitters. The simulated loss of 1:2 passive splitter is 0.6−0.8 dB at 10−40 GHz with the size of 300 µm × 250 µm.

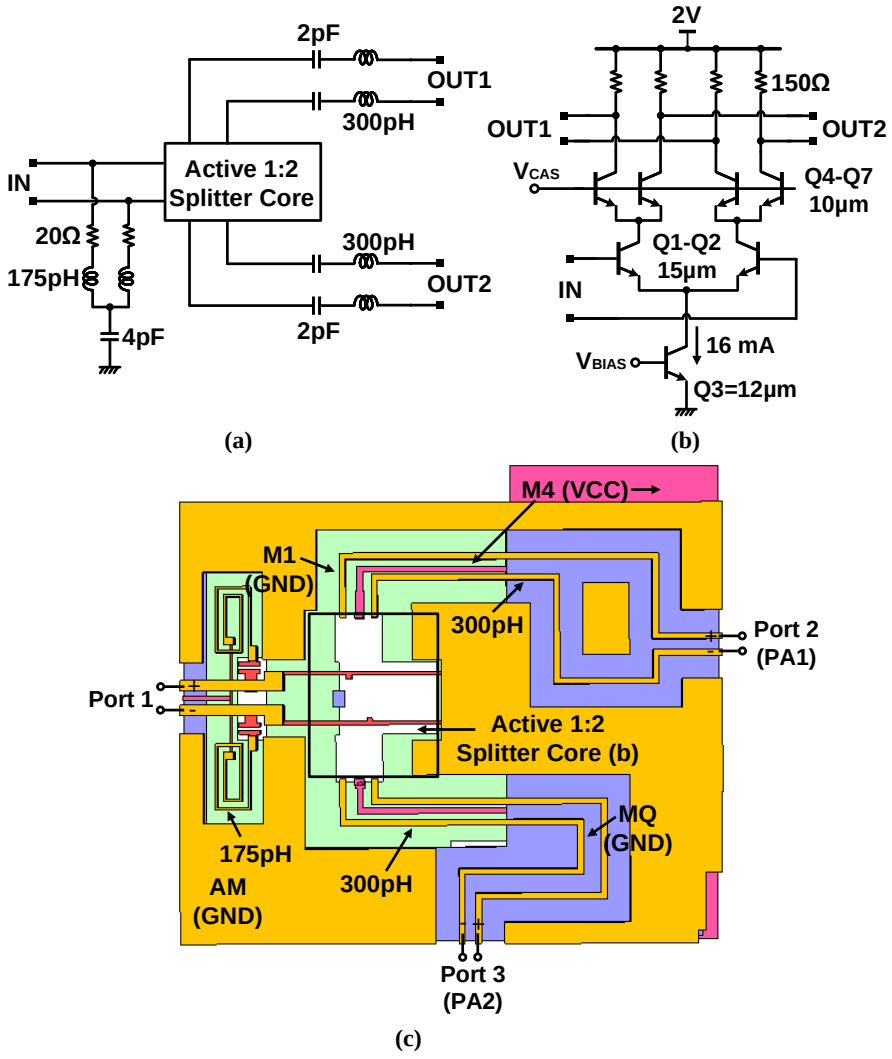


Figure 4.14: (a) Block diagram of 1:2 active splitter, (b) schematic of 1:2 active splitter core, and (c) EM layout of the active splitter.

4.4.6 1:2 Active Splitter

The block diagram of 1:2 active splitter is shown in Fig. 4.14a. A pair of 175 pH inductors are used together with 20 Ω resistors to provide matched condition from the previous stage. The active splitter core is shown in Fig. 4.14b and current splitting method is used in order to keep the linearity as well as to achieve high channel-to-channel isolation (-42 to -36 dBc). For this design, there is no control pin to turn on/off each splitter channel, but it can be done without degrading P_{out} and isolation by adding one dummy transistor at the common base. The active splitter consumes 16 mA through the current source. Careful biasing is required due to limited voltage headroom for three biplolar transistors, and V_{CB} of the CE and CB transistor is chosen to -0.3 V. If V_{CB}= -0.3 V and in order to keep $f_T > 150$ GHz and avoid kirk effect, current density should be between $0.4-1.5 \text{mA}/\mu\text{m}$, but for large signal operation, DC biasing should be $0.2-0.75$ mA/μm [70]. Therefore, the current density of 0.53 mA/μm and 0.4 mA/μm are chosen for CE and CB devices, respectively. For compact design, resistive loads are used for two differential pairs, and 300 pH of inductors are implemented to compensate high-frequency gain roll-off. The layout of the active splitter is carefully designed, and the passive structures and transmission lines are simulated together with RC-extracted splitter core (Fig. 4.14c). The simulated gain of the splitter is $4-9$ dB at $10-40$ GHz, with the OP_{1dB} of $-4-$-3 dBm, which is enough to drive PA.

4.4.7 PA with 1-bit Filter

The schematic of PA is shown in Fig. 4.15a. Wideband input matching is achieved by the feedback resistors and inductors in the previous stage. A psuedo-differential topology is implemented for improved linearity and 600 pH load iuductance is carefully designed for broadband gain response at $10-40$ GHz. In order to prevent low self-resonant frequency, the spiral inductor is placed under the deep trench isolation (DTI) without any metal grounds to

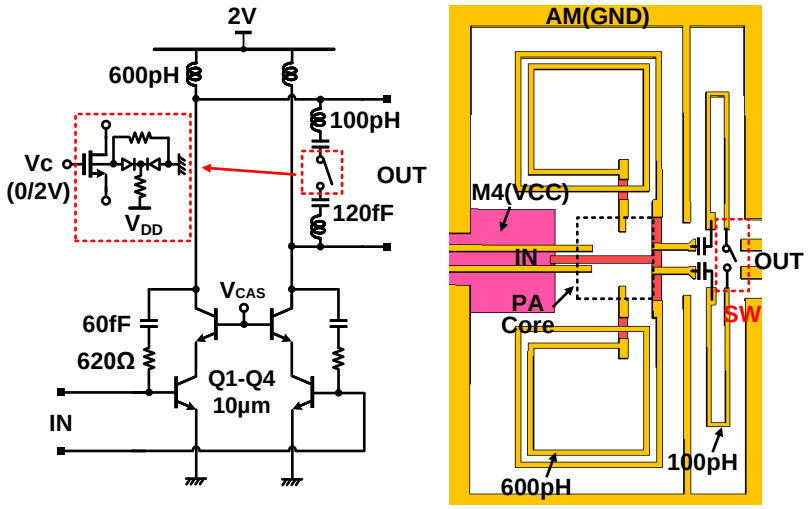


Figure 4.15: (a) Schematic of PA, (b) EM layout of PA.

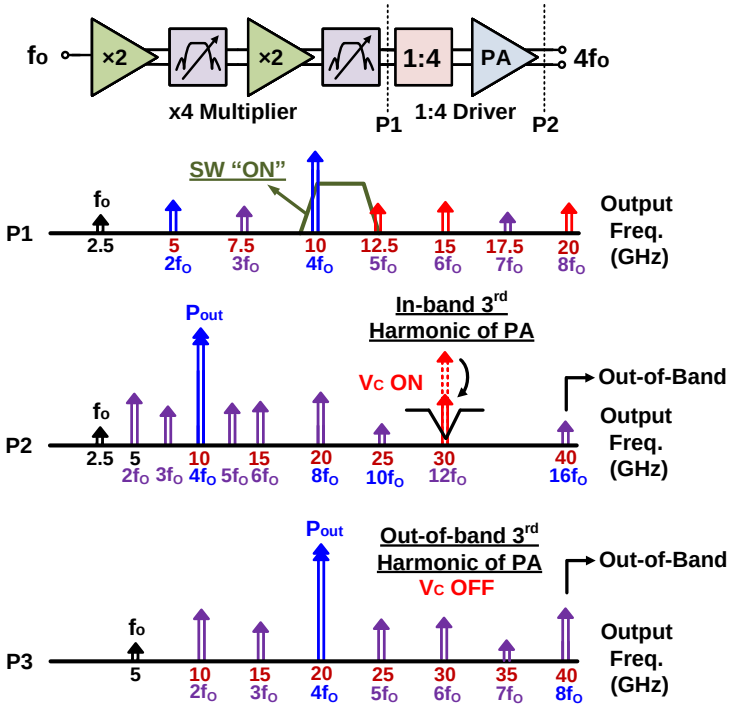
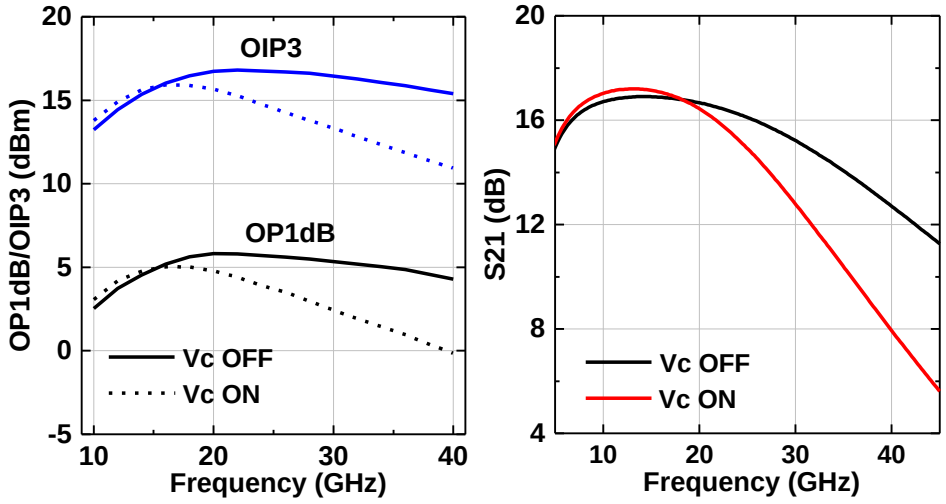


Figure 4.16: Operation of the notch filter in PA for 3rd harmonic (12th harmonic from the input) cancellation.

minimize the parasitic capacitance (Fig. 4.15b).Due to its nature characteristic of having higher 3rd order harmonic for higher input power, the simulated $3f_o$ ($12f_o$ from the input) level is



(a) (b)

Figure 4.17: Simulated (a) OP_{1dB}, OIP3, and (b) S_{21} of PA.

around ∼-25 dBc when PA approaches P_{1dB}. This $12f_o$ becomes the dominant harmonic content, especially when $12f_o$ is located at in-band of the interest (30−40 GHz). Therefore, additional ∼5 dB more rejection is necessary for > 30 dBc HRR, and it can be achieved by additional 1-bit (V_C) switch at the output node to control the gain response. The 1-bit switch operation is described Fig. 4.16. The input signal of 2.5 GHz is multiplied by 4 through the multiplier chain with >30 dBc HRR and, Fig.4.16-P1 shows all harmonics presented after the multiplier chain. Due to amplification stage, when the main tone approaches 3 dBm (close to the P_{1dB}) at 10 GHz, its 3rd harmonic content, $12f_o$ at 30 GHz, becomes the largest in-band harmonics (Fig.4.16-P2). The function of a 1-bit switch is to drop the high-frequency gain while keeping the gain of main tone, resulting in improved HRR by ∼5 dB. When the input frequency is at 5 GHz (Fig.4.16-P3), the desired signal is located at 20 GHz and its 3rd harmonic is located at 60 GHz, which is out-of-band of the bandwidth. Therefore, V_C is OFF to maximize the output power. Moreover, the gain of PA rolls up rapidly after >45 GHz, it automatically rejects high frequency harmonics, therefore, the effect of $12f_o$ becomes minimal. The simulated OP_{1dB} of PA is 3−5 dBm (V_C OFF) and 0−5 dBm (V_C ON), and V_C is only activated when the output frequency is <20 GHz (Fig.

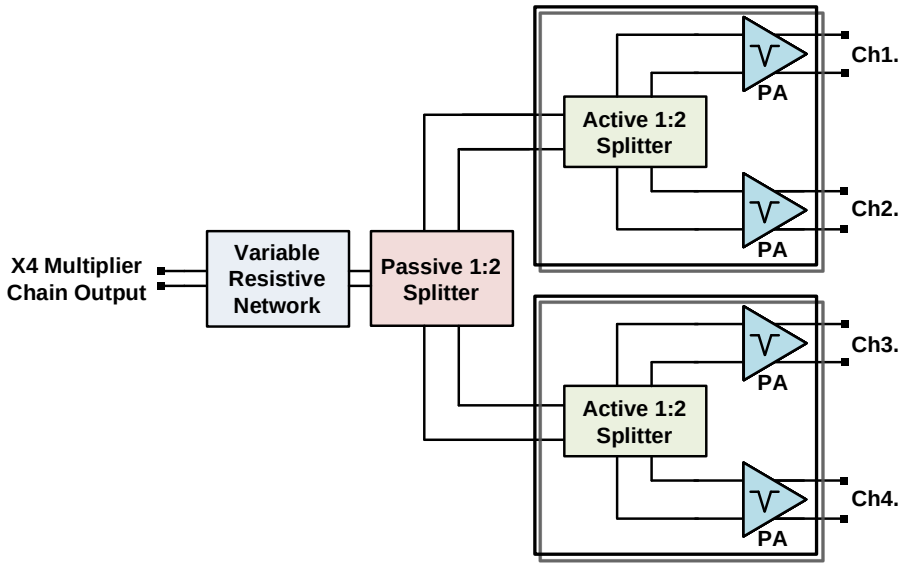


Figure 4.18: Block diagram of 1:4 TX driver.

4.17a). Fig 4.17(b) presents the simulated S_{21} of the PA for each switch operation.

4.4.8 1-to-4-Channel TX driver

Fig. 4.18 presents the block diagram of the 1:4 TX driver. The S_{21}, OP_{1dB}, and HRR of the standalone 1:4 TX driver is simulated to clarify whether the HRR limiting factor comes from multiplier chain or 1:4 TX driver (Fig. 4.19). The switch in PA reduces the gain by $4-8$ dB at $30-42$ GHz range, improving worstcase HRR by the same amount for $10-14$ GHz signal coming from the $\times 4$ multiplier chain ($2.5-3.5$ GHz from the input). The switch operation at PA can lead to HRR $>$ 40 dBc up to for $>$ 22 GHz output, but is mainly operated in $10-14$ GHz range since the limiting factor of HRR at $>$15 GHz output is not 3rd harmonic of TX driver ($12f_o$ from the input), but other harmonics generated by multiplier chain ($2f_o$, $6f_o$, $8f_o$, etc). The OP_{1dB} of the 1:4 TX driver is -0.5 to 5.3 dBm when the switch is on and OP_{1dB} drop is mainly coming from reduced gain at $>$ 25 GHz to improve HRR, but it can be recovered to 3.5 to 5.5 dBm by switching off V_C. The gain control range of 1:4 TX driver is $\sim$ 12 dB, coming from the variable resistive network. The required input dynamic range of 1:4 TX driver for +3 dBm P_{out} is -9.5 to

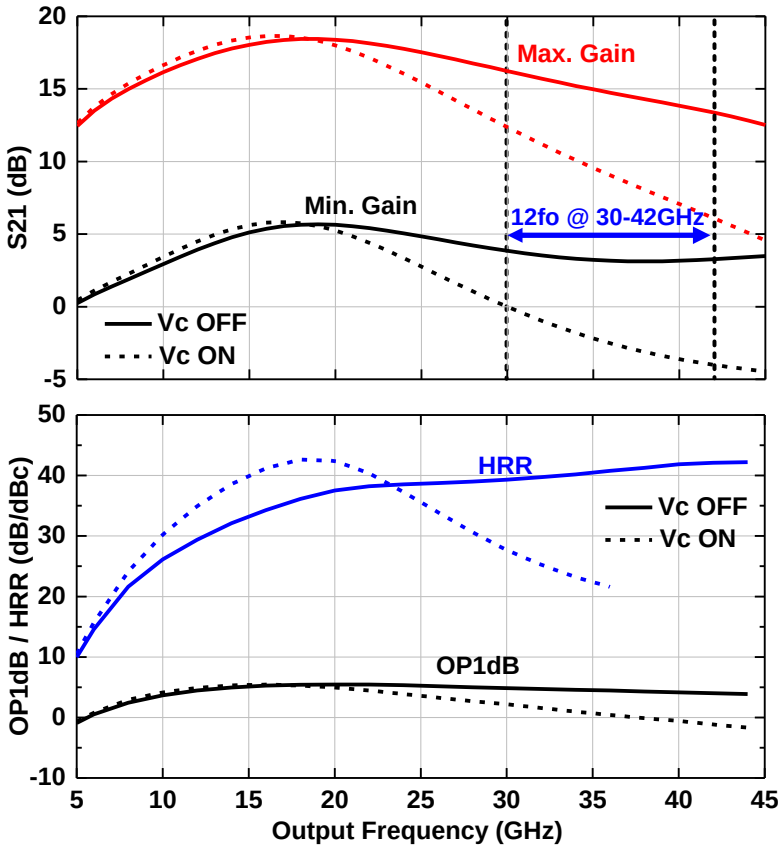


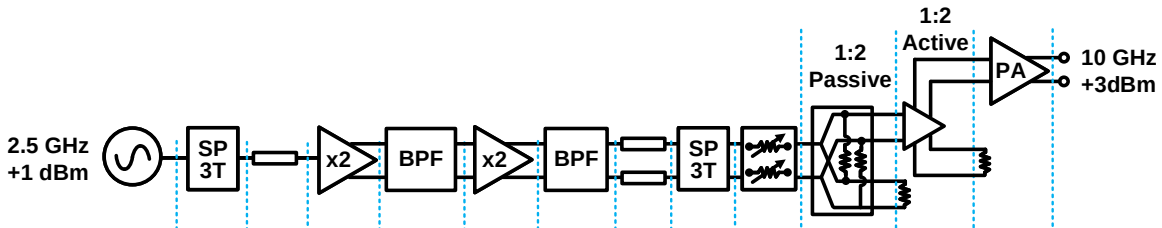
Figure 4.19: Simulated S_{21}, OP_{1dB}, and HRR of 1:4 TX driver.

-2 dBm, which is enough to generate from the x4 multiplier chain.

4.4.9 System simulation

Fig. 4.20 presents the output power and HRR of several critical harmonics ($2f_o$, $5f_o$, $6f_o$, $8f_o$ and $12f_o$) at the output of each blocks with the input of 2.5 GHz and the output of 10 GHz at +1 dBm input power.

The gain setting voltage, V_{Ctrl}= 0.37 V from variable resistor network, is applied in order to set the output power of +3 dBm. The switches in two bandpass filters are turned on for better harmonic rejection of $5f_o$, $6f_o$, and the switch in PA is also turned on to reject $12f_o$ further by $4-5$ dB. The worstcase HRR is $\sim$31 dBc and it is from $12f_o$ (3rd harmonic PA). Fig. 4.21 shows the simulated output power and HRR with different harmonic contents at $10-40$ GHz. Note that



HRR2 (dB)	57	52	N/A	N/A	23	35	35	34	34	34	35	37
HRR5 (dB)	52	52	41	50	44	49	48	48	48	48	48	49
HRR6 (dB)	50	50	24	38	32	40	40	40	40	41	41	33
HRR8 (dB)	51	51	39	49	19	29	29	29	29	29	29	32
HRR12 (dB)	57	56	56	59	38	41	41	41	41	41	41	31
P_{out} (dBm)	1.5	1.4	4.7	-0.3	4.1	-0.8	-1	-2.5	-16.8	-20.3	-12.7	3

Figure 4.20: Simulated P_{out} and HRR after each building blocks for system-level simulation.

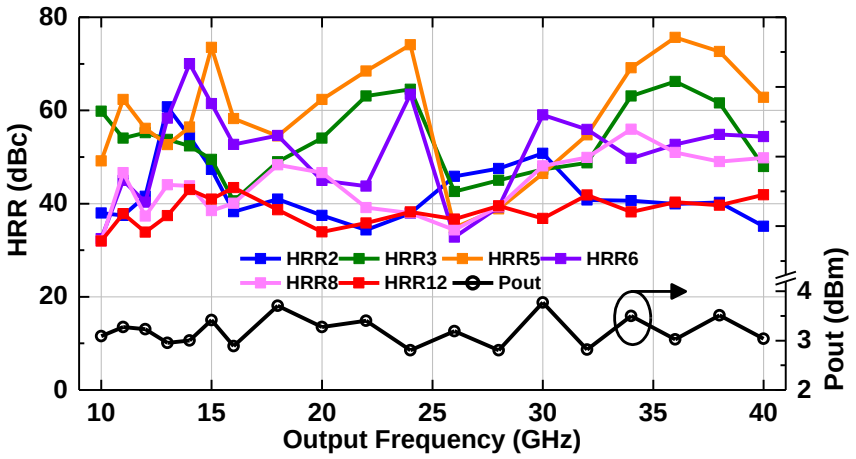


Figure 4.21: Simulated P_{out} and HRR at 10−40 GHz.

higher order harmonics ($12f_o$, $8f_o$, $6f_o$, etc) become out-of-band when the output frequency is increased (i.e, f_o= 10 GHz, $6f_o$= 60 GHz, $8f_o$= 80 GHz, $12f_o$= 120 GHz), and is not taken into account for worstcase HRR calculation. The simulated output power and HRR at channel 1−4 has <0.2 dB, <0.5 dB difference, respectively, providing identical performance at each output channels.

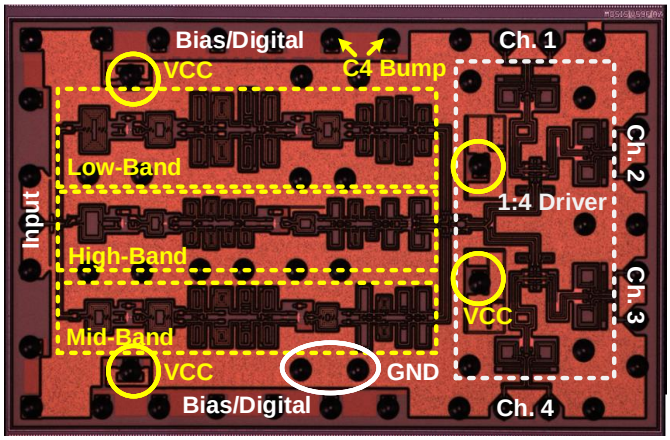


Figure 4.22: Chip microphotograph of 4-channel 10−40 GHz frequency quadrupler (3.65 × 2.2 mm^2).

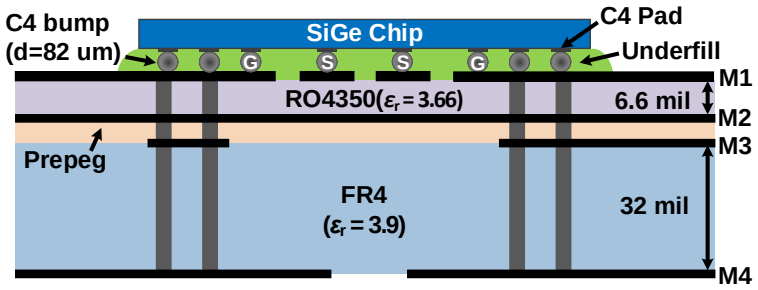


Figure 4.23: Cross-section of the printed circuit board with the SiGe flip-chip (RO4350B+FR-4).

4.5 Packaging

The chip was fabricated in the GF8HP 0.12-µm SiGe BiCMOS process. The multiplier chain consumes 60−84 mW with an input power of +1 dBm, and 1:4 TX driver consumes 236 mW from a 2 V supply (39 mW for each PA, 40 mW for 1:2 active splitter), resulting in overall power consumption of 296−320 mW. For one-channel operation, only 139−163 mW is needed, but from current design, there is no control to turn each active splitter and PA on and off individually. Fig. 4.22 shows the chip microphotograph of 4-channel frequency quadrupler, with the size of 8.03 mm^2 (3.65 × 2.2 mm^2). The chip is flipped directly on PCB to minimize inductance from the connection. 82-µm diameter, 70-µm height lead-free C4 bumps (Sn 0.5%AgCu) are placed on top of the pad layers, with expected inductance of ∼50 pH (Fig. 4.23).

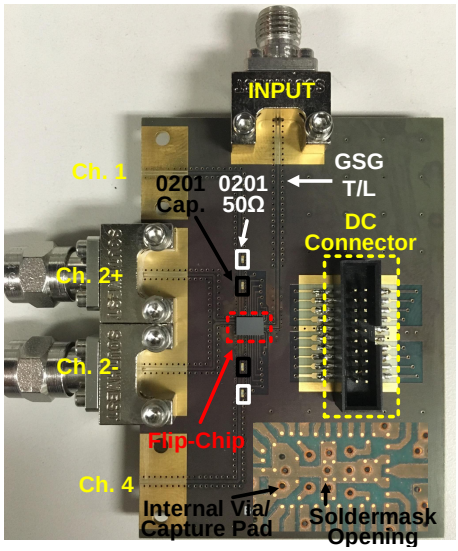


Figure 4.24: A connecterized 10−40 GHz quadrupler with flip-chip packaging.

Due to large number of pins required to control the chip and minimum pitch size of 250 µm for physical requirement of PCB fabrication, four V_{CC} pins are implemented internally to locate them closer to the most power consuming building blocks (i.e., PAs). The ground bumps are well distributed throughout the chip for proper heat removal, minimal ground inductance and mechanical stability. This flip-chip is placed on the a low-cost 6.6 mil Rogers 4350B laminate (ε_r = 3.66, $\tan\delta$ = 0.004 at 10 GHz) to deliver high frequency signals, on top of which a 32 mil FR-4 is used under it as a DC routing as well as mechanical support. Fig. 4.23 describes top-view of 10−40 GHz quadrupler chip on the PCB. For measurement purpose, only channel 2 output is routed out in differential, and two single-ended outputs are taken out in a single-ended manner with 0201 50 Ω termination on PCB. A differential 100 Ω ground coplanar waveguide (GCPW) line (W/S=11/5 mil) and single-ended 50 Ω GCPW line (W/S=14/5 mil) are used as a transmission line, and its loss and reflection coefficient are carefully designed by ADS momentum [71]. Fig. 4.25a shows two different paths from the flip-chip to the outputs. Path 1 (A) is connected to shorter line (0.75 inch), and is routed to the output (Ch. 2+). Path 2 (B) is connected to longer line (1.3 inch), and it is routed out to the output (Ch. 1). The RF routing of Ch.2- and Ch.4 are identical and vertically symmetrical. Fig. 4.25b shows the simulated reflection

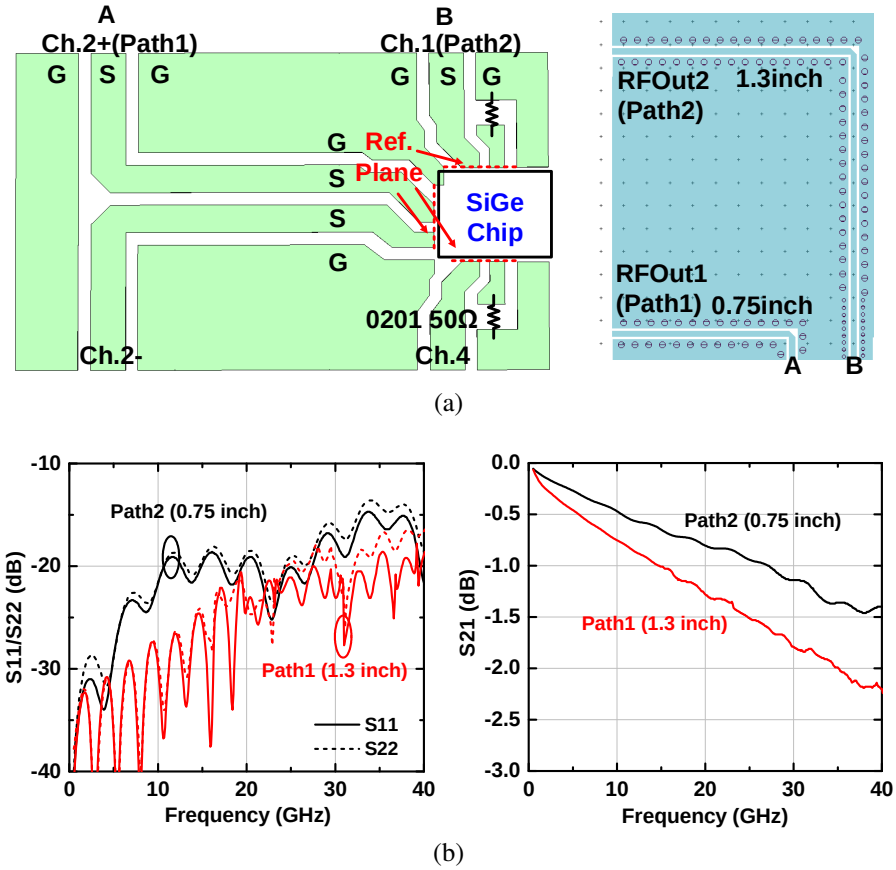


Figure 4.25: (a) RF output EM model for two different paths and (b) simulated S-parameters of both paths

coefficient and loss of two RF paths. Both lines have S_{11} of <-15 dB at 10−40 GHz, with the loss of 0.5−1.5 dB for Path 1 and 0.8−2.2 dB for Path 2.

4.6 Measurements

4.6.1 ×4 Multiplier Chain

The measurement of the multiplier chain itself is reported in [72]. The output power and harmonic contents with switch operation of bandpass filter, band selection is presented with worstcase HRR of > 30 dBc at 11−40 GHz (> 25 dBc at 10−11 GHz) and output power of -8 to +1 dBm.

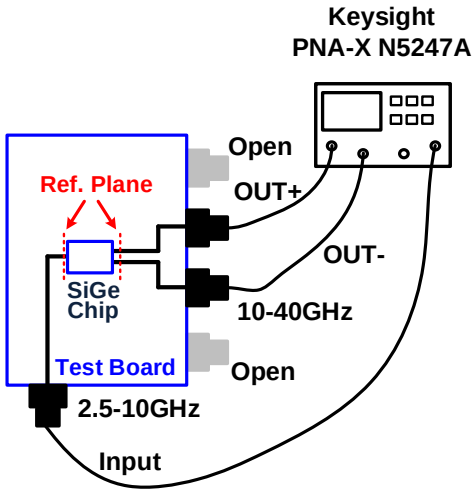


Figure 4.26: Measurement setup of 10−40 GHz frequency quadrupler.

It is also implemented as an LO path to drive down-conversion mixer for wideband imaging system [73].

4.6.2 ×4 Multiplier Chain with 1-to-4 Channel Driver

The 10−40 GHz quadrupler flip-chip on the PCB shown in Fig. 4.23 is measured using a Keysight N5247A PNA-X (Fig. 4.26). Due to the capability of using it as a signal source and a spectrum analyzer, both input and output are connected to N5247A. A 2.5−10 GHz single-ended signal is applied through the southwest connector attached to the PCB, and 10−40 GHz differential output signals are directly connected to PNA-X. The power calibration is performed by using power sensor and electronic calibration kit (E-Cal). The reference plane of the measurement is the input and output of the flip-chip, and the loss of external cables, connectors, and transmission line on the PCB are de-embedded.

The measurements are done with following steps : 1) Gain setting (V_{Ctrl}) vs P_{out} and HRR at low-band, 2) P_{out} and HRR with the effect of switch (SW) in bandpass filters, 3) P_{out} and HRR 1-bit switch in PA (V_C), and 4) overall performance with proper control parameters of each bands at 10−40 GHz.

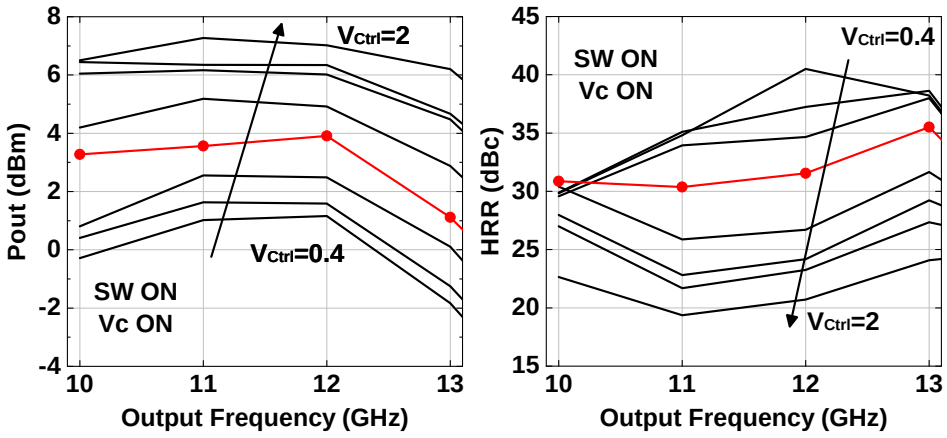


Figure 4.27: Measured P_{out} and HRR with different gain settings when filter SW is ON at low-band (10−13 GHz).

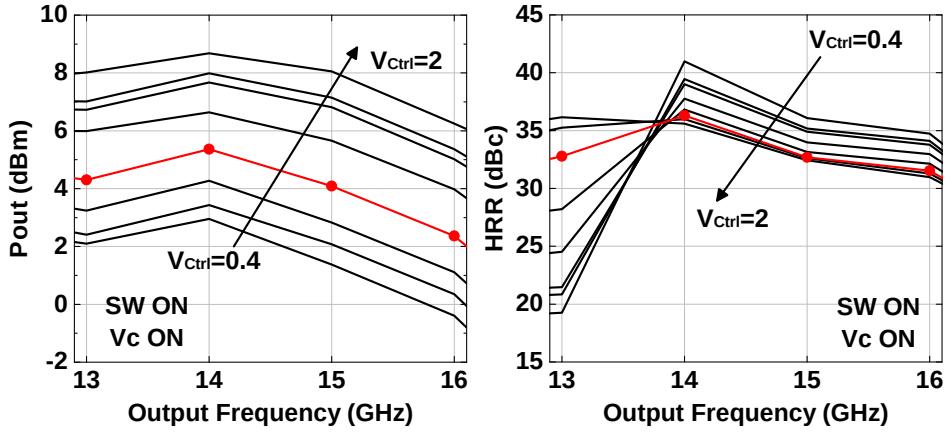


Figure 4.28: Measured P_{out} and HRR with different gain settings when filter SW is OFF at low-band (13−16 GHz).

Gain setting vs P_{out} and HRR

Fig. 4.27 and Fig. 4.28 present the measured P_{out} and HRR with different gain settings (V_{Ctrl}) at low-band operation (10−16 GHz). Other design parameters, such as P_{in} (1 dBm), switch in PA (V_C), switch in bandpass filter (SW) are fixed to investigate the effect of gain settings only. The maximum P_{out} of 6−7 dBm and 7−8.5 dBm is measured at 10−13 GHz and 13−16 GHz, however, the corresponding HRR is 19−22 dBc, 19−30 dBc, respectively. When V_{Ctrl}=0.5 V, P_{out} of 3−4 dBm with HRR of 30−39 dBc is measured at 10−16 GHz.

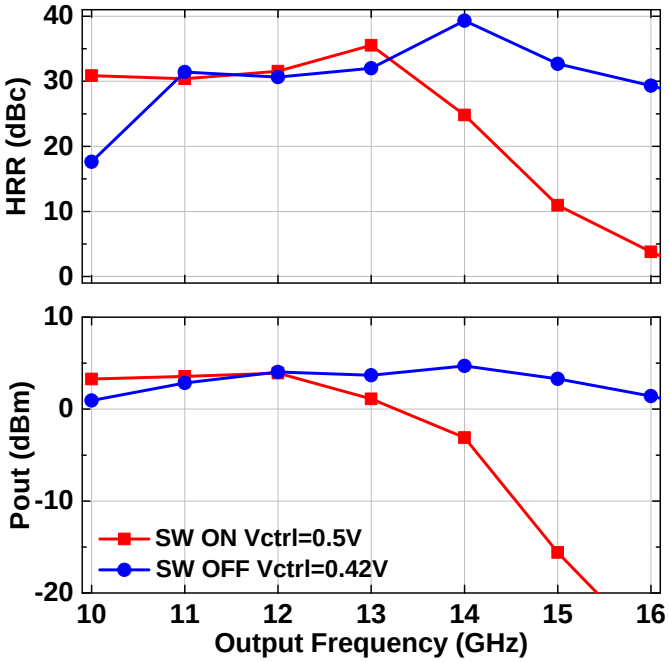
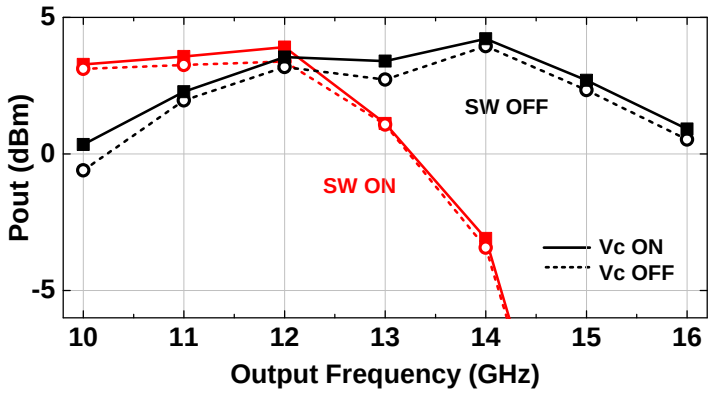


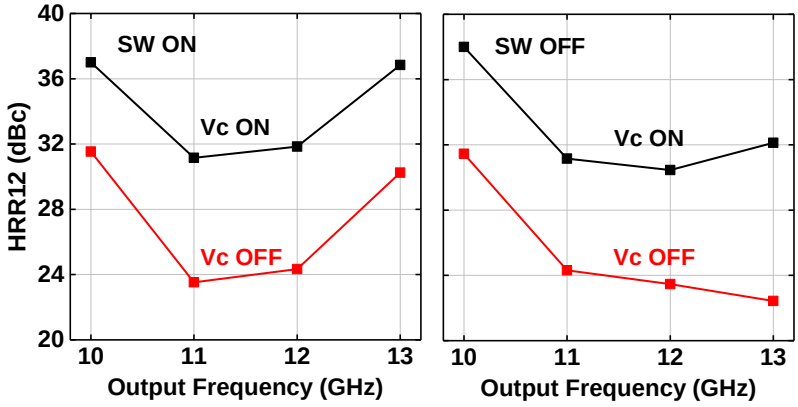
Figure 4.29: Measured P_{out} and HRR with filter SW ON/OFF operation.

P_{out} and HRR with the effect of switch in bandpass filter

Fig. 4.29 shows measured P_{out} and HRR with the switch operation in bandpass filter. When the switches are turned on, the passband of two bandpass filters are reduced, improving HRR at low-edge of the band (10−12 GHz). However, when the switches are off, the passband of two bandpass filter remains unchanged to pass the signal up to 16 GHz. The HRR of $2f_o$, $3f_o$, $5f_o$, $6f_o$ can be improved by switch operation especially at low-edge (10−12 GHz), however, the overall worstcase HRR is limited by the 3rd harmonic of 1:4 TX driver ($12f_o$). Note that only in-band $12f_o$ is taken into account for worstcase HRR, therefore any $12f_o$ >40 GHz is not included in HRR calculation. The output power of ∼3 dBm can be obtained from the measurement with different gain state for either switch operation with worstcase HRR of 30−40 dBc at 10−16 GHz.



(a)



(b)

Figure 4.30: (a) P_{out} and HRR vs Freq with V_C ON/OFF, and (b) HRR12 vs Freq with V_C ON/OFF when SW is ON (left) and OFF (right).

P_{out} and HRR with the effect of switch in PA

Fig. 4.30a-b show the measured P_{out} and HRR with the 1-bit switch in PA. Since $12f_o$ content is only considered as an in-band harmonic up to 13 GHz output ($4f_o$), $10-13$ GHz region is main interest of rejecting $12f_o$ with 1-bit switch operation. Fig. 4.30a shows the output power with V_C ON and OFF of the PA with switch operation (SW) in the bandpass filter, and output power difference of $\sim$1 dB is measured between V_C ON (dashed line) and V_C OFF (solid line) state, as expected from Fig. 4.19. Fig. 4.30b describes measured HRR12 at $10-13$ GHz output when the bandpass switch (SW) is ON (left) and OFF (right).

The measured HRR12 when V_C is ON at $10-13$ GHz is $30-36$ dBc (left), $31-38$ dBc

Freq (GHz)	10	11	12	13	14	15	16
SW	ON			OFF			
VC	ON						
V_{Ctrl}	0.5			0.42	0.4	0.42	0.5

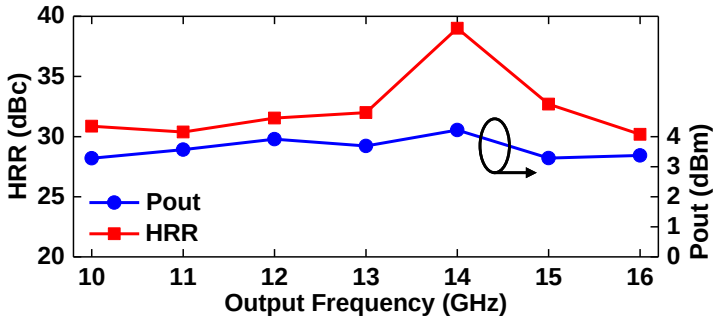


Figure 4.31: Summarized P_{out} and HRR vs Freq. at low-band operation.

Freq (GHz)	16	17	18	19	20	21	22	23	24	25	26
SW	ON			OFF							
VC	ON				OFF						
V_{Ctrl}	0.5	0.45			0.6	0.5	0.6		0.8	2	

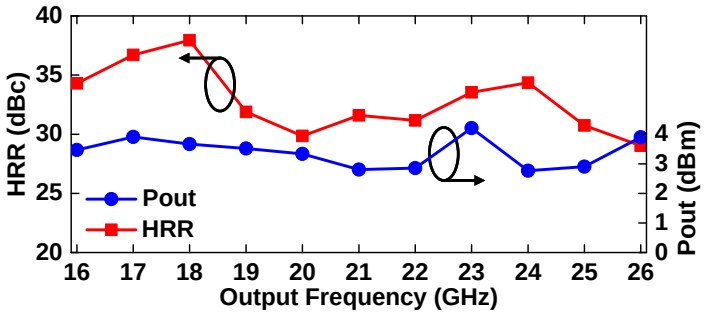


Figure 4.32: Summarized P_{out} and HRR vs Freq. at mid-band operation.

Freq (GHz)	26	28	30	32	34	36	38	40
SW	ON	OFF						
VC	OFF							
V_{Ctrl}	0	1	0.8	1	0.8		2	

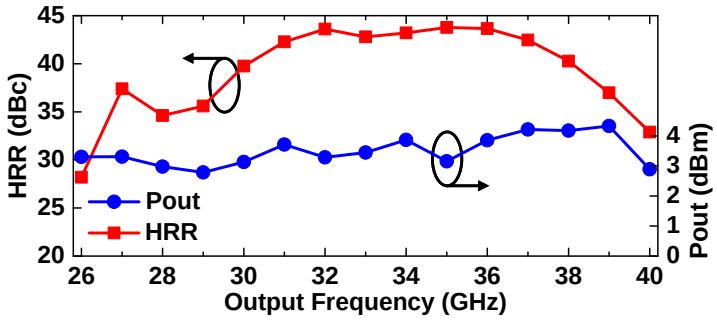


Figure 4.33: Summarized P_{out} and HRR vs Freq. at high-band operation.

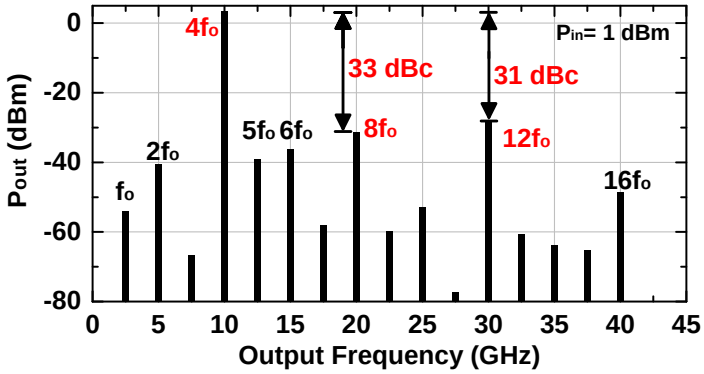


Figure 4.34: Measured harmonics at 10 GHz.

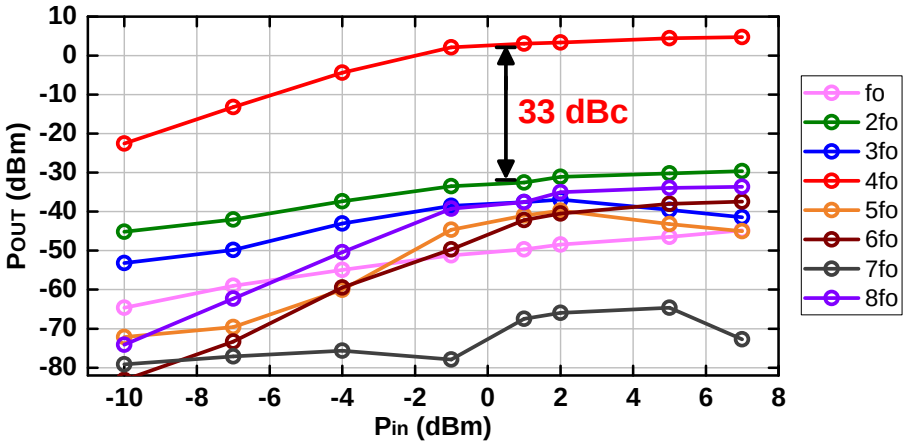


Figure 4.35: Measured P_{out} vs P_{in} for $4f_o$= 20 GHz output.

(right), respectively, which has 5−8 dB improvement compared to HRR12 with V_C OFF state, as expected in simulation.

Overall Measurements

Based on the measurements in previous sub-sections, P_{out} and worstcase HRR with optimum gain setting and switch operations is measured, and summarized in Fig. 4.31−4.33. In overall, the output power of +3 dBm with worstcase of >30 dBc is measured for each bands. For overlapping frequency, such as 16 GHz (low- and mid-band) or 26 GHz (mid- and high-band), the point which has better performance is chosen.

Fig. 4.34 presents the measured output spectrum of 10 GHz (low-band). The measured

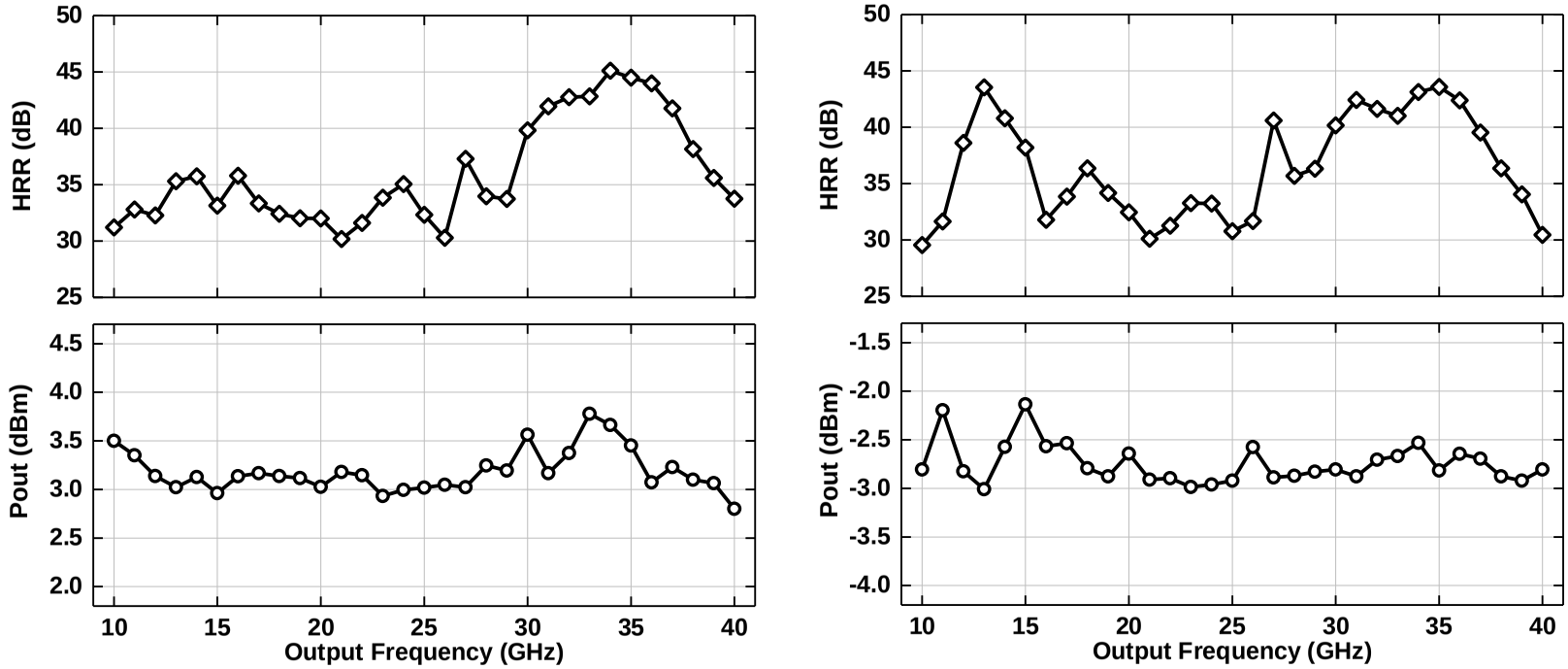


Figure 4.36: Worstcase HRR vs Freq. for +3 dBm and -3 dBm P_{out} at $10-40$ GHz.

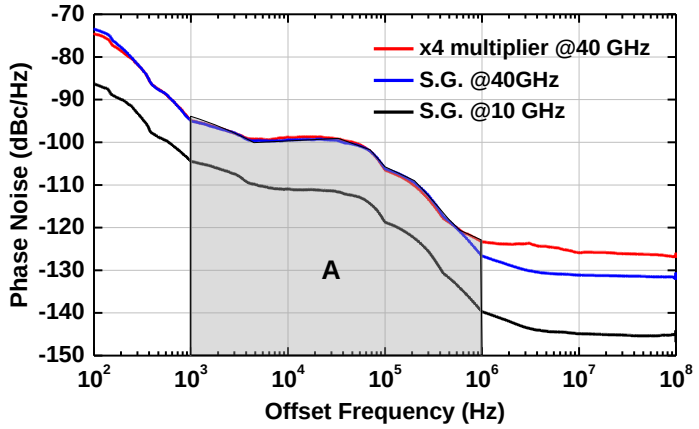
output power is >3 dBm, with harmonic contents all below <-30 dBc. The $5f_o$, $6f_o$ contents are well suppressed by switchable bandpass filter and $12f_o$ is further rejected by switch operation in PA (V_C). The worstcase HRR is 31 dBc at 10 GHz output with the input power of 1 dBm.

Fig. 4.35 shows the measured P_{out} vs P_{in} for each harmonics for output frequency of 20 GHz. The output power of >3 dBm with 33 dBc worstcase HRR is measured. The largest harmonic in this case is $2f_o$, and adjacent harmonics ($3f_o$, $5f_o$, and $6f_o$) are sufficiently suppressed by bandpass filter.

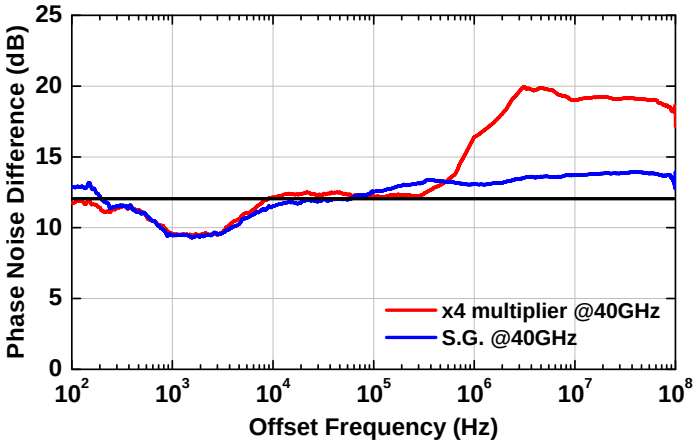
Fig. 4.36 presents overall $10-40$ GHz measurement for +3 dBm output (left) and -3 dBm output power (right). The worstcase HRR is maintained >30 dBc for both cases, implying that the signal purity of the output signal remains unchanged with the output power level from -3 to +3 dBm. The input return loss including bump inductance and T-line on PCB is <-10 dB for all three band operations. Table 5.1 summarizes recently reported several frequency multipliers operated up to V-band.

4.6.3 Phase Noise Measurement

The phase noise measurement is performed with signal generator and spectrum analyzer. At first, the phase noise of the signal generator is measured by directly connecting it to the spectrum analyzer, and its phase noise at 10 and 40 GHz input are shown in Fig. 4.37a. If no additional noise is added from the device, the theoretical phase noise difference would be $\sim$12 dB (20·logN), where N=4 is the multiplication factor. Fig. 4.37b shows the phase noise difference compared to phase noise at 10 GHz, and the measured PN difference agrees well with with the theoretical value (12 dB) up to 100 MHz offset frequency (blue line). Then, a 10-GHz input signal passes through the quadrupler chip and the measured phase noise and phase noise difference at 40 GHz are shown in Fig. 4.37 (red line).The phase noise difference agrees very well with the theoretical value up to $\sim$ 500 KHz offset, and starts deviating above >1 MHz offset. This is due to additional phase noise being added from the quadrupler chip. The summarized phase noise at



(a)



(b)

Figure 4.37: (a) Measured phase noise at 40 GHz, and (b) phase noise difference compared to phase noise at 10 GHz.

Table 4.3: Comparison Table of Reported Frequency Multipliers up to V-band

Ref.	[62]	[63]	[64]	[67]	[74]	[75]	[76]	[77]	**This work**
Tech.	SiGe 0.25-µm	HEMT 2-µm/0.5-µm	SiGe 0.13-µm	SiGe 0.13-µm	CMOS 65-nm	SiGe 0.1-µm	SiGe 0.13-µm	SiGe 0.13-µm	**SiGe 0.12-µm**
Freq. (GHz)	52−75	23−29.6	14−30	56−71	46−52	45−57	48−58	50−75	**10−40**
FBW (%)	36	25	73	23	12	24	19	40	**120**
Topology	×4	×4	×2	×8	×8	×4	×3	×4	×**4**
P_{in} (dBm)	8	4−5	0	2−6	-24	-8.8−-2.9	-2.5	-10	**1**
P_{out} (dBm)	-10	5−8.2	0−4	13.5 [a]	-6−-1.8	7.4−8.2	9.5	0	**3**
P_{DC} (mW)	11.7	54	12.7	410	55	150	220	92	**139−163**[b]
HRR (dBc)	∼10	10−25	>35	>40	>37	>22	>28	29	> **30**
Chip size (mm^2)	0.42	2	0.24	1.35	0.92	1.4	0.94	0.31	**8**[c]
Package	On-Wafer	On-Wafer	On-Wafer	On-Wafer	On-Wafer	On-Wafer	On-Wafer	On-Wafer	**Flip-chip**

[a] Multiplier+3-stage amp

[b] P_{DC} for one-channel operation.

[c] 4-channel flip-chip area.

Table 4.4: Measured phase noise at 10−40 GHz

	Phase Noise (dBc/Hz)			
Freq (GHz)	100 Hz	10 KHz	1 MHz	100 MHz
10	-84.7	-99	-132.4	-137.6
20	-80	-102	-130	-135
30	-77.6	-105	-128	-133.6
40	-74	-111	-123	-126

10−40 GHz output is shown in Table 4.4.

Fig. 4.38 presents the graphical comparison with state-of-the-art on-wafer VCO+PLL works to the commercial VCO+PLL with 10−40 GHz multiplier and external signal generator with 10−40 GHz multiplier [52, 56, 57, 78–85]. Based on the measured phase noise of -123 dBc/Hz at 40 GHz (red dashed line) using external signal generator, and with the remarkable improvement of commercial QFN based integrated VCO+PLL chipset, the phase noise of ∼-117 dBc/Hz is achieved at 40 GHz (blue dashed line), which is ∼10 dB better phase noise performance than state-of-the-art on-wafer VCO+PLL [86]. This implies that well-done integration of commercial chipset together with 10−40 GHz multiplier on PCB can replace an external high-volume, high-cost frequency source with a very high spectral purity. The integrated RMS jitter, is defined as

$$\text{RMS Jitter} = \frac{\sqrt{2 \cdot 10^{A/10}}}{2\pi f_o} \tag{4.9}$$

where A is the sum of integrated phase noise power in dBc (See Fig. 4.37a) over given bandwidth and f_o is the LO frequency. The RMS jitter is from 51−81 fs with 200 Hz to 500 MHz integration. Table 4.5 summraizes RMS jitter with different integration bandwidth.

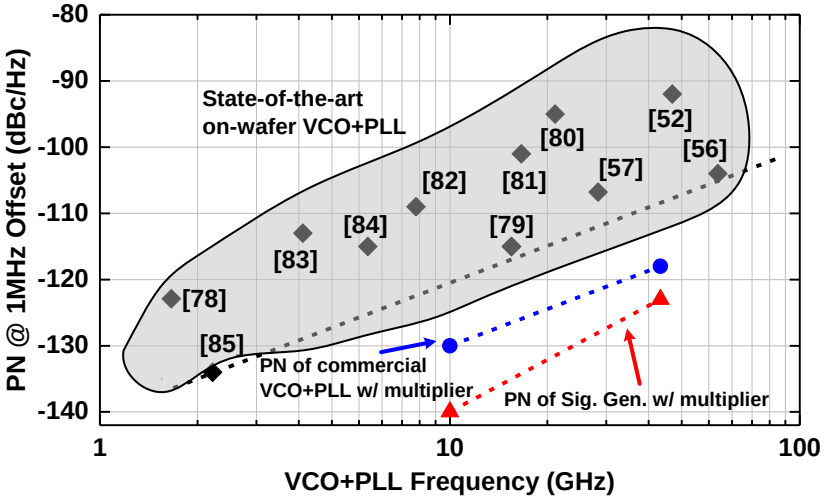


Figure 4.38: Phase noise performance comparison with on-wafer state-of-the-art VCO+PLL, 10−40 GHz quadrupler with commercial VCO+PLL chipset, and 10−40 GHz quadrupler with external signal generator.

Table 4.5: Calculated RMS jitter based on measured phase noise

RMS Jitter (fs)	20Hz-100MHz	200Hz-500MHz	20Hz-1GHz
10 GHz	64.3	87.9	109.7
20 GHz	43.7	59.4	74.5
30 GHz	40.1	50.9	61.9
40 GHz	57.4	80.9	103

4.7 Conclusion

This work presented a 4-channel 10−40 GHz frequency quadrupler chip with >30 dBc worstcase HRR and +3 dBm output power with flip-chip packaging. With the help of switch operation in the bandpass filters and PA, largest potential harmonic contents are greatly reduced, maintaining worst HRR >30 dBc over the entire bandwidth. Similar HRR performance is measured with -3 dBm, implying that the output power can be adjusted while maintaining HRR. The chip is flipped and placed on low-cost PCB with connecterized input and outputs. The frequency quadrupler design of having such a wideband (>100 % BW), high-purity, enough output power can be integrated with a high-performance signal source, and is consequently

combined with various system-level applications, such as high-resolution imaging radar, high-data rate communication link, and phased-arrays for 5G mobile system.

4.8 Acknowledgment

This work was supported by Analog Device Inc. (ADI) and Global Foundries.

Chapter 4, in part, is a reprint of the material as it appears in: H. Chung, Q. Ma, and G. M. Rebeiz, "A 10-40 GHz frequency quadrupler source with switchable bandpass filter and >30 dB harmonic rejection," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June, HI, 2017, pp.49-52. The dissertation author was the primary investigator and author of this material.

Chapter 4 is also, in full, has been submitted for publication of the material as it may appear in: H. Chung, Q. Ma, and G. M. Rebeiz, "A 10-40 GHz 4-channel frequency quadrupler with switchable bandpass filter and >30 dBc harmonic rejection with flip-chip packaging", *IEEE Journal of Solid-State Circuits)*, in preparation. The dissertation author was the primary investigator and author of this material.

Chapter 5

A Milliwatt-Level 70−110 GHz Frequency Quadrupler with 30 dBc Harmonic Rejection

5.1 Introduction

Millimiter-wave wave applications at 60 GHz and above has been actively investigated in the past few years and significant progress has been accomplished as demands of high data rate wireless communication, high-resolution radar and imaging system are steadily increased [28, 39, 40, 66, 87–90]. Furthermore, recent transition of 4G to 5G mobile communication not only moves attentions to 28- or 39-GHz range, but also attract next generation of 5G, potential frequency range of 71−76 or 81−86 GHz region [91]. Together with previous studies of automotive radar at 77 GHz [39, 40] and imaging system [92], W-band region can be expected as an excellent solution to fulfill various applications as the technology of silicon germanium (SiGe) and CMOS silicon-on-insulator (SOI) transistor enables to have f_{T} and f_{MAX} of 300−400 GHz. (2−3 times higher than W-band region).

The system performance of these systems at W-band is dependent on many different factors, but one of the most important building blocks to determine state-of-the-art is local oscillator (LO). There are several important figure of merits in local oscillator: tuning range (bandwidth), capability of frequency locking, output power, and phase noise. One approach is to design LO is to integrate voltage-controlled oscillator (VCO) on-chip by using conventional LC tank. However, design of VCO at W-band is challenging due to comparable tuning capacitors as transistor capacitance (C_{gs}, C_{gd}, etc), which decreases the tuning range ($< 10\%$) also degrades phase noise [55]. Furthermore, free-running VCOs are required to use with closed phase-locked loop (PLL), and it is very challenging due to the design limitation of frequency divider at these frequencies [53, 54] and huge power and area consumption [93]. As an alternative, injection locking with frequency multiplier can be chosen [94], having advantage of better power and area efficiency and better phase noise. However, the output bandwidth is still limited ($\sim$10 %), and the output power is dramatically dropped when locked frequency is deviated from the free-running oscillation frequency of the injected-locked multiplier.

Due to present design limitations, this work presents the use of $\times$4 frequency multiplication by cascading two frequency doublers together with inter-stage bandpass filter to suppress undesired harmonic generated by each doublers, shown in Fig. 5.1. The advantages of using frequency multiplier is to use of input signal at lower frequency ($17.5-27.5$ GHz) where high power signal generation is easier and has less distribution loss as well as better phase noise and relaxed requirement of implementing frequency synthesizer. Two amplification stages are also included in order to compensate the loss of passive components and deliver enough power to the second doubler and the output ($>$0 dBm). The frequency bandwidth of all building blocks is designed to have $70-110$ GHz (44 % BW) with two-channel output power of -1.5 to +2.9 dBm with harmonic rejection ratio (HRR) $>$29 dBc to drive two mixers for any W-band applications. For improved isolation between channels, separate VCC and GND planes are used for LO generation region and final amplification stage which is generally included in the receiver

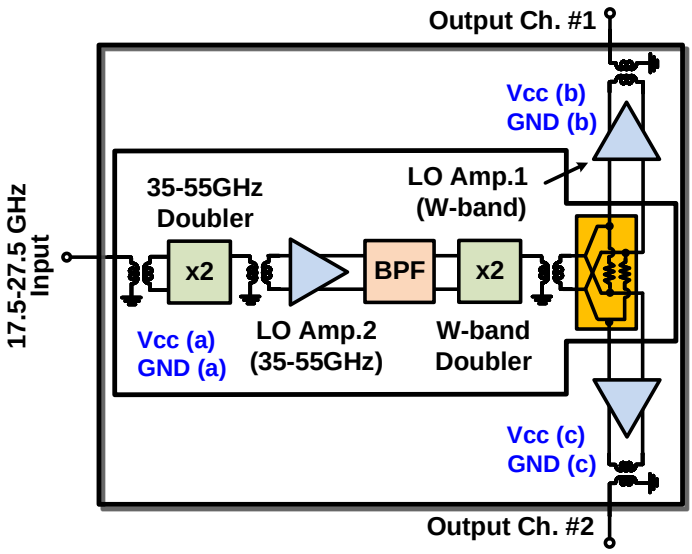


Figure 5.1: Block diagram of 2-channel 70−110 GHz frequency quadrupler.

design. This project consists of following sections. In section 5.2, brief information of technology used for this design is introduced. Section 5.3 describes circuit designs of frequency doublers, wideband bandpass filter and amplifiers. Section 5.4 shows the experimental results and Section 5.5 concludes this work and compares it with state-of-the-art frequency multipliers at different frequency ranges [62, 72, 75, 95–105].

5.2 Technology

The 70−110 GHz frequency quadupler is designed using GF8HP 0.12-µm SiGe BiCMOS process with seven metal layers including two thick metal layers, AM(= 4 µm) and LY (=1.25 µm), for low loss RF routing (Fig. 5.2). The f_T and f_{MAX} of the HBT transistor is 200 GHz. The 100-Ω differential coplanar waveguide (CPW) transmission line (9−6−10−6−9 µm) is implemented with AM and MQ ground plane, and a simulated loss of 1.05 dB/mm at 80 GHz. The simulated Q of the transmission line is 12 at 80 GHz. [39, 88]

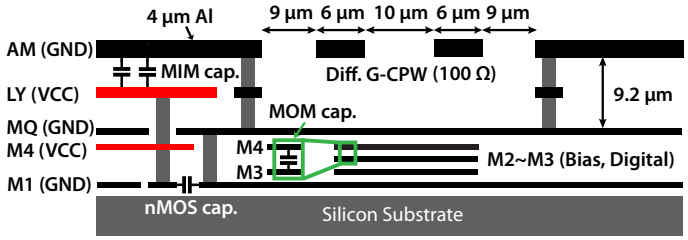
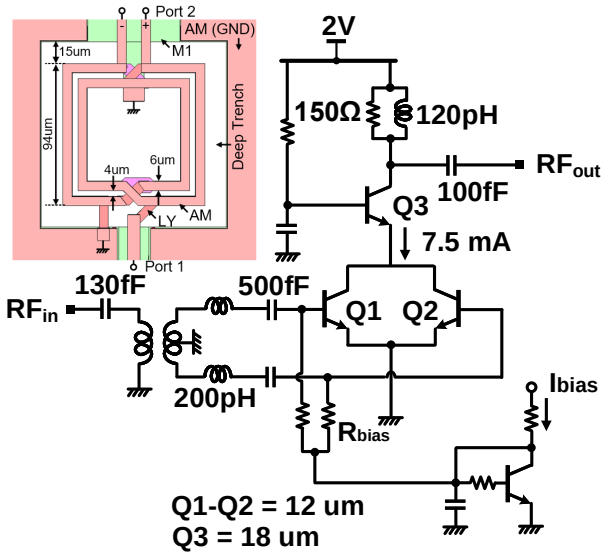


Figure 5.2: Differential GCPW stackup of GF8HP technology.

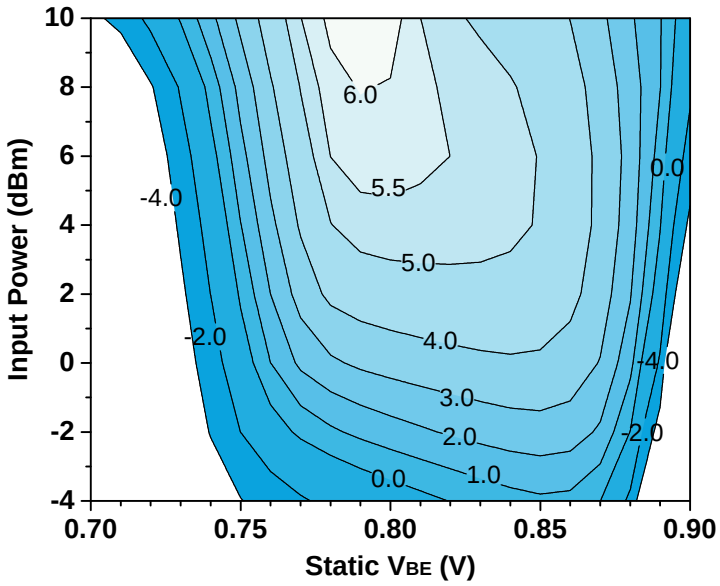
5.3 Circuits Designs

5.3.1 Doublers

The schematic of 35−55 GHz frequency doubler is shown Fig. 5.3a. A 17.5−27.5 GHz single-ended signal is converted into differential using a wideband 50 Ω single-ended to 100 Ω differential balun. A symmetric layout is required to minimize amplitude and phase imbalance for lower odd harmonic generation causing multiple undesired spurs at the output. The distance to the ground plane is 15-µm on each side with the width and spacing of 4-µm, 6-µm, respectively, and double-turned structure is used to minimize the area consumption. The simulated loss of the balun is 1.5 dB, and the amplitude and phase imbalance is < 0.5 dB, $< 2^\circ$ at 22.5 GHz. Additional series capacitance and inductances are used together with input balun for wideband input matching and the middle point of the secondary inductor is tapped to the ground for common mode rejection. Differential pair of bipolar transistors with connected collectors provide wideband ac short for fundamental and odd harmonics as well as in-phase 2nd harmonic and other even harmonics [65]. For differential pair, 12-µm transistor is used for large current handling for higher input power. For cascode transistor, larger transistor is used (18-µm) is used in order to keep current density of 1∼1.5 mA/µm for optimum f_T. All transistors are modeled using Sonnet EM Suite including the parasitics of interconnections up to AM layer [68]. The collectors of differential pairs are tied and connected to another common-base stage to increase output power as well as gain-bandwidth, and single-ended output is converted using output balun (not shown).



(a)

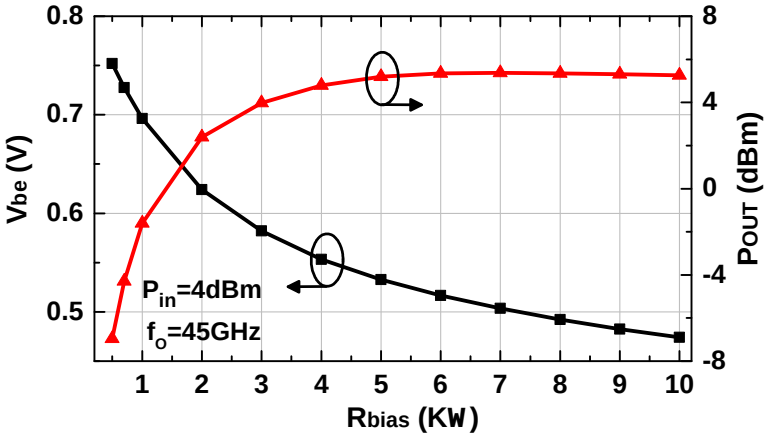


(b)

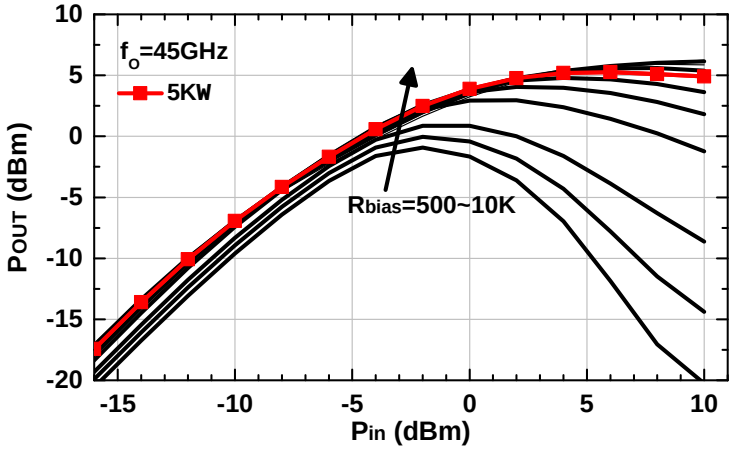
Figure 5.3: (a) 35−55 GHz frequency doubler schematic, (b) output power contour vs Input power and static V_{BE} at 45 GHz output.

In addition to the transistors and passive circuits, all interconnections between at the input and output and between transistors are also EM-modeled.

The desired $2f_o$ contents are determined by driving input power and base voltage, and output power contour with different input power and biasing condition is shown in Fig. 5.3b. By



(a)



(b)

Figure 5.4: (a) V_{BE} and P_{out} vs R_{Bias} (b) P_{out} vs P_{in} with different R_{Bias}.

applying static $V_{\mathrm{BE}} \sim 0.8$ V, output power of 1 dBm or higher is achieved with less than <-2 dBm input power. Also, output power of > 5 dBm is simulated with same bias condition with 3 dBm input power. Static V_{BE} of 0.8 V is above threshold voltage of the bipolar transistor (~ 0.7 V), but is decreased when input power is increased and the transistor is operated in class-B or class-C mode ($V_{\mathrm{BE}} = 0.7$ or lower) at high input power for larger $2f_o$. The doubler bias current at 0 dBm input power is 18.5 mA [65].

Furthermore, the resistance value of R_{Bias} is critical to the $2f_o$ output power and its effect is presented in Fig. 5.4. For high $2f_o$ generation at the output, V_{BE} of 0.7 or lower is required

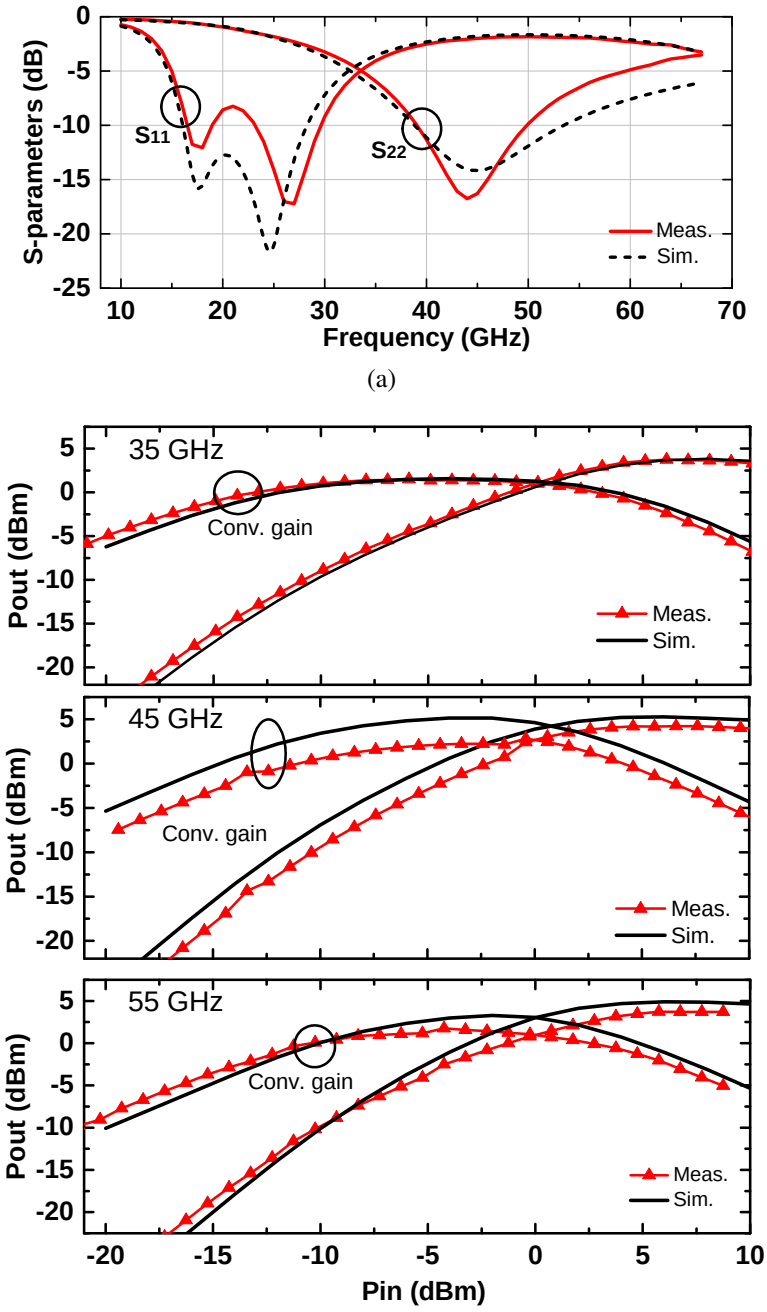


Figure 5.5: (a) Measured S-parameters, and (b) P_{out} and conversion gain of the 1st-stage doubler.

when the input signal is large, however, lower R_{Bias} value, such as 500 Ω or 1 KΩ, prevents V_{BE} from dropping enough for class B or C operation, resulting in lower output power (Fig. 5.4a). By increasing $R_{Bias} \sim 5$ KΩ, V_{BE} is 0.55 V when input power of 4 dBm and saturated output power

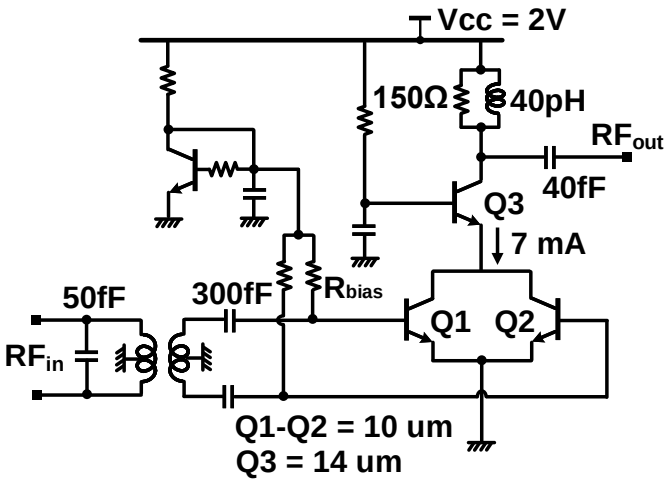
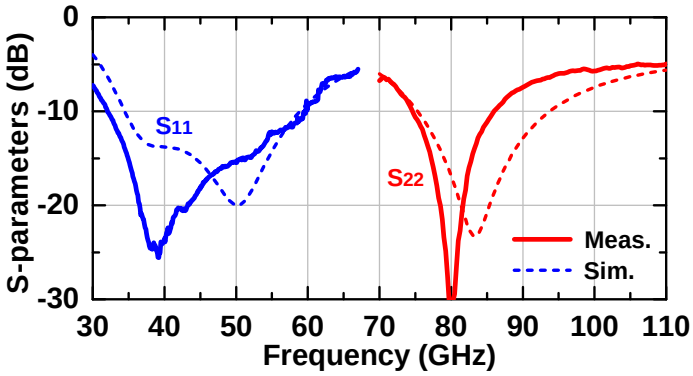


Figure 5.6: Schematic of 70−110 GHz frequency doubler.

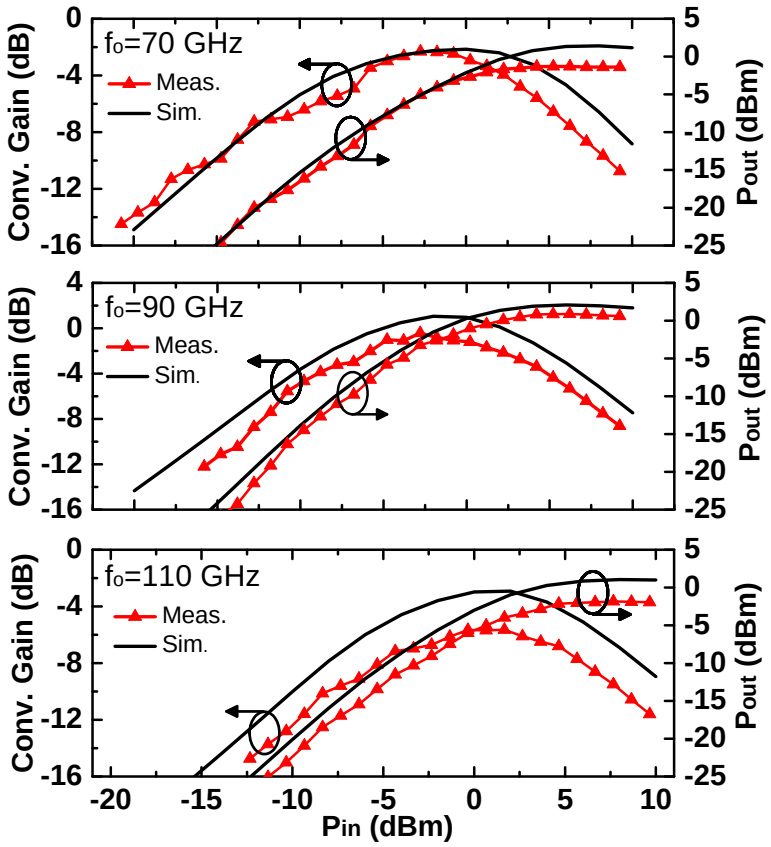
of 5.3 dBm. Fig. 5.4b presents output power versus input power with different R_{Bias}. As R_{Bias} is decreased, output power is also dropped when input power is > 0 dBm. At some point, the effect of increasing R_{Bias} does not affect saturated output power, and 5 KΩ is chosen for bias resistance.

Fig. 5.5a shows simulated and measured S-parameters of 35−55 GHz frequency doubler. The measured S_{11} is $<$ -8 dB at 17−32 GHz, and S_{22} is $<$ -10 at 38−52 GHz, having great agreement with the simulation. The large signal measurement is also done using spectrum analyzer at 35, 45, and 55 GHz and the measured output power and conversion gain are shown in Fig. 5.5b. The measured peak output power is 3−4.2 dBm at 35−55 GHz, with the peak conversion gain of 1.6−5.2 dB.

Another frequency doubler is implemented in a similar way to multiply 35−55 GHz by two and generate the output frequency of 70−110 GHz, and its schematic is presented in Fig. 5.6. Differential 35−55 GHz signal is applied and 1:1 transformer is implemented for wideband input matching. Similar base bias analysis for 70−110 GHz is done with different input drive power and it is also best for the largest output power with static V_{BE} of 0.8 V. Increasing input power decreases V_{BE} below threshold voltage to maximize $4f_o$ at the output with appropriate bias resistance value (5 KΩ). Similar effect is shown as the bias resistance below 1 KΩ for 70−110 GHz doubler, and output power of 2 dBm is obtained with $\sim$ 5 KΩ R_{Bias}. The bias current of



(a)



(b)

Figure 5.7: (a) Measured S-parameters, and (b) P_{out} and conversion gain of the 2nd-stage doubler.

W-band doubler at 0 dBm input power is 14 mA.

Fig. 5.7a shows S-parameters of 70−110 GHz frequency doubler, and measured S_{11} is $<$ -10 dB at 33−60 GHz and S_{22} is $<$ -7 dB at 75−86 GHz. The S-parameters of 70−110 GHz

doubler is measured using PNA up to 67 GHz standalone and with VDI WR-10 extenders for frequency extension for S_{22}. The output power and conversion gain at 70, 90 and 110 GHz output is shown Fig. 5.7b. Note that the test circuit of $70-110$ GHz frequency doubler has single-ended input with input balun instead of differential input with transformer (Fig. 5.7a, not shown for brevity). The measured peak output power is -1.9$-$0.9 dBm at $70-110$ GHz with the peak conversion gain of -5.7$\sim$-0.5 dB, which are $1-3$ dB lower than simulated. However, lower peak output power can be compensated by following stage W-band amplifier.

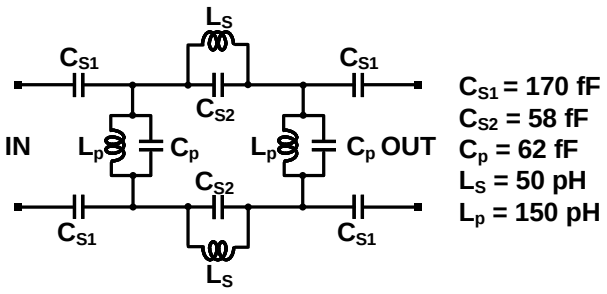
5.3.2 Bandpass Filters

The schematic of differential 3rd order 2-pole/1 zero bandpass filter is shown Fig. 5.8a. Wideband operation inevitably creates undesired adjacent harmonics (f_o, $3f_o$, etc) which is located close to the passband or even in-band of the filter. Especially, unfiltered harmonics(i.e., $3f_o$ when f_o=18 GHz) will generate multiple harmonics by inter-mixing with strong $2f_o$, creating $5f_o$ or self-mixing also generating $6f_o$ at the output. Therefore, sharp rejection is required to suppress adjacent harmonics sufficiently especially at higher frequency. The number of stage is carefully investigated to achieve wideband passband and sharp response with minimal area consumption.

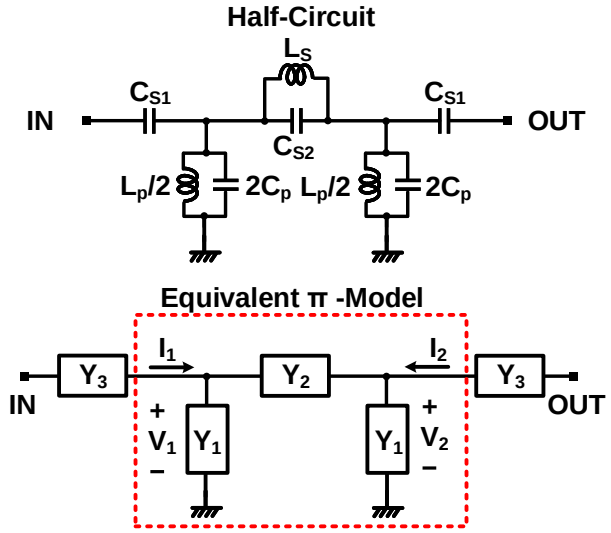
The filter response is investigated by using half-circuit analysis (Fig. 5.8b). The 3-stage shunt LC pairs are first analyzed by using equivalent π-model shown Fig. 5.8b, where Y_1=$jw2C_p$+2/jwL_p and Y_2=jwC_{s2}+2/jwL_s, respectively [32]. Due to the symmetrical structure, its Y-parameters can be simplified as

$$I_1 = Y_1V_1 + Y_2(V_1 - V_2) = (Y_1 + Y_2)V_1 - Y_2V_2 \tag{5.1}$$

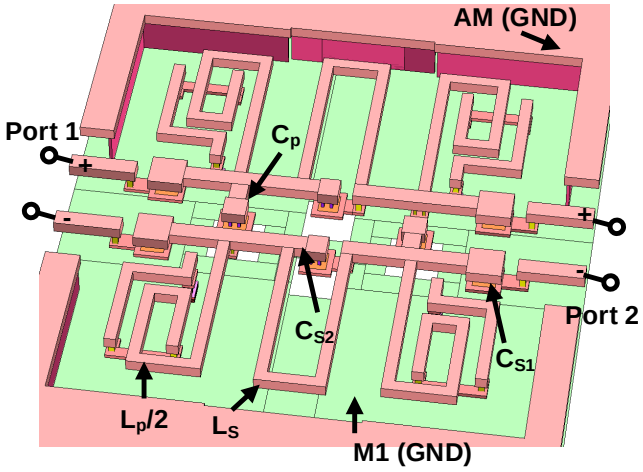
$$I_2 = Y_2(V_2 - V_1) + Y_1V_2 = -Y_2V_1 + (Y_1 + Y_2)V_2 \tag{5.2}$$



(a)



(b)



(c)

Figure 5.8: (a) Schematic of 3-stage elliptic bandpass filter, (b) half-circuit and equivalent pi-model and (c) sonnet layout.

$$Y_\pi = \begin{bmatrix} Y_1 + Y_2 & -Y_2 \\ -Y_2 & Y_1 + Y_2 \end{bmatrix} \tag{5.3}$$

The locations of the zero and pole can be found where $Y_{\pi,21}$=0 and $S_{\pi,11}$=0, as shown

$$Y_2 = 0 \tag{5.4}$$

$$Y_O^2 - Y_1^2 - 2Y_1Y_2 = 0 \tag{5.5}$$

where Y_O is the normalized characteristic admittance ($1/50\ \Omega$). According to the design parameters shown in Fig. 5.8a, one zero can be easily calculated, which is the resonant frequency of Y_2, and two poles are also calculated by using the equations shown

$$j\omega_z C_{s2} + \frac{1}{j\omega_z L_s} = 0 \tag{5.6}$$

$$\omega_p^4 \frac{C_p^2 L_p^2 L_s (1 + C_{s2})}{L_s + L_p} + \omega_p^2 \frac{L_p^2 L_s}{L_s + L_p} \left(\frac{Y_O^2}{4} - \frac{2C_p}{L_p} - \frac{C_p}{L_s} - \frac{C_{s2}}{L_p} \right) + 1 = 0 \tag{5.7}$$

where ω_z and ω_p refer to zero and pole of the bandpass filter. Note that the sharp rejection at the stopband only happens the side where the transmission zero presents, which is desirable to reject high-order harmonics. However, lower rejection at the lower frequency can also cause larger fundamental harmonic after bandpass filter resulting in higher non-desirable harmonics at the output (i.e, larger $2f_o$ at the output due to large f_o being multiplied by 2). One approach to solve it is to increase the number of the stage by simply adding additional shunt L and C in series, to create another transmission zero at lower passband frequency. This approach provides sharp rejection as the other side, however , is not chosen due to additional area consumption and

higher insertion loss caused by adding another shunt lumped components. Instead, by adding the series capacitors on each sides, better stopband response can be obtained since additional capacitors enable two poles being split further each other and provide better rejection. The effect of the adding series capacitors is presented in Fig. 5.9. Compared to the filter S_{21} without the series capacitance C_{s1}, the filter S_{21} with C_{s1} has $\sim$ 5 dB higher rejection at 17.5 GHz, which is the low-edge of the input frequency as well as wider filter passband with the help of pole splitting. Its series reactance value is also used for matching of the bandpass filter.

The transfer function of entire bandpass filter including series capacitance C_{s1} can be also derived by converting Y-parameters of capacitor and π-model filter into ABCD parameter and use cascade multiplication, shown as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{Total}} = \begin{bmatrix} 1 & 1/Y_3 \\ 0 & 1 \end{bmatrix}_{Y_3} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Y_\pi} \begin{bmatrix} 1 & 1/Y_3 \\ 0 & 1 \end{bmatrix}_{Y_3} \tag{5.8}$$

Fig. 5.8c shows the complete EM structure of the differential 3rd order 2-pole/1-zero bandpass filter. The effect of all inductors, metal-insulator-metal (MIM) capacitors and interconnections are taken into account in a single EM file to model entire structure accurately. M1 ground metal is placed under the inductor to avoid design uncertainty at the expense of lower Q of inductor [69].

The measured S-parameters of bandpass filter is shown in Fig. 5.10. Note that input and output balun is implemented together with the bandpass filter in the test chip, and simulated filter response with the baluns are also plotted. Without baluns, simulated insertion loss is $2.1-3.6$ dB with S_{11} of $<$ -10 dB at $35-55$ GHz (black solid line). Simulated S-parameters with baluns are also plotted and its insertion loss is $4.5-7.7$ dB at $35-55$ GHz (red dashed line). The measured

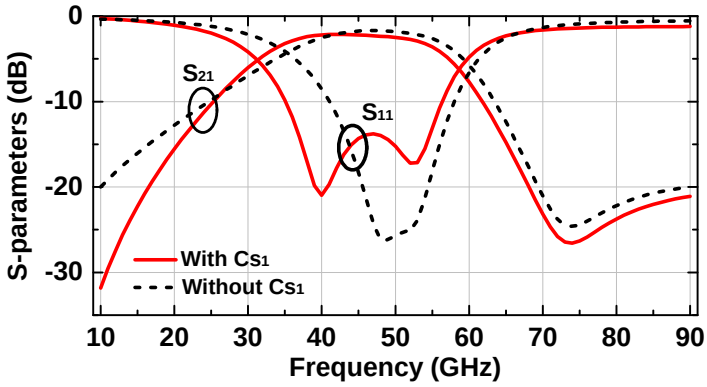


Figure 5.9: Simulated bandpass filter return loss and insertion loss with the effect of series capacitors C_{s1}.

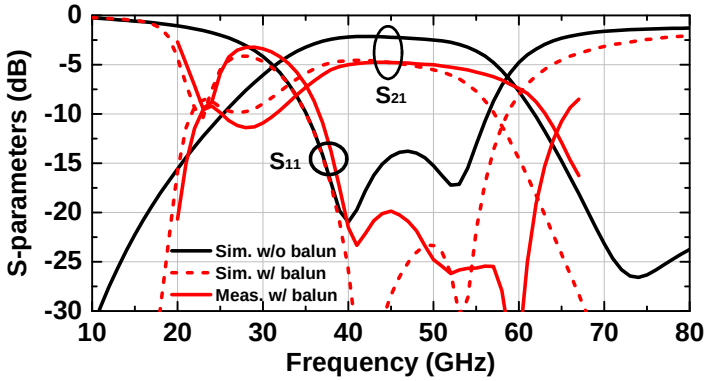
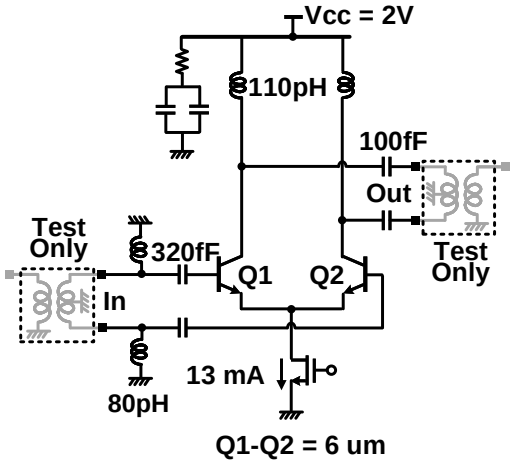


Figure 5.10: Simulated S-parameters of bandpass filter with and without balun and measured S-parameter with balun.

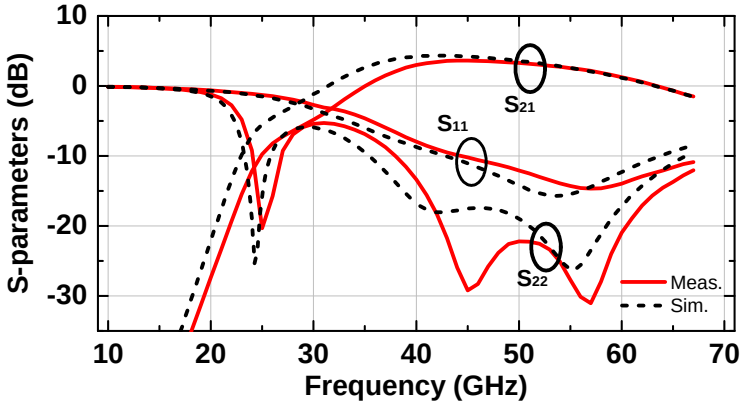
insertion loss has only 0.2−1.5 dB difference, resulting in 4.7−7.3 dB at 35−55 GHz with S_{11} < -10 dB at 35−55 GHz. (red solid line)

5.3.3 Amplifiers

The one-stage common-emitter (CE) 35−55 GHz amplifier is implemented right after single-ended doubler output followed by single-ended to differential balun to compensate the passive loss of the bandpass filter and balun (Fig. 5.11a). The simulated small signal differential gain is 5−6.5 dB. In order to test the circuit performance, it is connected with input and output balun and measured using single-ended configuration, and the single-ended small signal gain is 0−3.6 dB at 35−55 GHz with S_{11} < -7 dB and S_{22} < -10 dB at > 38 GHz, and its measurement



(a)

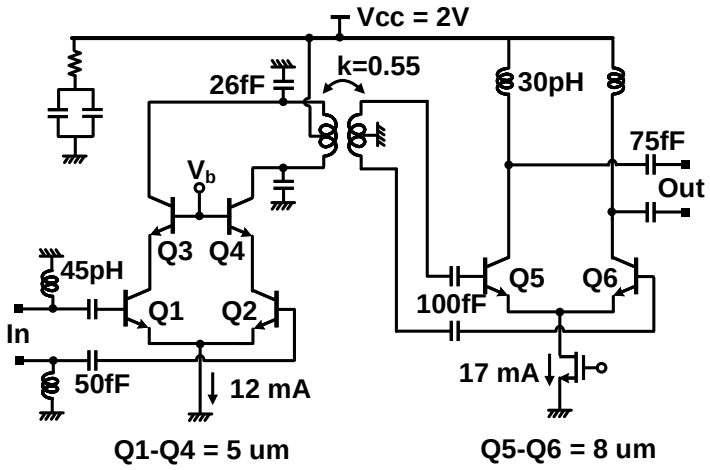


(b)

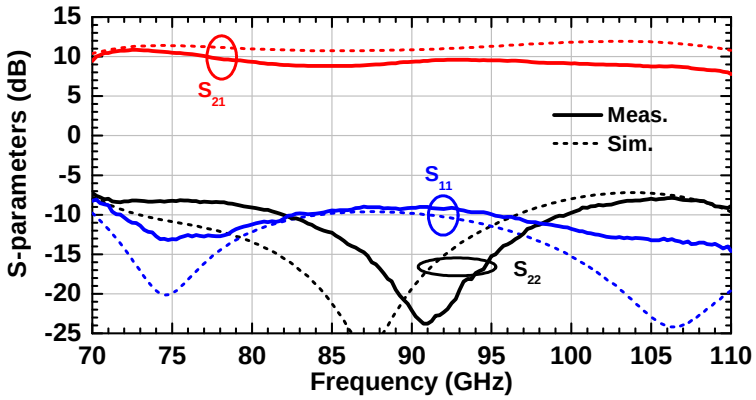
Figure 5.11: (a) Schematic, (b) S-parameters, of 35−55 GHz amplifier.

result agrees well with the simulation (Fig. 5.11b). The measured OP_{1dB} and P_{sat} is -3.5 to 1.3 dBm, and -1 to 3.9 dBm at 35−55 GHz, respectively.

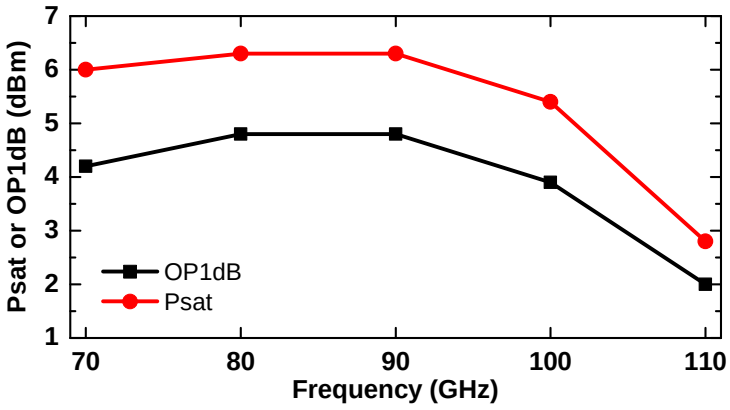
A wideband two-stage W-band amplifier is also implemented right before the output to boost output power. (Fig. 5.12a). In order to achieve wideband gain response, double-tuned transformer is used between two stages. A vertically coupled primary and secondary inductors (L_p=100 pH, L_s=100 pH) are implemented with top two metals (AM, and LY) with magnetic coupling factor of 0.5−0.6, providing broadband gain response with minimum ripples [106]. The simulated S_{21} has very flat gain response of 10.4−12 dB with <1 dB gain ripple at 70−110 GHz. For S-parameter measurement at W-band, two-port standard short-open-load-thru (SOLT) and



(a)



(b)



(c)

Figure 5.12: (a) Schematic, (b) S-parameters, and (c) OP_{1dB} and P_{sat} of W-band amplifier. (Input and output balun for W-band amplifier are used for test-circuit measurement, but are not shown for brevity)

thru-reflection-line (TRL) calibration are both done to remove the effect of probes as well as the input and output pads. The reference plane of the measurement is input and output of the chip. W-band input and output baluns are connected for test circuit measurement purpose (not shown for brevity). The measured small-signal gain of the W-band amplifier shows a flat gain response at 70−110 GHz with a 8−10.9 dB with $\sim$ 1 dB gain ripple. Measured S_{11} and S_{22} agree well with the simulation with the level of $<$ -7 dB (Fig. 5.12b). Measured $OP_{1\text{dB}}$ and P_{sat} are also presented in Fig. 5.12c with $OP_{1\text{dB}}$ of 2−4.8 dBm, and P_{sat} 2.8−6.3 dBm, respectively.

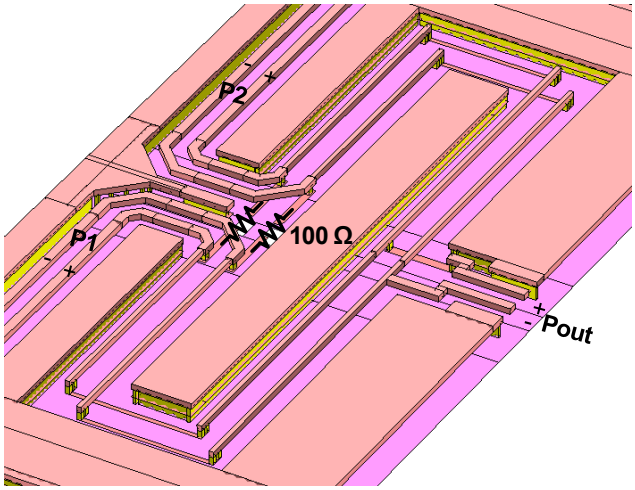
5.3.4 Wilkinson Divider and Bias Circuit Design

The differential Wilkinson power divider is implemented after W-band frequency doubler to split output power into two W-band amplifiers Fig. 5.13a). The simulated loss of Wilkinson divider is 1.3 dB at 90 GHz with good input and output matching as well as isolation (Fig. 5.13b).

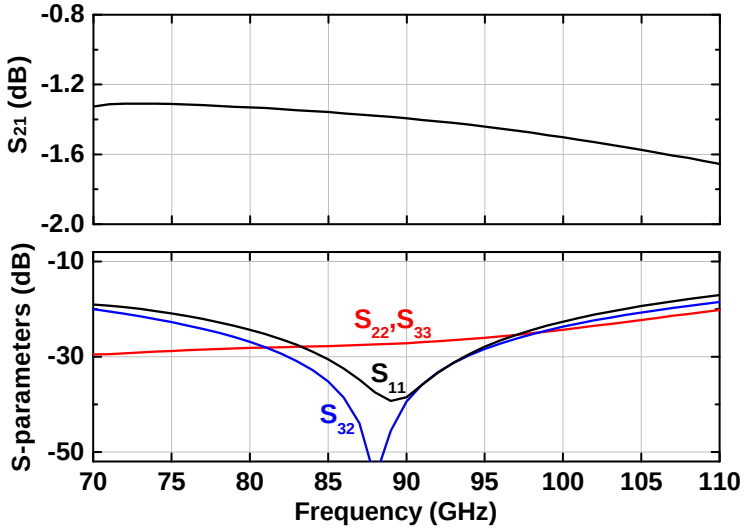
The chip is biased either using external voltage source or internal proportional to absolute temperature (PTAT) circuits in order to maintain constant gain and output power versus temperature up to 80^{o}C. The transistors are biased at 0.8−0.85 mA/μm and the PTAT increases the current density to 1.1−1.2 mA/μm at 80^{o}C. Fig. 5.14 presents the simulated output power versus temperature at the output of the quadrupler chip at 90 GHz with and without using PTAT bias.

5.4 Measurements

The chip microphotograph of the 70−110 GHz frequency quadrupler is shown in Fig. 5.15. The static DC current is 97 mA for a 2 V supply, but it is increased to 125 mA if the input power increases to 5 dBm. Note that this quadrupler can generate 2-channel output at the same time and 85 mA is consumed for a single-channel operation. The overall chip size is 1.9 mm^2 (1.58×1.2 mm^2). The chip is not designed to be fitted into a rectangle, and one of the test circuits (35-55 GHz doubler) is implemented inside the quadrupler chip. Due to the uneven distribution



(a)



(b)

Figure 5.13: (a) Layout and (b) S-parameters of differential Wilkinson divider.

of the DC pads around the chip, the chip is placed on the printed circuit board (PCB) and all bias voltages and digital controls are applied through bond-wires. One input and two-outputs are single-ended and coaxial probe and WR-10 probe are used to for input and output.

Fig. 5.16 shows the power measurement setup for 70−110 GHz quadrupler circuit. The input signal of 17.5−27.5 GHz is generated using a Agilent 8257D signal generator and input power is monitored by using power sensor and 10 dB coupler. The output signal of 70−110

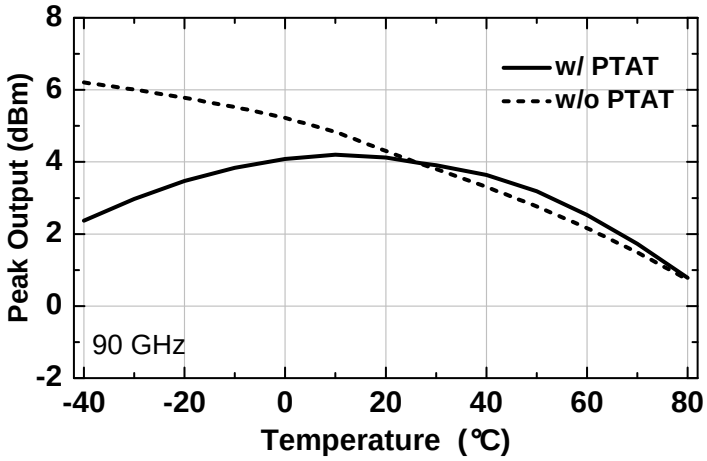


Figure 5.14: Simulated output power at the quadrupler chip with and without using PTAT bias at 90 GHz.

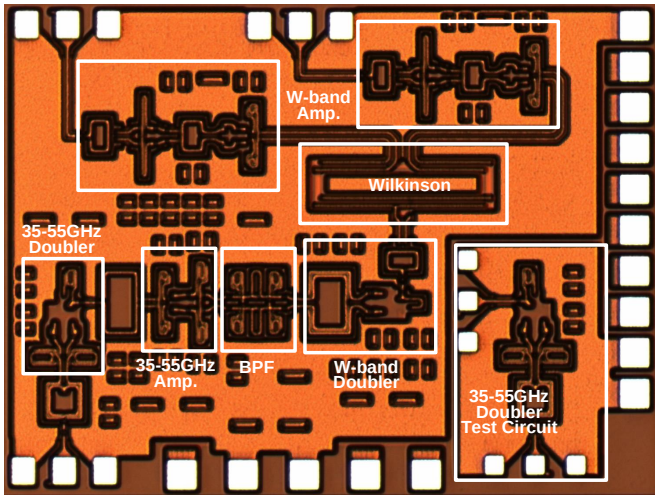


Figure 5.15: Chip microphotograph of W-band frequency quadrupler (1.58×1.2 mm^2).

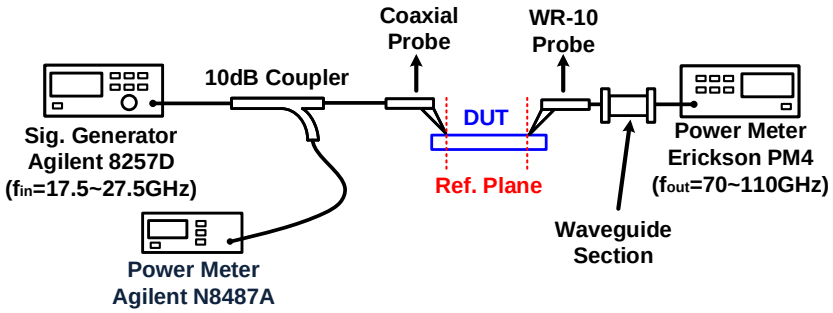
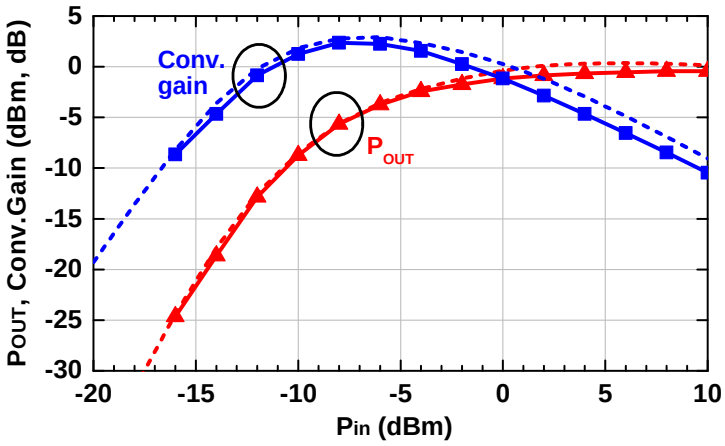
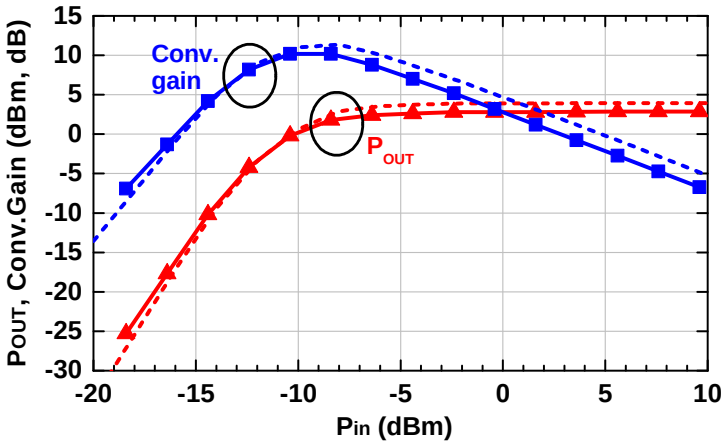


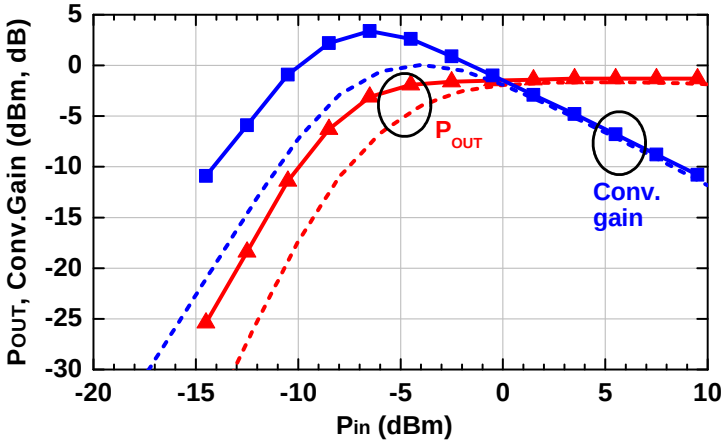
Figure 5.16: Power measurement setup.



(a)



(b)



(c)

Figure 5.17: Measured P_{out} and conversion gain of the quadrupler at (a) 70 GHz, (b) 90 GHz, and (c) 110 GHz.

GHz is connected to the PM4 Erickson power meter (PM4, Virginia Diode, Inc.) using WR-10 probe to measure the output power. The loss of the input and output probes as well as cable and waveguide losses are de-embedded, and the reference plane of the power measurement is GSG probe tips, and the simulation takes into account of the loss of pads.

Fig. 5.17a-c shows P_{out} and conversion gain vs P_{in} at low-, mid- and high-frequency of the desired bandwidth. (70, 90, and 110 GHz). The measured peak output power of -0.4 dBm, 2.9 dBm and -1.5 dBm is achieved at 70, 90, and 110 GHz, respectively with very good agreement with the simulation. The measured peak conversion gain is also presented and is 2.4, 10.2, and 3.4 dB, respectively. Fig. 5.18 presents measured DC current versus input power at 90 GHz and the main contributor of increasing DC current with increased input power is two frequency doublers.

The simulated and measured peak output power vs frequency over $70-110$ GHz is presented in Fig. 5.19a. The measured peak output power is -1.3 to 2.9 dBm at $70-110$ GHz with <1 dB difference from the simulation. The output power versus frequency with different input power is also presented in Fig. 5.19b. Higher than 0 dBm output output power is measured with the input power of -5 dBm at $80-105$ GHz and lower output power at <80 GHz and >105 GHz can be compensated by increasing input power. Fig. 5.19c shows conversion gain versus frequency with different input power. The peak conversion gain of 10 dB, 7.5 dB, and 2.8 dB with 3-dB bandwidth of 25 GHz or higher are measured.

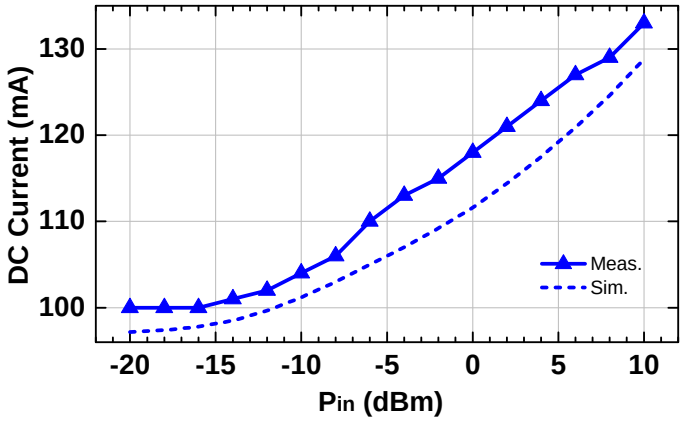


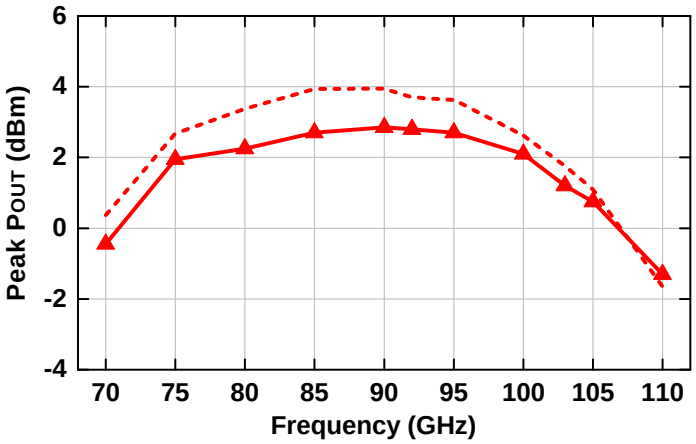
Figure 5.18: DC current vs P_{in} at 90 GHz output.

In addition to output power measurement (4th), 3rd and 5th harmonics are also measured with the measurement setup shown in Fig. 5.20. Due to limited frequency range of using spectrum analyzer, balanced mixer (WR-10 or 7-65 GHz mixer) is used to down-convert the output signal, and LO signal is generated using VDI-AMC 332, 334-335 multiplier chains depending on the harmonic frequency to be measured. Due to wide output bandwidth, $3f_o$ varies from $52.5-82.5$ GHz, and therefore, two separate measurement setups are required. Either setups are used based on whether $3f_o$ is above (Fig. 5.20a) or below 70 GHz (Fig. 5.20b). In addition, 5th harmonic is also measured using the setup shown in Fig. 5.20a, however, due to wide output bandwidth, $5f_o$ varies from $87.5-137.5$ GHz, and is only measured when $5f_o < 110$ GHz. The measured 3rd, 4th (desired output), and 5th harmonics when $4f_o$ = 75 GHz and 85 GHz are shown in Fig. 5.21a-b. The measured peak 3rd harmonic (56.25 GHz) and 5th harmonic (93.75 GHz) are -31 dBm and -60 dBm, respectively, agreeing with simulation very well and resulting in worst harmonic rejection of -33 dBc (Fig. 5.21a). In the same manner, 3rd and 5th harmonics are measured when $4f_o$ = 85 GHz, having worst HRR of -40 dBc (Fig. 5.21b).

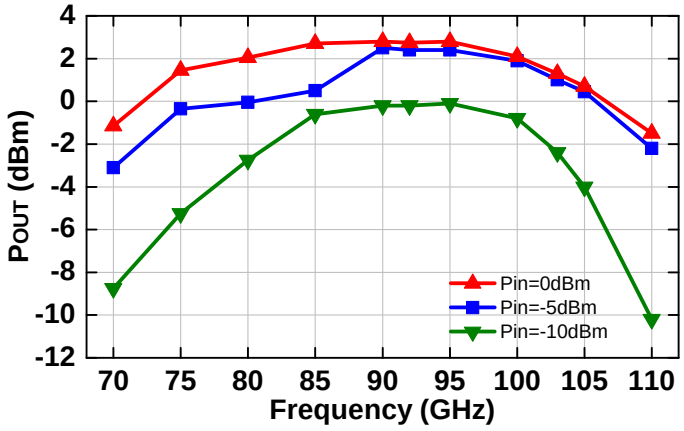
The overall 3rd and 5th harmonic level together with desired 4th harmonic is shown in Fig. 5.22 The 3rd and 5th harmonics are present below -26 dBm, resulting in $>$ 29 dBc worstcase HRR at $70-110$ GHz together with -1.3 dBm to +2.9 dBm output power. Table **??** summarizes state-of-the-art frequency multiplier works with different frequency bands.

5.5 Conclusion

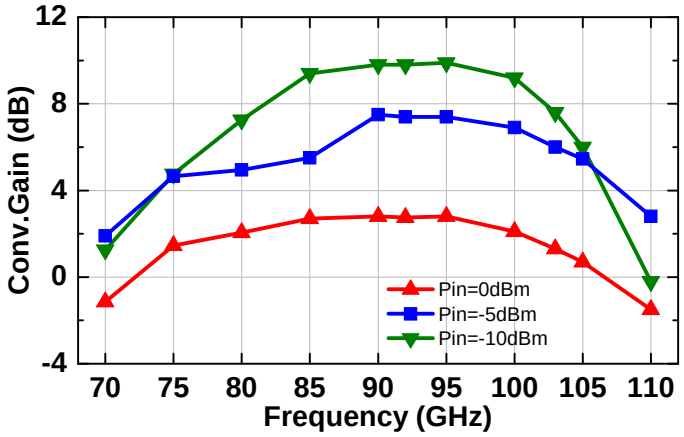
This work presented a 2-channel $70-110$ GHz wideband frequency quadrupler in GF8HP 0.12 µm SiGe BiCMOS process. The x4 frequency multiplication is achieved based on cascaded frequency doubler and inter-stage bandpass filter is implemented to reject adjacent undesired harmonics. Two inter-stage amplifiers are also implemented to drive enough power to the second frequency doubler and boost output power. The measured peak output power is -1.5 to 2.9 dBm



(a)

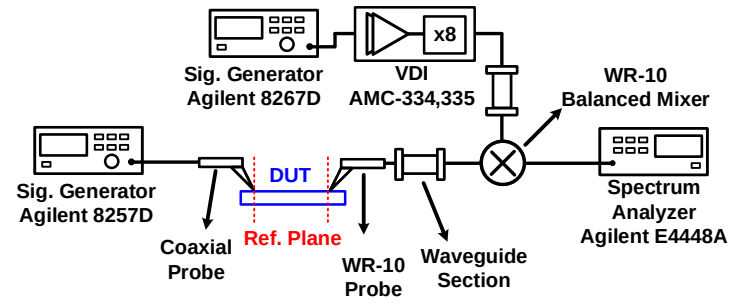


(b)

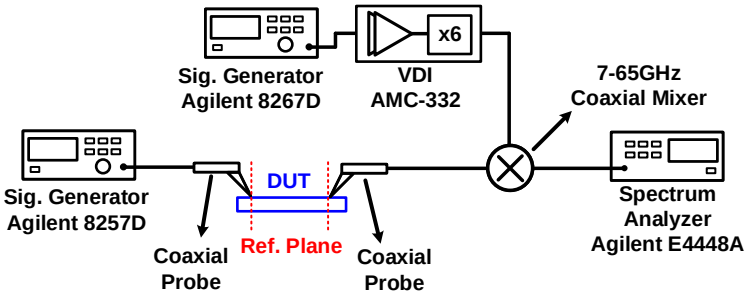


(c)

Figure 5.19: (a) P_{out} vs output frequency, (b) P_{out} vs output frequency with different P_{in}, and (c) conversion gain vs output frequency with different P_{in}.



(a)



(b)

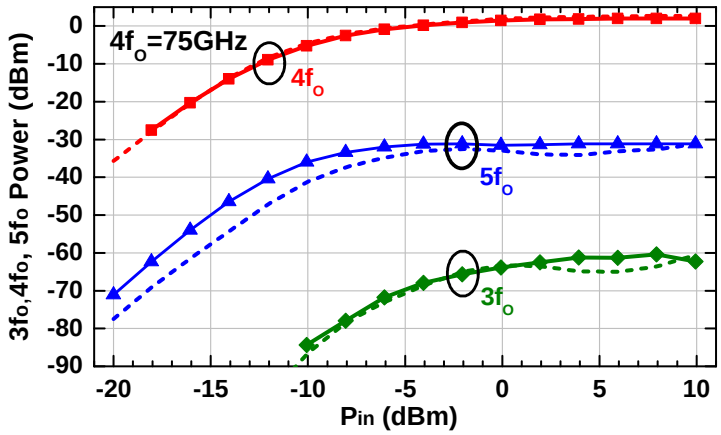
Figure 5.20: (a) Measurement setup of 3rd and 5th harmonics and (b) 3rd harmonic when $3f_o < 70$ GHz.

from $70-110$ GHz, with the worstcase harmonic rejection ratio (HRR) of > 29 dBc. The chip is 1.9 mm^2 and consumes 240 mW for 2-channel/ 170 mW for 1-channel operation with the input power of 0 dBm. It can be utilized high frequency LO source for various applications such as point-to-point communication, automotive radar (E-band), and high-resolution imaging system (W-band).

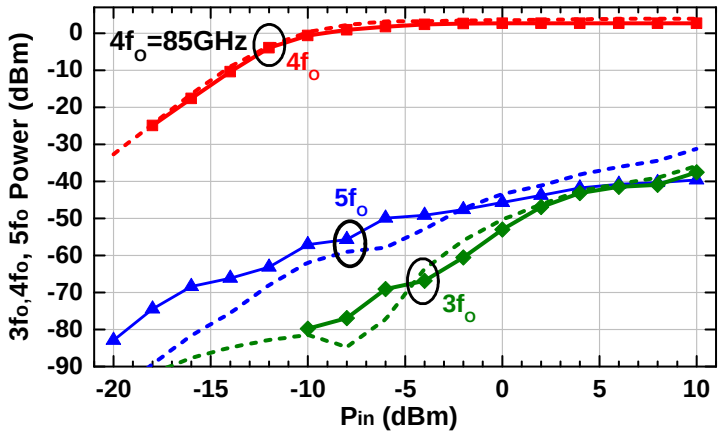
5.6 Acknowledgment

This work was supported by the Keysight Technologies and Global Foundries.

Chapter 5, in part, contains material that is currently being prepared for submission for publication as may appear in: B.-H. Ku, H. Chung and G. M. Rebeiz, "A Milliwatt-Level $70-110$ GHz Frequency Quadrupler with 30 dBc Harmonic Rejection", *IEEE Trans. Microw. Theory Techn.*, in preparation. The dissertation author was the secondary investigator and second author



(a)



(b)

Figure 5.21: Measured $3f_o$, $4f_o$ and $5f_o$ (a) when $4f_o$ = 75 GHz, (b) $4f_o$ = 85 GHz.

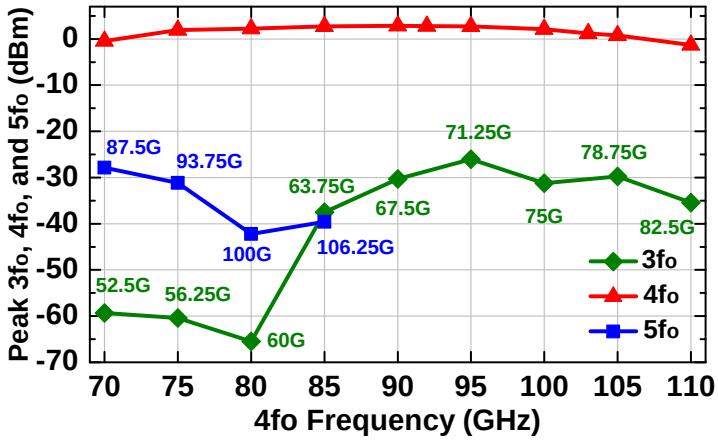


Figure 5.22: Measured $3f_o$, $4f_o$ and $5f_o$ harmonics.

Table 5.1: Comparison Table of State-of-the-art Frequency Multipliers

Ref.	Tech.	BW (GHz)	Topology	P_{out} (dBm)	P_{DC} (mW)	HRR (dBc)	Chip size (mm^2)
[95]	SiGe 90 nm	200−230	×4+PA	8	2900	N/A	3.63
[96]	SiGe 55 nm	138−152	×4+PA	0.5	630	N/A	1.95
[97]	SiGe 0.13-µm	121−137	×4	-2.4	35	N/A	0.38
[99]	SiGe 0.13-µm	124−132	×4	4.4	115	N/A	0.66
[100]	SiGe 0.13-µm	128−156	×4	0−4	132	N/A	0.17
[101]	SiGe 0.13-µm	116−136	×8	0−3	178	∼ 17	0.38
[102]	SiGe 0.13-µm	93−113	×4	0	124	N/A	0.39
[103]	CMOS 45 nm SOI	88−104	×2	10.2	241	N/A	0.27
[104]	CMOS 65 nm	88−99	×9	8.5	438	>31	0.45
[105]	SiGe 0.13-µm	72−80	×4	-4	79	N/A	0.42
[62]	SiGe 0.25-µm	52−75	×4	-10	11.7	∼ 10	0.42
[75]	SiGe 0.1-µm	45−57	×4	7.4−8.2	150	>22	1.4
[72]	SiGe 0.12-µm	10−40	×4	-8−1	60−84	>30	3.96
This work	**SiGe 0.12-µm**	**70−110**	**×4**	**-1−3**	**170**	**> 30**	**1.9**

of this material.

Chapter 6

A 4-Channel 10–40 GHz Wideband Receiver with Integrated Frequency Quadrupler for High Resolution Millimeter-Wave Imaging Systems

6.1 Introduction

Wideband local positioning systems and high-resolution radar imaging systems have been an area of research for several years with applications in security imaging, medical diagnostics and automotive radars. These systems require high image resolution to perform accurate object detection [60, 61, 107], and a critical factor is the system bandwidth. For instance, in order to achieve less than 5 mm range resolution, the system needs to operate over at least 30 GHz. Previously, this was achieved using systems above 100 GHz [61, 107], where 30 GHz is a small fractional bandwidth, but the work in [60, 61] showed that 10–40 GHz FMCW imaging systems can penetrate thick clothing and shoes, and is a preferred frequency range for security imaging.

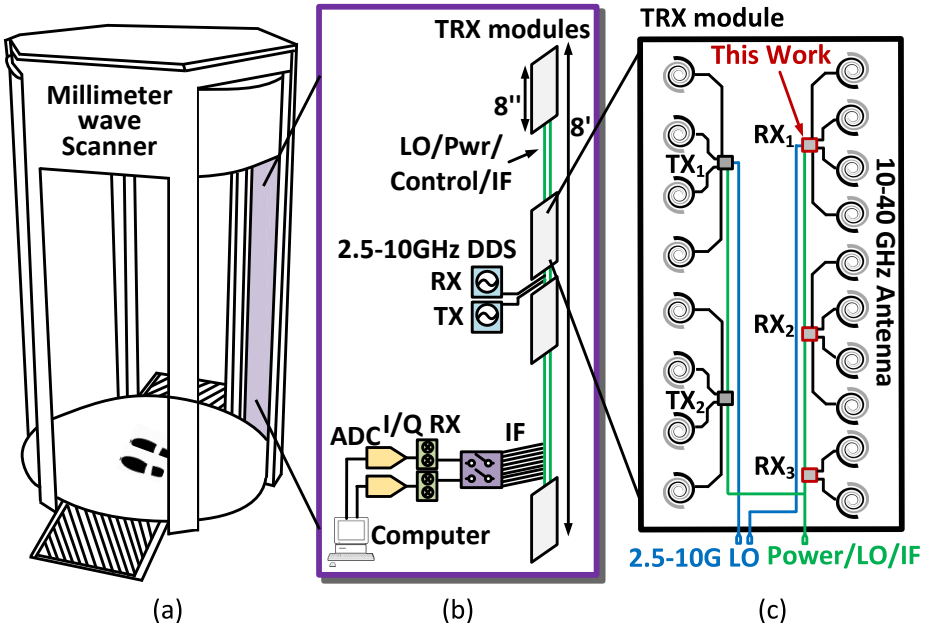


Figure 6.1: (a) Millimeter-wave portal security system, (b) linear array with TRX modules, (c) TX and RX chips with wideband antennas.

One important application is the airport security scanner. As shown in Fig. 6.1, multiple 10–40 GHz FMCW transceiver module boards are stacked in a linear fashion, and this covers the complete body range. Each transceiver board consists of 8 TX elements and 10 RX elements, and each SiGe chip can drive 4 elements. To reduce the cost of the direct-digital-synthesizer (DDS) and LO routing complexity, frequency quadruplers are integrated on the TX and RX chips. As a result, the required input LO chirp signals are reduced to 2.5–10 GHz.

This work presents the wideband 10–40 GHz 4-channel receiver with integrated LO quadrupler and its flip-chip packaging. The system-level measurements and FMCW experiements show that this work can be used in wideband, high-linearity, and high-resolution imaging systems.

6.2 Design

The wideband 4-channel receiver consists of two 0.3–42 GHz 2-channel receivers, a 10–40 GHz LO quadrupler, and an IF switch matrix (Fig. 6.2). The receiver core includes a low

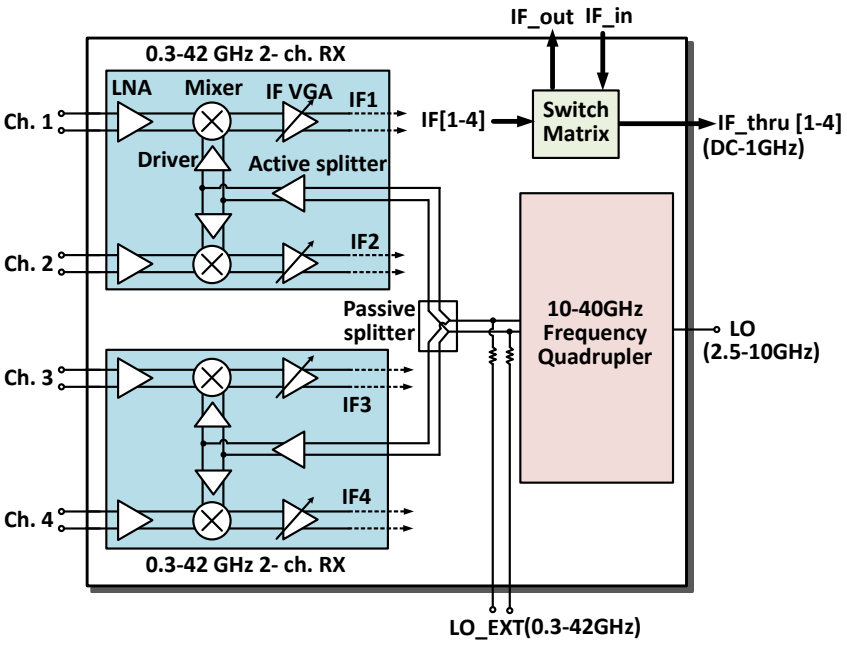


Figure 6.2: Block diagram of the 4-channel wideband receiver chip.

noise amplifier (LNA), a double-balanced mixer, and an IF variable gain amplifier (VGA). The chips requires a single-ended 2.5–10 GHz LO input, which is quadruplied to 10–40 GHz with high harmonic rejection ratio (HRR) [72]. Additionally, an external LO source (LO_EXT) is resisitively coupled to the output of the LO quadrupler, which can be used to drive the 4-channel receiver directly without frequency multiplication. The output LO signal from the quadrupler is split into two channels and amplified to drive the mixers. The RF ports are differential since they will be attached to wideband differential antennas such as a tapered slot or spiral antennas. The 4-channel IF outputs a switch matrix, which either pass the 4 IF output signals directly (IF_thru), or multiplexes any 2 IF signals (IF_out) from the local 4 IFs and external IF inputs (IF_in).

6.2.1 Low Noise Amplifier

Fig. 6.3 presents the schematic of low noise amplifier (LNA). The differential LNA is implemented using a single-stage cascode amplifier with resistive feedback. The common-emitter (CE) pairs are realized using 10 μm npn HBT transistors, biased at 4.5 mA. The resulting current

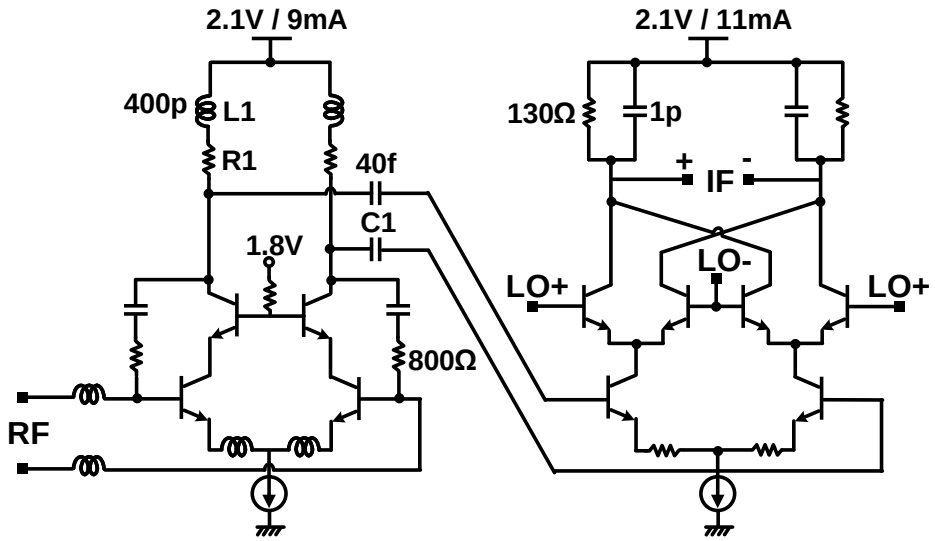


Figure 6.3: Schematic of the wideband LNA and double-balanced mixer.

density (0.45 mA /μm) presents a good trade-off between the optimum noise performance and optimum gain response. For common-base (CB) devices, a smaller size is used (5 μm) to reduce the parasitic capacitance at the output node. At the base of the CB pairs, no capacitance is used due to self-resonance problems over such a wide frequency range. Instead, a large biasing resistor is used to improve the common-mode rejection. To overcome the intrinsic cascode amplifier gain roll-off behavior and result in a broadband LNA, both resistive feedback and LC peaking techniques are used. The resistive feedback suppresses extra amplifier gain at lower frequencies and improves the linearity, while the LC peaking compensates the gain roll-off at the higher frequencies. A large feedback resistor value is chosen (800 Ω) to minimize noise figure(NF) degradation. LC peaking is implemented at the LNA output using wideband 400 pH single-turn inductors (L1) and 40 fF series capacitors (C1). The inductors are EM simulated with a self-resonance frequency of 61 GHz, allowing operation to $>$ 42 GHz. Also, 50 Ω load resistors are inserted to de-Q the output matching network but still generate a voltage gain at low frequencies (0.3-10 GHz). Input impedance matching is done using resistive feedback at $<$20 GHz and using 30 pH degeneration inductors and 120 pH series inductors at $>$20 GHz. The

simulated LNA available power gain is 11.5±1 dB from DC to 50 GHz with a NF of 2.5-4.5 dB, and an IP1dB of -13 ±2 dBm.

6.2.2 Double-Balanced Mixer

The mixer employs a double-balanced structure to reduce LO and RF leakage to the IF port (Fig. 6.3). To linearize the mixer, the gm-stage is degenerated using 20 Ω resistors. The degeneration also enhances the mixer bandwidth due to its negative feedback. At the IF port, an RC network is used to filter out unwanted high frequency components, such as LO leakage and the upper sideband mixing components. The cutoff frequency of the RC filter is designed so that the overall IF receiver bandwidth is around 1 GHz at the high-gain setting. Due to the significant voltage drop over the load resistor, the voltage headroom of each npn device is carefully chosen to avoid voltage limited distortion. Additionally, relatively larger transistor size (10 μm) is used to lower the device knee voltage (minimum V_{CE} required for active region). The mixer consumes 11 mA from a 2.1 V supply. The simulated mixer voltage conversion gain is 8±0.7 dB from DC to 50 GHz, with a single-sideband NF of 6-12 dB, and an IP1dB of -8±1 dBm. The LNA and mixer are co-optimized for wideband operation at the amplifier output using RLC network.

6.2.3 IF Amplifier

The first stage of the IF amplifier is a standard voltage feedback op-amp (Fig. 6.4a). By changing the resistance value across the op-amp (A1) from 600 Ω to 6 kΩ, around 18 dB variable gain is obtained. In this design, the variable resistors are implemented using PMOS devices with an external control voltage for their V_{GS}. Fig. 6.4b presents 1-stage op-amp (A1) and HBT devices are used to increase the open-loop gain. To drive a 100 Ω differential load, a voltage buffer is used after the op-amp. The voltage buffer employs a local negative feedback (formed by Q1 and Q2) to increase the input impedance and reduce the output impedance. As a result, the

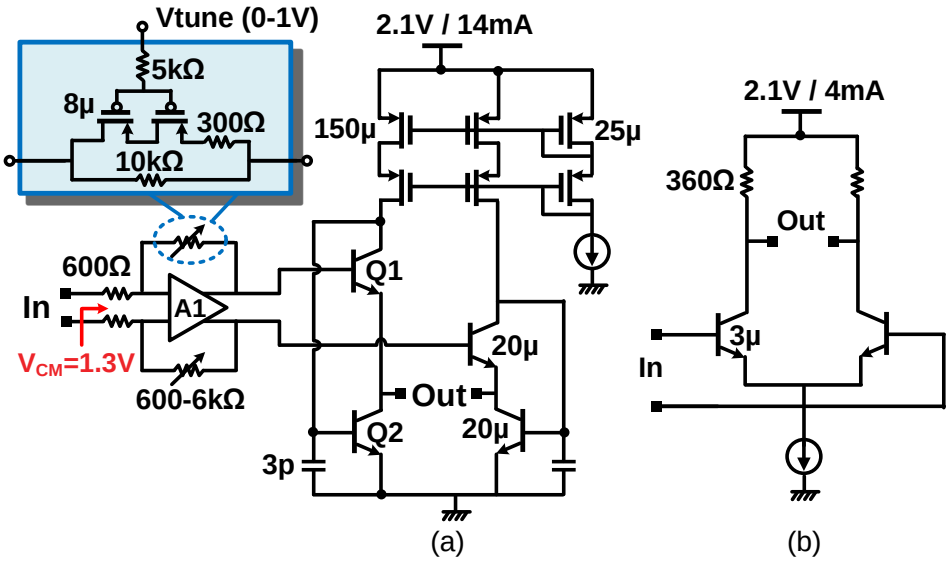


Figure 6.4: Schematic of (a) IF amplifier, and (b) 1-stage op-amp (A1).

voltage swing at the op-amp output can be delivered to the 100 Ω up to 1 GHz with almost no amplitude reduction. Moreover, the negative feedback in the voltage buffer significantly suppress its nonlinear distortion, which improves the IF amplifier output IP3. To stabilize the amplifier at high frequencies, a 3 pF capacitor is added within the feedback loop to reduce the loop gain beyond 1 GHz. The IF amplifier consumes 16 mA, and has a simulated OP1dB and OIP3 of +3.3 dBm and +23 dBm, respectively.

6.2.4 1-to-2 LO Splitter and Driver

The schematic of the LO driver is shown in Fig. 6.5. The first stage is an active splitter, which split the input LO signal into two channels in current mode. Compared to voltage splitting, current splitting is less sensitive to the parasitic loading capacitance and is more wideband. To handle a wide range of input LO power, large transistor size (13 μm) is chosen for the CE devices.

After splitting, a voltage buffer is used in each LO channel before driving the mixer. Each buffer branch is biased at 6 mA to achieve a P_{sat} of 0-3 dBm. The complete LO driver is designed inductorless in order to avoid any undesired magnetic coupling from the LO driver to the LNA.

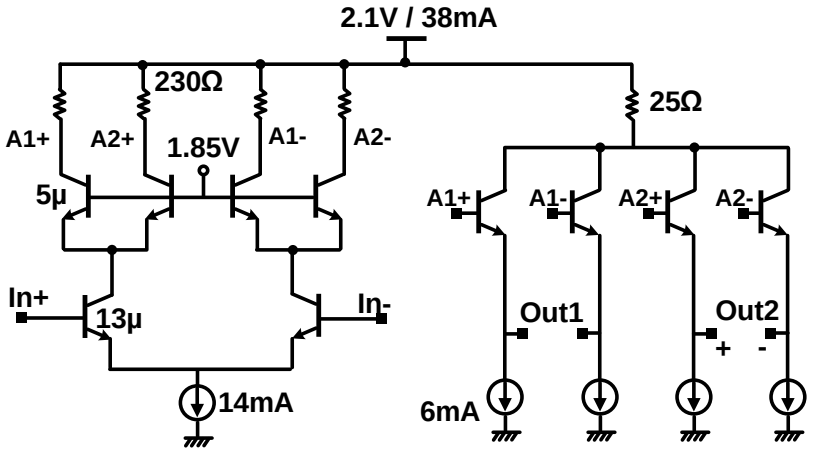


Figure 6.5: Wideband 1:2 inductorless LO splitter and driver.

This is because the LO power is substantially larger than the incoming RF signal. As a result, even a small amount of LO leakage through coupling may desensitize the receiver or radiate out from the antenna. The complete 1:2 LO driver consumes 38 mA, with a simulated gain of 5-7 dB from the input port to each channel output at DC to 45 GHz. Since the mixers require a minimum -5 to -3 dBm LO power for optimum gain and noise performance, a minimum LO power of -10 dBm is needed at the LO port.

6.2.5 2-Channel Receiver Measurement

Each receiver channel excluding the LO splitter and LO driver consumes 36 mA from a 2.1 V power supply. The complete 2-channel receiver block is designed and fabricated, and it consumes 232 mW (110 mA $\times$ 2.1 V). The receiver core shows a measured power conversion gain of 21 dB and 39 dB at low- and high-gain settings, respectively. The measured 3-dB gain bandwidth, regardless the gain settings, is $>$ 40 GHz and covers the 0.3–42 GHz range. The measured SSB NF of the receiver is 6.8–9.5 dB and 7.8–10.5 dB at high and low gain settings.

6.2.6 10-40 GHz LO Quardupler

A high harmonic-rejection 10–40 GHz LO quadrupler has been developed in [72]. To achieve >30 dB HRR over the entire bandwidth, the input signal is split into 3 different bands with switchable elliptic filters: 2.5–4 GHz (low-band), 4–6.5 GHz (mid-band) and 6.5–10 GHz (high-band). These bands generate an output at 10–16 GHz, 16–26 GHz and 26–40 GHz, respectively. The output power is 1 to -8 dBm at 10–40 GHz.

6.3 Measurements

6.3.1 Flip-chip 4–Channel Wideband Receiver

The wideband receiver is designed in a 0.12 μm SiGe BiCMOS technology (GlobalFoundries GF8HP) [89] and the chip photograph (3.6 mm $\times$ 2.3 mm) is shown in Fig. 6.6a. The chip was flipped on a 4-layer PCB with the stack-up shown in Fig. 6.6b for connectecrized measurements. RF channel 3 is transitioned in a differential fashion using a 100 Ω grounded-coplanar-waveguide (G-CPW) lines, while RF channels 1 and 2 are connecterized in single-ended fashion with one port terminated with 50 Ω. The complete IC consumes 260 mA from a 2.1 V including the LO multiplier and drivers.

The differential power conversion gain is measured using Keysight N5247A PNA-X. The IF frequency is fixed at 100 MHz, and 0 dBm LO is used at 2.5–10 GHz. As shown in Fig. 6.7, the complete receiver chip with packaging presents 19–36 dB variable gain and a 3-dB bandwidth of 10–40 GHz. The SSB NF, IP1dB, and IIP3 are also measured with external baluns used at the RF and IF ports. The measured SSB NF at the center frequency of 25 GHz is 9.3 (8.2 dB), and the measured overall IP1dB and IIP3 at 25 GHz are -17.2 dBm (-33 dBm) and -6.5 (-14) dBm, at low gain (high gain) settings, respectively. Table 6.1 summarize the key performance of the chip. Note that at the high gain mode, the P1dB is limited by the IF amp output buffer, which has

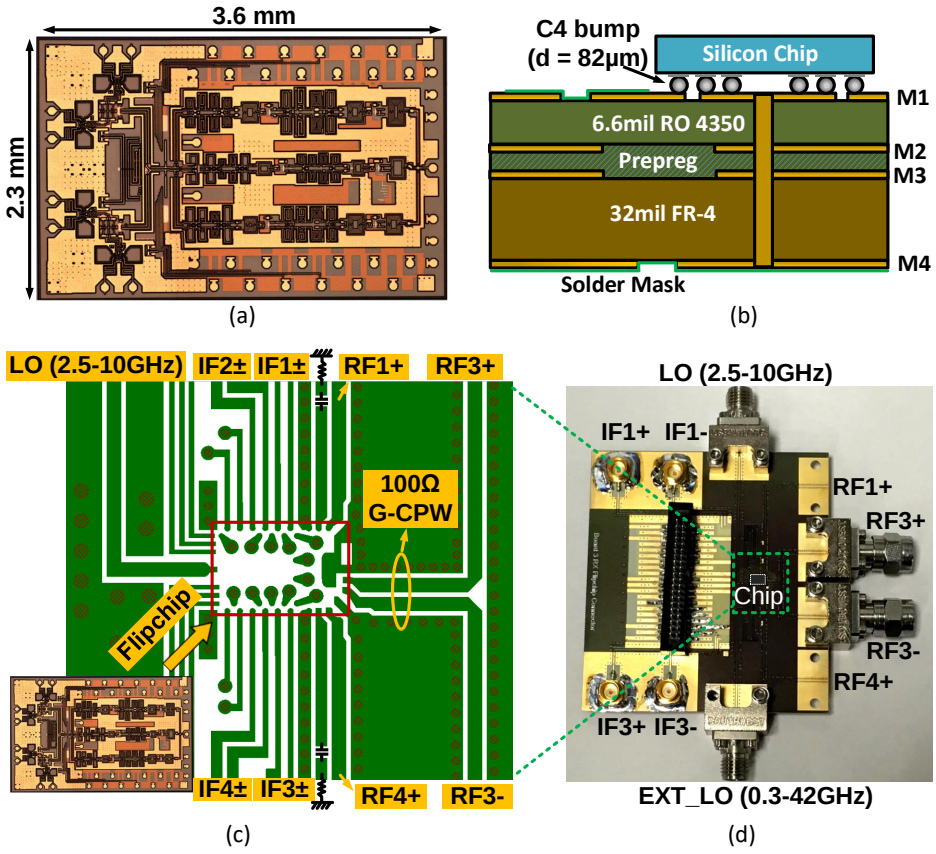


Figure 6.6: (a) Chip microphotograph (b) PCB stack-up (c) G-CPW transition around the chip area (d) flip-chip test board.

a negative feedback loop to suppress the IM3 distortion. As a result, the IIP3 in the high gain mode is 19 dB higher than the IP1dB. Table 6.1 summarizes the measured performance with the packaging.

6.3.2 FMCW Range Resolution Experiment

To demonstrate the imaging detection capability, an FMCW experiment has been performed using the wideband receiver. Fig. 6.8 and Fig. 6.9 present the measurement setup, where an additional 10–40 GHz TX chip with flip-chip packaging is used to transmit the FMCW signal. The TX chip consists of the same LO quadrupler that is used in the RX chip, and with a PA at the output to deliver up to +3 dBm RF power at 10–40 GHz. Two identical horn antennas with 20 dBi

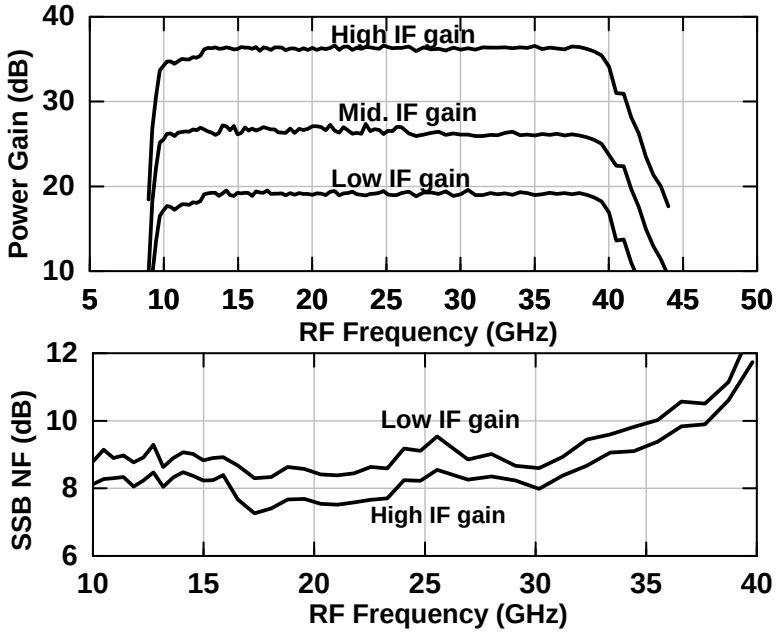


Figure 6.7: Measured differential power conversion gain and SSB NF of the 4-channel flip-chip wideband receiver.

gain are used. To fit with the antenna bandwidth, the chips are operated at 15–27 GHz, and this allows 12 GHz FMCW bandwidth with a theoretical range resolution of 1.25 cm. The LO chirp signals (3.75–6.75 GHz) are generated by the Keysight M8195A AWG with a ramping speed of 600 MHz/μs. To ensure the LO signals for TX and RX are synchronized, the differential output of the AWG is split into 2 single-ended outputs, and fed into the TX and RX chips, respectively. Two 0.5 cm diameter stainless steel spheres are used as targets for detection. The spheres are located at about R = 0.65 m from the antenna, with a separation ($\triangle$R) in between. The received

Table 6.1: Measured Chip Performance With Packaging

	High gain mode	**Low gain mode**
3dB RF BW (GHz)	10-40	
3dB IF BW (GHz)	1.1	1.8
Gain (dB)	36	19
SSB NF (dB)	8.2	9.3
IP1dB / OP1dB (dBm)	-33 / 2	-17.2 / 0.8
IIP3 / OIP3 (dBm)	-14 / 22	-6.5 / 12.5
Power Consumption (mW)	546	

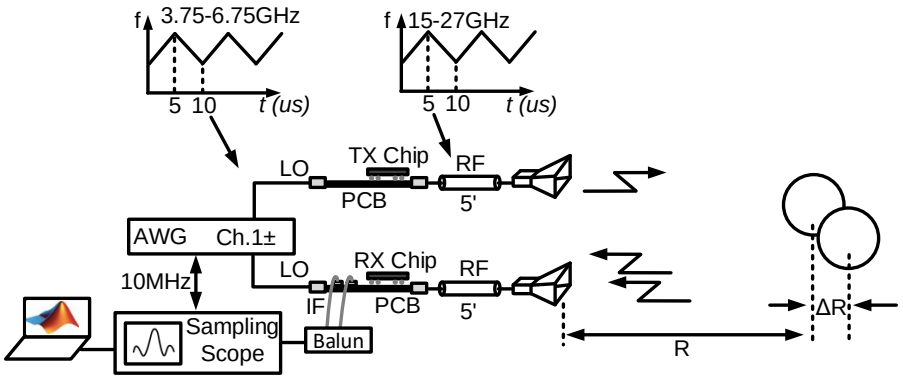


Figure 6.8: FWCW measurement setup using wideband RX and TX chips.

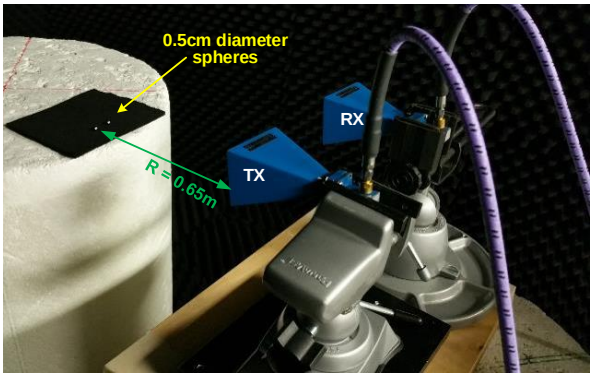


Figure 6.9: Picture of the FWCW measurement setup.

IF signal is 20–50 MHz and is sampled by the real-time sampling scope and then imported to Matlab for FFT and signal processing.

Experiments have been done with different $\triangle$R values. Fig. 6.10a presents the normalized IF spectrum (after FFT) for 2 spheres with $\triangle$R = 4.2 cm. Note that the x-axis has been converted to range and expressed in distance. To verify that the observed two peaks in the spectrum represent the actual two spheres, two experiments are done with and without the 2nd sphere. As expected, the two spectrums overlap for the first peak (sphere 1) but only the spectrum with 2 spheres shows the second peaking. To explore the smallest detectable distance, the two spheres are positioned with $\triangle$R = 1.3 cm. The measurement shows two clear peaks with a 15 dB drop in between at R =

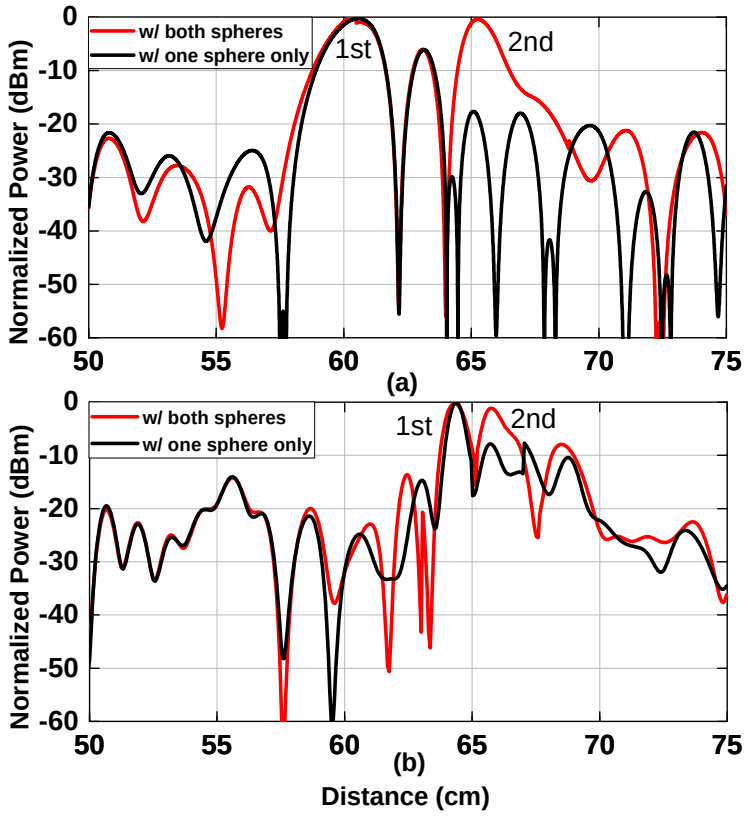


Figure 6.10: Measured normalized and processed IF spectrum for two metal sphere targets with a separation of (a) 4.2 cm and (b) 1.3 cm.

64.4 and 65.7 cm, respectively (Fig. 6.10b). This is close to the theoretical range resolution limit of a 12 GHz bandwidth, i.e. 1.25 cm. If the full 10–40 GHz bandwidth is utilized, the imaging system shown in Fig. 1 will be able to perform imaging detection with 0.5 cm range resolution.

6.4 Conclusion

This paper presented a 4-channel 10–40 GHz wideband receiver with integrated LO quadrupler and flip-chip package. The chip is optimized for low-noise and high-linearity, and the system-level measurements shows that this FMCW system can be used in wideband and high resolution imaging systems.

6.5 Acknowledgment

This work was supported by Analog Device Inc. (ADI) and Global Foundries.

Chapter 6 is mostly a reprint of the material as it appears in: Q. Ma, H. Chung and G. M. Rebeiz, “A 4-Channel 10–40 GHz Wideband Receiver with Integrated Frequency Quadrupler for High Resolution Millimeter-Wave Imaging Systems”, *IEEE International Microwave Symposium (IMS)*, June, PA, 2018, pp. 883-886. The dissertation author was the secondary investigator and second author of this paper.

Chapter 7

A low EVM SiGe BiCMOS 40–100 GHz Direct Conversion IQ Modulator for Multi-Gbps Communications Systems

7.1 Introduction

With the increasing demand of high data rate communications, wideband mm-wave transceivers have been a high-demand research area. Compared to FCC bands below 40 GHz, Q-, V-, E-, and W-bands provide larger available bandwidths and are capable of delivering multi-Gbps data rate. One of the remaining challenges is to build direct-conversion IQ modulators that cover multiple mm-wave bands and present low quadrature error and low EVM. Currently, this is done using GaAs or InP MMICs in a ceramic multi-chip module which leads to a large area on the board and in high cost. To reduce the cost, mm-wave silicon-based IQ modulators have been studied in the recent years [108–110]. However, published work covers only 1-2 of these bands and exhibits a large EVM, e.g. $>5\%$, for multi-Gbps data rate.

In this work, a wideband 40–100 GHz direct conversion IQ modulator with flip-chip

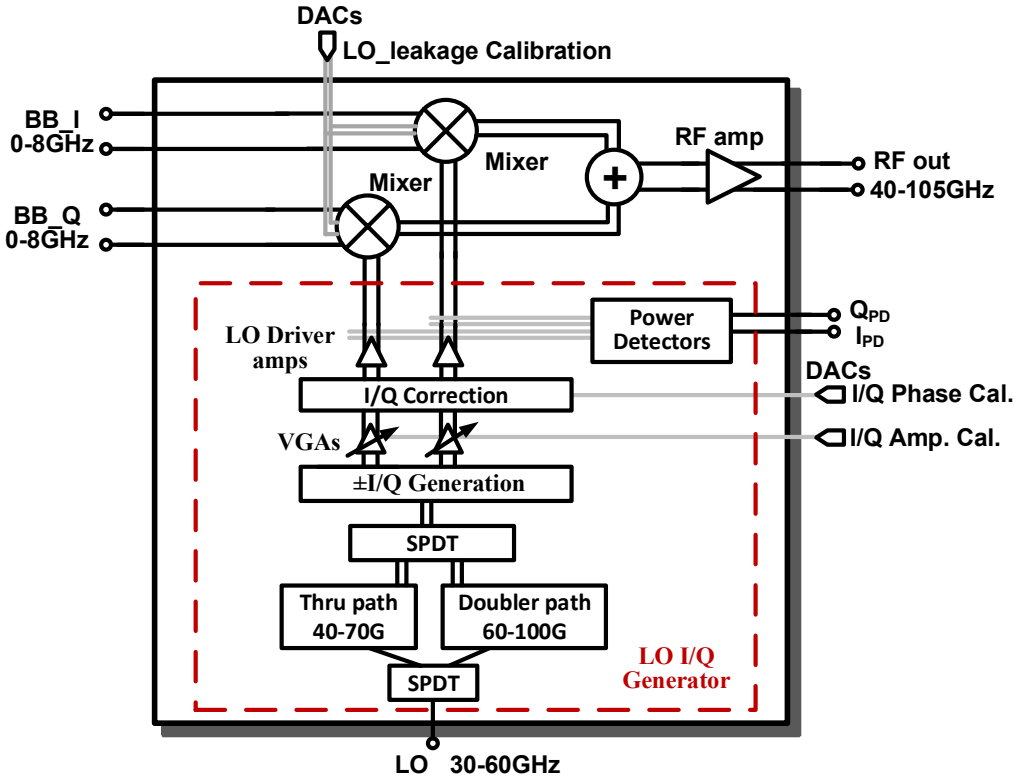


Figure 7.1: Block diagram of the 40–100 GHz direct-conversion IQ modulator.

packaging is presented in 0.12 µm SiGe BiCMOS technology. With the on-chip wideband IQ correction capability, the modulator maintains a single-sideband (SSB) >42 dBc and a LO leakage rejection >35 dBc over the entire bandwidth. A 64-QAM modulated signal with a data rate of 12 Gb/s and 2.4% error vector magnitude (EVM) is successfully demonstrated at 72 GHz.

7.2 Design

Fig. 7.1. presents the wideband IQ modulator. The signal path consists of two high-linearity double-balanced up-conversion mixers and an wideband RF amplifier. The output of the I/Q upconverters are summed using a wideband Wilkinson combiner and then fed into a differential RF amplifier. The base-band (BB) inputs are differential, dc-coupled, and with a bandwidth covers up to 8 GHz BB. The LO leakage of the modulator can be calibrated using

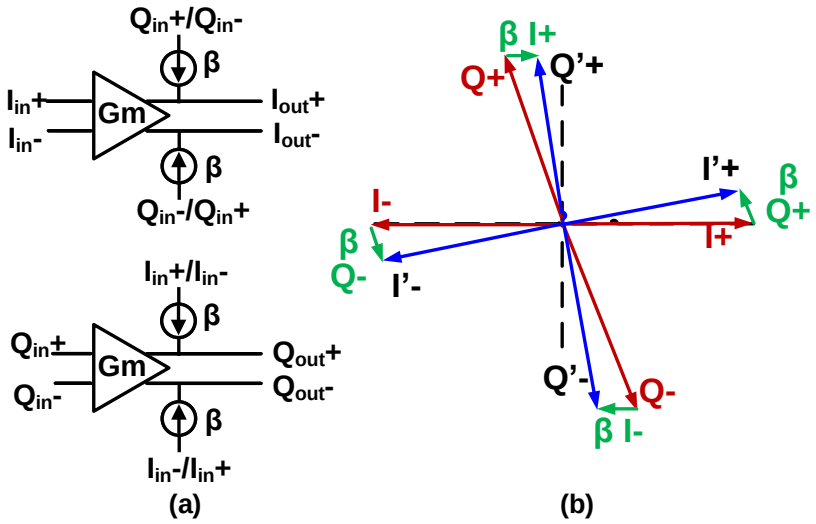


Figure 7.2: (a) LO I/Q phase error correction circuit, and (b) graphical view of the I/Q correction.

external digital-to-analog converters (DACs).

The 40-100 GHz LO I/Q generator consists of 3 parts: a frequency doubler, I/Q generation, and the I/Q phase correction. To ease the LO source generation, a frequency doubler is used (doubler path) to cover the 60−100 GHz band. Below 60 GHz, the fundamental LO (thru path) is used to minimize the undesired harmonic distortion. The two LO paths are designed to have an overlap of 10 GHz (60−70 GHz) to take into account any variation in process and temperature.

The wideband I/Q phase generation is implemented using a 2-stage constant phase polyphase filter (PPF) [111]. In theory, this type of PPF maintains a constant 90° phase difference between the I and Q channels at any frequency. In practice, however, due to process variation and the parasitic inductance of the interconnections, a non-zero I/Q phase error will be present. To overcome this issue, a wideband I/Q phase correction circuit is developed which is capable to correct the quadrature phase error up to +/- 20° . As shown in Fig. 7.2, by steering a small potion (β) of the input I+/I- (or I-/I+) signals and adding them to the Q+/Q- output channels (same for I channels), the relative phase difference between the I and Q paths can be reduced (or increased). The amount of phase correction depends on the value of β, and is controlled by the external DACs. In addition to the residual phase error, the constant phase PPF inherently exhibits I/Q amplitude

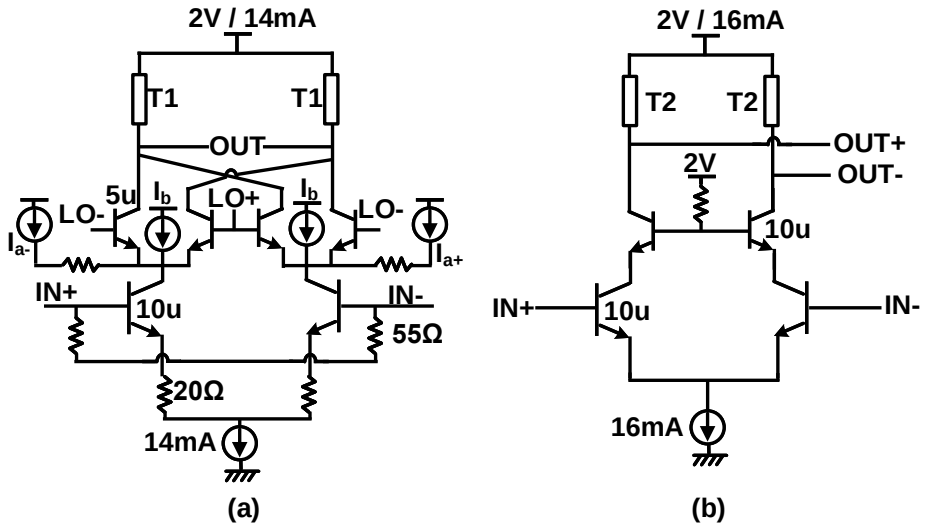


Figure 7.3: Schematic of (a) high-linearity up-conversion mixer, (b) and wideband 40−100 GHz RF amplifier.

error over frequency. This is solved by using high-gain LO drive amplifiers, which saturate both the I/Q LO signals at the mixers and eliminate the quadrature amplitude error. Moreover, fine amplitude tuning can also be performed using the integrated constant-phase variable-gain-amplifiers (VGAs) through the external DACs. At the output of the LO I/Q generator, power detectors are used to monitor the I/Q LO amplitudes.

The I/Q up-conversion mixers employ double-balanced structure to reduce the LO and IF to RF port feed-through (Fig. 7.3a). The mixer gm-stage is resistively degenerated to improve the input power handling capability and increase the IF bandwidth. Wideband input impedance matching is realized using two 55 Ω resistors. At the output, a differential transmission line (T1) is used as the inductive load. To maximize the output bandwidth, it is preferred to use smaller transistors for the switching quads for reduced parasitic capacitance. This, however, results in a small biasing current given an optimal current density for the device. On the other hand, the gm stage requires a large biasing current to maximize the input (and output) P1dB. As a result, an IF bleeding current (I_b) is used which increase the linearity of the gm-stage without increasing the dc current of the switching quads. In addition, an extra pair of current sources ($I_{a\pm}$) are used to

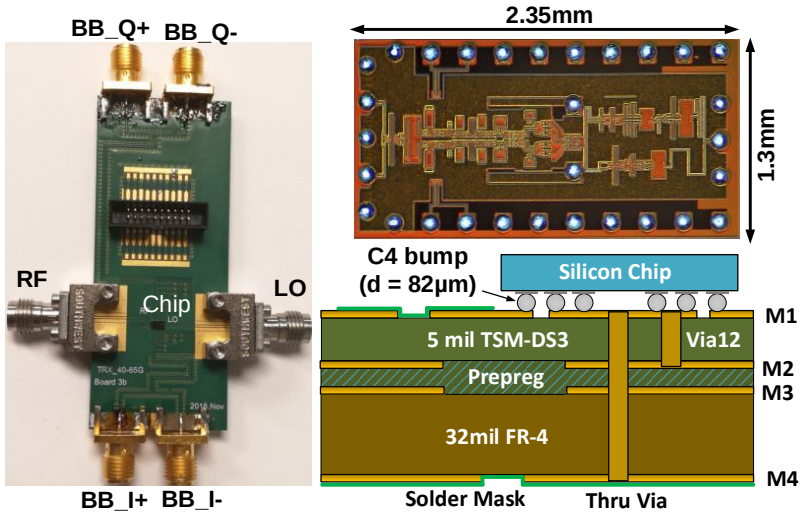


Figure 7.4: Flip-chip test board, chip microphotograph, and PCB stack-up.

generate a dc offset between the two Gilbert cell branches, and reduce the LO leakage.

The RF amplifier used after the I/Q mixers and Wilkinson combiner has a moderate gain and output P1dB (-3 dBm), and is mainly designed for wideband operation (Fig. 7.3b). In addition, a wideband inter-stage matching network is used between the I/Q mixers and the RF amplifier to cover the $40-100$ GHz RF bandwidth.

The I/Q modulator results in simulated IP1dB of -10 dBm with I and Q bandwidth of 8 GHz, a conversion gain of $8-9$ dB, and an OP1dB of -2 to -3 dBm at $40-100$ GHz. The simulated output noise is -155 dBm/Hz at 70 GHz, and allows for the generation of a 64-QAM 2 GBaud/s signal with $>$ 50 dB signal-to-noise ratio (SNR) at 7 dB average power back-off (-10 dBm average output power).

7.3 Measurements

The wideband modulator is designed in a 0.12 μm SiGe BiCMOS technology (GlobalFoundries GF8HP) [89] and the chip photograph (1.3 mm $\times$ 2.35 mm) is shown in Fig. 7.4. The complete IC consumes 250 mA from a 2 V power supply. The chip is flipped on a 4-layer

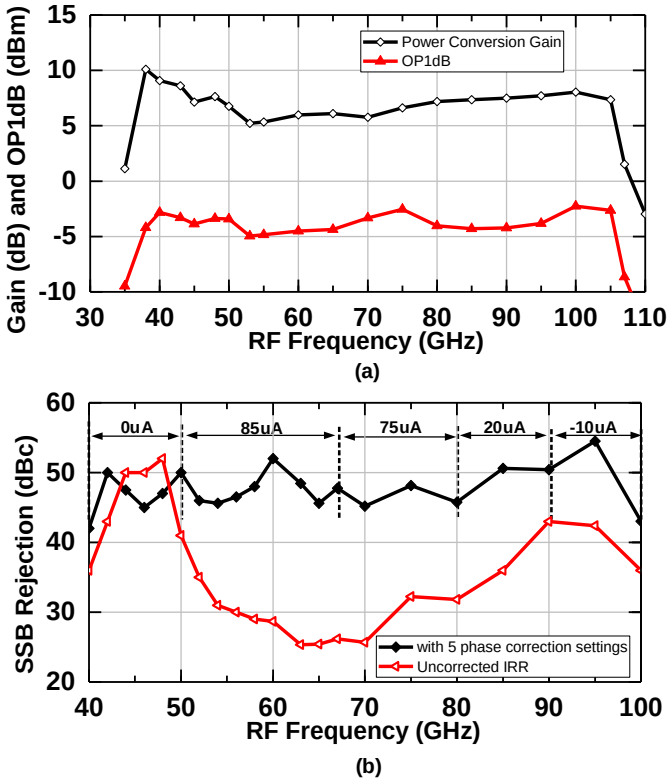


Figure 7.5: (a) Measured IQ modulator power conversion gain and output P1dB, (b) measured SSB rejection with and without IQ phase correction.

PCB with the stack-up shown in Fig. 7.4 for connectecrized measurements. A rat-race balun is implemented on the PCB to convert the differential RF output into a single-ended coaxial port. Due to the limited bandwidth of the balun, 3 different PCB boards with different balun designs are built to cover the 40−100 GHz band: 40−70 GHz (rat-race balun with 1.85 mm coaxial connectors) , 60−85 GHz (rat-race balun centered at 75 GHz and 1 mm connectors), and 80−100 (rat-race balun centered at 90 GHz and 1 mm connectors).

The IQ modulator power conversion gain and output P1dB are measured under SSB mode and with a fixed IF at 100 MHz. The reference planes were calibrated to be at the connectors. The modulator results is a conversion gain of 5−8 dB and an OP1dB of -3 to -5 dBm at 40−105 GHz (Fig. 7.5a). The measured single-sideband (SSB) rejection ratio of the modulator at 40−100 GHz is shown in Fig. 7.5b. With only 5 different phase correction settings using the external

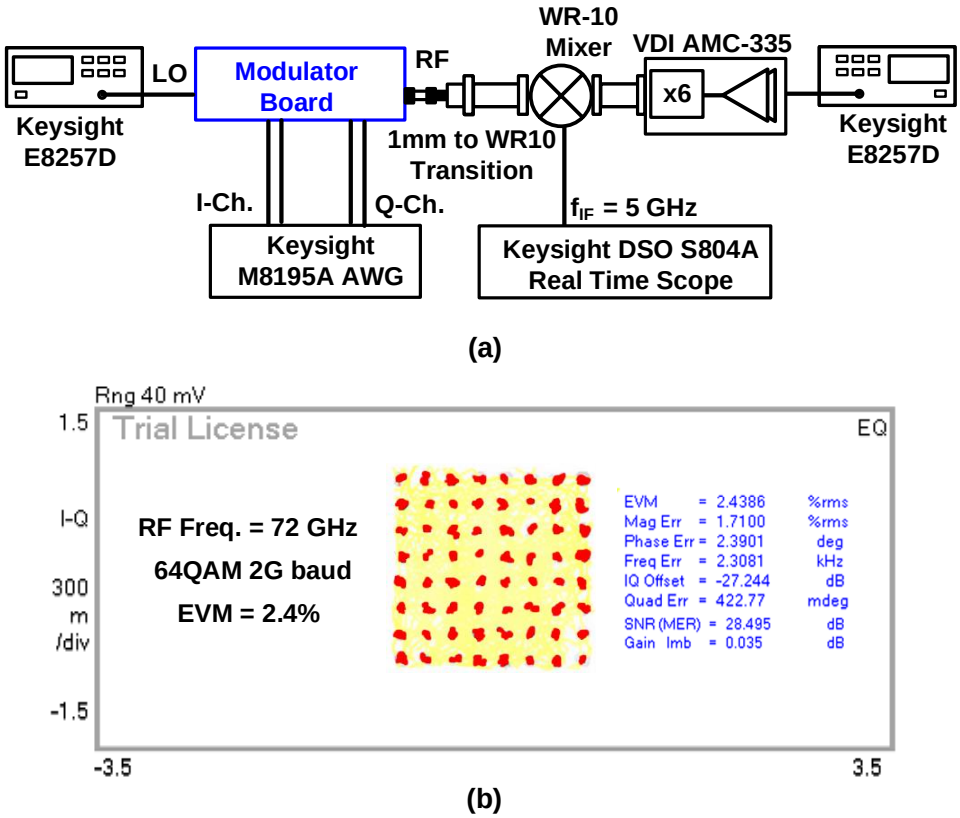


Figure 7.6: (a) EVM measurement setups, and (b) measured constellation at 72 GHz with 64-QAM 2 GBaud/s data rate at 4-dB back-off (12 Gb/s).

DACs, the overall SSB rejection can be maintained above 42 dBc over the entire 40−100 GHz frequency range. Each correction setting is valid for an instantaneous bandwidth of at least 10 GHz. These regions can be changed (re-centered to different frequencies) depending on the bias current. If no correction is applied, the modulator presents an intrinsic SSB rejection $>$ 25 dBc at 40−100 GHz. The measured LO leakage rejection with and without calibration is better than 35 dBc, compared to the signal level at the output P1dB.

Fig. 7.6a presents the setup for the vector signal measurements, where the baseband I/Q data is generated using a Keysight M8195A AWG, and the single-ended LO is provided by a Keysight E8257D signal generator. Below 72 GHz, the setup is fully coaxial and the modulator output is down-converted using a wideband mixer. For RF frequencies above 75 GHz, a 1 mm to WR-10 transition is used at the 1 mm coaxial RF port of the modulator board, and a WR-10

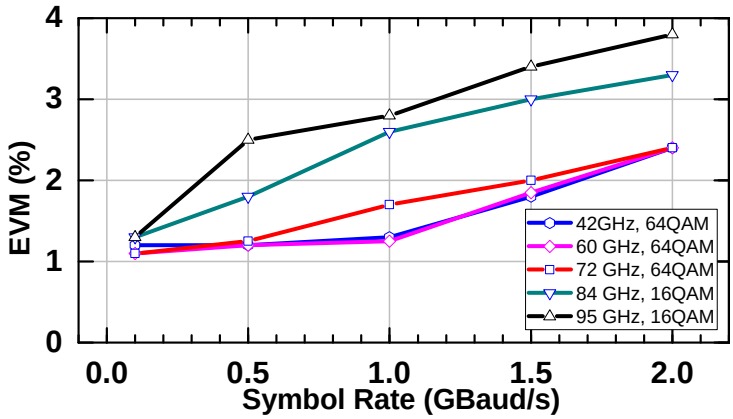


Figure 7.7: Measured EVM for 16/64QAM with 4-dB back-off at different data-rates and carrier frequencies.

mixer is employed for down-conversion. The WR-10 mixer local oscillator is generated using a VDI AMC-335 frequency multiplier. The modulated signal is down-converted to an IF of 5 GHz and demodulated using a real-time scope running the Keysight VSA 89600 software. Fig. 7.6b presents the measured constellation at a data rate of 12 Gb/s (2 GBaud/s) with the modulator operating at 4 dB back-off from P1dB. The measured EVM is 2.4% (-32 dB).

Fig. 7.7 presents the measured EVM at different data-rates and RF center frequencies. During these measurements, the modulator is always at 4 dB back-off from P1dB (back-off is defined from the peak of the constellation). Below 72 GHz, the modulator shows less than 2% EVM up to 9 Gb/s (64-QAM, 1.5 GBaud/s), and less than 2.4% EVM up to 12 Gb/s (64-QAM, 2 GBaud/s). At 84 and 95 GHz, a higher EVM is measured as the signal bandwidth is increased, indicating that the system SNR is starting to be limited by the measurement system noise (thermal noise and LO phase noise).

Fig. 7.8 presents detailed constellations at 60 GHz and 72 GHz. The 60 GHz is chosen with a low bandwidth (1 GBaud) and high-order modulation (64-QAM) and shows an excellent EVM of 1.3 % and a data rate of 6 Gbps (Fig. 7.8a). The 72 GHz is chosen with the widest tested bandwidth (8 Gbaud/s) and a high order modulation of 32-QAM (Fig. 7.8b). A 40 Gbps waveform can be achieved with an EVM of 5.2 % (-25.6 dB). This data rate is limited by the

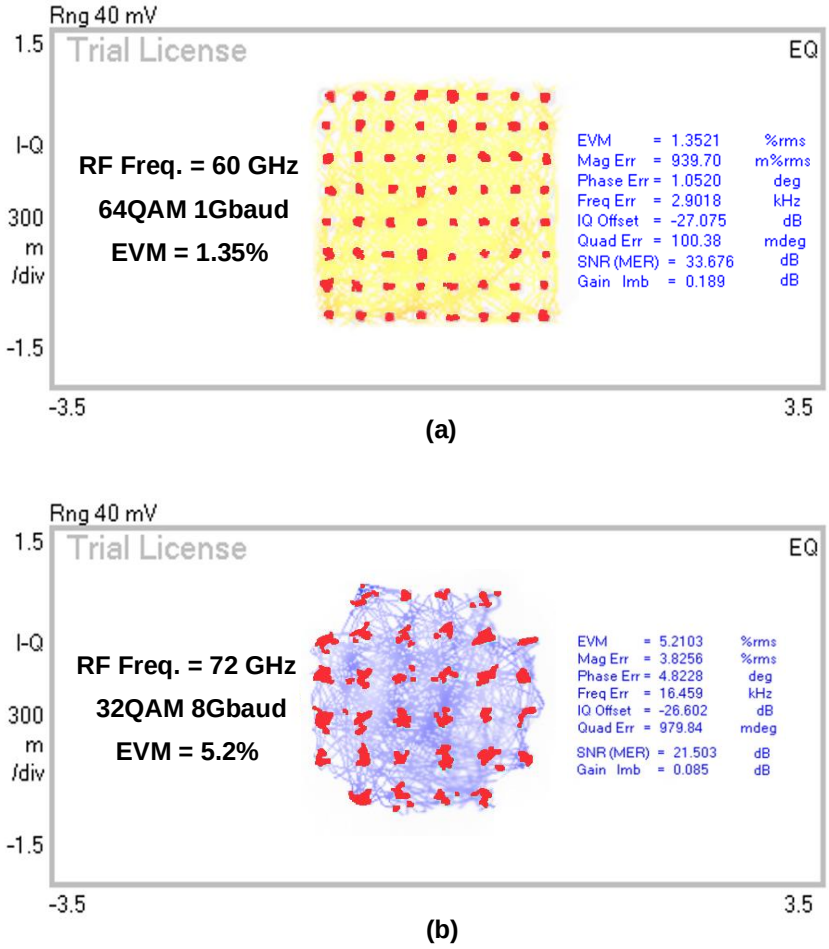


Figure 7.8: Measured EVM (a) at 60 GHz with a 64-QAM 1 GBaund/s waveform (6 Gbps data rate), and (b) at 72 GHz with a 32-QAM 8GBaud/s waveform (40 Gbps data rate).

external mixer response and the DSO scope (real time BW of 8.6 GHz) and not by the SiGe IQ modulator.

Fig. 7.9 presents 60 GHz measurements taken for 16- and 32-QAM waveforms versus back-off from P1dB (defined from constellation peak). The EVM is SNR limited at $0.7-1$ % up to -2 dB back-off, and remains <3 % even up to P1dB+2 dB. This shows that the I/Q modulator can have a wide range of operation and with low EVM.

Table 7.1 compares this work to the other published wideband modulators. This work achieves state-of-art performance in terms of RF bandwidth, wideband SSB operation, as well as the low EVM at multi-Gbps data rate.

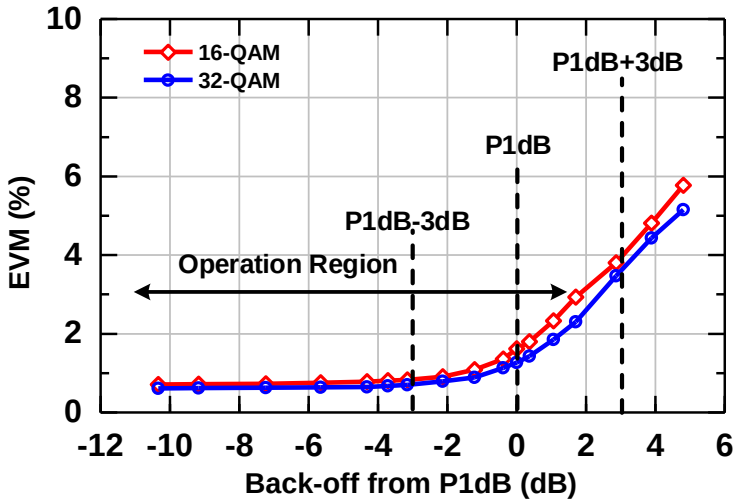


Figure 7.9: Measured EVM at a carrier frequency of 60 GHz and with different back-offs for 16- and 32-QAM waveform with BW=100 MHz.

7.4 Conclusion

This work presents a 40–100 GHz wideband direct conversion IQ modulator with flip-chip packaging. With wideband on-chip IQ correction capabilities, the modulator maintains a single-sideband (SSB) >42 dBc over the entire bandwidth, and results in very low EVM values under a wide range of waveforms, data rates and carrier frequencies. The IQ modulator can be used in wideband radios and instrumentation systems and can achieve a very low EVM for multi-Gbps communications and test systems.

7.5 Acknowledgment

This work was supported by the Keysight Technologies and Global Foundries.

Chapter 7, in full, is a reprint of the material as it appears in: Q. Ma, H. Chung and G. M. Rebeiz, “A low EVM SiGe BiCMOS 40–100 GHz direct conversion IQ modulator for multi-Gbps communications systems”, *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June, PA, 2018, pp. 188-191. The dissertation author was the secondary investigator and second author

of this paper.

Table 7.1: Performance Comparison of Different Wideband Modulators

Reference	[108]	[109]	[110]	[112]	**This work**
Technology	65nm CMOS	0.18μm SiGe	40nm CMOS	0.15μm GaAs	**0.12μm SiGe**
Bandwidth (GHz)	64-84	70-100	62-86	51-68	**40-100**
IRR (dB)	40-50	18-42	30-46	30-40	**42-51**
Data Rate	40Mb/s	8.75Gb/s	4.5Gb/s	3Gb/s	**12Gb/s**
EVM* (%)	2	6.6	6	4.9	**2.4**
LO Leakage (dBc)	<-30	<-18	<-40	<-15	<**-35**
Packaged	No	Yes	Yes	No	**Yes**

Chapter 8

A 35–105 GHz High Image-Rejection-Ratio IQ Receiver with Integrated LO Doubler and $>$ 40 dB IRR

8.1 Introduction

With the increasing demand for high data-rate communications, wideband mm-wave transceivers have been a high-demand research area. Compared to FCC bands available below 40 GHz, the Q-, V-, E-, and W-bands provide larger available bandwidths and are capable of multi-Gbps systems. One of the challenges is to build direct-conversion IQ receiver that covers multiple of bands and present low quadrature error and low NF. Currently, this is done using GaAs or InP MMICs in a multi-chip module, and leads to a large area and higher cost. To reduce the cost, silicon-based IQ receivers have been studied in the recent years [88, 109, 113]. However, the published work covers one or two bands and can only maintain $<$ 30 dBc IRR over the RF bandwidth.

In this paper, a 35–105 GHz wideband direct conversion IQ receiver with flip-chip

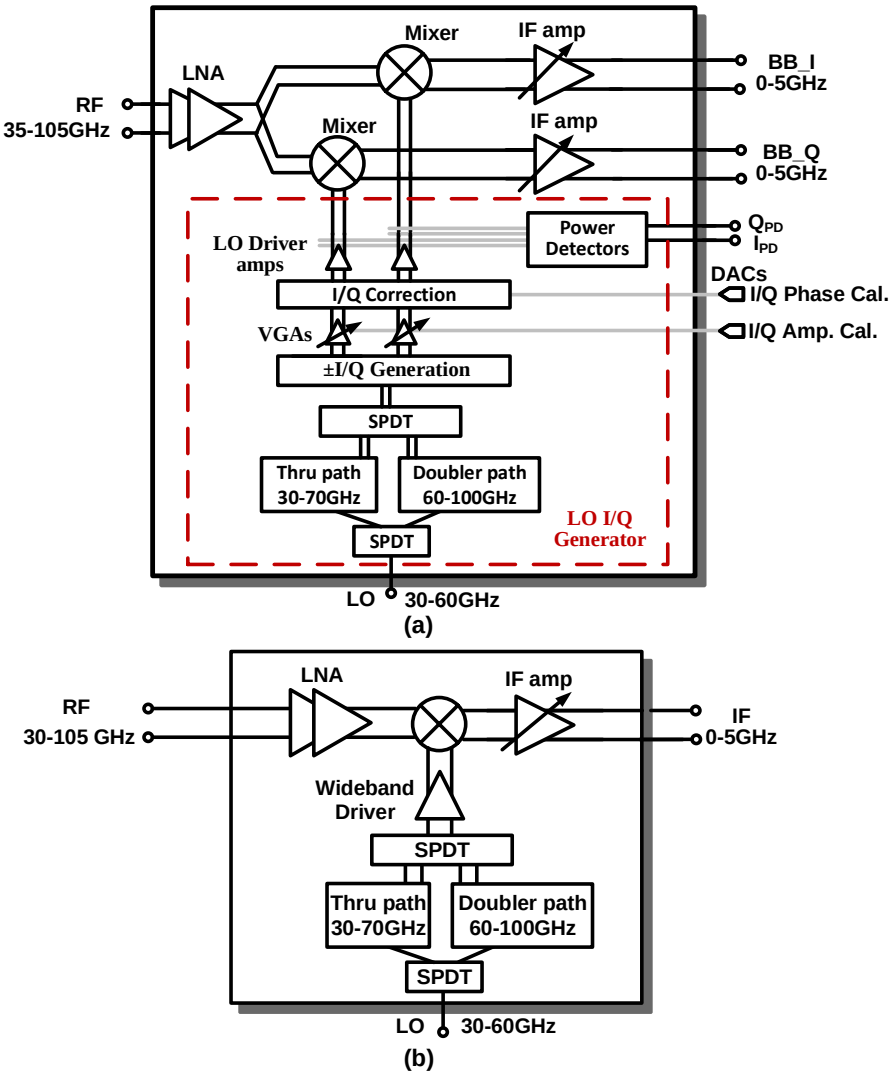


Figure 8.1: Block diagram of (a) 35–105 GHz IQ receiver, and (b) 30–105 GHz IF receiver.

packaging is presented. With an on-chip wideband IQ correction capability, the IQ receiver maintains an IRR >40 dBc and a DSB NF of 5–12 dB. An 30–105 GHz IF receiver is also realized with packaging using the same LO network. Both receivers can be used in multi-Gbps communication systems.

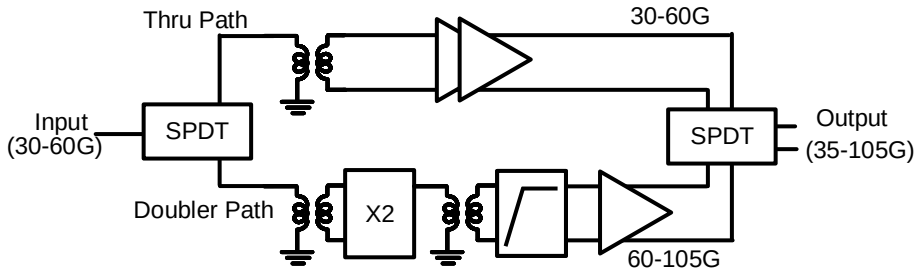


Figure 8.2: Implementation of the LO thru and doubler paths.

8.2 Design

Fig. 8.1 presents the block diagram of the wideband IQ receiver and IF receiver. In the IQ receiver (Fig. 8.1a), the 40–100 GHz LO I/Q generator consists of 3 parts: frequency doubler, I/Q generation, and I/Q phase correction. A block diagram of the LO path is shown in Fig. 8.2, and consists of a straight-thru and a doubled path. Below 60 GHz, the fundamental LO (thru-path) is used to minimize the undesired harmonic distortion. Above 60 GHz, a frequency doubler is used to lower the input LO frequency. Therefore, wideband transformers are required before and after the doubler to maintain a differential circuit. To minimize the fundamental LO feedthrough in the doubler path, a high pass filter (HPF) is added with a cut-off frequency of $\sim$ 60 GHz. After the LO doubler, a wideband I/Q signal is generated using a differential 2-stage constant-phase polyphase filter (PPF) [111]. In theory, the PPF can maintain a constant 90° phase difference between I and Q channels at any frequency. In practice, however, due to process variation and the parasitic inductance of the interconnection, a non-negligible (+/-5-10° at $35-105$ GHz) I/Q phase error will be present, and this will greatly reduce the image rejection. To overcome this issue, an ultra-wideband I/Q phase correction circuit is developed which is capable of correcting the quadrature phase error up to +/- 20° . As shown in Fig. 8.3, by steering a portion (β) of the I signal and adding it to the Q branches (similarly adding Q to I), the relative phase difference between the output I and Q paths can be reduced or increased depending on the polarity of summing. The amount of phase correction depends on the value of β, which is controlled using external DACs. In

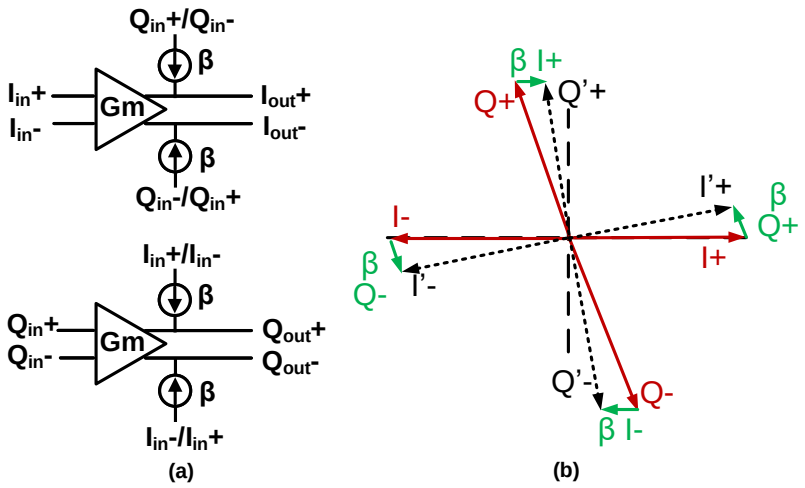


Figure 8.3: (a) LO I/Q phase-error mechanism, and (b) graphical view of the I/Q correction.

addition, the constant phase PPF inherently exhibits I/Q amplitude mismatch over frequency. This is solved by using high-gain saturated LO driver amplifiers at the mixers, and this eliminates the quadrature amplitude error. Moreover, fine amplitude tuning can be performed using integrated constant-phase variable-gain-amplifiers (VGAs) through the external digital-to-analog converters (DACs). In the IF receiver (Fig. 8.1b), the same LO path is used and is followed by a wideband LO driver amplifier.

Fig. 8.4a presents the wideband LNA design in the IQ receiver. The LNA consists of 2 cascode amplifier stages which provide high gain as well as good reverse isolation. The common-emitter transistors in the LNA are biased at 0.5mA/μm, which achieves a good trade-off between the noise and gain performance. The LNA input matching is designed with consideration of the parasitic capacitance from the GSG pads and the bump inductance from the flip-chip package. Differential transmission lines ($Z_{0,\text{diff}}$ = 120 Ω) are used to realize the inductance above 100 pH, e.g. T1-T6. A tapped L-C-L configuration is used at the output of each cascode stage as it provides a wide matching bandwidth. A 10 Ω resistor is used to de-Q the output matching network and provides wider overall gain response. The LNA consumes 20 mA and provides 12 dB voltage gain when loaded with the I/Q mixers. The LNA in the IF receiver chip has the same architecture shown in Fig. 8.4a but with slightly different L, C values to match with a single

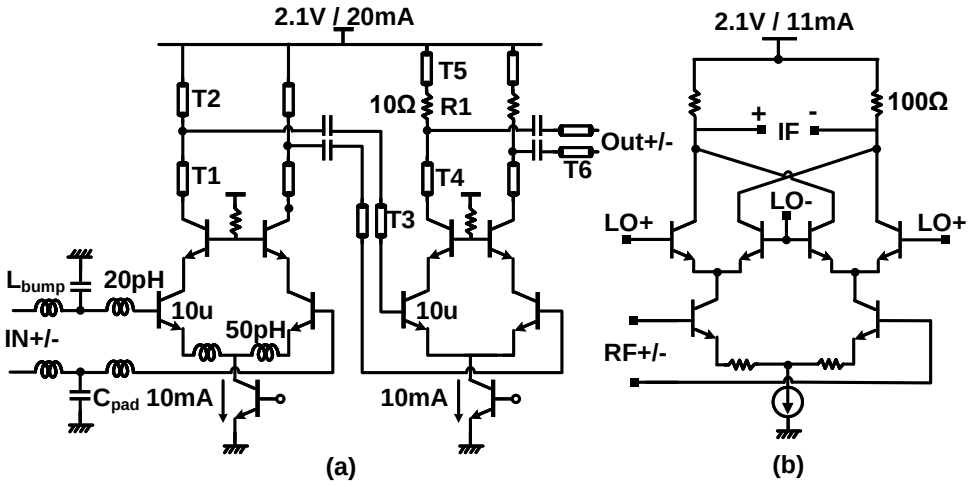


Figure 8.4: Schematic of 30–105 GHz (a) wideband LNA, and (b) down-conversion mixer.

mixer. The mixers are double-balanced mixer with resisitive degeneration to have a high input P1dB (Fig. 8.4b). The IF variable gain amplifier (VGA) provides 12.5 and 15 dB continuous variable gain for IQ receiver and IF receiver, respectively, and both are designed to have greater than 5 GHz baseband (IF) bandwidth.

8.3 Measurements

Both receivers are designed in a 0.12 μm SiGe BiCMOS technology (GlobalFoundries GF8HP) [89] and the IQ receiver chip photo is shown in Fig. 8.5. The chips are flipped on a 4-layer PCB with the stack-up shown in Fig. 8.5 for the connecterized measurement. A rat-race balun is implemented on the PCB to convert the differential RF output into single-ended. Due to the limited bandwidth of the balun, 3 different PCB boards with different balun designs are built to cover the 35–105 GHz range: 30–65 GHz, 60–85 GHz, and 80–105 GHz. The IQ receiver and IF receiver chips consume 285 mA and 120 mA, respectively, from a 2.1 V supply.

The power conversion gain and NF measurement are performed on chip with GSG RF probes. During the measurement, the IF frequency is fixed at 100 MHz. The IQ receiver results in 21–33 dB flat gain at 35–105 GHz, and the IF receiver shows an average gain of 18–33 dB at

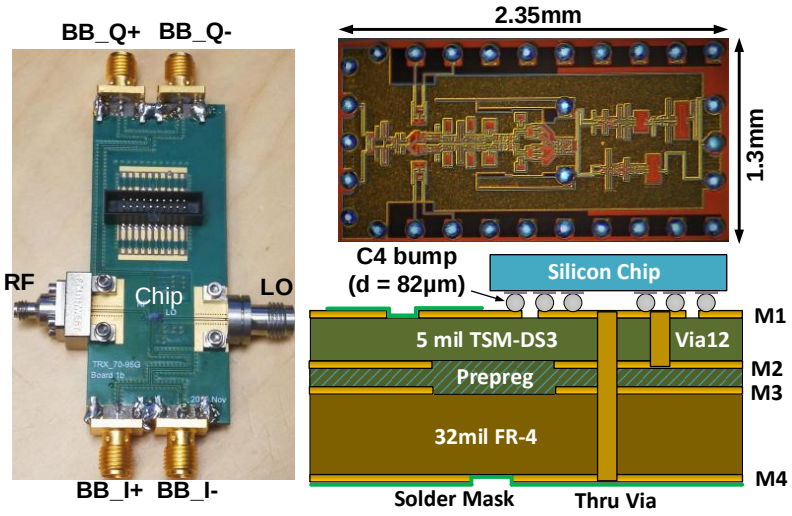


Figure 8.5: Flip-chip test board, chip microphotograph, and PCB stack-up.

30–105 GHz (Fig. 8.6). In general, the measured gain agrees well with simulations, except that the inductive peaking at 90 GHz shifts up to 100 GHz. This is because some load inductors are over-estimated in the EM simulations. Fig. 8.7 presents the simulated and measured DSB NF of both receivers at high IF gain settings. Both receivers result in a measured NF of $5-11.5$ dB at $35-105$ GHz. At the low IF gain settings, the NF only degrades by 0.2–0.4 dB for both receivers.

The IF bandwidth, linearity, and IRR performance of both receivers are measured on the PCB board with the flip-chip package. The measured 3-dB IF bandwidth of both receivers is 5 GHz at low IF gain setting and 4 GHz at high IF gain settings (not shown). During the IRR measurement, an external 90° coupler is used to sum the I/Q IF outputs. As shown in Fig. 8.8, the IQ receiver maintains an IRR better than 40 dBc at 35–105 GHz with only 5 phase correction settings. Each correction setting is valid for an instantaneous bandwidth of at least 10 GHz. Note that the measured IRR also includes the quadrature error from the external 90° coupler. Fig. 8.9 presents the measured input P1dB and IP3 for both receivers at low IF gain settings. At a center frequency 65 GHz, the measured input P1dB and IP3 are -21.5 dBm and -11 dBm for the IQ receiver, and -17.5 dBm and -7.5 dBm for the IF receiver, respectively. In the IP3 measurements,

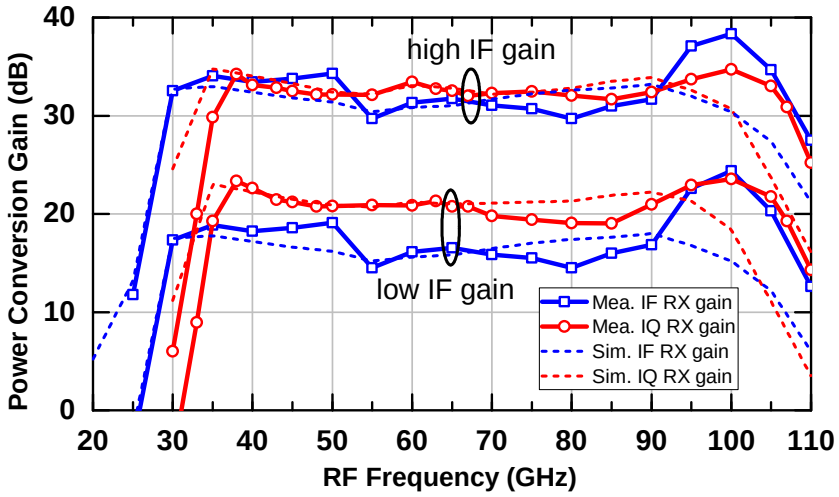


Figure 8.6: Measured power conversion gain and of the IQ receiver (red) and IF receiver (blue).

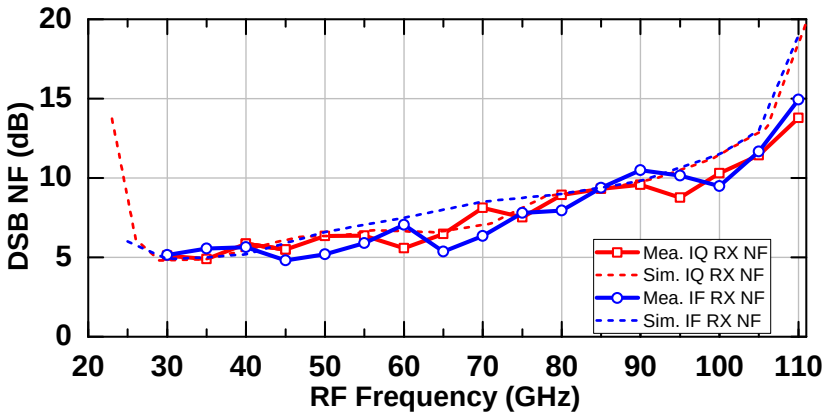


Figure 8.7: Measured DSB NF of the IQ receiver (red) and IF receiver (blue).

a 100 MHz two-tone spacing is used and the measurement is done up to 65 GHz as it is difficult to generate a two-tone signal beyond 67 GHz. At the high-gain setting, both receivers are limited by the IF VGAs thus have a constant output P1dB (-2 dBm) and output IP3 (+8.8 dBm) over frequency.

Table 8.1 compares the wideband IQ receiver to other publications. This work achieves state-of-art performance in terms of RF bandwidth and wideband IRR performance.

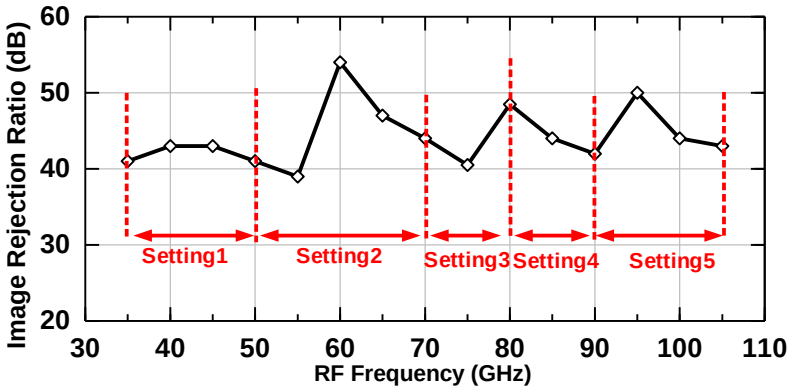


Figure 8.8: Measured image rejection ratio of the IQ receiver.

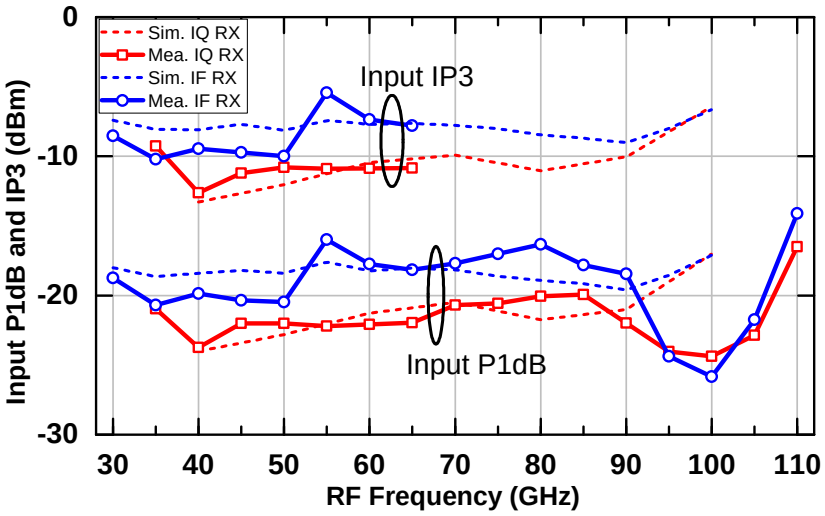


Figure 8.9: Measured input P1dB and IP3 of the IQ receiver (red) and IF receiver (blue).

Table 8.1: Performance Comparison of the Wideband IQ Receiver

Reference	[113]	[88]	[109]	This Work
Technology	90nm CMOS	0.12μm SiGe	0.18μm SiGe	**0.12μm SiGe**
Bandwidth (GHz)	76–88	76–84	70–100	**35–105**
Gain (dB)	-3	13–34*	37	**21–33**
IRR (dB)	>40	>20	>20	**>40**
DSB NF (dB)	N/A	11.4–13	6–9	**5–11.5**
Package	No	Yes	Yes	**Yes**

*Voltage conversion gain

8.4 Conclusion

This work presented a 35–105 GHz IQ receiver and a 30–105 GHz IF receiver with flip-chip packaging. With the on-chip wideband IQ correction capabilities, the IQ receiver maintains a IRR $>$40 dBc over the entire bandwidth. The presented IQ receiver and IF receiver can be used in low-cost and wideband multi-Gbps communication systems.

8.5 Acknowledgment

This work was supported by the Keysight Technologies and Global Foundries.

Chapter 8, in full, is a reprint of the material as it appears in: Q. Ma, H. Chung and G. M. Rebeiz, "A 35–105 GHz high image-rejection-ratio IQ receiver with integrated LO doubler and $>$ 40 dB IRR", *IEEE International Microwave Symposium (IMS)*, June, PA, 2018, pp. 595-598. The dissertation author was the secondary investigator and second author of this paper.

Bibliography

[1] H. J. Liebe, T. Manabe, and G. A. Hufford, "Millimeter-wave attenuation and delay rates due to fog/cloud conditions," *IEEE Trans. Antennas and Propagation*, vol. 37, no. 12, pp. 1617–1623, Dec. 1989.

[2] S. Rangan, T. S. Rappaport, and E. Erkip, "Millimeter-wave cellular wireless networks:potentials and challenges," *Proceedings of the IEEE*, vol. 102, no. 3, pp. 366–385, March 2014.

[3] P. Candra, V. Jain, P. Cheng, J. Pekarik, R. Camillo-Castillo, P. Gray, T. Kessler, J. Gambino, J. Dunn, and D. Harame, "A 130nm SiGe BiCMOS technology for mm-wave applications featuring HBT with f_T/f_{MAX} of 260/320 GHz," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2013, pp. 381–384.

[4] W. Haensch, E. J. Nowak, R. H. Dennard, P. M. Solomon, A. Bryant, O. H. Dokumaci, A. Kumar, X. Wang, J. B. Johnson, and M. V. Fischetti, "Silicon CMOS devices beyond scaling," *IBM Journal of Research and Development*, vol. 50, no. 4.5, pp. 339–361, July/Sep. 2006.

[5] E. G. Larsson, O. Edfor, F. Tufvesson, and T. L. Marzetta, "Massive MIMO for next generation wireless systems," *IEEE Trans. Comm. Magazine*, vol. 52, no. 2, pp. 186–195, Feb 2014.

[6] A. Zanella, N. Bui, L. Vangelista, and M. Zorzi, "Internet of things for smart cities," *IEEE Internet of Things Journal*, vol. 1, no. 1, pp. 22–32, Feb 2014.

[7] Y. Cho and G. M. Rebeiz, "0.7−1.0-GHz reconfigurable bandpass-to-bandstop filter with selectable 2- and 4-pole responses," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 11, pp. 2626–2632, Nov 2014.

[8] D. Shin, C.-Y. Kim, D.-W. Kang, and G. M. Rebeiz, "A high-power packaged four-element X-band phased-array transmitter in 0.13-µm CMOS for radar and communication systems," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, pp. 3060–3071, Aug 2013.

[9] K.-J. Koh and G. M. Rebeiz, "An X- and Ku-band 8-element phased array receiver in 0.18-µm SiGe BiCMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 6, pp. 1360–1371, June 2008.

[10] B.-W. Min and G. M. Rebeiz, "Single-ended and differential Ka-band BiCMOS phased array front-ends," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 10, pp. 2239–2250, Oct 2008.

[11] T.-S. Chu, J. Roderick, and H. Hashemi, "An integrated ultra-wideband timed array receiver in 0.13 μm CMOS using a path-sharing true time delay architecture," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2834–2850, Oct 2007.

[12] D.-W. Kang, J.-G. Kim, B.-W. Min, and G. M. Rebeiz, "Single and four-element Ka-band transmit/receive phased-array silicon RFICs with 5-bit amplitude and phase control," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 3534–3543, Dec 2009.

[13] K. Grenier, D. Dubuc, P.-E. Poleni, M. Kumemura, H. Toshiyoshi, T. Fujii, and H. Fujita, "Integrated broadband microwave and microfluidic sensor dedicated to bioengineering," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 3246–3253, Dec 2009.

[14] T. Yilmaz, R. Foster, and Y. Hao, "Towards accurate dielectric property retrieval of biological tissues for blood glucose monitoring," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3193–3204, Dec 2014.

[15] K. Kim, N. Kim, S.-H. Hwang, Y.-K. Kim, and Y. Kwon, "A miniaturized broadband multi-state reflectometer integrated on a silicon MEMS probe for complex permittivity measurement of biological material," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 5, pp. 2205–2214, May 2013.

[16] T. Roberts and K. M. Noujeim, "A compact, tethered E-band VNA reflectometer," in *2016 IEEE MTT-S International Microwave Symposium (IMS), CA*, May 2016, pp. 1–3.

[17] K. Staszek, S. Gruszczynski, and K. Wincza, "Ultra-wideband dual-line multiprobe reflectometer," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 4, pp. 1324–1333, April 2017.

[18] M. A. Abou-Khousa, M. A. Baumgartner, S. Kharkovsky, and R. Zoughi, "Novel and simple high-frequency single-port vector network analyzer," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 3, pp. 534–542, May 2010.

[19] ——, "Ka-band vector reflectometer based on simple phase-shifter design," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 2, pp. 618–624, Feb. 2011.

[20] M. Fallahpour, M. A. Baumgartner, A. Kothari, M. T. Ghasr, D. Pommerenke, and R. Zoughi, "Compact Ka-band one-port vector reflectometer using a wideband electronically controlled phase shifter," *IEEE Trans. Instrum. Meas.*, vol. 61, no. 10, pp. 2807–2816, Oct. 2012.

[21] A. Grichener and G. M. Rebeiz, "A 15-50-GHz quasi-optical scalar network analyzer scalable to terahertz frequencies," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 8, pp. 2622–2633, Aug. 2012.

[22] A. Alazemi and G. M. Rebeiz, "A 100-300 GHz free-scale network analyzers using compact Tx and Rx modules," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 11, pp. 4021–4029, Nov. 2016.

[23] I. Nasr, J. Nehring, K. Aufinger, G. Fischer, R. Weigel, and D. Kissinger, "Single- and Dual-port 50-100-GHz integrated vector network analyzers with on-chip dielectric sensors," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 9, pp. 2168–2179, Sep. 2014.

[24] B.-H. Ku, H. Chung, and G. M. Rebeiz, "A 70-110 GHz single-chip SiGe reflectometer with integrated local oscillator quadrupler," in *IEEE MTT-S International Microwave Symposium (IMS), HI*, June 2017, pp. 980–982.

[25] J. Nehring, M. Dietz, K. Aufinger, G. Fischer, R. Weigel, and D. Kissinger, "A 4-32-GHz chip set for a highly integrated heterodyne two-port vector network analyzer," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 3, pp. 892–905, Mar. 2016.

[26] J. Nehring, M. Schütz, M. Dietz, I. Nasr, K. Aufinger, R. Weigel, and D. Kissinger, "Highly integrated 4-32-GHz two-port vector network analyzers for instrumentation and biomedical applications," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 1, pp. 229–244, Jan. 2017.

[27] H. Chung, Q. Ma, M. Sayginer, and G. M. Rebeiz, "A $0.01-26$ GHz single-chip SiGe reflectometer for two-port vector network analyzers," in *IEEE MTT-S International Microwave Symposium (IMS), HI*, June 2017, pp. 1259–1261.

[28] W. Shin, B.-H. Ku, O. Inac, Y.-C. Ou, and G. M. Rebeiz, "A $108-114$ GHz 4×4 wafer-scale phased array transmitter with high-efficiency on-chip antennas," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 9, pp. 2041–2055, Sep. 2013.

[29] E. R. Ethlers, C. Hutchinson, R. L. Rhymes, T. E. Shirley, and B. Y. Wong, "Integrated directional bridge," 2007. [Online]. Available: https://patents.google.com/patent/US7309994

[30] K. Komoni, S. Sonkusale, and G. Dawe, "Fundamental performance limits and scaling of a CMOS passive double-balanced mixer," in *2008 Joint 6th International IEEE Northeast Worksho on Circuits and Systems and TAISA Conference*, 2008, pp. 297–300.

[31] M. Sayginer and G. M. Rebeiz, "An eight-element 2-16-GHz programmable phased array receiver with one, two, or four Simultaneous beams in SiGe BiCMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4585–4597, Dec. 2016.

[32] D. M. Pozar, *Microwave Engnieering*. Wiley, 2005.

[33] N. Somjit, I. Robertson, and M. Chongcheawchamnan, *Microwave and millimeter-wave design for wireless communications*. Wiley, 2016.

[34] S. Rehnmark, "On the calibration process of automatic network analyzer systems," *IEEE Trans. Microw. Theory Techn.*, pp. 457–458, Apr. 1974.

[35] M. Hiebel, *Fundamentals of Vector Network Analyzer communications*. Rohde&Schwarz, 2011.

[36] A. Ferrero and F. Sanpietro, "A simplified algorithm for leaky network analyzer calibration," *IEEE Microwave and Guided Wave Letters*, pp. 119–121, Apr. 1995.

[37] H.-J. Eul and B. Schiek, "A generalized theory and new calibration procedures for network analyzer self-calibration," *IEEE Trans. Microw. Theory Techn.*, pp. 724–731, Apr. 1991.

[38] H. H. Meinel, "Commercial applications of millimeterwaves: history, present status, and future trends," *IEEE Trans. Microw. Theory Techn.*, vol. 43, no. 7, pp. 1639–1653, July 1995.

[39] B.-H. Ku, O. Inac, M. Chang, H.-H. Yang, and G. M. Rebeiz, "A High-linearity 76−85-GHz 16-element 8-transmit/8-receive phased-array chip with high isolation and flip-chip packaging," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 10, pp. 2337–2356, Oct. 2014.

[40] R. Feger, C. Wagner, S. Schuster, S. Scheiblhofer, H. Jäger, and A. Stelzer, "A 77-GHz FMCW MIMO radar based on an SiGe single-chip transceiver," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 5, pp. 1020–1035, May 2009.

[41] V. Jain, F. Tzeng, L. Zhou, and P. Heydari, "A single-chip dual-band 22-29-GHz/77-81-GHz BiCMOS transciever for automotive radars," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3469–3485, Dec. 2009.

[42] D. del Rio, I. Gurutzeaga, A. Rezola, J. F. Sevillano, I. Velez, S. E. Gunnarsson, N. Tamir, C. E. Saavedra, J. L. Gonzelez-Jimenez, A. Siligaris, C. Dehos, and R. Berenguer, "A wideband and high-linearity E-band transmitter integrated in a 55-nm SiGe technology for backhaul point-to-point 10-Gb/s link," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 8, pp. 2990–3001, Aug. 2017.

[43] A. Li, S. Zheng, X. Luo, and H. C. Luong, "A 21−48 GHz subharmonic injection-locked fractional-N frequency synthesizer for multiband point-to-point backhaul communications," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 8, pp. 1785–1799, Aug. 2014.

[44] A. Arbabian, S. Callender, S. Kang, B. Afshar, J. C. Cheien, and A. M. Niknejad, "A 90 GHz hybrid switching pulsed-transmitter for medical imaging," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2667–2681, Aug. 2010.

[45] M. Tiebout, H. D. Wohlmuth, H. Knapp, R. Salerno, M. Druml, J. Kaeferboeck, M. Rest, J. Wuertele, S. S. Ahmed, A. Schiessl, and R. Juenemann, "Low power wideband receiver and transmitter chipset for mm-wave imaging in SiGe bipolar technology," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 5, pp. 1175–1184, May 2012.

[46] Q. Ma, D. M. W. Leenaerts, and P. G. M. Baltus, "Silicon-based true-time-delay phased-array front-ends at Ka-band," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 9, pp. 2942–2952, Sep. 2015.

[47] H. Al-Rubaye and G. M. Rebeiz, "W-band direct-modulation $>$20-Gb/s transmit and receive building blocks in 32-nm SOI CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 9, pp. 2277–2291, Sep. 2017.

[48] Q. Ma, H. Chung, and G. M. Rebeiz, "A low EVM SiGe BiCMOS 40-100 GHz direct conversion IQ modulator for multi-Gbps communications systems," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2018, pp. 188–191.

[49] B. Sadhu, Y. Tousi, J. Hallin, S. Sahl, S. Reynolds, O. Renström, K. Sjögren, O. Haapalahti, N. Mazor, B. Bokinge, G. Weibull, H. Bengtsson, A. Carlinger, E. Westesson, J.-E. Thillberg, L. Rexberg, M. Yeck, X. Gu, D. Friedman, and A. Valdes-Garcia, "7.2 A 28GHz 32-element phased-array transceiver IC with concurrent dual polarized beams and 1.4 degree beam-steering resolution for 5G communication," in *IEEE International Solid State Circuits Conf. (ISSCC)*, Feb. 2017, pp. 128–129.

[50] K. Kibarloglu, M. Sayginer, and G. M. Rebeiz, "An ultra low-cost 32-element 28 GHz phased-array transceiver with 41 dBm EIRP and 1.0$-$1.6 Gbps 16-QAM link at 300 meters," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2018, pp. 73–76.

[51] H.-T. Kim, B.-S. Park, S.-M. Oh, S.-S. Song, J.-M. Kim, S.-H. Kim, T.-S. Moon, S.-Y. Kim, J.-Y. Chang, S.-W. Kim, W.-S. Kang, S.-Y. Jung, G.-Y. Tak, J.-K. Du, Y.-S. Suh, and Y.-C. Ho, "A 28GHz CMOS direct conversion transceiver with packaged antenna arrays for 5G cellular system," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2018, pp. 69–72.

[52] D. Murphy, Q. J. Gu, Y.-C. Wu, H.-Y. Jian, Z. Xu, A. Tang, F. Wang, and M. C. F. Chang, "W-band direct-modulation $>$20-Gb/s transmit and receive building blocks in 32-nm SOI CMOS," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1606–1617, July 2011.

[53] S. Kang, J.-C. Chien, and A. M. Niknejad, "A W-band low-noise PLL with a fundamental VCO in SiGe for millimeter-wave applications," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 10, pp. 2390–2404, Oct. 2014.

[54] S. Shahramian, A. Hart, A. Tomkins, A. C. Carusone, P. Garcia, P. Chevalier, and S. P. Voinigescu, "Design of a dual W- and D-band PLL," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 1011–1022, May 2011.

[55] E. Socher and S. Jameson, "Wideband tuning range W-band colpitts VCO in 90 nm CMOS," *Electron. Lett.*, vol. 47, no. 22, pp. 1227–1229, Oct. 2011.

[56] C. Jany, A. Siligaris, J. L. Gonzalez-Jimenex, P. Vincent, and P. Ferrari, "A programmable frequency multiplier-by-29 architecture for millimeter wave applications," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 7, pp. 1669–1679, July 2015.

[57] D. Shin, S. Raman, and K.-J. Koh, "7.2 A 28GHz 32-element phased-array transceiver IC with concurrent dual polarized beams and 1.4 degree beam-steering resolution for 5G communication," in *IEEE International Solid State Circuits Conf. (ISSCC)*, Feb. 2016, pp. 50–51.

[58] W. Deng, T. Siriburanon, A. Musa, K. Okada, and A. Matsuzawa, "A sub-harmonic injection-locked quadrature frequency synthesizer with frequency calibration scheme for millimeter-wave TDD transceivers," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 7, pp. 1710–1720, July 2013.

[59] L. E. Milner, J. T. Harvey, M. E. Parker, L. T. Hall, M. C. Rodriguez, M. C. Heimlich, and S. J. Mahon, "A 25 to 45 GHz SiGe receiver MMIC sub-harmonic injection-locked quadrature frequency synthesizer with frequency calibration scheme for millimeter-wave TDD transceivers," in *European Microwave Integrated Circuits Conference (EuMIC)*, Sep. 2016, pp. 548–551.

[60] D. M. Sheen, J. L. Fernandes, J. R. Tedeschi, D. L. McMakin, A. M. Jones, W. M. Lechelt, and R. H. Severtsen, "Wide-bandwidth, wide-beamwidth, high-resolution, millimeter-wave imaging for concealed weapon detection," in *SPIE Defense, Security, and Sensing*, 2013.

[61] J. L. Fernandes, J. R. Tedeschi, D. M. Sheen, and D. L. McMakin, "Three-dimensional millimeter-wave imaging for concealed threat detection in shoes," in *Proc. SPIE 8715, Passive and Active Millimeter-Wave Imaging XVI*, May 2013.

[62] N.-C. Kuo, Z.-M. Tsai, K. Schmalz, J. C. Scheytt, and H. Wang, "Frequency Quadruplers for a 77 GHz subharmonically pumped automotive radar transceiver in SiGe," in *Erupoean Microwave Integrated Circuits Conf.(EMIC), France*, Sep. 2010, pp. 365–368.

[63] G.-Y. Chen, H.-Y. Chang, S.-H. Weng, C.-C. Shen, Y.-L. Yeh, J.-S. Fu, Y.-M. Hsin, and Y.-C. Wang, "Design and analysis of a Ka-band monolithic high-efficiency frequency quadrupler using GaAs HBT-HEMT common-base/common-source balanced topology," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 10, pp. 3674–3689, Oct. 2013.

[64] S. Chakraborty, L. E. Milner, X. Zhu, L. T. Hall, O. Sevimli, and M. C. Heimlich, "A K-band frequency doubler with 35-dB fundamental rejection based on novel transformer balun in 0.13-µm SiGe technology," *IEEE Electron Devices Letter*, vol. 37, no. 11, pp. 1375–1378, Nov. 2016.

[65] J.-J. Hung, T. M. Hancock, and G. M. Rebeiz, "High-power high-efficiency SiGe Ku- and Ka-band balanced frequency doublers," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 2, pp. 754–761, Feb. 2005.

[66] B. Cetinoneri, Y. A. Atesal, A. Fung, and G. M. Rebeiz, "W-band amplifiers with 6-dB noise figure and milliwatt-level 170-200-GHz doublers in 45-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 692–701, Mar. 2012.

[67] N. Mazor, O. Katz, B. Sheinman, R. Carmon, R. Ben-Yishay, R. Levinger, A. Bruetbart, and D. Elad, "A SiGe V-band x8 frequency multiplier with high spectral purity," in *European Microwave Integrated Circuits Conference (EuMIC)*, Sep. 2015, pp. 77–80.

[68] Sonnet. ver. 16.52, Sonnet Software Inc., Syracuse, NY, USA, 2011.

[69] K. T. Ng, B. Rejaie, and J. N. Burghartz, "Substrate effects in monolithic RF transformers on silicon," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 1, pp. 377–383, Jan. 2002.

[70] GF8HP model guide, Globalfoundries. Inc., Milpitas, CA, USA.

[71] Advanced Device System, Keysight Technologies Inc., Santa Rosa, CA, USA, 2014.

[72] H. Chung, Q. Ma, and G. M. Rebeiz, "A 10-40 GHz frequency quadrupler source with switchable bandpass filters and > 30 dBc harmonic rejection," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2017, pp. 49–52.

[73] Q. Ma, H. Chung, and G. M. Rebeiz, "A 4-channel 10-40 GHz wideband receiver with integrated frequency quadrupler for high resolution millimeter-wave imaging systems," in *IEEE MTT-S International Microwave Symposium (IMS), PA*, June 2018, pp. 883–886.

[74] J.-S. Kim, H.-M. Oh, C. W. Byeon, J. H. Son, J. H. Lee, J. Lee, and C.-Y. Kim, "V-band $\times 8$ frequency multiplier with optimized structure and high spectral purity using 65-nm CMOS process," *IEEE Microw. Wireless Compon. Lett. (MWCL)*, vol. 27, no. 5, pp. 506–508, May 2017.

[75] Y.-S. Yeh and B. A. Floyd, "A 55-GHz power-efficient frequency quadrupler with high harmonic rejection in 0.1-µm SiGe BiCMOS technology," in *IEEE Radio Frequency Integrated Circuits Symp. (RFIC), AZ*, May 2015, pp. 267–270.

[76] N. Mazor, O. Katz, B. Sheinman, R. Carmon, R. Ben-Yishay, R. Levinger, A. Bruetbart, and D. Elad, "A high suppression frequency tripler for 60-GHz transceivers," in *IEEE MTT-S International Microwave Symposium (IMS), AZ*, May 2015, pp. 1–3.

[77] S. Yuan and H. Schumacher, "Novel frequency quadrupler design covering the entire V-band in 0.13-µm SiGe process," in *IEEE Silicon Monolithic Integrated Circuits in RF System (SiRF), CA*, Jan. 2014, pp. 101–103.

[78] J.-C. Chien, P. Upadhyaya, H. Jung, S. Chen, W. Fang, and A. M. Niknejad, "A pulse-position-modulation phase-noise-reduction technique for a 2-to-16 GHz injection-locked ring oscillator in 20 nm CMOS," in *IEEE International Solid State Circuits Conf. (ISSCC)*, Feb. 2014, pp. 52–53.

[79] M. K. amd S. Choi, T. Seong, and J. Choi, "A low-jitter and fractional resolution injection-locked clock multiplier using a DLL-based real-time PVT calibrator with replica-delay cells," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 2, pp. 401–411, Feb. 2016.

[80] A. Elkholy, M. Talegaonkar, T. Anand, and P. K. Hanumolu, "A 6.75-to-8.25 GHz 2.25 mW 190 fsrms integrated jitter PVT-insensitive injection-locked clock multiplier using all-digital continuous frequency-tracking loop in 65 nm CMOS," in *IEEE International Solid State Circuits Conf. (ISSCC)*, Feb. 2015, pp. 1–3.

[81] J. D. Cali, C. M. Grens, S. E. Turner, D. S. Jansen, and L. J. Kushner, "20-GHz PLL-based configurable frequency generator in 180 nm SiGe-on-SOI BiCOMS," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC), AZ*, May 2015, pp. 401–404.

[82] M. Ferriss, J.-O. Plouchart, A. Natarajan, A. Rylyakov, B. Parker, J. A. Tierno, A. Babakhani, S. Yaldiz, A. Valdes-Garcia, B. Sadhu, and D. J. Friedman, "An integral path self-calibration scheme for a dual-loop PLL," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 4, pp. 996–1008, Apr. 2013.

[83] Z.-Z. Chen, Y.-H. Wang, J. Shin, Y. Zhao, S. A. Mirhaj, Y.-C. Kuan, H.-N. Chen, C.-P. Jou, M.-H. Tsai, F.-L. Hsueh, and M.-C. F. Chang, "A sub-sampling all-digital fractional N-frequency synthesizer with -111dBc/Hz in-band phase noise and an FOM of -242 dB," in *IEEE International Solid State Circuits Conf. (ISSCC)*, Feb. 2015, pp. 268–269.

[84] X. Gao, O. Burg, H. Wang, W. Wu, C.-T. Tu, K. Manetakis, F. Zhang, L. Tee, M. Yayla, S. Xiang, R. Tsang, and L. Lin, "A 2.7-to-4.3 GHz, 0.16psrms-jitter, -246.8 dB-FOM, digital fractional-N sampling PLL in 28 nm CMOS," in *IEEE International Solid State Circuits Conf. (ISSCC)*, Feb. 2016, pp. 174–175.

[85] E. Temporiti, G. Albasini, I. Bietti, R. Castello, and M. Colombo, "A 700-kHz bandwidth ΣΔ fractional synthesizer with spurs compensation and linearization techniques for WCDMA applications," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 9, pp. 1446–1454, Sep. 2004.

[86] Analog Device Inc. "Microwave wideband synthesizer with integrated VCO", datasheet ADF5356, Oct, 2017. .

[87] S. Zihir, O. D. Gurbuz, A. Kar-Roy, S. Raman, and G. M. Rebeiz, "60-GHz 64- and 256-elements wafer-scale phased-array transmitter using full-reticle and subretical stitching techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4701–4719, Dec. 2016.

[88] S. Y. Kim, O. Inac, C.-Y. Kim, D. Shin, and G. M. Rebeiz, "A 76—84 GHz 16-element phased-array receiver with a chip-level built-in self-test system," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, pp. 3083–3098, Aug. 2013.

[89] F. Golcuk, T. Kanar, and G. M. Rebeiz, "A 90 - 100-GHz 4 x 4 SiGe BiCMOS Polarimetric Transmit/Receive Phased Array With Simultaneous Receive-Beams Capabilities," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, pp. 3099–3114, Aug. 2013.

[90] J. May and G. M. Rebeiz, "Design and characterization of W-band SiGe RFICs for passive millimeter-wave imaging," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 3, pp. 1420–1430, May 2010.

[91] J. G. Andrews, S. Buzzi, W. Choi, S. V. Hanly, A. Lozano, A. C. K. Soong, and J. C. Zhang, "What will 5G be?" *IEEE Journal on Selected Areas in Communications*, vol. 32, no. 6, pp. 1065–1081, June 2014.

[92] A. Arbabian, S. Callender, S. Kang, B. Afshar, and J.-C. Chein, "A 90 GHz hybrid switching pulsed-transmitter for medical imaging," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2667–2681, Dec. 2010.

[93] C.-C. Wang, Z. Chen, and P. Heydari, "W-band silicon-based frequency synthesizers using injection-locked and harmonic triplers," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 5, pp. 1307–1320, May 2012.

[94] Z. Chen and P. Heydari, "An 85−95.2 GHz transformer-based injection-locked frequency tripler in 65 nm CMOS," in *IEEE MTT-S International Microwave Symposium (IMS), CA*, May 2010, pp. 776–779.

[95] H.-C. Lin and G. M. Rebeiz, "A SiGe Multiplier Array With Output Power of 5-8 dBm at 200-230 GHz," *IEEE Trans. Microw. Theory Techn.*, vol. 52, no. 3, pp. 993–1000, July 2016.

[96] A. Bossuet, T. Quemerais, S. Lepilliet, J.-H. Fournier, E. Lauga-Larroze, C. Gaquiere, and D. Gloria, "A 135-150 GHz frequency quadrupler with 0.5 dBm peak output power in 55 nm SiGe BiCMOS technology," in *IEEE Biploar/BiCMOS Circuits and Tech. Meeting. (BCTM), MA*, Oct. 2015, pp. 186–189.

[97] Y. Wang, W. Goh, and Y.-Z. Xiong, "A 9 % power efficiency 121-to-137 GHz phase-controlled push-push frequency quadurpler in 0.13 µm SiGe BiCMOS," in *IEEE International Solid State Circuits Conf. (ISSCC)*, Feb. 2012, pp. 262–264.

[98] L. Wang, Y.-Z. Xiong, B. Zhang, S.-M. Hu, and T.-G. Lim, "Millimeter-Wave frequency doubler with transistor ground-shielding structure in 0.13 µm SiGe BiCMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 5, pp. 1304–1310, May 2011.

[99] Y. Li, G. Wang-Ling, and Y.-Z. Xiong, "A 124 to 132.5 GHz frequency quadrupler with 4.4 dBm output power in 0.13 µm SiGe BiCMOS," in *IEEE European Solid State Circuits Conf. (ESSCIRC)*, Sep. 2015, pp. 132–135.

[100] S. Kueppers, K. Aufinger, and N. Pohl, "A fully differential 100−140 GHz frequency quadrupler in a 130 nm SiGe:C technology for MIMO radar applications using the bootstrapped Gilbert-cell doubler topology," in *IEEE Silicon Monolithic Integrated Circuits in RF System (SiRF)*, Jan. 2017, pp. 37–39.

[101] V. Valenta, S. Yuan, A. Trasser, and H. Schumacher, "F-band frequency octupler in 0.13-µm SiGe:C BiCMOS with 2 mW output power," in *IEEE MTT-S International Microwave Symposium (IMS), WA*, June 2013, pp. 1–3.

[102] V. Valenta, A. C. Ulusoy, A. Trasser, and H. Schumacher, "Wideband 110 GHz frequency quadrupler for an FMCW imager in 0.13-µm SiGe:C BiCMOS process," in *IEEE Silicon Monolithic Integrated Circuits in RF System (SiRF), TX*, Jan. 2013, pp. 9–11.

[103] G. Liu, J. Jaymon, J. Buckwalter, and P. Asbeck, "Frequency doublers with 10.2/5.2 dBm peak power at 100/202 GHz in 45 nm SOI CMOS," in *IEEE Radio Frequency Integrated Circuits Symp. (RFIC), AZ*, May 2015, pp. 271–274.

[104] N. Mazor and E. Socher, "Analysis and design of an X-Band-to-W-Band CMOS millimeter-wave active multiplier with improved harmonic rejection," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 5, pp. 1924–1933, May 2013.

[105] H. P. Forstner, F. Starzer, G. Haider, C. Wagner, and M. Jahn, "Frequency Quadruplers for a 77 GHz subharmonically pumped automotive radar transceiver in SiGe," in *Erupoean Microwave Integrated Circuits Conf.(EMIC), Italy*, Sep. 2009, pp. 188–191.

[106] J. Long, "Monolithic transformer for silicon RF IC design," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.

[107] F. Ahmed, M. Furqan, B. Heinemann, and A. Stelzer, "A SiGe-based broadband 140—170 GHz downconverter for high resolution FMCW radar applications," in *2016 IEEE International Conference on Microwaves for Intelligent Mobility (ICMIM), San Diego, CA*, 2016, pp. 1–4.

[108] W. H. Lin, H. Y. Yang, J. H. Tsai, T. W. Huang, and H. Wang, "1024-QAM High Image Rejection *E*-Band Sub-Harmonic IQ Modulator and Transmitter in 65-nm CMOS Process," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 11, pp. 3974–3985, Nov. 2013.

[109] S. Shahramian, Y. Baeyens, N. Kaneda, and Y. K. Chen, "A 70-100 GHz Direct-Conversion Transmitter and Receiver Phased Array Chipset Demonstrating 10 Gb/s Wireless Link," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 5, pp. 1113–1125, May 2013.

[110] D. Zhao and P. Reynaert, "A 40 nm CMOS E-Band Transmitter With Compact and Symmetrical Layout Floor-Plans," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 11, pp. 2560–2571, Nov. 2015.

[111] J. Kaukovuori, K. Stadius, J. Ryynanen, and K. A. I. Halonen, "Analysis and Design of Passive Polyphase Filters," *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 55, no. 10, pp. 3023–3037, Nov. 2008.

[112] Z.-M. Tsai, H.-C. Liao, Y.-H. Hsiao, and H. Wang, "V-Band High Data-Rate I/Q Modulator and Demodulator With a Power-Locked Loop LO Source in 0.15-/spl mu/m GaAs pHEMT Technology," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 7, pp. 2670–2684, July 2013.

[113] Y. T. Chou, Y. H. Lin, and H. Wang, "A high image rejection E-band sub-harmonic IQ demodulator with low power consumption in 90-nm CMOS process," in *2016 46th European Microwave Conference (EuMC), London*, June 2016, pp. 1417–1420.