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### Authors

Wang, Pin J.  
Kim, Jong S.  
Lee, Chin C.

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# Fluxless Bonding of Large Silicon Chips to Ceramic Packages Using Electroplated Eutectic Au/Sn/Au Structures

PIN J. WANG,<sup>1</sup> JONG S. KIM,<sup>1,2</sup> and CHIN C. LEE<sup>1,3</sup>

1.—Electrical Engineering and Computer Science, Materials and Manufacturing Technology, University of California, Irvine, Irvine, CA 92697-2660, USA. 2.—Present address: Applied Materials, Santa Clara, CA, USA. 3.—e-mail: clee@uci.edu

A fluxless process of bonding large silicon chips to ceramic packages has been developed using a Au-Sn eutectic solder. The solder was initially electroplated in the form of a Au/Sn/Au multilayer structure on a ceramic package and reflowed at 430°C for 10 min to achieve a uniform eutectic 80Au-20Sn composition. A 9 mm × 9 mm silicon chip deposited with Cr/Au dual layers was then bonded to the ceramic package at 320°C for 3 min. The reflow and bonding processes were performed in a 50-mTorr vacuum to suppress oxidation. Therefore, no flux was used. Even without any flux, high-quality joints were produced. Microstructure and composition of the joints were studied using scanning electron microscopy with energy-dispersive x-ray spectroscopy. Scanning acoustic microscopy was used to verify the joint quality over the entire bonding area. To employ the x-ray diffraction method, samples were made by reflowing the Au/Sn/Au structure plated on a package. This was followed by a bonding process, without a Si chip, so that x-rays could scan the solder surface. Joints exhibited a typical eutectic structure and consisted of (Au,Ni)Sn and (Au,Ni)<sub>5</sub>Sn phases. This novel fluxless bonding method can be applied to packaging of a variety of devices on ceramic packages. Its fluxless nature is particularly valuable for packaging devices that cannot be exposed to flux such as sensors, optical devices, medical devices, and laser diodes.

**Key words:** Indexing terms, fluxless bonding, fluxless soldering, AuSn solders, die attachment, ceramic package

## INTRODUCTION

Despite the popularity of plastic packages, ceramic packages are still being used in high-reliability applications and in high-power electronics.<sup>1-3</sup> Ceramic packages provide semiconductor chips with mechanical support, heat dissipation, and environmental protection. To make joints between chips and packages, silver-filled epoxy, glass, and solders are common bonding materials used in industries.<sup>4</sup> Silver epoxy is cheap and can be operated at low temperature, but it has low thermal and electrical conductivities and may cause outgassing.<sup>5</sup> Glass has excellent thermal stability. Glass joints,

however, break easily between bonded objects with different coefficients of thermal expansion (CTE) because glass is brittle and barely deforms under stress.

In this research, 80Au-20Sn eutectic solder was chosen to bond Si chips and alumina packages due to its high strength, resistance to thermal fatigue and creep, and desirable melting temperature (278°C). To fabricate the eutectic 80Au-20Sn alloy, a Au/Sn/Au three-layered structure was electroplated sequentially on the ceramic package, followed by an initial reflow process. Compared with other solder fabrication methods, i.e., vacuum deposition and preform rolling, the electroplating method is less costly and can easily produce layers thicker than 10 μm. It is also possible to achieve fluxless bonding using the electroplating process. Flux or scrubbing

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action is known to cause voids and uneven thickness in joints.<sup>6</sup>

After the 80Au-20Sn solder was produced, the Si chip was bonded onto the ceramic packages without using any flux. The reaction kinetics of producing the 80Au-20Sn alloy by reflowing the electroplated Au/Sn/Au structure had been investigated.<sup>7</sup> The microstructure of Au-Sn eutectic solder bumps fabricated by plating and reflow processes had been studied.<sup>8</sup> In this research, we focused on producing high-quality Au-Sn eutectic joints between large Si chips and ceramic packages using electroplated Au/Sn/Au layers. Commercial ceramic packages have a wide thickness variation on the outer Ni/Au layers, which affects joint formation and microstructure. The design of the Au/Sn/Au structure thus needs to consider this thickness uncertainty. The resulting joint has to be strong enough to sustain the thermal expansion mismatch between Si and ceramic. In what follows, the experimental design and procedures are first presented, followed by results and discussion. Finally, a short summary is given.

## EXPERIMENTAL PROCEDURES

Gyroscope microelectromechanical systems (MEMS) sensors employed in this study were built on 4-inch silicon-on-insulator (SOI) wafers. The base (handle) wafer of the SOI is 500  $\mu\text{m}$  in thickness. After the sensors were fabricated, the SOI wafers were diced into 9 mm  $\times$  9 mm chips, then deposited with a 0.03  $\mu\text{m}$  Cr layer and a 0.1  $\mu\text{m}$  Au layer on the backside of the chips in a high vacuum ( $2 \times 10^{-6}$  torr) E-beam evaporation system. The Cr layer acted as an adhesion layer and the Au layer protected the Cr layer from oxidation.

Side-brazed dual-in-line ceramic packages were purchased from a package vendor. Based on the specifications, the die-attach pad on the package has a metallic structure of W/Ni/Au. The thickness ranges of the Ni layer and Au layer vary from 2.5  $\mu\text{m}$  to 9  $\mu\text{m}$  and from 1.5  $\mu\text{m}$  to 5.7  $\mu\text{m}$ , respectively. The large thickness uncertainty on these metal layers makes this project difficult. However, all commercial ceramic packages have large uncertainty in the Ni/Au layer thickness. The bonding experiment was thus designed to overcome potential problems associated with this uncertainty. The goal was to demonstrate the feasibility of using the electroplated Au/Sn/Au multilayer structure to bond large Si chips to commercial ceramic packages that have large uncertainty in the Ni and Au thickness. The process also had to be entirely fluxless.

To fabricate the 80Au-20Sn eutectic solder, an 11  $\mu\text{m}$  gold layer was first electroplated on the die-attach pad. The Au plating bath was neutral non-cyanide plating solution at pH 7 based on a sulfite complex with mild agitation. The current density and process temperature were 4.6  $\text{mA}/\text{cm}^2$  and 60°C, respectively. This was followed by 7.5  $\mu\text{m}$  of tin, plated in a stannous Sn-based bath at a current

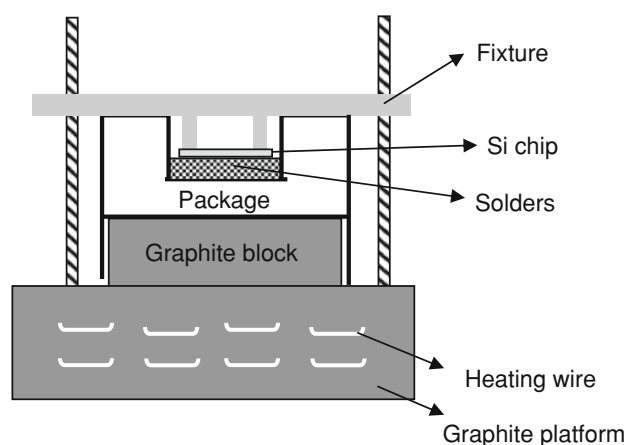


Fig. 1. Cross-sectional sketch of the bonding assembly. A special fixture holds the chip on the edges to apply slight pressure.

density of 21.5  $\text{mA}/\text{cm}^2$  for 30 min. The temperature and pH were 43°C and 1, respectively. Immediately after this, a thin Au film was plated over the Sn for 1 min, with an expected thickness of 0.1  $\mu\text{m}$ . Prior to the final Au plating process, the sample was soaked in 25% sulfuric acid for 30 s to reduce or remove possible oxide layers on the Sn layer. This thin outer Au layer reacted with Sn atoms and formed  $\text{AuSn}_4$  intermetallic compounds as soon as it was plated.<sup>9</sup> It was this thin  $\text{AuSn}_4$  layer that protected the inner Sn from oxidation when the sample was exposed to air. Oxidation prevention is an essential requirement to realize fluxless bonding technology.<sup>10-12</sup> The total amount of plated Au and Sn atoms, if mixed uniformly, will give the 80Au-20Sn eutectic composition. The resulting ceramic package with alumina/W/Ni/Au/Au (plated)/Sn (plated)/Au (plated) structure was mounted on a heater graphite platform in a 50-mTorr vacuum oven to suppress oxidation during the reflow process.<sup>13</sup> The initial reflow was performed at 430°C with a reflow time of 10 min. After the reflow process was finished, the ceramic package was allowed to cool naturally to room temperature in the vacuum environment.

The SOI chip with the Cr/Au structure and the ceramic package with the alumina/W/Ni/80Au-20Sn structure were held together by a fixture with a static pressure of 0.26 psi to ensure intimate contact. A cross-sectional sketch of the assembly is depicted in Fig. 1. The SOI chip was designed to have a 750- $\mu\text{m}$ -wide band on each side so that the fixture could contact these bands and apply slight pressure without touching the active region of the sensor. The fluxless bonding was carried out at 320°C, a typical process temperature for the 80Au-20Sn eutectic, with a dwell time of 3 min at a 50-mTorr vacuum. To evaluate joint quality, scanning acoustic microscopy (SAM) was used. The microstructure and composition of joints were observed under scanning electron microscopy with energy-dispersive x-ray spectroscopy (EDX). The etchant 95%  $\text{C}_2\text{H}_5\text{OH}$ :4%  $\text{HNO}_3$ :1%  $\text{HCl}$  was

employed to enhance the visibility of the microstructure. The  $\theta-2\theta$  x-ray diffraction (XRD) method was utilized for phase identification. To have access to the solder surface, samples of ceramic packages plated with the Au/Sn/Au structure were reflowed at 430°C for 10 min, followed by the bonding process at 320°C for 3 min, but without a Si chip. The resulting phases of the solder produced in this way were expected to be nearly the same as those of the solder joint with the Si chip present. This is a reasonable expectation because the only layer on the chip that will react with the molten solder is the 0.1  $\mu\text{m}$  of Au.

## RESULTS AND DISCUSSION

Figure 2 shows the image of a working chip attached to the pad of a ceramic package. The Si chip is still well attached after wire bonding. No cracks are observed. Several samples were examined by transmission scanning acoustic microscopy (TSAM). On the TSAM images, dark regions represent voids, cracks, delamination or contamination; light gray regions show variation in solder thickness and microstructure; and white regions indicate nearly perfect joints. Figure 3 shows a TSAM image of a typical die-attached package. Approximately 60% of the area is perfectly bonded while the remaining 40% of the area shows thickness and microstructure variations. The attached SOI chip was tested in bonding strength with a hand tool but the Si chip always broke first. This indicates that the bonding strength was high enough for real applications. Due to the CTE

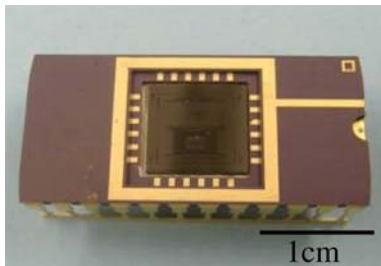


Fig. 2. Photograph of a working chip attached to a ceramic package.

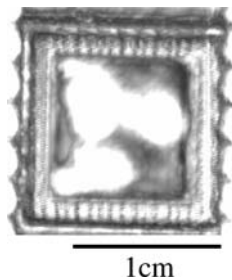


Fig. 3. TSAM image of a ceramic package attached with a 9 mm  $\times$  9 mm SOI chip using 80Au-20Sn, showing that 60% of the pad region is perfectly bonded while the remaining 40% has variation in thickness and microstructure.

mismatch between the Si chip and the ceramic package, the joint must have high quality to withstand shear stresses.

Figure 4 shows back-scattered electron (BSE) images of the cross-section of the sample that was reflowed at 430°C, followed by bonding at 320°C. Perfect bonding is achieved on most of the cross-section. The joint thickness is approximately 60  $\mu\text{m}$  and the thickness of the remaining Ni layer is about 4  $\mu\text{m}$ . Two regions, dark and bright, are observed. The dark region tends to aggregate next to the Ni layer. Global and local compositions were detected using EDX, as presented in Table I. The results indicate that the global composition consists of 65 at.% Au, 31 at.% Sn, and 3 at.% Ni. According to the isothermal section of the Au-Ni-Sn ternary system at room temperature shown in Fig. 5,<sup>14</sup>

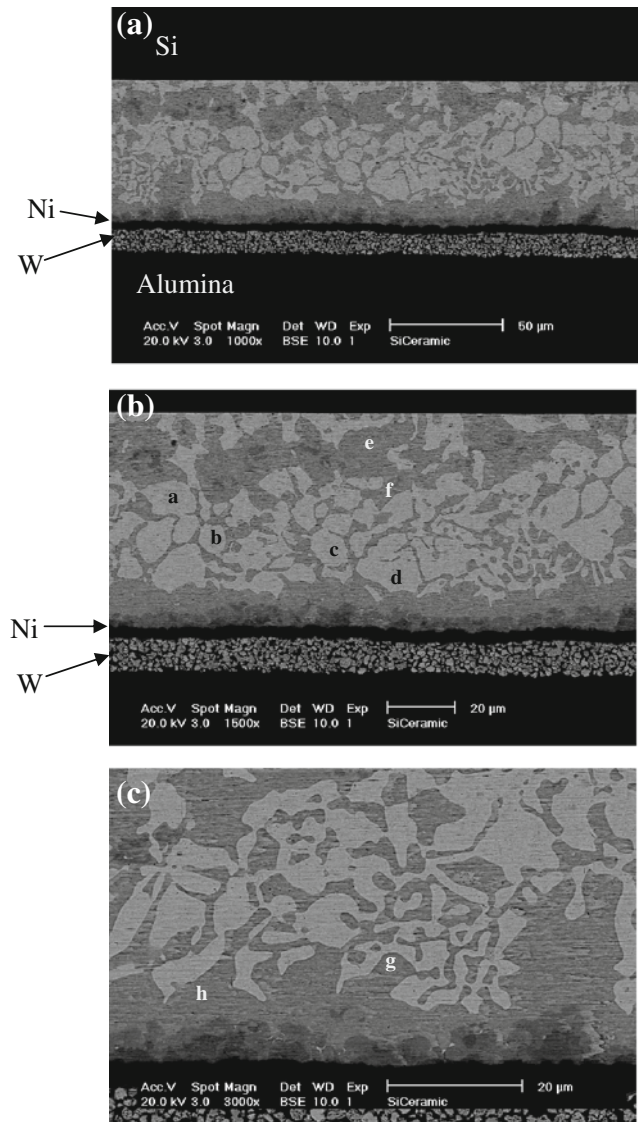


Fig. 4. BSE images of the joint: (a) low-magnification image showing perfect joints over the entire bonding interface, and (b, c) high-magnification image shows a eutectic structure. EDX compositions over the entire cross-section and on eight spots are given in Table I.



**Table I. EDX Results on the Cross-Section of the Joint Shown in Fig. 4b and c. The Composition is Expressed in at.%**

	Ni	Au	Sn
<i>Global</i>	3.8	65.1	31.1
<i>Bright region</i>			
a	3.8	90.2	3.2
b	3.2	91.7	5.2
c	6.2	87.7	6.0
d	2.9	91.8	5.4
<i>Dark region</i>			
e	15.0	57.1	27.9
f	15.0	52.3	32.7
g	16.2	50.5	33.3
h	16.5	52.1	31.4

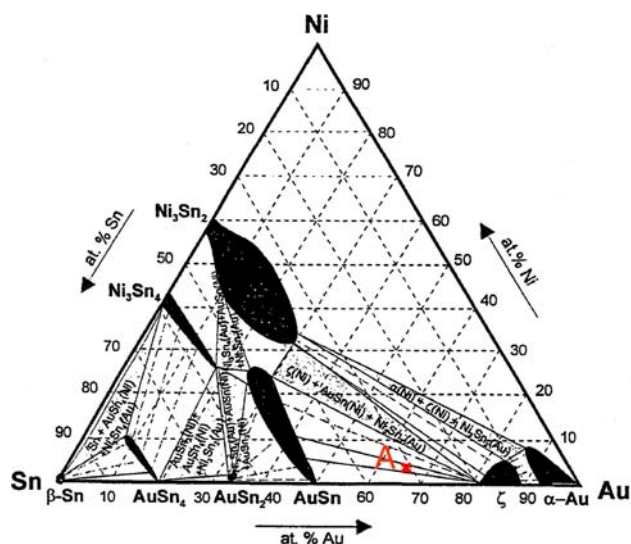


Fig. 5. Isothermal section of the Au-Ni-Sn ternary system at room temperature (Copyright 1998 IEEE).<sup>14</sup>

this global composition falls at point A, which is comprised of the two phases (Au,Ni)Sn and (Au,Ni)<sub>5</sub>Sn. The local compositions at eight spots, marked a, b, c, and d on the bright region, and e, f, g, and h on the dark region, were also detected. It was observed that a certain amount of Ni atoms diffuse into the 80Au-20Sn eutectic solder, especially in the dark region. The bright region has a Au-rich composition of 87 at.% to 91 at.% Au with 6 at.% Sn and a small amount of Ni, corresponding to the (Au) solid solution and the (Au,Ni)<sub>5</sub>Sn phase. The dark region consists of 50 at.% to 57 at.% Au, 27 at.% to 33 at.% Sn, and 15 at.% to 16 at.% Ni. It probably consists of (Au,Ni)Sn, (Au,Ni)<sub>5</sub>Sn, and (Ni,Au)<sub>3</sub>Sn<sub>2</sub> phases. Because the depth of the interaction volume of beam electrons in the Au-Sn alloy is approximately 1.5 μm to 2 μm, which is larger than the width of some dark phases, the EDX composition analysis might not be accurate here. In fact, when the dark region was magnified, various gray levels showed up. These varying gray levels might indicate these different phases.

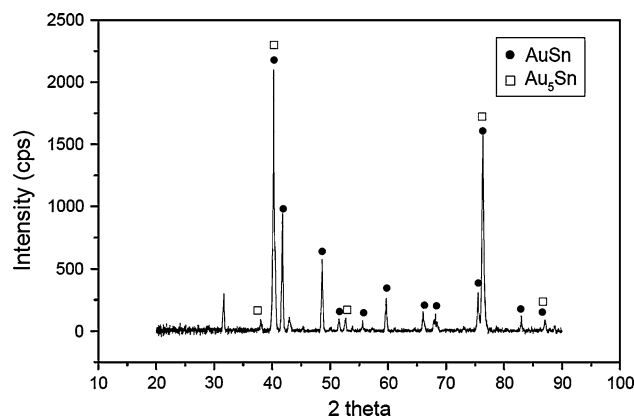


Fig. 6. XRD spectra from the Au-Sn alloy on the pad region of a ceramic package that has been reflowed at 430°C and 320°C sequentially.

To determine the phases of the solder joint, the XRD method was performed on the sample that had gone through two subsequent reflow processes at 430°C and 320°C, respectively, without a chip, as explained in the section “Experimental Procedures.” Figure 6 presents the XRD pattern. Several strong peaks associated with AuSn and Au<sub>5</sub>Sn phases appear. On the other hand, phases corresponding to peaks at 31.64° and 43.00° cannot be identified. Since the (Au) solid solution and the (Ni,Au)<sub>3</sub>Sn<sub>2</sub> phase are not detected in the XRD pattern, the bright region and the dark region in Fig. 4 should represent the (Au,Ni)<sub>5</sub>Sn phase and a mixture of (Au,Ni)<sub>5</sub>Sn and (Au,Ni)Sn phases, respectively. This microstructure differs from that of the 80Au-20Sn eutectic, where the bright region corresponds to the Au<sub>5</sub>Sn phase and the dark region is the AuSn phase. The phenomenon of the dark region containing both Au<sub>5</sub>Sn and AuSn phases has been also observed in Ref. 7.

In the present design, the plated Au/Sn/Au multilayer structure reacted completely during reflow and bonding to form a molten phase which further reacted with the outer Au layer on the pad of the ceramic package. BSE images of the resulting joint (Fig. 4) show that the pure Au layer does not exist anymore. Thus, the Au layer originally on the ceramic package has reacted completely and become a part of the Au-Sn alloy joint. During reflow and bonding, the underlying Ni layer was thus exposed to the molten phase. Upon cooling to room temperature, it was found that a significant amount of Ni atoms had diffused into the Au-Sn alloy joint. This observation is consistent with the microstructure results of reflowing a Ni/Au/Sn structure at 290°C.<sup>15,16</sup> While the eutectic microstructure and evolution of the plated Au/Sn on Ni after reflow were already investigated in Refs. 15 and 16, our research focus was to bond large Si chips to commercial ceramic packages without using any flux. The results show that nearly perfect joints were

achieved. The joint exhibits a Au-Sn eutectic-like microstructure with Ni. Regardless of the large CTE mismatch between Si chips and alumina packages, the joint is strong enough to withstand the stress developed.

When Ni atoms dissolved in the 80Au-20Sn eutectic alloy, (Au,Ni)Sn and (Au, Ni)<sub>5</sub>Sn phases were formed. At present, quantitative data are not available to evaluate the composition of Ni in (Au,Ni)Sn and (Au,Ni)<sub>5</sub>Sn ternary compounds. The existence of the Ni<sub>3</sub>Sn<sub>2</sub> phase and the (Au) solid solution needs to be further confirmed because they were not detected in the XRD analysis.

### REFLOW AND BONDING MECHANISM

Based on the discussion above, the reflow and bonding mechanism is now presented. Figure 7a shows the electroplated ceramic package with the alumina/W/Ni/Au/Au (plated)/Sn (plated)/Au (plated) structure. As the temperature increases, the Sn layer starts to melt at 231°C. The molten phase (*L*) dissolves AuSn<sub>4</sub> compounds on the surface and reacts with the underlying Au atoms through liquid–solid interactions. When the temperature reaches the 430°C reflow temperature, the (*L*) phase dissolves all Au-Sn compounds, including AuSn<sub>4</sub>, AuSn<sub>2</sub>, and AuSn, because the reflow temperature is higher than the melting temperatures of these three compounds: AuSn (419°C), AuSn<sub>2</sub> (309°C), and AuSn<sub>4</sub> (252°C).<sup>17</sup> The homogeneous eutectic 80Au-20Sn alloy, with a melting temperature of 280°C, is formed after the initial reflow, as depicted in Fig. 7b. The SOI chip deposited with Cr/Au layers is then bonded to the ceramic package at 320°C. The solder melts and turns into a molten phase, which dissolves the thin Au layer on the SOI chip and thus directly contacts the Cr layer on the SOI chip, as illustrated in Fig. 7c. On cooling to room temperature, the solder solidifies and the joint is achieved.

To avoid any degradation of SOI chips caused by a high bonding temperature, an initial reflow at 430°C was performed in our process. Based on our previous study, breakage occurred along Si chips and alumina substrates if bonding was conducted at 320°C directly on the Au/Sn/Au structure without the initial reflow. In the temperature range of 231°C to 320°C, the Sn layer in the Au/Sn/Au structure melted and dissolved the Au atoms. The Au composition in the molten phase increased as the reaction continued. When the total composition approached the AuSn phase, the amount of molten phase became small when compared with the AuSn solid grains. The molten phase could not flow and wet uniformly over the gap between the chip and the substrate due to the solidifying AuSn grains. Voids and gaps, thus, were formed. To ensure all Au-Sn compounds are dissolved in the molten phase, the reflow at 430°C is performed prior to the bonding process.

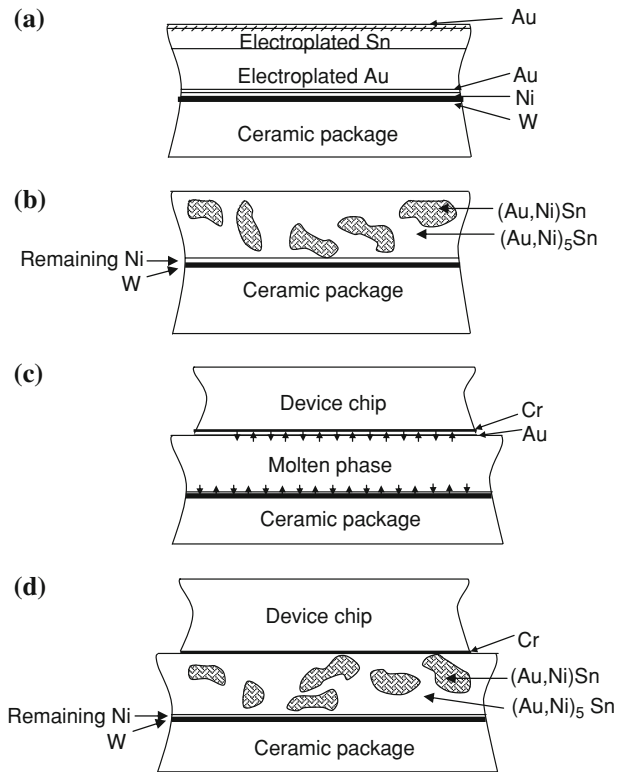


Fig. 7. The reflow and bonding mechanism: (a) after electroplating; (b) after initial reflow, the homogeneous eutectic 80Au-20Sn alloy is formed; (c) at the bonding temperature of 320°C; (d) after cooling to room temperature, the joint is made between the Si chip and the ceramic package.

The ceramic package can easily withstand the temperature of 430°C.

### CONCLUSIONS

In this research, fluxless bonding between large SOI chips (9 mm × 9 mm) and commercial ceramic packages has been successfully developed. The Au/Sn/Au multilayer structure was electroplated over ceramic packages. When the thin outer Au layer was plated, it reacted with Sn atoms to form the AuSn<sub>4</sub> compound, which protects the inner Sn from oxidization. After the reflow process, the Au/Sn/Au multilayer structure turned into the eutectic 80Au-20Sn alloy with dissolved Ni atoms. The SOI chip with Cr/Au was then bonded to the ceramic package with the eutectic 80Au-20Sn solder in a 50-mTorr vacuum. High-quality joints were made without using any flux. The joint demonstrates a Au-Sn eutectic-like microstructure that consists of (Au,Ni)Sn and (Au,Ni)<sub>5</sub>Sn phases. The fluxless bonding process reported offers the electronics industry an attractive means for fabricating the Au-Sn eutectic alloy on a package and subsequently bonding a device without flux. This fluxless nature is valuable in various applications such as photonic devices, microwave devices, MEMS devices, sensor devices, and biomedical devices, where the use of flux is detrimental.

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### REFERENCES

1. E. Jung, *MRS Bull.* 28, 51 (2003).
2. R. Therrien, S. Singhal, A. Chaudhari, W. Nagy, J. Marquart, J.W. Johnson, A.W. Hanson, J. Riddle, P. Rajagopal, B. Preskenis, O. Zhitova, J. Williamson, I.C. Kizilyalli, and K.J. Linthicum, *IEEE MTT-S International Microwave Symposium Digest* (2006), p. 710.
3. S.B. Park, R. Joshi, and B. Sammakia, *IEEE Twenty-First Annual Semiconductor Thermal Measurement Management Symposium* (2005), p. 214.
4. J.Z. Shi, X.M. Xie, F. Stubhan, and J. Freytag, *Trans. ASME* 122, 168 (2000).
5. S.K. Kang, R.S. Rai, and S. Purushothaman, *IEEE Trans. Compon. Packag. Manuf. Technol. A* 21, 18 (1998).
6. K. Mizuishi, M. Tokuda, and Y. Fujita, *IEEE Electronic Components Conference* (1988), p. 330.
7. S. Bonafede, A. Huffman, and W.D. Palmer, *IEEE Trans. Compon. Packag. Technol.* 30, 604 (2006).
8. R. Venkatramna, J.R. Wilcox, and S.R. Cain, *Metall. Mater. Trans. A* 28A, 699 (1997).
9. D. Kim, J. Kim, G.L. Wang, and C.C. Lee, *Mater. Sci. Eng. A* 393, 315 (2005).
10. C.C. Lee, C.Y. Wang, and G. Matijasevic, *IEEE Trans. Compon. Hybr. Manuf. Technol.* 14, 407 (1991).
11. G.S. Matijasevic, C.C. Lee, and C.Y. Wang, *Thin Solid Films* 223, 276 (1993).
12. C.C. Lee and J. Kim, *Proceedings of the 10th IEEE International Symposium on Advanced Packaging Materials* (Irvine, CA, March 16–18, 2005).
13. C.C. Lee, D.T. Wang, and W.S. Choi, *Rev. Sci. Instrum.* 77, 125104 (2006).
14. S. Anhöck, H. Oppermann, C. Kallmayer, R. Aschenbrenner, L. Thomas, and H. Reichl, *Proceedings of IEEE/CPMT Berlin International Manufacturing Technology Symposium* (1998), pp. 156–165.
15. J.Y. Tsai, C.W. Chang, Y.C. Shieh, Y.C. Hu, and C.R. Kao, *J. Electron. Mater.* 34, 182 (2005).
16. J.Y. Tsai, C.W. Chang, C.E. Ho, Y.L. Lin, and C.R. Kao, *J. Electron. Mater.* 35, 65 (2006).
17. H. Okamoto and T.B. Massalski, eds., *Phase Diagram of Binary Gold Alloys* (Metals Park, OH: ASM International, 1987), pp. 278–289.