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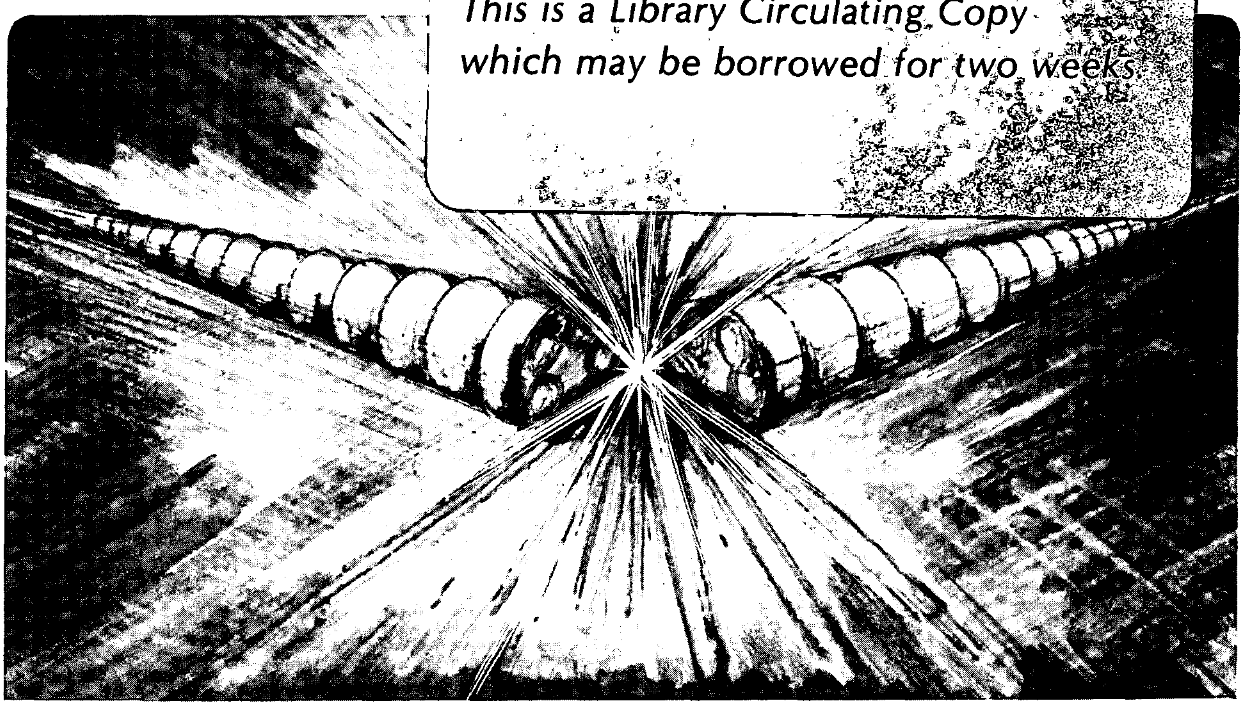

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Summary

The Multiple Beam Experiment MBE4 (1) is designed to accelerate four cesium ion beams from 200 kV to about 1MV using an induction linac and to demonstrate the process of current amplification simultaneously with acceleration.(2) The injected beam is obtained from a source using a Marx generator providing typically 10mA/beam with a length of 1.6 meters. This is equivalent to a beam duration time of about 3 μsec. Twenty four acceleration gaps in groups of four are distributed along the length of the machine which will be some 16 meters long when completed. Each group of four acceleration gaps with appropriate quadrupoles form one section of the machine, identified as A through F.

Careful tailoring of the acceleration voltage waveforms at each gap is required to accelerate the beam, amplify the current and provide longitudinal focussing. Ideal voltage waveforms for each gap were generated (3) for a gap voltage limit initially set at 30 kV. These waveforms are shown in Fig. 1. The waveforms for the first 4 gaps are triangular with an approximate width of 3 μsec, becoming flatter and shorter at subsequent gaps as the beam bunch velocity increases.

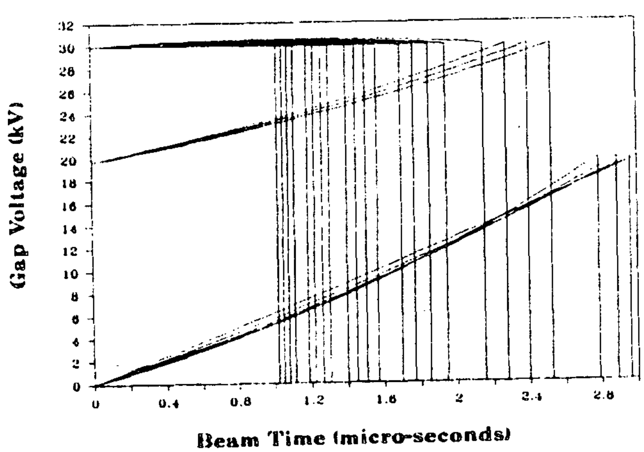

Fig. 1. Ideal Accelerating Voltage Waveforms for all 24 Gaps

Ninety two nickel-iron tape wound cores capable of 6.8 mVsec./core and twenty six silicon steel tape wound cores capable of 24 mVsec./core were available. Groups of cores at the first eight gaps have been used in conjunction with an appropriate number of pulsers to provide the necessary accelerating voltage waveforms together with the pulser waveforms at every fourth acceleration gap which provides the longitudinal focussing of the beam. This paper will deal with the performance of the pulsers for the first eight gaps of acceleration and expectations for the next four, currently under construction.

Introduction

Three different pulser circuit types were initially identified as possible solutions for generating the required waveforms for the machine. These pulsers were identified by the generated voltage waveforms which are (1-cosωt), parabolic, and trapezoidal, the trapezoidal being only relevant to the later part of the machine waveforms. It was found necessary during pulser modelling to add a simple capacitor discharge waveform to this list. Some basic performance characteristics were established for the (1-cosωt) and parabolic waveforms using the nickel-iron cores. The (1-cosωt) circuit as shown in Fig. 2 consists of a charged capacitor discharging via a series inductance into a core load that is paralleled by an uncharged capacitor. The parabolic waveform is achieved by paralleling the core with a resistor instead of a capacitor, the resistor being small enough to dominate the load impedance. The core impedance initially increases with time and during this period the load impedance needs to be almost constant in order to generate a parabolic voltage waveform. Because of the additional resistor loss and lower load impedance, this circuit configuration has not been used or developed further.

Basic performance characteristics were then established for the (1-cosωt) and capacitor discharge waveforms using the silicon steel cores. These characteristics together with those already established for nickel-iron cores are used to construct the pulsers for the first 12 acceleration gaps.

Initial attempts to generate trapezoidal waveforms with a 2 μsec wide flat top using a single pulser were not successful. Development of these pulsers will continue and a flat top pulse is expected to be more readily achievable as the required pulse width decreases.

A pulser standard was established which could operate at a maximum charge voltage of 30 kV with a peak current of 10 kA. A thyratron is used to provide the switch function and to date either an English Electric CX 1538 or ITT F227 is used. A total stored energy equivalent to 1 μF is available with a repetition rate dictated by the charging supply; the repetition rate is currently 1 pulse every 5 secs. Each pulser is a self-contained unit including the core reset but excluding the charge power supply. A total of 12 pulsers can be arranged below and at either side of the core assembly for one section.

MBE 4 Core Model Development

The first cores to be tested and used

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exclusively in section A of MBE 4 are the nickel-iron cores. These cores are made with 0.001 inch thick material, are 1/2 inch wide and have a final assembly inner diameter of about 13 inches and an outer diameter of about 33 inches. Maximum flux capacity is about 6.8 mVsec. with about a 7% variation among samples.

In attempting to model core behavior with the computer program Spice (4) it was found that considering the core as a simple resistor gave reasonable agreement in amplitude and time. A value of 5 Ω per core was chosen for nickel-iron cores based on the measured performance characteristics; again about a 7% variation was observed among the samples. Since the beam load current is small its effect and the equivalent resistance can be ignored.

Figs. 2 and 3 show the circuit arrangement and basic computer model for a core package containing six nickel-iron cores, and a (1-cosωt) arrangement at a charge voltage of 20 kV. A better model for this circuit is obtained by adding a series resistance and inductance between the voltage source and the core load. This represents the voltage source impedance and core leakage inductance. The predicted and measured values for this circuit at different charge voltages can be seen in Figs. 4 and 5 respectively.

A Spice listing for this circuit, including the series resistance and inductance between the voltage source and the load, with several values of charge voltage follows:

```
*SEC A, COS, 6 AST CORES
C1 1 3 .3U IC=24
R1 3 7 1
V1 0 7 0
L2 1 5 2.5U
L1 5 2 40U
C2 2 0 .04U
RC 2 4 28.5
V2 4 0 0
.TRAN 100NS 5U UIC
.PLOT TRAN V(2) (0,25)
.WIDTH OUT =80
.OPTIONS LIMPTS=9000 NOPAGE ITL5=9000
.ALTER
C1 1 3 .3U IC=20
.ALTER
C1 1 3 .3U IC=15
.ALTER
C1 1 3 .3U IC=10
.ALTER
C1 1 3 .3U IC=5
.END
```

In section B, we added silicon steel cores to the inventory. These are made with 0.002 inch thick material, 1.37 inches wide with the same assembly dimensions as the nickel-iron cores and with a 23.9 mVsec. flux capacity. Additional circuit models were required for these cores for both the capacitor discharge and (1-cosωt) configurations. The risetime of the capacitor discharge voltage waveform is dictated by the longitudinal focusing required for the head of the beam and is typically 0.8 μsec. The step function skin depth is about 0.001 inches so the magnetic field distribution can be considered uniform. The dominant effect is again core loss. However, driving the core from the time when the magnetic flux has been established towards saturation there is an almost linear increase in current. A better approximation to model the core is a resistance in parallel with an inductance. Again the effects of the core secondary can be ignored. The core leakage inductance can be modelled as an inductance in series with the load equivalent circuit and can be lumped together with the interconnection inductance between the pulser and core. The model is completed by adding a resistance in series with this inductance to represent the voltage source resistance.

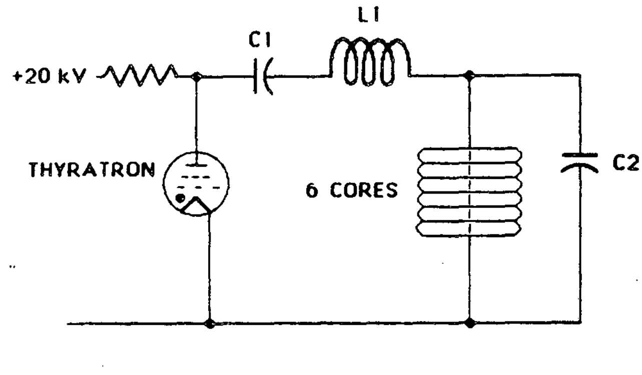

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Fig. 2 Circuit Diagram for a Core Package containing 6 Nickel-Iron cores, and a (1-cosωt) Pulser

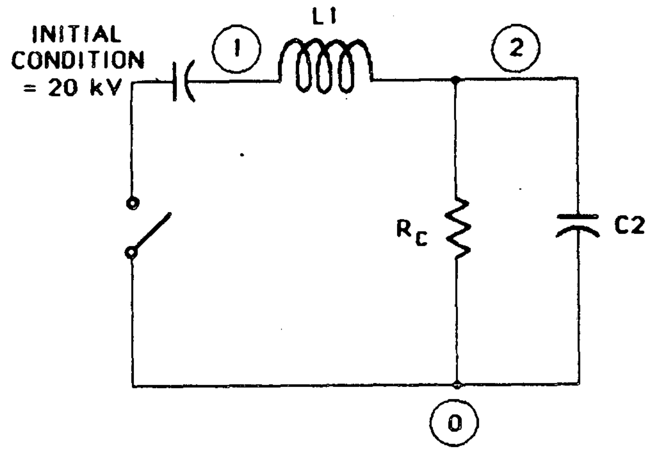

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Fig. 3 Spice Model for a Core Package containing 6 Nickel-Iron Cores and a (1-cosωt) Pulser

A sequence of measurements was made at different charge voltages for the capacitor discharge circuit using 2 silicon steel cores in series to show how the load impedance varied with time. This is shown in Fig. 6.

Using the data for the capacitor discharge circuit Fig. 6 and assuming the initial load equivalence is resistive, the values of resistance for various charge voltages were established. The resistance value for a given charge voltage was used to compute the core current. This resistance value was modified until the computed core current matched the measured core current at the time the core voltage was at a maximum. This was repeated for each charge voltage and the resistance values obtained are given in Table 1.

These load equivalence parameters were used to generate the computed voltage waveforms for the capacitor discharge and (1-cosωt) circuits, and are shown with the measured waveforms at Figs. 7, 8, 9, and 10. A total of 2.5 μH was used in the model to represent the lumped leakage inductance and a resistance of 1 Ω in series with this inductance models the source resistance.

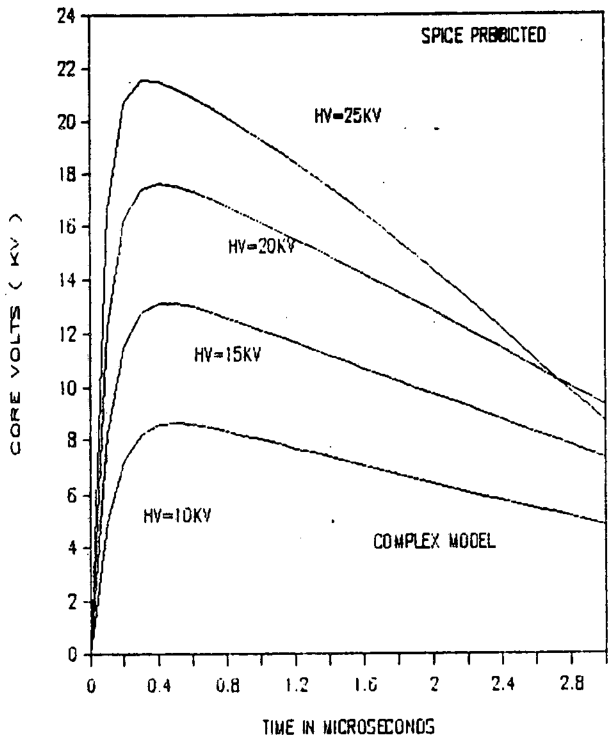

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Fig. 7 Spice Predicted Core Voltage for a 2 Silicon Steel, Capacitor Discharge Pulser at Different Charge Voltages

The Spice model does not predict the ringing that was observed at gap 8 for the capacitor discharge circuit both with and without the addition of a load capacitance of 700 pF, which is typical of its load capacitance. It would if it were modified by the addition of a small inductance between the core load capacitance and the core equivalence of a resistance in parallel with an inductance. This appears to be a reasonable modification.(6) The core model for a 0.3 μF capacitor charged to 25 kV discharging into two silicon steel cores is 2 μH in series with the combination of 30 Ω in parallel with 30 μH. Initial computed results using this model for 2 silicon steel cores have shown good agreement with the measured performance for voltage and current waveforms for both capacitor discharge and (1-cosωt) circuits.

Section A Pulsers

A core arrangement for the first four gaps, section A, was established based on the voltage waveform requirements as indicated in Fig. 1. Each gap has 12 nickel-iron cores arranged as shown in Fig. 11. Two pulsers were allocated to each gap, each pulser producing a (1-cosωt) voltage waveform. Two degrees of adjustment are available for each pulser, charge voltage and firing time. The arrangement for each gap is generally 6 cores/1 main pulser and 2 cores/1 auxiliary pulser.

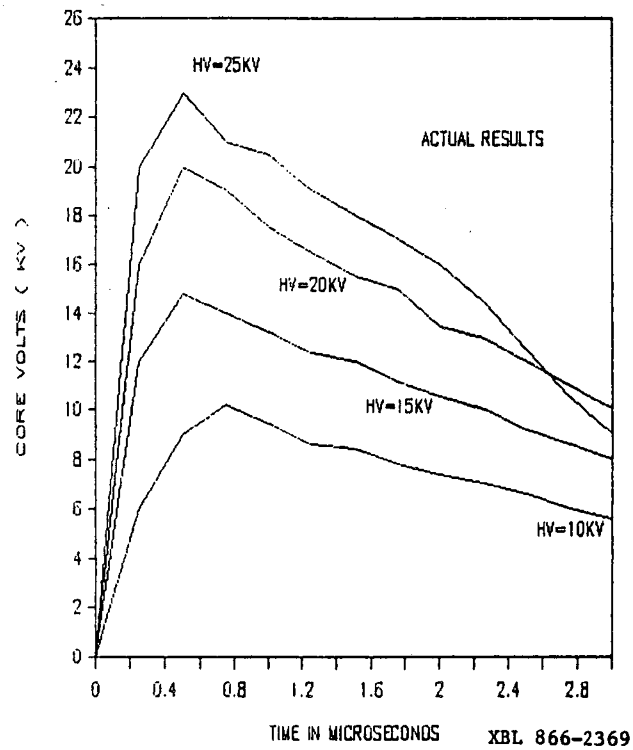

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Fig. 8 Measured Core Voltage for a Core Package containing 2 Silicon Steel Cores and a Capacitor Discharge Pulser at Different Charge Voltages

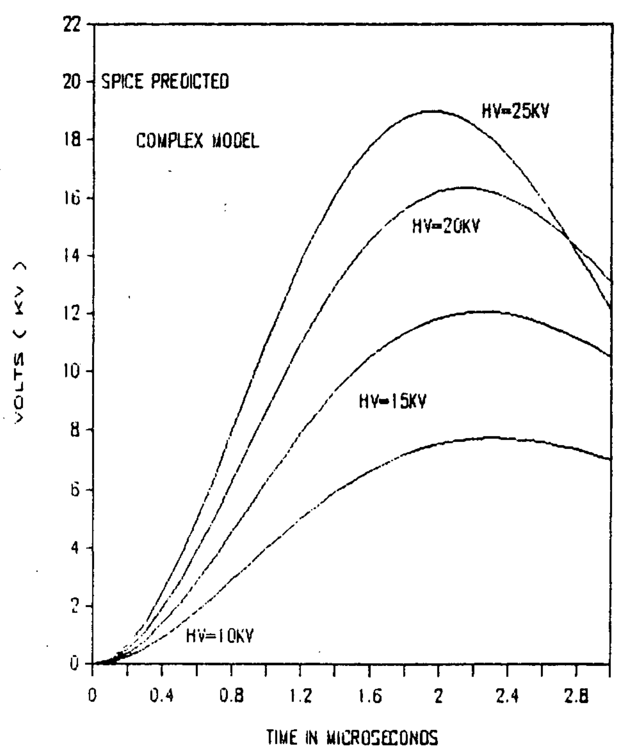

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Fig. 9 Spice Predicted Core Voltage for a Core Package containing 2 Silicon Steel Cores and a (1-cosωt) Pulser at Different Charge Voltages

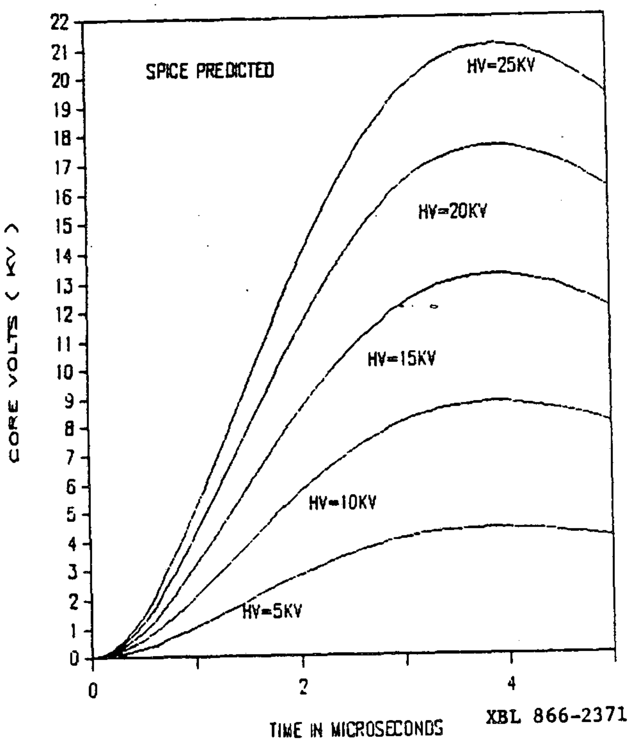

Fig. 4 Spice Predicted Core Voltage for a Core Package containing 6 Nickel-Iron Cores and a (1-cosωt) Pulser at Different Charge Voltages

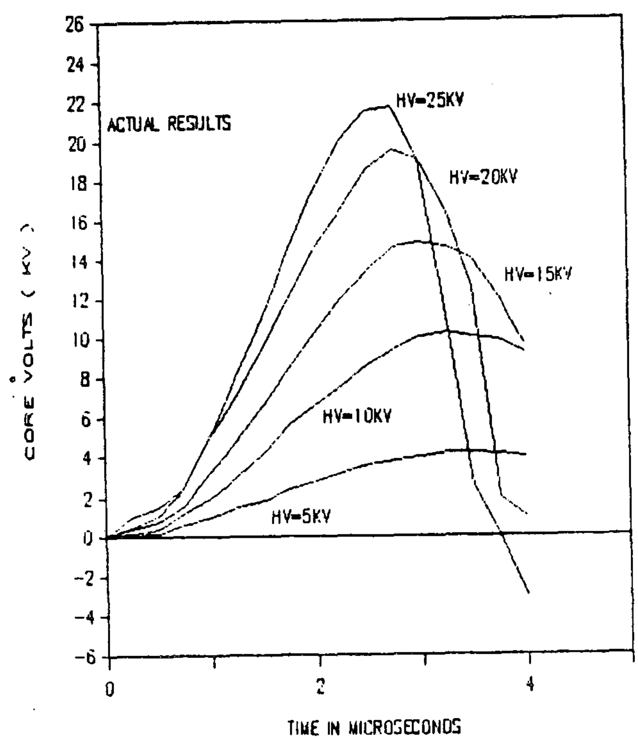

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Fig. 5 Measured Core Voltage for a Core Package containing 6 Nickel-Iron Cores and a (1-cosωt) Pulser at Different Charge Voltages

The core load inductance was calculated from L = μ (core area/path length) and used in conjunction with the appropriate resistance equivalence at a specific charge voltage to generate computed voltage and current waveforms. The inductance value was modified using the measured current waveform as reference until the computed waveform matched the measured waveform up to saturation. This was done at different charge voltages and the values obtained given in Table 1.

An analytically derived model for magnetic induction cores (5) is, in its simplest form, a resistance in parallel with an inductance. The derived load equivalence for a 2 silicon steel core pulser is 17Ω in parallel with 68.6 μH.

Table 1: Values of resistance and inductance at different charge voltages for a model of a core package containing 2 silicon steel cores

Charge volts kV	10	15	20	25
Resistance Ω	18	21	25	30
Inductance μH	105	80	55	30

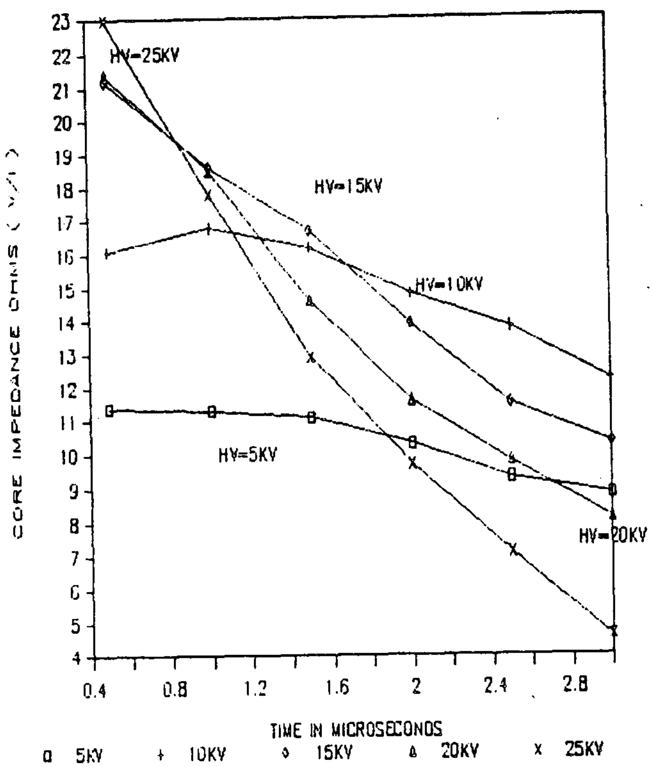

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Fig. 6 Measured Values of Core Impedance with Time for a Core Package containing 2 Silicon Steel Cores for the Capacitor Discharge Pulser at Different Charge Voltages.

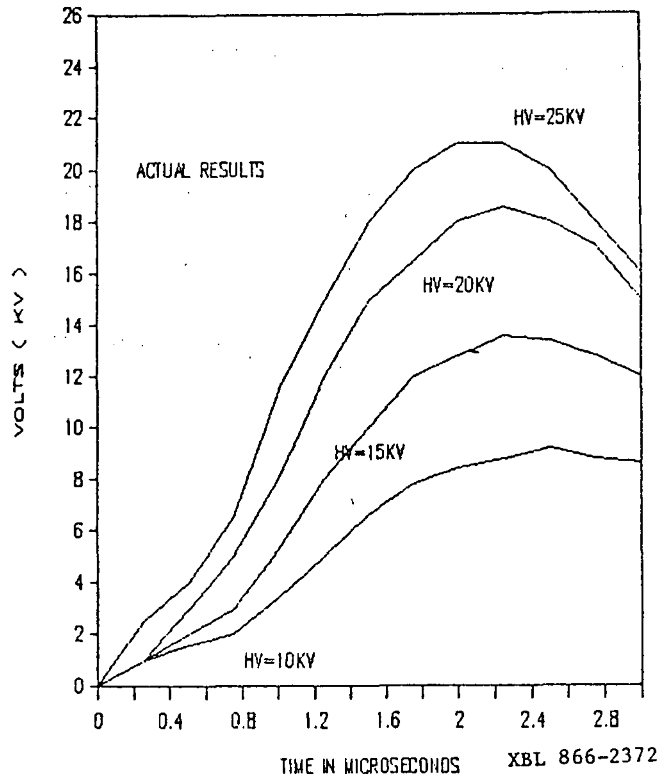

Fig. 10 Measured Core Voltage for a Core Package containing 2 Silicon Steel Cores and a (1-cosωt) Pulser at Different Charge Voltages

Modelling the performance of the circuit to optimize components and minimize test set-up time was done using the program Spice as described previously. Generally, a fixed resistance was used to model the core, as the core losses dominate the load impedance.

The trim voltage waveforms needed to compensate for the longitudinal space charge force at the ends of the beam bunch were designed after measurements were made with beam acceleration. Correction to the tail of the beam was made using a (1-cosωt) pulser and 3 nickel-iron cores at gap 4. The correction required at the head of the beam was exaggerated by the characteristic of the Marx generator. Because of the difficulty in controlling the trailing edge of the voltage waveform, this created a correction problem that was deferred to section B, where the rise time of the waveform at gaps 6-8 would be used. A composite waveform for gaps 4 is shown in Fig. 12 with the individual pulser voltages.

Section B Pulsers

A core package arrangement for the four gaps in section B was constructed based on the voltage waveform requirements as outlined in Fig. 1 and expected pulser performance. A combination of silicon steel cores and nickel-iron cores are used together with a minimum of two pulsers per gap to provide the required synthesized accelerating voltage waveforms. A combination of (1-cosωt) pulsers driving nickel-iron cores and capacitor discharge pulsers driving silicon steel cores provide most of the accelerating voltage. The circuit components were again optimized by modelling the various circuit configurations using Spice as defined earlier. A trim pulser similar to that used in section A, gap 4, was added to gap 9 to correct the tail of the beam. A composite of the voltage for gap 8 is shown in Fig. 13.

The rising edge of the voltage waveforms at gaps 6, 7, and 8 were adjusted by the addition of a series inductance in the capacitor discharge pulser circuit so that they match the predicted value. This provides the correction for longitudinal beam spreading and Marx voltage errors.

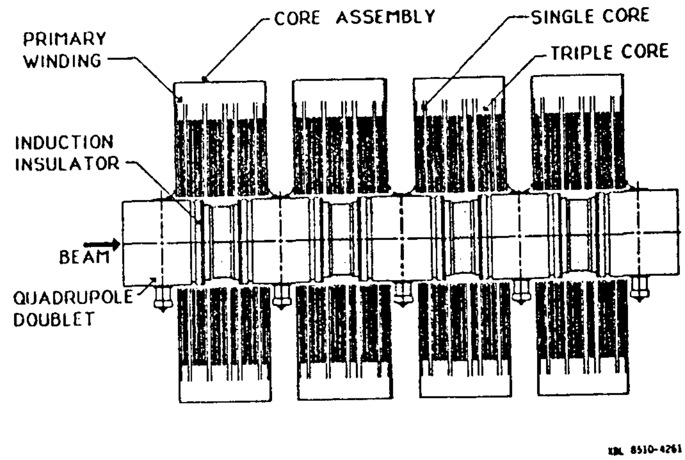

Fig. 11 Accelerator Section A

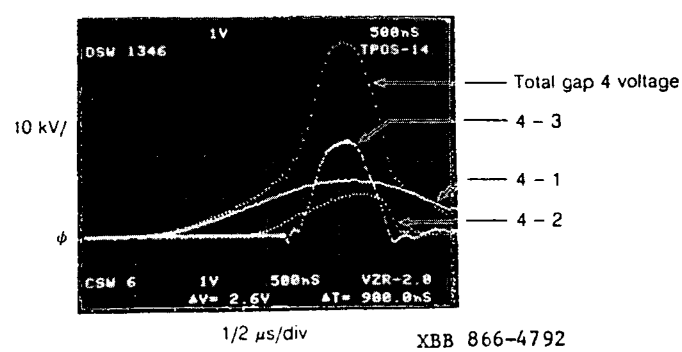

Fig. 12 Individual Pulser and Composite Accelerating Voltage Waveforms at Gap 4

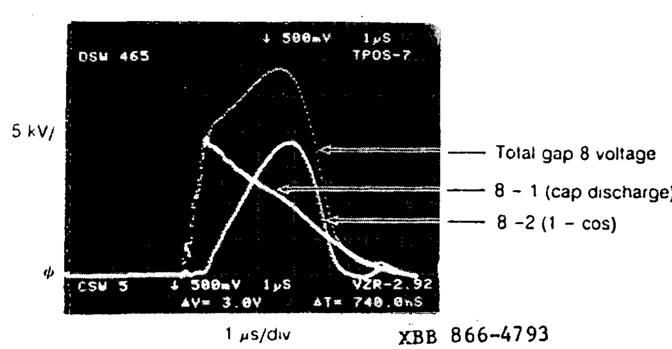

Fig. 13 Individual Pulser and Composite Accelerating Voltage Waveforms at Gap 8

Oscillations were observed on the voltage waveform produced by the capacitor discharge circuit at gap 8. These were effectively damped by modifying the added series inductance so that there are two inductors of equal value and converting these into series reject circuit by the addition of appropriate parallel capacitors. The resonant frequencies were based on the measured oscillations observed on the voltage waveform which were 3 MHz and 8 MHz.

Section C Pulsers

The accelerating voltage waveforms required for the four gaps in this section, as shown in Fig. 1, are trapezoidal with a flat top width of 2 μsec and an amplitude of 30 kV. A core arrangement using 4 silicon steel cores at each gap will provide the necessary mVsec needed together with nickel-iron cores at gap 14 for a beam tail correction pulser circuit.

Two pulsers per gap for gaps 11-13 using existing circuitry are currently being constructed together with a pulser arrangement at gap 14 similar to that used at gap nine; this is scheduled for operation at the beginning of September 1986.

Conclusions

The computer program SPICE proved to be a useful aid in determining the pulser voltage waveshaping component values with a simple resistor as a core equivalence particularly for a limited range of charge voltages. The complex non-linear behavior of the core load could be better modelled by making a series of measurements on the cores using a capacitor discharge pulser. No attempts were made to model the pulser behavior during core saturation; however, the measured data indicate a core impedance that falls rapidly towards zero in the well documented manner.

The analytical solution and subsequent core model performance as a load for a pulser shows a good degree of agreement with the measured performance. Data obtained using these models will allow core package arrangements and pulser configurations to be more readily investigated.

Whenever possible, multiple core loads were connected together electrically in series to present as high an impedance as possible. This minimized the thyratron load current and provided the highest voltage transfer ratio between core voltage and charge voltage.

The pulsers in Section A have been operating satisfactorily since October 1985 and those in Section B since April 1986. To date, the maximum pulser operating level is a charging voltage of 25 kV and a peak load current at saturation of about 5 kA. The voltage transfer ratio, core voltage to charge voltage, is typically 0.8.

Using a minimum of two pulsers at each gap and with the freedom to control the charge voltage and trigger time to better than 10 nsec for each pulser it has been possible to match the required accelerating voltage to within 1% (7).

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