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Low Phase Noise Pulse Rotary Wave Voltage Controlled Oscillator

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***Abstract*— This paper presents a low phase noise, wide tuning range voltage controlled oscillator. The oscillator uses a rotary wave oscillator topology, with pulse regenerative gates used as amplifiers. Pulse gates confer a paticular low-duty cycle pulse waveform whose arrival time is very weakly dependent on amplitude or pulse width. This reduces the root mean square value of Impulse Sensitivity Function, thereby reducing the phase noise. Further, the oscillator rejects common mode supply noise by double inversion of signals in every stage. Timing signals are ground referenced so the supply can be used as a control voltage. The fabricated 2.96 GHz oscillator in GFUS8RF(130nm) has phase noise of -132.2dBc/Hz @ 10MHz offset. The oscillator has a tuning range of 2.64GHz to 2.96GHz with average phase noise of -130.71dBc/Hz @ 10MHz offset.**

I. Introduction and Concepts

High precision, low phase noise, multi phase voltage controlled oscillators are needed in many RF applications ranging from radio links to ADCs. Rotary wave oscillators are noted for their low jitter timing distribution [1]. Such oscillators have very small tuning range and are usually phase locked to get good timing performance. Pulsed wave oscillators have been widely studied and the linear pulse oscillator has been shown to have best conventional phase noise properties [2]. In contrast, this work uses the Rotary wave oscillator topology replacing the amplifiers with pulse-gates having regenerative pulse properties. The work combines the pulse phase noise properties originating out of smaller ISF [3] and non linear amplification properties of rotary wave oscillators (transistors in cut-off have negligible noise current), to make a stable pulse rotary wave clock. Multi-phase output in the ring oscillators are limited by the inverter delay. Pulse based rotary wave design gives the ability to tap phases in the T-line without the constraint of buffer delay.

II. Design

A. Oscillator Topology

The oscillator design is a transmission line ring with 16 buffering points folded so that the speed of light delay along the TM-line is matched to the buffer delay between the folded access points. In contrast to previous work, the buffer elements are very non-linear pulse-gates [4] that sense a rising edge on input and output a pulse. By design, the buffer is insensitive to both the pulse width and amplitude once a threshold is met and the pulse-shape lowers the active duty cycle of the oscillator. These properties reduce the RMS average ISF (Impulse Sensitivity Function) [3], resulting in substantial phase noise improvement. Internally the signals are buffered (double inversion) [5] improving high frequency supply noise rejection. LC Oscillators typically have one phase output. In contrast, the described oscillator has 16 equally-spaced pulse taps, each with identical jitter and drive.

B. Pulse Gate

The pulse-gates used as non-linear amplifiers are shown in Figure 1. The amplifier is a self-reseting pulse generator. V_{crit} is pulled down on the rising edge of the signal at V_{in}. This pulls up V_{out} and pulls down V_{reset}, causing the PMOS to pull up V_{crit}, which causes V_{out} to pull down. The generated pulse at V_{out} is relatively insensitive to the input pulse shape or amplitude. After the pulse output, but before the reset has concluded, the input is insensitive to further pulses and the output is low impedance to ground, suppressing the reverse wave in the TM-line. After a suitable delay, V_{reset} returns to its steady state awaiting the next incoming pulse.

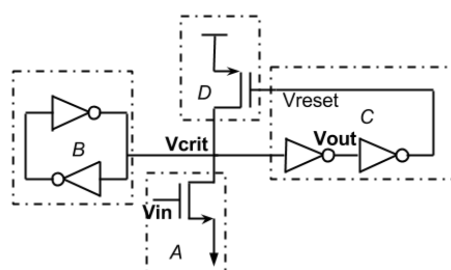


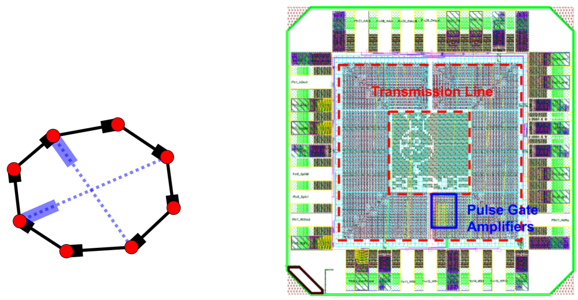
Fig. 1: Pulse-gate Topology. **A:** Input Logic for V_{crit} Pull Down **B:** Threshold control for V_{crit} **C:** Reset Loop and Pulse Width Control **D:** Pull up for V_{crit}

C. Fabricated Design

Pulse buffers are interleaved along the TM-loop as shown in 2a. The buffers maintain the direction of the traveling wave by active cancellation of the reverse wave. The fabricated design used co-planar transmission lines with a bottom ground plane. Sizing of the buffers must overcome the loss in the transmission line. Ideally the transistors can be

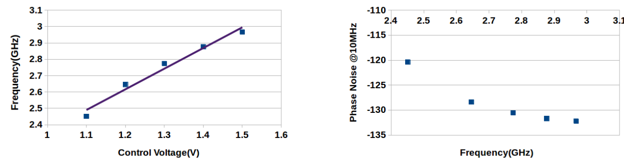
TABLE I: Comparison with Other Oscillators

Ref	Technology	Phase Noise	Power	Measurement Frequency	Tuning Range	Phases	Topology	Area
This Work	130nm	-132.2dBc/Hz@10MHz	68.7mW	2.96 GHz	2.67-2.96 GHz	16	Rotary Wave	$0.66mm^2$
[6]	110nm	-140.8dBc/Hz@3MHz	52.8mW	3.05 GHz	3.05-3.65 GHz	12	Rotary Wave	$1mm^2$
[7]	130nm	-132 dBc/Hz@3MHz	1.4 mW	5 GHz	4.9-5.65 GHz	1	LC	-
[8]	180nm - VCO	-128 dBc/Hz@1MHz	7.2 mW	1.79 GHz	1.59-1.98 GHz	1	LC	0.69 mm^2
	180nm - QVCO	-127 dBc/Hz@1MHz	8.6mW	2 GHz	1.83-2.24 GHz	2	LC	1.36 mm^2
[9]	130nm	-114dBc/Hz@1MHz	12-31 mW	6 GHz	5.5 - 9.2 GHz	8	Active Inductor	0.12 mm^2
[10]	180nm	-126 dBc/Hz@1MHz	3 mW	2.47 GHz	2.23 - 2.68 GHz	8	LC	1.14 mm^2



(a) (b)

Fig. 2: (a)The transmission line (Black-solid line) is folded and buffers (red circle) connect across multiple segments to feed-forward (blue-dashed line) a pulse (b))Die Micrograph with folded Transmission Line and Buffers as shown



(a) (b)

Fig. 3: Control Voltage-vs-Operating Freq.: Linear Behavior(b) Phase Noise@10MHz-vs-Operating Frequency

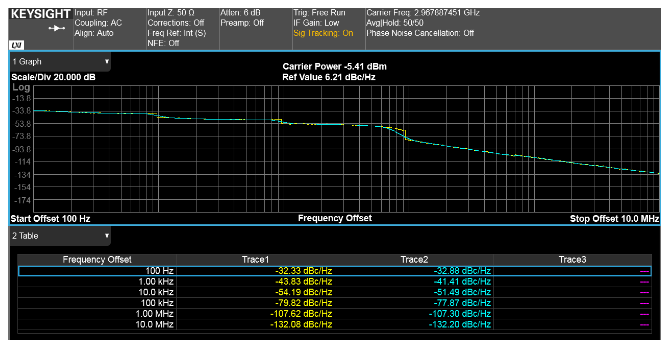


Fig. 4: Measured Phase Noise@10MHz for freq.=2.96GHz

sized to just compensate for the loss. However, this creates a very small tuning range and little process slack in the oscillator, for both transistor gm variance and TM-line loss. The fabricated design chose to over design buffers to ensure a wide operation supply and variance range at the cost of total power dissipation.

III. Results and Comparison

The layout of the fabricated oscillator is shown in 2b. Its phase noise spectrum at 2.96GHz is shown in Figure 4. The oscillator has linear frequency depenence with control voltage as shown in 3a. Phase noise measured @10 MHz offset across the frequency range is shown in 3b. 10 MHz was chosen to avoid flicker and power supply coupled noise sources on these free-running (not phase locked) oscillators. The oscillator has comparable phase noise performance with other rotary wave and LC oscillator designs and outputs a 16 phase clock with $21pSec$ phase to phase separation, which is better than any other design at this phase noise and power numbers. Overall, pulse rotary wave clocks offer an methodology to bridge the gap between LC oscillators and Ring oscillators. They offer multi-phase output benefits of ring oscillators but at phase noise which is comparable with LC oscillators. High power consumption is the trade-off for multi-phase output.

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