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IRVINE

Energy-Efficient CMOS Integrated Circuits and Systems for Brain-Machine Interfaces

DISSERTATION

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for the degree of

DOCTOR OF PHILOSOPHY

in Electrical and Computer Engineering

by

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DEDICATION

To my family

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40th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)

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A Fully-Integrated 1 μW/Channel Dual-Mode Neural Data Acquisition System for Implantable Brain-Machine Interfaces **2021**

ABSTRACT OF THE DISSERTATION

Energy-Efficient CMOS Integrated Circuits and Systems for Brain-Machine Interfaces

By

Omid Malekzadeh Arasteh

Doctor of Philosophy in Electrical and Computer Engineering

University of California, Irvine, 2021

Professor Payam Heydari, Chair

Restoring the ability to walk in individuals with chronic spinal cord injury is an ambitious goal that has been rigorously pursued in recent years. While there have been a number of attempts to enable walking in those patients, no universally accepted biomedical solution exists to address this grand challenge to this day. Brain-machine interfaces (BMIs) are one of the promising platforms to restore motor and sensory functions in people with paraplegia. However, fully-implantable BMIs must address a number of critical issues to become clinically viable, in particular excessive overall power dissipation and inadequate interference resilience in neural recording.

In this dissertation, an energy-efficient electrocorticography (ECoG) array architecture for fully-implantable BMIs is presented. A novel dual-mode analog signal processing method is introduced that extracts neural features from high-γ band (80-160 Hz) at the early stages of signal acquisition. This approach utilizes a distinct optimized signal pathway based on power envelope extraction to achieve significant power savings for digitization and processing. A prototype incorporating a 32-channel ultra-low power signal acquisition front-end was fabricated in 180nm CMOS process and successfully tested *in vitro* and *in vivo*.

Next, an ultra-low power mixed-signal neural data acquisition system is presented. The dual-mode data acquisition system enables a novel low-power hybrid-domain neural decoding architecture for implantable BMIs with high channel count. The fully-integrated custom chip implemented in 180nm CMOS process achieves excellent performance with significant back-end power-saving advantage compared to prior works. The fabricated prototype was further evaluated with *in vivo* human tests at bedside, in addition to electrical characterization.

Finally, common-mode interference phenomenon in multi-channel biosignal recording systems employing a shared-reference scheme is studied. While it is well-understood that a shared-reference scheme causes impedance mismatch at the input terminals of bioamplifier, and thus limits the maximum achievable common-mode rejection ratio (CMRR), a theoretical study that can provide quantitative assessment of this source of degradation is still lacking. This section provides an equivalent electrical circuit model of the input interface consisting of an electrode array and bioamplifiers, followed by a complete analysis to formulate the CMRR degradation.

Chapter 1

Introduction

1.1 Motivation

Restoring the ability to walk in individuals with chronic spinal cord injury is an ambitious goal that has been rigorously pursued in recent years. While there have been a number of attempts to enable walking in those patients, no universally accepted biomedical solution exists to address this grand challenge to this day. Brain-machine interfaces (BMIs) are one of the promising approaches to restore motor and sensory functions in people with paraplegia. Such platforms incorporate a cyber-physical system (CPS) that interacts directly with the brain in order to establish a seamless walking experience by exploiting neural interfaces, wireless communication devices and robotic prostheses.

Despite the natural desire for a non-invasive approach to implement BMIs, there is a growing need to realize fully-implantable systems that could potentially outperform the existing proposed solutions by accurately decoding the task-specific neural information. The inherent advantage of a minimally-invasive neural implant is that it can facilitate signal acquisition with higher spatiotemporal resolution in the vicinity of brain tissue, however, a number of

critical issues need to be addressed. Most importantly, to become clinically viable, the overall power consumption must be minimized to prolong the operation time in such biomedical implants.

To realize an energy-efficient interference-resilient BMI that could be fully implanted, this dissertation presents (1) a novel dual-mode array architecture which aims to significantly reduce the power dissipation in the mixed-signal and digital back-end with negligible overhead in the front-end acquisition (2) a fully-integrated 1μW/channel neural data acquisition system based on the proposed dual-mode operation (3) a detailed common-mode interference analysis in biosignal recording systems.

1.2 System Overview

Fig. 1.1 shows the overall proposed CPS that encompasses an electrocorticography (ECoG)-based BMI to restore walking. The main components include two implanted units, one inside the skull and one over the chest area, and external robotic prosthetic legs. To allow neural recordings with improved spatiotemporal resolution, a high-density subdural electrode grid is surgically placed over the motor cortex area of the brain. The neural signals are obtained by a custom-designed miniaturized multi-channel recording system, which is located in the skull unit. To minimize the heat dissipation in the vicinity of brain tissue, the recording system consumes microwatt-level power to avoid any cell/tissue damage.

Once the neural data are acquired, serialized and digitized in the skull unit, they are transferred to the chest-wall unit via a tunneling cable, where the power-hungry modules such as general-purpose digital signal processor (DSP) and wireless transceivers (TRX) are located. Further signal processing and neural decoding are performed in DSP, and the control commands are relayed to the external robotic prostheses via TRX. In this approach, brain signal

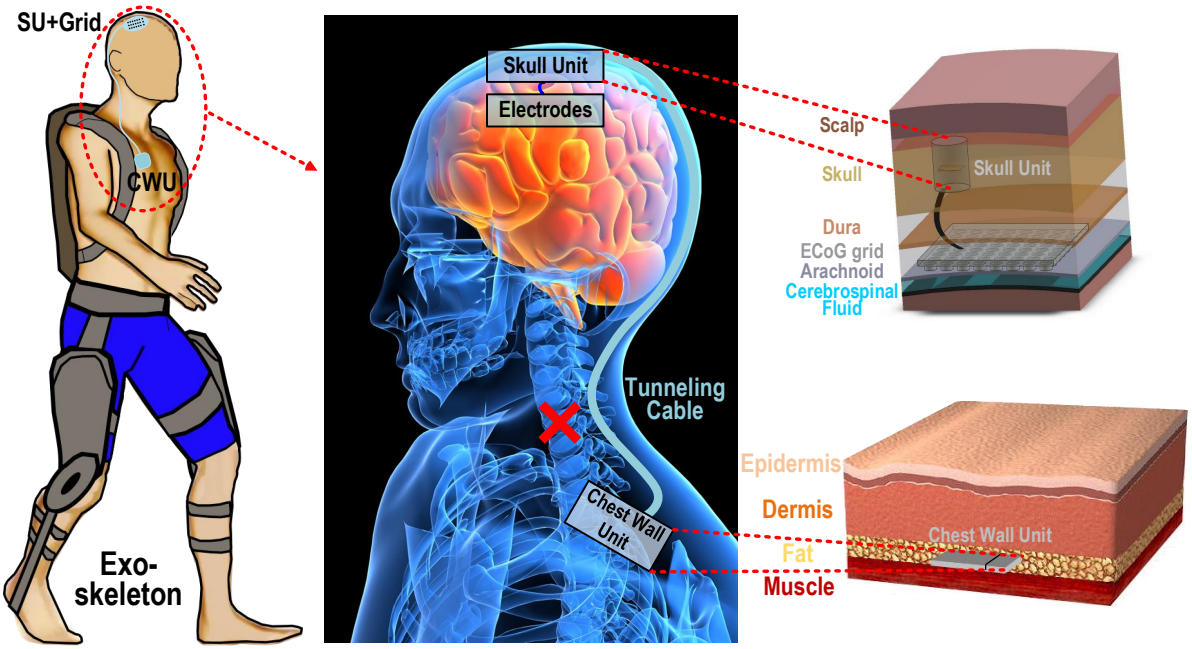

Figure 1.1: Proposed cyber-physical system incorporating a fully-implantable ECoG-based brain-machine interface to restore walking.

acquisition, processing and wireless transmission are achieved in a manner that eliminates direct exposure of brain to high transmit power, avoiding any potential risks associated with radio-frequency radiation. In the next section, a brief review of brain signals, biopoetential electrodes and state-of-the-art biosignal recording systems is presented.

1.3 Background

1.3.1 Brain Signals

Bioelectric potentials are produced as a result of electrochemical activity of a certain class of cells, known as excitable cells in the tissue [3]. The excitable cells exhibit two states: rest and active. At the rest state, the cell membrane is more permeable to K+ ions than Na+ ions and thus the internal medium builds a potential difference (-40 to -90 mV) relative

to the exterior, to counteract the K+ ions diffusion gradient and reach an equilibrium. Once the excitable cell undergoes electrical stimulation either artificially or by the central nervous system, its membrane's permeability to Na+ ions increases such that its potential difference reaches +40 mV. However, this will be followed by a sharp decrease in the potential difference as the membrane returns to its resting state. This cycle of cellular potential is referred to as the action potentials (AP) which is fundamental in generation of different biopotential signals such as electrocardiography (ECG), electromyography (EMG), electroencephalography (EEG), electrocorticography (ECoG) and local field potentials (LFP). In BMI applications, EEG, ECoG, AP and LFP are commonly used to observe neural activity.

The existence of electric impulses was first reported by Richard Caton in 1875 [4]. Caton studied the animal brains using a galvanometer and observed small electric currents from the exposed cerebral hemisphere of monkeys and rabbits. In 1890, Adolf Beck published his findings on "electrical oscillations" in the brain and noted that these oscillations ceased after sensory stimulation, a first description of desynchronization in electrical brain potentials [5]. Three decades later in 1924, Hans Bergers recorded the first human EEG, invented the electroencephalogram and successfully observed alpha rhythms from the brain [6]. ECoG was pioneered by Wilder Penfield and Herbert Jasper in early 1950s, primarily for identifying the epileptogenic zones for surgical resection [7]. Although, EEG is considered as an effective non-invasive method for brain signal acquisition, ECoG offers higher signal power, higher spatial resolution and a broader spectral content which are crucial for future BMI systems. Thus, high-density (HD) ECoG grids serve as a suitable platform for motor signal acquisition and sensory cortex stimulation. ECoG signals exhibit a robust predictable decrease in α (8-12 Hz) and β (13-30 Hz) band powers, and increase in high-γ (80-160 Hz) band power over the motor cortex (i.e., the brain areas that control movement) in response to movements [1, 8, 9, 10, 11]. These key finding are the main motivation behind implementing a fully-implantable BMI that could be used to restore walking for patients with spinal cord injury.

1.3.2 Biopotential Electrodes

Although the input impedance of readout circuits in CMOS technology is typically very high, a non-zero current would still flow from the brain to the input amplifiers. This necessitates a transducer interface which converts the ionic current to electrical current, often called the biopotential electrode [12]. The principal operation of this interface is based on the electrode-electrolyte interaction which governs the current flow. The electrolyte (i.e. brain tissue) contains no free electrons and the electrode contains no free cations or anions, thus a chemical reaction (oxidation/reduction) is necessary to allow the current flow. However, this will disturb the neutrality of the solution and creates a charge gradient at the electrode-electrolyte interface, causing a potential difference referred to as half-cell potential. Since the biopotential electrodes exhibit mismatches in reality, the half-cell potentials give rise to a differential DC electrode voltage offset (DEO) which can be quite large ($\sim$ 50mV). To illustrate this effect, we can use a circuit model for the biopotential electrode, as depicted in Fig. 1.2. C_A and R_A represent the electrode impedance, R_s is the resistance of the electrolyte solution and V_{hc} is the half-cell potential. Depending on the neural signal of interest, different electrode types with distinct impedances could be used. For ECoG, the electrode impedance is typically between 1 kΩ to 5 kΩ and for EEG, the electrode impedance is roughly a few MΩ and can be reduced to a few kΩ by applying a gel between the scalp and the electrode.

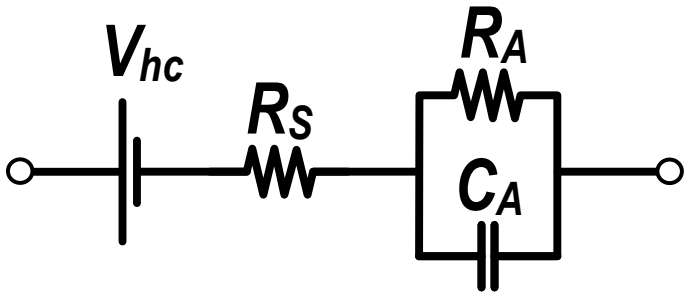

Figure 1.2: Biopotential electrode circuit model.

1.3.3 Biosignal Recording

The bioamplifier provides the low-noise amplification of ECoG signal while drawing minimum current from the supply to reduce the power burden in a multi-channel acquisition system. In addition, the bioamplifier needs to filter out the DEO, reject the common-mode interference, and exhibit high input impedance to minimize the differential error caused by the impedance mismatch. In this section, a brief review of prior works is presented.

Numerous designs of bioamplifiers have been reported in the past and the purpose of this section is not to present a comprehensive survey but rather focus on the key design aspects of selected works which have proven effective. As mentioned, DEO is inevitable in biomedical signal acquisition systems and hence, it needs to be filtered out to avoid amplifier saturation. Passive components such as capacitor and resistor can be used to create the high-pass filter but require significant area which is impractical for a multi-channel acquisition system. R. Harrison et al. [13] used a MOS-bipolar pseudoresistor element in the feedback path of a capacitively-coupled amplifier to realize the low-frequency high-pass corner. This is an effective method for rejecting DEO as it eliminates the need for a very large resistor at the cost of linearity and process variation.

An obvious concern with low-frequency operation of MOS transistors is the presence of flicker (1/f) noise. To reduce the 1/f noise contribution, transistor sizing can be increased but this approach creates an area overhead. A. Avestruz et al. [14] purposed an AC-coupled chopper amplifier to minimize the 1/f noise. This design utilizes a switched capacitor integrator in the feedback path to create the high-pass corner and uses capacitive feedback to set the midband gain accurately. The chopping before the input capacitor (C_{in}) of the OTA generates a parasitic resistor which reduces the overall input impedance significantly. In another implementation by N. Verma et al. [15], chopper switches are placed at the virtual ground node of the OTA. However, this will cause the parasitic switched capacitor resistor

to form a high-pass filter with C_{in}, necessitating careful design of the input capacitor and an area overhead. In a different approach, R. Muller et al. [16] proposed to use a mixed-signal feedback to realize the high-pass corner. This architecture employs an open-loop chopper amplifier, delta-sigma modulated capacitive DAC and ADC. The input offset is cancelled through the mixed-signal servo-loop which is only active at DC. This is advantageous since the input impedance can be much higher at the in-band frequency, $Z_{in} = 1/(4f_{chop}(C_{DAC} + C_{PAR}))$, compared to $Z_{in} = 1/(2f_{chop} \cdot C_{in})$ at DC.

To further reduce the noise contribution at lowest power consumption, several works have employed different current-reusing techniques to boost the overall amplifier transconductance, g_m but without increasing the bias current. This merit is captured in the noise efficiency factor (NEF) [17], defined by:

$$NEF = V_{rms,in}\sqrt{\frac{2I_{tot}}{\pi U_T \cdot 4kT \cdot BW}} \tag{1.1}$$

where $V_{in,rms}$ is the input-referred noise voltage of the amplifier, I_{tot} is the total current dissipated by the amplifier, U_T is the thermal voltage, kT is the product of Boltzmann constant and temperature, and BW is the amplifier's bandwidth in Hz. NEF is used to compare different amplifier topologies and represents the factor by which noise is greater compared to an ideal single bipolar junction transistor (BJT) with the same total current and bandwidth. As such, the theoretical limit is 1 for single-ended and 2 for a differential pair of BJTs. The inverter-based amplifier [18] is the simplest structure employing current-reuse. B. Johnson and A. Molnar [19] applied transistor stacking to share bias current among the input differential pairs of four amplifiers. In this approach, the bias current for each channel's differential pair is generated by the output drain currents of the preceding channel's differential pair in an orthogonal fashion. Since this technique involves combining $2 \cdot N$ branches at the output for N-channel inputs, it creates an increased complexity and power of the peripheral circuits in high channel-count systems, thus degrading NEF. Y. Chen et

al. [20] applied multi-chopping to current-reusing technique to further improve NEF but the number of chopper switches represents a trade-off between signal bandwidth and Gaussian noise. F. Yaul and A. Chandrakasan [21] proposed the "squeezed-inverter" structure in which the N-type and P-type transistors have separate bias voltages, allowing the supply voltage to be reduced. As a result, this amplifier structure can achieve an improved power efficiency factor (PEF) defined as $NEF^2 \cdot V_{DD}$ where V_{DD} represents the supply voltage. Most recently, L. Shen et al. [22] have reported one of the best NEF to date by utilizing multiple inverter stacking approaches.

An important design consideration in bi-directional BMI systems is the presence of stimulation artifact which could saturate the amplifiers. H. Chandrakumar and D. Markovic [23] used an auxiliary amplifier at the input to cancel the large-signal common-mode artifact. They also utilized the auxiliary-path technique to boost the input impedance as opposed to the positive feedback loop technique [24] which suffers from stability issues. It is worth noting that the differential- and common-mode artifacts can also be suppressed by template subtraction [25] at the cost of increased complexity.

1.4 Dissertation Outline

This chapter provided the motivation and system overview of the proposed fully-implantable BMI to restore walking in patients with spinal cord injury. A brief review of the fundamentals in brain signals, biopotential electrodes and biosignal recording was presented, which serves as a prelude to neural signal acquisition studied comprehensively in this work.

Chapter 2 introduces the dual-mode array architecture for HD-ECoG implantable BMIs, providing a detailed description of the proposed approach and demonstrating a fabricated prototype in 180nm CMOS process. The design, implementation and human testing of a dual-mode 32-channel signal acquisition front-end chip, capable of acquiring and pre-processing of ECoG signals, is further discussed in Chapter 2.

Chapter 3 presents an ultra-low power mixed-signal neural data acquisition system that enables a novel low-power hybrid-domain neural decoding architecture for implantable BMIs with high channel-count. A fully-integrated chip in 180nm CMOS technology is demonstrated, providing a proof-of-concept for future use in implantable BMIs. The design, implementation and human testing of the fabricated prototype are further discussed in Chapter 3.

Chapter 4 studies the common-mode interference phenomenon frequently encountered in multi-channel biosignal recording systems employing a shared-reference scheme. A detailed analysis of the common-mode rejection is presented using an equivalent electrical circuit model of the input interface consisting of an electrode array and differential bioamplifiers.

Chapter 2

Dual-Mode Array Architecture for High-Density ECoG-Based BMIs

2.1 Introduction

Approximately 330,000 people are living with chronic spinal cord injury (SCI) in the US alone, and currently there are no biomedical approaches capable of restoring motor function after SCI. Recent advances in neurophysiology and nanoscale electronics have made it possible to realize fully implantable brain-machine interfaces (BMIs) for medical applications. Large-scale miniaturized ECoG arrays are considered to be a promising signal platform for fully implantable BMIs due to their signal stability, high signal-to-noise ratio (SNR) and spatial resolution [26, 27]. However, these favorable attributes often come at the expense of excessive power consumption. Therefore, energy efficient BMI architectures inspired by prior studies of human motor control are of high interest to make such invasive BMIs a clinical reality.

It is perceived that the primary motor cortex, M1, encodes high-level kinematic parameters

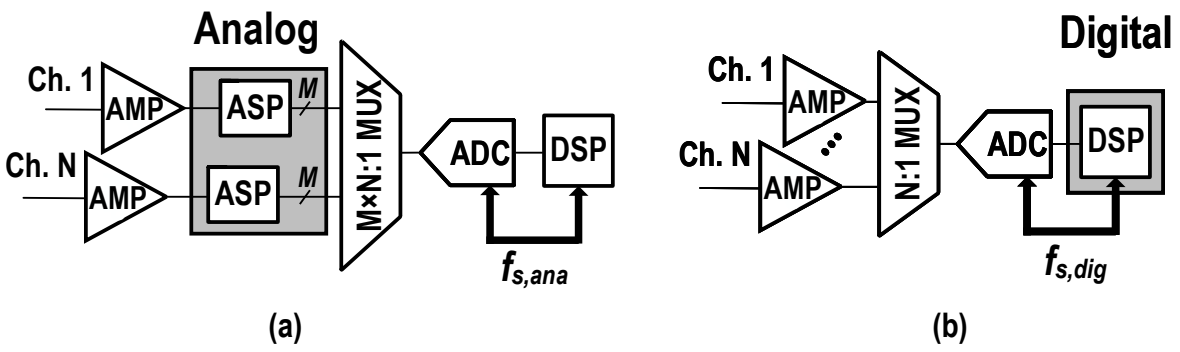

Figure 2.1: Existing architectures for multi-channel feature extraction in brain-machine interfaces based on (a) analog and (b) digital signal processing.

for upper and lower extremity movements (i.e., duration and speed), and interacts with subcortical/spinal networks that execute low-level motor control (i.e., muscle activation or movement trajectories) [1, 28, 29, 30, 31]. High spatiotemporal resolution ECoG recordings from M1 contain rich movement information related to upper and lower extremities in γ-band [8, 9, 10, 11]. In particular, high-γ (80-160 Hz) band exhibits consistent changes in power levels during movement and idle states [1], and thus these patterns can be utilized as the central neural features to enable practical BMIs for prosthetic control in SCI patients.

Shown in Figs. 2.1(a)-(b) are general block diagrams of the analog- and digital-based multi-channel architectures, each comprised of an N-channel front-end, a multiplexer, and a mixed-signal and digital back-end.

The analog-based architecture utilizes analog signal processing (ASP) to form an M-element neural-feature vector based on spectral decomposition [14, 32, 33]. Although this approach reduces the signal bandwidth and lowers the sampling rate (f_s) of the mixed-signal and digital back-ends, it has several limitations at the circuit- and architecture-level. For example, an analog neural spectral-processing integrated circuit is implemented in [14] for M=4 that amplifies and processes neuronal activity with variable bandwidth and power filtering characteristics. The signal chain includes a power-hungry tunable heterodyning amplifier based on a dual-nested chopper architecture, which suffers from a limited input impedance and

requires an anti-alias filter. An analog energy extractor for local field potential is introduced in [32] for M=6, which allows for a compact design and low power consumption. However, this approach offers limited degree of freedom to control the selectivity and sensitivity of the transfer characteristics of the filters used as part of the energy extractor. [33] reports a single-channel neural recording prototype, capable of extracting sub-banded energy across four (M=4) different frequency bands. This architecture utilizes a power-hungry variable gain amplifier to satisfy the dynamic range and settling requirements of discrete-time signal conditioning and digitization. To avoid anti-aliasing in the sampled-data system, it allows for limited tuning of each sub-band parameters which are controlled by the clock frequency. Moreover, a complex switching matrix can be employed to share the bulky energy extractors in multi-channel acquisition, which is not amenable to large-scale neural recording.

The digital-based multi-channel architecture implements the neural feature extraction entirely in the digital back-end [15], as shown in Fig. 2.1(b). This approach requires higher f_s compared to the analog-based architecture due to a significantly larger bandwidth of raw ECoG signal, resulting in higher dynamic power dissipation. Although power and clock gating techniques can be applied to reduce the power consumption, it is still advantageous to avoid the data-processing power bottleneck by limiting the signal bandwidth before multiplexing/digitization.

Inspired by our work in [1], this chapter presents a scalable dual-mode array architecture which exploits ultra-low power (ULP) ASP to extract relevant neural features of ECoG signals to enable prosthetic control in implantable BMIs. The rest of this chapter is organized as follows. Section 2.2 discusses the system-level specifications and implications of neural feature extraction. Section 2.3 presents the proposed dual-mode array architecture. Section 2.4 describes the circuit design and analysis. Section 2.5 presents experimental results including electrical and human neurological measurements. Section 2.6 concludes this chapter.

2.2 System-Level Considerations and Implications

In this section, we discuss important challenges in state-of-the-art ECoG-based implantable BMIs and investigate the system-level specifications and implications.

First, the input-referred integrated RMS noise from the front-end amplifier should fall below the cortical background noise ($\sim$5-10μV) to allow for high-fidelity signal acquisition [34]. Second, to reduce the power-line 50/60-Hz interference, the common-mode rejection ratio (CMRR) of the amplifier is desired to be larger than 70dB [35]. Third, for multi-channel acquisition with a common-reference electrode that has comparable impedance to channel electrode's, the input impedance must be large enough ($>>$ 1MΩ) to avoid any signal attenuation and CMRR degradation. Finally, to satisfy the thermal dissipation requirement in the vicinity of the brain, it is crucial to reduce the overall power consumption of the multi-channel neural recording to keep the temperature increase below 1°C.

An effective approach to extend the longevity in battery-powered implantable BMIs is to exploit the unique characteristics of ECoG signal. It has been observed that power spectral density of ECoG signals attenuates with frequency [36], and therefore, it spans a wide dynamic range ($\sim$48 dB across 2-200 Hz). While spectral equalization helps reduce the dynamic range, relax the resolution requirement and achieve power-saving in the front-end and mixed-signal blocks, there is still a major bottleneck due to the mandated compute-intensive and power-hungry statistical data processing in the digital back-end. [1] studied the important signal characteristics of raw ECoG and power envelopes during walk and idle states. Fig. 2.2 shows raw ECoG, γ-band, and its power envelopes (P_γ). As can be seen, changes in P_γ exhibit distinguishable amplitude-modulated voltage variations between walk and idle states which occur in time scale of seconds, implying that both sampling rate and resolution requirements can be significantly relaxed for such signals compared to raw ECoG. These attributes suggest that extracting neural features early in the signal chain using a distinct

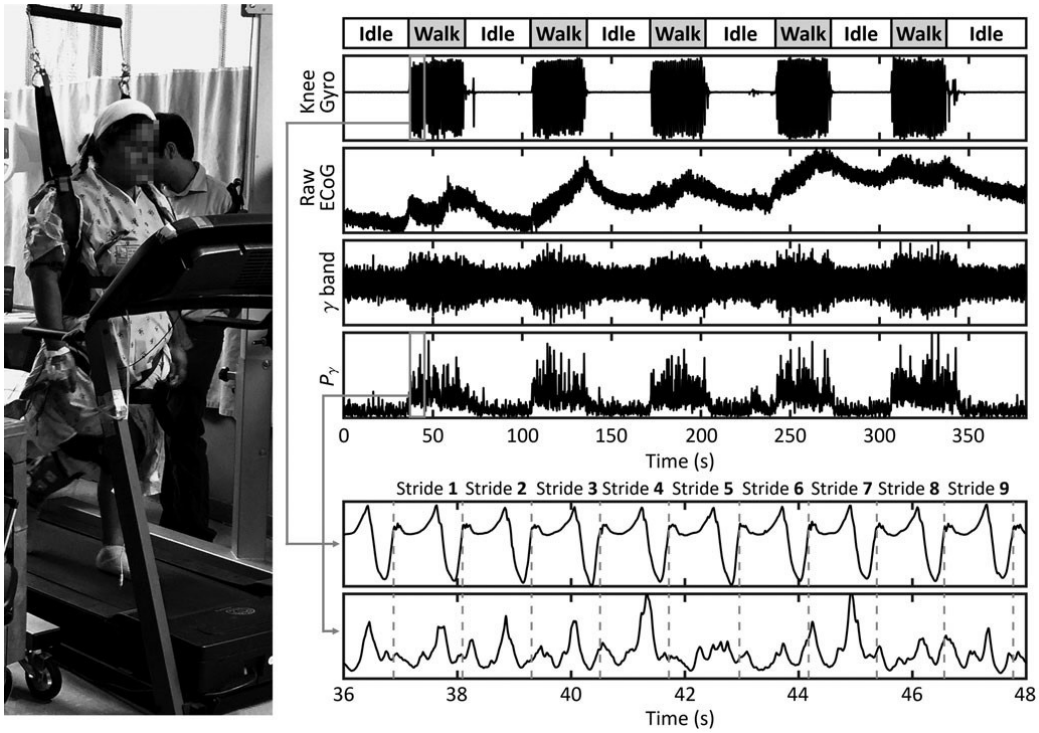

Figure 2.2: Example of the experimental setup and signal processing steps used for recording of motor cortical activity with ECoG grid during a causal walking task. Data from knee gyroscope, ECoG data in its raw, γ-band filtered and power envelopes (P_γ) are shown. A close-up of P_γ and knee gyro signals is illustrated for comparison during individual gait cycles [1].

signal pathway is highly beneficial to minimize the system power dissipation, leading to an energy-efficient neural recording architecture.

2.3 Proposed Dual-Mode Array Architecture

Given that power envelopes of γ-band can be used to decode movement intentions [1], it is sensible to use a single envelope detector in the analog domain to produce low-bandwidth features for clustering and classification in the digital back-end. However, based on prior work [8, 9, 10, 11], a specific frequency range within γ-band needs to be identified by human training and data collection/processing of raw ECoG for decoding. Therefore, the front-end

circuitry should be capable of acquiring raw ECoG signal and extracting the power envelopes within this identified frequency range. This notion calls for a dual-mode approach to neural recording with two distinct regimes of operation: (1) full-band (FB) mode for raw ECoG signal acquisition with moderate-resolution (8-10 bits) and high sampling rate $f_{s,FB}$ (>13 kS/s), and (2) base-band (BB) mode for power envelope extraction with low-resolution (3-4 bits) and significantly reduced sampling rate $f_{s,BB}$ (>260 S/s). Initially, brain activity across the full-spectrum is momentarily observed during the FB mode operation to compute the feature weights in the digital back-end. Subsequently, these weights are fed back to the front-end and the system reverts to BB mode to perform feature extraction. While an implantable high-density ECoG-based BMI needs the FB data for training, calibration and validation purposes, it will primarily operate in BB mode for prosthetic control which accounts for majority of the time.

Fig. 2.3(a) shows the proposed dual-mode array architecture. The 32-channel signal acquisition system consists of a 32-element dual-mode front-end (DMFE) array, FB/BB time-multiplexers (MUXs), a programmable-gain instrumentation amplifier (InAMP), and FB/BB output buffers (Buffs), a serial peripheral interface (SPI) and a digital circuitry (DIG). The system communicates with the back-end (i.e., DSP or host PC) via SPI, which provides access to internal registers to update feature weights, and select operation mode (FB/BB) or acquisition method (either channel-specific or multiplexed). The latter option is employed to acquire signals from one specific channel or all channels during each operation mode.

To study the power-saving advantage of the proposed architecture in Fig. 2.3, a simple power analysis is presented. Biased to operate in subthreshold region, each DMFE includes a front-end amplifier (AMP) and neural pre-processing (NP^2) module with power consumption of P_U and P_{NP^2}, respectively. Following the FB MUX, m stages of post-multiplexing amplification/buffering are employed with N-times higher bandwidth compared to the front-end amplifier (N denotes the number of channels). Assuming unity-gain bandwidth product

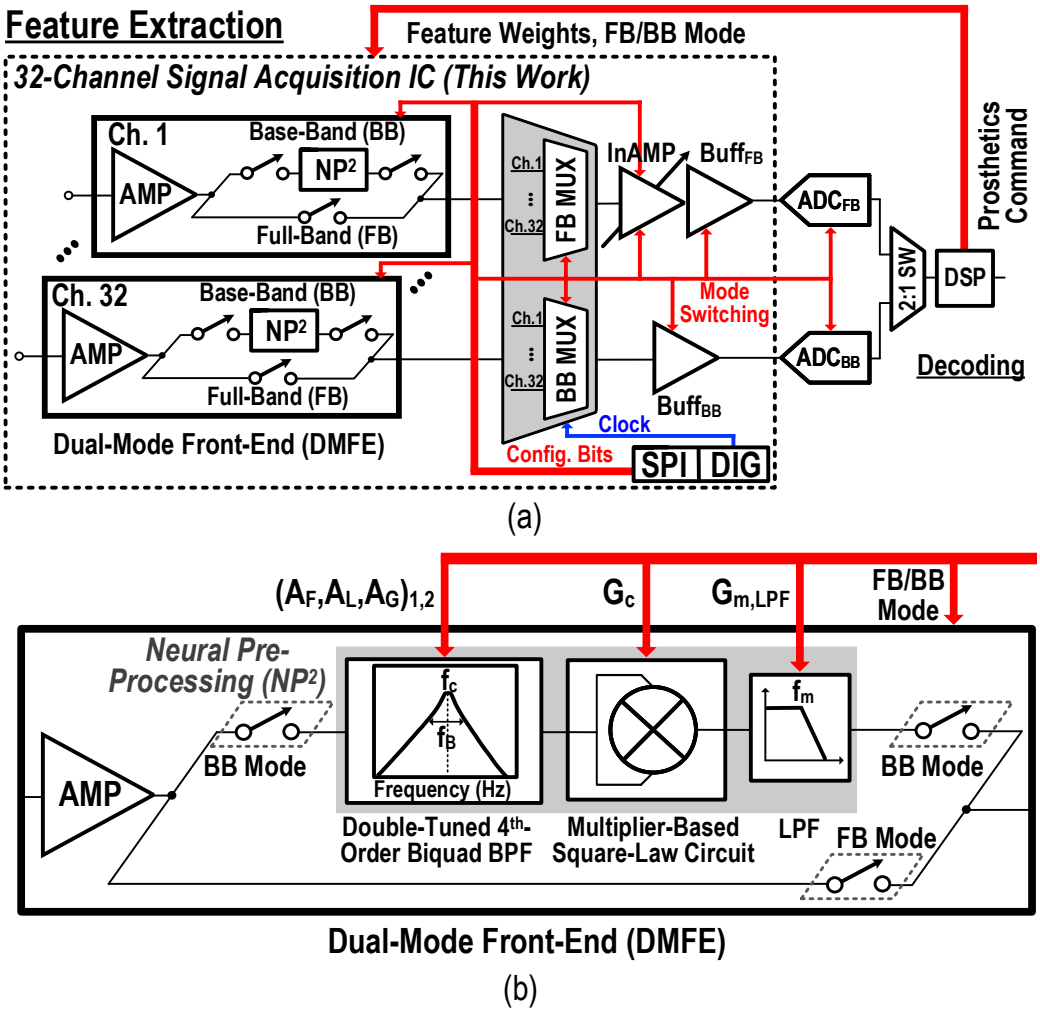

Figure 2.3: Proposed dual-mode array architecture: (a) overall system diagram (b) dual-mode front-end module.

varies linearly with bias current in weak-inversion, each post-multiplexing gain stage approximately consumes $N \cdot P_U$ (to the first-order). Assuming a bandwidth reduction factor of η for the BB operation mode compared to the FB counterpart, the power consumption of the BB output buffer is approximately $N \cdot (\eta P_U)$. Specifically, neural signals in FB mode and extracted features in BB mode occupy a bandwidth of ∼200 Hz and ∼4 Hz per channel, respectively, resulting in $\eta \approx 0.02$. Moreover, the total dynamic power dissipation of MUX, ADC and DSP is represented by P_D for FB mode and ηP_D for BB mode. While FB operation requires multiplexing, post-multiplexing amplification/buffering, digitization

and post-processing with an excessive bandwidth and power consumption, BB operation achieves significant power-saving in the respective blocks with minimum power overhead, P_{NP^2}, in DMFE. To deduce the power-saving advantage, the ratio of system powers $P_{sys,FB}$ and $P_{sys,BB}$ in FB and BB modes is calculated, as follows:

$$\frac{P_{sys,FB}}{P_{sys,BB}} \approx \frac{N \cdot P_U(1+m) + P_D}{N \cdot [P_U(1+\eta) + P_{NP^2}] + \eta \cdot P_D} \tag{2.1}$$

Given $f_{s,BB} = \eta f_{s,FB}$, BB MUX consumes proportionally less dynamic power compared to FB MUX. Furthermore, the power consumption of BB ADC is reduced compared to that of FB ADC due to decreased sampling rate and resolution [37]. It is expected that at low-SNR (<5-bit resolution), component matching and/or minimum realizable capacitance will impose a limit on power dissipation. However, low-bandwidth processing still continues to improve the overall system power consumption. This notion proves to be important for DSP in BB mode as dynamic powers associated with processing ($\propto f_{s,BB}^k$ where k denotes the algorithm complexity) and memory accesses ($\propto f_{s,BB}$) are reduced significantly [38]. For a quantitative comparison, ULP ADCs and DSP from literature are used to evaluate Eq. (2.1) for N=32 and m=2. Reported ULP ADCs consume as small as 2.7nW for 1kS/s with 6-bit resolution (BB ADC) and 97nW for 40kS/s with 10-bit resolution (FB ADC) [39]. On the other hand, commercially available DSPs (e.g., C5517 by Texas Instruments) consume milliwatt-level power. Since the desired input-referred noise typically requires P_U to be greater than a few μW and P_{NP^2} introduces a small overhead, the second terms in the numerator and denominator of (2.1) will dominate $P_{sys,FB}$ and $P_{sys,BB}$, and the power-saving advantage will thus be significant ($\sim \frac{1}{\eta} = 50$). It is noteworthy that an activity-based mechanism realized in the digital back-end will allow for further power-cycling of BB mode during extended idling periods (i.e., night-time sleep).

To allow differential recording of neural signals with respect to a common-reference electrode from ECoG grid, each AMP employs a fully-differential topology. Considering that the differential input impedance of AMP is approximately equal to 295MΩ at 60Hz (C_{in}=18pF) and assuming 1kΩ electrode impedance with N=32, the input interface CMRR of a common-reference scheme with similar recording and reference electrode impedance reaches 79.5dB. However, the overall CMRR is still limited by AMP to 76.5dB as reported in Section 2.5.1. Two switchable pathways are incorporated for dual-mode operation. In FB mode, the amplified signals are multiplexed using FB MUX with fast reset switches to mitigate the channel ghosting and eliminate large artifact residues (Section 2.4.2). The multiplexed output is further amplified, digitized by FB ADC (off-chip in this work), and processed by the external digital back-end. In BB mode, NP^2 module performs feature extraction on amplified neural signals based on the appropriate feature weights computed in the back-end (*cf.* Fig. 2.3(a) and (b)). Extracted power envelopes are then multiplexed and digitized by off-chip BB ADC prior to digital processing. Shaded in Fig. 2.3(b), NP^2 module carries out two main operations: band-pass filtering (BPF) and envelope detection using power extraction and averaging. A double-tuned fourth-order biquad realizes the BPF to capture high-γ-band modulations. The center frequency f_c and bandwidth f_B (hence, the quality factor Q) of the BPF are adjusted via A_F, A_L and A_G parameters to achieve better selectivity, reduced pass-band ripple and high out-of-band attenuation (Section 2.4.1). A multiplier-based square-law circuit performs analog multiplication to obtain signal power and its conversion gain, G_c, is optimized with respect to the input level to minimize signal-dependent noise folding and voltage offsets (Section 2.4.3). Lastly, a low-pass filter (LPF) with a corner frequency of f_m extracts power envelopes that modulate high-γ-band signals. To match the characteristic time scale of ECoG signals during movements, f_m is adjusted via $G_{m,LPF}$.

2.4 Circuit Design and Analysis

2.4.1 Dual-Mode Front-End Design

Fig. 2.3(b) shows the block diagram of the proposed DMFE. Based on our earlier work in [35], AMP is realized by an operational transconductance amplifier (OTA) within a capacitive feedback loop, which uses a differential stage with regenerative load to boost the open-loop gain. The mid-band gain is set to 40 dB and the frequency response exhibits a high-pass corner of ∼2 Hz and a low-pass corner of ∼200 Hz. All active and passive components within AMP are adequately sized to minimize mismatch and process variations to attain high CMRR. To improve the common-mode output resistance of tail current source in AMP (see Amplifier II in [35]), and hence the CMRR, supply voltage in this design is increased to 0.8V to allow a higher drain-source voltage for a given bias current.

Figs. 2.4(a)-(b) depicts detailed realization of NP^2 module. The fourth-order Butterworth BPF is realized by cascading two biquad G_m-C filters and an interstage LPF buffer with high corner frequency to avoid loading effect of the second biquad. The filter characteristics of each biquad section with center frequency, $f_{0,k}$, bandwidth, BW_k, and mid-band gain, $H_{mid,k}$ for $k = 1, 2$, are derived as follows:

$$f_{0,k} = \frac{1}{\sqrt{A_{G,k}A_{L,k}(A_{F,k} + 1 + \frac{A_{F,k}}{A_{L,k}})}} \frac{G_{mF,k}}{2\pi C_F} \tag{2.2}$$

$$BW_k = \frac{A_{L,k} + A_{G,k}}{A_{G,k}A_{L,k}(A_{F,k} + 1 + \frac{A_{F,k}}{A_{L,k}})} \frac{G_{mF,k}}{2\pi C_F} \tag{2.3}$$

$$H_{mid,k} \approx \frac{A_{F,k}}{1 + \frac{A_{L,k}}{A_{G,k}}} \tag{2.4}$$

where $A_{F,k} = C_k/C_F$, $A_{L,k} = 2C_{L,k}/C_F$ and $A_{G,k} = G_{mF,k}/G_{mB,k}$ for $k = 1, 2$. While 80-160 Hz is designated in this work to be the maximum frequency range of interest, the desired

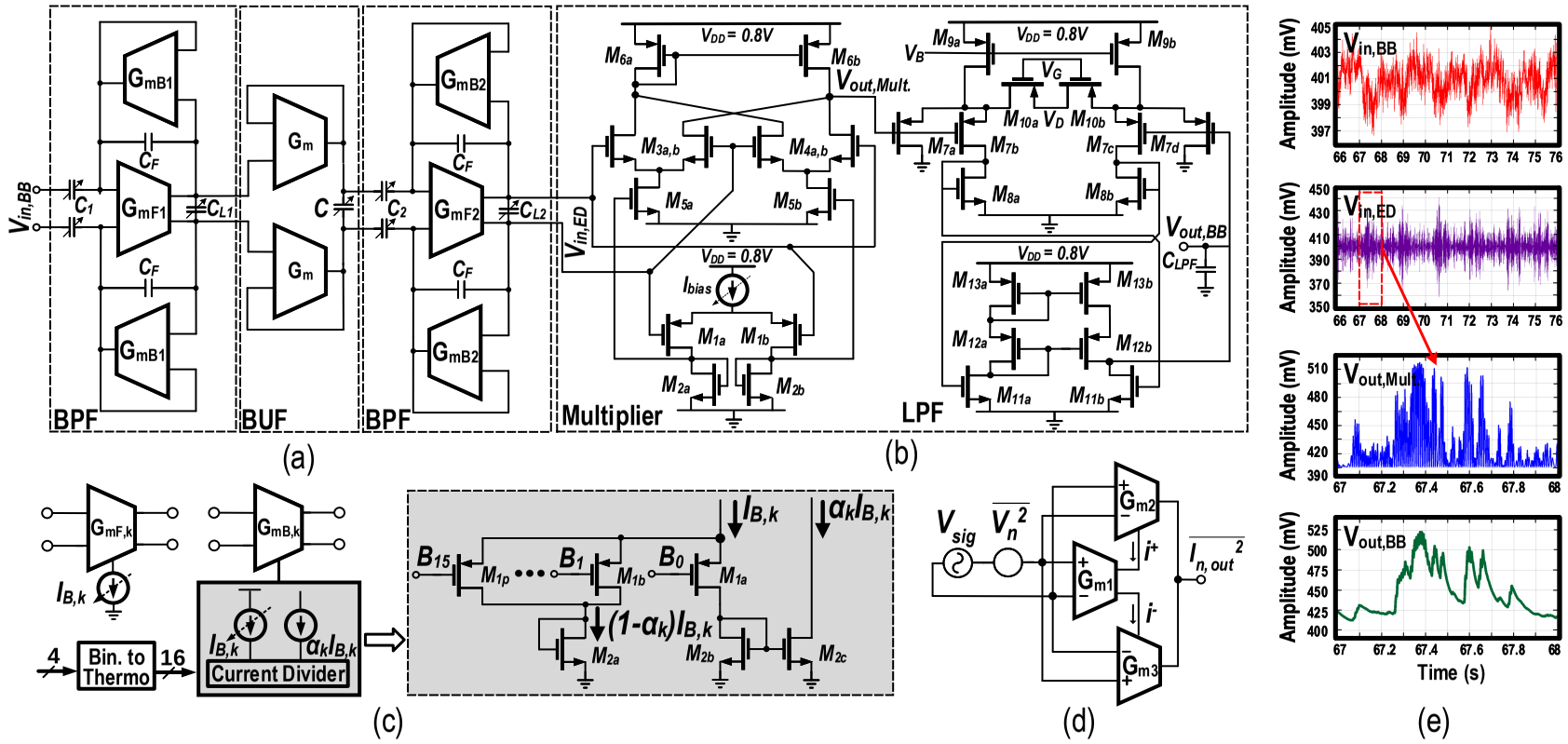

Figure 2.4: Neural pre-processing module including (a) double-tuned 4th-order filter, (b) multiplier-based envelope detector, and (c) G_m bias tuning and current division circuitry. (d) Block diagram model of Gilbert cell for noise analysis. (e) Voltage waveforms from each stage of neural pre-processing.

neural features may reside within a narrower range of this band. Each BPF is designed to allow for the required flexibility in frequency-range selection by tuning these parameters, which are represented by the ratios of the same physical quantity. Therefore, they are less prone to process/mismatch variation; an essential feature required in large-scale systems. On the other hand, $G_{mF,k}/C_F$ in (2.2) and (2.3) is more susceptible to the process variation, which is calibrated in an open loop fashion by varying $G_{mF,k}$ through a tunable bias current (7-bit current bank), $I_{B,k}$ for $k = 1, 2$, as shown in Fig. 2.4(c). While this digital calibration incurs an area overhead that could be further addressed by sharing the same bias current locally among a cluster of channels in favor of reduced die area, it alleviates the testing time and complexity associated with off-chip current trimming in large-scale systems.

To control $A_{G,k}$, the bias current of $G_{mB,k}$ cell is obtained from a current divider that takes a reference current of $I_{B,k}$ and produces $\alpha_k I_{B,k}$, where α_k denotes the division factor for $k = 1, 2$. Bias tuning of $G_{mB,k}$ is achieved by converting a 4-bit binary code to a 16-bit thermometer code which is applied to current divider. Shaded in Fig. 2.4(c), a digitally controlled current division circuitry is implemented using parallel PMOS switches, M_{1a-1p}, a diode-connected transistor, M_{2a}, and a current mirror, $M_{2b,c}$. Each switch acts as a small parallel resistor when it is ON and as an open-circuit with minimal leakage current when it is OFF. All PMOS switches have an equal output resistance except for M_{1a} whose drain-source voltage may differ slightly from M_{1b-1p}. Fig. 2.5 shows the ideal and realized transfer characteristics of current divider. α_k is swept across every digital code from 0000 to 1111, which scales $I_{B,k}$ ($\sim$680pA) by α varying from 1 to 1/16. For a maximum division factor of 1/16, the output current exhibits less than 6% error at $\sim$42.5pA. To accommodate wide tunability of $A_{F,k}$ and $A_{L,k}$, each C_k and $C_{L,k}$ is realized by a 4-bit binary-weighted capacitor bank for $k = 1, 2$. Since independent tuning of $f_{0,k}$ and BW_k is not viable, a look-up table is generated off-line based on (2.2)-(2.4) for all possible combinations of $A_{F,k}$, $A_{L,k}$ and $A_{G,k}$ which spans the entire solution space. Thereafter, a subset of the solution space which satisfies the desired specifications for $f_{0,k}$, BW_k, and $H_{mid,k}$ for $k = 1, 2$ is found using brute-

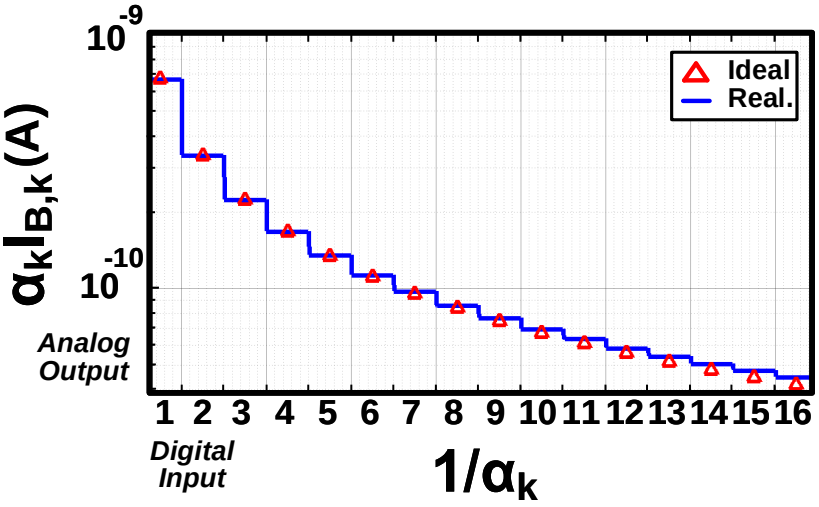

Figure 2.5: Linearity of current divider (ideal versus realized).

force search. Controlled by the digital back-end, this look-up table approach allows for a robust mechanism to extract neural features by reconfiguring the parameters $A_{F,k}$, $A_{L,k}$, $A_{G,k}$, G_c, and $G_{m,LPF}$. It is worth mentioning that only one lookup table is used for all channels since the same neural features are extracted from each one.

Shown in Fig. 2.4(b), the envelope detector consists of a four-quadrant multiplier (Gilbert cell) and a source-degenerated OTA-C filter. Both multiplier and OTA-C filter use current folding technique to limit transistor stacking and operate with low supply voltage. A 4-bit binary-weighted current source is used to vary I_{bias} and adjust the conversion gain of the multiplier. Transistors $M_{9a,b}$ mirror the current from a 4-bit binary-weighted current source to allow tunability of transconductance, $G_{m,LPF}$, in OTA-C filter. To achieve a corner frequency of a few Hz, source-degeneration and current splitting are applied to M_{7a-d} to greatly reduce $G_{m,LPF}$. The voltage waveforms at constituent stages of neural pre-processing from a recorded ECoG signal are shown in Fig. 2.4(e). Fig. 2.6 shows the frequency response of the double-tuned 4th-order biquad filter with a center frequency of 120 Hz and bandwidth of 80 Hz and degnerated low-pass filter with a 3-dB corner frequency of 4 Hz.

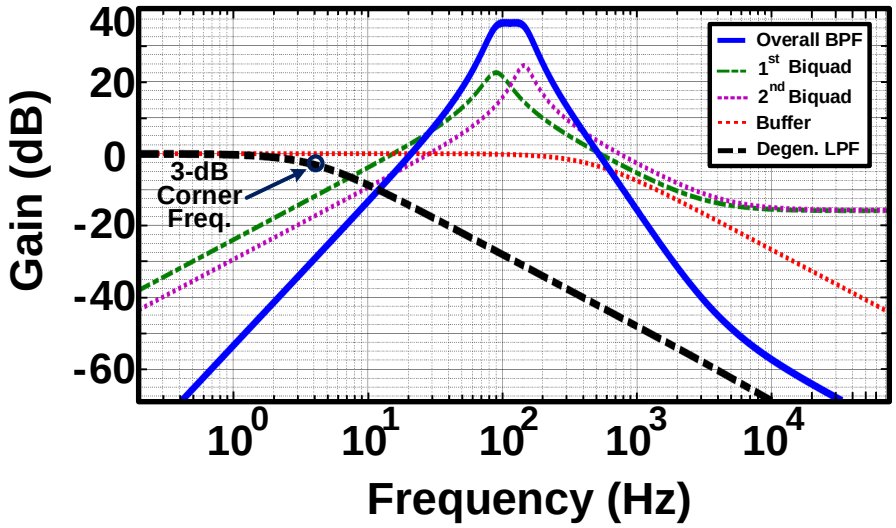

Figure 2.6: Frequency response of double-tuned fourth order band-pass and degenerated low-pass filter.

2.4.2 Post-Multiplexing and Interfacing Modules Design

Similar to [35], an external clock is provided to generate non-overlapping clocks (CLK_{1-32}) with 1/64 duty-cycle for FB/BB channel multiplexing with an additional option to select individual channels. In FB mode, a digitally-programmable InAMP is used to accommodate 20–40 dB of additional post-multiplexing amplification with 3dB gain steps. Shown in Fig. 2.7(a), the AC-coupling network with approximately 2-Hz highpass corner frequency is employed between AMP and InAMP to filter out the voltage offset introduced by each AMP during single-channel acquisition. For multi-channel acquisition, in order to avoid large transients during channel-multiplexing, a reset/bootstrap mechanism is introduced to the AC-coupling network in FB MUX. This is achieved by applying CLK_{FB} to reset switches during the non-overlapping intervals (T_R), which ensures that the output voltage stays at reference voltage V_{ref} after each channel switching. To mitigate the long settling time of AC-coupling network, an auxiliary pair of switches is used to bootstrap the voltages across the AC-coupling capacitors to V_{ref}. It is noteworthy that the AC-coupling network is rendered ineffective in multi-channel acquisition due to the reset/bootstrap operation. Each

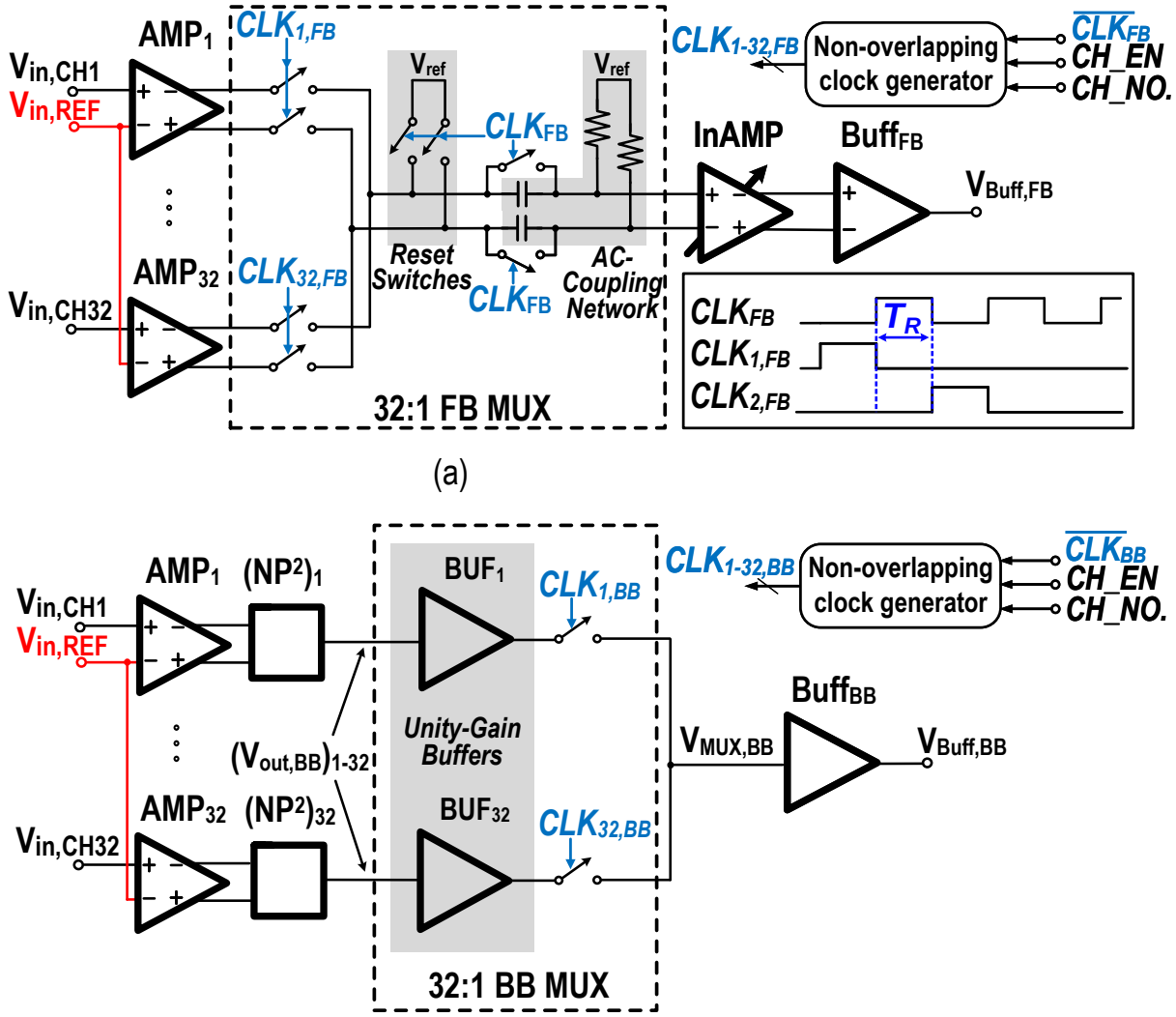

Figure 2.7: Multiplexing operation: (a) full-band (b) base-band.

switch is realized by a T-network of transmission gates with dummy devices to mitigate charge-injection and clock-feedthrough effects. Fig. 2.7(b) indicates the multiplexing operation in BB mode. No additional gain is required after envelope detection. Nevertheless, a unity-gain buffer is placed before BB MUX switch to buffer the high-impedance output node of envelope detector ($V_{out,BB}$) from the shared multiplexed output node ($V_{MUX,BB}$). FB/BB output buffers are used to drive an external ADC in this implementation.

2.4.3 Noise Analysis of Multiplier-Based Square-Law Circuit

In this section, noise interactions that happen in the multiplier-based envelope detector are further studied. The Gilbert-cell multiplier of Fig. 2.4(b) is modeled as three transconductors, G_{m1}, G_{m2} and G_{m3} in Fig. 2.4(d). It is evident that small-signal multiplication is achieved by applying a small AC signal (i^+/i^-) to each bias current of G_{m2} and G_{m3}. The filtered neural signal and noise contributions from the previous stages are represented by V_{sig} and $\overline{V_n^2}$, respectively. Due to the non-linear behavior of analog multiplier, signal and noise at the input undergo multiplication that results in an increased noise power. Three major sources of noise contribution are identified in a multiplier-based envelope detector [40]: (a) signal-dependent noise due to mixing between signal and noise, (b) noise self-mixing due to mixing of noise with itself, and (c) intrinsic circuit noise, which is the sum of all existing device noise (e.g., thermal and flicker noise) powers in the envelope detector. Therefore, the total current noise power at the output of envelope detector $\overline{I_{n,out}^2}$ is expressed, as follows:

$$\overline{I_{n,out}^2} = \overline{I_{n,sig}^2} + \overline{I_{n,n}^2} + \overline{I_{n,ED}^2} \tag{2.5}$$

where $\overline{I_{n,sig}^2}$, $\overline{I_{n,n}^2}$, $\overline{I_{n,ED}^2}$ represent the signal-dependent, self-mixing, envelope detector current noise powers. As discussed, high-γ brain signals are observed to be amplitude modulated (AM) during kinetic movements, which can be thought of as a carrier signal with an underlying modulating function. This AM signal is assumed to be a sinusoidal carrier f_c at the center of high-γ-band whose average power, $A_c^2/2$, is equivalent to the total signal power within the band modulated by a normalized baseband function, $m(t)$, whose modulation frequency and index are defined by f_m and a_m, respectively. Hence, the signal at the input of multiplier is readily expressed, as follows:

$$V_{sig,AM} = A_c[1 + a_m m(t)]\cos(2\pi f_c t) \tag{2.6}$$

It is observed that power spectral density of brain signals follows a $(\frac{1}{f})^p$ characteristic where $p = 2 \sim 4$ [36]. Thus, the total signal power $(\frac{A}{f})^p$ across the high-γ bandwidth f_B is calculated by integration, as follows:

$$\overline{V_{sig,\gamma}^2} = \int_{f_c-0.5f_B}^{f_c+0.5f_B} (\frac{A}{f})^p \, df = \frac{A^p}{(-p+1)} f^{(-p+1)} \Big|_{f_c-0.5f_B}^{f_c+0.5f_B} \tag{2.7}$$

The average noise power from the front-end circuitry preceding the multiplier, $\overline{V_n^2}$, is obtained by integrating the overall power spectral density of all noise sources (i.e., thermal and flicker noise) over f_B. As such, the equivalent white power spectral density, $\overline{V_n^2}/f_B$, is readily used to calculate the output noise of the envelope detector across the LPF bandwidth of f_m. Assuming $m(t)$ has zero average value, $\overline{I_{n,sig}^2}$ and $\overline{I_{n,n}^2}$ are thus derived, as follows:

$$\overline{I_{n,sig}^2} = 6G_c^2 \overline{V_{sig,\gamma}^2}[1 + a_m^2 \overline{m^2(t)}] \frac{f_m}{f_B} \overline{V_n^2} \tag{2.8}$$

$$\overline{I_{n,n}^2} = 3G_c^2 \frac{f_m}{f_B} (\overline{V_n^2})^2 \tag{2.9}$$

where G_c $\big(= I_{bias}/(2nV_{th})^2$, where n represents sub-threshold slope$\big)$ is conversion gain of the multiplier.

The envelope detector average current noise power, $\overline{I_{n,ED}^2}$, is found by summing the thermal and flicker noise contributions of transistors (M_{1-6}), shown in Fig. 2.4(b), and integrating its noise power spectral density over the bandwidth f_m:

$$\begin{aligned}\overline{I_{n,ED}^2} &= 8kT\gamma(g_{m1} + 2g_{m2} + 2g_{m3} + g_{m6})f_m \\ &+ \frac{2K_p}{C_{ox}(WL)_1}\left[g_{m1}^2 + \frac{K_n(WL)_1}{K_p(WL)_2}(2g_{m2})^2 + \frac{K_n(WL)_1}{K_p(WL)_3}(2g_{m3})^2 + \frac{(WL)_1}{(WL)_6}(g_{m6})^2\right]\int_{0.1f_m}^{f_m} (\frac{df}{f})\end{aligned} \tag{2.10}$$

where K_p and K_n denote the process-dependent flicker noise constants for PMOS and NMOS

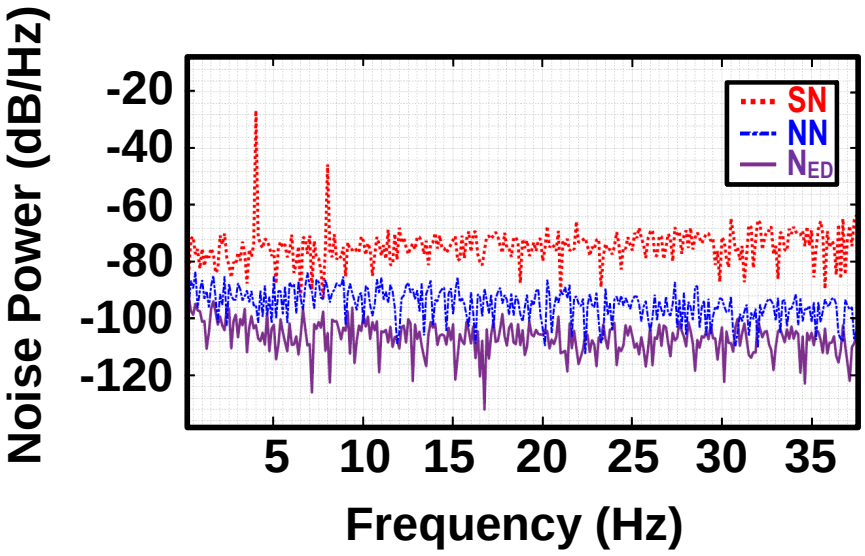

Figure 2.8: Simulated noise power of each contributing sources (SN: signal-dependent noise, NN: self-mixing noise, N_{ED}: intrinsic noise of envelope detector).

devices, respectively. C_{ox} represents the gate-oxide capacitance per unit area. Shown in Fig. 2.8, noise power of each contributing source at the output of multiplier is plotted for an AM input signal, similar to (2.6), with the following parameters: A_c=50 μV, f_c=120 Hz, f_m=4 Hz and a_m=0.5. As expected, signal-dependent noise contribution is much more significant compared to the intrinsic transistor noise of envelope detector and varies with the input signal amplitude.

To arrive at the output SNR, one needs to find the average power of the output signal ($\overline{I^2_{sig^2,out}}$) which can be found by integration, assuming $m(t)$ has zero average value:

$$\begin{aligned}\overline{I^2_{sig^2,out}} &= \lim_{T\to\infty}\frac{1}{2T}\int_{-T}^{T}\left(G_c V^2_{sig,AM}\right)^2 dt \\ &= \frac{3}{2}G_c^2\left(\overline{V^2_{sig,\gamma}}\right)^2\left[1+6a_m^2\overline{m^2(t)}+a_m^4\overline{m^4(t)}\right]\end{aligned} \tag{2.11}$$

Omitting small noise contribution of envelope detector for simplicity and assuming 50% duty-cycled square wave for $m(t)$, output SNR (SNR_{out}) is found as a non-linear function

of input SNR (SNR_{in}) :

$$SNR_{out} = \frac{\overline{I^2_{sig^2,out}}}{\overline{I^2_{n,out}}} = SNR_{in}\frac{(1+a_m^2)^2 + 4a_m^2}{4(1+a_m^2) + \frac{2}{SNR_{in}}}\frac{f_B}{f_m} \tag{2.12}$$

SNR_{in} in (2.12) is a function of high-γ bandwidth and is derived from (2.7), i.e.,

$$SNR_{in} = \frac{A^p}{\overline{V_n^2}}\frac{(Q-1/2)^{-(p-1)} - (Q+1/2)^{-(p-1)}}{(p-1)f_B^{p-1}} \tag{2.13}$$

As defined before, Q denotes the BPF quality factor. It is evident from (2.13) that lowering Q by reducing f_c (i.e., constant bandwidth) to contain only the neural features of interest provides the highest SNR_{in}. As predicted in [36], SNR_{in} is expected to degrade with the sharper roll-off (i.e., higher p value), particularly above 80 Hz. However, the premise of high-γ AM modulations implies that with higher a_m, which may further improve over time with co-adaptation of an implanted BMI, it is advantageous to perform low-noise analog power envelope extraction to achieve higher SNR as derived in (2.12), while attaining significant power-saving at the system-level. Two special cases of (2.12) are considered: (a) low and (b) high input SNR. For (a), it can be seen that the output SNR becomes proportional to SNR_{in}^2. However, for (b), it is understood that with increasing the signal amplitude, the signal-dependent noise term also increases and therefore, the output SNR is proportional to SNR_{in}.

2.4.4 Transient Analysis of Post-Multiplexing Modules

Since FB MUX operates at significantly higher frequency compared to BB MUX, subsequent amplification stages in FB mode must satisfy more stringent settling time and bandwidth requirements. Given n_{FB}-bit resolution for FB ADC, the amplified output voltage is required to reach its full-scale level within $0.69(n_{FB}+\varepsilon)\tau_{FB}$ for the conventionally adopted error

margin of $1/2^{\varepsilon}$ LSB ($2 \leq \varepsilon \leq 4$). τ_{FB} is defined as the time constant of an equivalent RC circuit modeling the output load of the post-multiplexing amplification stage in FB mode. Similarly, for n_{BB}-bit resolution of BB ADC, the amplified output voltage is required to settle within $0.69(n_{BB}+\varepsilon)\tau_{BB}$, where τ_{BB} is the equivalent time constant in BB mode. The output voltage settling required in each mode of operation should be succeeded within one sampling period, i.e., $0.69(n_{FB}+\varepsilon)\tau_{FB} \leq \frac{0.5}{f_{s,FB}}$ and $0.69(n_{BB}+\varepsilon)\tau_{BB} \leq \frac{0.5}{f_{s,BB}}$. Hence, the ratio of the minimum required bandwidths for FB/BB post-multiplexing stages is expressed as follows:

$$\left(\frac{\tau_{BB}}{\tau_{FB}}\right)_{min} = \frac{(n_{FB}+\varepsilon)f_{s,FB}}{(n_{BB}+\varepsilon)f_{s,BB}} \approx \frac{n_{FB}}{n_{BB}}\frac{1}{\eta} \tag{2.14}$$

(2.14) signifies that the minimum required bandwidth for post-multiplexing stages is approximately two orders of magnitude higher in FB compared to BB mode for $\varepsilon = 2$ and $\eta = 0.02$, given the different settling requirements. This is to be expected, as time-multiplexed FB operation requires significantly higher sampling rate and resolution than BB operation.

2.5 Experimental Results

In this section, electrical and biomedical measurements are presented. Electrical characterization was done prior to any biomedical testing to ensure proper functionality and reliable recording of the system. *In vivo* human tests involved EEG and ECoG measurements. DMFE array recorded reliably in all testings and showed on-par performance with commercial systems while consuming significantly less power.

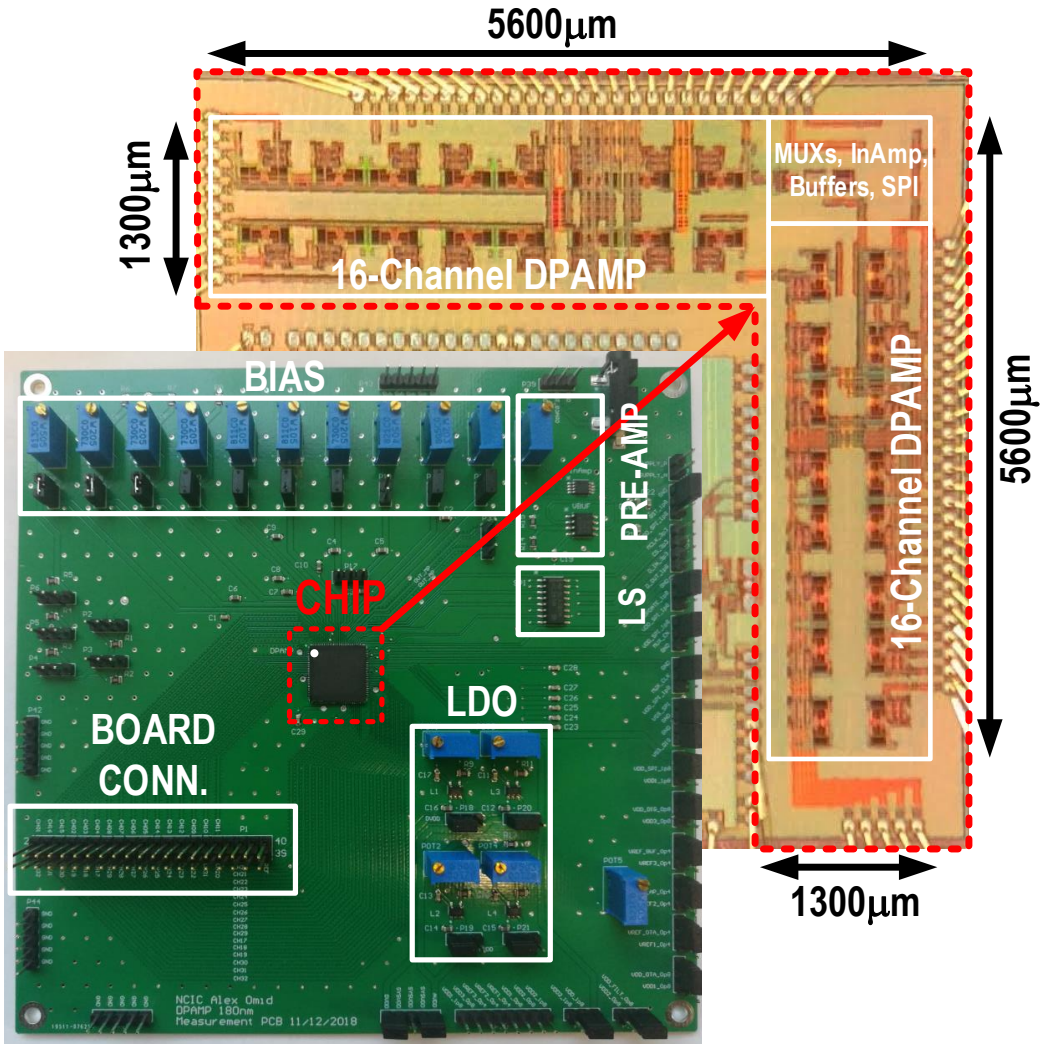

Figure 2.9: Chip micrograph and custom-designed printed circuit board.

2.5.1 Electrical Measurements

The prototype is fabricated in 180nm CMOS process. Fig. 2.9 shows the chip micrograph along with the custom-designed printed circuit board (PCB). An L-shaped geometry was employed to accommodate DMFE array, placing each channel in the proximity of the pad ring. The pads are located around the perimeter and incorporates a 2kV HBM ESD protection circuitry with a few pA of leakage current. Following a modular design, two 16-channel DMFE arrays were constructed perpendicular to each other with shared building blocks,

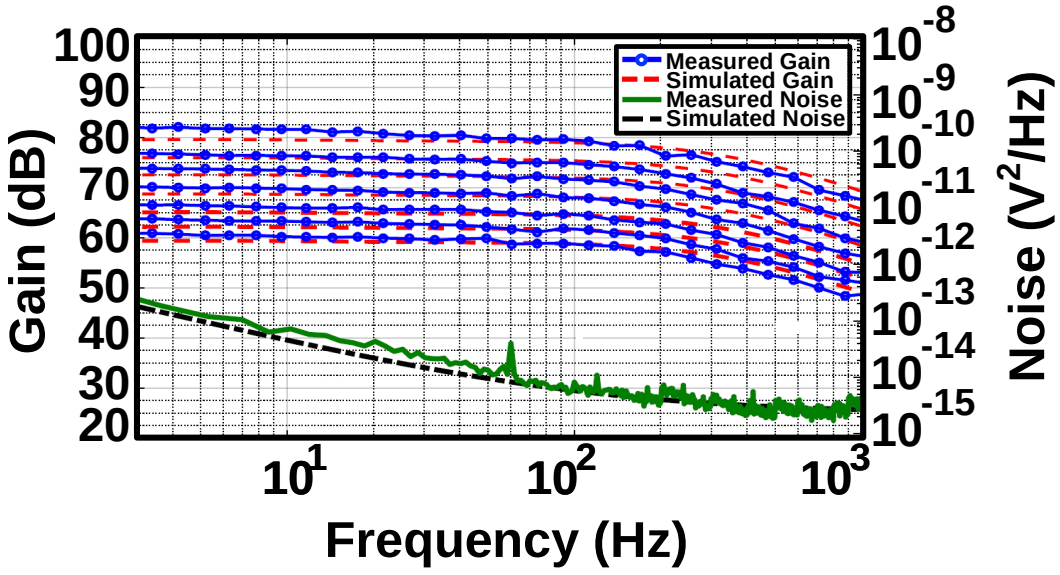

Figure 2.10: Measured and simulated results of total gain in different settings and input-referred noise for a single channel (i.e., AMP and InAMP) in FB mode.

including InAMP, output buffers, digital circuitry and SPI placed at the intersection. This approach is pursued to allow seamless integration of more channels with less routing overhead and inclusion of other common blocks such as low-dropout (LDO) regulators, ADCs and reference buffers in the finalized design. Global bias is provided externally and local bias is generated internally within each module and is tuned via current banks. The custom-designed PCB includes bias, SPI level shifters (LS), LDO regulators for chip supply, and pre-amplifier (TI-INA826, not shown in Fig. 2.3(a)) before external ADC to meet the dynamic range requirements. The chip operates at 0.8V supply voltage and consumes 59.4 μW in FB and 34.6 μW in BB mode (excluding bias). Each DMFE consumes 1.05 μW power and 0.245 mm^2 area, allocating 0.205 μW power and 0.145 mm^2 area for feature extraction only.

To characterize the overall amplification and input-referred noise in FB mode, an Agilent 33250A waveform generator with external attenuators and an Agilent E4448A spectrum analyzer were used. The nominal gain setting of InAmp provides an additional 20dB of gain, with 3dB steps up to $\sim$40 dB. Shown in Fig. 2.10, the total measured gain in different

settings and input-referred noise are compared with simulation results. For an InAmp gain setting of 23 dB, an overall gain of 63 dB and an RMS input-referred noise of 1.49 μV were achieved across a 2-200-Hz bandwidth. While the lower corner frequency realized by pseudo-resistor is expected to vary across the process corner, it is simulated and measured to be below 2 Hz, which helps acquire low-frequency activity of the brain in θ-band (4-8 Hz). For an input common-mode signal of $100mV_{pp}$, the measured CMRR and PSRR are better than 76.5 dB and 79 dB, respectively. The calculated dynamic range of AMP for $\sim$1% total harmonic distortion is 60.2 dB. Table 2.1 provides a performance summary of the DMFE and comparison with similar prior works. Based on a dual-mode ASP architecture, the DMFE consumes 1.05 μW of power and occupies 0.245 mm^2 of die area per channel while achieving an NEF of 4.09 and a PEF of 10.04. The DMFE achieves the lowest feature-extraction power dissipation with superior NEF and PEF compared to prior works. The power consumption of each block in the front-end is summarized in Table 2.2. The power dissipation of AMP is represented by P_U in (2.1), while InAMP and FB buffer constitute the post-amplification stages. The power dissipated by biquads, interstage buffers, multiplier, degenerated LPF and buffer sum up to represent P_{NP^2}. Lastly, BB buffer is used to approximate ηP_U in (2.1). As indicated, AMP takes a significant portion of the total power consumption in both BB and FB mode given that the first-stage amplification requires more power dissipation to minimize the input-referred noise. In NP^2 module, the multiplier introduces voltage offset that can be minimized by increasing the bias current, and hence raising the power consumption. Nevertheless, the BB-mode, compared to FB-mode operation, still achieves approximately 2 times lower power dissipation in the front-end with the premise that the mixed-signal and digital back-end would require significantly less power, achieving 50$\times$ power-saving as discussed in Section 2.3.

Table 2.1: Dual-Mode Array Performance Comparison

Reference	TBCAS 2018 [41]	TBCAS 2016 [42]	TBCAS 2015 [43]	CICC 2017 [44]	ISSCC 2014 [45]	This Work
Process (nm)	180	180	180	65	130	180
Architecture	AMP	ASP	DSP	DSP	ASP	DM-ASP
No. of channels	1	16	8	1	1	32
Supply Voltage (V)	1.8	0.9	1.8(A)/1(D)	0.8	1.3-1.8	0.8
Gain (dB)	35.04	40	40	22-43	20-44	60-81.47(FB)/57-76(BB)
Bandwidth (Hz)	9.3k	0.3-7k	0.5-100	250	130	2-200
IR-Noise (μV_{rms})	3.2	4.57	0.81	1.90-2.91	4.9	1.49
NEF	1.94	4.77	4.0	4.17-4.47[a]	6.46[a]	4.09
PEF	6.77	15.45	12.96	13.88-15.97[a]	54.27-75.14[a]	10.04-13.38[b]
CMRR (dB)	76	81	100	82	>90	>76.5
Feature Extraction/Total Power per channel (μW)	NA/4.5	7/15	7/34	0.307-0.769	0.33/0.9	0.205/1.05
Area per channel (mm^2)	0.072	0.116	3.125	2	8.6	0.245

[a] Estimated from reported results [b] For operation with 0.6 to 0.8V supply

Table 2.2: Front-End Power Consumption Breakdown

Block	BB	FB
AMP	798 nW	798 nW
Biquads	2.4 nW	-
Int. Buffer	4 nW	-
Multiplier	160 nW	-
Degen. LPF	9.36 nW	-
Buffer	80 nW	-
InAMP*	-	920 nW
FB Buffer*	-	137 nW
BB Buffer*	25 nW	-
Total	1.08 μW	1.86 μW

*Power consumption of shared blocks is divided by channel count

2.5.2 Human Neurological Measurements

The experiments carried out in this study were approved by the Institutional Review Boards of the University of California, Irvine and the Rancho Los Amigos National Rehabilitation Center, and are considered non-significant risk. Two human subjects (A and B) provided informed consent to participate in EEG and ECoG recordings, respectively. Single-channel and multi-channel acquisition in FB were done for EEG, in conjunction with commercial systems to validate the performance on Subject A. Similarly, single-channel and multi-channel ECoG recording in FB and BB were done at the bedside with Subject B, who was undergoing epilepsy treatment. A summary of correlation coefficients from all recordings in each frequency sub-band is presented in Table 2.3. For brevity, methods and results from *in vivo* ECoG recordings are described in the following sections.

Methods: One male patient undergoing ECoG implantation for epilepsy surgery evaluation was recruited (Subject B). The subject had a 4×8 mini-grid (Integra LifeSciences, Plainsboro NJ). Fig. 2.11 shows the location of implanted electrodes (derived by co-registering CT and MR brain images). The ECoG grid placed over the left hemispheric (LH) motor arm area was used to record brain activity during sleep (baseline) and a flexion task in FB and BB modes, respectively. Fig. 2.12 shows the hospital setup for *in vivo* ECoG recording. 32

Table 2.3: Sub-Band Correlation Coefficients

Signal/Mode/Acq. Method	θ (4-8 Hz)	α (9-12 Hz)	β (13-30 Hz)	low-γ (30-70 Hz)	high-γ (80-160 Hz)	γ (80-100 Hz)	Raw
EEG/FB/Single	0.982	0.989	0.984	0.952	-	0.907	0.946
EEG/FB/Multiplexed	0.899	0.914	0.729	0.686	-	0.407	0.871
ECoG/FB/Single	0.998	0.989	0.961	0.948	-	0.889	0.924
ECoG/FB/Multiplexed	0.992	0.987	0.979	0.842	0.584	-	0.964
ECoG/BB/Single	-	-	-	-	-	-	0.769
ECoG/BB/Multiplexed	-	-	-	-	-	-	0.60-0.84

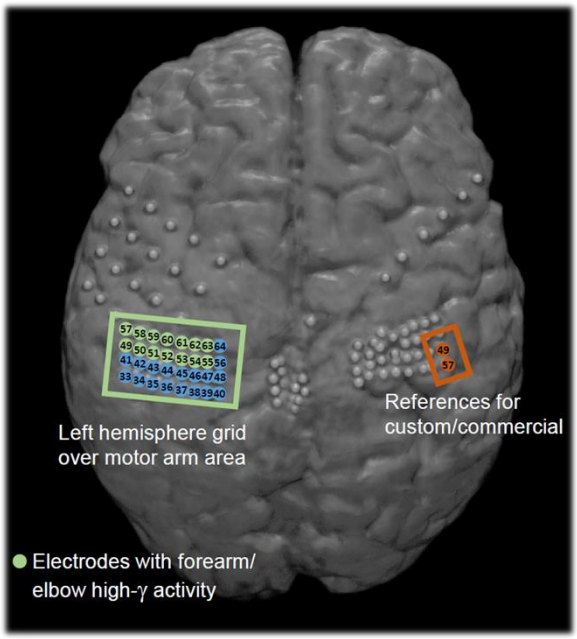

Figure 2.11: MR-CT fused image from Subject B, showing implanted ECoG grid over arm motor area of the brain.

electrodes from LH grid were used to record ECoG signals by custom (chip) and commercial (Biopac EEG100C, NeXus-32) systems, simultaneously. The chip was battery-powered and Biopac MP150 data acquisition was used to digitize the analog output. Arduino provided the clock (CLK) and reset (RST) signals for the chip. A host PC was responsible for chip configuration, synchronization between custom and commercial system outputs, demultiplexing and post-processing of ECoG recordings. For FB single-channel and multi-channel recording, EEG100C and NeXus-32 were used in parallel with the chip to capture baseline activity, respectively. The subject was asleep during these experiments. For both BB single-channel and multi-channel recording, NeXus-32 was used in parallel with the chip. The subject was verbally instructed to perform elbow flexion for two 15-second periods with an idling period of 15 (single-channel) and 10 (multi-channel) seconds in between. Since NeXus-32 did not natively extract envelopes, chip-equivalent processing (i.e., band-pass filtering, power extraction and low-pass filtering) were applied in order to draw a comparison between the two acquisition systems. As depicted in Fig. 2.11, a subset of LH electrodes, which

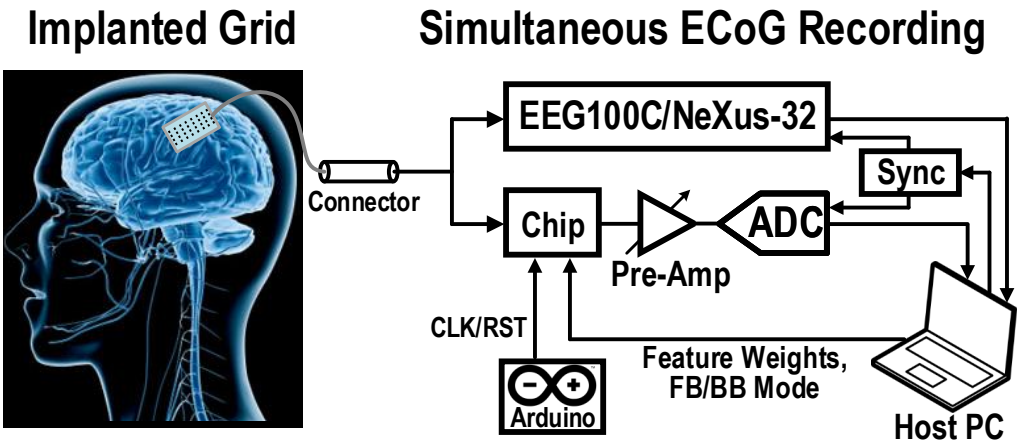

Figure 2.12: Hospital setup.

was determined by clinical cortical mapping procedures to correspond to forearm/elbow flexion, was used to collect brain activity for analysis during sleep (baseline) and an elbow flexion task. Given separate reference electrodes for custom chip and NeXus-32, the split reference was compensated for by common-mode averaging in post-processing [46]. The Pearson correlation was calculated between the outputs of custom and commercial systems for comparison. Additionally, correlations were calculated for physiological sub-bands to further ascertain the accuracy of the chip in comparison with the commercial system.

Results: FB single-channel and multi-channel recordings from custom and commercial systems are shown in Fig. 2.13(a)-(b). For BB single-channel, the extracted envelope is shown in Fig. 2.14, along with a spectrogram of raw ECoG from NeXus-32 which exhibits power increase across high-γ-band during movement. For BB multi-channel recording, a few extracted envelopes are shown in Fig. 2.15. Unlike the FB-mode data, which can be seamlessly compared between the commercial and custom systems, the comparison of the BB-mode data requires extensive signal processing, as discussed earlier. Considering that the analog implementation introduces a number of noise sources (Section 2.4.3), the digital chip-equivalent operators suffer mainly from insignificant quantization and rounding errors, giving rise to lower correlations reported for the BB-mode data as compared to the FB counterpart.

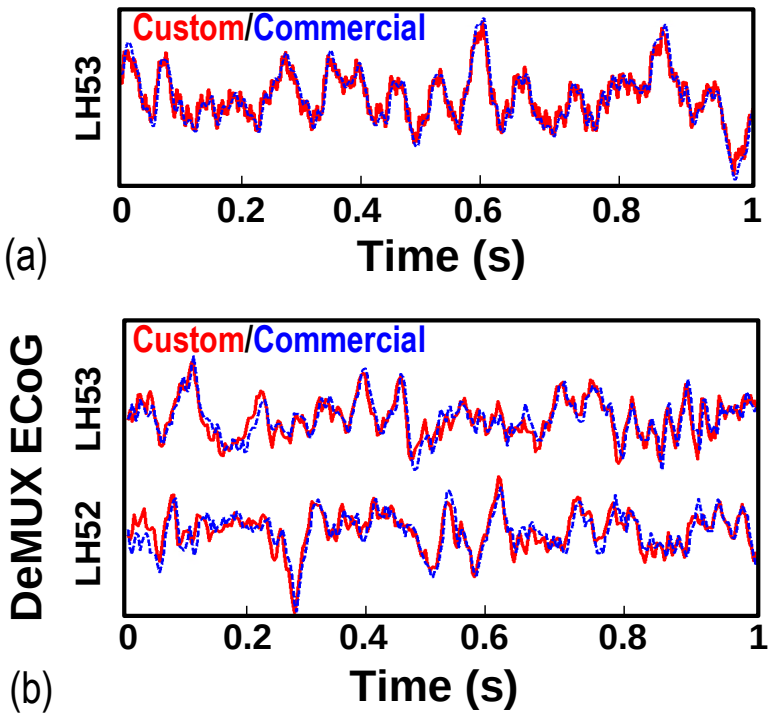

Figure 2.13: Normalized ECoG time-series data from (a) single-channel recording and (b) de-multiplexed recording in FB mode.

2.6 Conclusion

A dual-mode array architecture for high-density ECoG implantable BMIs was presented. The 180nm CMOS chip includes a 32-channel signal acquisition front-end capable of acquiring and pre-processing of ECoG signals. Each channel employs a DMFE which consumes 1.05μW and 0.245 mm^2 area, allocating 0.205μW and 0.145 mm^2 area for feature extraction only. *In vivo* ECoG recordings have demonstrated the feasibility of extracting power envelopes during movements using our ULP dual-mode prototype. Compared to commercial systems, our chip is capable of acquiring power envelopes with significantly less power consumption.

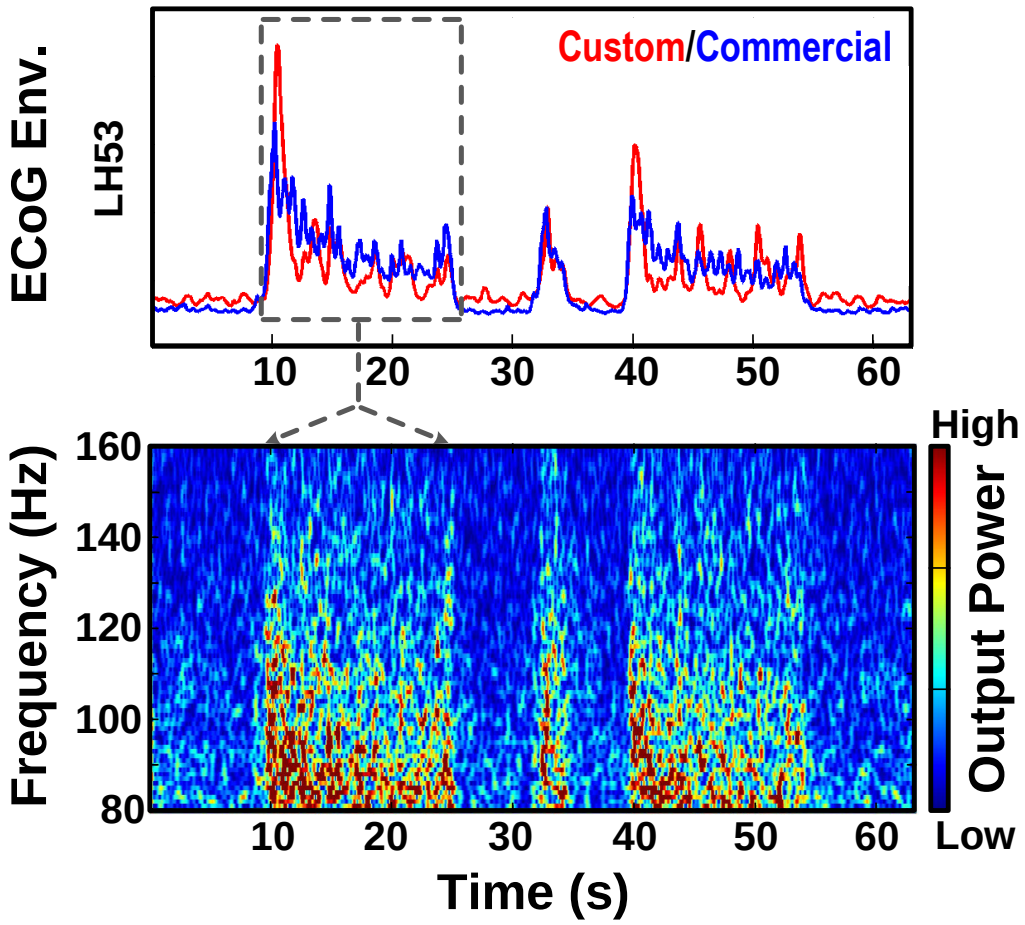

Figure 2.14: Normalized ECoG power envelope time-series data from single-channel recording in BB mode (top) and spectrogram of raw ECoG from commercial system (bottom).

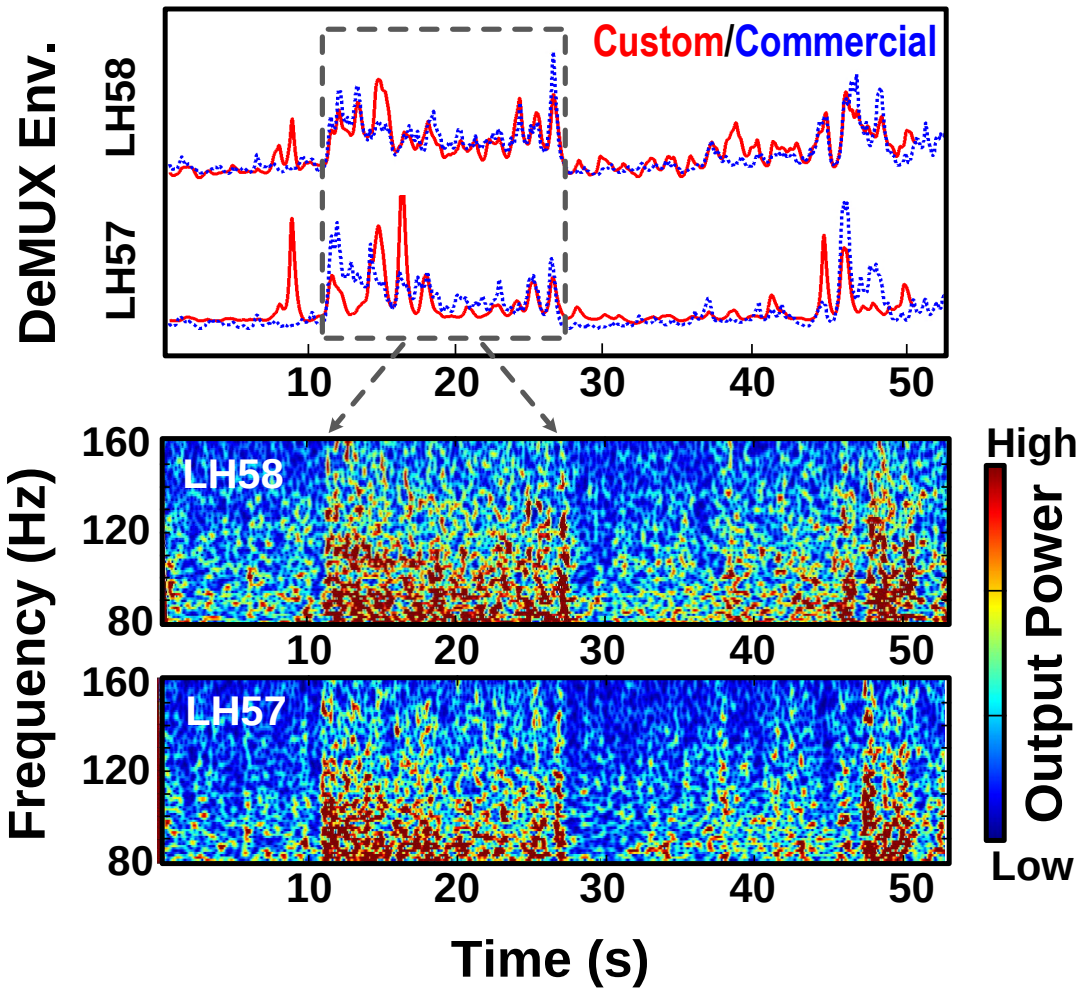

Figure 2.15: Normalized ECoG power envelope time-series data from de-multiplexed recording in BB mode (top) and spectrogram of raw ECoG from commercial system (bottom).

Chapter 3

Mixed-Signal Neural Data Acquisition System for Implantable BMIs

3.1 Introduction

Restoration of neurological functions impaired by spinal cord injury necessitates implantable brain-machine interfaces (BMIs), capable of neural signal acquisition, processing, and wireless connectivity to external base-station and end-effectors. While electrocorticography (ECoG)-based BMIs provide superior signal stability, electrode longevity and spatial resolution/area coverage for accurate decoding of neural activity, the overall power dissipation needs to be minimized to allow prolonged battery life which is a critical aspect of biomedical implants. Existing neural decoding architecture for implantable BMIs is primarily based on conventional power-hungry brain signal acquisition and processing approaches, which are ill-suited for high channel-count systems [47]. Shown in Fig. 3.1, a standalone data acquisition (DAQ) captures neural signals of varying amplitudes across a wide range of frequencies (near DC up to 1 kHz) and provides digitized samples to a back-end processor for

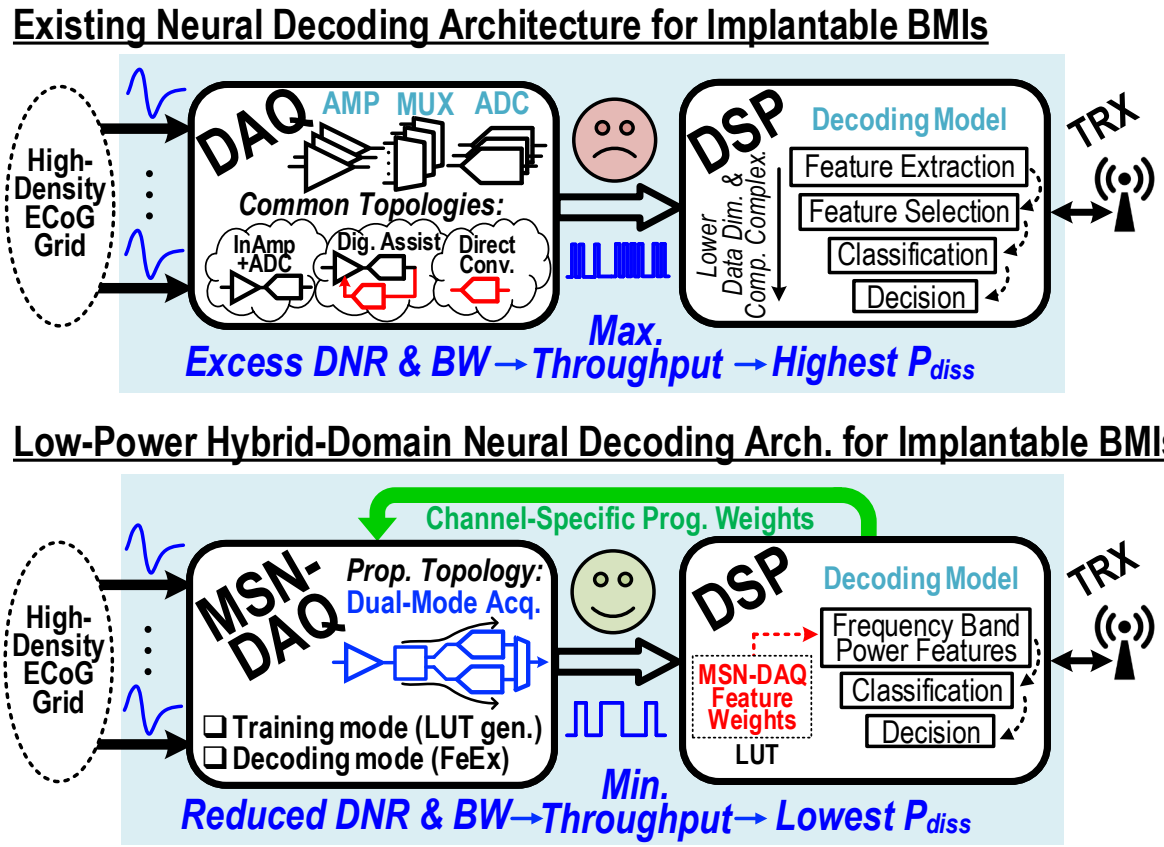

Figure 3.1: Conventional and proposed neural decoding architectures for high channel-count implantable brain-machine interfaces.

decoding purposes. However, the relevant physiological neural information, such as movement intentions, is typically encoded within a fraction of frequency range (e.g., high-γ band) whose content requires significantly less dynamic range and bandwidth compared to the raw neural signal. As such, conventional DAQ is bound to operate with an excess dynamic range and bandwidth that result in an unduly high data throughput, placing a significant power and computing burden on digital signal processor (DSP). Recent works do not address this prominent data-processing power bottleneck for massive channel-count systems, including several neural recording architectures based on capacitively-coupled InAmp+ADC [48], DC-coupled digitally-assisted amplifier [16] and direct conversion (time-based [49], delta-sigma [50]) schemes.

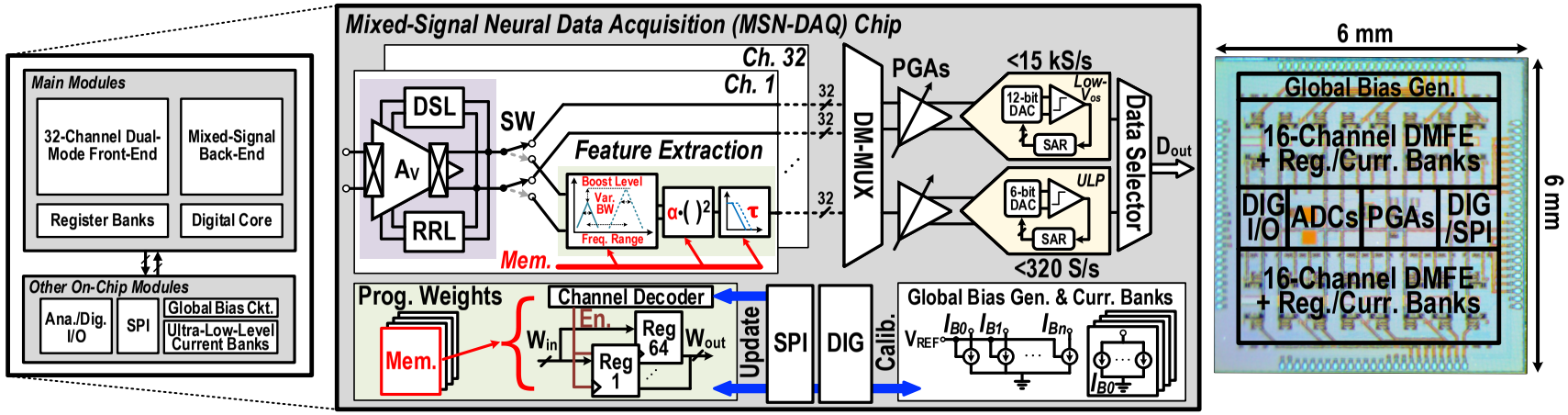

Figure 3.2: System architecture of the mixed-signal neural data acquisition (MSN-DAQ) chip and a micrograph of its fabricated prototype.

Inspired by our work in [51], the proposed mixed-signal neural DAQ (MSN-DAQ) enables a novel low-power hybrid-domain neural decoding architecture for implantable BMIs by adopting dual-mode acquisition that is intended for distinct use in training and decoding procedures, with the latter accounting for the majority of operation time. In training mode, raw neural signals are collected by MSN-DAQ during a set of clinical trials and transmitted to an external base-station where decoder training takes place offline [52, 53]. While training helps improve decoding accuracy and provides a means of calibration and validation, it primarily involves data collection with increased bit-resolution and sampling rate, further justifying the dual-mode acquisition. Once the decoder's performance is optimized, identified features and their corresponding weights are computed in a lookup table to be transferred to DSP and subsequently applied to the channel-specific programmable weights on MSN-DAQ, marking the transition to decoding mode. Similar to [51], feature extraction is performed in analog domain using the stored weights, which facilitates the digitization with minimum required bit-resolution and sampling rate. Hence, the DSP power dissipation is significantly relaxed. Furthermore, no computationally-expensive algorithm needs to be executed on DSP for decoding in this proposed framework, and therefore, the back-end's complexity overhead remains relatively low with increasing number of channels, a highly desired attribute for real-time operation in implantable BMIs with multiple functionalities.

The rest of this chapter is organized as follows: Section 3.2 describes the proposed MSN-DAQ system and its circuit implementation. Experimental results including electrical and *in vivo* measurements are presented in Section 3.3, followed by concluding remarks in Section 3.4.

3.2 Proposed Mixed-Signal Neural DAQ

Fig. 3.2 shows the top-level system block diagram of MSN-DAQ. The main modules include a 32-element dual-mode front-end array with register banks to store channel-specific programmable weights, mixed-signal back-end consisting dual-mode multiplexer (DM-MUX), programmable gain amplifiers (PGAs), analog-to-digital converters (ADCs) with distinct bit-resolution and bandwidth requirements for training and decoding modes, and a digital core. Other on-chip blocks include serial peripheral interface (SPI), bias circuitry for global current generation, digitally-controlled ultra-low-level current banks and analog/digital input-output (I/O) modules.

3.2.1 Dual-Mode Front-End and Analog Interface Circuits

The dual-mode front-end includes a newly-added low-noise, folded-cascode chopper-stabilized amplifier array. Shown in Fig. 3.3 is the closed-loop amplifier incorporating two auxiliary loops across the output and folding nodes: (a) DC servo loop to further attenuate low-frequency signals and minimize the output offset, and (b) ripple reduction loop to minimize chopping ripples introduced by up-modulated voltage offset of the input stage, $G_{m,1}$. Given that the chopping mechanism eliminates the mismatch effect of transistors, high common-mode rejection ratio (CMRR) can be achieved. To further improve CMRR, input capacitors were adequately sized to reduce mismatch and the common-mode to common-mode attenuation was notably increased by using an input-injecting common-mode feedback (CMFB) network, which remarkably improves the source impedance by an additional loop gain factor.

Depending on acquisition mode, raw neural signal or extracted neural features are time-multiplexed and further amplified by the respective PGA. Since raw signals contain higher dynamic range and bandwidth, the required settling time prior to digitization is significantly

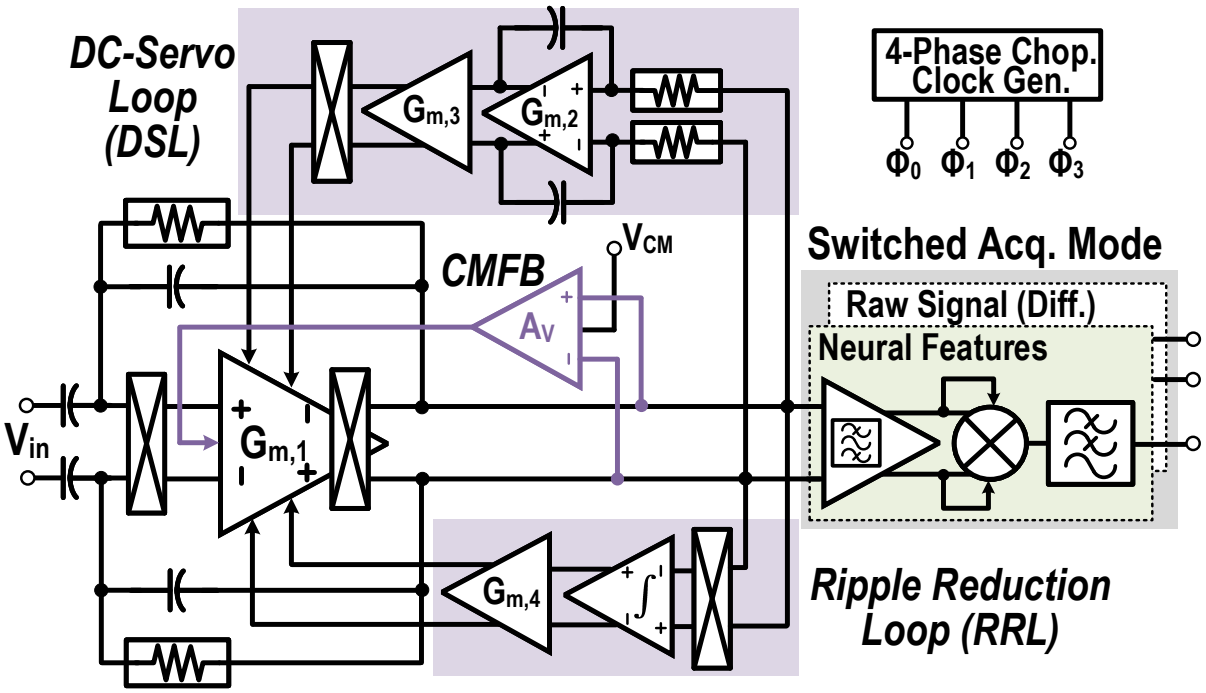

Figure 3.3: Schematic details of dual-mode front-end, incorporating DC-servo loop, ripple reduction loop and common-mode feedback.

shortened. A higher unity gain-bandwidth product required in training mode is achieved by increasing the transconductance, resulting in higher power consumption in this mode. Conversely, neural features do not suffer from this problem, and thus, the PGA consumes significantly less power in decoding mode.

3.2.2 Successive Approximation Register ADCs

To meet the stringent power requirements of neural data acquisition, successive approximation register (SAR) ADC is chosen. Shown in Fig. 3.4, the differential 12-bit SAR-ADC includes a V_{CM}-based binary-weighted capacitive digital-to-analog converter (DAC) array, a multi-stage offset-canceling comparator and a compact modular non-redundant SAR logic and control with minimum circuit overhead. The digitization begins with top-plate sampling of the amplified differential input signal, followed by the energy-efficient bit-cycling that is

accomplished by V_{CM}-based switching scheme. To satisfy the required resolution, a combination of circuit and layout techniques have been utilized. Most notably, the comparator employs three-stage pre-amplification with output offset cancellation (OOS) to minimize the input-referred voltage offset and the kickback noise introduced by the regenerative latch. Moreover, twisted differential signaling is applied between the DAC and the comparator to suppress common-mode noise (Fig. 3.4). To implement the SAR algorithm, a compact modular digital circuity based on non-redundant logic is used. Illustrated in Fig. 3.4, the entire SAR logic consists of only 12 MUXed D-flipflops and 11 OR gates. Moreover, a unique control circuitry (shaded in light blue) – consisting of only 1 D-flipflop, 1 inverter and 2 AND gates for each bit – is implemented to accommodate the V_{CM}-based switching procedure. The working principle is as follows: Initially, each D-flipflop in the control circuitry is reset by $CK_{S/H}$ during the sample and hold operation. Thus, all S_3 switches are enabled in the capacitive DAC, connecting the bottom plate of each capacitor to the common-mode voltage (V_{cm}). Next, SAR logic produces a leftward-propagating pulse that is sequentially captured by each stage in the shift register. Each in-between interval lasts for one clock period of CK_{SAR} and represents a comparison window. During each interval, one bit is resolved at a time and the result is stored in the corresponding MUXed D-flipflop. Starting with the most significant bit, the direction of binary search is determined by the stored value at the end of each comparison window. Given the inherent sequential operation of SAR algorithm within comparison windows, each control D-flipflop detects the transition instances and generate the necessary control signals by a simple combinational circuit. Depending on the outcome, the appropriate DAC switch (S_1 or S_2) is activated at the beginning of each comparison window immediately after S_3 is turned off. The detection and control signal generation continue until all bits have been resolved, and a new conversion takes place.

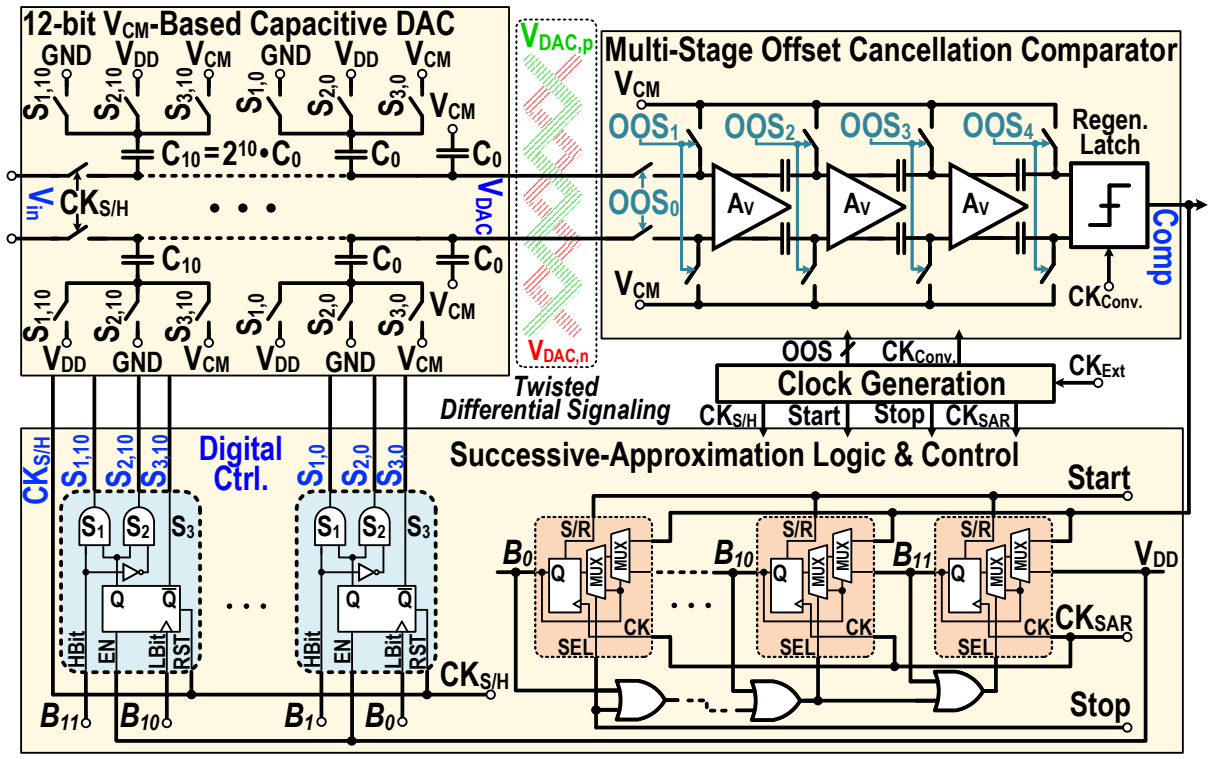

Figure 3.4: Schematic details of SAR-ADC, highlighting the digital logic and control circuitry for V_{CM}-based capacitive DAC.

3.3 Experimental Results

3.3.1 Electrical Measurements

MSN-DAQ chip achieves a measured 42.5-dB minimum closed-loop gain, 1.03 μV_{rms} input-referred noise (2-200 Hz), 2.37 noise efficiency factor (NEF), 5.62 power efficiency factor (PEF) at 1V supply voltage, and 88-dB average CMRR for a maximum 10mVpp interference within 50-160 Hz range. Fig. 3.5(a) shows the measured frequency response of MSN-DAQ across 3 neighboring channels and different gain modes for one channel. Based on measured FFT of the 12-bit SAR-ADC output for 193.17-Hz tone (i.e., upper edge of the frequency band) at maximum sampling rate of 15kHz, the ENOB, SFDR, and SNDR are 10.5, 65.2 dB, 64.78 dB, respectively, as depicted in Fig. 3.5(b).

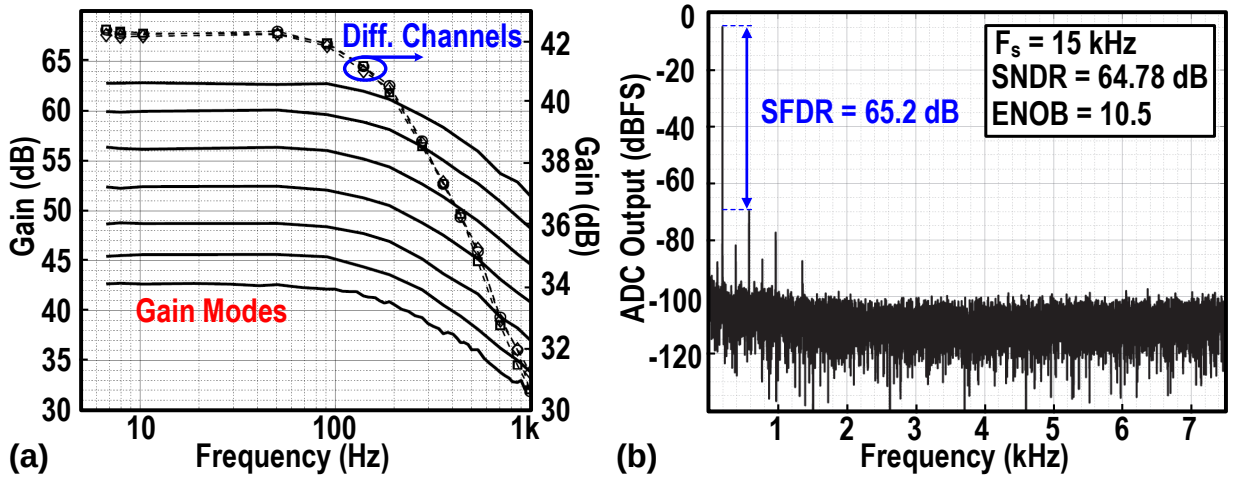

Figure 3.5: (a) MSN-DAQ measured frequency response and (b) ADC measured output power spectrum.

3.3.2 Biomedical Testing and *In vivo* Measurements

To further validate MSN-DAQ operation within a clinical context, neural recordings were carried out on an epileptic patient with implanted ECoG grids. The study was approved by the Institutional Review Board of the Rancho Los Amigos National Rehabilitation Center and the University of California, Irvine. Fig. 3.6 illustrates the experiment setup with connections between the implanted ECoG girds and the recording systems, including hospital clinical acquisition (i.e., Natus® Quantum™) and MSN-DAQ placed in a shielding enclosure. A similar setup was reproduced for the commercial Intan recording system (RHD2000), substituting Intan for MSN-DAQ to allow comparison with the custom chip. The raw neural data were acquired from 32 anteriorly placed electrodes over M1 (MG1-32) for ten 14-second idle periods and ten 14-seconds move periods during a hip flexion task. Fig. 3.7(a) shows a sample of acquired time-series data from three electrodes over the motor leg area that exhibited behavioral modulation. Fig. 3.7(b) show the spectrogram demonstrating μ-β power modulations for a pair of idle/move trials. After further statistical analysis of all the recorded trials, the power for idle and move states within each frequency band were plotted for both MSN-DAQ and Intan recording systems – as depicted in Fig. 3.8 – which exhibit similar

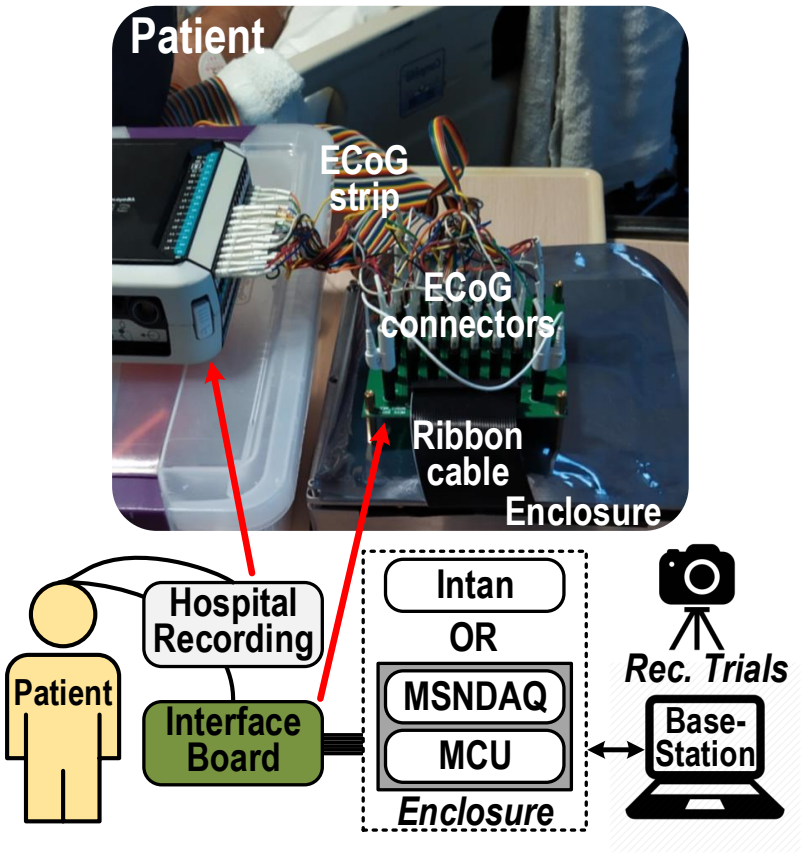

Figure 3.6: Hospital experiment setup, including the custom chip (MSN-DAQ) and commercial system (Intan).

distinguishable difference. Given that placement of ECoG grid was dictated by the patient's clinical needs, the highly-localized gamma activity correlated to hip flexion appeared to be less prominent, particularly for high-γ band which did not attain the expected distinguishable SNR range that have been previously observed in our prior works. Thus, the extracted high-γ features in decoding mode did not contain meaningful information regarding idle/move states. Nevertheless, to validate the operation in decoding mode, ECoG data containing high-γ modulations from previous hospital experiments were fed to MSN-DAQ by a high-resolution waveform generator. The extracted power envelope from an ECoG channel exhibiting high-γ modulation in response to an upper extremity movement task is shown in Fig. 3.9.

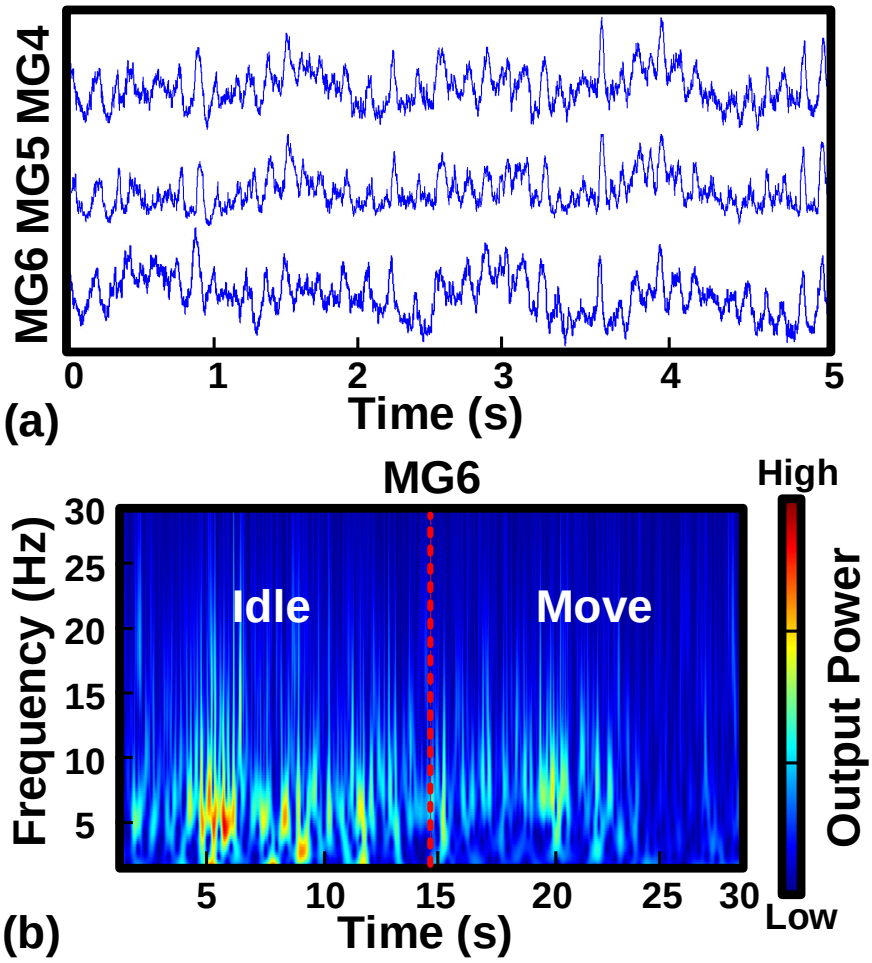

Figure 3.7: (a) ECoG time-series sample data from motor grid (MG) electrodes and (b) spectrogram of raw ECoG from MG6, acquired by MSN-DAQ.

3.4 Conclusion

A dual-mode mixed-signal neural data acquisition was presented. The 180nm CMOS chip enables a novel low-power hybrid-domain neural decoding architecture for implantable brain-machine interfaces that could achieve significant power-saving in high-channel count systems. In addition to electrical measurements, the prototype has been validated in a hospital setting with real-time human ECoG recording. A comparison with the most relevant prior works in Table 3.1 shows that the proposed MSN-DAQ achieves excellent CMRR and noise performance at lowest power consumption per channel.

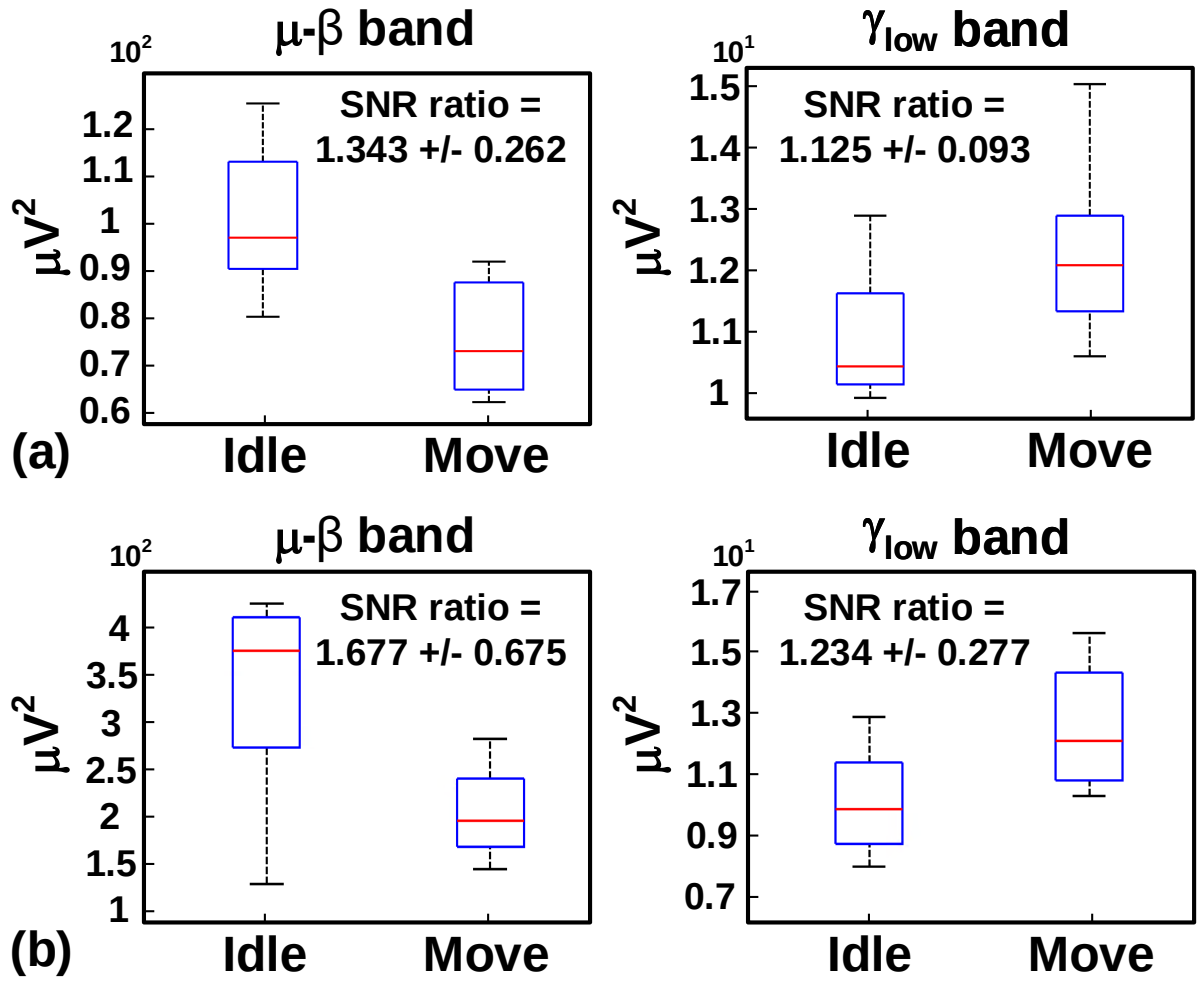

Figure 3.8: Box plots showing signal-to-noise power ratio (SNR) between idle and move states from (a) MSN-DAQ and (b) Intan recording system.

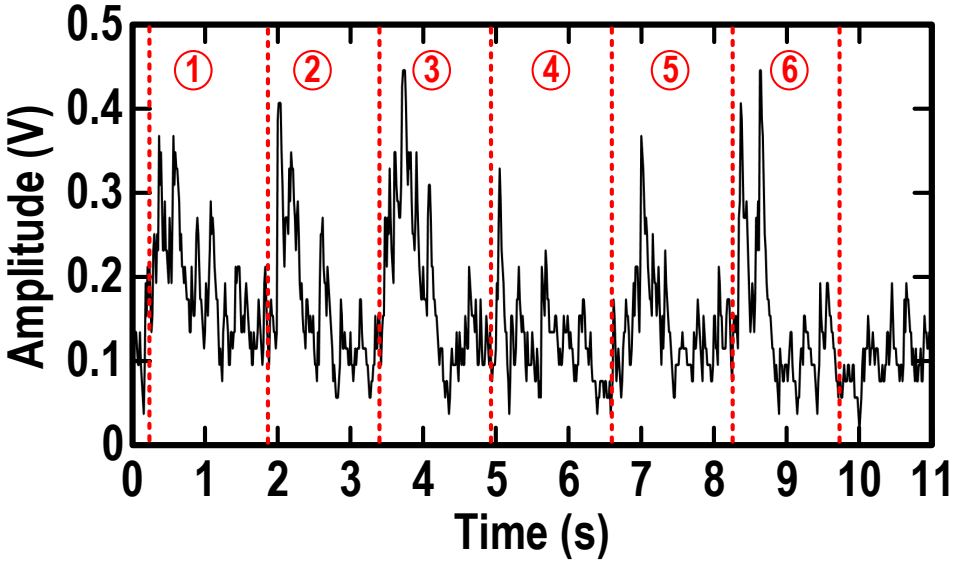

Figure 3.9: Extracted high-γ features in decoding mode, exhibiting power modulations during six consecutive elbow flexion and extension periods.

Table 3.1: MSN-DAQ Performance Comparison

	JSSC'15 [16]	TBCAS'18 [54]	JSSC'19 [49]	TBCAS'20 [55]	**This Work**
Tech. (nm)	65	180	180	65	**180**
Supply (V)	0.5	1.8	1.2	0.5, 2.5	**1**
Channel	64	16	4	64	**32**
Power/Ch. (μW)	2.3	3.26	3.9	2.98	**1.07**
BW (Hz)	1-500	0.59-117	200	1-1k	**2-200**
IRN (μV_{rms})	1.23	2.02	1.3	1.66	**1.03**
NEF	3.7	3.36	4.9	2.21	**2.37**
PEF	6.9	20.32	28.81	-	**5.62**
CMRR (dB)	88	67.1	>75	76	**88**
ADC Res.	15	10	-	16	**12**
ENOB	-	7.8	13.2	15.7	**10.5**

Chapter 4

Common-Mode Interference Analysis in Biosignal Recording Systems

4.1 Introduction

The presence of common-mode interference (CMI) is highly undesirable in biomedical signal acquisition and processing, as it necessitates an excessive dynamic range, higher linearity and additional high-Q notch filtering, without which the system will completely fail to operate. Historically, the 50/60-Hz power-line interference observed in biopotential recordings (e.g., two/three electrode ECG monitoring) has been thoroughly studied in a number of prior works [56, 57, 58], which provide detailed analysis and different mitigation techniques. More recently, with the advent of miniaturized electrode arrays and nanoscale electronics, implantable biomedical devices have introduced a new source of interference, namely the stimulation artifacts in bi-directional brain-machine interfaces. Similar to the power-line interference, electrical stimulation produces an in-band blocker with large common-mode component (>100mV) that is orders of magnitude greater than the biosignal (10-100μV).

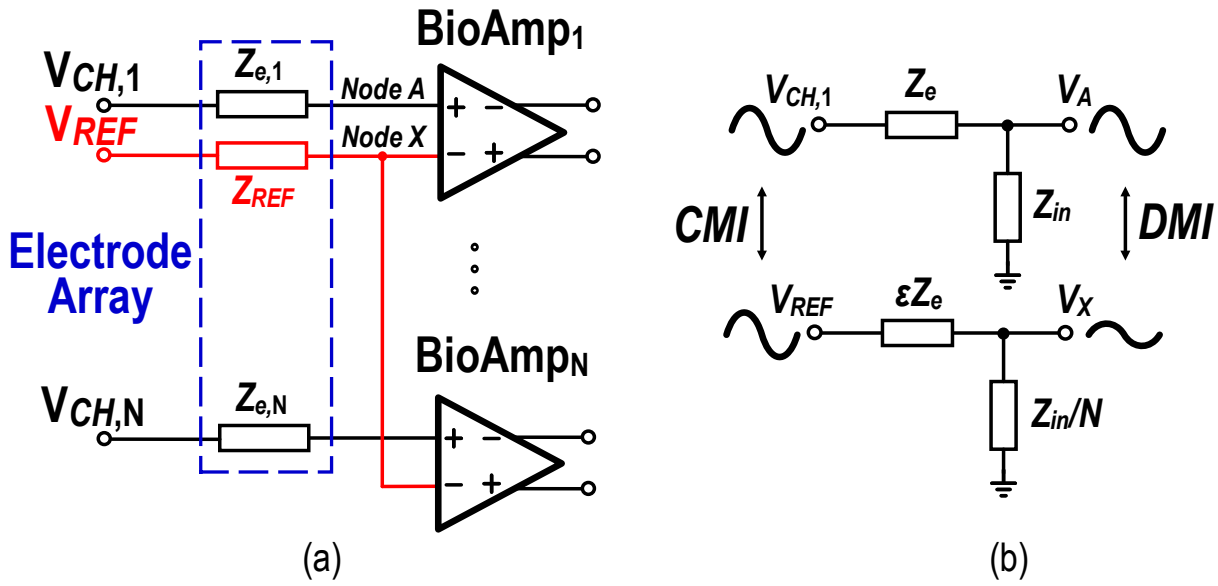

Figure 4.1: (a) Conventional N-channel biosignal acquisition front-end with shared reference (b) Simplified electrical model of the input interface [2].

While existing architectures rely on active shielding and bioamplifiers with high common-mode rejection ratio (CMRR) to suppress CMI, there still remains a major bottleneck within multi-channel recording systems that employ a shared-reference scheme. Shown in Fig. 4.1(a), a typical N-channel biosignal acquisition front-end consists of an electrode array and a set of differential bioamplifiers (BioAmps). Each BioAmp is connected to a biosignal electrode, as indicated by *Node A* for every channel, and a shared reference electrode, *Node X*. Since the latter node is attached to all N number of BioAmps, a systematic impedance imbalance exists, which together with the electrode's mismatch, give rise to unequal potential divider effect [56]. This phenomenon converts CMI present at the tissue-electrode interface to differential-mode interference (DMI), thereby limiting the maximum achievable CMRR in the system.

A simplified electrical model of the input interface for an N-channel neural amplifier system was presented in [2]. This model assumes an electrode impedance of Z_e and an input impedance of Z_{in} for each BioAmp, as depicted in Fig. 4.1(b). Hence, the total CMRR

($CMRR_T$) is expressed, as follows [2]:

$$\frac{1}{CMRR_T} = \frac{1}{ICMRR} + \frac{2(N\epsilon - 1)}{2|Z_{in}/Z_e| + N\epsilon + 1} \tag{4.1}$$

where ICMRR and ϵ represent the intrinsic CMRR of bioamplifier and the mismatch factor for the shared reference electrode, respectively. The second term in Eq. (4.1) approximates the CMRR degradation due to the unbalanced voltage division at the electrode-BioAmp interface. However, in deriving (4.1), a number of limiting assumptions have been adopted, which must be revised. For instance, 1) The input impedance of BioAmp is a combination of differential and common-mode impedances, thus Z_{in} needs to be revised in the foregoing analysis to account for both contributions. 2) When speaking of CMI to DMI conversion, it is important to note that the AC current flowing through the reference electrode may not be equally distributed among all BioAmps, as will be discussed later. Thus, Z_{in}/N illustrated in Fig. 4.1(b) needs to be modified, accordingly. This work provides a complete electrical circuit model of the input interface, followed by a generalized theory of CMRR degradation in multi-channel bioamplifiers.

4.2 Proposed Input Interface Model

In this section, the conventional N-channel biosignal acquisition front-end in Fig. 4.1(a) is revisited, where a complete representation of the input impedance of BioAmp is provided. Next, an equivalent electrical circuit model of the input interface is developed that lays the foundation for the subsequent analysis.

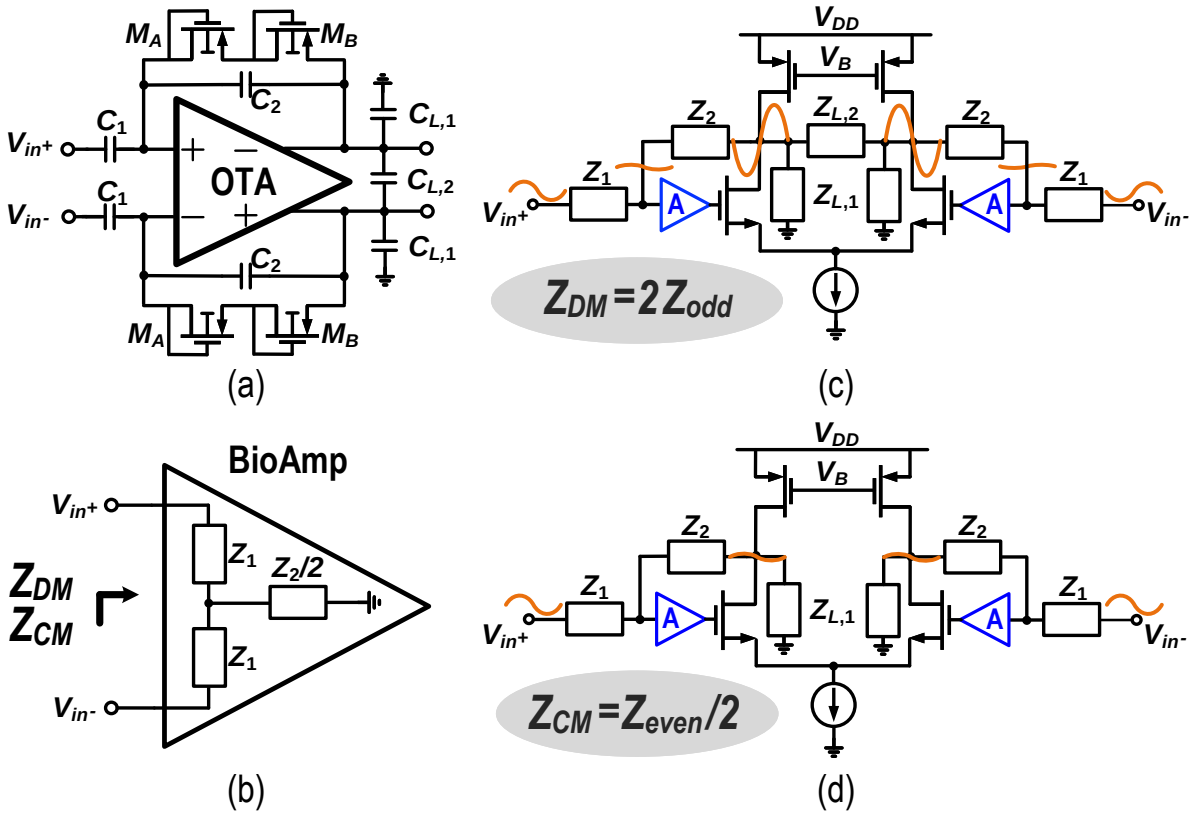

Figure 4.2: BioAmp (a) topology (b) input impedance model (c) differential-mode and (d) common-mode input impedance.

4.2.1 BioAmp Input Impedance

A widely used BioAmp is the capacitvely-coupled operational transconductance amplifier (OTA) that uses pseudo-resistors in the feedback network [13], as depicted in Fig. 4.2(a). Considering that the input impedance of BioAmp can be expressed in terms of a differential-mode (Z_{DM}) and a common-mode (Z_{CM}) component, a simple T-network is used to illustrate the input impedance of BioAmp, as shown in Fig. 4.2(b). Since OTA typically employs a cascade of two stages, it is modeled by a differential input pair with an effective transconductance of $A \times g_m$. To derive Z_{DM}, OTA is placed in a feedback configuration similar to BioAmp with both common loads ($Z_{L,1}$) and differential-mode loads ($Z_{L,2}$) present at the output, as shown in Fig. 4.2(c). Using half-circuit model, the odd impedance (Z_{odd})

representing half of Z_{DM} is readily calculated, as follows:

$$Z_{odd} = Z_1 + \frac{(r_{o,p}||r_{o,n})||(Z_{L,1}||\frac{Z_{L,2}}{2}) + Z_2}{1 + Ag_m\Big[(r_{o,p}||r_{o,n})||(Z_{L,1}||\frac{Z_{L,2}}{2})\Big]} \approx Z_1 \tag{4.2}$$

where $r_{o,p}$ and $r_{o,n}$ denote the output resistance of PMOS and NMOS transistors, respectively. Similarly, Z_{CM} is found by taking into account the source degeneration and disregarding $Z_{L,2}$, as depicted in Fig. 4.2(d). Using half-circuit model, the even impedance (Z_{even}), which is twice as large as Z_{CM}, is readily calculated:

$$Z_{even} = Z_1 + Z_p||[Z_2 + (Z_{L,1}||r_{o,p})] \approx Z_1 + Z_2 \tag{4.3}$$

where Z_p denotes the impedance of the parasitic capacitance at each input terminal of OTA. For a typical closed-loop gain of 40 dB, BioAmp requires a capacitive ratio of C_1/C_2=100. Therefore, Z_{CM} of BioAmp is mostly dominated by the equivalent impedance of the feedback capacitor (C_2) and the parallel parasitic capacitance, which is approximated by Z_2.

4.2.2 Electrode-BioAmp Interface

Based on the impedance representation in Fig. 4.2(b), the input impedance of each BioAmp is modeled using a two-port network, and thus an equivalent electrical circuit model for the electrode-BioAmp interface is developed, as depicted in Fig. 4.3. For each channel, Z_{in^+} represents the input impedance seen from the channel electrode accounting for the loading effects of the reference electrode and the remaining BioAmps. Likewise, Z_{in^-} represents the input impedance seen from the reference electrode including the loading effect of channel electrode. By further inspecting the input interface, two observations are made regarding the CMRR degradation.

Unlike the circuit shown in Fig. 4.1(b), the two-port network representation exhibits a "cou-

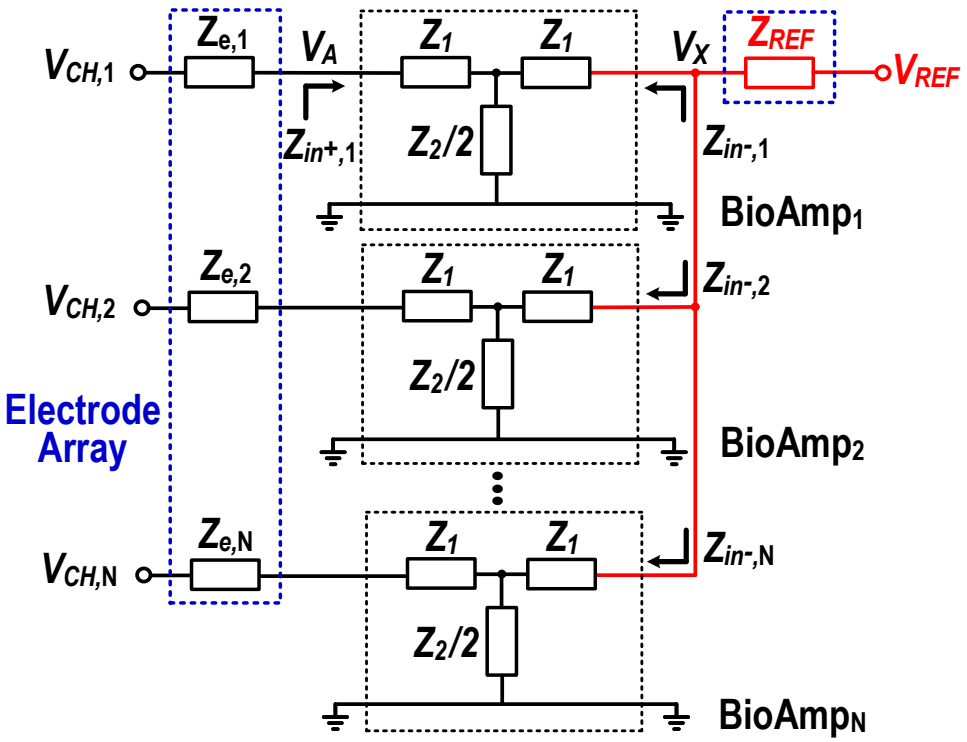

Figure 4.3: Proposed input interface model.

pled path" between nodes A and X [59]. Hence, in the absence of the shared connections at node X, the maximum achievable CMRR for a single channel is mainly determined by impedance mismatch between the channel and reference electrodes relative to Z_{CM}. Meanwhile, the shared connection in N-channel configuration creates unequal loading on each side of the two-port network, which becomes a major source of CMI to DMI conversion. While it is intuitive that the loading effect is more significant on the shared node, the extent of CMRR degradation heavily depends on how CMI appears across the channels with respect to the shared reference electrode, as will be discussed in Section 4.3.2. It is noteworthy that several prior works have employed positive feedback techniques (e.g., capacitive neutralization) to significantly boost Z_{DM} as a way to circumvent the loading effect. However, these techniques are known to pose instability issues, lower Z_{CM}, and degrade the maximum achievable CMRR, as mentioned above.

4.3 Theoretical Analysis

4.3.1 Total and Intrinsic CMRR Derivations

Similar to Eq. (4.1), it is possible to define an overall CMRR for a multi-stage differential system in terms of the following transfer functions: differential-to-differential mode gain (G_{DD}), common-to-common mode gain (G_{CC}), common-to-differential mode gain (G_{DC}) and differential-to-common mode gain (G_{CD}). Following the analysis in [59] and assuming negligible contributions of G_{CD} product terms, the total CMRR for n differential stages in cascade is

$$CMRR_T{}^{-1} \approx \sum_{k=1}^{n} (CMRR_k)^{-1}, \tag{4.4}$$

$$CMRR_k = \begin{cases} \left(\frac{G_{DD}}{G_{DC}}\right)_1, & \text{for } k = 1 \\ \left(\frac{G_{DD}}{G_{DC}}\right)_k \prod_{i=1}^{k-1} \left(\frac{G_{DD}}{G_{CC}}\right)_i, & \text{for } k > 1 \end{cases} \tag{4.5}$$

In a typical biosignal recording system, the first stage consists of the electrode-BioAmp interface, followed by a number of subsequent amplification stages. While it is straightforward to achieve high G_{DD}/G_{CC} ratio for each gain stage by employing a fully differential architecture, it becomes challenging to improve G_{DD}/G_{DC} which is mostly limited by the mismatches associated with on-chip passive and active devices. Since G_{DD}/G_{CC} ratio for each differential amplification stage is very large, $(G_{DD}/G_{DC})_{n=2}$ has dominant effect on the total CMRR. To quantify the main contributing sources to $(G_{DD}/G_{DC})_{n=2}$ (i.e., ICMRR), mismatches are considered for the BioAmp model of Figs. 4.2(c)-(d) and the ICMRR is readily calculated, as follows [60]:

$$\begin{aligned}\frac{1}{ICMRR} &\approx \frac{1}{CMRR_{OTA}} + \frac{1}{CMRR_{FB}} \\ &\approx \frac{\Delta g_{m,A}}{g_{m,A}(1+2g_{m,A}Z_{SS})} + \frac{\frac{\Delta Z_1}{Z_1} - \frac{\Delta Z_2}{Z_2}}{1 - \frac{\Delta Z_1}{2Z_1} + \frac{\Delta Z_2}{2Z_2}}\end{aligned} \tag{4.6}$$

where $[g_{m,A},\Delta g_{m,A}]$, $[Z_1,\Delta Z_1]$, $[Z_2,\Delta Z_2]$ and Z_{SS} represent the mean-value transconductance of OTA's first stage and its mismatch, feedback elements impedance and their associated mismatches and source degeneration impedance, respectively. As seen in Eq. (4.6), the ICMRR is limited by transconductance and feedback impedance mismatches. To minimize the contribution of the former, Z_{SS} can be increased. Meanwhile, the latter term is heavily dependent on the technology node and layout techniques (e.g., minimum unit capacitance, common-centroid placement) which sets an upper-limit for ICMRR if no trimming or enhancement technique is employed.

4.3.2 Input Interface CMRR Derivation

The electrode-BioAmp interface is yet another determining factor that affects the overall CMRR, as it constitutes the first stage of differential acquisition without any amplification. To avoid CMRR degradation, it is imperative to minimize $(G_{DD}/G_{DC})_{n=1}$ which is mainly determined by the impedance imbalance in the interface. In this work, the extent of impedance imbalance between nodes A and X for a given channel (BioAmp_1 in Figs. 4.4(a)-(b)) is studied for two general case scenarios of CMI. Starting with Fig. 4.4(a), CMI is assumed to be uniformly present across all channels with respect to the reference electrode. The common-mode AC currents passing through the channel and reference electrodes are absorbed by Z_{CM} of each BioAmp. Thus, it can be mathematically shown that the shared node experiences less loading effect as the equivalent input impedance looking into all remaining BioAmps is $\approx 2Z_{CM}/(N-1)$, which is much larger than Z_{REF}. On the other hand, if only one channel experiences CMI with respect to the reference electrode (BioAmp_1 in

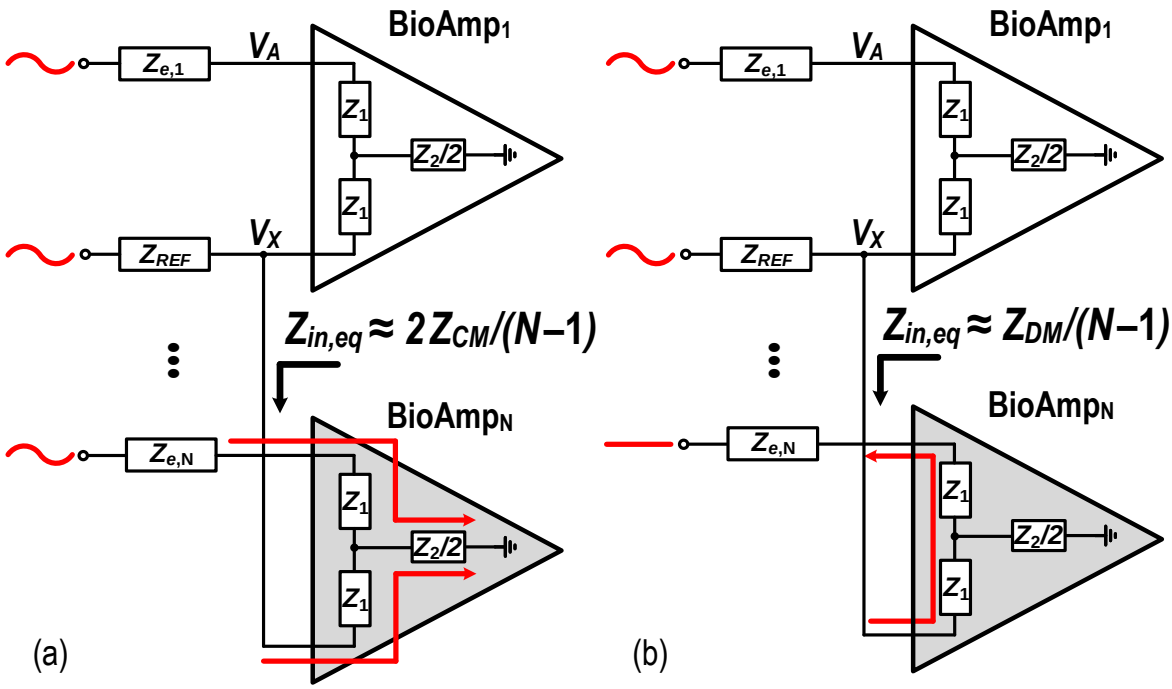

Figure 4.4: Electrode-BioAmp interface with (a) CMI across all channels (b) CMI across a single channel.

Fig. 4.4(b)), the equivalent input impedance at the shared node looking into all remaining BioAmps is significantly reduced, giving rise to severe loading effect. Depicted in Fig. 4.4(b), the AC current flowing from the reference electrode into the interference-free BioAmps circulates back through the channel electrodes provided that $(Z_{e,j} + Z_1) \ll Z_2$ for $j = 1, ..., N$, which holds true for a typical BioAmp. Hence, the equivalent input impedance looking into BioAmps reduces to $\approx Z_{DM}/(N-1)$, causing significant CMRR degradation.

Since loading on the shared node depends on the number of channels experiencing CMI with respect to the reference electrode, it becomes a necessity to obtain the input interface CMRR, $(G_{DD}/G_{DC})_{n=1}$, for a given channel (e.g., BioAmp$_1$) in terms of the voltage transfer functions (TFs) from all inputs to node A and X. For this reason, five distinct voltage TFs are identified in the input interface: (I) $V_A/V_{CH,1}$, (II) $V_A/V_{CH,m}$ where $m = 2, ..., N$, (III) V_A/V_{REF}, (IV) V_X/V_{REF} and (V) $V_X/V_{CH,j}$ where $j = 1, ..., N$. Shown in Fig. 4.5(a), each TF is distinguished by its signal path marked with an arrow. In addition, the channel

electrode and T-network impedances are substituted by a π-equivalent circuit, as seen in the dotted boxes. It is worth noting that contributions from TF-II is negligible and therefore, is not considered in the derivations for the sake of brevity.

To find an expression for TF-I, -III and -IV, $Z_{in^+,1}$ and $Z_{in^-,j}$ for $j = 1, ..., N$ should be derived. To begin with, Z-parameters of the two-port network modeling the BioAmp are calculated, as follows:

$$Z_{param} = \begin{bmatrix} Z_1 + Z_2/2 & Z_2/2 \\ Z_2/2 & Z_1 + Z_2/2 \end{bmatrix} \tag{4.7}$$

Subsequently, $Z_{in^+,1}$ terminated by Z_L is determined:

$$Z_{in^+,1} \triangleq Z_{11} - \frac{Z_{12}Z_{21}}{Z_{22} + Z_L} = (Z_1 + Z_L)||(Z_2/2) + Z_1 \tag{4.8}$$

where

$$Z_L^{-1} = Z_{TOT}^{-1} + Z_{REF}^{-1} \tag{4.9}$$

and

$$Z_{TOT}^{-1} = \sum_{i=2}^{N} (Z_{in^-,i})^{-1} \tag{4.10}$$

Similarly, $Z_{in^-,j}$ terminated by the channel electrode, $Z_{e,j}$ for $j = 1, ..., N$, is calculated to be:

$$Z_{in^-,j} \triangleq Z_{22} - \frac{Z_{21}Z_{12}}{Z_{11} + Z_{e,j}} = (Z_1 + Z_{e,j})||(Z_2/2) + Z_1 \tag{4.11}$$

By examining the equivalent circuit of Fig. 4.5(b)(i), TF-I is derived in terms of $Z_{in^+,1}$ and Z_L, expressed in Eqs. (4.8) and (4.9):

$$\frac{V_A}{V_{CH,1}} = \frac{1}{1 + Z_{e,1}/Z_{in^+,1}} \tag{4.12}$$

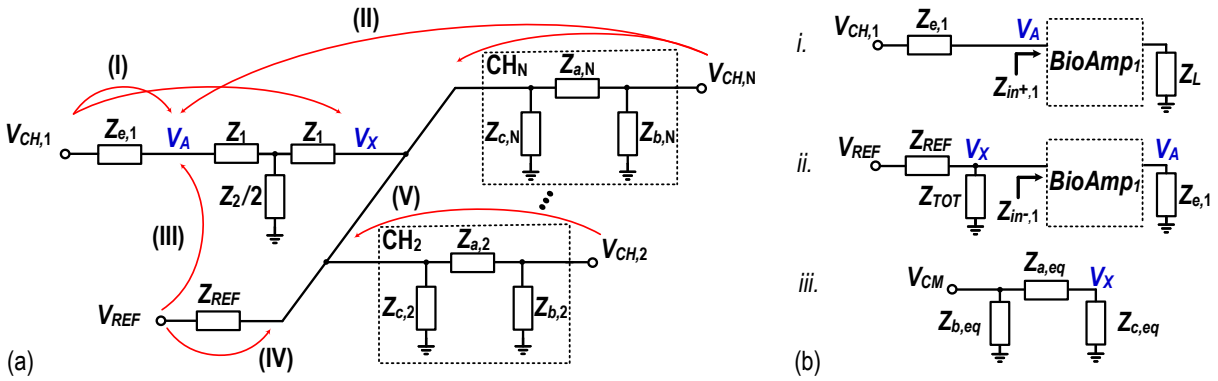

Figure 4.5: (a) Signal paths in the input interface considered for voltage transfer function analysis (b) equivalent circuits.

Similarly, TF-III and TF-IV are calculated based on the equivalent circuit of Fig. 4.5(b)(ii), i.e.,

$$\frac{V_A}{V_{REF}} \approx \frac{Z_{e,1}/Z_{REF}}{1 + Z_{in^-,1}/Z_L} \tag{4.13}$$

$$\frac{V_X}{V_{REF}} = \frac{1}{1 + Z_{REF}\sum_{i=1}^{N} Z_{in^-,i}^{-1}} \tag{4.14}$$

In deriving Eq. (4.13), it is assumed $Z_2 \gg Z_1 + Z_{e,1}$, which holds true for a typical BioAmp.

The π-equivalent circuit for each channel, as depicted in Fig. 4.5(a), helps simplify the calculations involving the effect of TF-V. By applying Y-Δ transformation, each impedance in π-network is readily expressed for the j-th channel, as follows:

$$Z_{a,j} = Z_{e,j} + 2Z_1 + \frac{2(Z_{e,j} + Z_1)(Z_1)}{Z_2} \tag{4.15}$$

$$Z_{b,j} = Z_{e,j} + Z_1 + Z_2(1 + \frac{Z_{e,j}}{2Z_1}) \tag{4.16}$$

$$Z_{c,j} = Z_1 + \frac{Z_2}{2}(1 + \frac{1}{1 + \frac{Z_{e,j}}{Z_1}}) \tag{4.17}$$

Assuming that CMI appears across the reference and M-number of channels, the equivalent circuit of Fig. 4.5(b)(iii) is obtained by merging parallel π-networks with Z_{REF}, whose equivalent impedances are derived, as follows:

$$Z_{a,eq}^{-1} = \sum_{i=1}^{M} (Z_{a,i})^{-1} + Z_{REF}^{-1} \tag{4.18}$$

$$Z_{b,eq}^{-1} = \sum_{i=1}^{M} (Z_{b,i})^{-1} \tag{4.19}$$

$$Z_{c,eq}^{-1} = \sum_{i=1}^{M} Z_{c,i}^{-1} + \sum_{i=M+1}^{N} Z_{in^-,i}^{-1} \tag{4.20}$$

Hence, the total voltage contribution to node X (i.e., summation of TF-IV and TF-V) is readily calculated:

$$\frac{V_X}{V_{CM}} = \frac{Z_{c,eq}}{Z_{a,eq} + Z_{c,eq}}, \tag{4.21}$$

Based on Eqs. (4.12), (4.13) and (4.14), the input interface differential-to-differential mode gain ($G_{DD,int}$) is defined:

$$\begin{aligned} G_{DD,int} &\triangleq (V_A - V_X)/V_{DM} \\ &= \Big(\frac{V_A}{V_{CH,1}} - \frac{V_A}{V_{REF}} + \frac{V_X}{V_{REF}}\Big)\Big|_{V_{CH,1}=V_{REF}=V_{DM}} \end{aligned} \tag{4.22}$$

The voltage contribution of $\big(V_X/V_{CH,1}\big)|_{V_{CH,1}=V_{DM}}$ is omitted from the above expression since it has negligible effect. Similarly, based on Eqs. (4.12), (4.13) and (4.21), the input interface common-to-differential mode gain ($G_{DC,int}$) is defined:

$$\begin{aligned} G_{DC,int} &\triangleq (V_A - V_X)/V_{CM} \\ &= \Big(\frac{V_A}{V_{CH,1}} + \frac{V_A}{V_{REF}}\Big)\Big|_{V_{CH,1}=V_{REF}=V_{CM}} - \frac{V_X}{V_{CM}} \end{aligned} \tag{4.23}$$

Finally, the total and the input interface CMRR, assuming ($Z_2 \gg Z_1 \gg Z_{REF}, Z_{e,j}$ for $j = 1, ..., N$), are derived:

$$\frac{1}{CMRR_T} = \frac{1}{ICMRR} + \frac{1}{CMRR_{int}} \tag{4.24}$$

$$CMRR_{int} = \left(\frac{G_{DD}}{G_{DC}}\right)_{int} = \frac{1 + \dfrac{1}{1 + \frac{Z_{REF}}{2Z_1} \times N}}{1 - \dfrac{1}{1 + \dfrac{Z_{REF}}{\frac{Z_2}{M} || \frac{2Z_1}{N-M}}}} \tag{4.25}$$

where $ICMRR$ is previously defined in Eq. (4.6). The closed-form expression in Eq. (4.25) shows that for an N-channel acquisition front-end, the maximum CMRR is achieved when $M{=}N$ and degrades with higher values of N.

4.4 Numerical Results

In this section, theoretical and circuit simulation results for a previously designed and fabricated 32-channel neural recording system in a 180nm CMOS process [51] are presented.

4.4.1 BioAmp CM & DM Input Capacitance

Simulated input capacitance of the BioAmp in [51] are compared with the model of Section 4.2.1. Each input and feedback capacitor is realized using MIM stacked structure with a capacitance of 18 and 0.2 pF, respectively. Common-mode (CM) and differential-mode (DM) capacitance for the BioAmp are shown in Fig. 4.6. Given that CM capacitance deviates from the ideal value of 0.4 pF, a behavioral model is used for de-embedding the parasitic

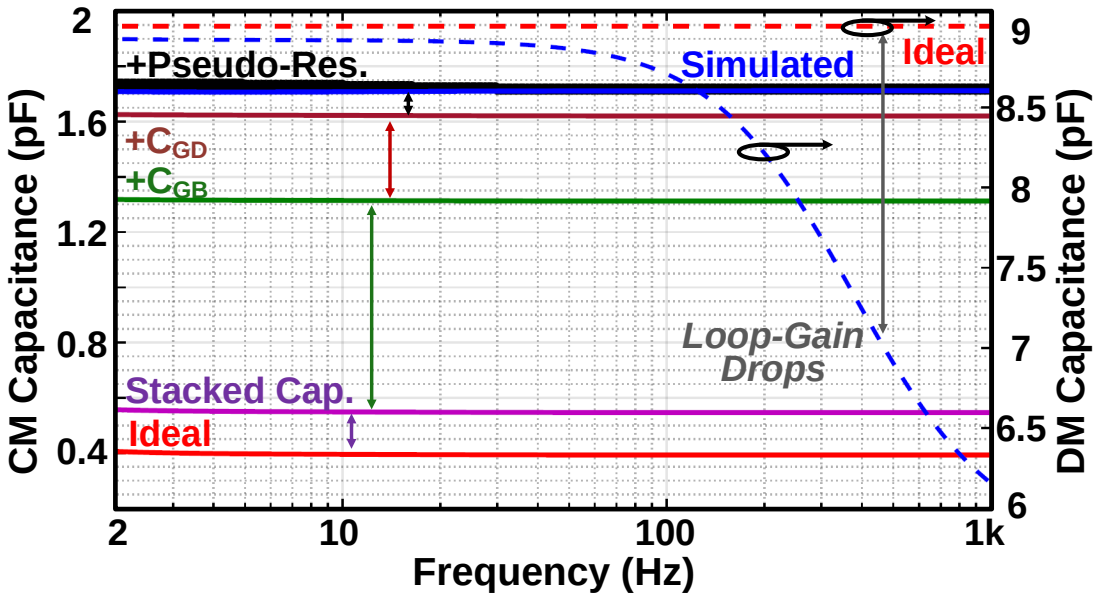

Figure 4.6: CM and DM capacitance seen from the input terminals of BioAmp (red and blue traces depict the ideal and simulated results, respectively).

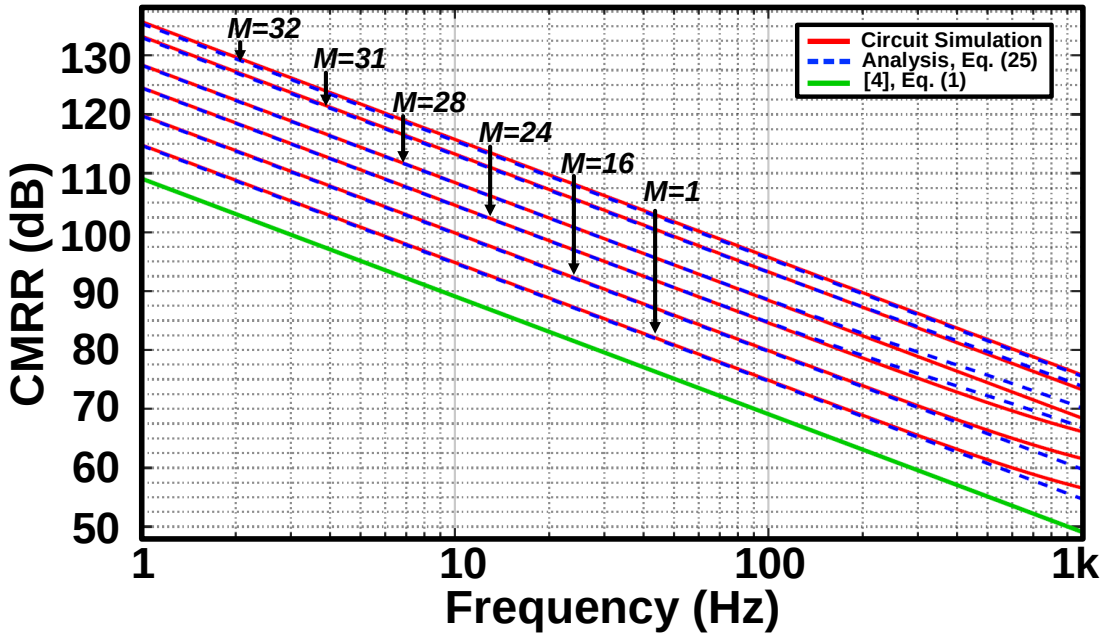

Figure 4.7: Simulated and predicted $\mathrm{CMRR}_{\mathrm{int}}$ given M-number of channels experiencing CMI in a 32-channel neural recording system.

capacitances which contribute ∼640fF to each input terminal of OTA. Since no chopping mechanism is employed in the BioAmp, the input pair transistors are sized adequately to reduce flicker noise and therefore, introduce significant gate-to-bulk (C_{GB}) and gate-to-drain (C_{GD}) parasitic capacitance. Furthermore, DM capacitance decreases as the loop gain of the BioAmp drops beyond the 3-dB bandwidth which gives rise to higher impedance, as predicted by Eq. (4.2) and deduced from Fig. 4.6.

4.4.2 Input Interface CMRR

The simulated input interface CMRR of the fabricated 32-channel electrocorticography (ECoG) acquisition front-end in [51] is compared with Eq. (4.25) and the second term of Eq. (4.1). Shown in Fig. 4.7, the simulated and predicted $\mathrm{CMRR_{int}}$ versus frequency is plotted for different values of M, assuming an electrode impedance of 1 kΩ (typical for ECoG electrodes). As depicted, the CMRR degradation due to the impedance imbalance increases with fewer number of channels experiencing CMI with respect to the reference electrode, which closely follows the analysis in this work. Assuming that $ICMRR$ and electrode mismatches are not the limiting factors, the maximum achievable CMRR ($CMRR_{max}$), coinciding with M=N, is found by evaluating Eq. (4.25) and Eq. (4.1) for different number of channels and the same impedance values (at 1 kHz) used in Section 4.4.1, as shown in Fig. 4.8.

4.5 Conclusion

In this brief, a detailed analysis of CMRR degradation is presented based on a proposed electrical circuit model of the input interface for a multi-channel biosingal recording system, exhibiting close agreement with circuit simulations.

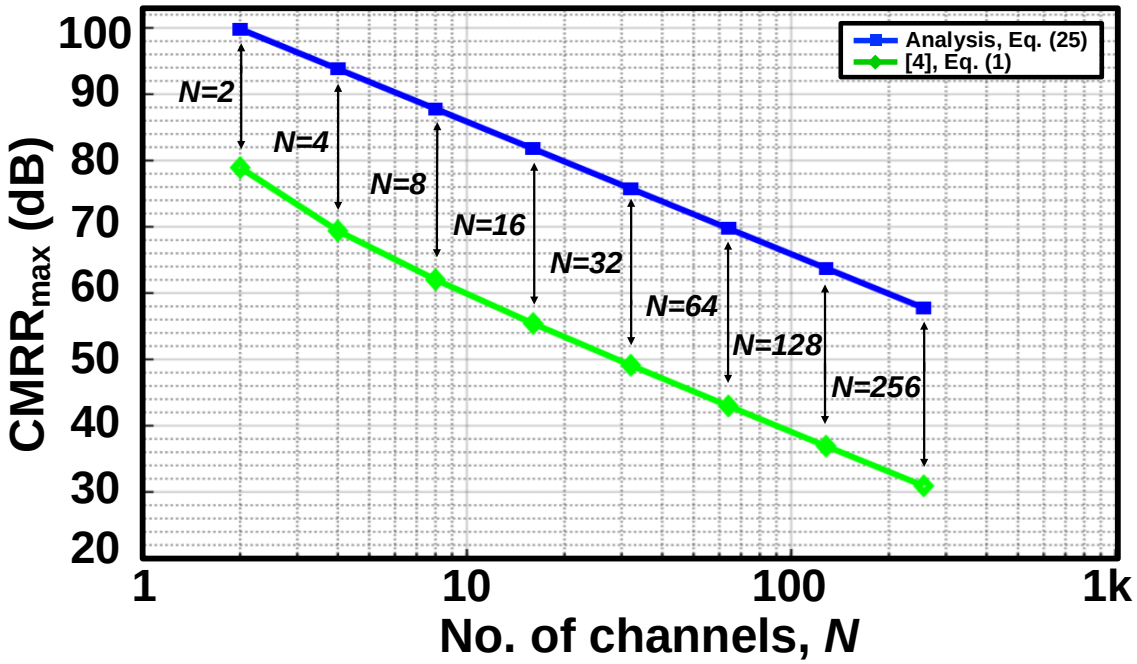

Figure 4.8: Maximum achievable CMRR for a multi-channel biosignal acquisition.

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