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Diagnostic Analysis of Silicon Strips Detector Readout in the ATLAS Semi-Conductor Tracker Module Production

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Abstract

The ATLAS Semi-Conductor Tracker (SCT) Collaboration is currently in the production phase of fabricating and testing silicon strips modules for the ATLAS detector at the Large Hadron Collider being built at the CERN laboratory in Geneva, Switzerland.
A small but relevant percentage of ICs developed a new set of defects after being mounted on hybrids that were not detected in the wafer screening. To minimize IC replacement and outright module failure, analysis methods were developed to study IC problems during the production of SCT modules.
These analyses included studying wafer and hybrid data correlations to finely tune the selection of ICs and tests to utilize the ability to adjust front-end parameters of the IC in order to reduce the rejection and replacement rate of fabricated components.
This paper will discuss a few examples of the problems encountered during the production of SCT hybrids and modules in the area of ICs performance, and will demonstrate the value of the flexibility built into the ABCD3T chip.

Keywords: ATLAS SCT; silicon detector; IC; ABCD3T;

1. Introduction

The ATLAS Semi-Conductor Tracker SCT [1] will consist of 4 cylindrical layers (barrel) in the central region of the Inner Detector [2], at 300, 373, 447, and 520 mm radii from the beam line, and 9 end-cap disks on each side of the barrel detector. The barrel and end-cap are populated with 4,088 silicon strips modules [3] [4] with a total area of silicon of 61 m^2. The ATLAS SCT module is built with two pairs of identical, single-sided silicon micro-strip sensors (768 AC-coupled, p-strips on n-type silicon, 80 μm strips pitch) glued back-to-back, with a 40 mrad stereo angle on a mechanical core (baseboard) made of thermal pyrolitic graphite (TPG) to transfer the heat generated by the readout electronics and sensors to the cooling pipe.

Each pair of strip sensors is wire-bonded to form double-long strips of 126 mm length. A hybrid flexible circuit made of copper/polyimide laminate is wrapped around the two sides of the sensors at the center of the module, bridged over the sensors.

The front-end readout of the SCT is handled by ASICs realized in the radiation hard DMILL technology as will be discussed in the next section. There are 12 ASICs on a module and they are glued and bonded on the hybrid, 6 on each side of the module. The full SCT requires ~50,000 ICs for a total of 6.2 million readout channels.

ASICs were tested on wafer at three institutes (CERN, Rutherford Appleton Lab and the Santa Cruz Institute for Particle Physics). During the wafer screening the ASICs were tested to verify their analogue front-end performance, such as gain and noise level, and their digital functions. They

were graded according to electrical specifications and then picked (diced) to be used on modules.

The production of the barrel modules is carried out by clusters of institutes from Japan, Scandinavia, UK and the USA. The end-cap modules are produced in Australia, Germany, Netherlands, Spain, Switzerland and the UK. Barrel module production is almost completed and the end-cap is underway. All modules need to satisfy several mechanical and electrical specifications and are classified following a highly controlled quality assurance process to achieve the same quality of production across multiple assembly sites. Similarly to the wafer screening, the front-end readout electronic on hybrid is tested for the uniformity of the threshold, response in the gain, timing, noise levels and noise occupancy per channel. The testing method is presented in section 3.

During the module production phase, a small but relevant percentage of the ASICs mounted on hybrids, but graded to be within the "perfect chip" specifications at the wafer level, developed new set of defects. Some of these unexpected defects turned out to be due to a higher sensitivity for some of the ASICs to small differences in the operating conditions. As discussed in section 4, this led to the development of dedicated analyses which took advantage of the flexibility built into the ASIC to adjust its front-end parameters, and included the correlation studies of the module response with the results obtained during the wafer screening.
In section 5 we present the studies performed in the case of two defects observed in the ASICs after being mounted on hybrids. Solutions were found that allowed us to keep using those chips. During the module production it was important to minimize IC replacement and outright module failure. These studies we are also demonstrating the value of the flexibility built into the ABCD3T chip.

2. The ATLAS SCT Readout electronics

The front-end readout of the SCT consists of ASICS realized in the radiation hard DMILL technology, named ABCD3T [5], featuring a 128-channel analogue front-end consisting of amplifiers and comparators, and a digital readout circuit, and operating at the LHC bunch crossing frequency of 40 MHz. The ABCD3T chip utilizes a "binary" scheme where the signals from the silicon detector are amplified and then compared to a threshold. Only the result of this comparison, based on a hit or no-hit logic, enters the input register and the digital pipeline. The channel-to-channel matching, although acceptable for the non-irradiated chips, is expected to deteriorate significantly in the lifetime of the experiment. To ameliorate this effect, an internal 4-bit trim DAC controlling the comparator offset is used for each channel [6]. The DAC has 4 selectable ranges. Because the optimum values of the currents required by the front-end amplifier decrease with irradiation, two 5-bit DACs are also implemented in the chip to adjust the operating point of the front-end amplifier: one to set the current in the front-end transistor (Preamp current) and the other to set the bias of the second stage amplifier and comparator (Shaper current or Ish).

The ABCD3T chip also contains a dedicated internal charge injection circuit to calibrate the chip. A voltage step across the calibration capacitor produces a charge being injected into the front-end of the chip with variable amplitude controlled by an 8-bit DAC which could range from 0 to 16 fC.

The calibration pulses are issued with a delay (Strobe Delay) relative to the clock. It is necessary to adjust the Strobe Delay for each chip to account for variations in the propagation delay of the integrator-comparator.

Wafers of 256 IC's were fabricated by ATMEL (Nantes, France).

Beyond the wafer fabrication by the foundry, the collaboration took responsibility for the rest of the production process. The various tasks were split over many institutes in order to share the work among the available resources. The wafer testing was shared by three institutes (CERN, Rutherford Appleton Lab and the Santa Cruz Institute for Particle Physics). The wafer sawing and chip picking was performed by third party vendors.

The complexity of the ABCD3T chip demanded the design and implementation of a sophisticated tester [7] to verify the analogue front-end

performance (gain and noise), the digital functions (control register, addressing, communication, pipeline, and output buffer), the power consumption, the linearity of the DACs, and the I/O Signals properties (timing, amplitudes, and duty cycles). The testing rate was 5 hours/wafer.

ASICs were graded into the following main classifications: a) Perfect (meets all specifications) b) 1 bad-channel (IC meets all specifications except for 1 channel) c) 2 bad-channel (IC meets all specifications except for 2 channels) d) Digitally perfect (passes all digital tests except perhaps full pipeline and has more than 2 bad channels) e) Bad (all else).

Tests of 1-bad-channel ICs in modules including irradiations have not shown any extra reliability problems beyond the loss of 1 channel.

3. SCT Hybrid Testing: method and typical results

An extensive suite of both hardware and software [8] has been developed to facilitate hybrid and module testing. The readout system is based on custom designed VME boards including low voltage and high voltage boards [9] [10] developed specifically for SCT production testing.

Two automated series of tests have been designed to simplify the testing procedure: a) characterization sequence aimed to perform a full characterization of a hybrid or a module for both digital and analogue performance and b) confirmation sequence with a reduced set of tests to ensure the basic digital and analogue functionality of the chips. The performance of the analogue part of the chip for each channel, such as gain, offset, noise, is tested by using the internal calibration circuit of the ABCD3T chip.

The basic method for the characterization of the analog circuitry of the ABCD3T chip consists of an efficiency scan for different discriminator threshold values with a fixed calibration charge. A typical "S-curve" from this measurement is shown in fig. 1, fitted to a complementary error function. The 50% point (vt50) indicates the threshold value which corresponds to the injected charge after amplification, and the width characterizes the output noise.

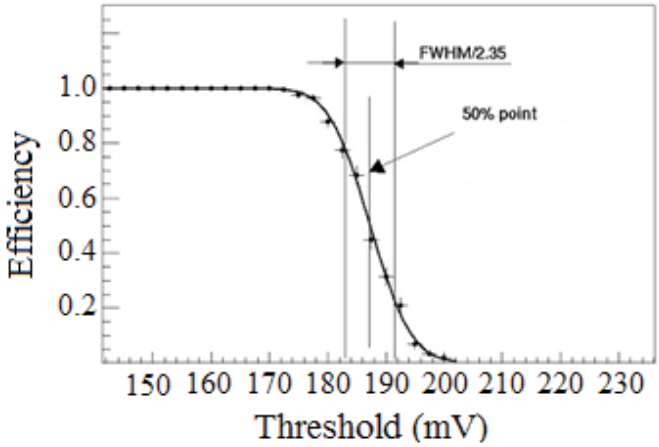

Fig.1. Example of a threshold scan for a singe channel with fixed injected charge. The midpoint of the transition gives the value of the threshold equal to the injected pulse after amplification. The width of the transition measures the electronic noise. The histogram is fitted to a complementary error function.

To measure the gain and offset, we perform a scan at three different calibration input charges (from 1.5 fC to 2.5 fC) in the confirmation sequence and ten charge values (from 0.5 fC to 8 fC) in the characterization sequence. The set of vt50 points versus calibration charge amplitude is the response curve of each channel. The gain is determined by the slope of a polynomial fit to the response curve, the offset is the intercept at zero charge injection and the input noise is determined by dividing the output noise by the gain. A typical set of plots that are obtained with a full characterization is shown for the 768 channels of the top side of a module (6 chips, 128 channels/chip) in fig. 2. Prior to the efficiency scan the optimal delay (Strobe Delay) of the input charge with respect to the clock for every chip must be determined. This is obtained with a Strobe Delay scan performed as the very first of the analogue test sequence to determine the correct Strobe Delay setting which is used during the analogue tests. A 4fC signal at 2 fC threshold is injected (using the internal calibration circuit) as the Strobe Delay is varied. A fit is made to both the rising edge and the falling edge of the signal to find the points at which the 50% efficiency is achieved.

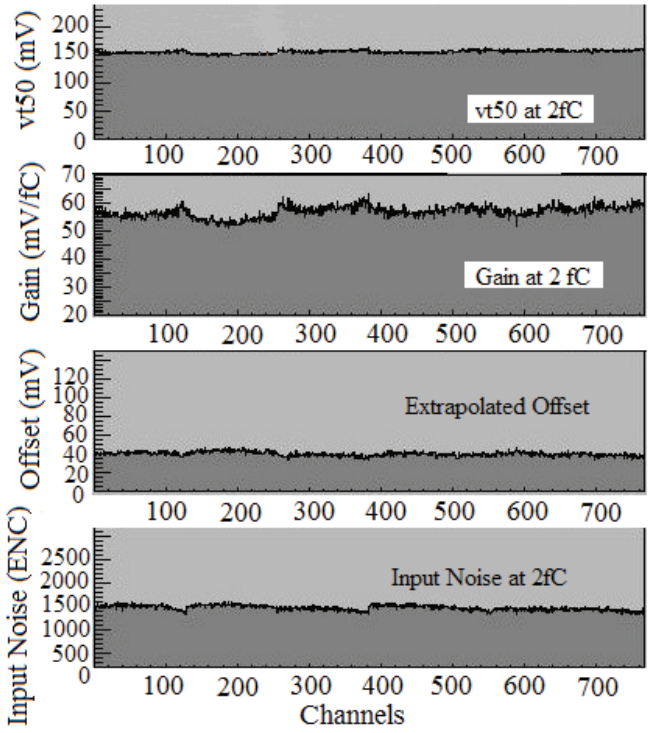

Fig.2. A set of plots obtained with a full characterization tests shown for the 768 channels of the top side of a module (6 chips, 128 channels/chip). The first plot (from the top) is the vt50, the second is the gain, the third is the offset, and the fourth is the input noise, for each channel.

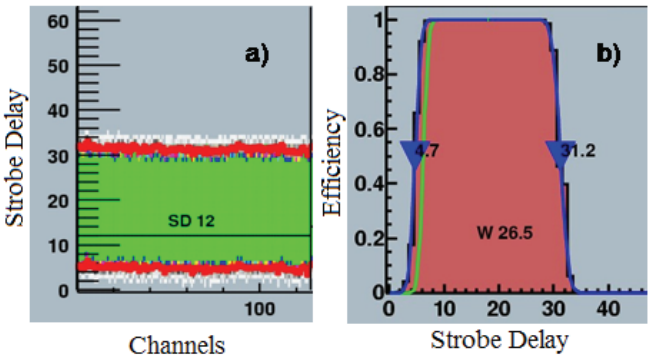

Fig.3. a) Strobe Delay at the 25% of the distance between minimum and maximum delay (horizontal line); b) the fit to both the rising edge and the falling edge of the signal to find the points at which the 50% efficiency is achieved as the Strobe Delay varies.

The Strobe Delay is then taken at the 25% of the distance between those two points with the reference to the rising edge of the Strobe Delay peak which correspond to the falling edge of the signal. Fig. 3a shows an example of a Strobe Delay plot and fig. 3b shows the signal efficiency fit for one chip. The horizontal line in fig. 3a indicates the 25% of the distance from the minimum delay.

4. Diagnostic Analysis Methods

A small but relevant percentage (< 5%) of IC's that met all the specifications at the level of wafer testing, developed a new set of defects after being mounted on production hybrids. While defects in the digital circuitry were considered as fatal and the chips were replaced, some of the defects in the analogue circuitry were instead studied to see if the performance of the ASIC could be improved by adjusting its front-end parameters. Small differences in the operating conditions of the two testing phases (wafer screening and hybrid tests), turned out to be the primary reason for the appearance of some of the new defects. This fact helped in identifying the area of sensitivity of the defective chips that needed to be studied. As described in Section 2, because of degradation due to irradiation, the ABCD3T chip provides the feature of adjusting the operating point of the front-end parameters such as the preamplifier and the shaper current (Ish). For the same reason, the analogue and digital voltage can also be adjusted. The capability of adjusting the Strobe Delay was also used in the analysis of defective chips. By measuring the response versus the Strobe Delay we were able to determine the transit time and the rise time of each channel. This flexibility of the chip turned out to be very important during production testing and was used as a tool for the diagnostic analysis. Software was also developed to study the data from the wafer screening. Useful information for the studies was: various settings parameters; gain and noise response of the chips, analogue current drawn individually by every chip (Icc) when the analogue supply voltage is applied; and the front-end DACs values. Correlation studies between wafer screening quantities and the results obtained from the same chips mounted on hybrids were performed.

5. Study of Defective ASIC

Amongst those defects that were considered for study we had: a) a very large spread of gain in all channels, a defect classified as "Large Gain Spread" (LGS) (fig. 4) and b) a block of contiguous channels for which the measured gain is 10% to 20% lower than their neighbours and the measured input noise is high (fig. 5).

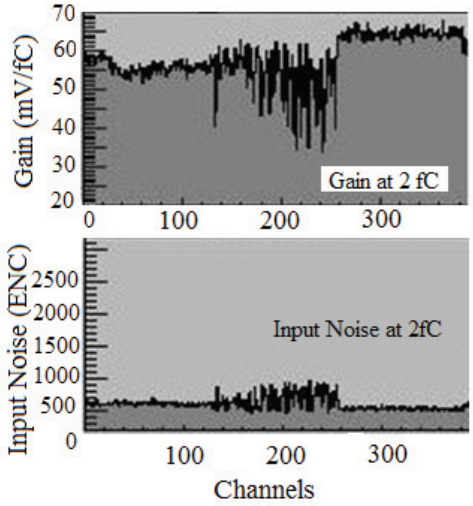

Fig.4. Example of LGS defect in the Gain (top) and the Noise (bottom). The second chip of the three chips shown here has the LGS defect.

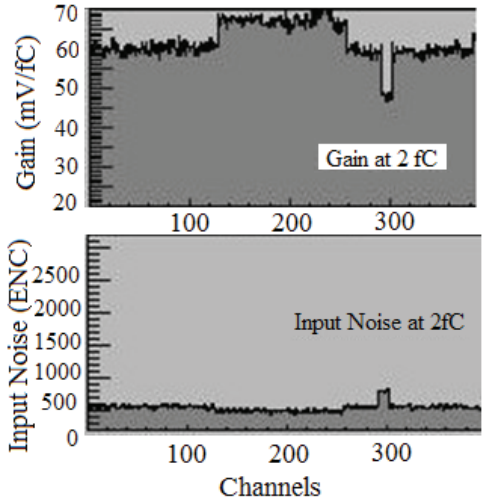

Fig.5. Example of BLG defect in the Gain (top) and the Noise (bottom). The third chip of the three chips shown here has the BLG defect.

This defect was called Block Low Gain (BLG). In the next two sections of this paper we will discuss the above effects. Solutions were found that saved a large fraction of the chips which otherwise would have been replaced.

5.1 Large Gain Spread (LGS)

Fig. 4 shows an example of a chip with the Large Gain Spread (LGS) defect. We used the data from the wafer screening to perform a comparison between the gain response of the twelve chips on the hybrid and the same chips when tested on the wafer. The result is shown in fig. 6.

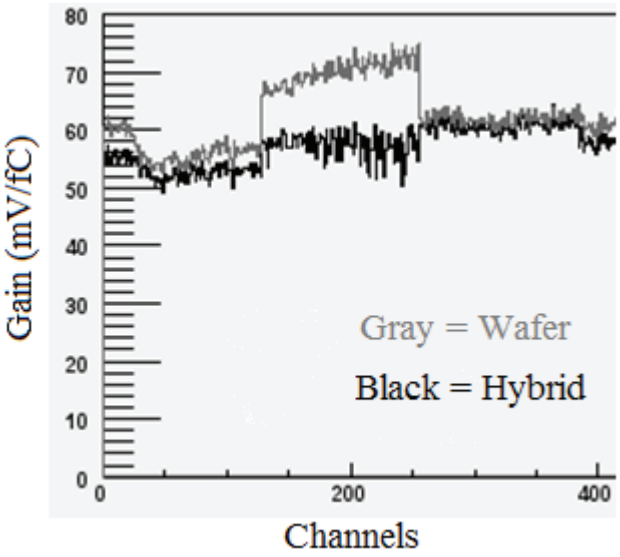

Fig.6. Wafer gain data (gray) compared to hybrid gain data (black) for 3 chips. The second chip has LGS.

The large difference in the gain of the defective chip between the wafer and hybrid test suggests sensitivity to the small differences in the operating conditions of the two tests. Fig 7 shows the gain vs Ish for four chips which show LGS and four normal chips. Clearly the LGS chips are much more sensitive to changes in Ish. Fig. 8 shows the gain vs Vcc (the analogue supply voltage) for a LGS chip (chip 9 in the figure) for three values of Ish and for a normal chip (chip 0). The slope for the LGS chip is significantly greater at the nominal value of Ish (30 µA) than at a lower value of Ish. Fig. 9 shows the rms of the gain in LGS chips and normal chips vs Ish. Lowering Ish to 20 µA brought most of the LGS chips into a satisfactory operating region.

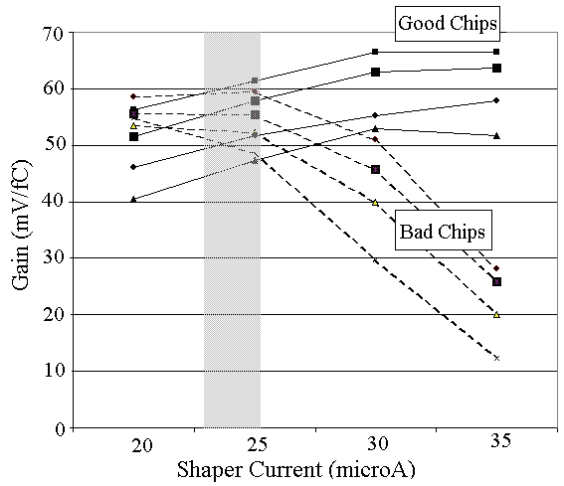

Fig.7. Gain vs Ish for good chips and LGS chips. T=0°C and Vcc=3.5 V (nominal).

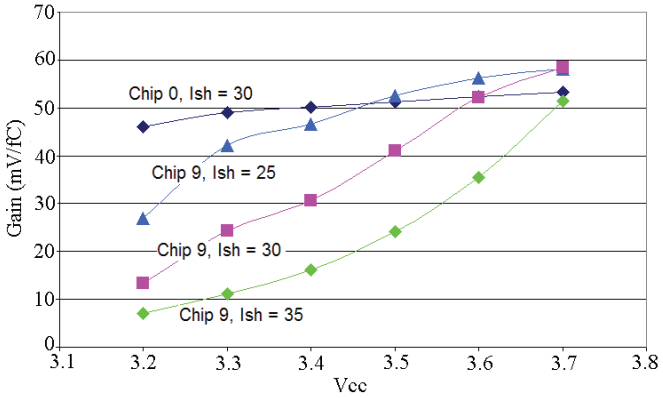

Fig.8. Gain vs Vcc of a LGS chip (Chip 9) at different Ish settings compared to a good chip (Chip 0) at nominal Ish setting.

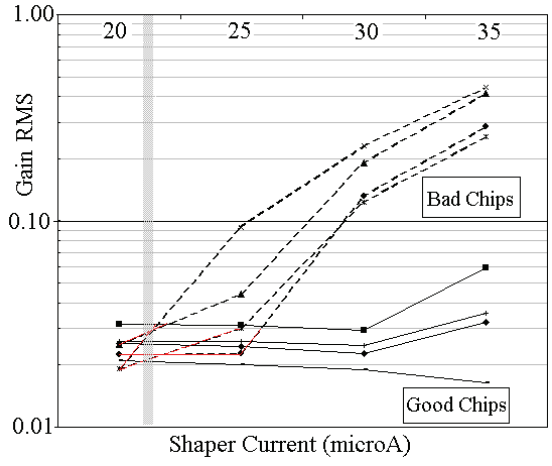

Fig.9. Gain RMS vs Ish for good chips and LGS chips. T=0°C and Vcc=3.5 V (nominal). The "gray" band indicates thee range of Ish at which the bad chips behave like good chips.

We also looked at the values of Icc of individual chips as measured on the wafer (on the hybrid we measure the overall Icc for all twelve chips) and we found a strong correlation between high Icc and chips with LGS. At the nominal value of the shaper current (30 µA), Icc for chips with the LGS defect is typically 20% higher than average, but that was not considered enough of a deviation for rejecting the chips during the wafer screening. Fig. 10 is a distribution of Icc for all chips from one particular wafer. The two chips with higher Icc are the ones that later on showed the LGS effect on the hybrid.

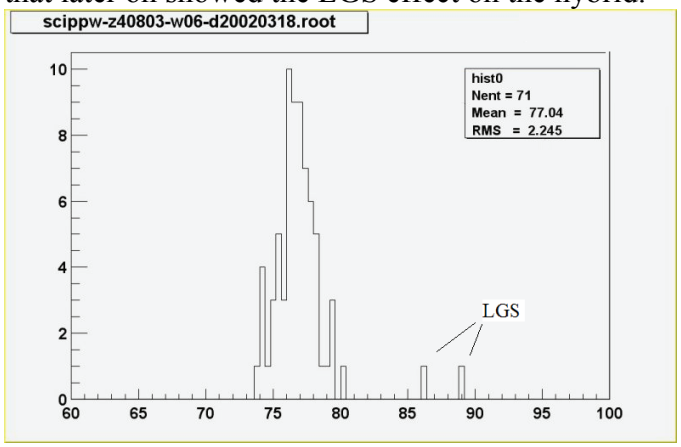

Fig.10. Distribution of Icc for chips coming from the same wafer.

We also analyzed the first 100 production hybrids and by looking at the deviation of Icc from the mean value of Icc per hybrid (fig. 11) we confirmed the strong correlation between higher Icc on wafers and LGS defects on hybrids.

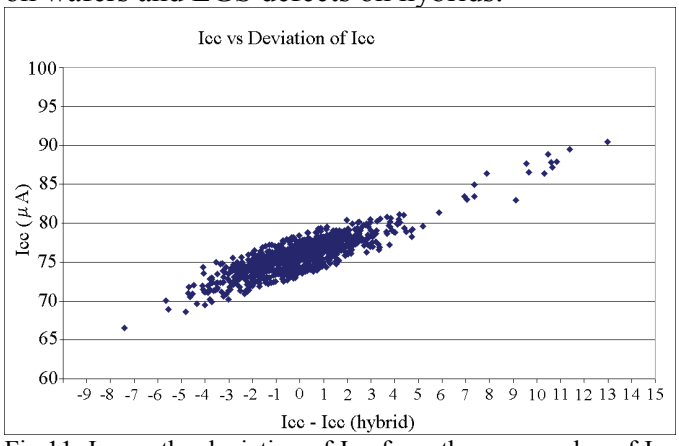

Fig.11. Icc vs the deviation of Icc from the mean value of Icc per hybrid for 100 production hybrids. All the chips known having the LGS defect correspond to the points above a deviation of 5 µA and higher Icc.

As it could be seen in the same figure, there are 17 points with higher Icc and larger deviation from

the mean Icc. Those points correspond to the chips with LGS defect.

A cut on Icc in the wafer data was then adopted to pre-select chips and to keep aside suspected chips with the LGS defect in the construction of subsequent hybrids. For the chips already used and that showed LGS we used a lower Ish setting, as demonstrated being a cure for this defect.

5.2 Block Low Gain (BLG)

The "Block Low Gain" (BLG) defect is seen as a block of continuous channels showing low gain and correspondingly higher noise (fig. 5). The noise was a critical issue and the reason for which this defect needed to be addressed since these channels failed the nominal noise cut. The wafer/hybrid comparison for the same chip (in fig. 12 it is the ninth chip) shows on the contrary that this chip has a block of high gain channels.

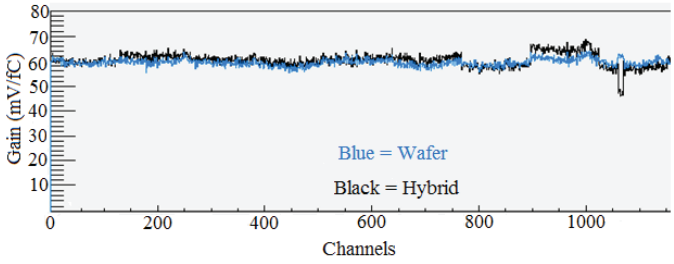

Fig 12. Wafer gain data (blue) compared to hybrid gain data (black) for 9 chips. The ninth chip has BLG. This is the same as the third chip on fig5.

This finding suggests that this defect as seen on the hybrid might be explained with a timing problem. For the channels that have indeed a higher gain the pulse is likely to start in the preceding time bucket. Fig. 13 shows the Strobe Delay plot for the three of the same group of chips of one side of the module (bottom side). The 3rd chip is the one with BLG and the affected channels have a longer Strobe Delay indicating that they have a shorter propagation delay. In the same figure the optimal Strobe Delay is shown at the 40% of the plateau. Studies of the Strobe Delay were conducted on hybrids with chips showing the BLG effect.

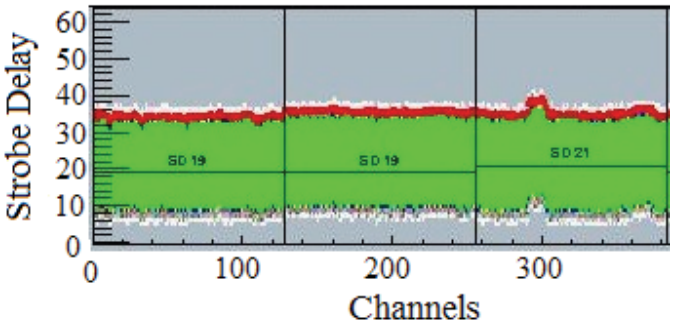

Fig.13. Strobe Delay plot for 3 chips. The horizontal line (per each chip) indicates the 40% from the rising edge of the Strobe Delay peak which correspond to the falling edge of the signal.

Fig. 14 shows (a) the gain and (b) the input noise as a function of the Strobe Delay averaged over 10 affected channels and 10 normal channels. The channels with the BLG defect reach a normal condition at a longer Strobe Delay and a significantly higher gain. The excess noise at the nominal Strobe Delay is apparently an artefact of using a too short Strobe Delay and it disappears as the Strobe Delay is increased.

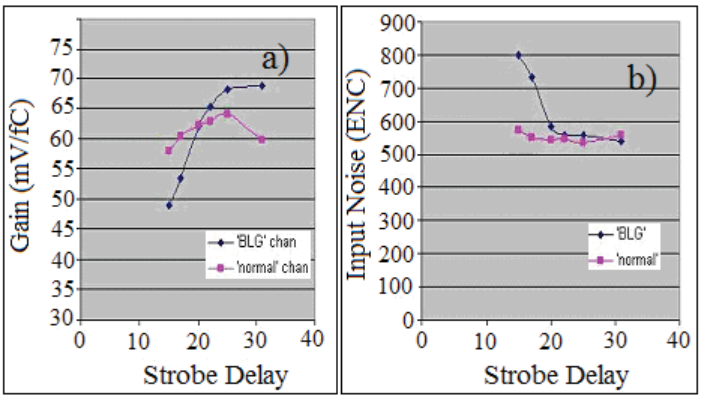

Fig.14. Gain and Input Noise vs Strobe Delay.

A hybrid built at UCSC with 2 chips showing this problem was irradiated with $2x10^{14}n/cm^2$ (1 MeV NIEL equivalent in Si) in the reactor in Ljubljana [11]. By comparing the Strobe Delay plots before and after irradiation we concluded that the radiation slows down the chip causing the Strobe Delay to decrease uniformly. The 'BLG' channels then become normal with the standard Strobe Delay after irradiation. The symptoms improve when Ish is lowered for the same reason.

About 2% of the chips used show the BLG defect and they can be used with a longer Strobe Delay.

6. Conclusions

During the SCT module production we were able to reduce the rate of ASIC replacements on hybrids with defective ASICs and increase the number of working modules. The diagnostic analysis developed to study defective chips made use primarily of the flexibility built into the chip to adjust its front-end parameters, demonstrating the value to have such capability. It was very useful to also have access to the detailed database containing the results from the wafer screening.

Acknowledgments

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