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Publication Date

2018-06-01

Peer reviewed

Electrical Characterization of High Performance Fine Pitch Interconnects in Silicon-Interconnect Fabric

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***Abstract*— The Silicon-Interconnect Fabric (Si-IF) is a highly scalable platform for heterogenous integration of dielets using a fine interconnect pitch (≤ 10 µm) and small inter-dielet spacing (≤ 100 µm) [1]. In our fine-pitch integration scheme, short links on Si-IF (≤ 500 µm) are used for inter-dielet communication, reducing the latency (≤ 35 ps) and energy /bit (≤ 0.04 pJ/b) [2]. In this paper, we demonstrate the excellent transfer characteristics of the Si-IF links, verified experimentally. The measured insertion loss in these short Si-IF links (≤ 500 µm) is ≤ 2 dB for frequencies up to 30 GHz. Further, the transfer characteristics show only a single pole, demonstrating an RC-link behavior. We show that assemblies on Si-IF have 16-25X lower parasitic inductance, and 6-40X lower parasitic capacitance compared to assemblies on interposers and PCBs. We illustrate that using the Simple Universal Parallel intERface for chips (SuperCHIPS) protocol [2] for data transfer, data rates of ≥ 10 Gbps/link are realizable at an energy/bit of ≤ 0.04 pJ/b. Subsequently, due to the high interconnect density, the overall bandwidth/mm is ≥ 8 Tbps/mm. This corresponds to an improvement of 120-300X in bandwidth/mm and a reduction of 100-500X in energy/bit compared to a conventional PCB-based integration.**

Keywords- Silicon-Interconnect Fabric; Fine Pitch Interconnects; SuperCHIPS

I. INTRODUCTION

System integration technologies today predominantly use packaged dies soldered on a PCB substrate. The low interconnect densities (0.4 – 1 mm pitch) in these substrates limit the data-bandwidth in these systems. Therefore, to meet the bandwidth requirements, serialization and de-serialization (SerDes) circuits are used that are power hungry (up to 30% of chip power). Moreover, due to the high package-to-die area ratio (2 – 10X), the inter-dielet spacing and consequently, the communication link lengths are large (> 10 mm). Therefore, complex transceivers are needed for data transfer over such long links, reducing the power efficiency. High interconnect densities and fine spaced dielet assemblies are needed to reduce the communication power and latency. Recent technology developments like silicon interposers achieve moderate interconnect densities (> 50 µm pitch) [3-6]. However, they are finally connected to PCBs, adding an additional level in the packaging hierarchy. They are also limited in size and inflate the overall packaging cost [3,7].

We are developing a package-less, fine-pitch, heterogeneous integration platform, the Silicon-Interconnect Fabric (Si-IF), to realize high interconnect densities ($> 4x10^6$ cm^{-2}) [1]. In our fine-pitch integration scheme, unpackaged dielets are assembled on Si-IF at small inter-dielet spacings (≤ 100 µm) using fine pitch interconnects (10 µm). This integration scheme allows for a large number of parallel short communication links between dielets, eliminating the need for SerDes. These short links (≤ 500 µm) can be driven by a simple inverter-based driver using the Simple Universal Parallel intERface for chips (SuperCHIPS) protocol [2,3]. Consequently, this leads to significant improvements in data bandwidth (120-300X) and dramatic reductions in energy/bit (> 100X) compared to a conventional PCB based integration scheme, which is discussed in detail in [2]. The Si-IF based integration approaches System-on-Chip (SoC)-like performances and allows for a technology heterogeneity.

We demonstrated the 10 µm pitch interconnects (Au-capped Cu pillars, Ø = 5 µm) using a solderless direct metal-metal (Au-Au) Thermal Compression Bonding (TCB) in [1]. Correspondingly, we showed the 100 µm inter-dielet spacing and alignment accuracy of ≤ 1 µm in [1]. The Si-IF assembly with the integration of multiple dielets (4, 9, 16 & 25 mm^2) on a 100 mm diameter Si-wafer is illustrated in Fig. 1. A total of 371 dielets were TCB bonded to the Si-IF using the fine-pitch (10 µm) interconnects, at 100 µm inter-dielet spacing. The effective silicon area is > 3100 mm^2, demonstrating Si-IF as a scalable heterogeneous integration platform. The assembly was passivated using Parylene C.

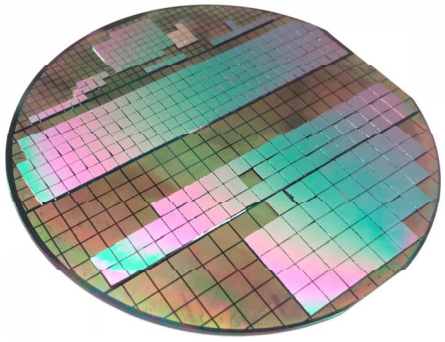

Figure 1. Fine-pitch integration of 371 dielets (4, 9, 16 & 25 mm^2) on a 100 mm diameter Si-IF using 10 µm pitch interconnects, at 100 µm inter-dielet spacing. The effective silicon area is greater than 3100 mm^2.

In this paper, we present the experimental characterization of the Si-IF links. We designed and fabricated the Si-IF and dielets with test structures for two-port S-parameter measurements, described in Section II. On-wafer RF measurements were performed to obtain the transfer characteristics of these links, discussed in Section III. Subsequently, the link parasitics were extracted from the measurements and compared with the simulated values. A

2377-5726/18/$31.00 ©2018 IEEE
DOI 10.1109/ECTC.2018.00197

comparative study of the overall parasitics in the Si-IF style integration with the PCB and interposer-based assemblies is also presented in Section III. Further, using the measured parasitics, a circuit-level simulation study was performed indicating that simple cascaded-inverter drivers are adequate for data transfer in Si-IF style integration (discussed in Section IV). Furthermore, the SuperCHIPS protocol for short-range low latency (≤ 35 ps), low energy (≤ 0.04 pJ/b), and high bandwidth (≥ 8Tbps/mm) is described, and the comparison of the performance benefits is discussed. Section V presents the conclusion.

II. Test Structures

We designed test structures to characterize the signal transfer between dielets when communicating using Si-IF. The dielets have metal pads that are connected to the Si-IF links using the fine pitch interconnects (10 µm). We designed daisy chain structures to represent signal flow between dielets when attached to Si-IF. In a real implementation, the links will be less than 500 µm, (typically 100 µm). However, measuring RF characteristics of short links is challenging due to the difficulty in probing and de-embedding of the probe-pad parasitics. Therefore, to get reliable measurements, three short links (585 µm) were cascaded in daisy chain fashion to form a long link between the two ports. Each link segment was terminated with Au-capped Cu pillars. The schematic of the cascaded structure and its cross-section are shown in Fig. 2. The characteristics of actual device under test (DUT), which is the short link segment, were later extracted using de-embedding techniques. The links were Ground-Signal-Ground (GSG) configured to achieve best results.

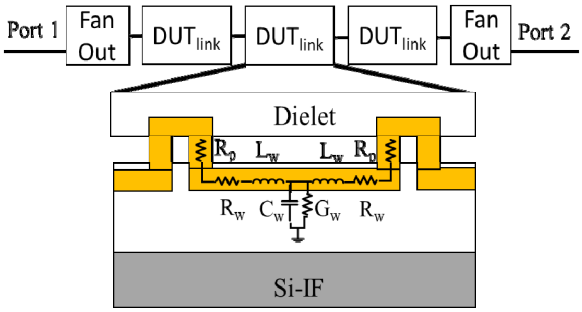

Figure 2. Schematic of three link segments (DUT) cascaded between the two ports and the cross-section of each link segment.

The test structures were fabricated using the process flow discussed in [1]. The fabricated Si-IF is shown in Fig. 3(a). Each link segment was 585 µm long; the width and height of the link were 2.1 µm and 1.3 µm respectively. The pitch of the links was 10 µm (same as the pillars). The diameter and height of the Cu pillars were both 5 µm. The pads on the dielet that complete the daisy chain were 17 µm long, 7 µm wide, 2 µm thick. The pads were 1 µm larger on each side to accommodate the alignment overlay tolerance.

De-embedding structures with fan-out wires shorted were designed to measure and de-embed the fan-out wire losses and the probe parasitics. The de-embedding structures are shown in Fig. 3(b). The dielets were precision aligned (≤ 1 µm) and assembled on the Si-IF using TCB [1], shown in Fig. 3(c). As mentioned earlier, the dielets were assembled to ensure the loss of the bonded interconnects are also included in the measurements. This would give us the actual link behavior when the dielets are in operation.

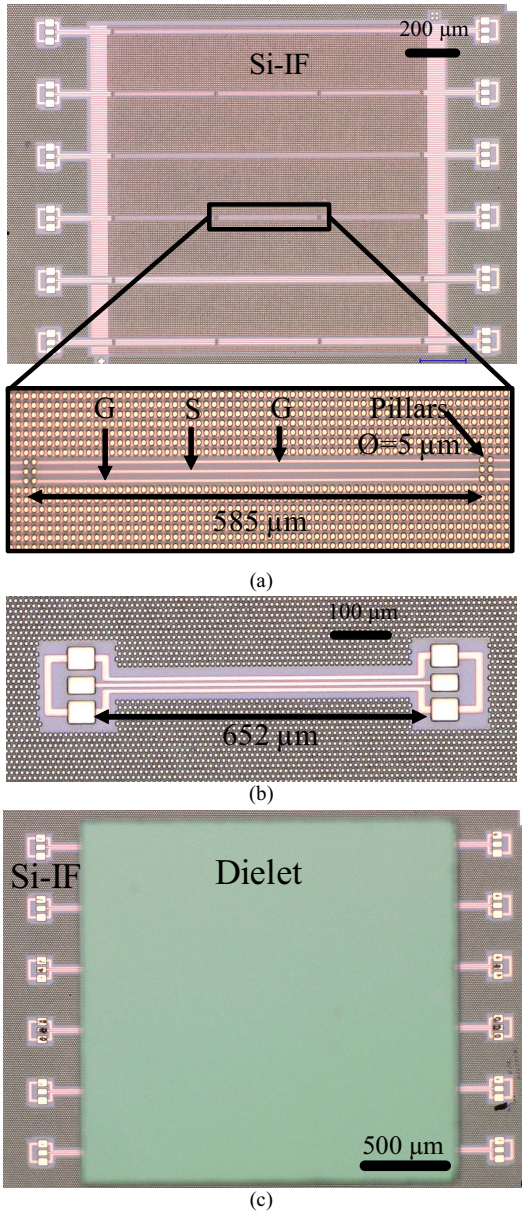

Figure 3. (a) Fabricated Si-IF test structure showing the 585 µm GSG configured link segments. The link segments are terminated with Au-capped Cu pillars (Ø = 5 µm, pitch = 10 µm) (b) Shorted fan-out wires structures used for de-embeddeding (c) Dielet precision aligned (≤ 1 µm) assembled on Si-IF using TCB to complete the daisy chain. This structure is used for the S-parameter measurements.

III. Results And Discussion

A. Insertion Loss Measurements

Two-port S-parameter measurements were performed on the bonded Si-IF structure in Fig. 3(c), using a 67 GHz Vector Network Analyzer (VNA). The S-parameters were measured for frequencies from 50 MHz to 30 GHz. To calibrate the GSG RF probes, the Line-Reflect-Reflect-Match (LRRM) standard was used. The key challenges in our measurements were (1) De-embedding the parasitics introduced by the probes and fan-out wires; (2) Extracting the characteristics of a single link segment from the cascaded structure. To overcome these problems, first, we measured the S-parameters of the de-embedding structures, and using the technique in [8,9], the probe and fan-out wire parasitics were de-embedded. Finally, using a similar technique, the S-parameters of each link segment is separated from the cascaded structure.

The measured insertion loss (S_{21}) of the 585 μm link segment after de-embedding is shown in Fig. 4. The insertion loss is observed to be less than 2 dB for frequencies up to 30 GHz for these short links. This loss includes losses in the Si-IF wires, the bonded interconnects (Cu pillars), and the pads on the dielets. The measured results were compared with the simulated values to show good agreement. The difference between the values can be attributed to the errors during measurement, calibration, and de-embedding. Additionally, the oscillation at 30 GHz is due to a resonance in the original measurement (cascaded structure, 2.5 mm long) that was not completely de-embedded. The insertion loss is significantly lower than existing interposer technologies [10-12].

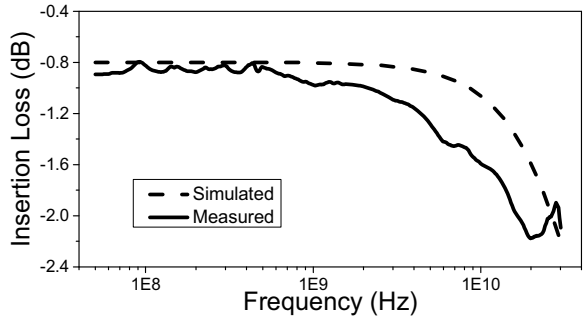

Figure 4. The measured and simulated insertion loss of a 585 μm link segment on Si-IF after de-embedding. Link dimensions: 2.1 x 1.3 μm^2.

It is observed that the transfer characteristics of these short Si-IF links has only a single pole. This establishes the RC-like behavior of short links on Si-IF (≤ 500 μm) compared to the RLC-like behavior of long links on interposer (> 3 mm) and PCB (> 10 mm). Further, this re-emphasizes that the inductance of Si-IF wires is not significant because the wirelengths are smaller than wavelength/10 (λ/10) of the propagating EM wave [2]. Therefore, there are no resonances and signal reflections. Consequently, complex transceivers with equalizers are not required for communication using Si-IF links because there is no inter-symbol interference. From the measured data, the insertion loss in a typical Si-IF link of 100 μm is estimated to be less than 0.8 dB. The RF characterization of shorter links (100 μm) is more challenging and is currently in progress.

B. Parasitics Extraction

The measured S-parameters were used to extract the parasitics in Si-IF links. An RLGC transmission line model of the link was used for the parasitics extraction. However, we established that the short Si-IF link segments cannot be modeled as transmission lines. Therefore, the S-parameters of the original cascaded structure, with de-embedded fan-out wiring were used for the parasitic extraction. The extracted parasitics are shown in Fig. 5, 6.

The extracted values include the parasitics of the interconnects and pads amortized across the length of the wires. The measured DC resistance of the links was 9.1 mΩ/μm. The resistance of the interconnects was extracted to be 75 mΩ per interconnect, which is comparable to the previous studies at larger pitch (20 μm) [13]. The resistance increases with frequency due to skin effect and proximity effect. Therefore, at high frequencies, the resistance of the link was 11.5 mΩ/μm and the resistance of interconnect was 130 mΩ. The variation in the extracted resistance is like the trend observed in [14].

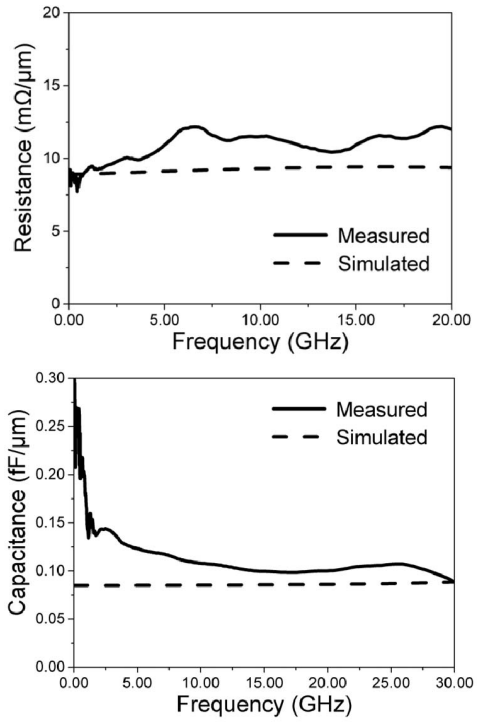

Figure 5. The extracted resistance and capacitance of the links from S-parameters (measured: solid, simulated: dashed) using RLGC line model.

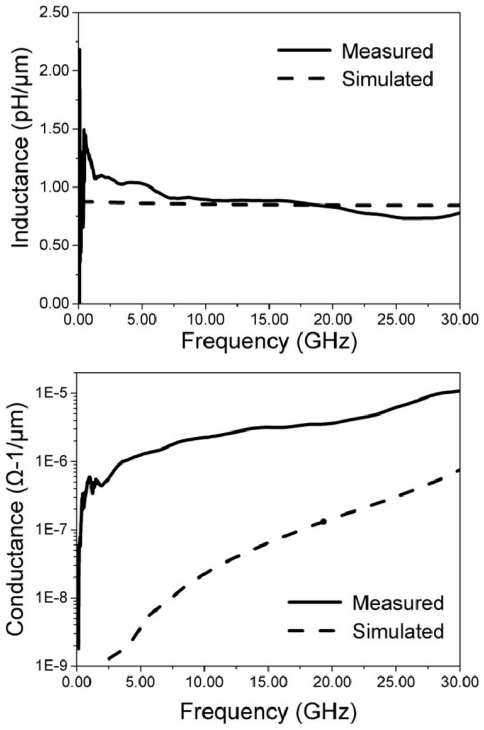

Figure 6. The extracted inductance and conductance of the links from S-parameters (measured: solid, simulated: dashed) using RLGC line model.

The measured capacitance is 0.10 fF/μm that includes the capacitance between fine-pitch (10 μm) pillars and the pad-capacitance due to the landing pad on the dielet. The measured inductance is 0.85 pH/μm. The decrease in inductance is consistent with the previous studies [13,14]. The measured inductance and capacitance are in reasonable agreement with the simulated models. Further robust experimental verification is under progress. We observe that the Si-IF trace parasitics are comparable to the on-chip global wiring parasitics in a 65-90 nm technology node [12]. This highlights the heterogeneous system integration efficiency using Si-IF that is close to a monolithic SoC.

C. Parasitics Comparison

A comparison of the total parasitics experienced by the signals in Si-IF, interposer, and PCB based assemblies is shown in Table. I. The values presented include the total parasitics of the traces, interconnects, and packages. The package parasitics are applicable only to PCB substrates. The major difference between interposer and Si-IF links is the length of the traces. Moreover, the capacitance due to Electro-Static-Discharge (ESD) protection is not included for Si-IF assemblies, which can add more than 0.1 pF of parasitic capacitance, because of the reasons mentioned in [2]. From the table, we notice that the Si-IF assemblies when compared to PCB have 25-35X lower parasitic inductance and 40-100X lower capacitance. Furthermore, the Si-IF assemblies when compared to interposer assemblies, have 6-9X lower parasitic inductance and 16-40X lower parasitic capacitance. The two major reasons for the impressive reduction of the parasitics in Si-IF assemblies are (1) package-less integration; (2) Short link lengths (≤ 500 μm) due to the small inter-dielet spacings (≤ 100 μm).

TABLE I. SI-IF VS INTERPOSER VS PCB PARASITICS COMPARISON

Technology	***Link length/ Wire pitch***	***Inductance (nH)*** *(Normalized to interposer)*	***Capacitance (pF)*** *(Normalized to interposer)*
Si-IF	100 μm/ 4 μm[a]	0.35 (0.11)	0.02 (0.02)
Si-IF	585 μm/ 10 μm[b]	0.52 (0.17)	0.06 (0.07)
Interposer	5 mm/ 6.4 μm [15]	3.125 (1)	0.855 (1)
PCB	20 mm/ 320 μm[c] [15]	~12 (3.84)	~2.0 (2.34)

a. Estimated from measured parasitics
b. Experimentally measured
c. Calculated

IV. CIRCUIT LEVEL ANALYSIS

A. Transceiver Circuit

As discussed earlier, the low insertion loss and RC-like behavior of the short links on Si-IF reduce the complexity of transmitters and receivers. Simple cascaded inverters can be used as transceivers for data transfer between dielets, which is just like a communication between different functional blocks in an SoC. To validate this theory, we performed circuit simulations with tapered buffer drivers designed in TSMC 16nm technology, shown in Fig. 7(a)-(b).

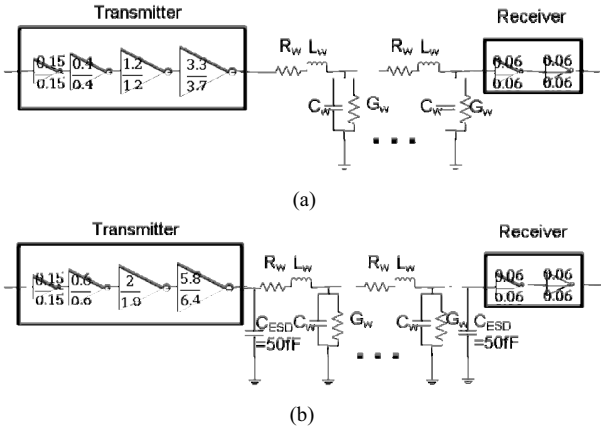

Figure 7. (a) Schematic of the transceiver circuit without ESD protection (b) Schematic of the transceiver circuit with ESD protection.

The extracted parasitics were used to create an RLGC equivalent circuit model of the Si-IF links. The wire width was assumed to be 2 μm while the wire pitch is 5 μm. This corresponds to a real situation, where the interconnects are in a staggered row configuration. The interconnect pitch

within a row is 10 µm while wiring pitch between wires of different rows is 5 µm. The wire-length was assumed to be 500 µm, which is the worst-case scenario. A load equivalent to fan-out 4 (FO4) was assumed at the end of the receiver. Two scenarios were evaluated, (1) with ESD; (2) without ESD protection, shown in Fig. 7(a), (b). The ESD protection adds significant load (50 fF per terminal) on the drivers, increasing the size of the driver and power by almost 2X. Due to the low contact area per interconnect and the minimal die handling in our assembly process, we predict that the ESD protection requirements to be much lower (< 50 fF) in our integration scheme [2], when compared to a PCB or interposer style integration.

In our simulations, a 10 Gbps pseudo random bit stream (PRBS) was presented as an input to the driver and the receiver output was analyzed. The rise and fall time were assumed to be 5% (10 ps) of the Unit Interval (UI). The input waveform, and the waveforms at the input and output of the receiver for the first scenario is shown in Fig. 8. The transmitted waveform across the link at the input of the receiver shows a full VDD swing (0.9 V) and < 20 ps rise/fall time. Consequently, the rise/fall time is < 5ps, at the output of the receiver. Therefore, these simulations show that simple inverters can be used to drive the links on Si-IF. The overall latencies from the input of the driver to the output of the receiver were 27.5 ps and 31.5 ps, for the scenarios with and without ESD protection respectively. Further, the average energy/bit for the PRBS data was 0.03 pJ/b and 0.06 pJ/b for the scenarios without and with ESD protection respectively.

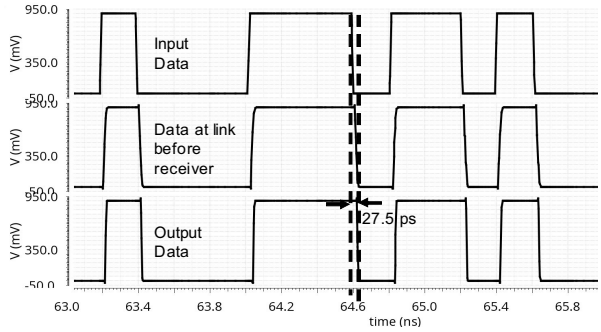

Figure 8. Simulated waveforms: 10 Gbps PRBS input; the transmitted data across the link before receiver; the receiver output..

B. *SuperCHIPS streaming protocol*

The Si-IF technology provides a large number of communication links due to the fine-pitch interconnects. This eliminates the need for SerDes, which are power hungry (23 pJ/b [16], 10 pJ/b [17]). As discussed in the previous section, simple transceivers can be used for data transfer and therefore, a simple communication protocol is needed to make efficient utilization of the Si-IF integration.

We propose the short-range (500 µm) SuperCHIPS protocol that makes effective utilization of the fine-pitch interconnects technology and achieves low energy (≤ 0.04 pJ/b), low latency (≤ 35 ps/ 1 clock cycle), and high bandwidth (8 Tbps/mm) communication between dielets. This protocol is particularly efficient for a streaming interface. In this protocol, all the peripheral links are configured as single ended signals to achieve maximum data-bandwidth. The data can be transferred either asynchronously or using a synchronous sourced clocking. The schematic of a typical I/O cell is shown in Fig. 9. In asynchronous mode, the data-rate per link can be as high as 10 Gbps as shown by the simulations, Fig. 8. For asynchronous transfer, latency is the most important parameter that is reduced with minimal ESD protection. In synchronous mode of transfer, the data-rate per link is up to 4 Gbps, because of the difficulty in clock generation and synchronization at higher frequencies.

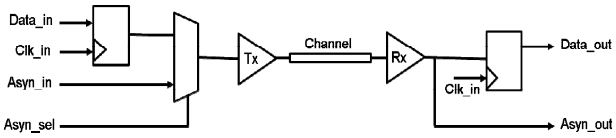

Figure 9. Schematic of the I/O cell in the short-range SuperCHIPS streaming protocol.

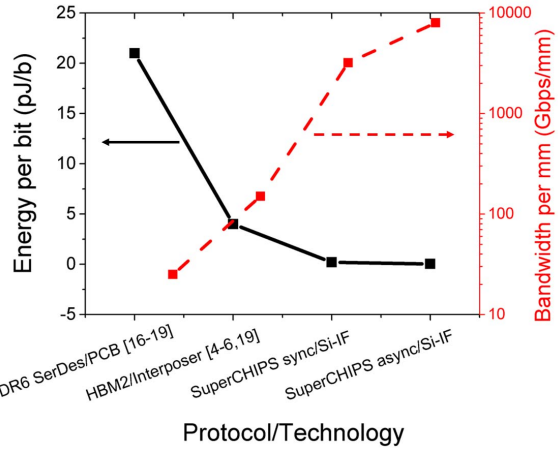

Figure 10. Comparison of energy/bit and bandwidth/mm among different protocol in PCB vs interposer vs Si-IF style integration.

The maximum data-bandwidth using the asynchronous mode is 2 Tbps/mm for a single wiring layer (4 µm wiring pitch). The Si-IF technology allows for 4 layers of wiring, therefore, increasing the bandwidth to 8 Tbps/mm. Furthermore, a reduction of wiring pitch to 2 µm increases the bandwidth by 2.5X. In synchronous mode of data transfer, the clock generation limits the bandwidth, which is 2.5X lower than the asynchronous mode. The energy/bit in asynchronous data transfer without ESD protection is ≤ 0.04 pJ/b. The energy/bit for synchronous data transfer is ≤ 0.2 pJ/b. Overall, the SuperCHIPS protocol corresponds to

a 120-300X improvement in data-bandwidth/mm and a 100-500X reduction in energy/bit, when compared to a PCB based integration scheme. Further, compared to interposer assemblies, the improvement in data-bandwidth/mm is 20-55X and the reduction in energy/bit is 20-100X. The comparison of bandwidth and energy among different technologies is shown in Fig. 10. The latency for the asynchronous transfer is ≤ 35 ps while the latency for synchronous transfer is 1 clock cycle.

V. Conclusion

We successfully demonstrated a package-less, fine-pitch, scalable heterogeneous integration platform, the Silicon-Interconnect Fabric. We show that the measured insertion loss of the short Si-IF links (≤ 500 µm) was ≤ 2 dB for frequencies up to 30 GHz. Further, we demonstrate RC-like behavior of these links, contrary to a transmission line (PCB links). We show that the links in Si-IF assemblies have 6-25X lower parasitic inductance and 16-40X lower parasitic capacitance compared to interposer and PCB-based assemblies. We present the SuperCHIPS protocol, where simple inverters are used for data transfer. Using circuit simulations of SuperCHIPS, we demonstrate that the energy/bit is ≤ 0.04 pJ/b and the latency is ≤ 35 ps. The data-bandwidth/mm is greater than 8 Tbps/mm. Therefore, the Si-IF platform exhibits high performance and exemplifies a superior substrate for heterogeneous integration of systems.

VI. Acknowledgement

The Defense Advanced Research Projects Agency (DARPA) through ONR grant N00014-16-1-263, the UC-MRPI, and the UCLA CHIPS Consortium supported this work. The views, opinions and/or findings expressed are those of the authors and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government. We thank Prof. Sudhakar Pamarti, Prof. Dejan Markovic, Dr. Boris Vaisband, Randall Irvin, Saptadeep Pal, Uneeb Rathore, and Sumeet Nagi for valuable discussions.

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