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Low-Inductance Asymmetrical Hybrid GaN HEMT Switching Cell Design for the FCML Converter in High Step-Down Applications

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Abstract—Proper utilization of GaN devices generally necessitates ultra-low inductance printed circuit board (PCB) layout in the main commutation loop or switching cell of a power converter. The flying capacitor multilevel (FCML) topology in particular contains many of these switching cells, thus design optimization becomes critical. A novel asymmetrical cell layout design with sub-1 nH commutation loop inductance is proposed and characterized for the FCML by utilizing a transient- and impedance-based measurement technique in conjunction with 3D field simulation. To validate its efficacy, this switching cell design is demonstrated within a prototype high performance step-down intermediate bus converter supply ($v_{out} = 48$ V) with wide input voltage range ($v_{in} = 48$ to 340 V).

I. INTRODUCTION

Hybrid switched capacitor topologies in general can achieve excellent simultaneous reduction in loss and volume by redistributing the energy processing requirements of bulky inductors to more energy dense capacitors and active switch components [1]. In particular, the flying capacitor multilevel (FCML) topology excels for regulated applications and remains competitive for wide input range conversion ratios as demonstrated by the high-performance prototypes in [2]–[5]. However, with multilevel topologies comes a greater quantity of active switching components, so maximizing switching speed and minimizing switching loss becomes critical. This work investigates the application of a standard low-inductance hybrid switching cell layout [6]–[8] to the FCML buck converter shown in Fig. 1 while simultaneously improving efficiency with the use of paralleled low-side FETs as shown in Fig. 2a. The remainder of the paper is organized as follows: Section II presents innovations in the switching cell layout highlighting the asymmetry in the complimentary switch pairs and the ultra-low commutation loop inductance; and Section III demonstrates experimental validation — both the commutation loop and the overall converter — with a high-performance multi-purpose hardware prototype. Finally, Section IV concludes the work.

II. SWITCHING CELL LAYOUT

The FCML switching cell is distinct from a typical half-bridge as the high-side (HS) source and low-side (LS) drain of complimentary FETs are not equipotential. There are instead two flying capacitors adjacent to the FETs as indicated in

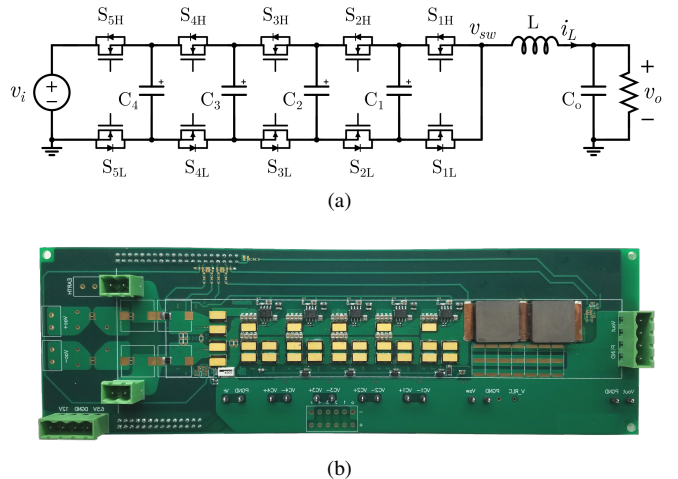


Fig. 1. 6-level FCML buck converter. (a) Full functional schematic. (b) Hardware prototype photograph (front-side).

Fig. 2a which altogether define the commutation loop of a single switching cell. The cascaded modularity of the FCML implies any inefficiency in the cell compounds with the number of levels. Thus, to markedly improve overall system performance for a large voltage step-down application, the core cell layout as illustrated in Fig. 2b is designed to be asymmetrical with low commutation loop inductance to optimize conduction losses and improve switching speed, respectively.

The utilization of GaN — instead of Si — devices enables improved converter performance considering system trade-offs in switching frequency, losses, and volume. GaN HEMTs have an inverse transconductance versus temperature relation which benefits current sharing when paralleling discrete components [9]. In addition, the GS61008T (GaN Systems) top-side-cooled GaN HEMT contains two symmetric interchangeable gate pins on either side of the package which specifically aids layout parallelization and allows for equivalent parasitic gate-loop inductance between all FETs [10]. GaN FETs also have high dv/dt transitions thus layouts with low parasitic inductances, especially when paralleling FETs, better enable full utilization of the devices. With sub-optimal layout, high gate resistance becomes necessary to dampen overshoot in V_{ds} during turn-on to prevent fatal over-voltages; this in turn increases switch overlap losses.

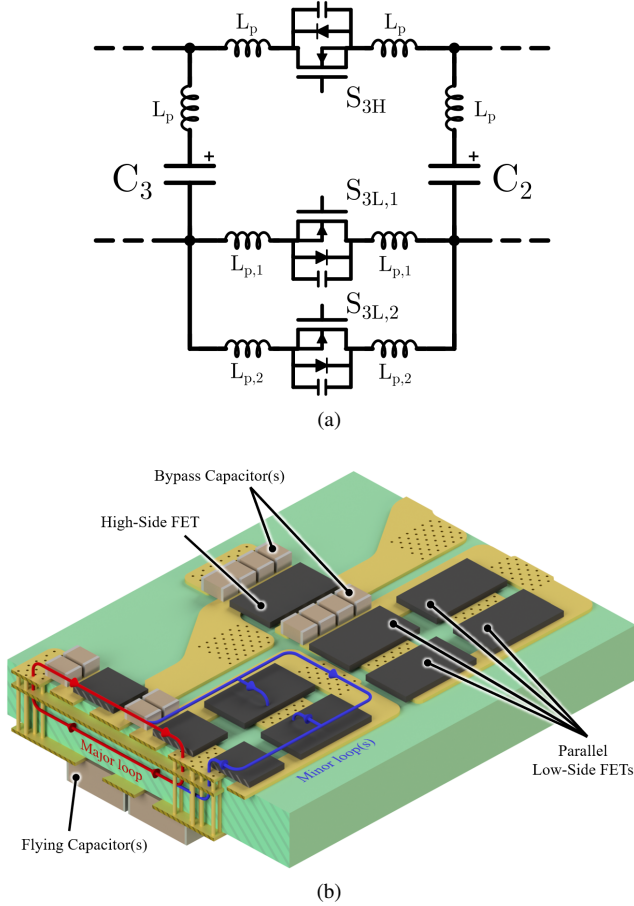


Fig. 2. Asymmetrical switching cell definition, implementation, and characterization. (a) Exemplar asymmetrical switching cell with inductive parasitics. (b) Rendered switching cell with delineations for major and minor commutation paths (exaggerated PCB layer thicknesses).

Many layout aspects are critically dependent on application voltage creepage and clearance requirements. Other FCML switching cell designs in [3], [11] implement various *vertical* layouts necessary at 1000 V and/or for high altitude applications whereas the *hybrid* layout proposed in this work meets a 400 V compatibility requirement in less stringent environmental conditions.

A. Asymmetrical Switching Cell

An asymmetrical switching cell — broadly defined by unequal on-state resistances between the HS and LS switches — aids in minimizing the overall conduction losses. In the case of a buck converter, as the voltage conversion ratio increases and the duty ratio D decreases, the rms current in the LS switches becomes much larger than the rms current in the HS switches, i.e., $I_{LS} = \sqrt{1-D} \cdot I_L$ and $I_{HS} = \sqrt{D} \cdot I_L$. Consequently, ohmic conduction losses in the LS switches quickly dominate and thermally limit the converter as the load increases. So for each cell, LS switches should optimally have equal losses to the HS switches. To best achieve this, the LS on-state resistance $R_{ds,LS}$ should be smaller than the HS $R_{ds,HS}$ to offset the relative difference in rms current. For a specified input/output conversion ratio $M = 1/D$, the

conduction losses in each cell can be equated as

$$P_{cond,HS} = I_{HS}^2 R_{ds,HS} = I_{LS}^2 R_{ds,LS} = P_{cond,LS} \quad (1)$$

to derive an ideal LS to HS on-state resistance ratio K as

$$K = \frac{R_{ds,LS}}{R_{ds,HS}} = \frac{D}{1-D}. \quad (2)$$

To achieve switching cell asymmetry, the desired K is achieved either using a single device for each side with different intrinsic $R_{ds,on}$ [12] or with discrete parallel devices. This design implements the latter with one HS FET and K paralleled LS FETs utilizing a single discrete device type. EPC manufactures a series of monolithic integrated GaN half-bridge cells, and various options are LS/HS asymmetric ($K = 4$) meant for high conversion ratio applications [12], [13].

The primary drawback to parallelization is increased switching overlap losses associated with the greater number of switches. For K parallel switches, each switch sees the full rated voltage and only $1/K$ of the rated current. However, the source and sink currents of the gate driving circuit must charge and discharge a larger effective input capacitance $C_{iss,K} = K \cdot C_{iss}$ and output capacitance $C_{oss,K} = K \cdot C_{oss}$ resulting in slower overall switching transitions. Thus determination of total losses when paralleling FETs is a multi-faceted optimization dependent on the gate driving layout and circuitry. With proper cell design, an asymmetric cell can achieve only marginally worse switching losses compared to a non-paralleled design, especially when conduction losses dominate within the overall converter as in the aforementioned high power, wide-conversion-ratio application.

Despite a larger cell area due to parallelization, small cell volume is obtained by fully utilizing the available surface area on the back-side to minimize overall converter height. For this layout, there is ample room on the back-side of the printed circuit board (PCB) to incorporate a sufficient amount of flying capacitance necessary for FCML operation. Although this bulk flying capacitance is too electrically distant to achieve fast switching commutation (i.e., large commutation loop) by itself, small bypass capacitors can be used locally to alleviate potential impairments in switching performance.

Compared to a conventional 2-level power converter, hybridized switch-capacitor topologies — by their very nature — tend to be ultra-low profile with distributed lower-voltage switches and lower inductance requirements. To maintain consistency in the converter height throughout, the primary buck inductor tends to also be low-profile. For this design a standard 1.6 mm PCB thickness makes up almost a quarter of the overall converter height, and thus an inset inductor becomes a reasonable consideration to maximize the fill factor of the hardware. The inductor with lateral fins is inspired by an existing series of "winged" IHLW™ inductors manufactured by Vishay; however, no commercially available options were rated for large enough saturation currents to fulfill the design needs of this work and a custom assembly utilizing

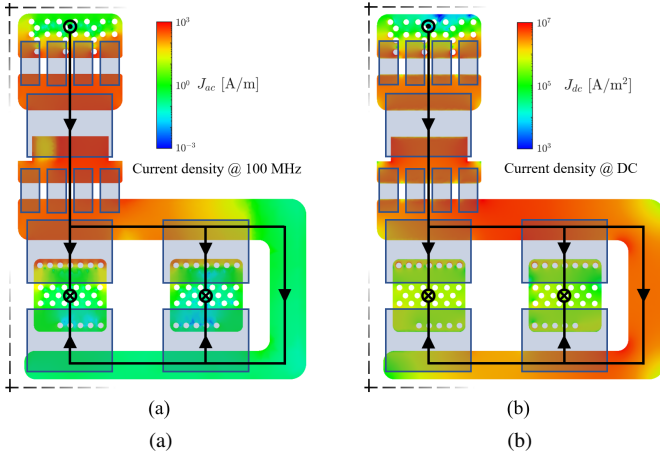


Fig. 3. Switching cell simulation (Q3D ANSYS) of front-side layer with excitation current $I_e = 1$ A. (a) Illustration of surface current density distribution at a commutation frequency of $f = 100$ MHz readily indicates the major and minor commutation paths. (b) Surface current density distribution at dc demonstrating proper current distribution between parallel FETs.

TABLE I
MEASUREMENT AND SIMULATION RESULTS OF
COMMUTATION LOOP INDUCTANCE L_c @ 100 MHz

FET(-)	A	AB	ABC	ABCD
Q3D sim.	0.40 nH	0.38 nH	0.38 nH	0.38 nH
Impedance meas. ¹	1.00 nH	0.93 nH	0.93 nH	0.94 nH
Transient meas. ²	1.09 nH	0.94 nH	—	—

¹ Measurement error in L_c is approximately ± 50 pH at 1 nH.

² Measurement error in L_c is approximately ± 100 pH at 1 nH.

commercial products¹ was constructed.

B. Commutation Loop Inductance

Reducing the commutation loop inductance diminishes voltage overshoot during switch transitions and can indirectly decrease switching losses, through purposeful reduction of deadtime and gate resistance; this is especially pertinent in a design with paralleled FETs. Overall, minimization of the various parasitic inductances in the switching cell layout were prioritized accordingly: (i) the common-source inductance in the paralleled LS FETs, (ii) the commutation loop inductance formed by the complimentary switch pair, and (iii) the gate loop inductance(s). These judgements are ultimately underscored by minimum voltage clearance requirements. A different prioritization of parasitics would result in a differently designed layout.

The *hybrid* switching cell as defined in [3], [6], [12], [14], [15] remains a competitive layout choice since all pertinent components are on the front-side of the PCB and the commutation loop path forms a low impedance path between the first (front-side) and second copper layers as denoted in Fig 2b. For low-profile GaN HEMT devices, the commutation loop trace width can be as wide as the component itself. In this 4-layer PCB design, the first copper layer is $70 \mu\text{m}$ (2 oz.), the

inner prepreg layer is $110 \mu\text{m}$, and the second copper layer is $35 \mu\text{m}$ (1 oz.) which forms a relatively small loop area. Maximization of trace width and minimization of loop area are first-order optimizations which reduce the overall commutation loop inductance L_c .

The proposed cell design uses only through vias which minimizes manufacturing complexity and cost; a more complex design with blind and buried vias could potentially utilize both the front and back-sides of the board to increase cell density without significant clearance concerns. An example of this extension to the hybrid cell layout design is presented in [6].

Two primary layout innovations — the asymmetrical switching cell and low commutation loop inductance — have been thus far discussed as mostly mutually exclusive design considerations. Typically in symmetric switching cell designs, the HS and LS FET(s) are evenly distributed to the greatest extent possible which equalizes the parasitic gate and commutation loop inductances of paralleled FETs [9], [16]–[18]. For the choice of GS61008T GaN FETs in a 6-level FCML at peak input voltage $v_{in} = 340$ V, the system design fully utilizes (with adequate margin) the device’s voltage rating limit ($V_{ds,nom} = 68$ V versus $V_{ds,max} = 100$ V), however it notably underutilizes the device’s continuous current rating limit ($I_{ds,nom} = 17$ A versus $I_{ds,max,cont} = 65$ A at $T_c = 100$ °C). The underutilized current capacity presents an opportunity — because of the asymmetric quantity of HS versus LS FETs — to also make the commutation path relative to each paralleled FET asymmetric (i.e., $L_{p,1} \neq L_{p,2}$ in Fig. 2a). Assuming symmetrical common-source inductance, gate inductance, and gate resistance, the closest LS FET $S_{L,A}$ which forms a *major* commutation loop with the HS FET S_H (see Fig. 2b) turns on slightly before the other LS FETs $S_{L,B-D}$ which form *minor* commutation loop paths. Thus for a short period, most current $I_{ds,nom}$ flows through $S_{L,A}$ until $S_{L,B-D}$ turn on and redistribute it equally.

III. EXPERIMENTAL VALIDATION

Utilizing preceding developments, a multi-purpose PCB hardware prototype capable of dc-dc and ac-dc operation as shown in Fig. 1b is designed to validate the switching cell efficacy. The converter is functionally a step-down intermediate bus converter supply ($v_{out} = 48$ V) with wide input voltage range ($v_{in} = 48$ to 340 V) and an output current rating of 14 A (or 650 W). The necessity of an asymmetrical switching cell structure is especially attractive for a high voltage step-down (or step-up) application, and a near-median input voltage of 240 V corresponds to a 5-to-1 conversion ratio where the conduction loss in the single HS and four paralleled LS FETs are ideally equivalent according to (2). The gate drive design is a cascaded bootstrap structure as outlined in [19] using one Silicon Labs Si8271 isolated gate driver to drive each side of each switching cell.

¹ $L = 2 \times 3.3 \mu\text{H}$, 28 A, Vishay IHLP6767GZER3R3M01

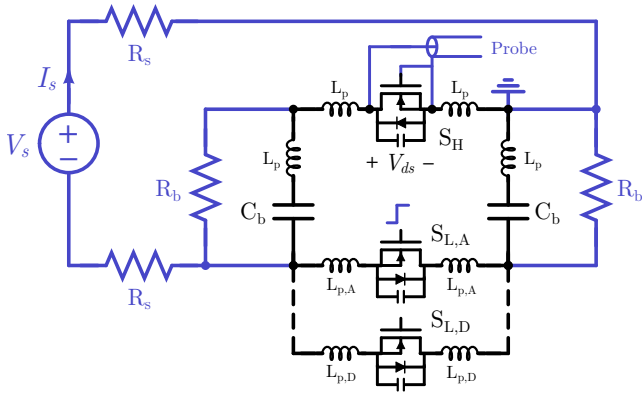


Fig. 4. Transient-based measurement test circuit schematic. $R_s = 100 \Omega$, $R_b = 100 \text{ k}\Omega$.

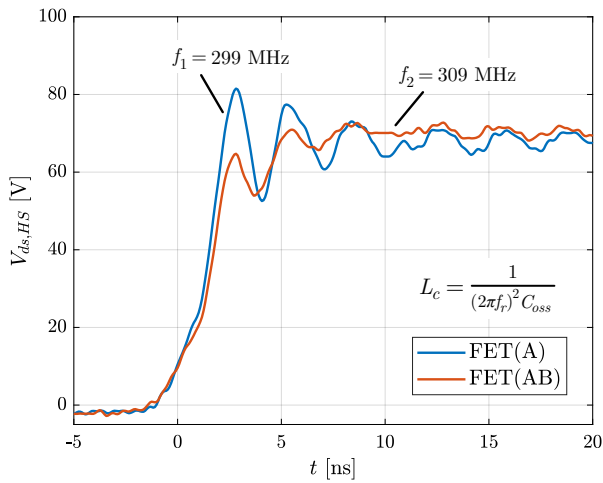


Fig. 5. Measured high-side $V_{ds,HS}$ during LS turn-on for varied configurations of paralleled low-side FETs. Input voltage $V_s = 70 \text{ V}$, sink current $I_s = 2 \text{ mA}$, and per-FET turn-on gate resistance $R_{g,on} = 4 \Omega$.

A. Switching Cell Evaluation

The overall commutation loop inductance L_c serves as a reductive but fair metric for quantifying switching cell performance as it is geometrically rather than operationally dependent. However, target inductances below 1 nH are especially difficult to measure with reasonable accuracy and so several simulation tools and experimental testbeds have been utilized for validation in this work. Different circuit configurations are enumerated simply as a combination of LS FETs A, B, C, and D as designated in Fig. 6. For instance, configuration “FET(AB)” denotes the device-under-test (DUT) which contains both LS FET A and FET B, while “FET(B)” denotes the DUT containing only LS FET B.

1) *3D field simulation*: Simulation using ANSYS Q3D, a 3D electromagnetic field solver, extracts values of L_c from the physical PCB geometry and these values are reported for different parallel quantities in Table I. Figures 3a and 3b are illustrations of current density at 100 MHz and dc frequencies, respectively, in the front-side copper plane. Current

distribution at $f = 100 \text{ MHz}$ illustrates a major (dominant) commutation path and weaker minor commutation paths, while at dc all current is shared equally amongst the paralleled LS FETs as expected.

2) *Transient-based measurement*: The pulse-based measurement captures a transient step-response in the HS V_{ds} of the switching cell for a LS turn-on transition. The FCML switching cell can be considered a more complex variation of the typical half-bridge cell except with an additional bypass capacitor between the HS drain and LS source. Consequently, a double-pulse test circuit [20] typically used for the latter is incompatible with the former. A specialized test circuit introduced in [3] and reproduced in Fig. 4, generates a ground-referenced voltage transient across a FET for a near-zero current I_{ds} . This voltage transient is then captured with a high-bandwidth oscilloscope utilizing a low-inductance probe². In principle, the dc voltage V_s is set to the desired steady-state value of V_{ds} ; the source resistors R_s ensure the auxiliary circuit path is higher impedance than the sensitive commutation loop; and the bypass resistors R_b dissipate energy in the bypass capacitors after the initial transient of the step response. Although not truly representative of the switching dynamics of the full system since $I_{ds} \approx 0$ and gate resistance $R_g = 4 \Omega$, the transient measurement does provide some intuition regarding the switching rise time and relative voltage overshoot at nominal operating conditions.

Figure 5 depicts measured HS drain-source voltage $V_{ds,HS}$ after LS FET turn-on for different configurations of paralleled LS FETs. The frequency of the observed resonance in $V_{ds,HS}$ yields a relationship for extracting L_c indirectly by utilizing the HS FET parasitic output capacitance $C_{oss,HS}$ (derated for operating voltage) if approximated as a second-order LC circuit as

$$L_c \approx \frac{1}{(2\pi f_r)^2 C_{oss}} \quad (3)$$

assuming minimal damping and a linear C_{oss} throughout the damped oscillation. If the waveform oscillations are heavily distorted, then an FFT can estimate the fundamental frequency component of resonance. Observed waveform distortion arises from changes in the transient impedance associated with dynamic $R_{ds,on}$ [21] as well as possible non-linearities in the capacitor ESR during large voltage swings [22], [23]. Evaluated results of (3) yield $L_c = 0.93 \text{ nH}$ including all paralleled FETs as shown in Table I. Measurements are highly repeatable, however uncertainty in resonant frequency and C_{oss} (taken from datasheet) reduce inductance estimation accuracy to within $\pm 100 \text{ pH}$ using this transient-based method at 1 nH.

3) *Impedance-based measurement*: With proper calibration and configuration, the impedance analyzer³ testbed provides relatively accurate measurements of impedance (magnitude

²Keysight MSOX4154A (1.5 GHz, 5 GSa/s) oscilloscope with N2894A (700 MHz) passive probe.

³Keysight E4990A impedance analyzer with 42941A impedance probe.

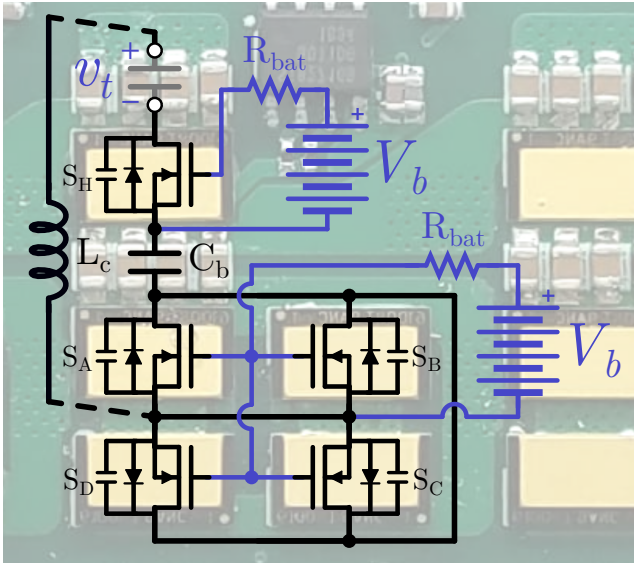


Fig. 6. Impedance-based measurement testbench and overlaid circuit schematic of the switching cell commutation loop across v_t . Batteries ($V_b = 6$ V, $R_{bat} = 1$ k Ω) keep the GaN FETs in the on-state.

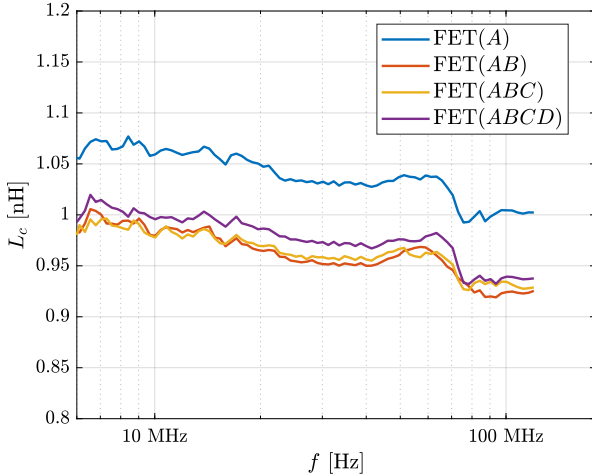


Fig. 7. Measured commutation loop inductance across frequency, $L_c(f)$, processed from direct impedance measurement of the DUT using an impedance analyzer. Results are shown for increasingly paralleled quantities of LS FETs.

and phase) across frequency. Measured data can be used to directly compute loop inductance as

$$L_c \approx \frac{1}{\omega} \cdot \left(X_{meas} + \frac{1}{\omega C_b} \right) \quad (4)$$

by assuming an equivalent series RLC circuit model, where the series (bypass) capacitance is a known quantity set by discrete components⁴ and X_{meas} is the measured reactance of the loop. For these measurements, the DUT is a single switching cell configured similarly to the actual hardware during normal power conversion operation. This includes the HS GaN FET, some combination of the paralleled LS GaN FETs, and one

⁴ $C_b = 4 \times 47$ nF, 450 V, TDK C2012X7T2W473K125AA

set of bypass capacitors as shown in Fig. 6. To maximize capacitance per unit volume, the bypass capacitor(s) in this DUT is a Class II dielectric and thus de-rates with applied voltage. The value of C_b used in (5) closely matches the manufacturer’s zero-voltage-bias specifications, however it can be refined by examining X_{meas} at low frequencies where the impedance of C_b dominates as

$$X_{meas} \approx X_{C_b} = -\frac{1}{\omega C_b}. \quad (5)$$

All the GaN FETs are held in an ohmic “on” state by utilizing two batteries which provide a stable, isolated, and noiseless $V_b = 6$ V dc voltage across each of the gate-source terminals, V_{gs} , for the HS and LS as shown in Fig. 6. Much of the loop area is defined by the GaN FETs, thus a testbench incorporating the FETs in an on-state captures the essential interactions of package inductance with the PCB traces including the solder joint to the pad, internal wire bonding to the die, and the die itself. These FETs must be in the on-state otherwise the impedance of C_{oss} irrevocably dominates the measurement and extraction of L_c becomes impractical.

Results for the inductance of the commutation loop across frequency, L_c , are shown in Fig. 7 for different circuit configurations. This data demonstrates that after the addition of the first minor loop path (FET B) to the major loop (FET A), additional paralleled LS FETs (FET C and D) negligibly reduce L_c . Evaluated results of (5) yield $L_c = 0.94$ nH @ $f = 100$ MHz including all paralleled FETs as shown in Table I. Repeated measurements indicate accurate inductance measurement to within ± 50 pH using this method, however accuracy degrades quickly for values below 1 nH and approaches the minimum resolution of the utilized impedance analyzer.

4) *Summary of experimental results:* Based on the results in Table I, the commutation loop inductance for the full system is approximately $L_c \approx 1.0$ nH especially considering the implicit reduction from the additional large but non-negligible minor commutation paths afforded by each parallel FET. For variations in experimental and simulation testbeds, the actual DUT differs slightly: the transient and impedance tests include all FETs and bypass capacitors while the Q3D simulation includes no real components but merely homogeneous rectangular segments. Inspection of Table I indicates increasing L_c for testbeds with additional physical components. This trend is expected, especially when considering device parasitics and consequential package height compared to an ideal copper short that is flush with the PCB surface. There is also good agreement between measurements taken utilizing the transient-based and impedance-based experimental methods.

B. Dc-dc Efficiency Evaluation

Although a multi-purpose prototype, the converter remains a highly volume-optimized design effective across a wide range of voltage conversion ratios with an enclosed box volume of 45 cm³ (2.7 in³) at a rated power throughput of 650 W resulting in an 14 W/cm³ (240 W/in³) volumetric power density.

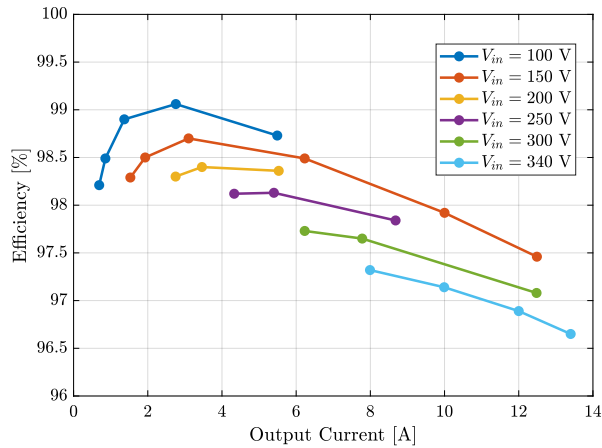


Fig. 8. Measured dc-dc efficiency measurements across various input voltages and resistive loads for the 6-level FCML buck converter with asymmetrical switching cell design. Switching frequency $f_s = 100$ kHz and output voltage $V_o = 48$ V.

The input/output efficiency for dc-dc operating conditions are recorded in Fig. 8 for a fixed output voltage across a range of input voltages and resistive loads. The present full-load efficiency at $P_o = 650$ W for a 7-to-1 conversion ratio is $\eta = 96.6$ %. Additionally, the efficiency results presented in Fig. 8 are thermally limited at $P_o = 650$ W with forced air cooling (400 LFM) and no heatsink.

IV. CONCLUSION

The proposed asymmetrical hybrid PCB layout design for the switching cell of flying capacitor multilevel (FCML) converter jointly utilizes the fast switching transitions of GaN semiconductors while minimizing conduction losses in high step-down dc-dc applications. Paired with the inherent benefits of a multilevel topology — lower voltage rated switches and smaller overall passive component volume — marked improvement of the layout, quantified by experimentally validated sub-1 nH commutation loop inductance, results in a simultaneously high step-down, high power density, high efficiency power converter.

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