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Los Angeles

**A 2-bit 1Gsps ADC Array with 32:1 Serializer in 45nm CMOS
SOI Technology**

A thesis submitted in partial satisfaction of the
requirements for the degree Master of Science
in Electrical Engineering

by

Geng Tian

2012

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ABSTRACT OF THE THESIS

A 2-bit 1Gsps ADC Array with 32:1 Serializer in 45nm CMOS SOI Technology

by

Geng Tian

Master of Science in Electrical Engineering

University of California, Los Angeles, 2012

Professor Mau-Chung Frank Chang, Chair

In this thesis, a SoC (system on chip) solution is proposed for the IF (intermediate frequency) band signal processing and transmission of a radiometer system. This highly integrated and low-power solution is designed for systems where low ADC resolution (< 2-bit) is needed but high-speed data transmission (> 10Gbps) and low-power operation (< 10mW/channel) is strongly desired.

The presented solution includes an array of 2-bit ADCs with duty cycle controlled AGC (automatic gain control) function and a low-power 32:1 serializer. AGC function is

included in the front end in order to cope with the wide range of input power (-10dBm ~ -20dBm). The AGC loop is controlled by digitized output duty cycle with an error of 2%. A current steering 5-level tree architecture serializer is designed to achieve a high serializing factor and low-power operation.

The circuit is designed using a 45nm SOI CMOS technology. It is capable of digitizing the IF signals using a power of 5.4mW/channel and transmitting the signals at 32Gbps. The serializer has an output reflection (S_{22}) of less than -10dB from DC to 32GHz with 400mV differential output swing. The serializer consumes less than 50mW of power (3.2mW/channel), and the AGC loop consumes 2.2mW/channel.

The thesis of Geng Tian is approved.

Yuanxun Ethan Wang

Dejan Markovic

Mau-Chung Frank Chang, Committee Chair

University of California, Los Angeles

2012

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I started working on this project at the end of the first academic year of graduate school in UCLA. Not only have I learned much while working on my thesis, but I will also be able to apply this knowledge to any future work in my career in the field of electrical engineering.

Finally, I would like to thank my family and friends for their continuing support through my graduate school studies.

CHAPTER 1

Introduction

1.1 Research Motivation

1.1.1 GeoSTAR System Introduction

A microwave radiometer is a system that detects electromagnetic energy which is noise-like in nature. The spatial as well as spectral characteristics of observed energy sources determine the performance requirements imposed on such a system [1].

Geostationary atmospheric remote sensing by microwave and millimeter-wave radiometers is a feature that has been long sought after. The Geostationary Synthetic Thinned Array Radiometer (GeoSTAR) was proposed in 2004 [2]. It synthesizes a large aperture to provide high spatial resolution from GEO (Geostationary Earth Orbit) without requiring a massive scanning antenna of a real-aperture system.

As illustrated in Figure 1, GeoSTAR consists of a Y-array of horn antennas and receivers, and a digital system which computes cross-correlation between the IF signals of the receivers. GeoSTAR is a system that provides high spatial resolution Earth orbit in discrete microwave bands from 50 to 180GHz. As shown in the system block diagram in Figure 2, in the IF band, the system proposed in 2004 requires 16 1-bit digitizers at 200Msps with a serializer. However, in the latest system digitizers with 2-bit resolution at 1Gsps are

strongly desired. Since the GeoSTAR system will contain more than 1000 units of receivers, the power consumption becomes the number one design parameter.

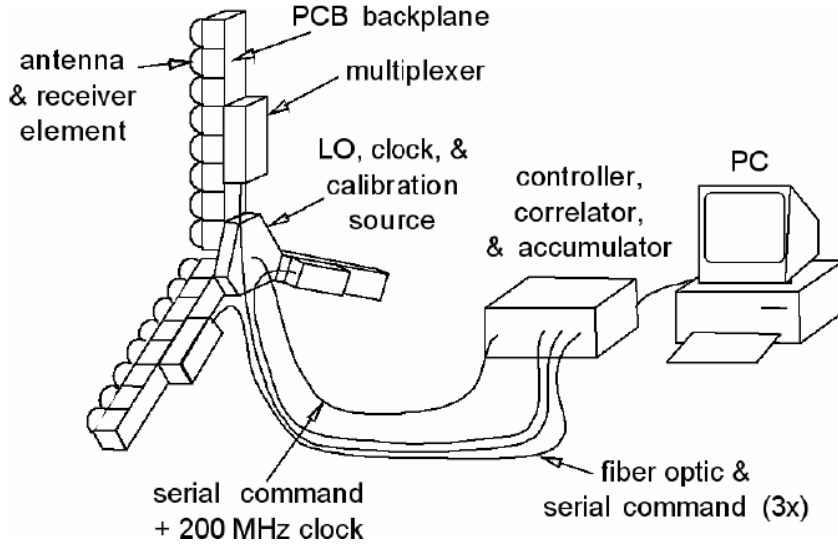


Figure 1 GeoSTAR configuration proposed in 2004 [2]

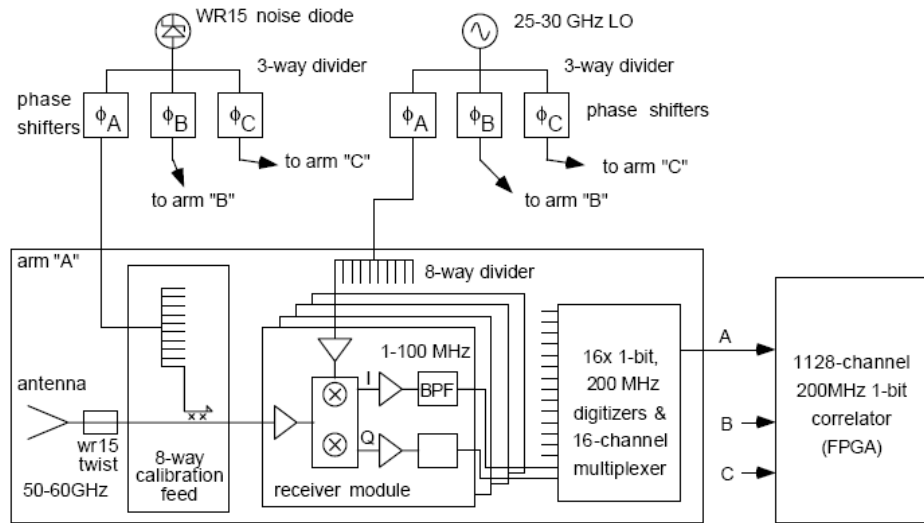


Figure 2 GeoSTAR system block diagram proposed in 2004 [2]

1.1.2 Motivation

For applications like GeoSTAR and other radio astronomy systems, often thousands of ADCs (analog-to-digital convertor) with at least 2-bit resolution are needed. These ADCs usually require AGC functions to achieve better results for digital correlation purposes. Power consumption, control precision and weight are of great concern for such systems. Existing designs cannot achieve all the above aspects with low cost [1, 2]. The current GeoSTAR system uses off-the-shelf 8-bit ADCs with no AGC function. With the increasing resolution and bandwidth of the digitized signals, an effective data link between the digitizers and the correlator needs to be designed. The main motivation behind this thesis is to propose a highly integrated, low-power solution for GeoSTAR baseband signal processing and transmission.

1.1 Organization of Thesis

In Chapter 2, the design challenge of this work will be presented. A review of the digitized correlation theory will be given. Then the design challenge for the AGC loop and the serializer will be presented separately.

In Chapter 3, the proposed approach will be presented. An overview of the technology will be given first. Then the top-level proposed system will be described. A novel duty cycle control function will be introduced, and finally other potential applications will be mentioned.

In Chapter 4, the design and simulation of IF band AGC loop will be presented. Each sub-section will go over the design and simulation of each circuit component. Section 4.1

presents the design and simulation of the VGA; section 4.2 presents the design and simulation of the 2-bit ADC; section 4.3 presents the design and simulation of the duty cycle control block; section 4.4 presents the design and simulation of the charge pump; and finally section 4.5 evaluates the performance of the designed AGC.

In Chapter 5, the design and simulation of the 32:1 serializer will be presented.

Finally in Chapter 6, a conclusion and performance comparison with other existing designs will be made.

CHAPTER 2

Research Challenge

2.1 AGC Loop Design Challenge

In modern radiometer systems, such as GeoSTAR, digitized cross-correlation is used to differentiate the power levels between two positions on the sky. Given the fact that the power of the incoming signal often varies over a wide range, AGC functions are strongly desired to maintain a small error between the digitized correlation and the ideal analog correlation. This section will first review the theory behind digitized correlation, and then present the challenge of AGC loop design.

2.1.1 Digitized Correlation Theory Review

It has been shown that a 2-bit (3-level) digitizer achieves the best tradeoff between the correlation accuracy and computation complexity [3]. Considering the computation complexity increases exponentially with the number of levels, modern radiometer systems use, at most, 3-level digitizers. It has also been demonstrated that the optimal threshold values for the 3-level digitizer are $[-0.9\sigma, 0, +0.9\sigma]$, where σ is the standard deviation of the IF signal. The relationship between RMSE and $V_{\text{ADC}}/\sigma_{x,y}$ is shown in Figure 3 where,

RMSE = the root mean square error of the digitized correlation comparing to the ideal analog correlation;

$V_{ADC}/\sigma_{x,y}$ = normalized ADC reference range with respect to the input standard deviation.

Different curves correspond to different quantization levels. For example, the pink curve shows the characteristics of a 3-level digitizer; the black curve shows the characteristics of a 31-level digitizer.

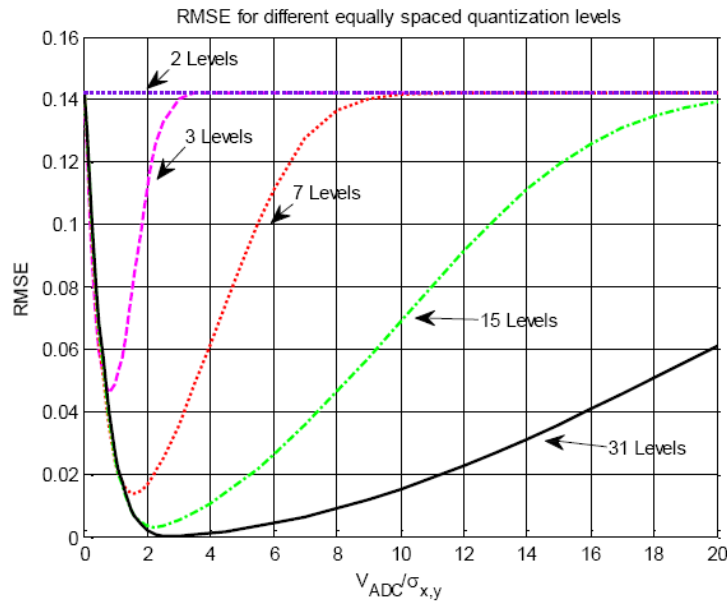


Figure 3 Root mean square error vs. ADC reference range (normalized) relationship for different equally spaced quantification levels [4]

This relationship clearly showed the advantage of using a 3-level digitizer, where the minimum RMSE can be achieved when the threshold is around 0.9σ . A 3-level digitizer can greatly reduce the computation complexity, while maintaining a relatively small RMSE.

Figure 3 also shows the importance of AGC function in a digitized correlation system. In order to maintain $V_{\text{ADC}}/\sigma_{x,y}$ at the optimum value, $\sigma_{x,y}$ has to be constant (since V_{ADC} , as the comparator threshold, cannot be changed). Therefore, AGC is usually required in microwave radiometer systems and the gain control accuracy becomes a challenge when designing such systems.

2.1.2 AGC Loop Design Challenge

AGC circuits are employed in many systems where the amplitude of an incoming signal can vary over a wide dynamic range. The role of the AGC circuit is to provide relatively constant output amplitude so that the system requirements can be relaxed for the following stages. If the signal level changes are much slower than the information rate contained in the signal, an AGC circuit can be used to provide a signal with a well-defined average level to the downstream circuits. In most applications, the time to adjust the gain in response to an input amplitude change should remain constant, independent of the input amplitude level and hence gain settling of the amplifier.

A schematic diagram of a common AGC system is shown in Figure 4. It consists of a VGA (variable gain amplifier), a detector, a low-pass loop filter, and a differential amplifier. The detector detects the power level of the output signal, and feeds that into an integrator. Then the signal is compared with a reference value, and the difference is amplified by a factor of A . The resulting voltage is then used to control the VGA in order to form a negative feedback.

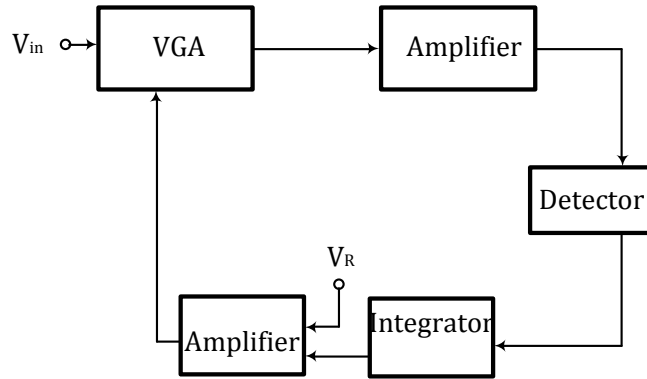


Figure 4 Schematic diagram of a common AGC system

The use of AGC in radiometer system presents a different problem as compared to the more conventional use of AGC. Normally the input (V_{in}) to AGC is a narrow band sinusoidal signal. However in the system of interest, V_{in} is a wide-band Gaussian random process with a bandwidth from 10MHz to 500MHz. The random noisy nature presented at the input of the system will cause a random noisy nature in the gain variation even after the system settles. Therefore, one of the design challenges is to maintain a small gain variation after the loop settles. It has been proven in [6] that the gain standard deviation is proportional to the quiescent DC gain of the forward loop amplifier. Their ratio is a function of the input power and the AGC loop parameters. The relationship is shown in the following equation:

$$\frac{\sigma_{K_0}}{K_0^2} \propto \left(\frac{m\bar{A}\bar{R}}{1+m\bar{A}\bar{R}} \right) \frac{T_f}{T_{ie}} \quad \text{where}$$

σ_{K_0} = standard deviation of AGC gain after the loop settles.

K_0 = quiescent amplifier gain corresponding to the quiescent gain bias.

m = a constant,

A = feedback amplifier DC gain,

\bar{R} = input power level,

T_f = VGA time constant,

T_{ie} = integrator time constant,

In this design, T_f is required to be 500MHz as per system specifications. The feedback amplifier DC gain is chosen to be at least 30 to achieve a small control error. As a result, in order to achieve small gain variation upon settling, the AGC feedback loop should have a very low cutoff frequency. This presents the challenge of achieving a very low cutoff frequency given the limited area ($240\mu\text{m} \times 850\mu\text{m}$).

2.1.3 Existing Solutions for AGC Loop for Radiometer

Many AGC solutions have been proposed over the years [7][8][9]. Figure 5 shows a commonly used AGC circuit for communication systems. It is composed of a VGA, a power detector (PD), a comparator and a loop filter. The output signal of the VGA is detected by the PD, amplified by the error amplifier, and then compared with a reference voltage (V_{ref}) to generate a control voltage (V_c). This voltage adjusts the VGA gain and keeps the output power at a constant level [7].

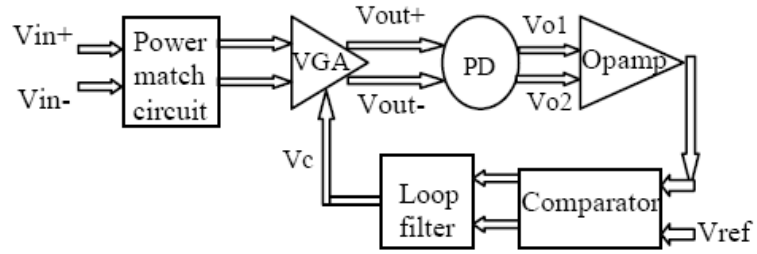


Figure 5 Classic AGC loop diagram [7]

However, the AGC loop presented in [7] is based on the control of output signal power. For the application of GNSS systems and GeoSTAR systems, AGC loops based on the control of digitized output duty cycle would be more appropriate. A commonly used duty cycle controlled AGC loop is shown in Figure 6 [8]. It is composed of a VGA, a 2-bit ADC, a charge pump and an off-chip capacitor. The ADC produces 2 bits: the sign bit (SIGN) and the magnitude bit (MAG). The charge pump driven by MAG, injects a current I_{UP} or I_{DOWN} into an off-chip capacitor to generate the control voltage of the VGA. By setting an appropriate ratio of I_{UP} to I_{DOWN} , the 1's and 0's ratio of MAG can be adjusted. Therefore, the normalized ADC reference range $V_{ADC}/\sigma_{x,y}$ can be adjusted accordingly.

However, the downsides of this design are that it requires a bulky off-chip capacitor and that the accuracy of $V_{ADC}/\sigma_{x,y}$ is limited by the mismatch between I_{UP} and I_{DOWN} . If the designer wants to use on-chip capacitors for the charge pump loading instead of off-chip, the area limits the value of such capacitors. As a result, I_{UP} and I_{DOWN} must be very small to maintain the same feedback loop cutoff frequency. This in turn degrades the matching

between I_{UP} and I_{DOWN} , resulting in very low accuracy when controlling the magnitude bit duty cycle.

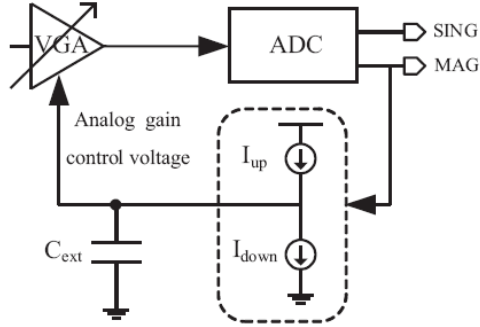


Figure 6 AGC in GNSS receivers based on charge pump [8]

In order to eliminate the use of off-chip capacitors, a digitally controlled AGC loop was introduced in [9]. As shown in Figure 7, it consists of a PGA (programmable gain amplifier), and a digital gain control unit. The magnitude bit is sent to a digital power detector to estimate the signal power at the input of ADC. The detected power P_{cal} is then compared to P_{ref} (the control word of the reference power level). The difference between the calculated power and the reference power is accumulated in an integrator. The output of the integrator is then decoded by a decoder to generate the gain control bits for the PGA. By adjusting P_{ref} to optimal value, $V_{ADC}/\sigma_{x,y}$ can be adjusted to generate minimum correlation error.

The disadvantage in such an AGC structure is that increasing the number of digital gain control bits will increase the design complexity and area. A limited number of bits results

in low resolution for the PGA gain control. Therefore, the benefit of adding the AGC loop will not be maximized.

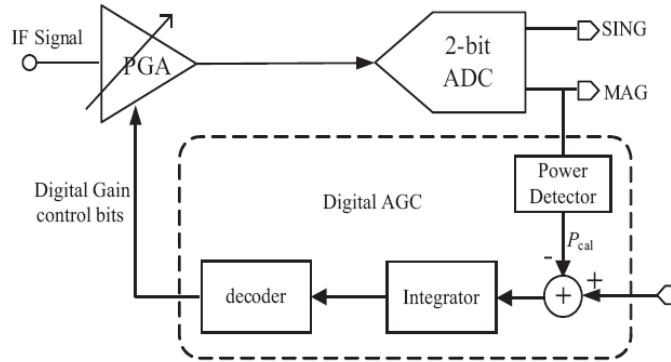


Figure 7 Digitally controlled AGC loop [9]

An innovative duty cycle controlled AGC loop addressing the design tradeoffs of existing designs will be presented in Chapter 3.

2.2 High-Speed Data Transmission Design Challenge

Figure 8 shows the major components of a typical high-speed electrical link system. A high-bandwidth transmitter serializes parallel input data for transmission. Differential low-swing signaling is commonly used for common mode noise rejection. At the receiver, the incoming signal is sampled, regenerated to CMOS values and deserialized. This work focuses on the design and simulation of the very first stage of the data link systems, the serializer. In this design, current-mode logic (CML) latches and multiplexers are adopted to construct the serializer. CML circuits have been extensively used in high speed applications [13]. In many cases, CML circuits can operate with lower signal voltages at

higher operating frequencies than static CMOS circuits [13]. However, CML circuits suffer from static power dissipation. Therefore, the major challenge when designing the serializer is to design an optimal structure given the high serializing factor and to achieve low-power operation at 32Gbps.

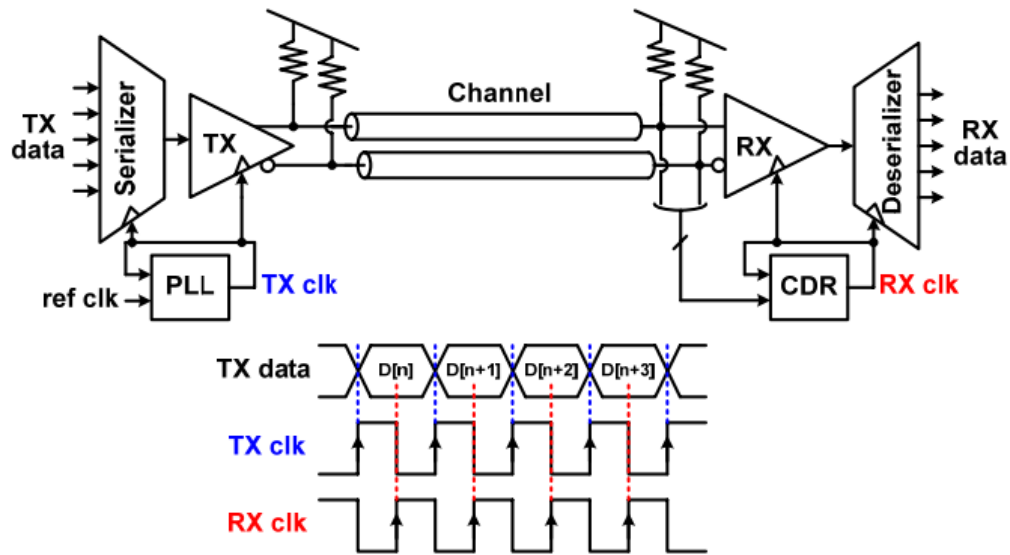


Figure 8 High-speed electrical link systems [14]

CHAPTER 3

Proposed Approach

3.1 45nm CMOS SOI Technology

Silicon on Insulator (SOI) technology refers to the use of a layered silicon-insulator-silicon substrate instead of conventional silicon substrates in semiconductor manufacturing. The main difference between bulk and SOI transistors is that bulk MOSFETs are built at the top of the surface of a monocrystalline silicon wafer, whereas in SOI, the top active silicon region is separated from the underlying mechanical substrate by a thick insulator layer called buried oxide. The SOI mechanical substrate may be high resistivity or low resistivity. This gives SOI technology great advantages, which include: lower parasitic capacitances, no latch-up effect, short channel effect reduction, inverse sub-threshold slope, integration density and power consumption, high resistivity substrate compatibility which reduces substrate coupling, high quality factor inductances, higher density metal to metal capacitors, and low attenuation constant transmission line at RF frequencies [15]. A device cross-section illustration of standard CMOS and SOI CMOS is shown in Figure 9. The layout of floating body transistors and body contacted transistors are shown in Figure 10.

However, in analog design where history effect is important, body contacted (BC) transistors are often used. By using a body contact, the BC MOSFET does not suffer from the kink effect. Thus, the DC characteristics of the device are exactly the same as

the bulk device. However this also adds additional capacitance created by the contact, as shown in Figure 11.

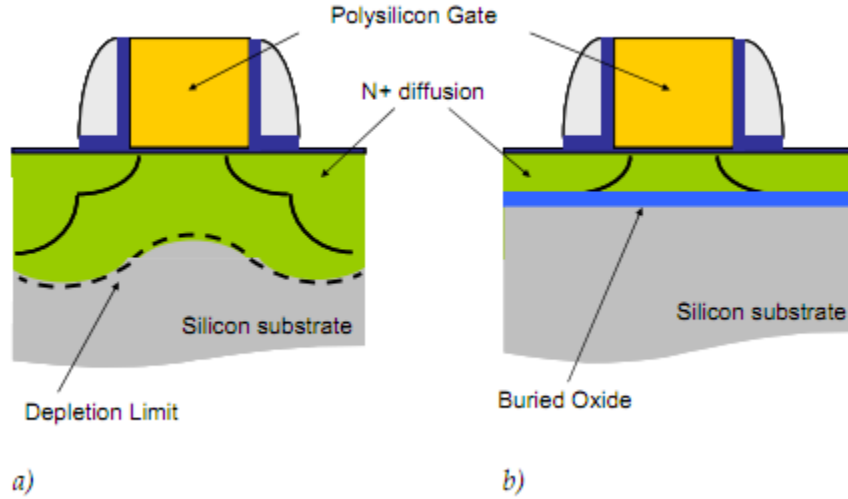


Figure 9 Standard CMOS cross-section vs. SOI CMOS [15]

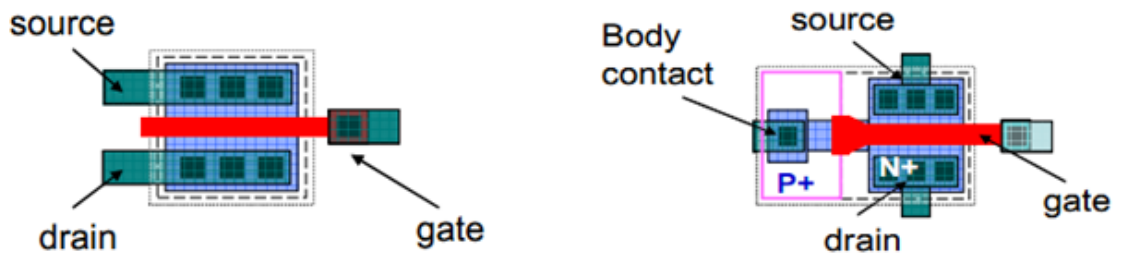


Figure 10 Floating body transistor vs. body contacted transistor layout [15]

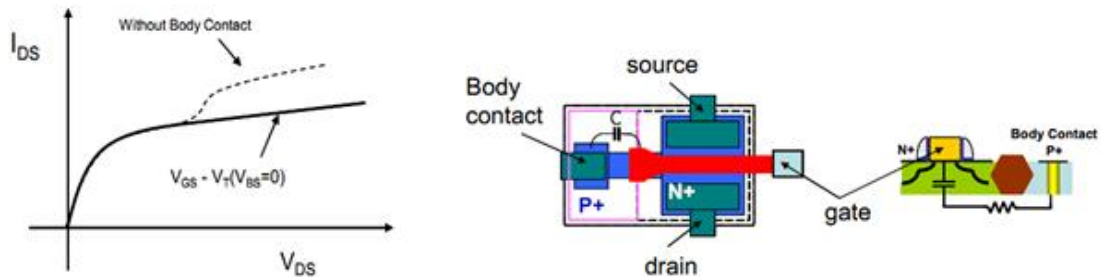


Figure 11 Parasitics of body contacted transistors in SOI technology [15]

3.2 Overview of the Proposed System on Chip

The proposed system has 16 base-band signal processing blocks and a 32:1 serializer, as shown in Figure 12. Each base-band block includes a VGA, a 2-bit ADC, a duty cycle control function and a Gm-C charge pump, all together forming an AGC loop.

16 input signals are first amplified by the VGAs. Each amplified signal is maintained at a constant power level with the help of the AGC loop. Each signal is then digitized by a 2-bit ADC forming a sign bit and a magnitude bit. Finally the 32:1 serializer serializes the 32 low-speed digital signals to 1 high-speed signal.

The proposed SoC has the capability of handling 16 parallel input IF signals. The bandwidth of these signals is from 10MHz to 500MHz, and the power can vary from -20 dBm to -10 dBm. The AGC loop maintains the VGA output signal power constant so that $V_{ADC}/\sigma_{x,y}$ always equals to 0.9, regardless of the input signal power. The 2-bit ADC samples the signal at 1Gsps which is right above the Nyquist rate. The 32:1 serializer has one 32Gbps output. It is clocked at 16 GHz and operates in half-rate mode. The 16GHz reference clock is generated by an on chip PLL. All signals are in differential mode.

The chip is designed using 45nm SOI technology with flip chip output connections to the package. The area of the proposed system is $240\mu\text{m} \times 825\mu\text{m}$.

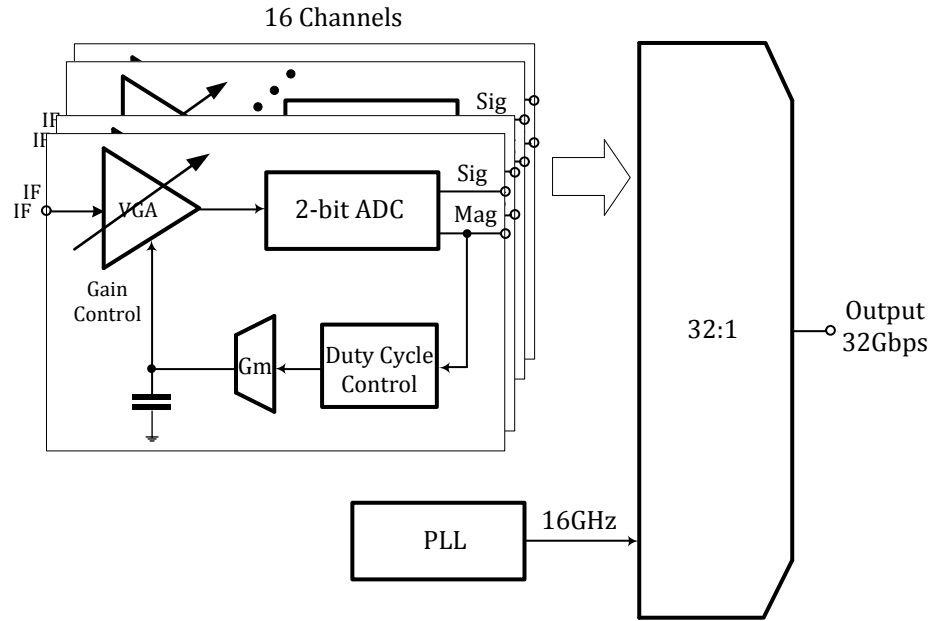


Figure 12 Proposed system diagram

3.3 Innovation and Significance of Technology

As discussed in section 2.1, a high precision duty cycle controlled AGC loop is strongly desired for this application. However, current designs do not offer a compact solution. Traditional structures use transistor width ratio to control the output duty cycle (as shown in Figure 6). A large current is required to ensure a good matching. As a result, the AGC consumes more power and requires a large off-chip capacitor to maintain a low cutoff frequency. In order to solve these problems, a novel duty cycle controlled AGC is proposed. The diagram is shown in Figure 13, where the duty cycle is controlled by the resistance ratio (R_1/R_2). Therefore, it can achieve high accuracy with no off-chip components.

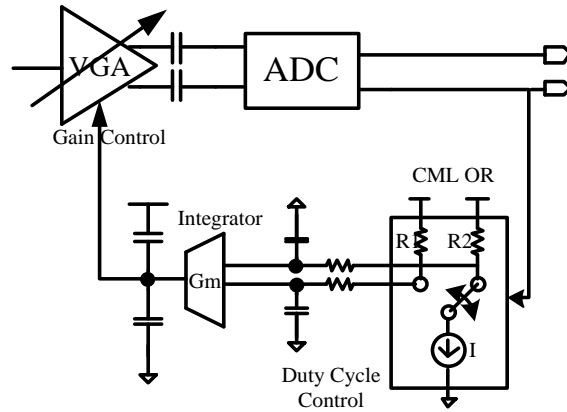


Figure 13 AGC loop with proposed duty cycle control block

In addition, the proposed design is intended to achieve state of the art low-power operation and high-speed data transmission by using CML latches and multiplexers.

3.4 Potential Applications

The low power ADC arrays with a serial output can be used in radiometer and interferometer instruments such as GeoSTAR. The unique properties of the proposed ADC array make it ideal for applications that require parallel digitization and power efficiency at high quantization rate. In addition to the GeoSTAR application, 32:1 serializers with 32Gbps outputs are essential building blocks of next generation high-speed data link systems, especially for fiber optics communication purposes.

CHAPTER 4

AGC Loop Design and Simulation

4.1 VGA Design and Simulation

Consider a multistage amplifier with a DC gain A_A and a -3dB bandwidth ω_A . Assume that it is formed by the cascade of n identical stages, each with a single pole response,

$$A_s(j\omega) = \frac{A_0}{1 + j\frac{\omega}{\omega_B}}$$

Assuming that there is no interaction among the stages, the overall transfer function of the multistage amplifier is

$$A_A(j\omega) = \left(\frac{A_0}{1 + j\frac{\omega}{\omega_B}} \right)^n,$$

The -3dB frequency of the multistage amplifier ω_A resulting from

$$|A_A(j\omega)| = \frac{A_A}{\sqrt{2}} = \frac{A_0^n}{\sqrt{2}}, \text{ is}$$

$$\omega_A = \omega_B \sqrt{2^{\frac{1}{n}} - 1}$$

The above relation shows that the bandwidth of the multistage amplifier ω_A will be less than the bandwidth of the individual stage ω_B . As has been proven, for a targeted VGA chain with certain gain and bandwidth, the required gain for each stage decreases if more stages are used, but the required bandwidth decreases if less stages are used [16].

However, the required gain-bandwidth product reaches minimum when the number of stages is 4. Although it has also been shown that with noise taken into consideration, a two-stage VGA has the most advantages [16].

Typical requirements for VGAs include bandwidth, tunable gain range and noise. In this design, VGA input signal bandwidth is from 10MHz to 500MHz. Voltage gain tunable range of at least 30dB is needed in order to cope with input power from -20dBm to 10dBm. The noise figure is not of great concern in this application because the output signals will be cross-correlated. A 3-stage VGA is adopted in this work.

The half circuit of a single stage VGA is shown in Figure 14. It uses a NMOS differential pair with resistor load R_1 . Source degenerating resistor R_2 tunes the gain. Thick oxide PFET with body-contact transistors are used to implement this tunable resistor. Small signal analysis of the voltage gain is shown in the following assuming both M1 and M2 are in saturation.

$$A = \frac{V_{out}}{V_{in}} = \frac{-R_1}{\frac{1}{g_{m1}} + (R_2 // r_{o1})}$$

When R_2 is large,

$$A = \frac{-R_1}{R_2 // r_{o1}};$$

When R_2 is small,

$$A = \frac{-R_1}{\frac{1}{g_m}} = -g_m R_1 = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{SS}} \cdot R_1$$

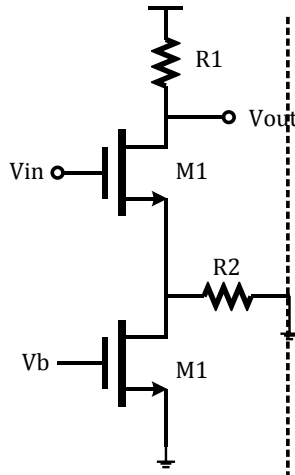


Figure 14 Half circuit of VGA

When it comes to the choice of transistors, both “avt” (analog transistors) and “tonfet” (thick-oxide transistors) with body contact are considered. Floating body transistors are not suitable for analog circuits because of the history effect. Simulation shows that there are no significant differences between the two transistors in terms of output impedance in the saturation region. The f_t of “avt” and “tonfet” are also of no significant differences. Both values are approximately 180GHz. From the design tradeoff point of view, “tonfet” takes up much more space than “avt”, but “tonfet” has higher V_{th} than “avt”. High V_{th} transistors are usually preferred in analog circuits because voltage variation will have less effect on the saturation current. Given the facts above, the conclusions that “tonfet” are preferred when area allows can be drawn.

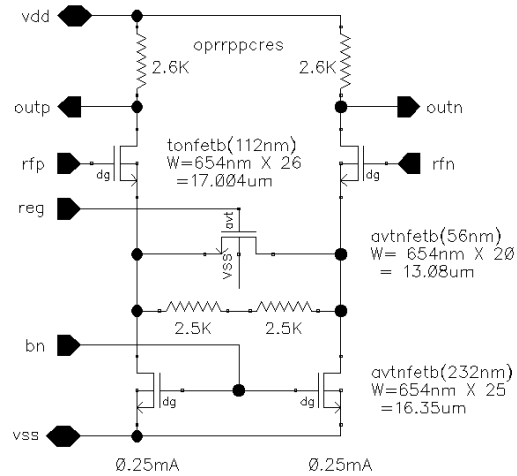


Figure 16 Circuit schematic of the second stage VGA

The 3-stage VGA chain is laid out. The VGA differential pair is interdigitated to ensure a good matching. The layout is shown in Figure 17.

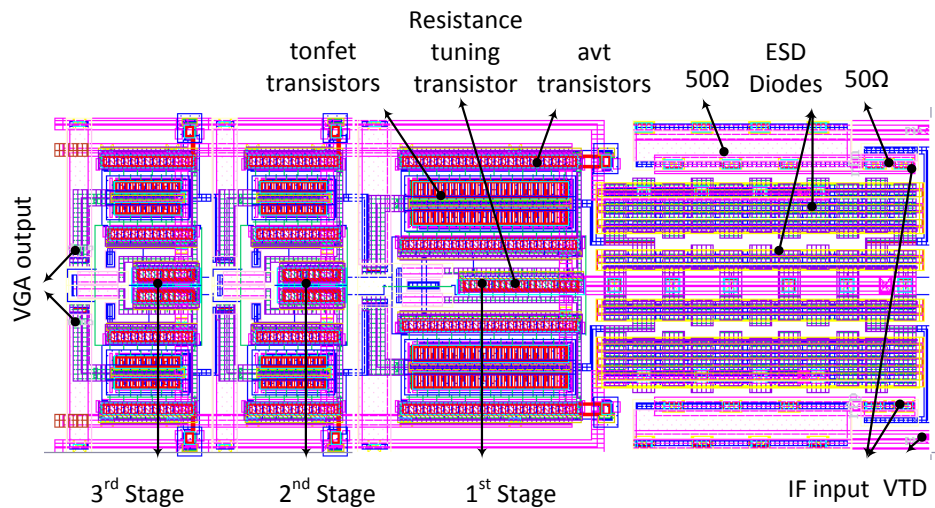


Figure 17 3-stage VGA chain layout

The post layout simulations were performed. Shown in Figure 18 is the AC response of the VGA chain at different corners. Figure 19 shows the mid-band VGA gain (at

100MHz) as a function of the VGA tuning voltage. It shows that the VGA gain has the best linearity when V_{reg} is in the range of 0.45V ~ 0.65V. The effective range is from 0.3V to 1V.

Three conditions are simulated corresponding to typical, slow and fast corners. Sigma corresponds to the process variation. Sigma=3 represents the fast corner, and sigma=-3 represents the slow corner. The design temperature range is from -25 °C to 75 °C. A 5% vdd variation is accounted, which means vdd varies from 0.95V to 1.05V.

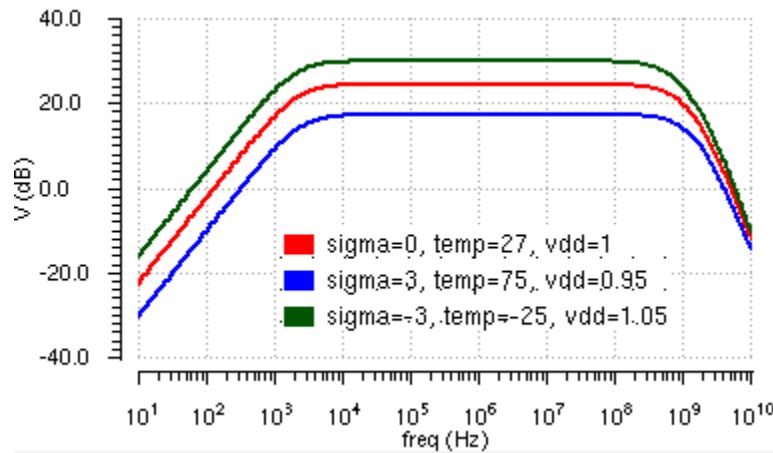


Figure 18 VGA chain AC response at different corners ($V_{reg} = 0.65$)

Noise is not of a concern in this application, with the reason being as follows. The outputs of VGAs will be cross-correlated between channels; therefore, uncorrelated noise does not contribute in the final results. It is reasonable to assume noise between each channels is uncorrelated; thus, the noise introduced in the VGA is not of a concern.

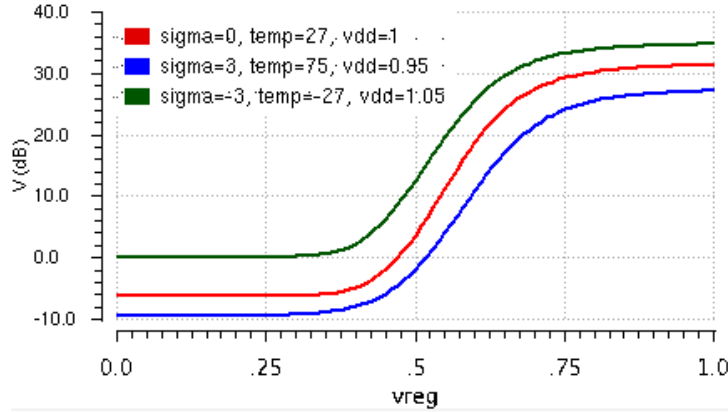


Figure 19 VGA mid-band gain as a function of the tuning voltage V_{reg}

4.2 2-bit ADC

As mentioned in Section 2.1.1, a 3-level digitizer results in the best trade off in terms of cost and performance. Too many bits will increase the calculation complexity for the correlator in the following stage. Any fewer bits would decrease the accuracy of the radiometer. Therefore, a 3-level digitizer is used in the project. 2-bit ADC generates a sign bit and a magnitude bit. The sign bit indicates the sign of the input signal, whether the differential input signal is above or below zero. The magnitude bit indicates the magnitude of the digitized signal, whether the differential input is within the range of positive and negative threshold or otherwise. Three comparators are needed to generate the initial results. Then an OR function is needed to generate the magnitude bit. The comparison threshold is generated using resistor DACs (digital to analog convertor) with large dimensions and large resistances for matching purposes and for achieving low static current consumption. Switched capacitors are used to perform the voltage addition and subtraction between the input signals and the reference threshold voltages. The switched

capacitor structure also serves as the sample and hold circuit. A dynamic Lewis-Gray comparator is adopted to perform the comparison at a clock rate of 1GHz.

4.2.1 Switched Capacitor

The switched capacitor topology is shown in Figure 20. Switches are controlled by two non-overlapping clock signals, *clkd* and *clkr*. When *clkd* is high and *clkr* is low, the voltage at node *q* equals to V_{cm} (the common mode voltage intended for the comparator), and the voltage at node *i* equals to V_{in} . When *clkd* is low and *clkr* is high, node *q* is floating and the voltage at node *i* equals to the reference voltage *ref*. Therefore the voltage at node *q* at the end of the operation is $V_{cm} + V_{in} - ref$. Switches are implemented by transmission gate using both PMOS and NMOS transistors. The circuit schematic is shown in Figure 21.

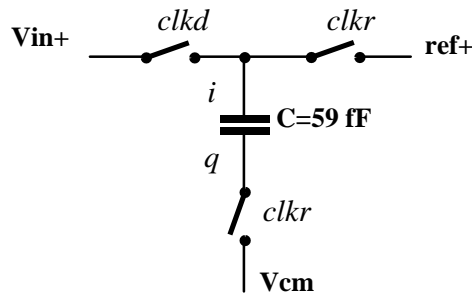


Figure 20 Switched capacitor structure

The switched capacitor operation can be summarized by the following expressions:

$$\text{node } i = \begin{cases} V_{in} + , & clkd = 1 \\ ref + , & clkd = 0 \end{cases} ,$$

$$\text{node } q = \begin{cases} V_{cm}, & \text{clk}r = 1 \\ V_{cm} + v_{in} - \text{ref}, & \text{clk}r = 0 \end{cases}$$

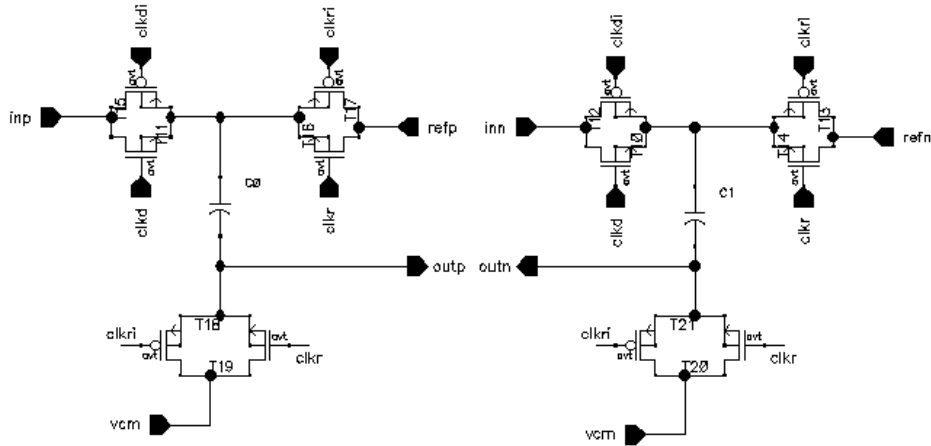


Figure 21 Circuit schematic for the switched capacitors

4.2.2 Comparator

The comparator is a Lewis-Gray dynamic comparator. When clock is low, $V_{out}^+ = V_{out}^- = V_{dd}$; when clock rises, it samples the input signal at the clock rising edge and regenerates a differential voltage at the output to a logic level. The circuit schematic is shown in Figure 22. As a result of the switched capacitor structure, the comparator compares the input differential voltage to $\text{ref}^+ - \text{ref}^-$. The inputs of the comparator are at the gate of T5 and T0.

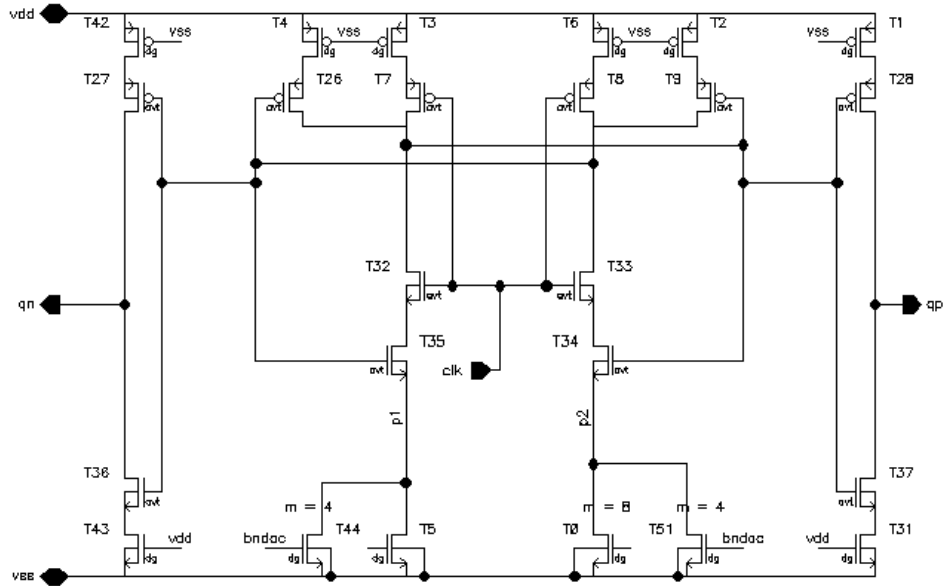


Figure 22 Dynamic comparator circuit schematic

4.2.3 Layout and Simulation Results

The 2-bit ADC is laid out. The layout is shown in Figure 23. The post layout simulation was performed.

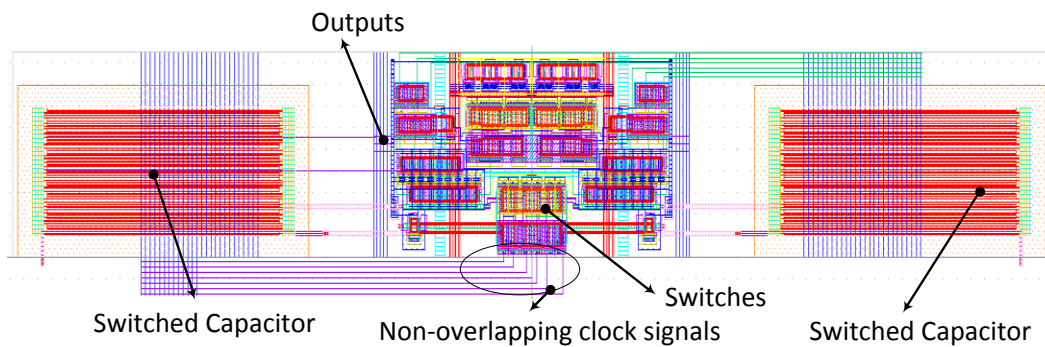


Figure 23 2-bit ADC layout

The post layout 2-bit ADC was simulated and investigated in terms of its dynamic performance. Spurious free dynamic range (SFDR) is the ratio of the rms value of the signal to the rms value of the worst spurious signal, regardless of where it falls in the frequency spectrum. The worst spur may or may not be a harmonic of the original signal. SFDR is an important specification in communication systems because it represents the smallest value of signal that can be distinguished from a large interfering signal (blocker). SFDR can be specified with respect to the actual signal amplitude. To test the dynamic performance of this ADC, the output is restored using an ideal DAC, and the Spurious Dynamic Range was calculated, the SFDR was simulated as well.

$$SDR = 20 \cdot \log \left(\frac{RMS(V_{VGA})}{RMS(V_{VGA} - V_{Restored})} \right), \text{ where}$$

V_{VGA} is the VGA output after threshold control loop settles;

$V_{Restored}$ is the waveform restored from ADC digital output.

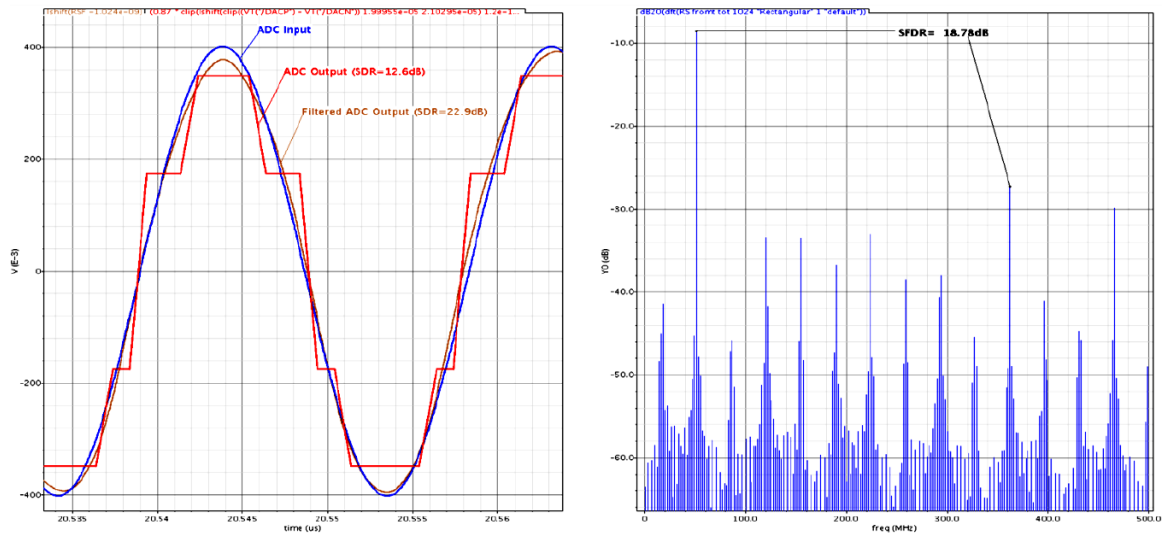


Figure 24 Post layout ADC simulation results

The input signal and the restored signal along with FFT based SFDR simulation results are shown in Figure 24. Simulated SFDR is 12.6 dB.

4.3 Duty Cycle Control

The Gaussian distributed signals from the output of VGAs will be digitized with respect to $\pm 0.9 \sigma$, in order to generate the magnitude bit. The duty cycle control block will compare the duty cycle of the magnitude bit with 36.812% and amplify that difference to a differential output V_c^+ and V_c^- . Resistors R1 and R2 are designed with a certain ratio so that the differential output is zero when current duty cycle for the non-inverting branch current is 36.812%. The common mode output was chosen to be 700 mV by manipulating the tail current value and the resistance value. This voltage was chosen in order for the integrator to achieve a high gain. The diagram of the duty cycle comparison block is shown in Figure 25 and Figure 26. The calculation for the resistance values is shown below:

$$i = \frac{1}{R1 + R2}(VDD - Vc - IR1);$$

the integration of current i over a period of Δt is :

$$\int_0^{\Delta t} i dt = \int_0^{\Delta t} \frac{1}{R1 + R2}(VDD - Vc - IR1);$$

during steady states, $\int_0^{\Delta t} i dt = 0$; therefore, $Vc = VDD - R1 \cdot Irms$.

In order to have $V_c = 0$ at 36.812% duty cycle, the resistance needs to satisfy the following:

$$\frac{R1}{R2} = \frac{I_2 rms}{I_1 rms} = \frac{36.812\%}{63.188\%}$$

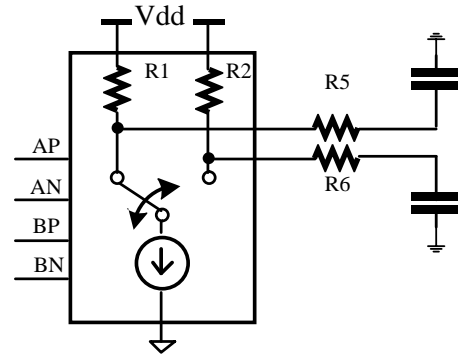
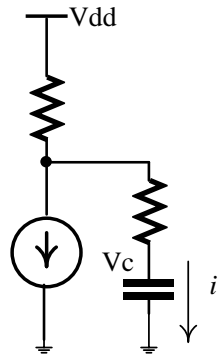


Figure 25 RC charge pump model Figure 26 Duty cycle control block model

This conversion mechanism has the advantage of differential operation. Two alternative solutions were considered: (1) use single ended output (either V_c^+ or V_c^-) and a reference voltage generated from the DAC as the differential input for the integrator; (2) use differential output (both V_c^+ and V_c^-) and differential reference voltage as the inputs for the integrator. In this case, the integrator will have a differential difference OTA structure. These two solutions have short comings of their own. For solution (1), the comparison is directly dependent on the tail current value which varies significantly over process corners and supply voltage; for solution (2), the OTA differential pairs will be constantly driven by a large signal (at least 100mV), which results in a small gain and significant asymmetry.

The diagram in Figure 26 describes the OR function block with duty cycle comparison amplification (RC load not shown here). AP, AN, BP, BN are two pairs of differential

inputs. Ideally, AP should have a duty cycle of 18.406% and BP has 81.594% during steady state. This block will perform an OR function first, then compare the duty cycle with 36.812%, and convert the difference to a differential voltage V_c^+ and V_c^- . The conversion gain can be derived as follows:

$$\begin{aligned}
 V_{c_{diff}} &= V_c^+ - V_c^- \\
 &= \frac{50K\Omega}{1-36.812\%} \cdot I_{tail} \cdot (1 - 2x - 36.812\%) - \frac{50K\Omega}{36.812\%} \cdot I_{tail} (2x + 36.812\%) \\
 &= -50K\Omega \cdot I_{tail} \cdot \left(\frac{1}{1-36.812\%} + \frac{1}{36.812\%} \right) \cdot 2x\%
 \end{aligned}$$

Therefore the duty cycle conversion gain can be given by:

$$\frac{V_{c_{diff}}}{2x\%} = -50K\Omega \cdot I_{tail} \cdot \left(\frac{1}{1-36.812\%} + \frac{1}{36.812\%} \right) \quad (1) \quad ; \text{ where}$$

$V_{c_{diff}}$ is the differential output, $x\%$ is the duty cycle error comparing to the ideal value, meaning signals AP and BP both have a duty cycle of $(x+18.406)\%$.

One extra resistor R4 (as shown in Figure 27) is needed for the current tail transistor (T6) to generate equal current for both branches. From the Thevenin equivalent, it can be calculated that,

$$V_{eq} = \frac{R_1}{R_1+R_5} \cdot V_{out} + \frac{R_1}{R_1+R_5} V_{dd} ;$$

$$R_{eq} = R_1 // R_3 ;$$

In order to maintain the same current, $R1/R3$ and $R2/R6$ need to be the same, and $R4$ needs to be set to the value of $R2//R4-R1//R3$. Transistor level implementation is shown in Figure 27. Body contact transistors “avtnfetb” (232nm) are used to generate the tail current. Body floating transistors “NFET” (40nm) are used to form the logic gates. Resistor $R4$ is added to balance the two branches, in order to generate the same current. All the resistor values are shown in Table 1. The current steering leakage values are shown in Table 2.

| R1 | R2 | R5 | R6 | R4 |
|---------|---------|---------|---------|---------|
| 47.477K | 81.495K | 47.477K | 81.495K | 17.009K |

Table 1 Resistor values

| A (V) | B (V) | I_p (A) | I_n (A) | $I_{V_c^+}$ | $I_{V_c^-}$ |
|-------|-------|-----------|-----------|----------------|----------------|
| 0 | 0 | 1.171n | 9.966u | 1.840 μ A | -1.823 μ A |
| 0 | 1 | 9.966u | 0.596u | -3.142 μ A | 3.159 μ A |
| 1 | 0 | 9.966u | 1.171n | -3.142 μ A | 3.159 μ A |
| 1 | 1 | 9.966u | 0.5959u | -3.142 μ A | 3.159 μ A |

Table 2 Current steering OR leakage current

Since this block serves as a duty cycle converter, the conversion factor is of interest in order to obtain the maximum gain needed for the integrator. The simplified conversion equation was given in (1). Simulation results of the V_c vs. duty cycle characteristic is shown in Figure 28. The x -axis corresponds to the duty cycle variation while the y -axis corresponds to the differential voltage V_c^- and V_c^+ . A test bench was used to obtain V_c given different duty cycle. The schematic is not shown here for simplicity; however, the

idea is to form a feedback loop in order to perform DC simulation and to avoid the long settling time required for transient simulation.

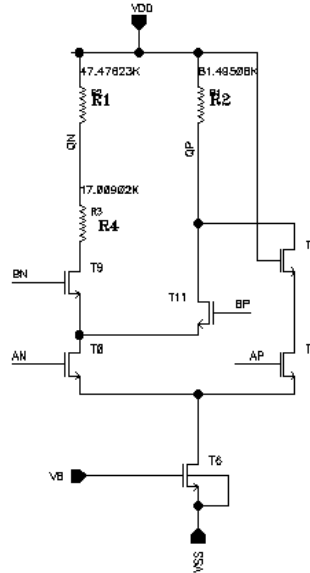


Figure 27 Current steering OR circuit schematic

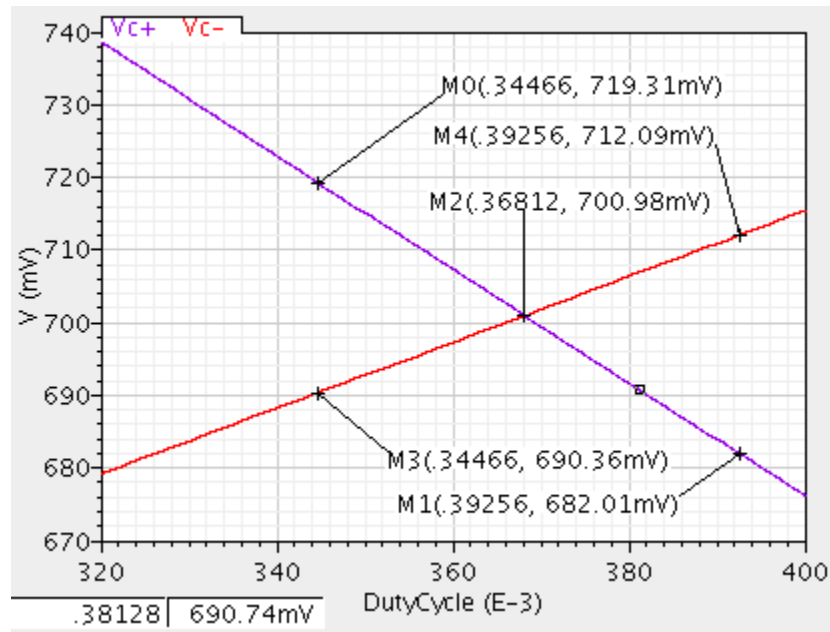


Figure 28 Duty cycle control block characteristic (differential output vs. duty cycle input)

4.4 Charge Pump (OTA)

A classic balanced OTA circuit is adopted to serve as the charge pump in the feedback loop. One of the main reasons to choose such topology is to achieve a wide output swing. Since the AGC loop requires a wide tuning range, a wide voltage swing at the VGA tuning node is highly desired.

The circuit diagram of a typical Gm-C filter is shown in Figure 29.

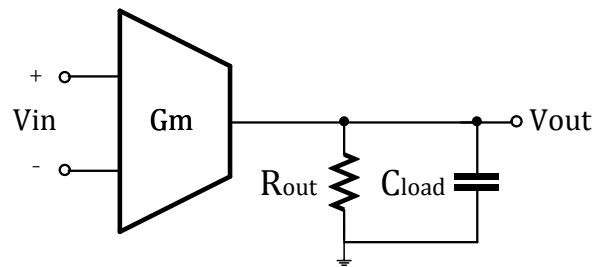


Figure 29 Gm-C loop filter diagram

The transfer function can be derived.

$$\frac{V_{out}}{V_{in}} = \frac{G_m R_{out}}{1 + j\omega R_{out} C_{load}} = \frac{1}{\frac{1}{G_m R_{out}} + j\omega \frac{C_{load}}{G_m}}$$

$$\omega_{-3dB} = \frac{1}{R_{out} C_{load}}, \quad \omega_{unity} = \frac{G_m}{C_{load}}$$

In the case when $G_m \gg R_{out}$, $A_v = G_m R_{out}$ at DC.

In this case, a low cutoff frequency is required ($f_{-3dB} = 1K$ Hz, $f_{unity} = 100K$). In order to maintain a small area, C_{load} cannot be too large. A reasonable value is 20pF.

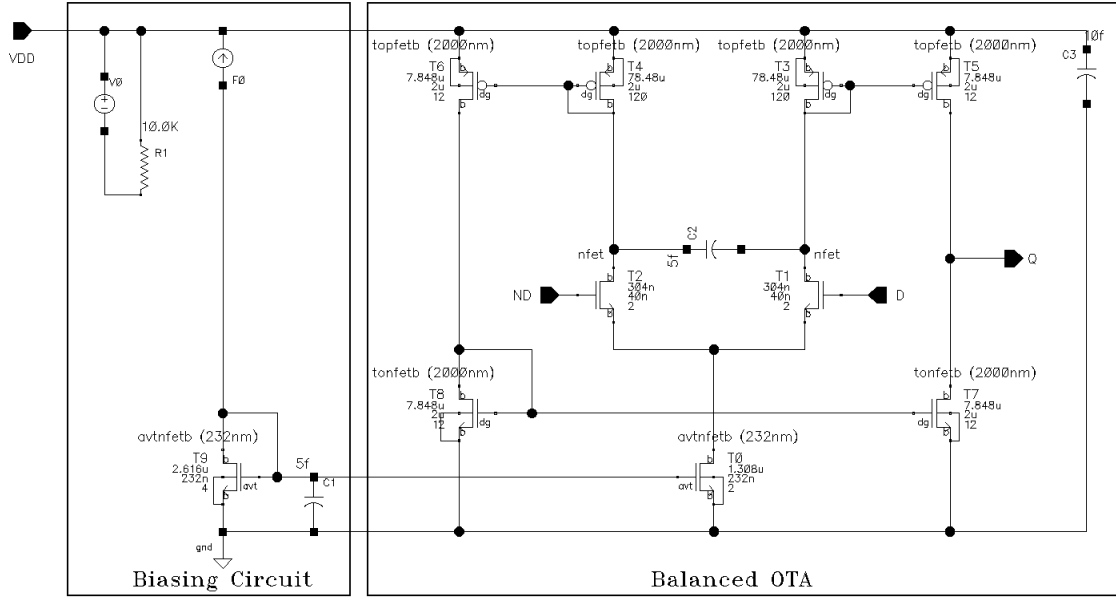


Figure 30 Balanced OTA circuit diagram

A first order DC gain analysis is as follows.

$$V_{out} = [V_{in}^+ \cdot g_{m1} \left(\frac{1}{g_{m3}} \parallel r_{o1} \parallel r_{o3} \right) \cdot g_{m5} - V_{in}^- \cdot g_{m2} \left(\frac{1}{g_{m4}} \parallel r_{o2} \parallel r_{o4} \right) \cdot g_{m6} \cdot \left(\frac{1}{g_{m8}} \parallel r_{o6} \parallel r_{o8} \right) \cdot g_{m7}] \cdot (r_{o5} \parallel r_{o7}),$$

Ignoring the short channel effect and assuming perfect matching it can be derived:

$$V_{out} = (V_{in}^+ - V_{in}^-) \cdot (g_{m1,2} \cdot \frac{1}{g_{m3,4}} \cdot g_{m5,6}) \cdot (r_{o5} \parallel r_{o7}),$$

If consider $\frac{g_{m5,7}}{g_{m3,4}} = \frac{W/L_{5,6}}{W/L_{3,4}} = \beta,$

$$\text{DC gain } Av = \frac{V_{out}}{V_{in}^+ - V_{in}^-} = g_{m1,2} \cdot \beta \cdot (r_{o5} \parallel r_{o7})$$

$$= \frac{g_{m1,2} \cdot \beta}{\lambda I_{5,7}} = \frac{g_{m1,2} \cdot \beta}{\lambda I_{3,4} \cdot \beta} = \frac{g_{m1,2}}{\lambda I_{3,4}} \quad (2)$$

This means $\beta \cdot (r_{o5} \parallel r_{o7})$ is constant. In order to achieve low 3dB frequency, $(r_{o5} \parallel r_{o7})$ should be large to reduce capacitor area. Therefore β should be small.

The device parameters at the designed operating point are as follows.

$$g_{m1,2} = 73.88 \mu S, \quad \beta = 0.1,$$

$$r_{o5} = \frac{1}{g_{ds5}} = \frac{1}{101.3nS} = 9.87M\Omega, \quad r_{o7} = \frac{1}{g_{ds7}} = \frac{1}{70.62nS} = 14.16M\Omega,$$

$$r_{o5} \parallel r_{o7} = 5.816M\Omega,$$

$$\text{Using equation (2), DC gain } Av = 73.88 \mu S \cdot 0.17 \cdot 5.8M\Omega = 72.84 = 37.25dB$$

Demonstrated in Figure 30 is the circuit schematic of the balanced OTA. T3, 4 both have 120 fingers. T5-T8 with 100, 12, 6 fingers were simulated. As predicted, DC gain remains the same but the cutoff frequency is proportional to the ratio β . In consideration of transistor matching, a ratio $\beta = \frac{1}{10}$ was chosen.

The charge pump (OTA) is then laid out. As shown in Figure 31, the differential pair is interdigitated for good matching. Capacitance load is laid out in a matrix.

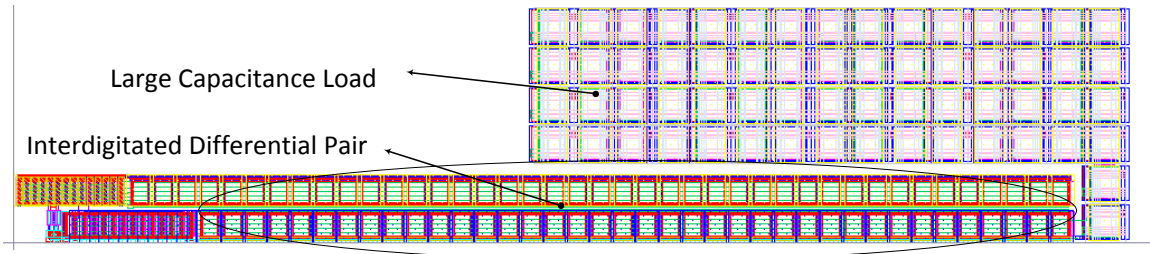


Figure 31 Charge pump (OTA) layout

Shown in Figure 32 is the DC sweeping behavior of the charge pump. As seen in Figure 32, the slope of V_{out} vs. V_{in} greatly degrades when V_{out} is above 0.8V. This means that if the VGA requires more than 0.8 V to achieve the desired V_{rms} , the duty cycle control accuracy will be greatly compromised. Considering the worst case where a -20dBm (22.5mV in 50Ω system) inputs is presented at the input and 20dB VGA voltage gain is available, a 0 dBm (225mV) output power can be achieved at the VGA output. Also taking into account of the large signal gain saturation, ADC voltage reference level is then designed to be 200mV at typical operating conditions.

AC response of the charge pump is presented in Figure 33 where it shows the -3dB cutoff frequency is lower than 2 KHz. The cutoff frequency is designed to be very small in order to obtain a smooth VGA gain variation over time, therefore not interfering with the information located at 10MHz ~500MHz. It also minimizes the gain fluctuation as modeled in section 2.1, where it showed the V_{rms} of the gain control voltage is proportional to the cutoff frequency of the feedback loop.

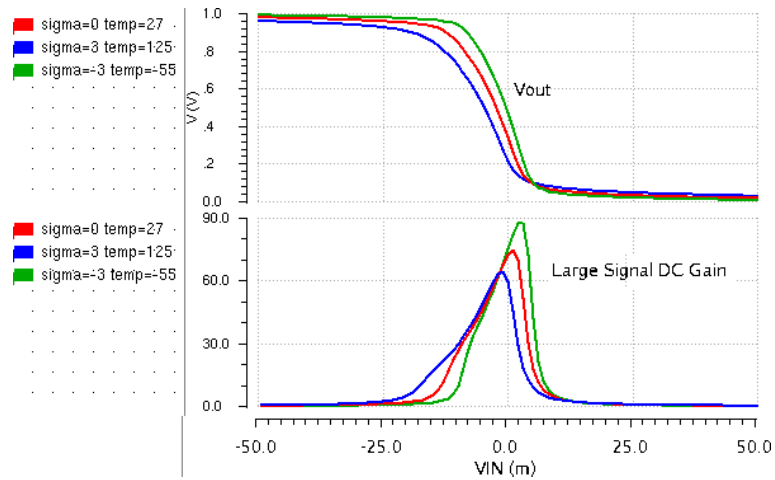


Figure 32 Charge pump DC sweeping behavior

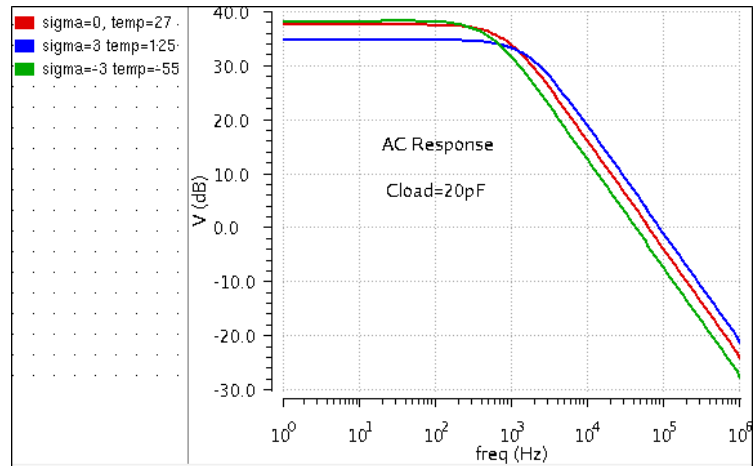


Figure 33 Charge pump small signal behavior

4.5 AGC Loop Performance

The AGC loop is to regulate the threshold voltage to the 0.9σ value, where σ is the input Gaussian random signal standard deviation. The VGA amplifies the signal with a certain tunable gain at the steady state. The comparator performs differential comparison at $\pm 200\text{mV}$. Two CML (Current Mode Logic) OR blocks will follow the comparators. One

loaded by a CML Latch generates the magnitude bit; the other one loaded by an RC integrator converts the duty cycle to differential voltage. At last, a Gm-C integrator generates the signal V_{reg} to control the VGA voltage gain. R1 and R2 shown in Figure 26 is laid out by a specific ratio so that $V_c = 0$, when magnitude bit has a duty cycle of 36.812%. This number corresponds to the probability of $x \geq |0.9 \sigma|$ following a Gaussian distribution. The comparison accuracy is set by the loop gain: duty cycle conversion gain combined with Gm-C integrator gain. Due to the fact that AGC loop contains time-variant components, the analysis for loop stability is not as straight forward as in LTI systems where phase margin can be easily simulated. Therefore, transient simulation over a long period was performed to verify its settling behavior and stability. As shown in Figure 34, differential voltage V_c settles over 150us. V_c is the differential output at the duty cycle control block. The common mode voltage of V_c is designed to be 700mV at the ideal duty cycle. As shown in the simulation results, a 2% error occurs after the loop settles. The AGC loop consumes 2.2mW of power.

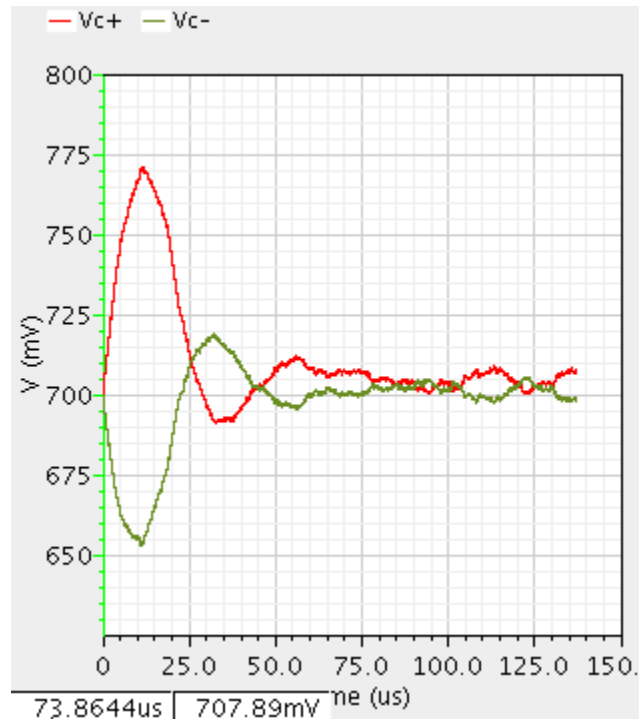


Figure 34 AGC loop transient settling behavior

CHAPTER 5

32:1 MUX Design and Simulation

Current steering latches are usually used for high-speed applications. This structure allows for a reduced voltage swing that is well defined. Reduction of the output swing increases the operating rate of the circuit. Furthermore, simulations indicate that switching of the current can be performed at a speed higher than the switching of the voltage [10]. As a result, these architectures provide the maximum operation speed for a given technology. The multiplexing at any level is performed by a combination of five latches and a multiplexer. The four latches L_1 - L_4 tend to retime the data. The fifth latch skews the data in one of the signal paths by on half of a clock period. As a result, the multiplexer samples both of the sequences starting from the middle of the data period.

As shown in Figure 35, a CML latch consists of an input tracking stage, T_{11} and T_{12} , utilized to sense and track the data variation and a cross-coupled regenerative pair, T_{13} and T_{14} , being employed to store the data [11]. The track and latch modes are determined by the clock signal inputs to a second differential pair, T_9 and T_{10} . When the signal V_{clk+} is high, the tail current I_{ss} entirely flows to the tracking circuit, thereby allowing V_{out} to track V_{in} . In the latch-mode, the signal V_{clk} goes to low, and the tracking stage is disabled. The regeneration circuit then will store the logic state at the output.

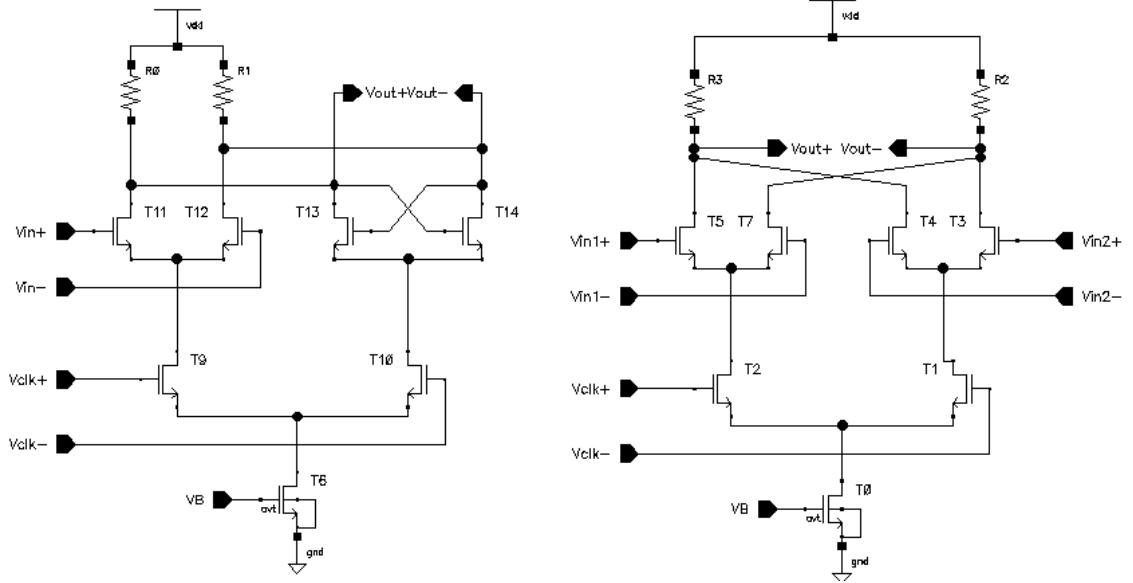


Figure 35 Current steering latch and multiplexer

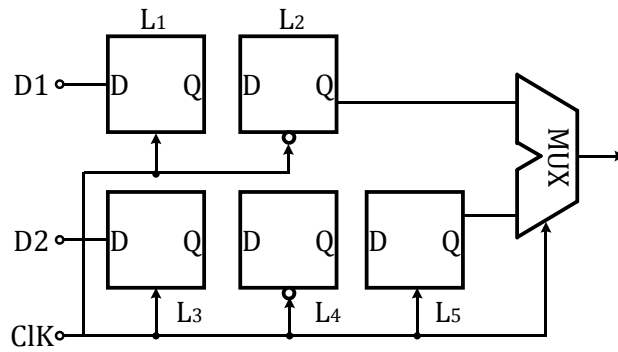


Figure 36 Two-to-one multiplexer

The output voltage swing is limited only by the tail current and the drain loading resistor.

$$V_{odm} = 2 \cdot I_{ss} \cdot R \quad \text{where,}$$

V_{odm} = output differential voltage swing maximum,

I_{ss} = tail current, R = drain loading resistance.

The design of the tail current value faces several tradeoffs. At high frequency, the parasitic capacitances of the transistors T_{11} and T_{12} degrade the required minimum gain for a proper tracking operation. Therefore, the tail current must be sufficiently high to achieve a wider range of linearity and a larger transconductance. On the other hand, an increase in the tail current means an increase in power.

Figure 36 shows a typical structure of a 2:1 mux, where the latches re-time the signals and the MUX interleaves the two channels at the output. This is the structure adopted in this work.

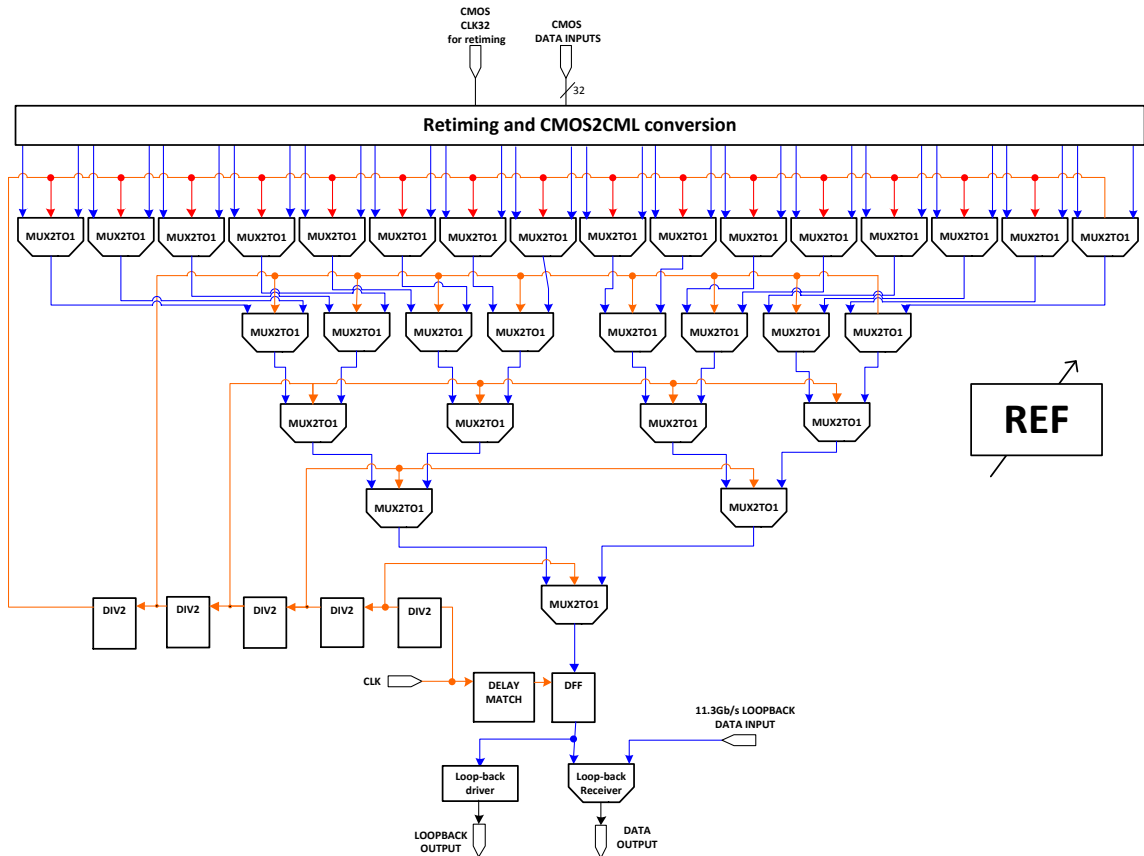


Figure 37 32:1 MUX diagram

As shown in Figure 37, the MUX consists of 5 levels of 2:1 MUXs. 16 GHz clock is provided by on-chip VCO, and four frequency dividers are used to generate the clock for each level. Five stages of inductive peaking output buffers are followed by the serializer; however, since the output buffers are not the focus of this work, the detailed design is not presented. The post layout simulated eye diagram is shown below. In this simulation, a 9 feet long coaxial cable S2P model is implemented as the transmission medium. As shown in Figure 38, the output buffer increased the eye opening at the output of the transmitter. A reasonable eye diagram is achieved at the receiving end. The serializer alone consumes 10mW of power.

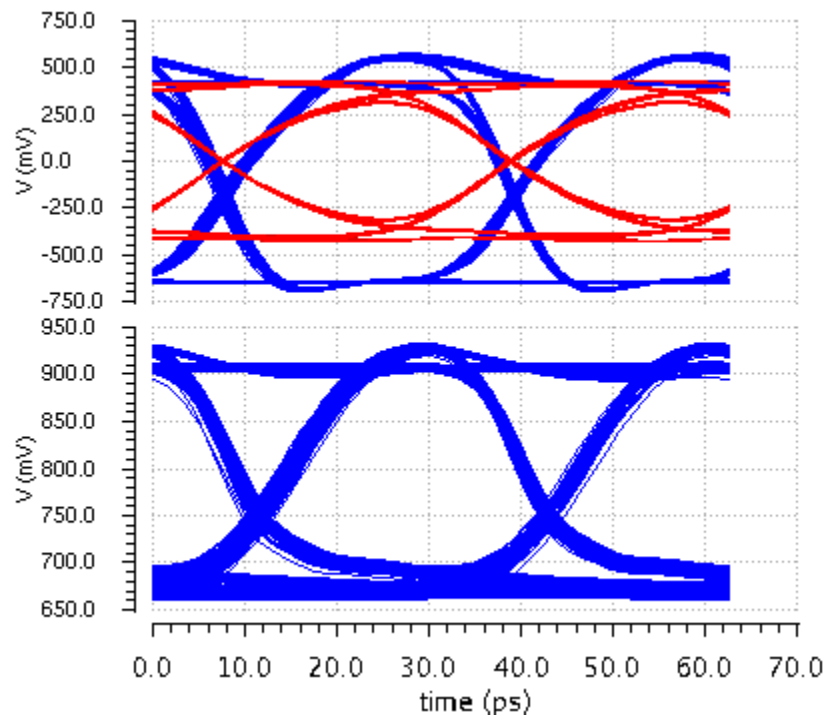


Figure 38 Transmitter eye diagram at typical corner

CHAPTER 6

Conclusion

An SoC solution for the base-band digitizing and high-speed transmission was proposed for the GeoSTAR system. It consists of an ADC array and a 32:1 serializer. The ADC array consists of 16 2-bit digitizers with duty cycle control functions. The 32:1 serializer adopts a tree architecture with 5 levels of MUXs. Each level has a serializing factor of 2.

A 3-stage VGA chain was designed achieving a bandwidth of 500MHz, a voltage gain tuning range of 35dB, and a power consumption of 1mW; a 2-bit ADC was designed achieving a SFDR of 12.6dB and a power consumption of 1mW; an AGC loop was designed achieving a duty cycle control error of 2%; a 32:1 serializer with 1Gbps input was designed achieving a single-ended eye opening of greater than 200 mV at the receiving end. The serializer alone consumes 10mW of power and the output buffer consumes 40mW of power. The area of the chip is $240\mu\text{m} \times 825\mu\text{m}$. A comparison of the designed serializer with the state of the art is shown in Table 3, where the combined power of the serializer and the output buffer is listed.

| Ref | Tech. | Rate | Supply | Power | Ser.factor |
|------|----------|----------|--------|---------|------------|
| This | 45nm SOI | 32(Gb/s) | 1 V | 50(mW) | 32:1 |
| [12] | 90nm | 40(Gb/s) | 1.2 V | 132(mW) | 4:1 |
| [13] | 65nm | 10(Gb/s) | 1V | 106(mW) | 16:1 |
| [13] | 45nm | 10(Gb/s) | 0.9V | 50(mW) | 16:1 |

Table 3 Comparison with existing MUX

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